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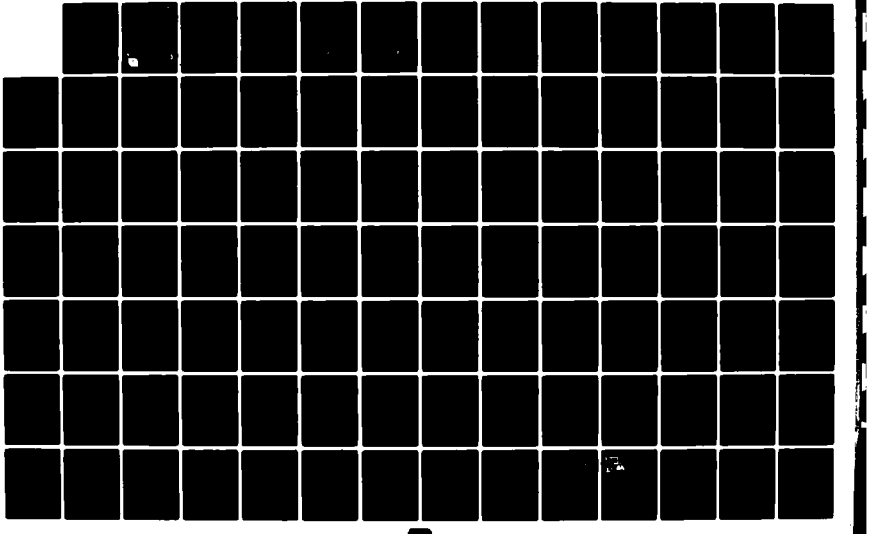

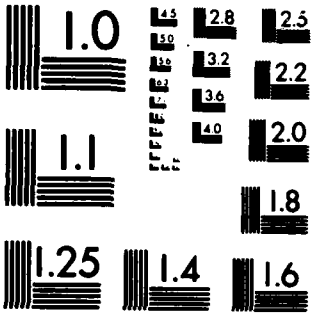

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ELECTRONIC PACKAGING AND INTERCONNECT TECHNOLOGY WORKING GROUP REPORT

(IDA/OSD R&M STUDY)

Richard J. Clark
General Electric Company
Working Group Chairman

August 1983

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INSTITUTE FOR DEFENSE ANALYSES
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This document records the activities and presents the findings of the Electronic Packaging and Interconnect Technology Working Group part of the IDA/OSD Reliability and Maintainability Study, conducted during the period from July 1982 through August 1983.

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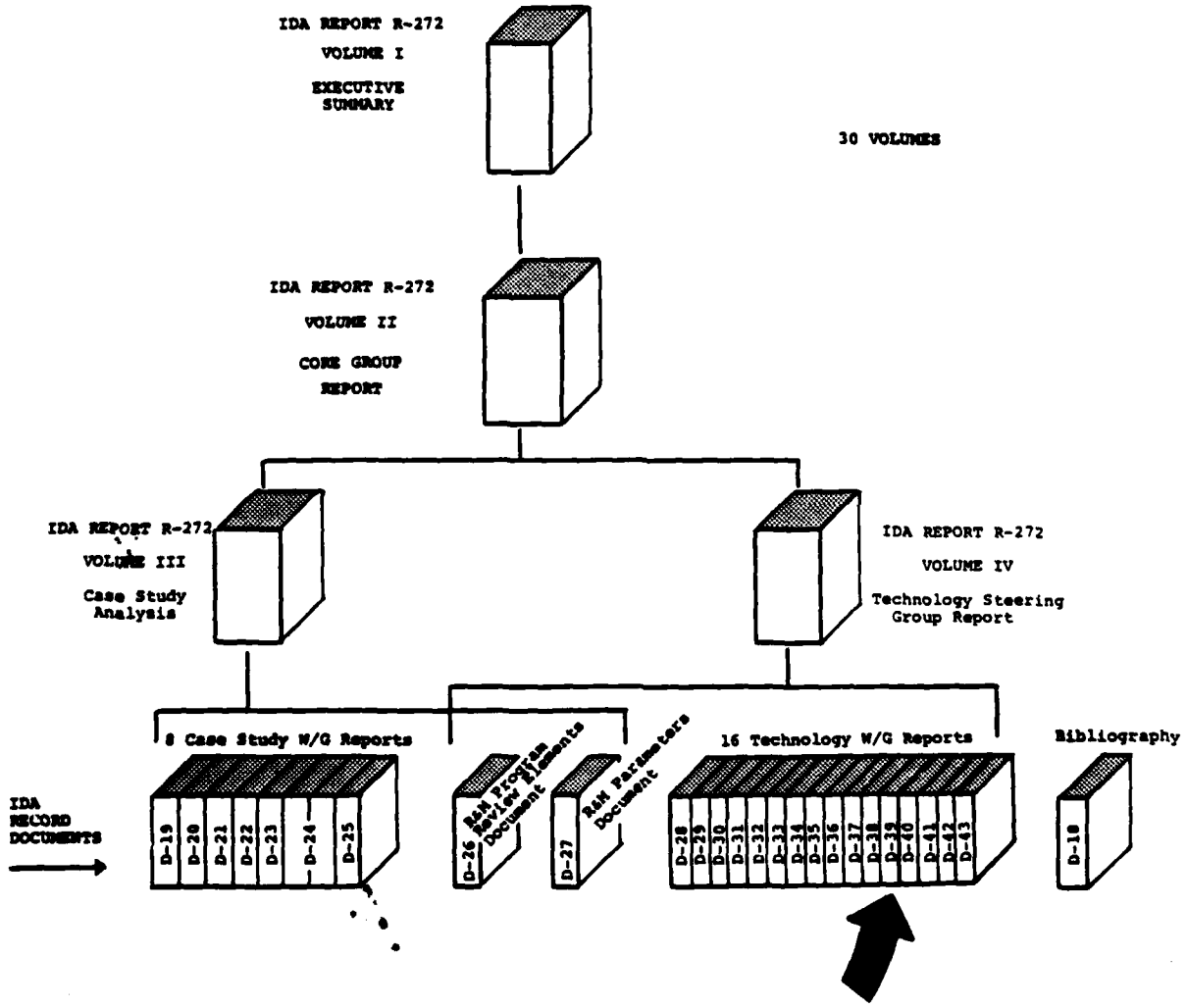
Contract MDA 903 79 C 0018
Task T-2-126

RELIABILITY AND MAINTAINABILITY STUDY

— REPORT STRUCTURE —



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PREFACE

As a result of the 1981 Defense Science Board Summer Study on Operational Readiness, Task Order T-2-126 was generated to look at potential steps toward improving the Material Readiness Posture of DoD (Short Title: R&M Study). This task order was structured to address the improvement of R&M and readiness through innovative program structuring and applications of new and advancing technology. Volume I summarizes the total study activity. Volume II integrates analysis relative to Volume III, program structuring aspects, and Volume IV, new and advancing technology aspects.

The objective of this study as defined by the task order is:

> "Identify and provide support for high payoff actions which the DoD can take to improve the military system design, development and support process so as to provide quantum improvement in R&M and readiness through innovative uses of advancing technology and program structure."

The scope of this study as defined by the task order is:

> To (1) identify high-payoff areas where the DoD could improve current system design, development program structure and system support policies, with the objective of enhancing peacetime availability of major weapons systems and the potential to make a rapid transition to high wartime activity rates, to sustain such rates and to do so with the most economical use of scarce resources possible, (2) assess the impact of advancing technology on the recommended approaches and guidelines, and (3) evaluate the potential and recommend strategies that might result in quantum increases in R&M or readiness through innovative uses of advancing technology.

The approach taken for the study was focused on producing meaningful implementable recommendations substantiated by quantitative data with implementation plans and vehicles to be provided where practical. To accomplish this, emphasis was placed upon the elucidation and integration of the expert knowledge and experience of engineers, developers, managers, testers and users involved with the complete acquisition cycle of weapons systems programs as well as upon supporting analysis. A search was conducted through major industrial companies, a director was selected and the following general plan was adopted.

General Study Plan

Vol. III	• Select, analyze and review existing successful program
Vol. IV	• Analyze and review related new and advanced technology
Vol. II	(• Analyze and integrate review results (• Develop, coordinate and refine new concepts
Vol. I	• Present new concepts to DoD with implementation plan and recommendations for application.

The approach to implementing the plan was based on an executive council core group for organization, analysis, integration and continuity; making extensive use of working groups, heavy military and industry involvement and participation, and coordination and refinement through joint industry/service analysis and review. Overall study organization is shown in Fig. P-1.

The basic technology study approach was to build a foundation for analysis and to analyze areas of technology to surface: technology available today which might be applied more broadly; technology which requires demonstration to finalize and reduce risk; and technology which requires action today to provide reliable and maintainable systems in the future. Program structuring implications were also considered. Tools used to accomplish

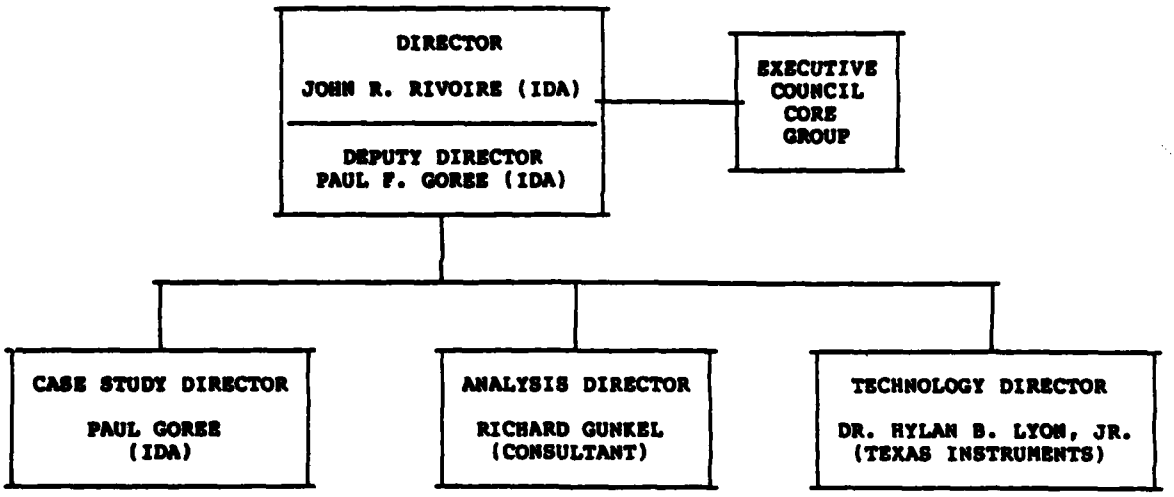

FIGURE P-1. Study Organization

this were existing documents, reports and study efforts such as the Militarily Critical Technologies List. To accomplish the technology studies, sixteen working groups were formed and the organization shown in Fig. P-2 was established.

This document records the activities and findings of the Technology Working Group for the specific technology as indicated in Fig. P-2. The views expressed within this document are those of the working group only. Publication of this document does not indicate endorsement by IDA, its staff, or its sponsoring agencies.

Without the detailed efforts, energies, patience and candidness of those intimately involved in the technologies studied, this technology study effort would not have been possible within the time and resources available.

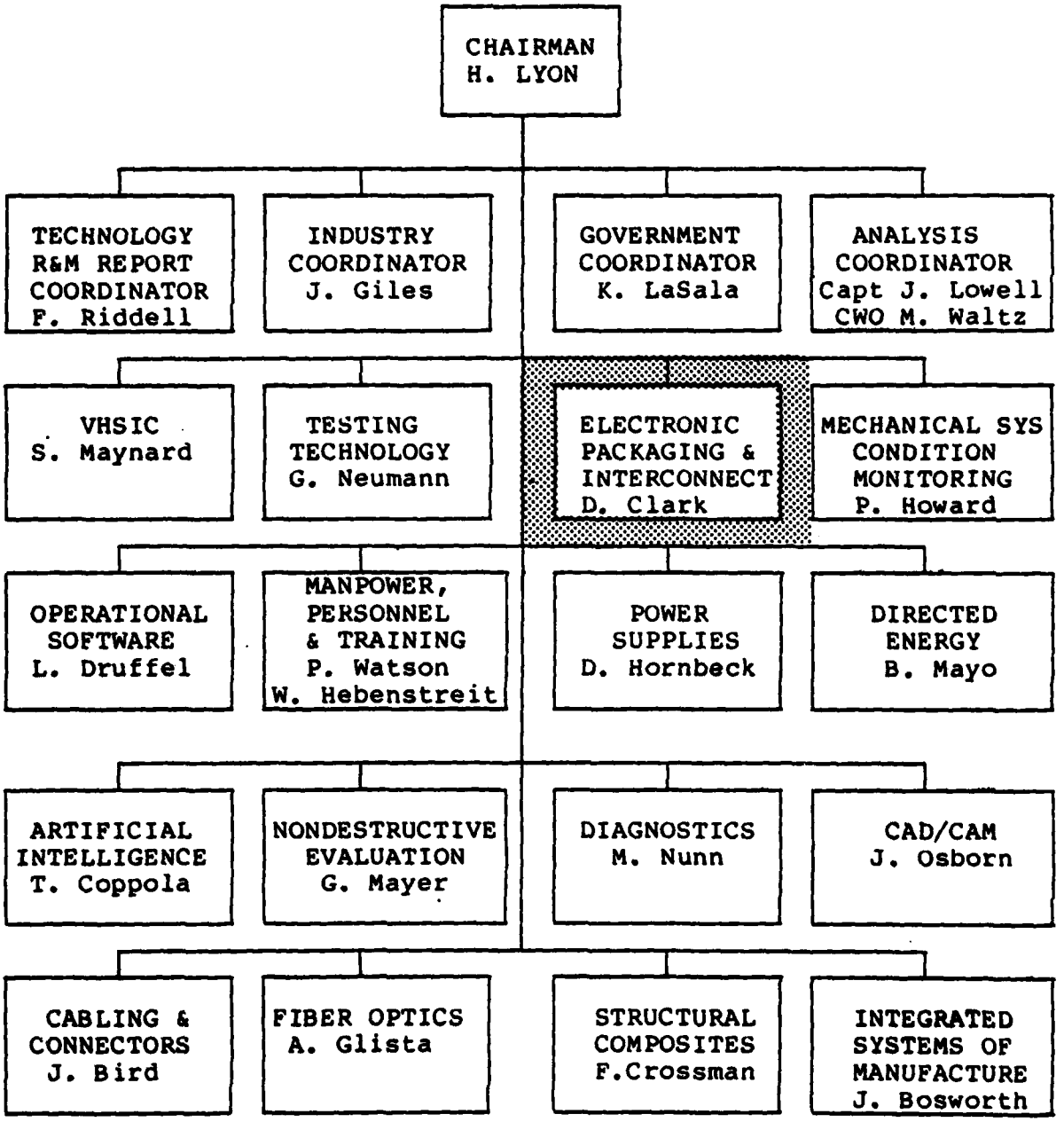

FIGURE P-2. Technology Study Organization

R&M STUDY

EPIC STUDY GROUP REPORT

ELECTRONIC PACKAGING AND INTERCONNECTION

FINAL REPORT

May 11, 1983

Study Group Members - R. J. Clark - Chairman
E. Blackburn
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I. Pratt
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M. Robbins
R. Unger
D. Zimmerman

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EXECUTIVE SUMMARY

The purpose of the Electronic Packaging and Interconnection of Components Study was to identify potential improvements in Reliability and Maintainability and Readiness tnrough the use of improved electronic packaging technology, and to recommend specific management policies and key technology development programs to accomplish the insertion of these technologies into military systems in the most effective and timely way.

Electronic Packaging for the purpose of this study is defined as the essential mechanical product design functions required to implement the electronic design into the final hardware assembly. Included are the following levels of packaging: chip, package, hybrids, printed wiring board, backplane, system interconnections and environmental control systems.

The primary packaging area with the greatest impact on system R&M is interconnections. These occur at all levels of packaging and have been shown to contribute to the greatest number of system failures in the field.

The interconnection design goal of the future should be to put more functionality or circuits on the silicon chips and thereby significantly reduce the numbers of interconnections at the higher packaging levels. This will result in a corresponding increase in circuit and system reliability due to two factors: (1) the chip level interconnections have proved to be the most reliable, (2) the higher levels of interconnections, which are less reliable, will be reduced in number as the system volume shrinks and numbers of connectors and cables between functional units are reduced.

The quantum improvements in R&M will only be attainable if the system architecture design programs at the basic chip levels include the essential packaging and interconnection parameters which will become part of the final system design. These must be

integrated into an overall CAD program for circuit partitioning, layout and interconnection.

The continued increase in IC device functionality by reduced feature size on the new VLSI chips will make available chip area which can be used for on-chip test and fault location circuits. Some emphasis is required in this area so that the required R&M improvements can be accomplished.

The retooling of our electronic manufacturing facilities will be required to make use of the latest automated processing, assembly and test equipment. These will improve the product producibility by reducing throughput time, improving yields and lowering cost. Incentives are therefore needed to encourage rapid introduction of these equipments into our production facilities.

An integral thread throughout the study has been the inter-relationships which exist between major technology areas such as VLSI/VHSIC, CAD/CAM, Packaging, and Cabling and Connectors. An integrated approach to solving these individual requirements is essential to successful implementation of the following recommendations.

1. DoD should fund a new task to broaden the VHSIC Integrated Design Automation program to include the determination, during the system architecture design and partitioning, of that mechanical design which best relates to the optimum VHSIC/VLSI chip design to ensure optimum packaging.

2. DoD should initiate additional incentive programs to encourage factory modernization including upgrading of existing manufacturing facilities to

include necessary automated production and inspection facilities to ensure that the predicted improvements in R&M are achieved.

3. The DoD must upgrade existing military test documents (e.g., MIL-STD-883) to accommodate the new technologies introduced by the VLSI/VHSIC systems. A study should be funded to revise the existing standards by including new or improved tests which have a significant impact on system R&M.

4. A DoD study should be funded to determine the real distribution of failures in electronic equipment, including a means of collating and filing failure data with sufficient detail to pinpoint the causes for electronic system failures including the IC chip or any other part of the associated packaging and interconnection levels.

5. It is recommended that a combined government and industry study be initiated to establish strategic military requirements in the electronic ceramic technology area. It is recommended that this be done in close cooperation with the VHSIC Program Office.

6. Future DoD contracts should include procurement incentives for the total Life Cycle Cost of the system being procured as opposed to singling out performance, initial cost, and MTBF. For long procurement production contracts, incentives should be made for the contractor to improve the reliability and maintainability of the system while a major portion of the production systems are yet to be built.

7. Establish a DoD focal point to coordinate and integrate the government packaging and interconnection programs with the cooperative commercial technology research and development ventures to ensure maximum synergistic benefits. The task force should include representatives of major commercial ventures such as microelectronics and Computer Technology Corporation (MCC), the Semiconductor Research Cooperative (SRC), military service, other government and industry members. The task force should provide guidance in the application of specific DoD packaging and interconnection design, development and implementation programs to facilitate VHSIC/VLSI technology insertion into selected DoD systems.

8. DoD should fund an effort to promote maximum interfacing and communication between government and industry by having a DoD task force recommend military packaging standards, outlines and configurations to an established standards committee and by having the military services further contribute to package standardization by increased participation and coordination with industry standards groups or committees, such as JEDEC, and by having military equipment designers make concerted efforts to include the packaging standards into new system designs.

R&M STUDY

ELECTRONIC PACKAGING AND INTERCONNECTION

EPIC STUDY OF COMPONENTS (EPIC) REPORT OUTLINE

I, SCOPE

The purpose of the Electronic Packaging and Interconnection of Components Study was to identify potential improvements in R&M and Readiness through the use of improved electronic packaging technology and to recommend specific management policies and key technology development programs to accomplish the insertion of these technologies into military systems in the most effective and timely way.

The basic electronic packaging areas considered are shown in Table 1.

Section II of the Study details the present state-of-the-art in electronic packaging and identifies the various critical packaging technologies. Also identified are the interfaces with the other functional areas that will require careful integration for optimized results.

Section III of the report defines the technical/management issues which impact the use of new packaging technology to improve system R&M, and provides a comprehensive listing of present and planned government-sponsored packaging programs including VHSIC R&D, VHSIC M&T, other R&D and M&T programs and planned commercially-sponsored programs such as the Microelectronic and Computer Technology Corporation packaging program.

Section IV makes specific recommendations in each of the identified areas.

Appendix A provides a bibliography of related technical reports, articles and studies which provide the necessary technical backup for the study recommendations. Appendix B consists of some of this backup material.

Table 1. ELECTRONIC PACKAGING SCOPE

1. Device Interconnection and Assembly

2. Packages

   Single Chip
   Multi-chip

3. Hybrid Packaging

4. Printed Wiring Board/Substate Interconnect (2nd level)

5. Backplane Interconnect (3rd level)

6. Connectors and Cabling

7. Environmental Protection

8. Thermal Management

9. Cabinets and Structures

10. Microwave Packaging

11. Packaging Interfaces

    1. Architecture/Partitioning
    2. VHSIC/VLSI
    3. CAD/CAM
    4. Testing
    5. Cabling and Connectors

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II. ELECTRONIC PACKAGING STATE-OF-THE-ART

Electronic packaging can be thought of as the "glue" that holds a system together and allows it to properly function. It is the effort necessary to translate electrical, mechanical and environmental requirements into hardware. This is illustrated in Figure 1.

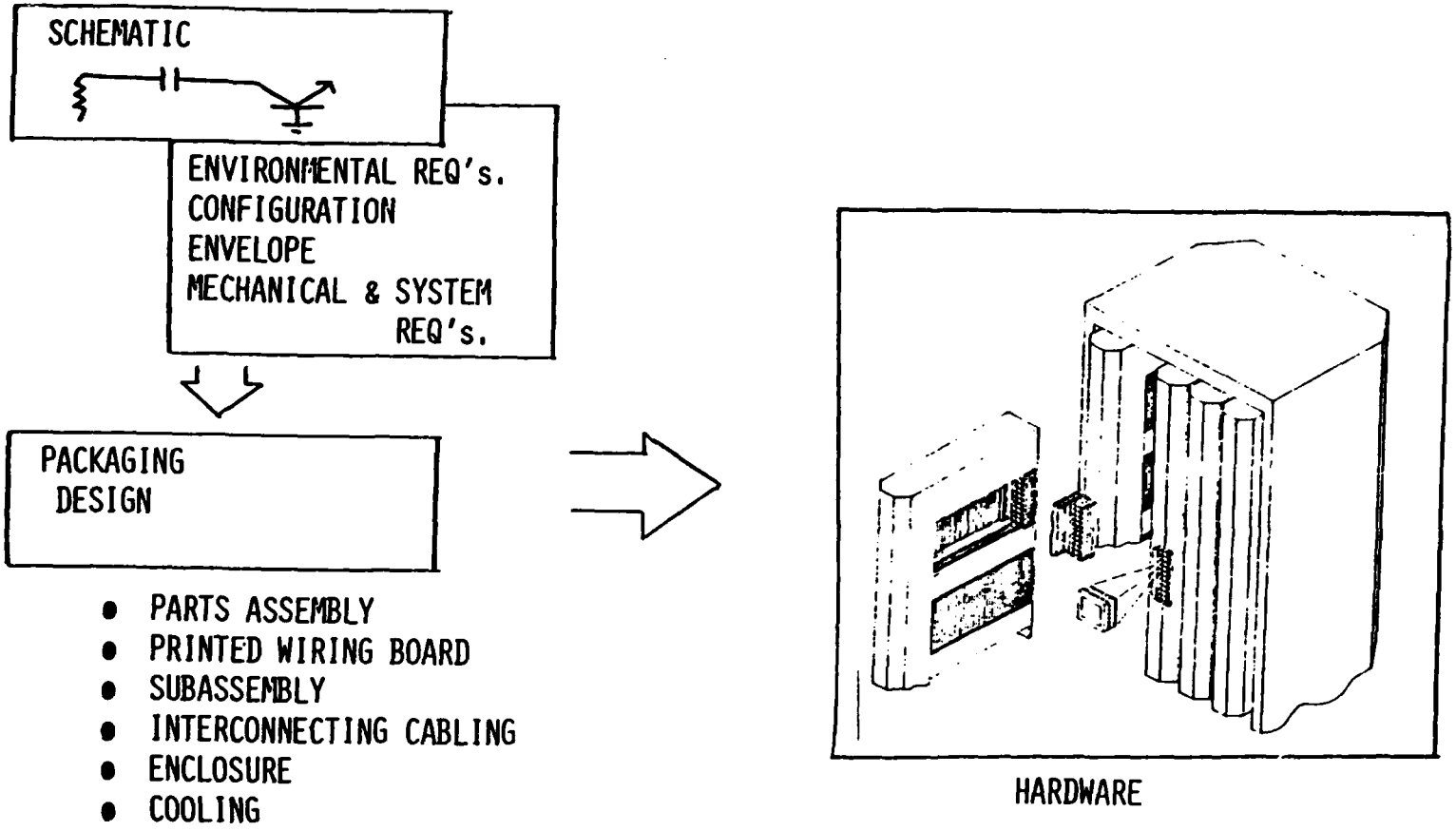
As an effort it is distinct in that it has only just recently begun to emerge as a separate discipline in the field of engineering. It is in fact, a marriage of the established disciplines of mechanical engineering, electrical engineering, manufacturing, materials engineering, device physics and process engineering. It is exactly this required blend of skills that has characterized electrical packaging through the years as more of an art than a science. This general lack of understanding and support of this complex subject has resulted in little generic progress in the field over the last twenty odd years or so.

To be sure, there have been some very clever solutions to systems packaging problems over the years, both in the commercial and military arenas. However, close examination shows these to be very application oriented and difficult to transport from one system to another.

Pieces and part of these specific solutions can be shown to be somewhat generic in nature. These are items such as:

- First level interconnect packages such as the dual in-line (DIP) flat-pack and chip carrier. (The phrase "first level interconnect" is associated with electronic components. It can be thought of as the wire bonds that connect an integrated circuit (IC) to the package that houses and protects the IC). Some of these packages are truly generic in that they are industry standards.

- PACKAGING CONVERTS ELECTRICAL DESIGN TO HARDWARE



- PARTS ASSEMBLY
- PRINTED WIRING BOARD
- SUBASSEMBLY
- INTERCONNECTING CABLING
- ENCLOSURE
- COOLING

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FIGURE 1. Electronic Packaging

- Second level interconnect structures such as multi-layer printed wiring boards (PWB's), double-sided PWB's and microstrip PWB's. These items are generic in the sense that the materials, processes, and techniques associated with their design, manufacturing, testing, and usage are well understood throughout the industry, to the point that they are "standard" items.

- Hybrid microcircuit packaging techniques lie somewhere between the two areas just mentioned. A hybrid microcircuit uses an insulating substrate on which is deposited thick or thin film circuit elements such as conductors, resistors, capacitors, and inductors, and to which is mounted active and passive devices in chip form and which is housed in a package which protects the completed circuit from the surrounding environment and provides a means for interconnecting it to surrounding circuitry. Like a PWB, a hybrid has a conductor pattern incorporated in it, but it is more like a first level interconnect structure in that it uses techniques such as wire bonding to interconnect its active elements to the substrate and it is typically being used as a packaged component on a printed wiring board.

- Third level interconnects can be thought of as those which are used to interconnect printed wiring boards within a Line Replaceable Unit (LRU). Accepted third level interconnect techniques include wiring harnesses, flex

circuitry, wirewrap and multi-layer motherboards. There are other techniques as well, but by far, wiring harnesses and motherboards are the most popular ones. Motherboards are gaining in popularity due to their economy and the ease in which they can accommodate controlled impedance circuit paths.

- Level four interconnect techniques are those used typically to interface motherboard assemblies with other elements comprising the LRU and to the LRU's external connectors. Common techniques used are wiring harnesses, cables and flex circuits. Fiber optic techniques are becoming useful in certain specific instances.

- The fifth level of packaging refers to those techniques used to interconnect the various LRU's to each other and to other platform systems. Wiring harnesses, cables and fiber optics techniques are again typically used here. The five levels of electronic packaging are illustrated in Figure 2.

- Connectors and thermal management techniques are other elements of electronic packaging that deserve some mention here. Connectors have evolved over the years into several different commonly used groups of different types styled for particular applications. There are PWB connectors, rack and panel connectors, gas tight connectors, etc. Military

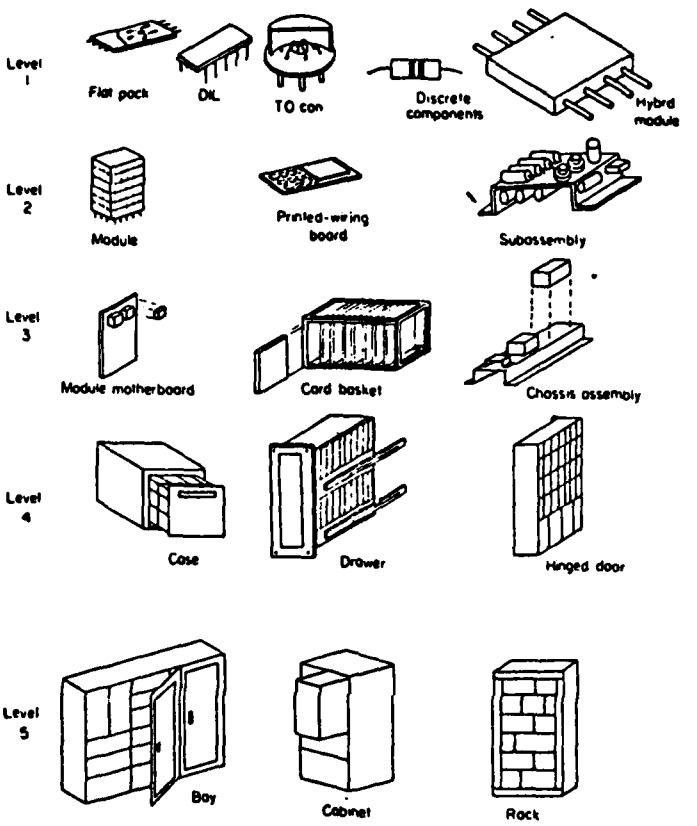

FIGURE 2. Packaging Levels and Available Components

specifications have played an important role in determining the types of connectors used today.

- In like manner, military specifications have guided the evolvement of thermal management techniques. The taboo in the use of direct air impingement for cooling has caused designers to use conduction cooling from the edges of PWB's via card guides nto a "cold wall" through which cooling air flows. In so-called high power situations, thermal planes which cover the front or back of a PWB are used to augment heat conduction into the cold wall. These techniques have been, for the most part, very satisfactory to this point in time.

What does all of this have to do with the reliability and maintainability (R&M) of today's/tomorrow's military electronic systems? Since the execution of electronic packaging tasks is what converts a system design into hardware, what is accomplished during this phase will have a significant impact on a system's ultimate reliability and maintainability.

Recent data indicates that less than two percent of all avionics failures involve IC components. Approximately sixty percent of all avionics failures can be attributed to higher level components (connectors and cabling). Another twenty-five percent were caused by maintenance and test procedures. The remaining failures fell into the category of overstress and abuse of system components. Figure 3 summarizes these failures.

What does this data imply with regard to packaging's effect on system R&M? Given the fact that it is quite easy to reach sweeping conclusions from such limited data, it is quite obvious

Failure Type	Failures (%)	
	Avionics	Aircraft
Cabling (B_n)	60.0	33.0
Maintenance (C_n)	24.8	13.6
Abuse (D_n)	11.4	6.3
Non-IC (E_n)	1.9	1.05
Total	98.1	53.95
Adding IC failures (F) (chip involvement)	1.9	1.05
Total avionics failures	100.0	55.00
Adding non-avionics failures		45.00
Total aircraft failures		100.00

FIGURE 3. Avionics and Aircraft Failure Sources

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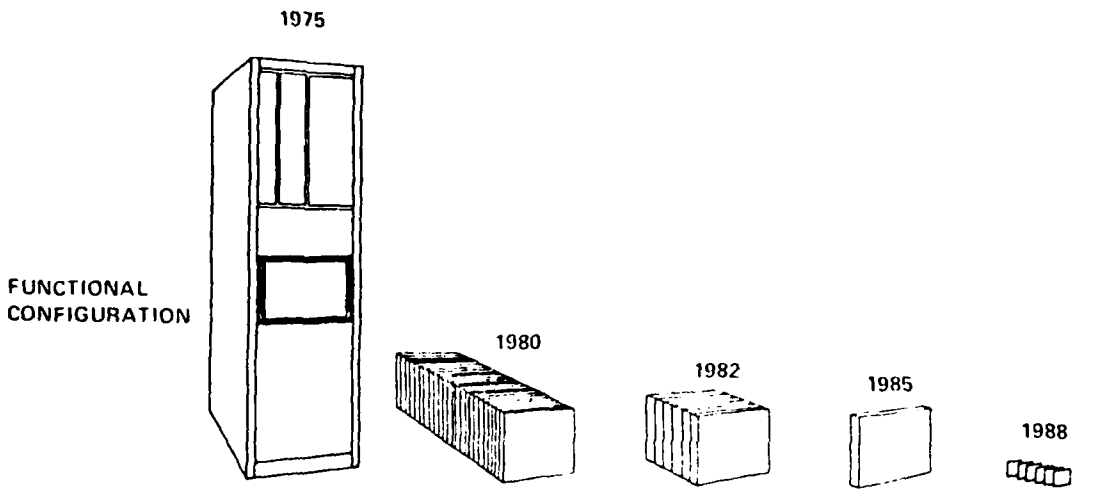
that the existing state-of-the-art of level three, four and five electronic packaging is not optimum with regard to system R&M. The large number of wires, cables, connectors, and contacts per connector appears to be at the root of this problem. If this is the case, then a thrust to reduce the numbers of wires, etc., would tend to lower the failure numbers we see today. Higher levels of integration, optimized system partitioning, data buss usage and fiber optics would tend to produce the desired results, however they bring along problems of their own. The first illustration in Fig. 4 shows that the wires, cables, connectors, etc. required in a 1975 vintage system can virtually all be replaced with the advent of the 1988 VHSIC based system, thus significantly reducing the number of failures associated with these items. Figure 5 is an illustration of the potential effect of system partitioning with an eye toward R&M. In the original system, there are a total of sixty level three and four interconnections. The illustration shows that the bulk of the level three interconnections exist between subassemblies A&B and C&D. By repackaging the system to combine the A and B functions and the C and D functions, a total of 32 interconnections are eliminated with a positive implication for system R&M.

SUMMARY

It can be concluded from the above that much can be done to improve the existing packaging state-of-the-art with regard to the reliability and maintainability of military electronic systems. Today's integrated circuits are typically much more reliable than the system's electronic packaging that surrounds them. The trend toward higher levels of integration, currently being augmented by the VHSIC program, is a positive one in that it allows more interconnects to be made at level one, the most reliable and least susceptible to damage of all levels of packaging. One must be



Semiconductor Technology	TTL/SSI/MSI	PMOS/NMOS	2μm CMOS	1¼μm VHSIC	0.5μm VHSIC
No. of Boards	60 Bds	24 Bds	6 Bds	1 Bd	4 6 Chips
Size	8 ft3	0.86 ft3	0.2 ft3	0.1 ft3	0 01 ft3
Gates/Chip	10-50	400	6K	30K	100K
Clock Rate	10MHz	20-40MHz	30-40MHz	40MHz	,100MHz
Power	3kW	1.6kW	300W	50W	3W

4900

FIGURE 4. Integration Levels Reduce System Size, Complexity, Power and Interconnects

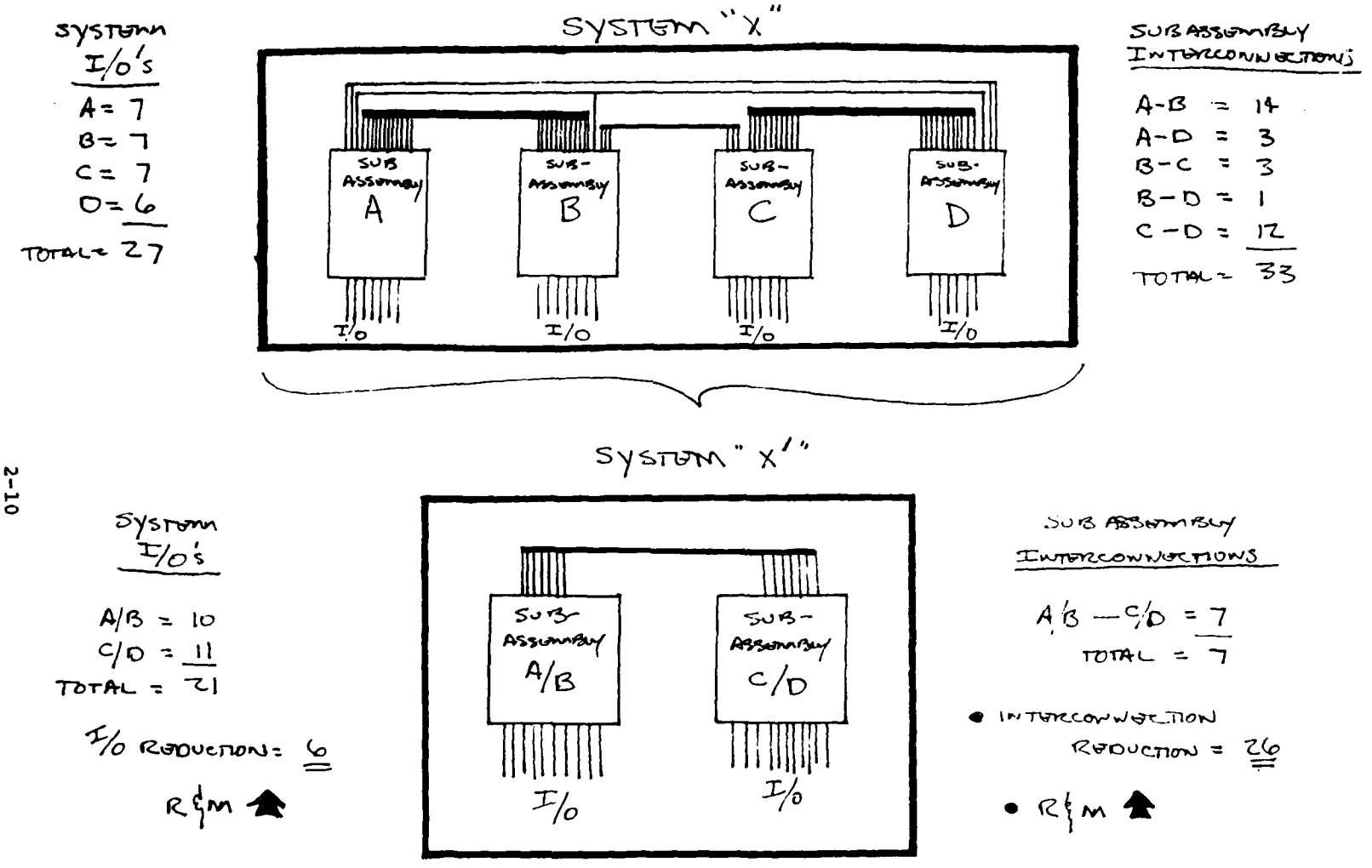


FIGURE 5. Proper Partitioning Improves System R&M

careful though to use proper system partitioning to make the most of the potential benefits of higher levels of integration.

System cooling techniques of today are reaching the limits of adequacy for dense systems. Newer packaging techniques such as chip carriers will tend to increase system power densities. The higher integration level of VHSIC/VLSI will offset this problem somewhat, but cooling techniques that exist today will not be adequate for tomorrow's denser systems.

Existing PWB materials will be adequate for the near term, but will become less and less adequate as clock speeds climb to and exceed 100 MHz.

Connectors that are common today will follow a like pattern. Pin counts, designs, and insulating dielectrics will suffice for some time, but will prove to be inappropriate with very quick rise times and high speed times.

III. TECHNOLOGY/MANAGEMENT ISSUES

A. TECHNOLOGY IMPACT

The primary impact of packaging new electronic technology on R&M is in the quantity and type and location of interconnections.

Interconnections in present systems are essentially evenly distributed between the IC level and the PWB level (Fig. 6). Since only about 2% of the system interconnection failures occur at the device level, the vast majority of failures occur at the higher level of system packaging, i.e., printed wiring boards (PWB) backplanes and system and subsystem cabling and connector systems (Fig. 7)(Ref. 1).

A convenient way to measure interconnection effectiveness is to use the modeling technique proposed by Dr. John Salzer, Salzer Technology Enterprises, in which he uses an interconnection reduction ratio, IRR to characterize the effectiveness of an interconnection method (Ref. 4).

This model concept reduces the electronic package to its basic elements, active device, resistor, capacitor, etc. These elements have two or three terminals, although some, like transformers, may have more. In turn, these components are interconnected to form the final electronic function. In doing so, the large number of interconnections within the package are reduced to relatively few upon leaving the package.

This reduction of nearly ten to one is therefore defined as the interconnection reduction ratio, IRR and is a measure of system interconnection effectiveness. It can also be shown that the IRR for a complete system is equal to the product of the IRR's of the individual levels.

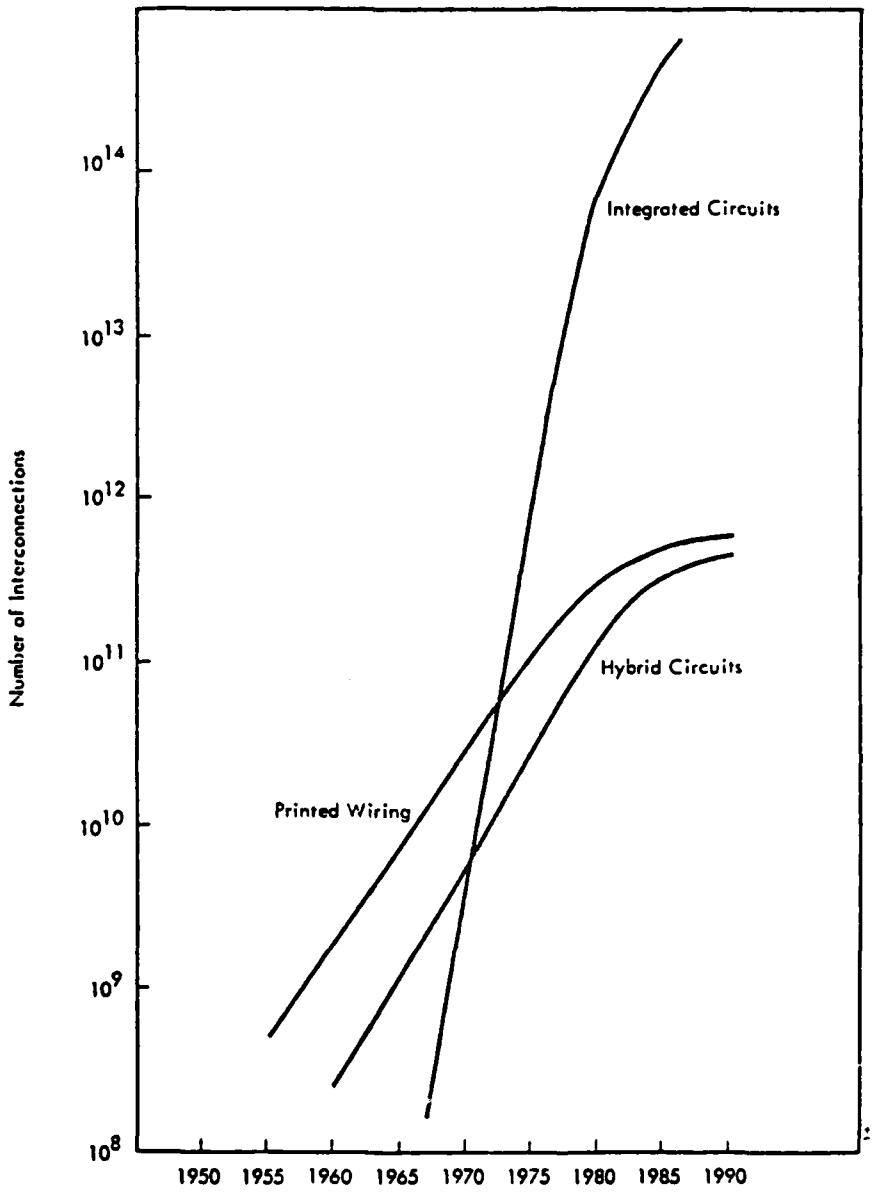


FIGURE 6. Interconnection Quantity Trends
Source: Gnostics Report

Failure Type	Failures (%)	
	Avionics	Aircraft
Cabling (B_n)	60.0	33.0
Maintenance (C_n)	24.8	13.6
Abuse (D_n)	11.4	6.3
Non-IC (E_n)	1.9	1.05
Total	98.1	53.95
Adding IC failures (F) (chip involvement)	1.9	1.05
Total avionics failures	100.0	55.00
Adding nonavionics failures		45.00
Total aircraft failures		100.00

FIGURE 7. Avionics and Aircraft Failure Sources
Source: SAR Report

A summary table of a typical system is shown below. (IRR at each level)

Level	Analog	Computer	Military Digital
0	60	300	150
1	1	1	10
2	8	15	25
3	6	8	15
4	4	6	8
Total Product	11520	216,000	4,500,000

The most striking difference is between level 0 and 1. Level 0 is the on-chip interconnection consisting of the metallization layer and polysilicon pattern. Because of batch fabrication techniques and the continued reduction in feature size (line widths and pad sizes), the cost of making interconnections at the chip level continues to go down. (See Fig. 8). Typical costs are combined with IRR to provide a more representative interconnection effic./cost figure of merit, IRRK or RK for short.

Chip Type	IRR	K	RK
Discrete	1	.83	.83
TTL	25	.025	.63
LSI	400	.008	3.20
VLSI	3,000	.005	15.00
64k RAM	15,000	.0007	10.00

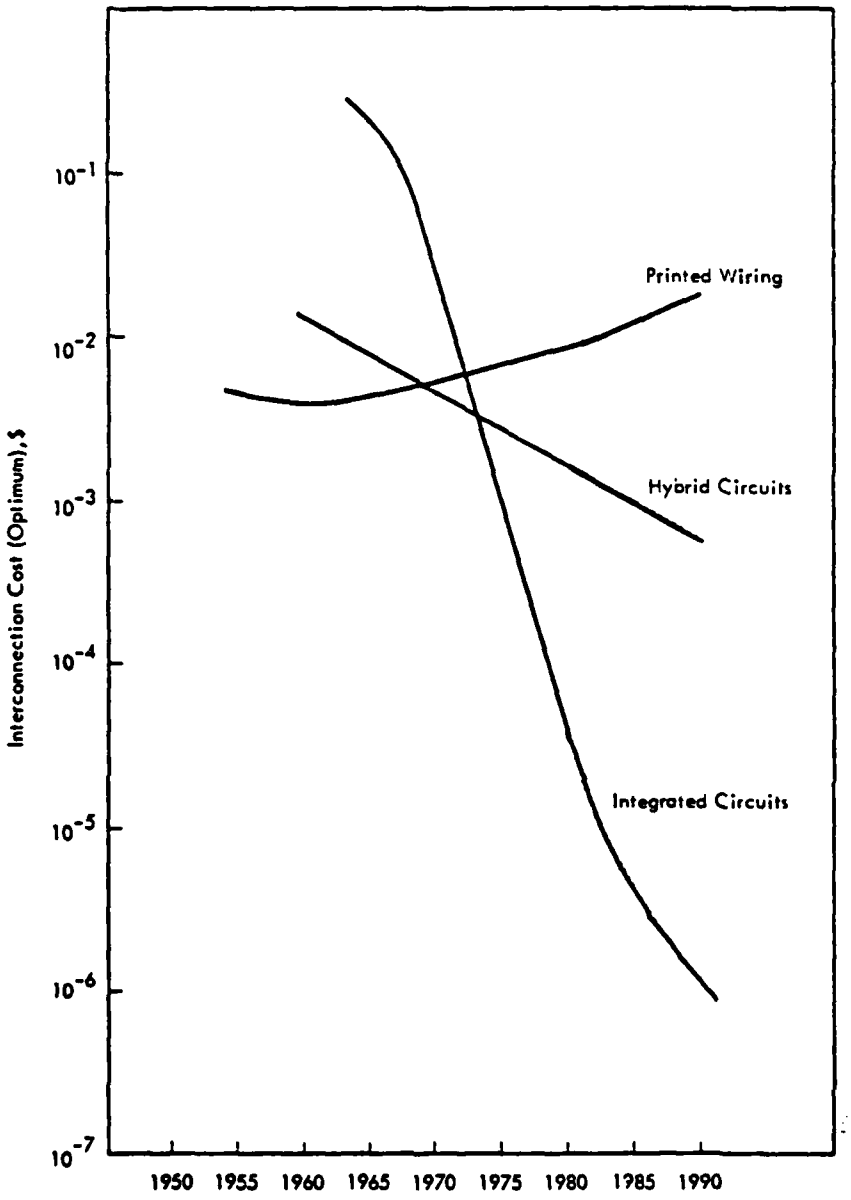


FIGURE 8. Interconnection Cost Trends
1950 Through 1990
Source: Gnostics Report

When integrated circuits, selected from current production, are designed into a system, their design determines the portioning interfaces precluding optimizing the interconnections between partitioned functions. Optimization can occur best when control of the integrated circuit design is exercised, as in custom VLSI. This has tended to proliferate the types of interconnections that are of reduced reliability and higher maintenance sensitivity.

The future trend is towards more interconnections at all levels but with the major increase at the chip level as new VLSI and VHSIC devices are released. Making interconnections at this level is most advantageous since it provides the lower cost and most reliable interconnection.

The need for integration of the chip architecture, interconnection and layout program with the packaging system CAD program is becoming evident as new LSI and VLSI chips are being designed with greater complexity and functionality operating at higher frequencies and clock rates and dissipating more power.

There has been developed a high degree of interconnection and placement capability at the printed wiring board level which has not been integrated into the chip layout programs. This expertise needs to be utilized and additional chip package programs should be developed which incorporate the various electrical parameters that will affect the final operation of the device. Unless this type of information is incorporated into the chip architecture design and layout programs, the expected improvement in system R&M will not occur.

The integrated design programs should have the following objectives:

- Overall system partitioning that minimizes interconnections

- Maximization of interconnections on silicon

- Design in BIT, fault isolation and appropriate redundancy

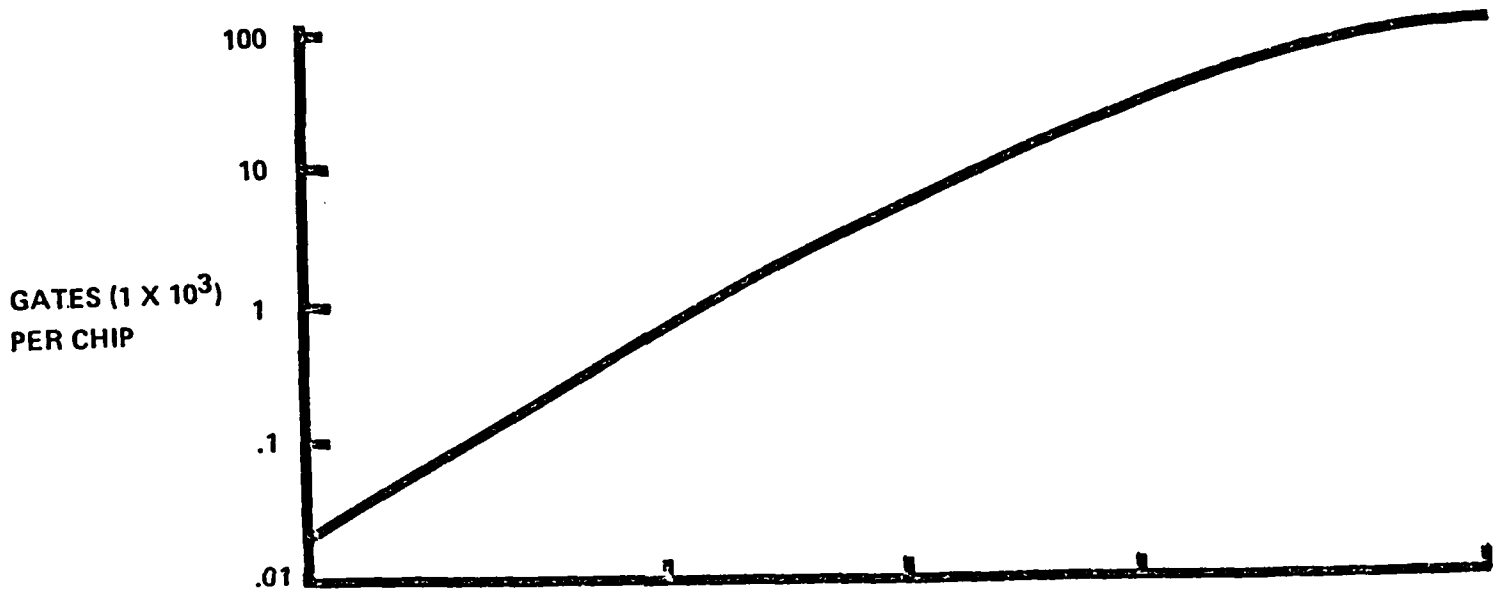
- Include thermal design guidelines in basic layout and partitioning programs

However, the increased use of VLSI/VHSIC devices with higher lead count packages in the 100 plus region will require higher interconnection density on printed wiring boards and hybrid substrates that in turn will require finer interconnect traces and spaces which are beyond current standard practice and will tend to reduce overall system reliability if not addressed.

The chart in Fig. 9 shows the effect of introducing VLSI chips in a typical system. While this chart shows a gradual reduction of chip feature to .5 μ, its basic trend would still be valid if larger chips were made using 2 μ processes. The important story here is the reduction in board quantities with the resultant reduction in system connectors, backplanes and cables. Other benefits are reduced size, weight and power requirements. The use of on-chip test and redundancy will also minimize failures caused by maintenance procedures. It should be mentioned here, however, that simple replacement of existing devices with VLSI equivalent functions on a pin-for-pin basis will not provide the R&M advantages of reduced packaging which could be achieved by a more comprehensive design procedure implemented in the early system design phase. This initiative combines a common interact effort in designing the package and the chip.

In a recent study, a series of scenarios show that as VHSIC devices are introduced system reliability and therefore availability does increase (Ref. 12).

Westinghouse had some preliminary information regarding the insertion of VHSIC technology in an F-16 radar computer. The



SEMI-CONDUCTOR TECH.	ECL/SSI	ECL/MSI	2 μm CMOS	1.25 μm VHSIC	0.5 μm VHSIC
GATES PER CHIP	10-50	400	6K	30K	100K
CLOCK RATE (MHz)	10	20-40	30-40	40	100
NO. OF BOARDS	60	24	6	1	4-6 CHIPS
SIZE (FT^3)	8	.86	.2	.1	.01
POWER	3 KW	1.6 KW	300 W	50 W	3 W

SOURCE: INTERNATIONAL MICRO ELECTRONICS CONFERENCE, FEBRUARY 1981, C. BROOKS & MICHAEL LUCAS

FIGURE 9. VLSI Impacts

data shown in Fig. 5 is compiled from the Westinghouse information and is based on the following three implementation scenarios;

1) An insertion of VHSIC chips (gate arrays with 8,000 gates) into a logic configuration with the number of boards remaining constant, as compared to the baseline configuration, but with the chip total being substantially reduced.

2) An insertion of the same VHSIC 8,000 gate array into a logic implementation that was reconfigured to maximize the use of the gate arrays while at the same time reducing the total board compliment.

3) An insertion of high density VHSIC chips (with an average per chip gate complexity of approximately 27,000 gates) into a logic implementation that was reconfigured to maximize the use of these high density chips and designed to minimize the board count. Some VHSIC gate arrays are included in this design.

It must be emphasized that the first two implementation scenarios use gate array chips, whle the third scenario used both gate arrays and the higher density custom/semi-custom VLSI chips. Some of the specific information obtained from Westinghouse is summarized below:

Configuration	SSI/MSI/LSI IC Pack. Ct.	VHSIC Pack. Ct.	VHSIC Gate Array Pack. Ct.	Performance	MTBF
Baseline	6,000	-	-	X	330
Scenario #1	895	-	55	X	756
Scenario #2	917	-	33	1.25x to 2.3x	1311
Scenario #3	600	yes *	5	2.8x to 3.0x	2067

*Number of high-density
VHSIC chips used was not defined

Figure 10 shows the MTBF as a function of the package count for the "baseline" Westinghouse configuration and the three scenarios detailed above. Note the significant impact on MTBF when new packaging is used (the difference between scenario #1 and #2, yields almost a factor of two increase in MTBF. Additionally, from the previous chart and Fig. 6, not only does the MTBF increase as a result of the VHSIC insertion, but the performance increases up to a factor of 3. It is apparent from this data that the system reliability is considerably enhanced when VHSIC technology is applied.

B. COMMERCIAL/GOVERNMENT TECHNOLOGY SYNERGISM

1. Commercial

It is highly desirable that synergism exist between commercial VLSI development and related government VHSIC efforts.

Some of the most significant recent VLSI advances have been made in Japan through programs sponsored and funded by Japan's Ministry of International Trade and Industry (MITI).

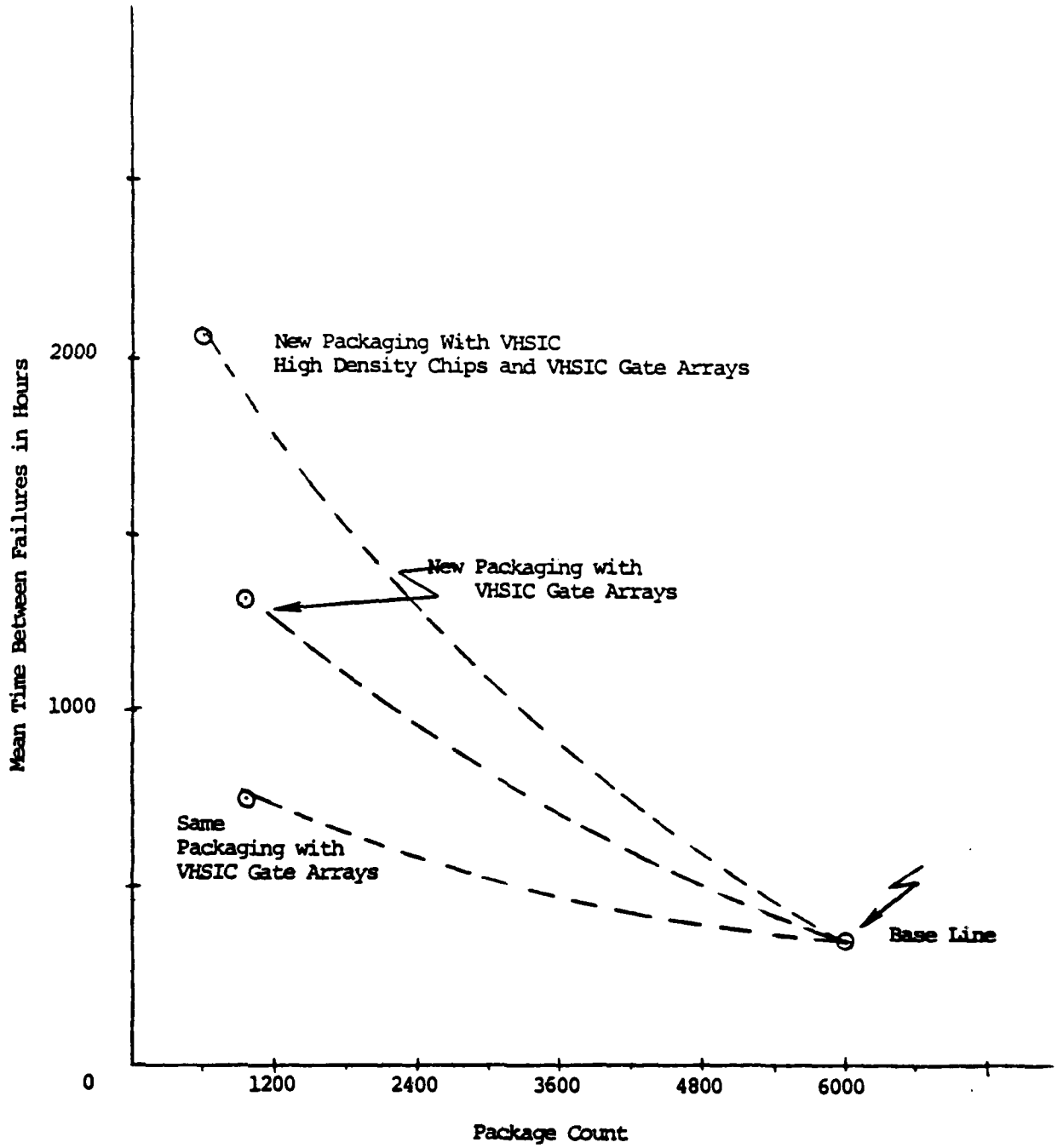


FIGURE 10. MTBF Versus Packaging for Westinghouse Data

The recent response to these needs in 1982 has been the formation of the Semiconductor Research Cooperative with Larry Sumney as Executive Director. A total of 13 U.S. companies have paid fees of at least $50,000. The total program for 1983 is expected to be over $10M, and will be used to fund universities in the form of individual grants and also to fund centers of, excellence. In addition to five initial grants, two research centers of excellence have been established. First, a Computer Design Center with first-year funding of $1.75M is a joint project between University of California at Berkeley and Carnegie Mellon University. The Microscience and Technology Center has been established at Cornell University, with initial funding of $1M. The three major areas of interest are micro-structure science production and engineering and systems and design. Packaging will be addressed in the production and engineering phase.

The other major entry into the field is Microelectronics and Computer Packaging Corporation (MCC). This consortium of U.S. firms will support research activities which will benefit all. The eleven initial corporations include: Digital Equipment Corporation, MOSTEK, RCA, Sperry Univac, Harris Semiconductor, NCR, Motorola, Control Data, Honeywell, National Semiconductor, and AMD. The sponsors contribute a minimum of $1.2M for participation in the CAD/CAM project which is one of four major thrusts. The others are system and chip packaging and interconnection, advanced computer architecture and software productivity. The microelectronics packaging task has been defined and includes the following tasks:

I. <u>DIE PREPARATION</u> - Develop technology for hermetic die capable of mass bonding in an automated manner for the majority of device technologies available or planned, and expandable to pin counts in excess of 400.

II. EQUIPMENT AUTOMATION - Develop equipment and processes for automated handling of devices in I from inner lead bond, through test, burn-in and including bonding into individual packages or direct attach to substrates.

III. DEVICE ENCAPSULATION - Develop materials and processes for mechanical protection of devices in I, allowing for direct attach to PC boards in minimum area and addressing thermal and reliability issues.

IV. HIGH DENSITY SUBSTRATES - Develop materials and production technologies for high density controlled impedance interconnect substrates (250 I/Os/in^2) capable of accepting direct attach devices from I and III and dissipating power up to 10W/in^2.

V. DEMONSTRATE TECHNOLOGY - Demonstrate the reliability, manufacturability and versatility of the technologies by building and testing a system test vehicle containing representatives of all options and operated under worse-case conditions.

Marshall Andrews of Harris Semiconductor is the MCC packaging task force leader. He estimates that $8 million funding will be required to fund the first three years. The total packaging program is expected to cost approximately $50 million and to last six years. Seven to ten companies are expected to join the packaging effort.

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2. Government

Advanced electronic packaging programs of interest to the military services have been compiled. A total of 44 projects have been separated into eleven packaging categories, as either Research & Development (R&D) or Manufacturing Technology (MT) efforts, with a listing of the number under way or those being negotiated or proposed. Of these programs 17 are R&D and 27 are MT, with 14 under way and 30 being negotiated or proposed.

Another listing provides a title of each project under each category along with the source and fiscal year of support. Included are the VHSIC-supported packaging efforts. A number preceding each title can be used to refer to another listing which includes a brief description of each project. Those projects under way include the name of the contractor and the contract number and the others include the service project identification number. For further information, names of individuals as contact points are included.

The listings indicate the lack of programs for joint CAD/CAM, packaging, and VLSI/VHSIC programs to provide for optimum design. They do not include efforts being expended on fiber optics as an interconnect medium, or specific improved packaging and manufacturing efforts aimed at cost reduction efforts which are carried out under system development contracts.

A copy of this portion of the report is included in the Appendix.

C. STANDARDIZATION

The initial philosophy in new VLSI/VHSIC device development has been to allow the device developer to package these parts in any style he preferred. It was this approach that for example, resulted in the VHSIC program having six contractors with six different packages.

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The OUSDRE Reliability and Maintainability (R&M) study asks us to assess the impact of VLSI/VHSIC on DoD system R&M. Experience in real world applications led to the establishment of standard configurations and outlines early in military system design history. Therefore, the most direct method to ensure improved system R&M in the future application of VLSI/VHSIC devices is to establish standards specific enough to channel efforts into a controlled number of different configurations. At the same time these standards must be broad enough to not stifle creative solutions to the difficult technology requirements of inserting VLSI/VHSIC into DoD systems of the future.

An analysis of the six packages proposed for use in the VHSIC program yields an appropriate example:

Contractor	Package Style	Centers
IBM	Pin Grid Array	100 mil
Honeywell	Pin Grid Array	100 mil
T.I.	Leadless Chip Carrier	50 mil
TRW	Chip Carrier with Berg Chips	25 mil
Hughes	Leaded Flat Pack	25 mil
Westinghouse	Under Study: LCC	20 mil
	Flat Pack	25 mil

Review of this list suggests that three package styles and three center spacings would have satisfied the VHSIC contractor's needs if the choice had been limited from the start of the program. These are: 1) Pin Grid Array on 100 mil centers, 2) Leadless Chip Carriers on 50 mil centers, and 3) Leaded Flat Packs on 25 mil centers.

In fact all three of these technologies pre-exist the VLSI/VHSIC programs and have proven themselves in military applications. Indeed, a review of the wide variety of package styles available (pin array, pad array, LCC, flat pac, gull wing, dual-in-line,

TO, etc.) on the many center-to-center spacings available (100 mil, 50 mil, 40 mil, 25 mil, 20 mil, 12.5 mil, etc.) reveals that it will be very difficult achieving predicted R&M improvements unless more standardization is achieved for military system applications.

Establishing a limited number of outlines for military systems does not imply that ideas that will result in broadening these outlines should be discouraged. It is a well known fact, however, that those assembly systems and processes with the greatest volume of production can be very closely characterized and thus yield a very consistent product. This consistency is what ultimately results in System Reliability and Maintainability.

D. MANUFACTURING

Military electronics hardware manufacturing is burdened with many part numbers, low volume, complex technology, and high reliability/quality requirements which directly affect cost to the government. Our future military design and manufacturing directions need to be guided to a blend of design for life cycle cost and manufacturability considered actions in order to improve the military systems reliability and maintainability/availability.

Today's military manufacturing environment is batch process-oriented, using manual material handling which is labor intensive and time consuming to set up and change process or tooling, along with a large work-in-process inventory on an outdated manufacturing floor. The result is a high rate of rework/scrap and excessive paperwork with poor traceability. In addition, the military reliability concern with the first failure as opposed to commercial with the average failure rate requires 100% inspection in product fabrication. With today's manual visual inspection techniques, we are susceptible to quality escapes and excessive costs due to increasing labor rates. As future military system designs improve

performance, reliability, and maintainability by reducing interconnections at higher levels of packaging, manufacturing capabilities will have to advance to accommodate the more complex first and second levels of packaging interconnections.

Emphasis needs to be placed in designing and manufacturing for the life cycle cost of the equipment. New manufacturing approaches need to be established that manufacture quality into the end-item product instead of inspecting to achieve quality/reliability. Some degree of factory automation must be used to improve the quality of the future military hardware designs. The inherent features of automation that enhance quality and reduce scrap and rework are:

- Repeatability and consistency of automated equipment
- Adaptability to rel-time process control
- An environment for controlled material handling to prevent damage
- Improved data collection and correlation.

In addition, new techniques for automated in-line inspection should be developed to reduce human intervention and improve consistency and efficiency of manufacturing. The use of automation including robotics will require standardization in hardware design. Benefits will be reduced cost through increased productivity and quality in manufacturing resulting in a more reliable product.

Future military electronics manufacturing facilities will need to be flexible for multiple part types, low volume, and required machine downtime without affecting product flow. They need to be user friendly, that is: easily modified and implemented

into existing facilities. The SEACAPS (Naval Weapons Center, RFP N60530-83-R-0086) effort is a start in the right direction to improve product flow from design to shipment. The result of programs like SEACAPS will be a less expensive, more reliable product for the government, and, at the same time, a more competitive position for industry through increased productivity and quality and reduced lead time in manufacturing.

Another example of programs addressing this need is the Air Force ESD GET PRICE program. Major programs already involved are the E-3 airborne warning and control system radar, F-16 radars, and ECM equipment.

This basic purchasing policy assures that when factories are modernized the savings resulting will be shared between the contractor and the government.

E. CRITICAL RESOURCES

At the present time more than 80% of the finished ceramic packages and substrates are made off-shore. Recent studies have shown an increasing requirement for ceramic chip carriers and pin grid array packages of a custom and semi-custom nature to house new LSI and VLSI/VHSIC chips. In addition, custom hybrids and multi-layer ceramic substrates will be required for chip interconnection and mounting.

It is therefore a strategic necessity to encourage development of on-shore technology and production capabilities in ceramic package and substrate design and fabrication. It is recommended that a combined government and industry study be initiated to establish strategic military requirements in the electronic ceramic technology area. It is recommended that this be done in close cooperation with the VHSIC Program Office.

F. TESTING METHODS

Reliability and maintainability of DoD hardware will be impacted by the new technologies that will characterize the systems implemented with VLSI/VHSIC chips. Organic materials are being used in VLSI/VHSIC packages in unprecedented amounts. Die attachment and electrical interconnect films will be present that will require package ambient atmosphere analysis tests to assess moisture and contamination levels. The large size die require elastic die attachment materials to relieve the stresses of the TCE mismatch between chip (si) and package Al_2O_3). The silver-glass and silver-polyimides used will introduce materials that need to be studied and controlled when used in packages. Die shear tests will have to be altered to reflect the large geometries involved. The large number of 1/0 on the chip have resulted in the need for new approaches in quality assurance to assess the integrity of tape interconnect bonds. The large cavity size and Range Seal area of the VLSI/VHSIC packages will require revision of existing tests or new tests for hermeticity. Solderability testing of new surface mount components and pin grid components needs to be included in the test methods.

Standards of thermal measurement need to be established to ensure that devices are operating in the low temperature ranges that yield long life. The pre-cap internal visual inspection requirements need to be revised to deal with the 1.25 μ features and/or tape decal that will make the workmanship impossible to assess.

IV. RECOMMENDED ACTION ITEMS

1. DoD should fund a new task to broaden the VHSIC Integrated Design Automation program to include the determination, during the system architecture design and partitioning, of that mechanical design which best relates to the optimum VHSIC/VLSI chip design to ensure optimum packaging.

2. DoD should initiate additional incentive programs to encourage factory modernization including upgrading of existing manufacturing facilities to include necessary automated production and inspection facilities to ensure that the predicted improvements in R&M are achieved.

3. The DoD must upgrade existing military test documents (e.g., MIL-STD-883) to accommodate the new technologies introduced by the VLSI/VHSIC systems. A study should be funded to revise the existing standards by including new or improved tests which have a significant impact on system R&M.

4. A DoD study should be funded to determine the real distribution of failures in electronic equipment, including a means of collating and filing failure data with sufficient detail to pinpoint the causes for electronic system failures including the IC chip or any other part of the associated packaging and interconnection levels.

5. It is recommended that a combined government and industry study be initiated to establish strategic military requirements in the electronic ceramic technology area. It is recommended that this be done in close cooperation with the VHSIC Program Office.

6. Future DoD contracts should include procurement incentives for the total Life Cycle Cost of the system being procured as opposed to singling out performance, initial cost, and MTBF. For long procurement production contracts, incentives should be made for the contractor to improve the reliability and maintainability of the system while a major portion of the production systems are yet to be built.

7. Establish a DoD focal point to coordinate and integrate the government packaging and interconnection programs with the cooperative commercial technology research and development ventures to ensure maximum synergistic benefits. The task force should include representatives of major commercial ventures such as microelectronics and Computer Technology Corporation (MCC), the Semiconductor Research Cooperative (SRC), military service, other government and industry members. The task force should provide guidance in the application of specific DoD packaging and interconnection design, development and implementation programs to facilitate VHSIC/VLSI technology insertion into selected DoD systems.

8. DoD should fund an effort to promote maximum interfacing and communication between government and industry by having a DoD task force recommend

military packaging standards, outlines and configurations to an established standards committee and by having the military services further contribute to package standardization by increased participation and coordination with industry standards groups or committees, such as JEDEC, and by having military equipment designers make concerted efforts to include the packaging standards into new system designs.

APPENDIX A

BIBLIOGRAPHY

APPENDIX A

BIBLIOGRAPHY

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APPENDIX B

BACK-UP MATERIAL

ELECTRONIC PACKAGING AND INTERCONNECTION STUDY GROUP

PACKAGING PROGRAMS

FINAL

	R&D	MT	PROJECTS UNDERWAY	PROJECTS PROPOSED OR BEING NEGOTIATED
CHIP INTERCONNECTION	1	3	0	4
CHIP PACKAGE	4	3	1	6
HYBRID PACKAGING	1	7	4	4
ASSEMBLY TECHNIQUES	2	4	1	5
SECOND LEVEL INTERCONNECT	3	3	1	5
SECOND TO THIRD LEVEL CONNECTORS	0	0	0	0
THIRD LEVEL	0	1	0	1
INTERCONNECT CABLING	0	0	0	0
THERMAL MANAGEMENT	0	1	0	1
EMI	0	0	0	0
MICROWAVE	4	5	5	4
OTHER	2	0	2	0
	17	27	14	30
TOTAL	44		44	

CHIP INTERCONNECTION (FIRST LEVEL INTERCONNECT)

1.	Decal/Tape 1st Level Interconnect (VHSIC R&D)	FY 84-85
2.	Tape Interconnect Materials/Processes (VHSIC MT)	FY 84-86
3.	Wire Bond Monitor Integral To Wire Bonded System (N MT)	FY 83
4.	Automation of Aluminum Wire-Ball Bonding System (N MT)	FY 83

CHIP PACKAGE

5.	High Density Multilayer Package Development	(VHSIC R&D)	FY 83-85
6.	Fine Pitch Chip Carriers	(VHSIC MT)	FY 85-86
7.	Pin and Pad Grid Arrays	(VHSIC MT)	FY 84-86
8.	Multichip Packages	(VHSIC R&D MT)	FY 84-87
9.	MT For VLSI Chip Carrier	(AF MT)	FY 84
32.	Improved Package For VHSIC	(AF R&D)	FY 80
43.	Advanced Package For GaAs Circuits	(A R&D)	FY 84-86

SUPPORT: VHSIC Very High Speed Integrated Circuit (DOD)
A Army
N Navy
AF Air Force

Program Type: R&D Research & Development
MT Manufacturing Technology

HYBRID PACKAGING

10.	LSI Hybrid Microcircuits	(A R&D)	FY 80-83
11.	Individual Die Testing With Temperature	(N MT)	FY 82
12.	Electrical Test and Screening of Chips	(A MT)	FY 84
13.	Automatic Sealing of Hybrid Packages	(A MT)	FY 84
14.	Automated Optical Microelectronic Inspection	(A MT)	FY 84
15.	Cost Effective Automated Laser Soldering System	(N MT)	FY 84
25.	Hybrid Microcircuit Packaging	(N MT)	FY 84
42.	Automatic Recognition of Chip Orientation For Automatic Die Attachment (Automatic Hybrid Die Bonder System)	(A MT)	FY 82

ASSEMBLY TECHNIQUES

16. Package Board Assembly of VHSIC Packages (VHSIC R&D) FY 84-85

17. Board Assembly, Rework, And Solder Process Control For VHSIC (VHSIC MT) FY 84-86

18. Printed Wiring Board For Leadless Chip Carriers (N MT) FY 84

24. Feasibility of Automatic PCB Fabrication Line (N MT) FY 84-85

39. Automation of Leadless Components on PWB (AF Tech Mod) FY 82

40. Solder Characterization (AF R&D) FY 84-87

SECOND LEVEL INTERCONNECT

19.	Chip Carrier Compatible PWB	(VHSIC R&D)	FY 83-84
20.	Multi Chip Board Technology	(VHSIC MT)	FY 84-86
21.	High Reliability Packaging Using HCC on Compatible PWBs	(AF MT)	FY 82
22.	R&D For Chip Carrier Compatible PWB	(AF R&D)	FY 82
23.	MT For VLSI Compatible Printed Wiring Boards	(AF MT)	FY 84
44.	High Density PWB Development	(AF R&D)	FY 84-86

SECOND TO THIRD LEVEL CONNECTOR

THRID LEVEL (BACKPLANE)

27. Third Level Interconnects For VHSIC Assemblies (VHSIC MT) FY 85-87

INTERCONNECT CABLING

THERMAL MANAGEMENT

26. Heat Pipe and Heat Pipe Module Frame (N MT) FY 84

EMI

MICROWAVE

28. Manufacturing Techniques For EHF Printed Circuits (N MT) FY 84

29. Automated Microstrip Circuit Board Assembly (N MT) FY 82-83

30. MT For High Reliability For Microwave Integrated Circuits (AF-MT) FY 83

31. MT For High Speed Digital Processor Packaging Techniques (AF - MT) FY 83

33. Development of Distributed Network Processors For AOSP (DARPA - R&D) FY 82
Fabricated With GaAs Digital Device Technology

34. High Speed Digital Processor Processor Packaging Technology (AF MT) FY 80

35. Microwave Package Development (Hermetic Seal Connector) (N - R&D) FY 83-87

36. Gigabit MSIC Testing and Interconnection (AF - R&D) FY 82

41. Leadless Chip Carrier Packaging/CAD CAM Wire Wrap (AF-R&D) FY 79-85
Interconnect For Subnanosecond ECL

OTHER

37. Modular Avionics (N R&D)

Module Development	FY 83 -85
Enclosure Development	FY 83 - 85

38. Standard Electronic Module (N R&D) FY 83

Electronic Packaging and Interconnection Study Group
Military Packaging Programs*

1.Decal/Tape 1st Level Interconnect (VHSIC R&D) Linder 202 692 7640

Develop assembly processes for decal and tape in perimeter and grid configurations, single and multilayer. Evaluate optimum material construction and fabrication processes, develop reliability and inspectability procedures and demonstrate ability to withstand military environmental stresses.

2. Tape Interconnect Materials and Processes (VHSIC MT) Pratt 201-544-2308

Establish production capability for flexible tape chip to package interconnection technique. Interconnect requirement is 200 or more I/Os.

3. Wire-Bond Monitor Integral to Wire Bonded System (Navy MT DNE 00199) Riggs 812-854-1299

Implement simultaneous bonding and pull testing capability to decrease testing costs and reduce field failures. Present techniques of destructive pull testing on a sampling basis and non-destructive pull are ineffective and costly.

4.Automation of Aluminum-Wire Bonding System (Navy MT DNE 00222) Riggs 812-854-1299

Facilitate the automation of the aluminum wire bonding for semiconductor device interconnections by optimizing the wire-and-ball formation process. The R&D which has made manual formation of aluminum ball bond possible must be optimized for automation of the bonding process.

5. High Density Multilayer Package Development (VHSIC R&D) Pratt 201-544-2308

Design, develop and tool for a high terminal count (100-400) integrated circuit package, which is representative of a family of packages, and is suitable for packaging VHSIC devices. Grid arrays will include development of 50 mil center packages and chip carriers will include perimeter terminal contacts on $\leq$ 25 mil centers.

6. Fine Pitch Perimeter Contact Packages (VHSIC MT) Layden 201-544-2378

Establish processes and controls for high yield low cost manufacture of fine pitch, high lead count perimeter chip carriers on $\leq$ 25 mil centers in the leadless carrier configuration.

* Those projects underway include contract numbers and names of contractors. All other projects are either proposed or are being negotiated.

7. High Count Pin and Pad Grid Array Package (VHSIC MT) Pratt 201-544 2308

Establish cost effective manufacturing processes for VHSIC high lead count pin and pad grid array chip carrier packages.

8. Fabrication and Assembly of Multichip Packages (VHSIC R&D MT) Layden 201-544-2378

Develop high density multiple device package and establish associated manufacturing processes and controls which include provisions for implementing burn-in and functional tests of devices prior to module assembly.

9. MT For VLSI Chip Carrier (AF-MT 421E510-4A07xxxx) Knapke 513-255-2461

Establish economical manufacturing capability for fabricating high-pinout, high speed, high density VLSI chip carrier packages.

10. LSI Hybrid Microcircuits (R&D Raytheon DAAK20-80-C-0302) Pratt 201-544-2308

Develop a comprehensive set of design guidelines for LSI hybrid microcircuits encompassing a broad range of generic semiconductor logic technologies and substrate interconnect technologies together with various individual chip packaging options.

11. Individual Die Testing With Temperature (MT Teledyne Tac N00164-82-C-0230) Riggs 812-854-1299

Reduce military electronic system costs by the insertion and automation of semiconductor die in high and low temperature testing prior to final assembly or packaging.

12. Electrical and Screening of Chips (MT Teledyne Tac-Hughes DAAH01-82-D-0015) Sulkowski 205-876-2147

Build a fully automated prototype system that will electrically test individual semiconductor chips at hot, cold and room temperatures.

13. Automated Sealing of Hybrid Packages (Army MT 3 84 1095) Wooten 205-874-8487

Establish an automated hybrid package sealing system controlled by a microcomputer, including moisture bake out, package sealing and leak detection. System will optimized for programming, process control and flexibility of package types.

14. Automated Optical Microelectronics Inspection (Army MT 5 84 1802)
~~Weston 205-874-8487~~
Lane - 202-394-1515

An automatic inspection system will be implemented for use on the M734 thick film hybrid amplifier, utilizing image digitation, stage translation and image processing. Areas of inspection will include orientation of an unblemished die, correct wire bonding routing and correct wire placement along a predetermined path.

15. Cost Effective Automated Laser Soldering Systems (Navy MT DNE 00197) Riggs 812-854-1299

Hand soldering methods are inefficient and subject to operator proficiency. Mass soldering techniques subject whole assemblies to excessive heat, resulting in component drift and induced mechanical stresses. An automated laser system will be implemented, which will convey the substrates, position the components, laser solder, inspect the solder joint and transfer to the test position.

16. Package Board Assembly of VHSIC Packages (VHSIC R&D) Pratt 201-544-2308

A family or families of a number of different style packages will be selected which can adequately house the Phase 1 contractors' VHSIC chips and the techniques developed for mounting, assembling and reworking each type package on a second level packaging board.

17. Board Assembly, Rework, and Solder Process Control For VHSIC (VHSIC MT) Riggs 812-854-1299

Improve the solderability of packages and PWB assemblies and reduce assembly costs. Establish optimized solder materials, processes and controls for closely spaced high lead count terminal packages for VHSIC applications.

18. Printed Wiring Board For Leadless Chip Carriers (Navy MT DNE 00286) Riggs 812-854-1299

The solder joint on the PWB will be made more flexible by plating up a copper pedestal and soldering the chip carrier to the pedestal. The pedestal will be achieved by an additional plating process following the normal printed wiring board process.

19. Chip Carrier Compatible PWB (VHSIC R&D) Crist 513-255-4474

Candidate materials with low dielectric constant (≤ 3.5) will be investigated and selected for fabricating printed circuit boards in multilayer configurations to demonstrate dielectric constant and loss factor over a wide operating range at DC and over the frequency range 100-1000 MHz. R&D and MT results from Air Force contracts on TCE will be used to achieve the desired TCE and low K within the same board material.

20. Multi-Layer Board Technology (VHSIC MT) Tewksbury 513-255-4474

Establish a production capability for direct attachment of large, surface mounted packages, with more than 200 I/O connections, to multilayer boards. The boards sould be able to withstand more than 500 thermal cycles and should have a dielectric constant less than 3.5, ability to define 5 mil line technology, and a coefficient of thermal expansion matched to the leadless carrier.

21. MT For High Reliability Packaging Using HCC on Compatible PCBs (AF MT F33615-82-C-5071) Knapke 513-255-2461

Establish fabrication techniques for printed wiring boards which are thermally, mechanically and electrically compatible with JEDEC Type C hermetic chip carrier packages.

22. R&D For Chip Compatible PWB (R&D Westinghouse F33615-82-C-5047) Crist 513-255-4474

To aid in the identification and understanding of HCC failure mechanisms, to formulate criteria for future PWBs amd identify new materials and processes to meet that criteria. To advance the state-of-the-art in PWB materials and interconnections for surface mounted HCCs.

23. MT For VLSI Comnpatible Printed Wiring Boards (AF-MT 481E508-4A07) Knapke 513-255-2467

Identify and establish multilayer printed wiring board fabrication techniques which utilize low dielectric constant materials for high speed VLSI devices.

24. Feasibility of Automatic PCB Fabrication Line (Navy MT DNE 00218) Raby 619-839-2678

Identify and establish the manufacturing criteria for a computer controlled automated assembly line for the fabrication of printed circuit board assemblies. Will utilize sensor robotics coupled with state of the art equipment applicable to the fabrication, soldering, cleaning, coating and testing of electronic assemblies.

25. Hybrid Microcircuit Packaging (Navy MT DNE 00303) Hill 202-692-7227

Establish manufacturing technology for testing and burn-in of individual memory chips (BORAM) before they are interconnected in a multichip hybrid package.

26. Heat Pipe and Heat Pipe Module Frame MT Technology (Navy MT DNA 81072) Linder 202-692-7640

Establish and assemble cost effective automated production processes for small avionics heat pipes for cooling electronic module frames. Provide an economic analysis of projected life cycle cost savings.

27. Third Level Interconnects For VHSIC Assemblies (VHSIC MT) McKee 714-225-6877

Establish improved methods to accomodate the large number of I/Os between printed wiring boards and the unit interconnect system (backplane and cable harness). Alternative low insertion force connectors and multi-level interconnect backplanes with integral power and ground planes will be incorporated. Shield coax and twisted pair lines will be utilized wherever possible within appropriate cost constraints. Automatic insertion equipment will be used where feasible.

28. Manufacturing Techniques For EHF Printed Circuits (Navy MT DNE 00034) Carson 714-225-6763

Establish techniques for high yield processing and testing of ehf circuit boards to include bonding, sputtering, improved jigging, masking and alignment. New microwave circuits will be made including fin circuits, suspended substrates and microstrip.

29. Automated Microstrip Circuit Board Assembly (MT Texas Instruments N00019-81-C-0338) Linder 202-692-7640

Establish an automated manufacturing process for fabrication of integrated microwave circuit boards to reduce fabrication time and cost with increased reliability.

30. MT For High Reliability Packaging of Microwave Integrated Circuits (AF MT 311E588-3A085205) McLaine 513-255-2644

Establish manufacturing criteria, identify approaches to reduce cost, and define concepts for high volume production for x-band Transmit/Receive TR hybrid MIC modules for airborne phased array radars. Integrate the fabrication assembly and testing techniques into a pilot production line demonstration.

31. MT For High Speed Digital Processor Packaging Techniques (AF MT 111E503 -38084260) Knapke 513-255-2461

Project will establish manufacturing methods for large high density interconnection substrates compatible with leadless hermetic chip carriers for use in airborne radar signal processors. Demonstration vehicles will be implemented containing at least 50 HCCs which are to operate at system clock

speeds of 20-50 MHz and perform electronic functions used in airborne radar signal processors.

32. Improved Package For VHSIC (R&D General Electric F33615-80-C-1191) Crist 513-255-4474

Develop a multilayer beryllia ceramic package with 200 terminals for a large bipolar silicon VHSIC chip. The package will provide stress relief among materials of differing thermal expansions and incorporate materials of high thermal conductivity.

33. Development of Distributed Network Processes For The AOSP Fabricated With GaAs Digital Device Technology (R&D Mayo Clinic MDA903-82-C-0175) Kseperis 201-544-4437

The objectives are: 1. the design of appropriate IC packaging technology; 2. interchip communications protocols for high speed GaAs ICs 3. logic board designs and fabrication techniques which will support frequency components up to 2GHz; 4. design rules applicable to large GaAs configurable gate arrays or macro cell arrays 5. CAD software necessary to support GaAs processors, both at IC and system levels.

34. High Speed Digital Processor Packaging Technology (MT Westinghouse F-33615-80-C-5046) Knapke 513-255-2461

Establish and demonstrate manufacturing processes and controls for dense packaging of high speed digital processor circuitry used in airborne radar signal processors. Electronic modules are to be fabricated using ECL circuitry to demonstrate packaging techniques.

35. Microwave Package Development (Hermetic Seal-Connector) (Navy R&D) Kidwell 317-353-7965

Develop optimum connectors and hermetic sealing processing for large microwave packages.

36. Gigabit MSIC Testing and Interconnection (R&D Magnavox F33615-82-C-1774) Tewksbury 513-255-6553

Development of testing and interconnecting techniques for packaging of gigabit medium scale GaAs ICs.

37. Modular Avionics (Navy R&D) Linder 202-692-7640

Develop advanced packaging techniques which will improve reliability and maintainability and reduce life-cycle costs of avionics equipment. Project includes module and enclosure developments.

38. Standard Electronic Modules SEM (Navy R&D) Riegle 812-854-1854

Coordinated module level standardization program. Primary usage has been in Navy shipboard or shoreboard equipment. Use in Air Force and Army equipments has been minimal because of differences in platform sizes.

39. Automation of HCC Components on PWBs (Tech Mod Martin Marietta F33657-82-C-2145) Opt 513-255-4084

Tech Mod Program which addresses the automation of the assembly of HCC components and the subsequent assembly of these and other leadless components on PWBs.

40. Solder Characterization (AF-R&D) Crist 513-255-4474

Establish a data base for the characteristics of solders in the plastic range. Study such effects as grain boundaries, contamination, and gold embrittlement on solder elasticity, extension to the plastic range and point of fracture.

41. Leadless Chip Carrier Packaging and CAD/CAM Supported Wire Wrap Interconnect Technology For Subnanosecond ECL (R&D Mayo Clinic F33615-79-C-1875) Anderson 513-255-6553

To refine and develop CAD design protocols for implementation of subnanosecond ECL in high speed computer modules using a wirewrap interconnection medium.

42. Automatic Recognition of Chip Orientation For Automatic Die Attachment (Automatic Hybrid Die Bonder System) (MT Kulicke & Soffa DAAH01-82-C-0878) Sulkowski 205-876-2147

Development and fabrication of an automatic hybrid circuit assembly system for semiautomatic or automatic operation. System will interface with a host computer in an automated factory setting and will include an assembly robot, closed circuit TV system mounted within the robot's end-of-arm tooling, operator controls, automatic tool changing system, waffle pack and component feeders, substrate workholders and a magazine feeder.

43. Advanced Package For GaAs Circuits (Army R&D) Layden 201-544-2378

The establishment of high speed digital GaAs interconnection and packaging capabilities utilizing CAD packaging capabilities to address design, reliability and materials development for the implementation of GaAs circuits in military systems.

44. High Density PWB Development (AF R&D) Crist 513-255-4474

To demonstrate the practicality of software developed for CAD of PCBs with optimum electrical, mechanical, and thermal characteristics through the building of full boards for test and evaluation. The work will extend the

IMPACT OF THE INSERTION OF VHSIC TECHNOLOGY ON SYSTEM LEVEL RELIABILITY/AVAILABILITY

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1.0 INTRODUCTION

The VHSIC program has emphasized the coupling of integrated circuit technology to complex system development and implementation. Foremost among the goals of this program is to significantly increase the mean-time-between -failures for systems utilizing VHSIC technology when compared to a more conventional non-VHSIC implementation. Not only does this increase the probability of a successful mission but it can contribute to lowering the hardware life cycle costs.

This report will indicate the potential impact of VHSIC technology insertion in the areas of both increased reliability and availability. A generalized view and discussion of the potential impact on life cycle costs will be provided.

2.0 GENERAL DISCUSSION

Many factors affect reliability and modeling the potential reliability of LSI/VLSI circuits becomes extremely complicated. Complete reliability modeling for systems involving these circuits is beyond the capabilities of computers available today. One microcircuit reliability prediction model[1] has the general format

$$\lambda_p = \Pi_Q \Pi_L \left\{ C_1 \Pi_V \Pi_{p_T} + (C_2 + C_3) \Pi_E \right\}$$

where

λ_p is device failure rate in F/10^6 hour
Π_Q is device quality factor
Π_L is learning factor
Π_T is temperature acceleration factor
Π_V is voltage derating stress factor (CMOS devices only)
Π_{p_T} is ROM and PROM programming technique factor
Π_E is application environment factor
C_1, C_2 is device complexity factor
C_3 is package complexity factor

The authors of the referenced paper tested this model against actual failure rate data for a variety of circuits, with the results being quite good. An examination of this paper emphasizes the complexity of developing reliability models for IC circuits. The VHSIC development program represents a tremendous challange from a reliability modeling point of view since it has attempted to cover a variety of technologies, design approaches, design tools, interconnection schemes, packaging techniques and built-in-test/fault tolerant approaches. Figure 1 gives a summary of some of these implementation approaches. Each of these approaches has the potential to effect the reliability. To further complicate matters, the built-in-test techniques and fault tolerant approaches can significantly improve maintainability, but will alter the reliability of the device.

In spite of the difficulties in developing a realistic model, the impact of VHSIC on both system reliability and maintainability as well as the life cycle costs is anticipated to be considerable. All of the VHSIC vendors expect significant improvement, but few have specific data that allows them to document the impact of applying VHSIC technology.

Several of the vendors are projecting VHSIC chip level failure rates based on extrapolations from their existing data or from the application of MIL STD 217B. These projected failure rates[2,3,4] are as follows:

VENDOR	Number of Chip Types	Chip Complexity (in equiv. gates)	Anticipated Chip Failure Rate (Failures/hour)
Westinghouse	6	5,000 to 31,000	19.4×10^{-6}
IBM	1	38,000	3×10^{-6} ('84)
			$.3 \times 10^{-6}$ ('87)
			6×10^{-8} ('89)
Hughes	3	Based on a 300 gate CMOS/SOS chip operating at room temperature	6.92×10^{-12}
VHSIC Goal	-	-	6×10^{-8}

Note that the VHSIC goal is $6x10^{-8}$ failures per hour. The Hughes failure rate can probably be discounted because of the vehicle used (a 300 gate-gate array) to determine the failure rate. IBM is anticipating meeting the VHSIC goal of $6x10^{-8}$ failures per hour when the device is in limited production about 1988). The calculations used in the subsequent sections of this report assume three values for the VHSIC failure rate; the first is the Westinghouse figure of $20x10^{-6}$ failures per hour, the second is 10^{-6} failures per hour, and the third is the VHSIC goal of $6x10^{-8}$ failures per hour.

There are two components to the availability equation; reliability and maintainability. The equation can be simply expressed as follows:

$$\text{Availability} = A(t) = 1 - \frac{MTTR}{MTBF}$$

where, MTTR is the mean-time-to repair

and MTBF is the mean-time-between-failure.

Based on the above equation, if the MTTR goes to zero the availability goes to one, regardless of the MTBF. This makes the case for a redundant system, in that while the MTBF is a finite value when a failure does occur, the MTTR effectively is zero. The second figure shows the dependence of availability on both the MTTR value and the MTBF. This figure emphasizes the importance of minimizing the MTTR. The change, or delta, in availability when comparing an MTTR of 2 hours to an MTTR of 16 hours is over a factor of eight across an MTBF range of 500 to 2000 hours. This places a heavy emphasis on the requirement for board level and system level tests that ensure the process of recovering from a system failure is as rapid as possible. This means that diagnostics be applied that determine which of the field replacable units (FRU) has failed. Once the faulty FRU has been replaced (which should be no more complicated than a board removal with a subsequent insertion of the new board), a new set of diagnostics must be run to verify the correct system operation. The use of an in-system diagnostic processor is probably mandatory to ensure the MTTR is minimized.

Figure 3 illustrates the impact on availability resulting from the number of field replacable units. Note that a relatively high availability (.946) for a unit with an MTBF of 300 hours and an MTTR of 16 hours yields an availability of only .33 when 20 field replacable units are contained in

the system. Note also the importance of a reduced MTTR, since a system with a MTBF of 300 hours and a MTTR of 2 hours yields a higher availability than a system with an MTBF of 2000 hours and a MTTR of 16 hours. Figure 3 emphasizes the heavy dependency availability has on both the MTBF and the MTTR.

There are many missions, however, where the effective MTTR is extended because the repair can not be performed until the mission is completed. In this situation, the critical parameter is the MTBF. The fourth figure shows two sets of curves for the probability of mission success. This is based on a constant hazard model ($e^{-\lambda t}$) and assumes a serial reliability configuration. Again, note the strong dependency of mission success on the number of field replacable units contained in the system.

Indirect savings from the application of VLSI can provide significant benefits; specifically, it allows the size, weight and power requirements to be significantly reduced in most electronic based systems. Data indicated that in avionics applications, IC's account for approximately 2% of the avionic failures and only 1% of the total aircraft failures.(5)5 The same data indicates that such items as cabling and maintenance operations contribute approximately 85% of the total avionics failures. Use of the VHSIC chips can significantly reduce the support hardware (like cables) as well as providing for a self-test concept that will minimize failures that occur as a result of the maintenance approach. When VHSIC technology is applied, emphasis should be placed on redesigning both the logic implementation and the packaging to maximize the advantages of the VHSIC insertion. A "pin-for-pin" replacement of existing SSI/MSI/LSI parts with VHSIC equivalents will reduce the total IC part count but will not significantly reduce the packaging necessary to support this type of system implementation.

3.0 EXAMPLES

3.1 Specific Manufacturers Examples

All six Phase I contractors were contacted regarding the availability of both VHSIC chip reliability data and information regarding the impact of VHSIC technology insertion on equipment "life cycle costs." Several of the manufacturers were willing to quote projected reliability figures. As

indicated in the previous paragraphs, these figures converged to the VHSIC reliability goal of $6x10^{-8}$ failures per hours.

Westinghouse had some preliminary information regarding the insertion of VHSIC technology in an F-16 radar computer.(6) The data shown in figure 5 is compiled from the Westinghouse information and is based on the following three implementation scenarios;

1) An insertion of VHSIC chips (in this case, 8000 gate-gate arrays) into a logic configuration with the number of boards remaining constant, as compared to the baseline configuration, but with the total chip count being substantially reduced.
2) An insertion of the same VHSIC 8000 gate-gate array into a logic implementation that was reconfigured to maximize the use of the gate arrays while at the same time reducing the total board compliment.
3) An insertion of high density VHSIC chips (with an average per chip gate complexity of approximately 27,000 gates) into a logic implementation that was reconfigured to maximize the use of these high density chips and designed to minimize the board count. Some VHSIC gate arrays are included in this design.

It must be emphasized that the first two implementation scenarios use gate array chips, while the third scenario used both gate arrays and the higher density custom/semi-custom VLSI chips. Some of the specific information obtained from Westinghouse is summarized below:

Configuration	SSI/MSI/LSI IC Pack. Ct.	VHSIC Pack. Ct.	VHSIC Gate Array Pack. Ct.	Performance	MTBF
Baseline	6,000	-	-	X	330
Scenario #1	895	-	55	X	756
Scenario #2	917	-	33	1.25x to 2.3x	1311
Scenario #3	600	yes *	5	2.8x to 3.0x	2067

*Number of high-density
VHSIC chips used was not defined

Figure 5 shows the MTBF as a function of the package count for the "baseline" Westinghouse configuration and the three scenarios detailed above. Note the significant impact on MTBF when new packaging is used (the difference between scenario #1 and #2, yields almost a factor of two increase in MTBF. Additionally, from the previous chart and figure 5, not only does the MTBF increase as a result of the VHSIC insertion, but the performance increases up to a factor of 3.

It is apparent from this data that the system reliability is considerably enhanced when VHSIC technology is applied. The following chart projects the impact of this technology on both acquisition costs and field support costs. Again, this data was obtained from Westinghouse.

Configuration	Total Package Count	Performance	Acquisition Cost	Field Support Cost
Baseline	6,000	x	x	x
Scenario #1	950	x	x	.43x
Scenario #2	950	1.25x to 2.3x	.6x	.2x
Scenario #3	600	2.8x to 3.0x	.33x	.1x

VHSIC technology insertion demonstrates up to a factor of three reduction in the purchase price and up to a factor of 10 reduction in field support cost. Note that the significant reduction in field support cost is partially attributable to reducing the number of maintenance stages from three to two.

3.2 Potential Effects of VHSIC Insertion on System Implementation

Since many of the vendors were not able to provide hard data on both the failure rate numbers and the impact of VHSIC insertion on life cycle costs, we can postulate as to the potential benefits. The following paragraphs discuss several possible implementation scenarios and detail the impact of VHSIC insertion on the reliability of these hypothetical systems. The sixth figure is a summary of VHSIC chips and their approximate gate complexity from the six Phase I vendors. There are two comments to be made regarding the numbers in figure 6. The first comment is that the determination of the number of equivalent gates is at best a good estimate, with each vendor having their own algorithm for this estimation. In

addition, many of the chip designs are still in a state of flux and final determination of both the number of devices and the number of equivalent gates is not possible.

Nonetheless, we can generate, based on the numbers in figure 6, an estimated gate complexity for a VHSIC chip. This number calculated to be approximately 16,000 gates if the gate array chips are included, and approximately 20,000 equivalent gates without the gate array chips.

The effect of the "average" VHSIC chip on a system implementation can be calculated by assuming a percentage of the total system is integrated into the VHSIC chips. For figures 7 and 8, a hypothetical system implementation of 200,000 gates, 300,000 gates and 400,000 gates was chosen. The MTBF was calculated for a baseline system implementation using SSI/MSI/LSI parts that yielded an average of 60 gates per integrated circuit package. A wide range of failure rates are available for these parts [7,8]; the assumed failure rates and the distribution of the usage of SSI versus MSI versus LSI is summerized in the following chart.

Type	% of Utilization	Assumed Failure Rate (f/hr)
SSI	45	3×10^{-9}
MSI	45	30×10^{-9}
LSI	10	300×10^{-9}

These numbers yielded a composite failure rate of 45×10^{-9} failures per hour.

A VHSIC based MTBF was then calculated based on three failure rates, the first being the Westinghouse projected figures of 20×10^{-6} failures per hour, the second is 10^{-6} failures per hour, and the third is the VHSIC goal of 6×10^{-8} failures per hour. Note that this is greater than a factor of 300 in the spread of failure rate numbers. To calculate the projected VHSIC based system level MTBFs, the following assumptions were made:

1. The non-VHSIC (SSI, MSI, LSI) failure rate is approximately 17×10^{-9} failures per hour. It is assumed that a large percentage of the LSI components become a part of the VHSIC chips.
2. Figure 7 assumes 25% of the logic remains in SSI, MSI, and LSI.
3. Figure 8 assumes 10% of the logic remains in SSI, MSI, and LSI.
4. All memory intensive components are separate.
5. The non-VHSIC integrated circuit average gate density per package is 60.
6. The "average" VHSIC integrated circuit gate density per package was 20,000.

The results of these calculations are shown in figure 7 and figure 8. Note in both of these figures the advantage of using VHSIC technology when the failure rate is less than 20×10^{-6} failures per hour. Using this higher number generates an MTBF which is lower than the SSI/MSI LSI implemented system, although this high failure rate does yield a system MTBF close to those of the non-VHSIC implemented system. What must be emphasized is these calculations do not include the potential benefits to the system level MTBF by the reduction in the board count, cable requirements, connectors; etc. If calculations were to be performed detailing all the sytem level components of the VHSIC implemented system, even with a component level failure rate of 20×10^{-6} failures per hour, it would show a substantial improvement in MTBF compared to the non-VHSIC system.

4.0 CONCLUSIONS

The following items summarize our conclusions regarding the impact on system level reliability/availability resulting from the application of VHSIC technology.

1. Alhough specific system level implementation studies were limited to one contractor, the data obtained from this study showed a range in the MTBF inprovement from factors of 2.3 to 6.2 and an increase in system level performance that ranged

from a factor of 1.25 to a factor of 3.0. In addition, life cycle costs were significantly impacted by a factor of 3 reduction in acquisition cost and up to a factor of 10 decrease in field suport cost.

2. The study of the VHSIC technology insertion on the hypothetical system continuing up to 400,000 gates, yielded system level MTBFs that were, at worst, comparable to an identical system implemention using SSI/MSI/LSI components. If the VHSIC goal of $6x10^{-8}$ failures per hour is achieved, then very significant (a factor of 10 at the component level) increases in MTBF will be obtained. In addition, insertion of VHSIC technology should substantially reduce system level failures through the reduction of system support components such as cables, connectors, printed circuit boards, etc. The combination of the VHSIC failure rate goal of $6x10^{-8}$ and the potential reduction of system support components should yield at least an order of magnitude improvement in MTBF's when compared to the SSI/MSI/LSI implemented system.
3. System level availability is a function of both MTBF and MTTR. At the system level emphasis must be placed on reducing the MTTR to as low a number as possible. The mechanism for recovering from a system failure should include the application of system level diagnostics (through the use of a diagnostic processor), the identification of the failed field replacable unit (FRU), with the subsequent removable of the failed FRU and insertion of a new FRU. System level diagnostics must then be run to verify system level operation. MTTR should be measured in terms of minutes rather than hours.
4. It is apparent that the vendors are in the very early stages of the system application of these complex integrated circuits. As a result, little specific system implementation information, particularly with regard to life cycle costs, is available from the vendors.

RECOMMENDATIONS

1. Direct the early planning for VHSIC technology demonstration and insertion through incorporation of VHSIC requirements in the DSARC and the Service's system acquisition review procedures (SSARC) for the signal and data processing portions of systems entering development in or after FY84 and production after FY86. VHSIC planning in appropriate system R&D programs exceeding $10M and system production programs exceeding $100M should be required. R&M committee should produce list of systems for which this would apply.

2. VHSIC technology has the ability to offer greater subsystem Ai due to built-in-test and potential for fault tolerant designs. An examination of current operational systems should be performed to establish system level Ai data based on the use of VHSIC. This study could be effectively performed by mapping VHSIC technology onto the existing system level R&M case studies.

3. The Defense Science Board Summer Study on Operational Readiness with High Performance Systems stated that "the maintenance concepts for high performance systems have been force fit into maintenance and repair structures which are often not well matched to today's systems. One should design such a structure in the light of technology and performance of modern systems. The VHSIC technology has the potential to increase Ao by impacting the cost of operational system field support and possible elimination of a level of maintenance. It is recommended that a study be performed to quantify the impact of VHSIC on Ao. It should give due regard to factors such as personnel, training, spares, survivability, transportation, response time, etc. and develop alternatives to the current maintenance concepts for high performance systems. This study should be performed as part of the VHSIC Technology Insertion Program.

4. It is recommended that adequate VHSIC reliability should be demonstrated before actual insertion in operational systems. The integrated circuit Ai will be demonstrated in the VHSIC program. In addition, a reliability and maintenance demonstrator at the system level should be developed as part of the VHSIC Technology Insertion Program.

5.0 REFERENCES

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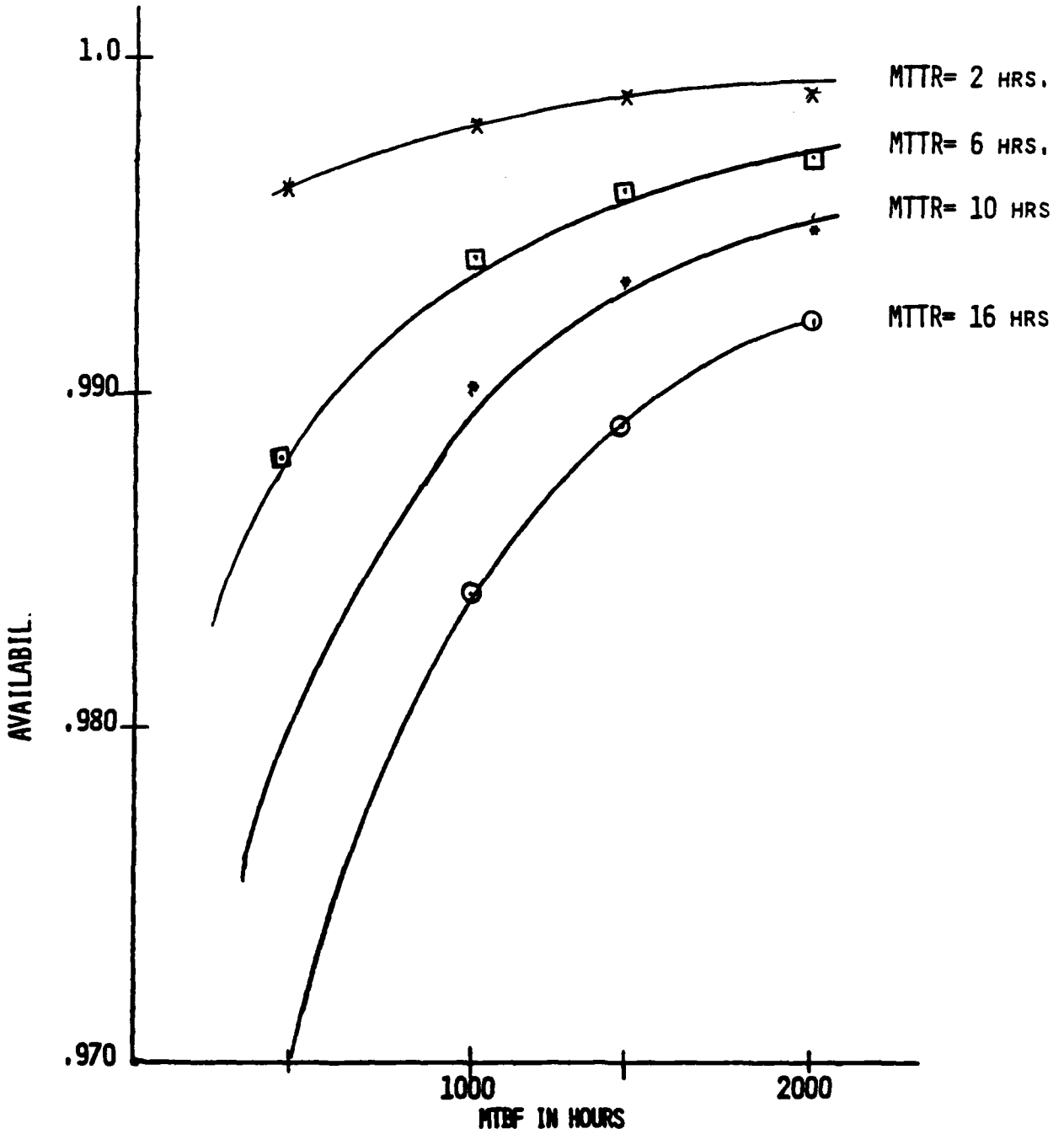
Contractor Service	Technology	Design Approach	Design Tools	Inter-connection Scheme	Packaging Technique	BIT/FT Approach
Honeywell (Air Force)	Bipolar ISL, CML	Custom-chip Based macrocell library	DAS (Unified Data Base) AIDA (Advanced integrated design automation)	Multiplier high speed lead bus & medium speed global bus	Multilayer ceramic carrier with beantape inter-connections	LSSD, signature analysis
Hughes (Army)	CMOS on SOS	Standard and custom reconfigurable chips	Hercules CAD data base	pipeline inter-connects	leaded ceramic flatpack, leads on 25 mil pitch	set/scan, signature analysis, redundancy
IBM (Navy)	NMOS	Master image with microcell library	VHD^{2}L (VHSIC Hardware design and description language) EDS engineering design system	pipeline on chip	single chip flexible film module package	LSSD, signature analysis, redundancy parity
Texas Instruments (Army)	Bipolar STL, NMOS	Programmable chip set	HDL, INTSIM (integrated simulator)	Multi-master synchronous parallel bus (S-bus)	JEDEC Type C leadless chip carrier	error correcting code, TMR
TRW/ Motorola (Navy)	Bipolar 3d TTL CMOS	Standard chip set	ADLIB/SABLE HSL-Hierachical Systems Language, multilevel database	V-bus inter connect (multiloop)	Ceramic Hermetic chip carrier, 132 edge chip attach	Set/Scan
Westinghouse	Bulk CMOS	Standard Cell	ISPS, LOGIC V, ASSIST, CABBAGE CALMA	Dual phase open drain bus and high speed ring net-work	leaded chip carrier with 25 mil pitch	RADSS (Scan/ set)

VHSIC Phase I Reliability - Related Approaches

FIGURE 1



AVAILABILITY VERSUS MTBF AS A FUNCTION OF MTTR

FIGURE 2

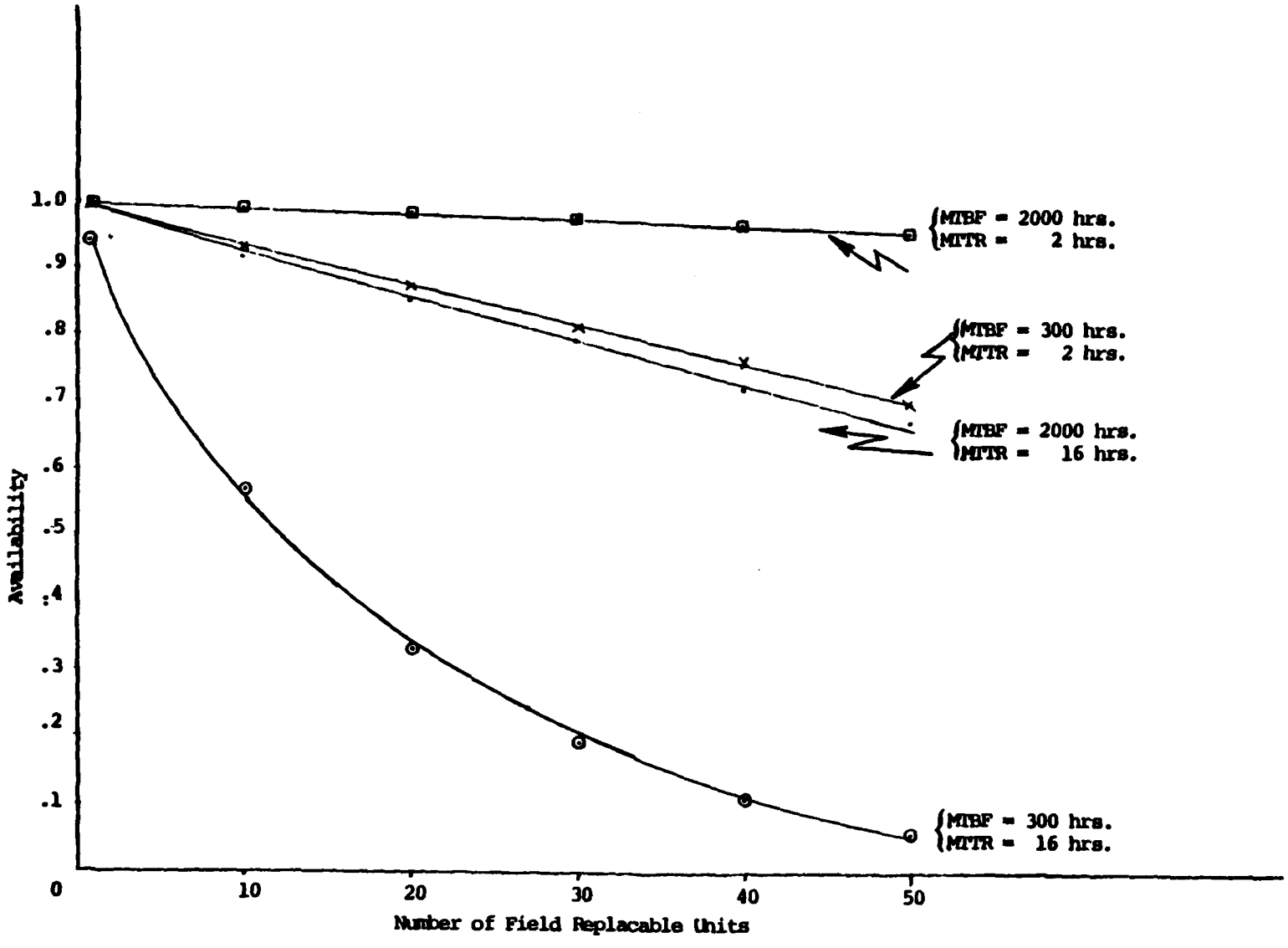
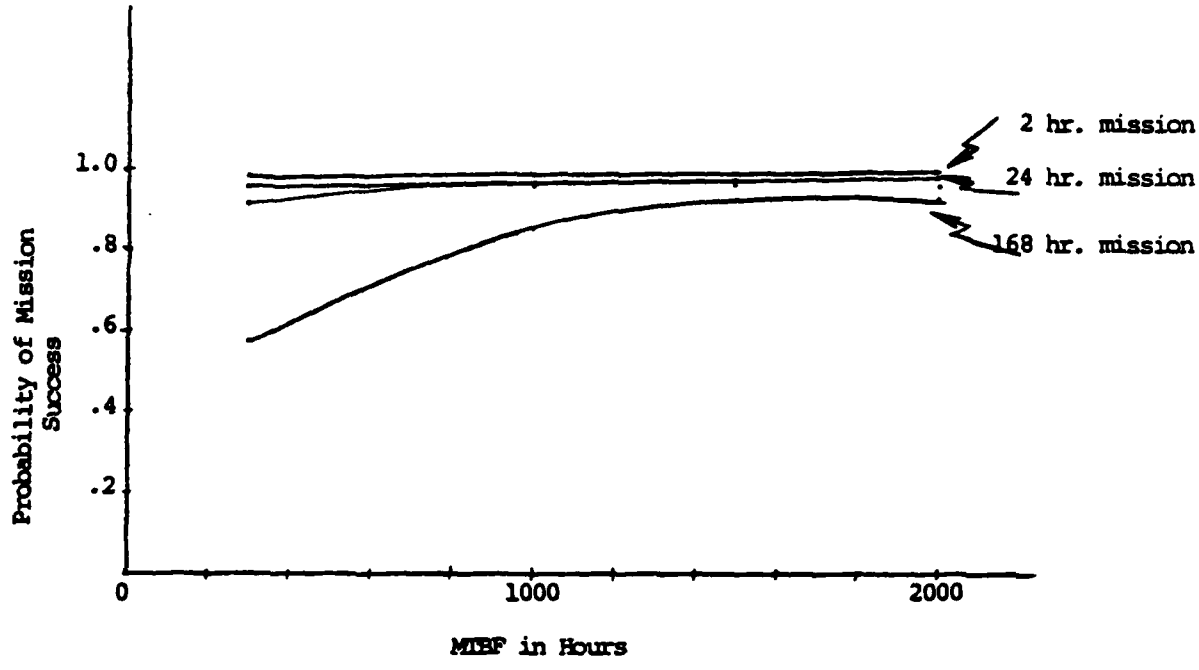


Figure 3
Availability Versus Number of Field Replacable Units as a Function of MTTR/MTBF



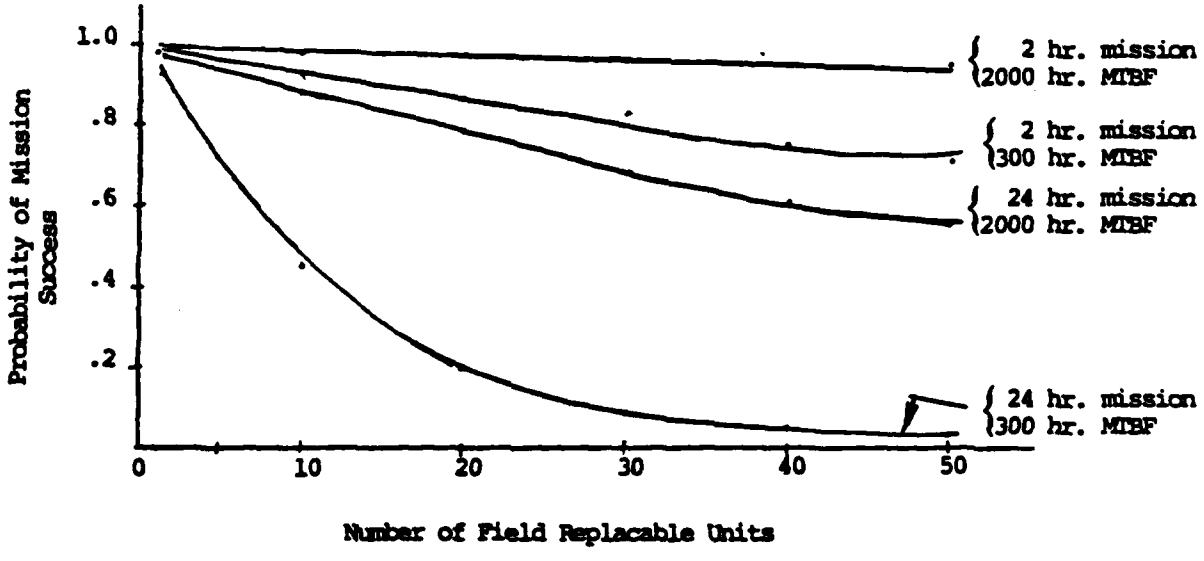
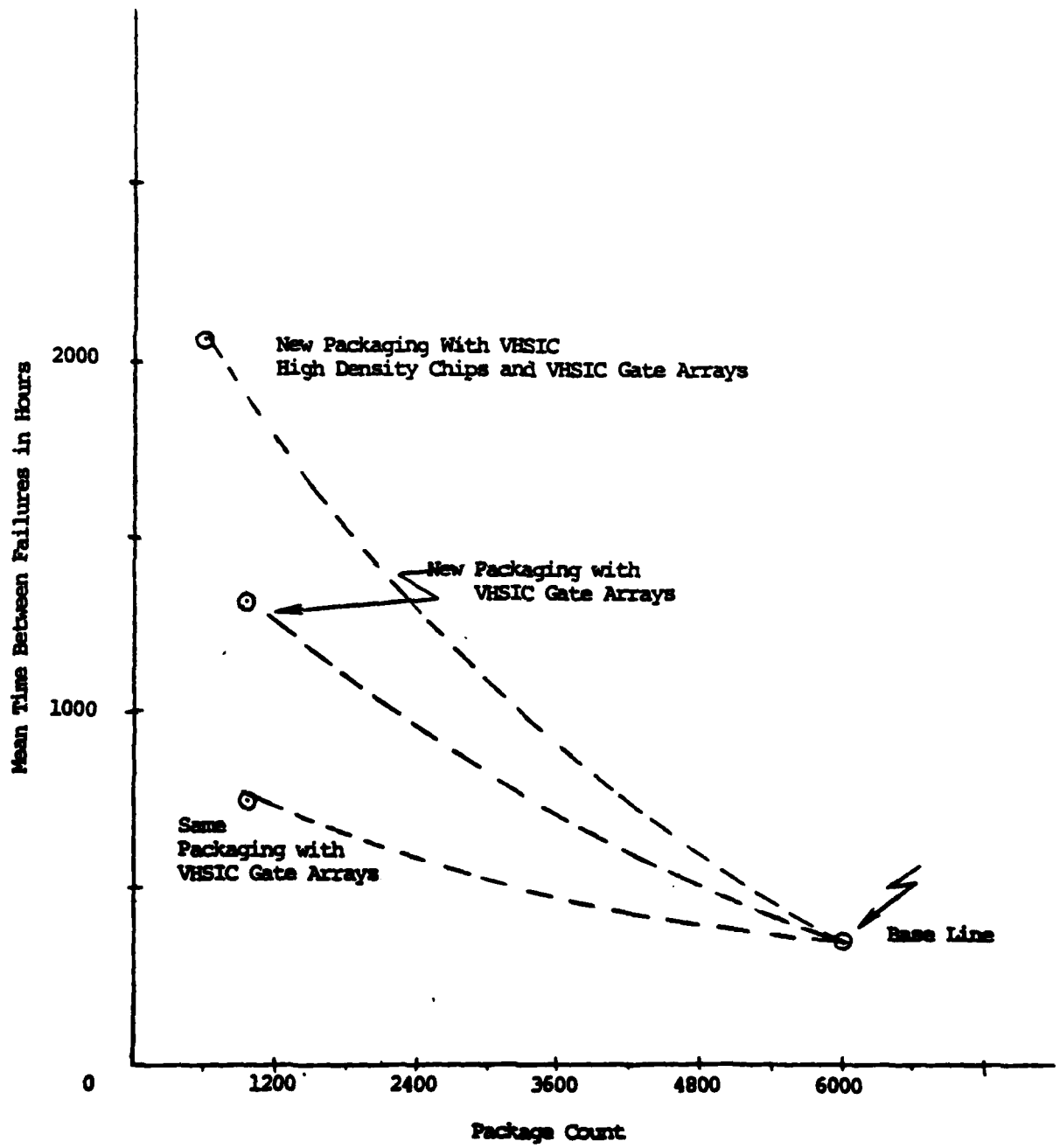


Figure 4

Probability of Mission Success Curves



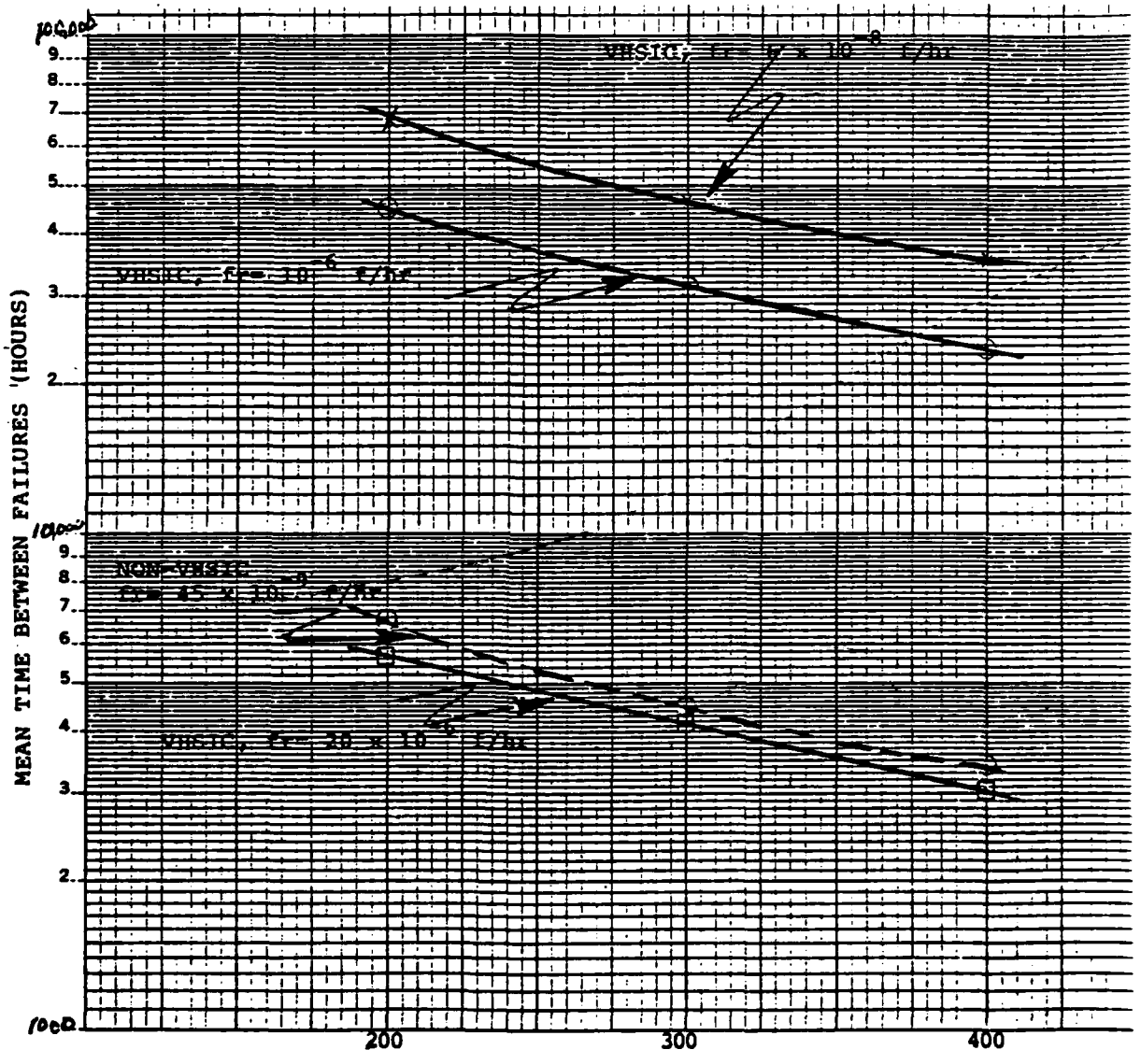
MTBF Versus Packaging for Westinghouse Data

Figure 5

Chip Type	Manufacturer	# of Devices	# of Equiv. Gates	# of I/O's	Comments
P^3	Honey.	117,000	11,500	160	10k bits of RAM
I/O CRTL	"	79,000	12,500	NA	
I/O CRTL	"	54,000	11,000	NA	
CORREL.	Hughes	97,300	24,300	124	
S^3	"	66,000	16,500	104	
ABD	"	59,700	14,900	25	
CMAC	IBM	NA	37,000	184	
GBU	TI	TBD	4,000	68	Gate Array
DPU	TI	TBD	10,000	84	Gate Array, with 52K ROM
DIU	"	TBD	10,000	84	" " " " "
ACS	"	TBD	10,000	68	" " " " "
VAG	"	TBD	10,000	68	" " " " "
VALU	"	TBD	14,300	84	Includes 96K of ROM
SR	"	TBD	NA	32	8Kx9 SRAM
MS	TI	TBD	4,000	108	Gate Array
WAM	TRW	48,000	16,000	113	
CAM	"	48,000	17,000	116	
FPM	"	90,000	NA	94	
AG	"	TBD	13,000	62	
PAU	West.	112,000	28,000	196	
ALU	"	90,000	22,500	196	
EXT-ALU	"	124,000	31,000	196	
CRTL.	"	120,000	30,000	204	
SCRAM	"	400,000	NA	52	
G.A.	"	20,000	5,000	120	Gate Array

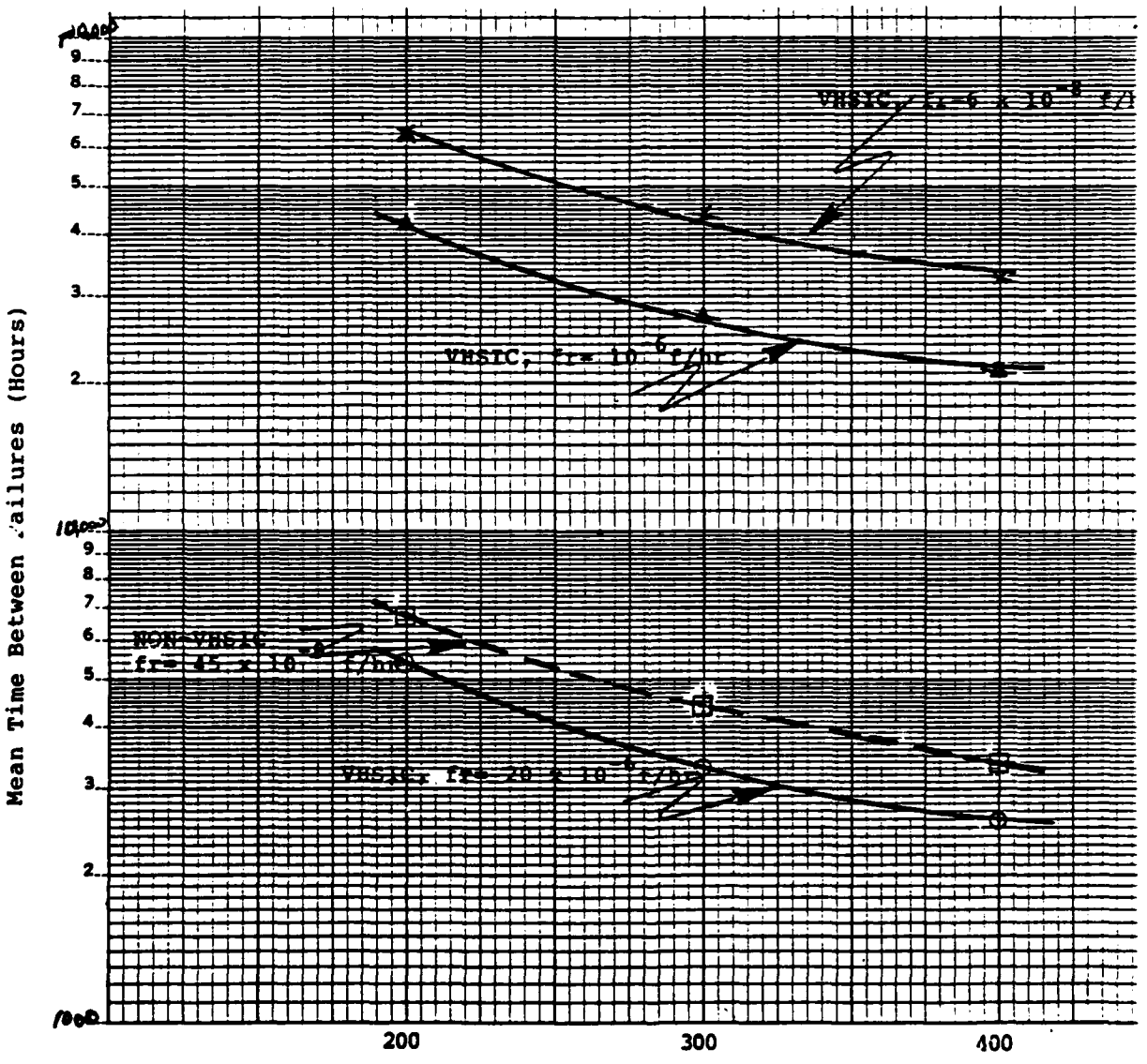
Parameter Summary of VHSIC Chips

FIGURE 6



MTBF VERSUS NUMBER OF GATES WITH 25% OF GATES IN SSI/MSI/LSI

FIGURE 7



Number of Gates (in thousands)
MTBF Versus Number of Gates with 10% of Gates in SSI/MSI/ LSI

FIGURE 8

The VLSI Connection in Two New Cooperative Research Programs

Jerry Werner, Editor-in-Chief

To counter increasingly threatening joint research programs abroad, two primarily U.S. programs; Semiconductor Research Corporation (SRC) and Microelectronics and Computer Technology Corporation (MCC), are moving into high gear. The SRC and MCC have many corporate members in common, but their focus and *modus operandi* are very different. Nevertheless, both deal with issues that vitally affect this country's ability to design and implement VLSI devices.

Both programs are responses to large-scale cooperative microelectronics and computer research and development efforts abroad, particularly in Japan, where the Ministry of International Trade and Industry (MITI) is sponsoring at least three such programs: 1) the Fifth-Generation Computer Program (Jones 1982), 2) the Supercomputer Program; and 3) the Next-Generation Industries Basic Technology Program (Werner 1982). These programs are designed to make Japan the leader in computers, telecommunication, and information processing by the end of this decade.

The SRC: Out of the Gate First

The SRC, a subsidiary of the Semiconductor Industry Association, is the more advanced of the two U.S. efforts. It was incorporated in late February 1982. To date, thirteen companies have joined the program (see Table 1), each paying at least the minimum annual membership fee of $50,000. (The fee is based on worldwide IC sales or, for captive producers, on equivalent IC production.) The SRC's budget, an expected $6 million in 1982 and $10 to $11 million in 1983, will fund research efforts in universities, in the form of individual grants or else by establishing "centers of excellence."

In May 1982, Larry Sumney (Figure 1) left the directorship of the Department of Defense's VHSIC Program to become the executive director of the SRC. Shortly thereafter, North Carolina's Research Triangle Park was chosen as the site of the SRC's headquarters; and Richard D. Alberts and Dr. Robert M. Burger were hired as assistant directors of operations and research programs, respectively. Both had previously held posts at the Research Triangle Institute (RTI), and had worked with Sumney on the VHSIC effort.

In October 1982, a request went out for proposals regarding innovative VLSI research concepts. At this writing, the SRC has received 166 responses from over 60 universities throughout the country. On November 16, 1982 the first awards were announced (see Table 2).

The individual SRC awards are for "contracted research, not grants," says Erich Bloch, vice president of technical personnel development at IBM, and chairman of the SRC board (see Figure 1). That research will typically be high-risk, but will have a high potential return. For example, Prof. Brooks and his colleagues at the University of North Carolina will try to transport the so-called "Parnas methodology" from the software development realm to the hardware (IC) one. The Parnas methodology lets a system be broken down into modules, using what Brooks calls "information hiding."

In addition to the individual awards, the SRC recently announced two research centers of excellence. The computer-

Company	Member of the SRC	Expected to join at least one MCC Program
Advanced Micro Devices	X	X
Burroughs		X
Control Data	X	X
Digital Equipment	X	X
E-Systems	X	
General Instrument	X	
Harris	*	X
Hewlett-Packard	X	
Honeywell	X	X
IBM	X	
Intel	X	
Monolithic Memories	X	
Mostek		X
Motorola	X	X
National Semiconductor	X	X
NCR	*	X
RCA		X
Silicon Systems	X	
Sperry Univac		X
Westinghouse	*	X

Notes: 1. * = considering membership.
2. Companies shown in blue are expected to participate in *both* efforts.

TABLE 1. Companies participating in the SRC and the MCC.

Subject of Award	Funding	Recipient
"Performance Enhancement of VLSI Through the Use of Advanced Coding Techniques"	$116,506	Prof. F. Pease, Stanford University
"Low-Resistance Ohmic Contacts for VLSI Technology"	$ 73,000	Prof. G. Robinson, Univ. of Minnesota
"Investigation of Multilevel Interconnection and Reactive Ion-Beam Source for VLSI Applications"	$109,815	Prof. T. Wade, Mississippi State University
Transfer of Software Methodology to VLSI Design"	$ 80,475	Prof. F. Brooks, Univ. of N. Carolina
"Thermal and Accelerated Dopant/ Surface Interactions During Vapor-Phase Growth in VLSI Device Fabrication"	$ 99,973	Prof. J. Greene, Univ. of Illinois

TABLE 2. The initial SRC awards.

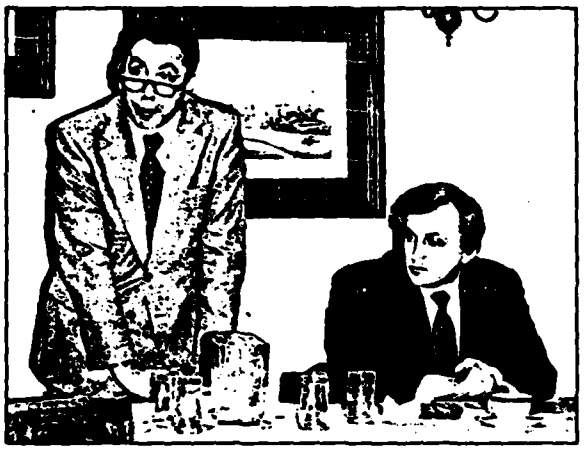


FIGURE 1. Erich Bloch (standing) and Larry Sumney outline the plans for the SRC.

aided design center, with first-year funding of $1.75 million, will be a joint effort between the University of California at Berkeley and Carnegie-Mellon University (Pittsburgh, PA). Although the plans for the CAD "center of excellence" are still in the early stages, U.C. Berkeley is expected to concentrate on the development of integrated design systems and stations. Those tools will be strongly influenced by ongoing IC design projects at the university, and include a heavy emphasis on simulation (process/circuit/logic/functional) and design verification. CMU is also developing an integrated design system, with an emphasis on the theoretical aspects of design synthesis (adding detail as designs proceed to lower hierarchical levels) and statistical process simulation.

The micro-science and technology center, with first-year funding of just under $1 million, will be at Cornell University. Cornell is also the site of the National Research and Resource Facility for Submicron Structures (NRRFSS), funded by the National Science Foundation. (See "University Scene" in the May/June 1982 issue of *VLSI DESIGN*.)

The SRC has the dual goals of expanding the generic base of knowledge in eight "major thrust areas" related to industry's needs (see Figure 2), and of producing more university graduates trained in microelectronics specialties, via funding for both professors and graduate students. Because SRC members range from little Silicon Systems ($16 million) to computer giant IBM ($26 billion), it's clear that not all the companies have joined for the same reasons. "We have a mixed set of SRC participants," acknowledges assistant director Burger. "The larger corporations, with substantial internal research programs, are more interested in long-range, more academic, wide-ranging research topics. Other of our members are more interested in university programs oriented towards today's problems." He says that research into synthetic lattices and extremely small devices are in the former category, whereas CAD research and work on low-resistance interconnects and contacts are in the latter group.

MCC: Conducting Research In-House

In contrast with the SRC, the Microelectronics and Computer Technology Corporation (MCC)—once operational—plans to support research that the MCC itself will do, *not* via independent research contracts with universities. (However, some grants may go to universities—especially in the field of artificial intelligence.) The MCC is the brainchild of Control Data Corporation chairman William C. Norris who, early in 1981, first proposed the idea of a joint R&D venture to help medium-sized firms stay competitive with IBM and with "Japan, Inc." Since then, discussions have continued among CDC and 16 other companies (see Table 1). MCC was incorporated on August 12, 1982, and task forces have been set up to zero in on four technology programs (as shown in Figure 2): microelectronics packaging, electronic computer-aided design and computer-aided manufacturing (CAD/CAM), advanced computer architecture (informally called the "Alpha-Omega Program"), and software productivity. The proposed goals of the four MCC programs are summarized below.

Microelectronics Packaging

As presently planned, this program calls for the accomplishment of five specific tasks:

1. *Development of a hermetic die* that, because of its passivation and bonding-pad preparation, can resist exposure to extreme environmental conditions without requiring an outside hermetically sealed package. This work would also address the bonding method, which is expected to be similar to IBM's solder bump/reflow technique.
2. *Development of the equipment* necessary to automate the process, from preparation of the die to attachment of the die to a substrate.
3. *Investigation into device (die) encapsulation* including ways to improve thermal conductivity between a die and the outside world.
4. *Development of a high-density substrate* that would allow interconnection of several die with 250 input/output pads per square inch. The power-dissipation goal is 10 watts/in^2.
5. *Demonstration of the packaging schemes via an overall system-test vehicle*. This test vehicle would be determined "a couple years down the line," according to Marshall Andrews, manager of package and assembly engineering for Harris Semiconductor Division, and the leader of MCC's packaging task force. Once built, the system-test vehicle would be subjected to environmental extremes and long-term life-cycling.

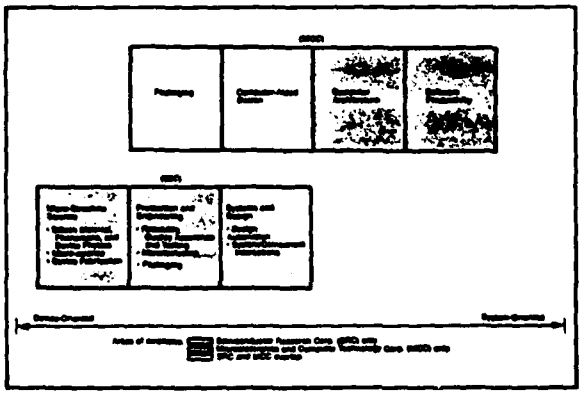


FIGURE 2. The SRC, a subsidiary of the Semiconductor Industry Association, is device-oriented, whereas the MCC is computer-system oriented. However, some areas do overlap.

COST MODELING ACROSS INTERCONNECTION LEVELS

by

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Introduction

While solutions to electronic interconnection problems require sophisticated techniques and components, their effectiveness has not been measured quantitatively. This paper presents a method for doing so.

This method is based on so-called interconnection reduction ratios, IRR, which characterize the effectiveness of an interconnection method or component. These measures were used in the past in unpublished reports and special presentations. This paper is not only the first general presentation on this topic, but also the first time the cost of interconnection is brought into the model.

The quantitative treatment of this topic affords a number of possibilities:

.. provides the rationale for some interconnection trends observed in the past,
.. points the direction of fruitful developments,
.. indicates relative market trends of various interconnection schemes.

We will define the concept of IRR, apply it to generalized interconnection components, develop some optimization rules and show how cost considerations can be applied to this methodology.

Basic Concept

The basic elements of an electronic system are transistors, diodes, resistors, capacitors, inductors, etc. Most of these elements have two or three terminals, although some (such as transformers) may have more.

A piece of electronic equipment - such as a minicomputer CPU - contains hundreds of thousands of these elements with a correspondingly even larger number of these terminals to interconnect. Yet, the wires leading to and from the unit number only in the hundreds.

Therefore, this electronic package reduced the total number of elemental terminals from many 100,000's to a few 100's. The ratio of these two numbers is defined as the *interconnection reduction ratio, IRR,* and is the measure of the effectiveness of interconnection for that electronic system.

Interconnection Levels

In going from the elemental components' terminals to the external connectors of the electronic black box, several levels of interconnection are passed through:

- *Level 0* - This is the metalization layer and polysilicon pattern on the integrated circuit chip. The IRR of a discrete chip is 1 (no reduction), while that of a TTL may be 25 (say, 20 gates, each containing six transistors, each transistor having three terminals; a total of 360 elemental terminals divided by 14 chip pads). An LSI chip may have an IRR of 400, while a 64k dynamic RAM calculates out to some 15,000.

- *Level 1* - This is the component package, the connection from the chip pads to the external package leads. In most cases this is a one-to-one connection (IRR = 1) except in the case of hybrids where the terminals of several chips are interconnected to fewer outside leads. Typical hybrid IRR's range from three to 20.

- *Level 2* - This is the printed wiring board level. The total lead count for all components or packages mounted divided by the total number of input-output fingers and/or leader contacts gives

the IRR. If all components are inserted and if only edge connectors are used, the PWB's IRR is the fraction of plated-through holes divided by the fingers. A medium-size commercial board may have an IRR of five to 15. The use of chip carriers would increase IRR, while hybrid packages would generally reduce it.

- *Level 3* - This is the motherboard or backplane. All the terminations of the daughter boards would be divided by the cabling leading away from the motherboard to get the IRR of this interconnection level. Typical IRR's may range from six to twelve.

- *Level 4* - This is the connection from the motherboard(s) to the external plug(s) of the system. If the connection is direct, the IRR is unity. If there is a junction box or equivalent, the IRR is larger.

Product Rule

To start with an example, assume that Level 2 (the printed wiring board) reduced the terminations by a factor of 12 ($IRR_2 = 12$) and Level 3 (the motherboard) reduced them by a factor of 5 ($IRR_3 = 5$), then the two levels together achieved a reduction of 60; in other words

$$R_{23} = R_2 . R_3 \qquad (1)$$

where the symbol IRR is replaced by R (ratio) to shorten the equation. For a total system, which has levels 0 to 4

$$R_{system} = R_{04} = R_0 . R_1 . R_2 . R_3 . R_4 \qquad (2)$$

The product rule is: *the IRR* (interconnection reduction ratio) *for a system equals the product of IRR's of the individual levels.*

Even Distribution

If interconnection reduction ratios were equally easy to achieve at any level, then the most efficient distribution of reductions would be even; that is, the IRR for any level would be the same. (The proof of this is not shown).

The total system IRR is defined by the circuit design requirement. To carry out the required logic or other circuit function, a certain number of transistor, diode, resistor, etc. elements are required. This defines the number of *starting terminations.*

Similarly, the function of the system or black box defines the number of external lines or *ending terminations* required. But

$$R_{system} = \frac{\text{starting terminations}}{\text{ending terminations}} \qquad (3)$$

Thus, the overall reduction ratio is defined by system design and requirement.

Even distribution means that

$$R_{\text{each level}} = \sqrt[5]{R_{system}} \qquad (4)$$

or

$$R_j = \sqrt[5]{R_{04}}, \quad j = 0, 1, \ldots 4. \qquad (5)$$

As an example, let the starting terminations be 1.5 million and the ending terminations 180. This gives a system IRR of approximately 8,300. The fifth root of this is about 6, so that even distribution would require each level to provide the relatively modest reduction of 6 only.

Suppose now that one level does not provide its reduction share; say, no reduction or an IRR=1. Then, the others would have to raise their IRR from 6 to the fourth root of 8,300 or nearly 10 in order to still achieve the same overall system IRR.

Now, if two levels did not do their share (IRR's of unity), then the remaining three levels would have to raise their IRR's to over 20 each (the third root of 8,300).

Differences in Interconnection Levels

Examples

In a practical situation the IRR's vary greatly from level to level. Three examples of different

Level	Analog	Computer	Military
0	60	300	150
1	1	1	10
2	8	15	25
3	5	8	15
4	4	6	8
Total	11,520	216,000	4,500,000

examples in the difference between Levels 0 and 1. Although the IRR's are expected to continue to increase at all levels, the disparity between Level 0 and the other levels will also.

Chip Level Integration

Level 0, the on-chip wiring, is the manifestation of the integration trend. It can be explained only by consideration of cost, which is twofold: the low cost of making a connection on the chip and the saving of cost at other levels as a consequence.

Because of batch fabrication - a waferful of circuits at a time - and miniaturization techniques the cost of making a connection at chip level can be incredibly low and shows every sign of becoming even lower. We are nowhere near reaching a limit.

Furthermore, making a connection at a lower level saves us the trouble of making some connections at a higher level. A Level-0 connection saves some connection cost at the higher levels; it saves some of the component package, some circuit board space, and so on.

Package Level

We see, therefore, that cost considerations make a very good argument for chip-level integration. But many of the same arguments also apply to Level 1 to some degree; why then did the industry do so little to increase the IRR of this level? In other words, why are there so few hybrid and multichip packages?

One reason we offer is that hybrid technology was first conceived of as a competitor to chip-level integration, a contest it could not win. With both chip-level and package-level integration largely under the preview of semiconductor companies, there was little incentive to assign substantial development funds and scarce engineering talent to the advancement of hybrid technology in preference to LSI.

Notice that this was not the case in companies whose work and control bridged all five levels, specifically IBM and Western Electric. Thus, OEM's which built their own semiconductor components found it advantageous to utilize Level 1 for effective interconnection. With the number of OEM's having in-house wafer fabrication increasing, we can expect to see a moderate resurgence of interest in hybrid and multichip packages.

Hybrid technology as an interconnection scheme has much better justification than as an integration scheme.

Chip Carriers

Where do chip carriers come in? They have two roles. One is a true Level-1 replacement of DIP's when mounted or socketed directly on printed wiring boards. In the other role they are mounted on intermediate ceramic substrates which in turn is mounted on printed-wiring boards.

In the first role they do exactly what our interconnection "theory" suggests: help even the distribution of IRR among levels. In this case, by offering more leads than DIP's, chip carriers reduce IRR_0 and by forcing a denser lead layout onto the PWB, they put more pressure on increasing IRR_2. But, they do not change IRR_1, which stays unity or less (in case of unused leads) just as DIP's do.

In the other configuration, the chip carriers are first mounted on ceramic substrates, which in turn are mounted on the PWB. This really establishes an added interconnection level between Level 1

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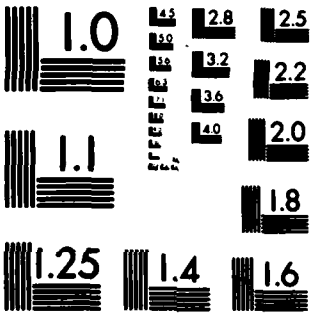

(chip-carrier) and Level 2 (PWB). In a flash of inventiveness, we will name this ceramic assembly Level 1.5, and proceed to mourn the passing of our elegant integer model.

The intermediate substrate strongly resembles a hybrid substrate and provides an IRR comparable to high density PWB's. It also removes some of the pressure on the PWB, which need not be as high in density and IRR.

Printed Wiring Boards

As the complexity and density of boards increases, their cost per square-inch also does. But the number of interconnection increases even more so that the cost per interconnection goes down. This is really the basis of including cost in our quantified comparisons.

Cost of Interconnection

Level 0

For a semiconductor design engineer the advent of LSI and VLSI are marvelous achievements of process development and ingenious innovations. For a packaging engineer they are simply advanced interconnection techniques. At this interconnection level typical IRR's range as follows:

Discrete chip	IRR = 1
TTL logic	25
LSI	400
VLSI	3,000
64k RAM	15,000

With these kinds of interconnection efficiency, it is not surprising that VLSI is a wide-ranging objective. The reason it is not used exclusively is cost, which varies greatly.

Design cost of VLSI runs into the $100,000's if not millions of dollars, so that large production volumes are needed to amortize the design cost. But with more circuitry per chip, the number made for each type generally diminishes.

We made some calculation of the approximate cost (K) of making a connection (so to say laying a wire) in each case, and then multiplied this by the IRR (or R for brevity). The resulting products "RK; we avoided C for cost so we do not get RC products) a more consistent pattern of comparison. Thus

Chip Type	R	K	RK
Discrete	1	.83	.83
TTL	25	.025	.63
LSI	400	.008	3.20
VLSI	3,000	.005	15.00
64k RAM	15,000	.0007	10.00

In the product RK we start to develop a more indicative figure of merit. This is borne out as we look at the other levels.

Other Levels

Some values for typical examples are listed in the following table:

Level	Item	R	K	RK
1	Plastic DIP	1	.5	.5
1	CerDIP	1	1.2	1.2
1	Simple Hybrid	3	2.7	8.1
1	Complex hybrid	5	1.5	7.5
2	Double-Sided	10	.5	5.0
2	Four-layer	13	.8	10.0
2	Multilayer	20	.7	14.0
3	Motherboard	6	2.2	12.0
3	Backplane	12	1.5	18.0

The RK products are empirical and we cannot prove that they are a rigorous figure of merit for t economic comparison of interconnections. But we can say that RK includes a cost consideration and puts in perspective the value of interconnection reduction ratio.

A few rationalizations can be made:

.. The cost of discretes and TTL's has been reduced so much that their useful life has been extended.
.. The travel toward VLSI will continue as long as the cost per element and per interconnection can be decreased.
.. The dual-in-line packages should continue to have a long life because of their cost effectiveness even though their IRR is unity.
.. Hybrid and multichip techniques may have reached a point of development where their broader use is logical.
.. Advances in computer-aided design (CAD) will make customized VLSI cost-effective.

Summary

The concept of interconnection reduction ratio (IRR) quantifies the effectiveness of interconnection products. It provides a new way of looking at the roles of and trends in LSI, hybrids, device packages, printed circuits and other interconnecting means.

Introduction of interconnection costs and combining them with IRR's give a very stable figure o merit, suggesting a possibly fruitful basis of analyzing trade-offs among the various interconnecti levels. The quantitative tools presented provide a useful perspective of electronic packaging. Further refinements of the methodology will provide added analytical tools for comparing the effectiveness of electronic interconnection methods and systems.

An Overview of the VHSIC Program and Packaging Needs

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Introduction

Electronics has played an increasing role in the development of military equipment as the technology progressed from vacuum tube capabilities through the transistor and more recently the integrated circuit. With further anticipated advancements, microelectronics (by integrated subsystem or system development) will become the cornerstone of the next generation of military equipment. An area that DOD is concentrating on, and which will probably play a significant part in this technology advancement, is the VHSIC program.

Under the VHSIC (Very High Speed Integrated Circuit) program, a new generation of integrated circuits (or systems) are being developed for real time signal processors. The program's intent is to meet both present and future military electronic system needs, and to assist in establishing increased domestic manufacturing capabilities to respond more readily to the Military's expanding system requirements for rapid collection, analysis and dissemination of battlefield information, and for effective weapons control through the high speed signal processors. Hundreds of millions of instructions per second capabilities, in the smallest size and weight tactical computers, are needed to solve the operational problems of fielded systems.[1,2]

VHSIC is being carried out by the 3 Military Services (Army, Navy, Air Force) with overall planning and coordination by the DOD (OUSDRE). The program is divided presently into 3 phases: 1, 2, and 3. A program definition phase (Phase O) which entailed analyses, partitioning studies, system architecture, chip architecture and design, design layouts and CAD modeling of various weapon systems designed for VHSIC, was completed in December, 1980. Building demonstration systems is the goal of the present Phase 1 (1981-1984) and the subsequent Phase 2.

Phases 1 and 2

Construction of an electronic brassboard system by each of the six Phase 1 contractors (Honeywell, Hughes, IBM, TI, TRW and Westinghouse) necessitates an evolution in the technology for integrated circuit signal processing, the chips to be in the order of 10 to 100 times more complex than the LSI and VLSI as used today. Under Phase 1, the chip must provide a functional throughput rate (FTR) capability (gates per chip x rates at which operations are performed) of 5×10^{11} gate-Hz/cm^2 with a minimum clock rate of 25 MHz. For Phase 2, the FTR rises to 10^{13} with an increase in clock rate to 100 MHz. One of the most sophisticated consumer microprocessors developed has a FTR of 5.3×10^{11} with a clock rate of 11 MHz, essentially one half the VHSIC Phase 1 speed requirement.[3] Another recent VLSI design, considered a "landmark", resulted in the fabrication of 430,000 transistors on about 40 mm^2 for a packing density of over 1,000,000 FETS/cm^2 on a single chip "micromain frame", and a FTR of 6×10^{12}, exceeding the goal set for Phase 1.[4] In addition to increasing chip size, the required speed and circuit density for VHSIC necessitate scaling down circuit configurations by enhancing lithography capability from present 3.0 to 1.25 um feature sizes under Phase 1 and further reduction to submicrometer feature sizes (0.5 to 0.8 um) under Phase 2. Under both Phases 1 and 2, the contractors will have to establish pilot lines to demonstrate production of the required functioning systems with the small feature sizes.

Phase 3

Phase 3 consists of a multiplicity of VHSIC support programs and is being conducted in parallel with the overall program by various contractors including semiconductor, communication, and military system companies, plus universities and research institutes. The placing of hundreds of thousands of gates in a single chip creates formidable technology and design problems. Phase 3 has been structured to provide a wide range of research and development efforts on various VHSIC related and specialized technologies and design concepts to support Phases 1 and 2. Between 50 and 60 contracts have been awarded. Key technology problems include

development of new lithography methods capable of submicrometer exposures and growth of low defect silicon substrates. Key design thrusts include development of new structures for high speed processing, innovative architectural and design concepts for improving performance and increasing packing density, new testing concepts, use of new semicustom designs to permit wide usage of a specific chip by various military systems users, and development of software for design and chip operation. As the program proceeds, new efforts will probably address those technical problem areas which continue to be common to the Phase 1 contractors, such as hardware description language, reliability, test and fault tolerance, environmental tolerance and vulnerability reduction, and packaging techniques.

Chip Technology and Design

VHSIC implies large digital integrated circuits or systems with typical logic-gate propagation delays in the order of one (1) nanosecond or lower[5]. Silicon (Si) and gallium arsenide (GaAs) are used for fabricating integrated circuits with high speed requirements. The fastest commercial IC logic is a silicon bipolar ECL series with typical delays of 700 ps at 30 mW, although delays as low as 300–400 ps have been demonstrated at power levels of a few mW per gate. Commercial silicon MOS propagation delays are a few nanoseconds and delays as low as 230 ps for minimally loaded NMOS gates have been published. In contrast GaAs with propagation delays ranging down to less than 50 ps are being developed to achieve higher speed operating devices.[6] For VHSIC, the decision was made to pursue the silicon technologies essentially because of the maturity of both the silicon material and its digital IC technology, as compared with GaAs. Efforts are underway, however, to develop GaAs bipolar structures and gate arrays under support from DARPA (Defense Advanced Research Projects Agency).

A variety of silicon technologies and several chip design approaches are being used to meet the chip applications in the brassboards. The silicon technologies selected include bipolar (ISL, CML, CSSL), CMOS/SOS, NMOS, bipolar STL, triple diffused bipolar and bulk CMOS. Design approaches include customized macrocell architecture in which specific macrocells are interconnected for specific functions; a programmable chip set architecture or gate array configuration where custom functions may be achieved by chip surface interconnection schemes; and by alternative chip sets where each chip is designed to perform a single or set of functions. The latter can provide for higher circuit density in comparison to the first two approaches, whereas the first two provide for shorter chip development cycles. The number of chip types being developed by each of the six Phase 1 contractors vary between 2 and 8; however the number of chips per VHSIC set for the brassboards vary between 4 up to approximately 6300, the latter a memory intensive design.

Technology Insertion

Each of the brassboards of the six Phase 1 contractors is intended for insertion into and upgrading of existing military systems and for new systems that will require the use of VHSIC technology. The brassboard categories include electro-optical, anti-jam communication, acoustic, multi-mode fire and forget, electronic warfare and airborne radar processors. A number of Army systems for VHSIC insertion include the TOW missile; the PLRS (Position Locating Reporting System) user units, a part of the Battlefield Information Distribution System (BIDS), which must be capable of high capacity, real time and jam resistant digital data interchange for large numbers of ground units; the M-1 Tank fire control system, where electronics are required for improved automatic tracking through increase in real time operations from present 200,000 operations/second to several millions of operations/second; and the Advanced Quicklook, a high mobility integrated electronic communication and intelligence gathering system.[7] Other new systems include advanced target acquisition and fire control with electro-optical processors, and the military computer for automation on the battlefield for weapon systems control, command and control, equipment control, communications and combat support services.[8]

Packaging - Background

Packaging provides mechanical and environmental protection for the integrated circuits and includes bonding areas between the circuit and package leads. The packages are mounted normally onto boards which are combined in a form of modular construction on a chassis for ease of assembly and maintenance. This type design will remain for VHSIC Phase 1 packaging, although changes will take place in most device packages because of the relatively large size chips and their large number of pads.

The dual-in-line package (DIP) emerged as the major configuration in the mid 1960's and is still the major form of individual integrated circuit packaging. The increasing demand for high density packaging has been met by efficient mountings of DIPs onto complex multilayered boards, and, to a degree, by the use of hybrid microcircuit design and fabrication. As LSI and VLSI are developed, the DIPs and related type packages required for these larger and more complex integrated circuits, are occupying excessive board area and

interfering with higher operating speeds due to various parasitic effects including resistance of the extended lines (within and between packages), lead inductance and capacitance. The fabrication of VLSI chips has indicated two of its major problem areas as interconnection between chips and packaging (managing off chip connections and the heat generated). Within a CPU, two thirds of the signal delay, on the average, can occur between chips. Hybrid multilayered configurations have been used for such applications where the increased integrated circuit (bare chip) packing density permits higher speeds.[9,10]

The inefficiency of the DIP as a package for LSI and VLSI circuits has led to increased development of the chip carrier and pin grid array package (introduced in the early 1970's and 1960's, respectively), each a high volume device package. In contrast to the DIP, both are generally square packages (DIPs are rectangular). The chip carrier has terminals on the perimeter (the DIP uses 2 sides only), while the pin grid array has a matrix of terminals on the bottom of the package. Both types occupy less surface and provide more terminals than the DIP in a typical mounting arrangement.[11] The increasing usage of both configurations is due, to a large degree, to the package standardization efforts of JEDEC (Joint Electron Device Engineering Council) JC-11.3.1 Task Group.

VHSIC Package Needs

The VHSIC chips being developed under Phase 1 vary in size from 220 up to 360 mils on a side (31 up to 84 mm^2), and the number of pads per chips range from 84 up to 244. Connections from chip to package will be by wire bonding, by tape bonding, and by a "Decal" approach, a flexible thin (0.3 mil) polyimide film with 8 um of copper. The power consumption will range from 0.7 up to 3.0 watts per chip. In selecting package designs, the contractors are tending to follow the package standards that either have been established or are being developed by JEDEC, i.e., chip carriers with 40 and 50 mil centers (established), and chip carriers with 20 and 25 mil centers and 100 mil pin grid array packages (to be developed). Four (4) of the Phase 1 contractors are using chip carrier type package designs with one (1) being able to satisfy his requirements with a JEDEC standard chip carrier (84 terminals with 50 mil centers). The other three (3) are developing 132, 148, 156 and 220 terminal carriers with center to center spacings of 16.67 and 25 mils. The remaining two (2) contractors are using pin grid array configurations with either 5 or 6 conductive layers and 180 and 240 pins with 100 mil centers. One contractor will use an alumina board for ceramic carrier surface mounting whereas all the others will probably use epoxy type PC boards for flexible lead or pin mounting. Thermal management will include conduction cooling, heat dissipation by a thermal plane, and airflow over a heat sink.

Packaging and Related Problems

As the VHSIC chips increase in size and achieve the high circuit density and speed planned, there is, as noted, the corresponding demand for improvement in interconnection and packaging. The increase in logic elements results in more pads per chips and the corresponding need for space efficient packages with more terminals, necessitating an increase in interconnection density both on and between chips. Such capabilities are undeveloped today for general applications. A number of the packaging and related problems which face the Phase 1 contractors and which will become more pronounced under Phase 2 as clock speeds and circuit densities increase further include:

Overcoming fatigue of the solder joints, due to mismatch in thermal expansions as evidenced by poor thermal cycle performance, to permit surface mounting of chip carriers to PC boards.

Demonstrating adequate automatic bonding of chips in carriers. Wire bonding to pads on 4.5 mil centers and lower are being considered, which imply pads in the order of 3.0 mils on a side or less. Need for high bond yields becomes critical because of difficulties with rework and discarding expensive chips with a poor bond cannot be tolerated.

Developing board materials which have dielectric constants (<4) below that of the present epoxy-glass, with high density fine line (<5 mil) and space multilayering and reduced via (6 mil) capabilities, to minimize board size and parasitic effects and to provide minimum signal degradation as clock speeds increase.

Developing beam tape and area beam tape to provide for bonding to smaller size pads on the periphery and center of a chip, to permit chip pretestability, and to interconnect chip to package or substrate.

Establishing increased domestic support for design, development and manufacturing of advanced packages. The ceramic package market is presently foreign dominated.

Demonstrating that ceramic chip carriers and associated sockets for test and burn-in, with terminals on 20 or 25 mil centers, or less, can be manufactured cost effectively.

Demonstrating process control of metallized beryllia for use in new package structures. Present experience is limited particularly when compared with alumina.

Development of improved thermal management techniques to minimize the thermal gradient from chip junction to the heat sinks as systems increase in size and number of devices.

Insuring that packages do not present impedance discontinuity to transmission line interconnects between individual packages containing high speed switching devices.

Development of packaging techniques to avoid or reduce electromagnetic interference, electrostatic discharge induced failures, and alpha-particle-induced soft errors.

Package Standardization

The emphasis placed on technology insertion by all the Military Services increases the significance of achieving interoperability between VHSIC developments. Of foremost concern is the design of commonality of signal processing functions within each VHSIC chip for application in as broad a spectrum of military electronic systems as possible. Beyond this, various chip functional interconnecting interoperability factors must be considered including the electrical interfaces (voltage supply and related electrical requirements), bus protocols (modes of circuit operation), interconnect standards, (hardware connections) and packaging. Each of these factors should be addressed to achieve some level of uniformity or standardization.

The contractors are generally following the existing standards activity of JEDEC, at least in terms of package types and terminal spacings. However it is obvious that the Phase 1 packaging developments contain a number of formats which make integration of VHSIC chips from different contractors into one system difficult in terms of a practical assembly process. Included are a variety of configurations, different mounting procedures and a wide range of both terminals and physical package sizes.

The longer range problem of combining several of the Phase 1 (and later Phase 2) manufacturers' chips or packages on a common board has not been addressed. Selection of a "standard" mounting scheme entails resolving thermal management procedures, mounting preferences (surface vs thru hole), use of leadless vs leaded carriers, selection of area grid vs perimeter terminations, numbers of terminals, spacing of terminals and package sizes. Resolution of the problem must insure use of processes and techniques which are common to a wide range of manufacturers and permit achievement of design requirements including weight and space savings. It is possible that DOD will lead a Phase 3 effort in this area.

Conclusions

The intent of the VHSIC program is to aid DOD in meeting future objectives in high speed, high throughput signal and data processing in support of requirements for military systems in the mid-eighties and beyond.

New packages, including chip carrier and pin grid array type designs, which include a large number of terminals, are being developed to house relatively large size chips with large numbers of pads.

The Phase 1 manufacturers' package designs are following, generally, the standards established by or under consideration by JEDEC. The problem of mounting each VHSIC manufacturers' packages on a common board must still be addressed, and is being considered by DOD as a Phase 3 support item.

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