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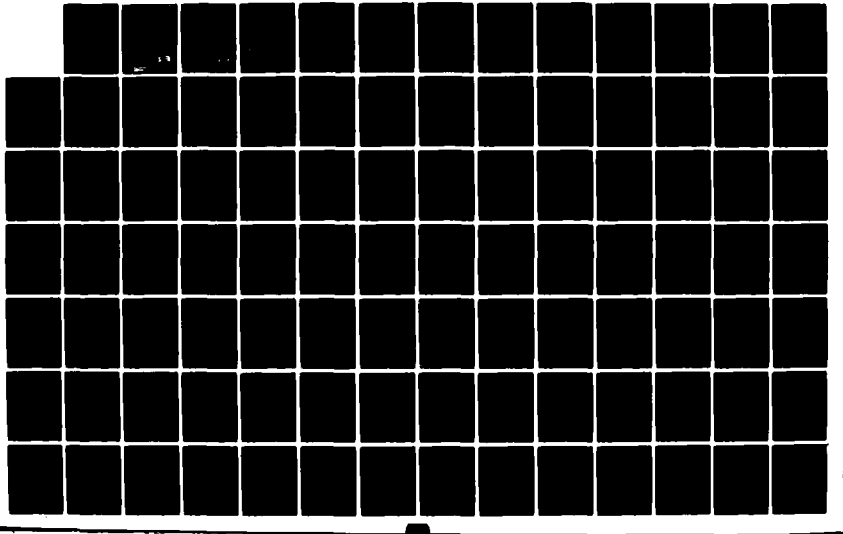

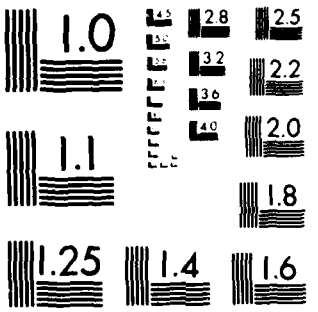

THEORETICAL-EXPERIMENTAL ANALYSIS OF THE EFFECTS OF GRAIN BOUNDARIES ON THE ELECTRICAL PROPERTIES OF SOI MOSFETS

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B. BACKGROUND AND OVERVIEW

The military's need for a high-data-rate target acquisition/tracking system requires high-speed and high-packing-density integrated-circuit (IC) logic. Fabricating ICs in thin films of silicon deposited on insulating substrates (SOI) has many potential advantages in this regard over conventional processing in bulk silicon. For example, the devices are dielectrically isolated and hence the ICs they constitute have low parasitic capacitance, which portends high speed and enables high packing density, and they can be designed to be highly radiation-tolerant, e.g., to suppress latch-up in CMOS ICs.

A common SOI technology is silicon-on-sapphire (SOS), which until recently had been the only possibly viable silicon thin film for ICs. The SOS technology however is plagued by fundamental problems and has not conformed to expectations. Recent work on recrystallization of polycrystalline silicon (polysilicon) films deposited on silicon-dioxide has demonstrated remarkable improvement in film quality, and thus has identified another possibly viable SOI technology for ICs. The polysilicon-on-SiO_2 technology not only has the advantages alluded to above, but also enables the fabrication of non-planar, "three-dimensional" ICs having active devices stacked on top of others (e.g., stacked CMOS) and consequently higher areal device densities.

Virtually all the research to date on polysilicon-on-SiO_2 has concentrated on the recrystallization technology, e.g., recrystallization by laser heating or by graphite-strip heating. This emphasis has been warranted, but now, to effectively promote SOI ICs, physical modeling of the devices, i.e., SOI MOSFETs, must be done in conjunction with the technological development. That is, the influence of grain boundaries and other defects in

the polysilicon on the electrical characteristics of the MOSFETs must be analyzed so that the technology can be refined and the transistors and circuits optimally designed to effectively minimize this detrimental influence. This modeling will reveal the influence of grain boundaries on the electrical characteristics of the MOSFETs, will describe the electrical interaction (charge coupling) between adjacent layers of the MOSOI structure, and will hence result in device models that can be used in computer simulation programs to aid the optimal design of SOI ICs.

This modeling, theoretical with experimental support, is the objective of this research. We describe in this first annual report the development of a physical model for the thin-film SOI (insulating substrate) MOSFET that will form the basis of a computer model for existing circuit simulation programs, e.g., SPICE. The model will thus enable computer simulation of SOI ICs, e.g., stacked CMOS, the prevalent basis for three-dimensional ICs. The model characterizes the (effective) field-effect mobility, the threshold voltage, and the source-drain leakage of a MOSFET fabricated in recrystallized polysilicon-on-SiO_2. The resulting physical model for the SOI MOSFET describes the influence of the grain boundaries and defects in the channel on the electrical characteristics of the transistor in terms of its properties, e.g., the channel length, the doping density, the film and oxide thicknesses, and the grain-boundary trap density. Such a model is essential in the optimization of the SOI technology and of the designs of SOI MOSFETs and ICs. It is also useful in developing grain-boundary passivation techniques, which we propose to do perhaps in the second year of this project.

We stress that this work has relied heavily on technological support from H.-W. Lam and his SOI development group at Texas Instruments, Inc. Dr. Lam and his colleagues at TI have supplied SOI material and devices to us for

electrical characterization to corroborate and guide the model development, and have collaborated with us in the development of the theory to ensure its practicality. Through this collaboration, we have fulfilled in essence the first-year tasks of the contract.

There are two basic effects in thin-film SOI MOSFETs that distinguish them from their bulk-silicon counterparts: 1) the effect of charge coupling between the front and back gates, which renders the (front-gate) threshold voltage dependent on the back-gate bias; and 2) the effect of grain boundaries on the channel conductance, which produces an effective turn-on characteristic that occurs beyond the strong-inversion threshold. Sections C and D of this report concern exclusively the former, whereas Sections E and F concern the latter. In Section G the combination of both effects is analyzed.

(We note that Sections C-G of this report are manuscripts of papers that have or will be published in the archival literature. Thus cross-references are made through the list of literature references at the end of each section rather than directly to the section containing the material cited.)

We describe in Section C our analytic characterization of the threshold voltage of enhancement-mode thin-film SOI MOSFETs. The charge coupling between the front and back gates of thin-film silicon-on-insulator (recrystallized Si on SiO_2) MOSFETs is analyzed, and closed-form expressions for the threshold voltage under all possible conditions are derived. The expressions clearly show the dependence of the linear-region channel conductance on the back-gate bias and on the device parameters, including those of the back silicon-insulator interface. The analysis is supported by current-voltage measurements of laser-recrystallized SOI MOSFETs. The results suggest how the back-gate bias may be used to optimize the performance of the SOI MOSFET is particular applications.

The threshold-voltage model includes: (1) accounting for fast surface states at the back Si-SiO_2 interface, which evidently are prevalent in typical SOI structures; (2) considering the possible potential drop in the underlying silicon substrate and its influence on the dependence of the threshold voltage on the back-gate bias; the (3) removing possible discrepancies between the theoretically defined threshold voltage and its measured value, which can be obtained in different ways.

The analysis of the charge coupling between the front and back gates is extended in Section D to describe the current-voltage characteristics of the thin-film SOI MOSFET. A simple analytic model for the steady-state, strong-inversion characteristics is developed. The model, simplified by a key approximation that the inversion charge density is described well by a linear function of the surface potential, clearly shows the dependence of the drain current on the device parameters and on the terminal voltages, including the back-gate (substrate) bias. The analysis is supported by measurements of current-voltage characteristics of thin-film (laser-recrystallized) SOI MOSFETs. The dependence of carrier mobility on the terminal voltages, especially the back-gate bias, is analyzed and shown to underlie discrepancies between the theoretical (constant mobility) and experimental results at high gate voltages. The mobility dependence on the back-gate bias enhances the strong influence of the back gate on the drain current, especially when the device is saturated.

The second peculiarity of SOI MOSFETs that distinguishes them from their bulk counterparts, i.e., that due to grain boundaries in the channel region, is demonstrated in Section E where we describe our preliminary analysis of the effects of grain boundaries on the channel conductance. A physical model that describes these effects on the linear-region (strong-inversion) channel

conductance of SOI (polysilicon on silicon-dioxide) MOSFETs is developed and supported experimentally. The model predicts an effective turn-on characteristic that occurs beyond the strong-inversion threshold, and henceforth defines the "carrier mobility threshold voltage" and the effective field-effect carrier mobility in the channel, which typically is higher than the actual (intragrain) mobility. These parameters, which are defined by the properties of the grain boundaries, can easily be misinterpreted experimentally as the threshold voltage and the actual carrier mobility.

In Section F, moderate inversion is analyzed. Our model for the effects of grain boundaries on the strong-inversion (linear region) conductance of SOI MOSFETs is extended to account for moderate inversion. The extension, which is supported by measurements of laser-recrystallized devices, predicts a nearly exponential dependence for the conductance on the (front) gate voltage that is controlled by the grain boundaries.

In Section G, our analyses of the charge-coupling and grain-boundary effects are combined to describe how the two effects are superimposed. The linear-region conductance of SOI MOSFETs is modeled by properly combining theoretical descriptions of the effects of grain boundaries in the channel region and of charge coupling between the front and back gates. The model is supported by measurements of thin-film SOI MOSFETs with and without grain boundaries. The theoretical-experimental analysis clearly distinguishes the charge-coupling effect from the grain-boundary effect, both of which can be beneficial to the MOSFET performance, and shows that the effects are not simply superimposed.

In Section H, extensions and applications of our SOI MOSFET model described in Sections C-G are discussed. This work is preliminary, and hence the descriptions are brief. They do however illustrate how our basic modeling

can be used for actual SOI device and circuit structures. The model extensions include: 1) accounting for the orientation of the grain boundary(ies) in the channel; 2) accounting for "large" voltage drops across the grain boundaries, which enables a characterization of the drain current in all regions of operation, e.g., the saturation region; and 3) studying the turn-off/turn-on transients in the SOI MOSFET with a floating body, which causes an overshoot in the drain current that affects the speed (propagation delay) of the device. The latter analysis, coupled with the steady-state model, will facilitate our development of a charge model for the SOI MOSFET to be used in SPICE to simulate the large-signal, transient characteristics of SOI integrated devices and circuits, e.g., stacked CMOS.

In Section I, we list our publications and presentations that have resulted from the first-year support of the contract. The section of this report corresponding to each published paper is also noted.

C. THRESHOLD VOLTAGE OF THIN-FILM SILICON-ON-INSULATOR (SOI) MOSFETs

I. Introduction

The recently demonstrated [1], [2] dramatic improvement in the quality of polycrystalline-silicon (polysilicon) films yielded by zone-melting recrystallization has spurred new interest in silicon-on-insulator (SOI) integrated circuits and devices. This new technology provides an alternative to silicon-on-sapphire (SOS) in the fabrication of monolithic circuits comprising advantageous dielectrically isolated devices [3]. The silicon-on-oxide (hereinafter termed SOI) technology furthermore has the flexibility to possibly enable the fabrication of radiation-hardened non-planar ("three-dimensional") integrated circuits [4].

Because SOI films are thin, the electrical properties of MOSFETs fabricated in them are typically influenced by the charge coupling between the front and back gates. For example, the (front-gate) threshold voltage V_{Tf} differs considerably from that of the bulk counterpart and depends on the bias and properties of the back gate. Although much emphasis has been placed on the recrystallization technology, little work has been done on the characterization of the electrical properties of SOI MOSFETs.

Worley [5] derived an analytic model for V_{Tf} of the SOS transistor in which similar charge coupling occurs. However his model, which is unnecessarily complex, pertains only to the usual SOS case in which the back silicon surface is depleted. Sano, et al. [6] developed a rigorous numerical model for V_{Tf} of the SOI MOSFET that illustrated important parametric dependences. However because no analytic expressions were derived, their illustrations were limited and provided little physical insight. Furthermore their model is not useful in SOI circuit analysis.

Barth [7], using a comprehensive numerical analysis, developed an analytic model for V_{Tf} that includes a dependence on the back-gate bias and

properties. However the model does not adequately account for the cases in which the back silicon surface is accumulated or inverted. Furthermore the maximum value of V_{Tf} of the SOI MOSFET, which can exceed the threshold voltage of the bulk counterpart [6] when the back surface is accumulated, is incorrectly described.

In this paper we present a general steady-state analysis of the charge coupling between the front and back gates of the SOI MOSFET that yields closed-form expressions for V_{Tf} under all possible steady-state charge conditions of the back surface. We initially assume a uniform doping density in the silicon film, but later the analysis is extended to account for the nonuniform density resulting from a deep boron implant commonly used in the n-channel MOSFET to suppress the back-surface leakage. To render the model applicable to SOI circuit analysis, we use the depletion approximation [5], [7], the general validity of which we discuss. The results can also be applied to SOS MOSFETs by setting the back-gate insulator capacitance to zero.

The analysis yields a description of V_{Tf} in terms of the back-gate bias and the properties of the device, including those of the back $Si-SiO_2$ interface, i.e., the fixed charge and fast surface-state densities. Consideration of the effect of charge in the silicon substrate [8] is included and shown to be typically insignificant. The analysis also leads to a simple characterization of the drain current in the linear region (low drain voltage) of operation.

Results of current-voltage measurements of laser-recrystallized SOI MOSFETs are discussed and shown to support the analysis. These measurements reveal, in accord with the analysis, that the back gate not only affects the back-channel conduction but also, in typical devices, can significantly affect the front-channel conduction. The results therefore indicate how well the

back-gate parameters must be controlled across an SOI wafer to ensure acceptable chip yield. Furthermore they suggest how the back-gate bias may provide a control by which optimal SOI MOSFET performance in particular applications is derived. This control does not exist in SOS MOSFETs.

II. Threshold Voltage of a Completely Depleted SOI MOSFET

The device we analyze is the four-terminal enhancement-mode SOI MOSFET (n-channel) illustrated in Fig. 1. It is fabricated in a recrystallized silicon (we ignore the grain boundaries) film on an insulating layer of silicon dioxide, which has been thermally grown or deposited on a silicon substrate. The front (conventional metal or polysilicon) and back (silicon substrate) gates compete for charge in the film body, which is manifested as the dependence of the (front-gate) threshold voltage on the back-gate bias and properties. Although the analysis refers directly to the device structure in Fig. 1, it can be applied to any MISIM device, e.g., the SOS MOSFET.

If the silicon film is sufficiently thick, it will never be completely depleted, and hence there will be no interaction, in steady-state, between the two gates. In this case, the conduction in the front as well as the back channel is described by conventional bulk MOSFET theory [9]. However the film thickness of typical SOI MOSFETs is thin enough that complete depletion can occur, thereby coupling the two gates and rendering the threshold voltage of each gate dependent on the conditions at the other. We now analyse these dependences.

To emphasize the charge coupling, we neglect small-geometry effects [10] and consider the one-dimensional active portion of the MOSFET shown in Fig. 2. The front (ϕ_{sf}) and back (ϕ_{sb}) surface potentials are the band bending from a hypothetical neutral film-body point to the respective surface. The

electrostatic potential at this point, if the source is grounded, is just the built-in potential of the source-film body junction. Thus in analogy to bulk MOSFET theory [9], we can write

$$V_{Gf} = \psi_{sf} + \psi_{of} + \Phi_{MS}^{f} \tag{1}$$

and

$$V_{Gb} = \psi_{sb} + \psi_{ob} + \Phi_{MS}^{b} \tag{2}$$

where V_{Gf} and V_{Gb} are the front- and back-gate voltages, ψ_{of} and ψ_{ob} are the potential drops across the front- and back-gate oxides, and Φ_{MS}^{f} and Φ_{MS}^{b} are the front and back gate-body work-function differences. We have not included in (2) a possible potential drop in the silicon substrate (back gate) [8]. We justify this neglect later in this section. Note that the difference between (1) and (2) would follow directly by summing the potential drops between the two gates.

If the silicon film is completely depleted, except for perhaps narrow inversion or accumulation layers at the surfaces, then the charge density is $-qN_A$, and integration of Poisson's equation across the film yields

$$\psi_b \equiv \psi_{sf} - \psi_{sb} \simeq \left(E_{sf} - \frac{qt_b N_A}{2\varepsilon_s}\right) t_b \tag{3}$$

where E_{sf} is the electric field at the front-surface edge of the depletion region, t_b is the film thickness, and N_A is the doping density in the film, assumed for now to be uniform.

Applying Gauss' theorem to the front surface, we get

$$\psi_{of} = \frac{1}{C_{of}} (\varepsilon_s E_{sf} - Q_{ff} - Q_{cf}) \tag{4}$$

where $C_{of} = \varepsilon_o / t_{of}$ is the front-gate oxide capacitance, Q_{ff} is the fixed charge density at the front Si-SiO_2 interface, and Q_{cf} is the front-surface carrier charge density, which in our V_{Tf} analysis represents inversion charge. We have not explicitly in (4) accounted for fast surface states at the front interface since they can be implicitly accounted for by modifying Q_{ff} in a strong-inversion analysis. At the back surface,

$$-\psi_{ob} = \frac{1}{C_{ob}} (\varepsilon_s E_{sf} - qN_A t_b + Q_{fb} - qN_{sb}\psi_{sb} + Q_{cb}) \tag{5}$$

where $C_{ob} = \varepsilon_o / t_{ob}$, Q_{fb}, and Q_{cb} are the back-gate counterparts of C_{of}, Q_{ff}, and Q_{cf} respectively, and N_{sb} is the fast surface-state density assumed to be uniformly distributed over the energy gap. We explicitly account for N_{sb} in (5) because the surface-state charge will vary with V_{Gb}. In (5) we have implicitly expressed the electric field at the back-surface edge of the depletion region as $(E_{sf} - qN_A t_b / \varepsilon_s)$.

We relate V_{Gf} to ψ_{sf} and ψ_{sb} by combining (1), (3), and (4):

$$V_{Gf} = V_{FB}^f + \left(1 + \frac{C_b}{C_{of}}\right) \psi_{sf} - \frac{C_b}{C_{of}} \psi_{sb} - \frac{Q_b/2 + Q_{cf}}{C_{of}} \tag{6}$$

where $V_{FB}^f = \Phi_{MS}^f - Q_{ff}/C_{of}$ is the front-gate (bulk MOSFET) flatband voltage, $C_b = \varepsilon_s / t_b$ is the depletion capacitance, and $Q_b = -qN_A t_b$ is the depletion-region areal charge density. Similarly we relate V_{Gb} to ψ_{sf} and ψ_{sb} by combining (2), (3), and (5):

$$V_{Gb} = V_{FB}^{b} - \frac{C_b}{C_{ob}}\psi_{sf} + (1 + \frac{C_b + C_{sb}}{C_{ob}})\psi_{sb} - \frac{Q_b/2 + Q_{cb}}{C_{ob}} \qquad (7)$$

where $V_{FB}^{b} = \Phi_{MS}^{b} - Q_{fb}/C_{ob}$ is the back-gate (bulk MOSFET) flatband voltage and $C_{sb} = qN_{sb}$. Equations (6) and (7) are the two key relations that describe the charge coupling between the front and back gates when the film body is completely depleted. Combining them leads to the description of the (front-gate) threshold voltage V_{Tf} in terms of V_{Gb} and the device parameters. We now detail the description of V_{Tf} for each possible steady-state charge condition at the back surface.

A. Accumulated Back Surface

When the back surface is accumulated, ψ_{sb} is virtually pinned at zero. We define the threshold condition [9] of the front surface by $\psi_{sf} = 2\phi_B$ where $\phi_B = (kT/q)\ln(N_A/n_i)$ is the film-body Fermi potential; then $Q_{cf} \simeq 0$ ($<< -Q_b$), and (6) yields

$$V_{Tf} \simeq V_{Tf}^{A} \triangleq V_{FB}^{f} + (1 + \frac{C_b}{C_{of}})2\phi_B - \frac{Q_b}{2C_{of}} \quad . \qquad (8)$$

Because ψ_{sb} is virtually independent of V_{Gb} for this condition, so is V_{Tf}.

B. Inverted Back Surface

When the back surface is inverted, $\psi_{sb} = 2\phi_B$. Then the threshold voltage for this case is given by (6) as

$$V_{Tf} \simeq V_{Tf}^{I} \triangleq V_{FB}^{f} + 2\phi_B - \frac{Q_b}{2C_{of}} \quad . \qquad (9)$$

As is V_{Tf}^A, V_{Tf}^I is independent of V_{Gb}, again because ϕ_{sb} is virtually invariant for this condition.

C. Depleted Back Surface

When the back surface is depleted, ϕ_{sb} is strongly dependent on V_{Gb}; its value ranges from about zero to $2\phi_B$ between the onsets of accumulation and inversion respectively. The values of V_{Gb} (V_{Gb}^A and V_{Gb}^I) corresponding to these onsets when the front surface is inverted ($\phi_{sf} \approx 2\phi_B$) are defined by (7) with $Q_{cb} \approx 0$ ($<< -Q_b$):

$$V_{Gb}^A \approx V_{FB}^b - \frac{C_b}{C_{ob}} 2\phi_B - \frac{Q_b}{2C_{ob}} \quad ; \tag{10}$$

$$V_{Gb}^I \approx V_{FB}^b + (1 + \frac{C_{sb}}{C_{ob}})2\phi_B - \frac{Q_b}{2C_{ob}} \quad . \tag{11}$$

The dependence of V_{Tf} on V_{Gb} for $V_{Gb}^A < V_{Gb} < V_{Gb}^I$ is obtained by combining (6) and (7) to eliminate ϕ_{sb} and letting $\phi_{sf} = 2\phi_B$, $Q_{cf} \approx 0$, and $Q_{cb} \approx 0$. The result is

$$\begin{aligned} V_{Tf} &\approx V_{Tf}^A - \frac{C_b\, C_{ob}}{C_{of}(C_b + C_{ob} + C_{sb})} (V_{Gb} - V_{Gb}^A) \\ &\approx V_{Tf}^I - \frac{C_b\, C_{ob}}{C_{of}(C_b + C_{ob} + C_{sb})} (V_{Gb} - V_{Gb}^I) \quad . \end{aligned} \tag{12}$$

Thus as V_{Gb} increases from V_{Gb}^A to V_{Gb}^I [an increase of $2\phi_B(1 + (C_b + C_{sb})/C_{ob})$], V_{Tf} decreases linearly with V_{Gb} from V_{Tf}^A to V_{Tf}^I [a decrease of $2\phi_B(C_b/C_{of})$]. The entire dependence of V_{Tf} on V_{Gb} for the SOI MOSFET (*n*-channel) with its film body completely depleted is plotted in

Fig. 3. The discontinuities in the slope of the plot are unreal because the transitions from one surface charge condition to another are not abrupt as was implicitly assumed in the analysis. Actually the surface potential corresponding to inversion and accumulation differs from $2\phi_B$ and zero, respectively, by a few thermal voltages (nkT/q where $n \sim 5$) depending on the degree of inversion and accumulation. These differences, which can be evaluated by numerically solving Poisson's equation in the film [7], however are typically small relative to the variation in surface potential between inversion and accumulation and hence do not significantly affect the $V_{Tf}(V_{Gb})$ characteristic. This is tantamount to the fact that the effective widths of the inversion and accumulation layers (across which the nkT/q is dropped) are typically much smaller than t_b [7], which was assumed in the derivation of (3).

The simplifying assumptions underlying our analysis were made to enable the derivation of closed-form expressions for V_{Tf} that could be used in an SOI MOSFET model amenable to computer-aided circuit simulation. In addition to the assumption discussed above, we also neglected in (2) the possible potential drop in the silicon substrate [8]. If the substrate is p-type and lowly doped ($\sim 10^{15} cm^{-3}$) and if Q_{fb}/q is high ($\sim 5 \times 10^{11}$ cm^{-2}), which are typically the case [11], then for $V_{Gb}^A < V_{Gb} < V_{Gb}^I$, vis-a-vis, when V_{Tf} varies with V_{Gb}, the substrate surface is inverted [12], and hence the potential drop is fixed at about twice the Fermi potential of the substrate. This means that the $V_{Tf}(V_{Gb})$ characteristic in Fig. 3 would simply shift to the left by this drop. For typical values of t_{ob} ($\sim$ 1 μm), this drop is much less than $(V_{Gb}^I - V_{Gb}^A)$, but for thinner t_{ob} it is not. If the substrate is n-type, the surface is typically accumulated for $V_{Gb}^A < V_{Gb} < V_{Gb}^I$, and the potential drop is negligible.

III. General Characterization of the Threshold Voltage of SOI MOSFETs

To generalize the analysis described in Section II, we must define the conditions for which the assumption that the silicon film is completely depleted is valid. The complete-depletion condition depends on the relative values of t_b and

$$x_{d(max)} = \left[\frac{2\varepsilon_s(2\phi_B)}{qN_A}\right]^{1/2} , \tag{13}$$

the maximum depletion-region width extending from an inverted surface [9]. In using (13) we are implicitly assuming that the transitions from depletion to neutrality in the film occur abruptly. Actually these transitions occur over a few Debye lengths L_D [9]. However $L_D << x_{d(max)}$, irrespective of N_A, and hence the charge in a transition region is much smaller than that in the associated depletion region. Consequently the charge coupling between the front and back gates effected by overlapping transition regions is negligible, and an analysis based on this depletion approximation is sufficiently accurate for developing SOI MOSFET models for computer-aided simulation. We consider the following three cases.

A. Case I: $t_b > 2x_{d(max)}$

In this case the film body can never be completely depleted by any combination of V_{Gf} and V_{Gb}. Consequently there is no charge coupling between the front and back gates, and V_{Tf} is given by the bulk MOSFET theory [9]:

$$V_{Tf} = V_{Tf0} \triangleq V_{FB}^f + 2\phi_B + \frac{qN_A x_{d(max)}}{C_{of}} . \tag{14}$$

B. Case II: $t_b < x_{d(max)}$

In this case the film body is necessarily completely depleted at the threshold condition of the front gate, irrespective of V_{Gb}. Thus V_{Tf} and its dependence on V_{Gb} are given directly by the results of Sections II-A, II-B, and II-C, which are plotted in Fig. 3. Note that V_{Tf} can exceed V_{TfO}. This is the case when the electric field at the back surface is sufficiently positive (same direction as E_{sf}), for example, when the back surface is accumulated. Then since the integral of the electric field over the depleted film at threshold is fixed at about $2\phi_B$, E_{sf} will increase as t_b decreases, and hence V_{Tf} can become very high.

C. Case III: $x_{d(max)} < t_b < 2x_{d(max)}$

In this case the depletion condition of the film body at threshold depends on V_{Gb}. To describe this dependence, we first define V_{Gb}^C as the value of V_{Gb} above which the film is completely depleted when the front surface is inverted. Recognizing that the depletion-region width extending from the back surface at $V_{Gb} = V_{Gb}^C$ is $[t_b - x_{d(max)}]$, we can write [9]

$$V_{Gb}^C = V_{FB}^b + \left(1 + \frac{C_{sb}}{C_{ob}}\right) \frac{qN_A}{2\varepsilon_s} [t_b - x_{d(max)}]^2 + \frac{qN_A}{C_{ob}} [t_b - x_{d(max)}] \quad . \qquad (15)$$

Now for $V_{Gb} < V_{Gb}^C$, the silicon film is not completely depleted, and V_{Tf} is V_{TfO} given by (14). For $V_{Gb} > V_{Gb}^C$, V_{Tf} is given by the results of Section II. That is, for $V_{Gb}^C < V_{Gb} < V_{Gb}^I$, V_{Tf} is given by (12), and for $V_{Gb} > V_{Gb}^I$, it is given by (9). As V_{Gb} increases from V_{Gb}^C to V_{Gb}^I, V_{Tf} decreases from V_{TfO} to V_{Tf}^I.

In Fig. 4 we have plotted the dependences of V_{Tf} on V_{Gb} for several ratios of t_b and $x_{d(max)}$, which is fixed by N_A as described in (13). As expected, the sensitivity of V_{Tf} to V_{Gb} diminishes as t_b increases, and interestingly the sensitivity of V_{Tf} to t_b is reduced as V_{Gb} is decreased. We note that the dependence of V_{Tf} on V_{FB}^b ($= \Phi_{MS}^b - Q_{fb}/C_{ob}$) is also given by the plots in Fig. 4. These plots are thus important in identifying ways to suppress the influence of Q_{fb}, which is difficult to control uniformly across an SOI wafer. As evident in Fig. 4, one such way is to apply a sufficiently negative V_{Gb}. The dependence of V_{Tf} on N_A is implied by Fig. 5 in which we have plotted V_{Tf} versus V_{Gb} for several values of $x_{d(max)}$, defined by N_A in (13), relative to t_b, which is fixed. We see that V_{Tf} becomes less sensitive to N_A as V_{Gb} decreases. Furthermore as N_A decreases [vis-a-vis, $x_{d(max)}$ increases], the sensitivity of V_{Tf} to V_{Gb} is enhanced until $x_{d(max)}$ reaches t_b.

D. Deep-Boron-Implanted Film Body

It is common in the fabrication of n-channel SOI MOSFETs to implant boron deep into the film body so as to avoid depletion or inversion at the back surface [13]. This implant serves to suppress the back-surface leakage current as well as to negate the dependence of the front-channel conduction on the back-gate parameters, e.g., Q_{fb}.

To account for this implant in our analysis we approximate the resultant nonuniform doping density $N_A(x)$ by a step profile as shown in Fig. 6. For the case of interest in which the depletion region from the inverted front surface extends to the implanted region [$t_s < x_{d(max)}$], but not to the back surface, the charge distribution and the electric field and electrostatic potential variations in the film body are as illustrated in Fig. 6. The threshold voltage of the n-channel MOSFET in this case is [9]

$$V_{Tf} = V_{FB}^{f} + 2\phi_B + \frac{q(N_{Af}t_s + N_{Ab}x_{di})}{C_{of}} \tag{16}$$

where N_{Af} and N_{Ab} are the front and back doping densities in the film body that define the step at $x = t_s$ (see Fig. 6) and x_{di} is the extent of the depletion into the implanted ($N_A = N_{Ab}$) region. We stress that V_{FB}^{f} includes the front gate-body work-function difference defined by $N_A = N_{Af}$, and hence implicitly accounts for the equilibrium potential barrier at $x = t_s$, $\Delta\phi_B = (kT/q)\ln(N_{Ab}/N_{Af})$. That is, when the front surface is strongly inverted, $\psi_{sf} \simeq 2\phi_B + \Delta\phi_B$ as indicated in Fig. 6. Integration of Poisson's equation yields

$$x_{di} = -t_s + \left[t_s^2\left(1 - \frac{N_{Af}}{N_{Ab}}\right) + \frac{2\varepsilon_s\psi_{sf}}{qN_{Ab}}\right]^{1/2} . \tag{17}$$

Inserting (17) into (16) then gives the desired expression for V_{Tf}.

We note that this result can be simplified in most cases because N_{Ab} ($>> N_{Af}$) is typically high enough that the square-root term in (17) is approximated well by the first two terms of its Taylor-series expansion. Then (17) becomes

$$x_{di} \simeq \frac{\varepsilon_s\psi_{sf}}{qt_sN_{Ab}} - \frac{t_sN_{Af}}{2N_{Ab}} , \tag{18}$$

which, with (16) and the threshold condition $\psi_{sf} = 2\phi_B + \Delta\phi_B$, yields

$$V_{Tf} \simeq V_{FB}^{f} + \frac{C_{bf}}{C_{of}}\Delta\phi_B + \left(1 + \frac{C_{bf}}{C_{of}}\right)2\phi_B - \frac{Q_{bf}}{2C_{of}} \tag{19}$$

where $C_{bf} = \varepsilon_s/t_s$ and $Q_{bf} = -qN_{Af}t_s$. Note the similarity between (19) and

V_{Tf}^{A} defined in (8). The threshold voltage is uniquely defined by N_{Af}, N_{Ab}, t_s, and the front-gate parameters; it does not depend on the back-gate parameters.

IV. Experimental Support and Discussion

To provide experimental support for the analysis described in this paper, we measured linear-region $I_D(V_D,V_{Gf},V_{Gb})$ characteristics of four-terminal SOI MOSFETS (*n*-channel) fabricated at Texas Instruments [11]. The silicon film is 0.5 μm thick and was laser-recrystallized after being deposited on a 1-μm-thick layer of silicon-dioxide ($C_{ob} \approx 3.5 \times 10^{-9}$ F/cm^2), which had been thermally grown on a p-type silicon substrate with resistivity of 6-8 Ω-cm. The film was doped by ion implantation that yielded, based on SUPREME-II calculations [11], $N_A \approx 2 \times 10^{16}$ cm^{-3} near the front surface and $N_A \approx 10^{15}$ cm^{-3} at the back surface. No deep boron implant was done. The front gate is n^+ polysilicon, and the gate oxide thickness is 600 Å ($C_{of} \approx 5.8 \times 10^{-8}$ F/cm^2). Large devices ($Z = L = 40$ μm) were selected to avoid unnecessary complications, e.g., small-geometry effects [10].

For strong-inversion conditions in the linear region [$V_D << (V_{Gf}-V_{Tf})$], I_D is approximately related to V_{Tf} by [9]

$$I_D \approx \frac{Z}{L} \mu_{nf} C_{of} (V_{Gf} - V_{Tf}) V_D \tag{20}$$

where the terms have their usual meanings. We note that V_{Tf} in (20), which is the threshold voltage implied by the linear extrapolation of the measured $I_D(V_{Gf})$ characteristic to the V_{Gf} axis, is not exactly the threshold voltage we defined in Section III, but is typically ~ 0.1 V higher [14]. This

difference, which reflects the difference between ψ_{sf} and $2\phi_B$, is however not strongly dependent on V_{Gb} [12], and hence (20) can be used in conjunction with our measurements to check our theoretical predictions for $V_{Tf}(V_{Gb})$.

If the back-channel current I_{BC} is significant, it must be added to (20):

$$I_D \rightarrow I_D + I_{BC} \quad . \tag{21}$$

Note that I_{BC} could be expressed in the form of (20) with the back-gate parameters and voltage substituted for μ_{nf}, C_{of}, V_{Tf}, and V_{Gf}. The back-gate counterpart to V_{Tf} could further be characterized as was V_{Tf} using the analysis described in Sections II and III.

Because of I_{BC} and its dependence on V_{Gf} implied by our analysis, V_{Tf}^I cannot be determined from the direct extrapolation of (20) with sufficient accuracy to measure the dependence of V_{Tf} on V_{Gb}. Furthermore the conductance properties of the MOSFETs measured are influenced by grain boundaries in the laser-recrystallized (poly)silicon film. Grain-boundary scattering, which depends on V_{Gf}, affects the channel mobility μ_{nf} in (20) and causes an apparent increase in V_{Tf} [15]. Thus the common measurement of threshold voltage based on the extrapolation of (20) yields ambiguous results for these devices.

However it is possible to detect the dependence of V_{Tf} on V_{Gb} for these devices using the experimental method we now describe. For a given V_{Gb}, we measure

$$\Delta I_D \triangleq I_D(V_{Gf} > V_{Tf}) - I_D(V_{Gf} << V_{Tf}) \quad , \tag{22}$$

which is merely the change in I_D that occurs when the front-surface condition is altered from accumulation to strong inversion. Recognizing that $x_{d(max)} < t_b < 2x_{d(max)}$ in these devices and referring to Section III-C and to (20) and (21), we can write

$$\Delta I_D \simeq \Delta I_{D1} \triangleq g_{mf}(V_{Gf} - V_{TfO}) \qquad \text{for } V_{Gb} < V_{Gb}^C \quad , \tag{23}$$

$$\Delta I_D \simeq \Delta I_{D2} \triangleq g_{mf}[V_{Gf} - V_{Tf}(V_{Gb})] \qquad \text{for } V_{Gb}^C < V_{Gb} < V_{Tb}^I \quad , \tag{24}$$

$$\Delta I_D \simeq \Delta I_{D3} \triangleq g_{mf}(V_{Gf} - V_{Tf}^I) + g_{mb}(V_{Gb} - V_{Tb}^I) \qquad \text{for } V_{Tb}^I < V_{Gb} < V_{TbO} \quad , \tag{25}$$

and

$$\Delta I_D \simeq \Delta I_{D4} \triangleq g_{mf}(V_{Gf} - V_{Tf}^I) + g_{mb}(V_{TbO} - V_{Tb}^I) \qquad \text{for } V_{Gb} > V_{TbO} \tag{26}$$

where

$$g_{mf} = \frac{Z}{L} \mu_{nf} C_{of} V_D \tag{27}$$

and where g_{mb}, V_{Tb}^I, and V_{TbO} are the back-gate counterparts of g_{mf}, V_{Tf}^I, and V_{TfO} respectively. We have neglected the grain-boundary effects on channel conductance, which are significant only for relatively low values of V_{Gf} [15].

We see from (23) and (26) that at a fixed V_{Gf}, ΔI_D is independent of V_{Gb} when V_{Gb} is sufficiently low ($< V_{Gb}^C$) or sufficiently high ($> V_{TbO}$). When $V_{Gb}^C < V_{Gb} < V_{Tb}^I$, (24) shows that ΔI_D increases with increasing V_{Gb} because V_{Tf} is decreasing; whereas when $V_{Tb}^I < V_{Gb} < V_{TbO}$, (25) shows that it increases with V_{Gb} because of back-channel conduction. Note then that the difference between ΔI_{D4} and ΔI_{D1} reveals quantitatively the shift in V_{Tf} resulting from the corresponding change in V_{Gb}. From (23) and (26) we have

$$\Delta I_{D4} - \Delta I_{D1} = g_{mf}(V_{TfO} - V_{Tf}^{I}) + g_{mb}(V_{TbO} - V_{Tb}^{I}) \tag{28}$$

$$\equiv g_{mf}(V_{TfO} - V_{Tf}^{I})(1 + \frac{\mu_{nb}}{\mu_{nf}}) \quad ; \tag{29}$$

the equivalent expression (29) follows from (28) when we note from (9) and (14) that

$$V_{TfO} - V_{Tf}^{I} = \frac{qN_A}{C_{of}}[x_{d(max)} - \frac{t_b}{2}] \quad , \tag{30}$$

and hence that $(V_{TbO} - V_{Tb}^{I})$ can be expressed similarly. Thus if μ_{nf} and μ_{nb} are known, then measuring $(\Delta I_{D4} - \Delta I_{D1})$ implies, via (29), $(V_{TfO} - V_{Tf}^{I})$, which reflects the influence of V_{Gb} on V_{Tf}.

We have plotted in Fig. 7 the measured dependence of ΔI_D on V_{Gb}, which resulted when $V_{Gf} = \pm 1$ V was used to invert and accumulate the front surface. As predicted by our analysis, ΔI_D saturates when V_{Gb} is sufficiently low or high. For comparison we plot also in Fig. 7 the calculated (estimated) $\Delta I_D(V_{Gb})$ dependence obtained from (23) - (27). For the calculations, g_{mf} and g_{mb} were <u>estimated</u> from linear-region $I_D(V_{Gf},V_{Gb})$ measurements, and V_{Tf} and V_{Tb} were evaluated using our analysis, the same measurements, and estimated device parameter values [11]. The fact that the theoretical and experimental curves in Fig. 7 have the same basic shape supports our analysis. We note that the fast surface states at the back $Si\text{-}SiO_2$ interface ($N_{sb} \approx 3 \times 10^{11}$ cm^{-2}/eV [11]) stretch-out the $\Delta I_D(V_{Gb})$ curve along the V_{Gb} axis. This stretch-out, which is described by ΔI_{D2}, reflects variation in the charge of the surface states resulting from change in V_{Gb}, i.e., in ψ_{sb}.

An obvious discrepancy between the calculated and measured results plotted in Fig. 7 is the difference between the respective values of (ΔI_{D4}-ΔI_{D1}). This difference implies a discrepancy between our theoretical and experimental estimations of ($V_{Tf0} - V_{Tf}^{I}$) based on (30) and (29) respectively. The measurements yield 0.21 V whereas the theory predicts 0.14 V. Because the grain boundaries tend to reduce I_D [15], they are probably not the cause of this discrepancy. More plausible reasons are the nonuniform $N_A(x)$ and/or uncertainty in t_b. Approximating the actual $N_A(x)$ by a step profile or assuming about a 10%-thinner t_b will remove the discrepancy [12].

The theoretical and experimental results plotted in Fig. 7 imply that in typical SOI MOSFETS the charge condition of the back surface, which is defined by V_{Gb} and the properties of the Si-SiO_2 interface, can significantly affect the conduction properties of the front surface, and vice versa. We note that the back-gate influence on I_D is even stronger for thinner silicon films and for lower doping densities in the film as implied by Figs. 4 and 5.

The variations in V_{Tf} and I_D discussed above, which result from changes in the back-surface charge condition, can be induced by variations in V_{FB}^{b}, i.e., Q_{fb}, as well as in V_{Gb}. Hence the results indicate how well Q_{fb} must be controlled across an SOI wafer to ensure acceptable chip yield. To exemplify further the sensitivity of V_{Tf} to Q_{fb}, we note from (12), when V_{Gb} is fixed such that the film body is completely depleted (e.g., V_{Gb} = 0 for the devices used in our measurements), that

$$\frac{dV_{Tf}}{dQ_{fb}} \simeq \frac{-C_b}{C_{of}(C_b + C_{ob} + C_{sb})} \quad . \tag{31}$$

Hence for the devices measured, in which C_{sb} is significant, $dV_{Tf}/d(Q_{fb}/q) \approx 0.08 \times 10^{-11}$ V-cm^2. Consequently variations in (Q_{fb}/q) larger than 10^{11} cm^{-2} produce considerable changes in V_{Tf}. As evidenced by (31), this sensitivity is more pronounced in devices with thinner t_b.

In most cases the sensitivity of I_D to the back-gate properties is undesirable, and processes like a deep-boron implant in the n-channel MOSFET are used to suppress it. However there may be applications in which the front-back-gate charge coupling can be exploited to improve the MOSFET performance. As indicated in Fig. 3 it is possible to bias the back gate ($V_{Gb} \approx V_{Tb}^I$) such that V_{Gf} can simultaneously turn the back and front channels on and off. In this case, when the device is on ($V_{Gf} > V_{Tf}^I$), I_D is enhanced by I_{BC} as well as by an effective reduction in V_{Tf} due to V_{Gb}, which increases the front-channel conduction. When the device is off ($V_{Gf} << V_{Tf}^I$), the leakage is low because V_{Tb} is increased above V_{Tb}^I, which implies that the back channel is off. The front-channel leakage is thus concomitantly further reduced because of an effective increase in V_{Tf}.

VI. Summary

The charge coupling between the front and back gates of thin-film uniformly doped SOI MOSFETs has been analyzed, and closed-form expressions for the threshold voltage V_{Tf} under all possible steady-state conditions have been derived. The expressions clearly show the dependence of channel conductance in the linear region on the back-gate bias V_{Gb} and on the device parameters, including the fixed charge density Q_{fb} and the fast surface-state density N_{sb} at the back Si-SiO_2 interface. The threshold voltage of an n-channel SOI MOSFET having a deep boron implant that negates the influence of the back gate was also described.

The analysis, which characterizes directly the linear-region (strong inversion) drain current I_D, was supported in essence by measurements of this current in laser-recrystallized SOI MOSFETs [11]. Although the $V_{Tf}(V_{Gb})$ dependence cannot be measured directly, measurements of changes in I_D produced by variations in V_{Gb} yielded results that are basically in agreement with the theoretical predictions. This novel experimental method can be generally used to characterize $V_{Tf}(V_{Gb})$ of thin-film SOI MOSFETs.

An n-channel MOSFET was assumed in the analysis, but the corresponding results for p-channel MOSFETs can be easily derived analogously Hence the analysis can provide a basis for optimizing the performance of SOI CMOS integrated circuits. For example it describes how a negative V_{Gb}, despite reducing the current-drive capability in n-channel MOSFETs, could be used to diminish the sensitivity of V_{Tf} to Q_{fb} and to the silicon film parameters, e.g., thickness, all of which may vary considerably across an SOI wafer. Alternatively it describes how a deep boron implant could provide the same desensitization, thus enabling the use of V_{Gb} to optimize the performance of the p-channel MOSFET. The analysis indicated also that the current-drive capability of the SOI MOSFET could possibly be enhanced without significant increase in leakage by proper choice of V_{Gb}.

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FIGURE CAPTIONS

Fig.1. Four-terminal SOI MOSFET structure. The terminal voltages are referenced to the source voltage ($V_S = 0$).

Fig. 2. One-dimensional active portion of the SOI MOSFET. To simplify the notation, the front gate is labeled M even though it is typically polysilicon.

Fig. 3. Theoretical dependence of V_{Tf} on V_{Gb} for a completely depleted SOI MOSFET. For reference, the corresponding bulk MOSFET threshold voltage V_{Tf0} [Eq. (14)] is indicated.

Fig. 4. Theoretical dependences of V_{Tf} on V_{Gb} and t_b for the four-terminal SOI MOSFET with fixed N_A, which defines $x_{d(max)}$ [Eq. (13)] and $Q_{d(max)} = -qN_A x_{d(max)}$. The parameter α is used to simplify the scaling of the V_{Tf} axis.

Fig. 5. Theoretical dependences of V_{Tf} on V_{Gb} and N_A [through $x_{d(max)}$] for the four-terminal SOI MOSFET with fixed t_b. The parameter β is used to simplify the scaling of the V_{Tf} axis. Note that ϕ_B, which depends on N_A, varies slightly from one curve to another.

Fig. 6. The doping density profile $N_A(x)$ and its step-function approximation for the n-channel SOI MOSFET with a deep boron implant. The charge distribution $\rho_d(x)$and the electric field $E(x)$ and electrostatic potential $\phi(x)$ variations follow from the approximate profile when the front surface is strongly inverted and the depletion approximation is used.

Fig. 7. Calculated and measured ΔI_D versus V_{Gb} for a four-terminal laser-recrystallized SOI MOSFET reflecting the dependence of V_{Tf} on V_{Gb}.

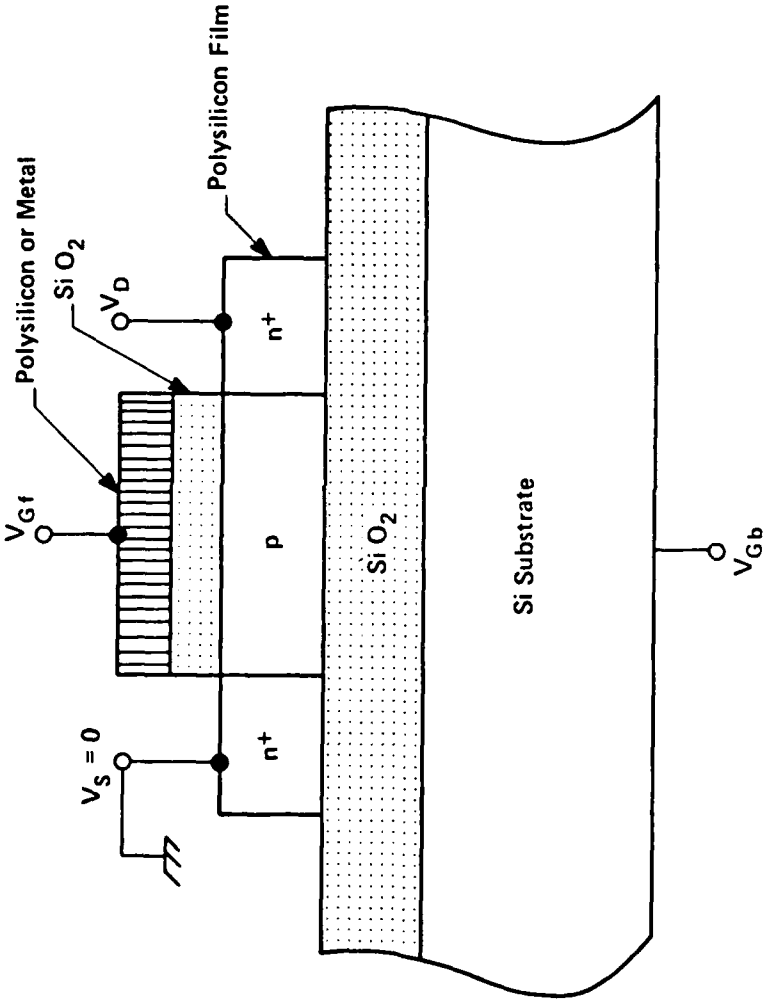
Polysilicon Film
Polysilicon or Metal
Si O_2
V_D
V_{Gf}
$V_S = 0$
n^+
p
n^+
Si O_2
Si Substrate
V_{Gb}

Fig. 1

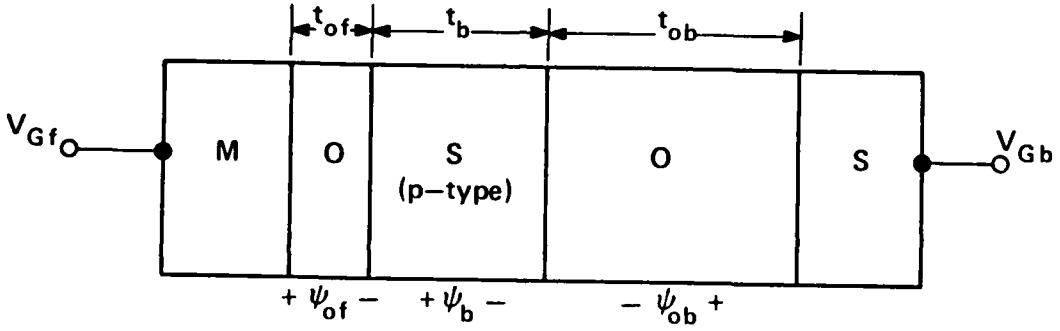

Fig. 2

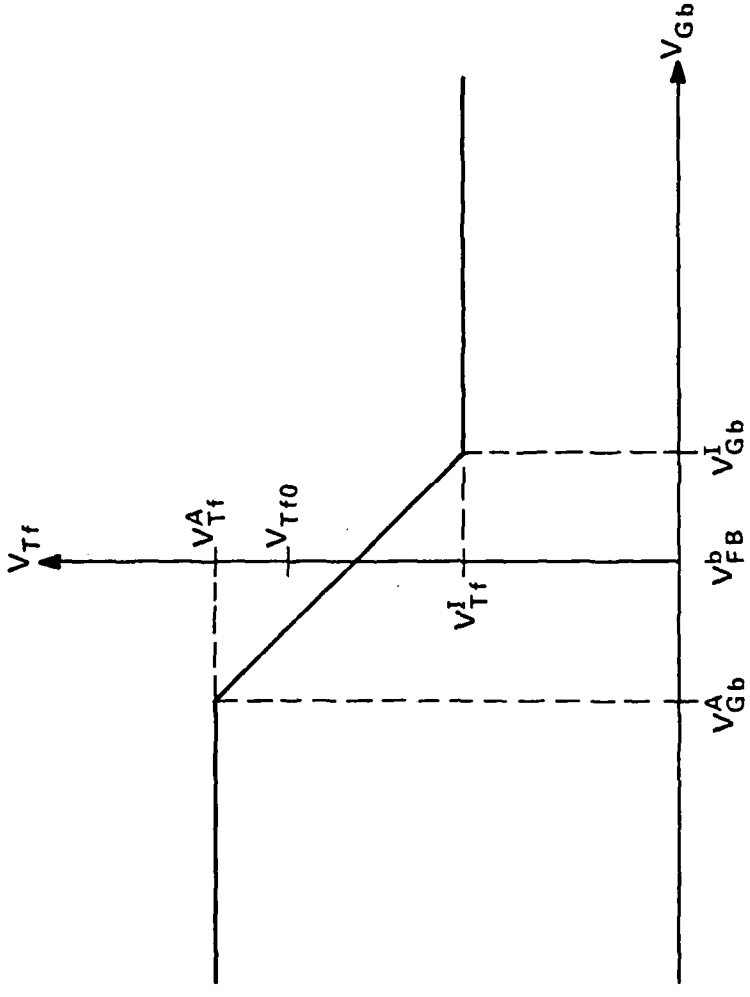

Fig. 3

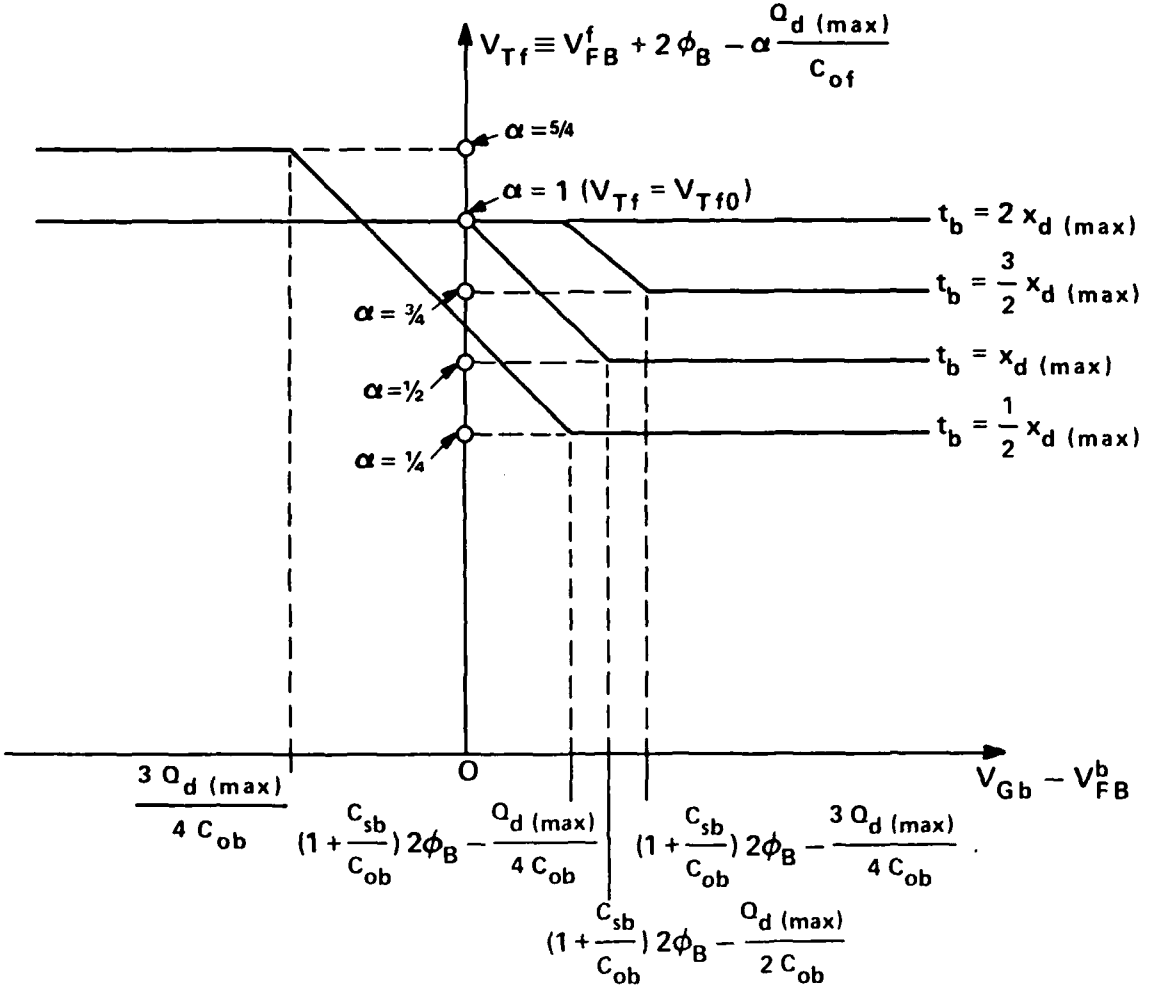
$V_{Tf} \equiv V_{FB}^{f} + 2\phi_B - \alpha \frac{Q_{d\,(max)}}{C_{of}}$
$\alpha = 5/4$
$\alpha = 1\ (V_{Tf} = V_{Tf0})$
$\alpha = 3/4$
$\alpha = 1/2$
$\alpha = 1/4$
$t_b = 2\,x_{d\,(max)}$
$t_b = \frac{3}{2} x_{d\,(max)}$
$t_b = x_{d\,(max)}$
$t_b = \frac{1}{2} x_{d\,(max)}$
O
$V_{Gb} - V_{FB}^{b}$
$\frac{3\,Q_{d\,(max)}}{4\,C_{ob}}$
$(1 + \frac{C_{sb}}{C_{ob}})\,2\phi_B - \frac{Q_{d\,(max)}}{4\,C_{ob}}$
$(1 + \frac{C_{sb}}{C_{ob}})\,2\phi_B - \frac{3\,Q_{d\,(max)}}{4\,C_{ob}}$
$(1 + \frac{C_{sb}}{C_{ob}})\,2\phi_B - \frac{Q_{d\,(max)}}{2\,C_{ob}}$

Fig. 4

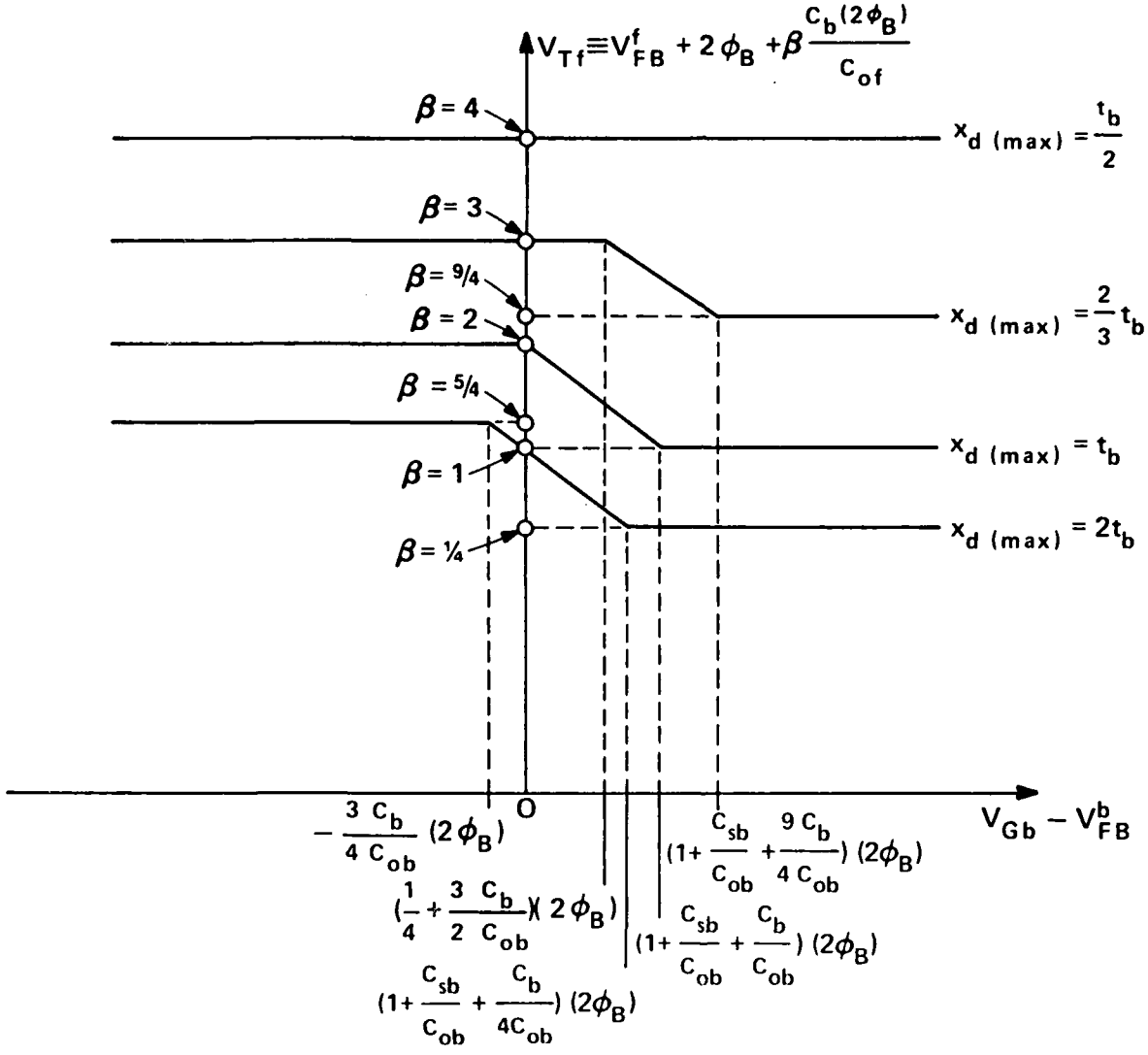
$V_{Tf} \equiv V_{FB}^{f} + 2\phi_B + \beta \frac{C_b(2\phi_B)}{C_{of}}$
$\beta = 4$
$\beta = 3$
$\beta = 9/4$
$\beta = 2$
$\beta = 5/4$
$\beta = 1$
$\beta = 1/4$
$x_{d\,(max)} = \frac{t_b}{2}$
$x_{d\,(max)} = \frac{2}{3} t_b$
$x_{d\,(max)} = t_b$
$x_{d\,(max)} = 2t_b$
O
$V_{Gb} - V_{FB}^{b}$
$-\frac{3\,C_b}{4\,C_{ob}}(2\phi_B)$
$(\frac{1}{4} + \frac{3}{2}\frac{C_b}{C_{ob}})(2\phi_B)$
$(1 + \frac{C_{sb}}{C_{ob}} + \frac{C_b}{4C_{ob}})(2\phi_B)$
$(1 + \frac{C_{sb}}{C_{ob}} + \frac{C_b}{C_{ob}})(2\phi_B)$
$(1 + \frac{C_{sb}}{C_{ob}} + \frac{9\,C_b}{4\,C_{ob}})(2\phi_B)$

Fig. 5

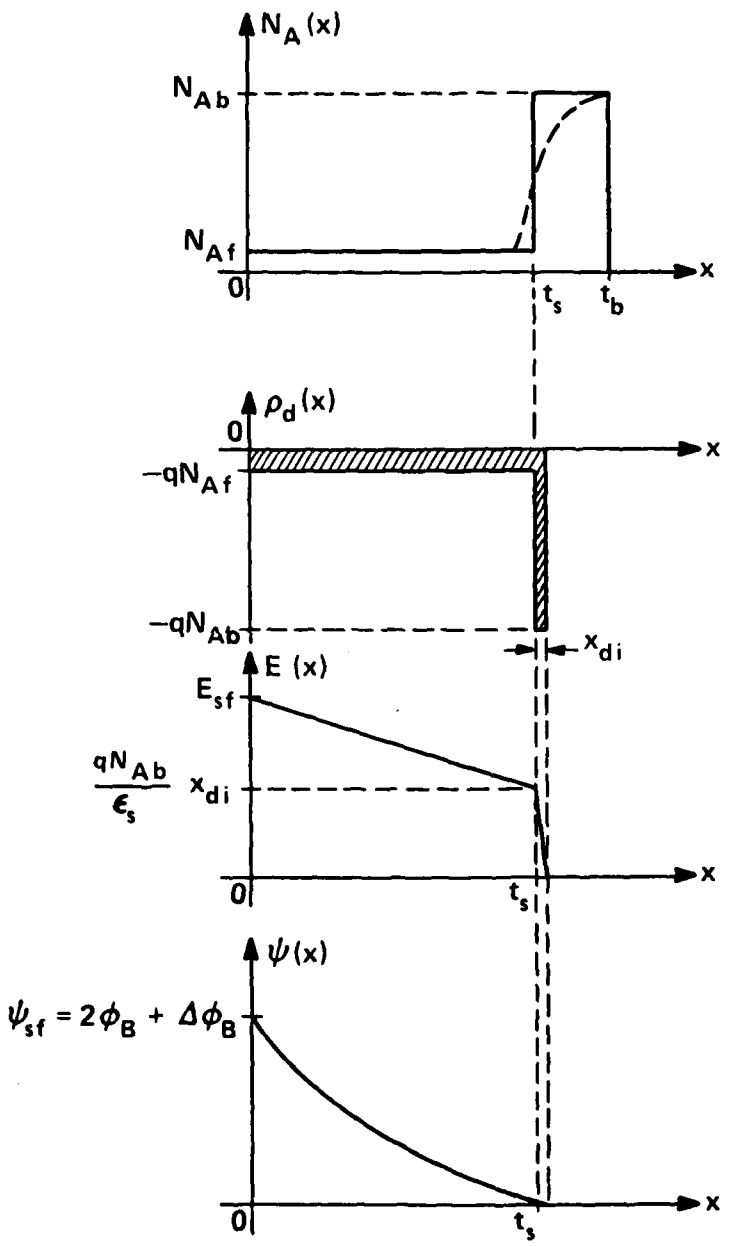
$N_A(x)$
N_{Ab}
N_{Af}
0
x
t_s
t_b
$\rho_d(x)$
0
x
$-qN_{Af}$
$-qN_{Ab}$
x_{di}
E (x)
E_{sf}
$\frac{qN_{Ab}}{\epsilon_s}$
x_{di}
0
x
t_s
$\psi(x)$
$\psi_{sf} = 2\phi_B + \Delta\phi_B$
0
x
t_s

Fig. 6

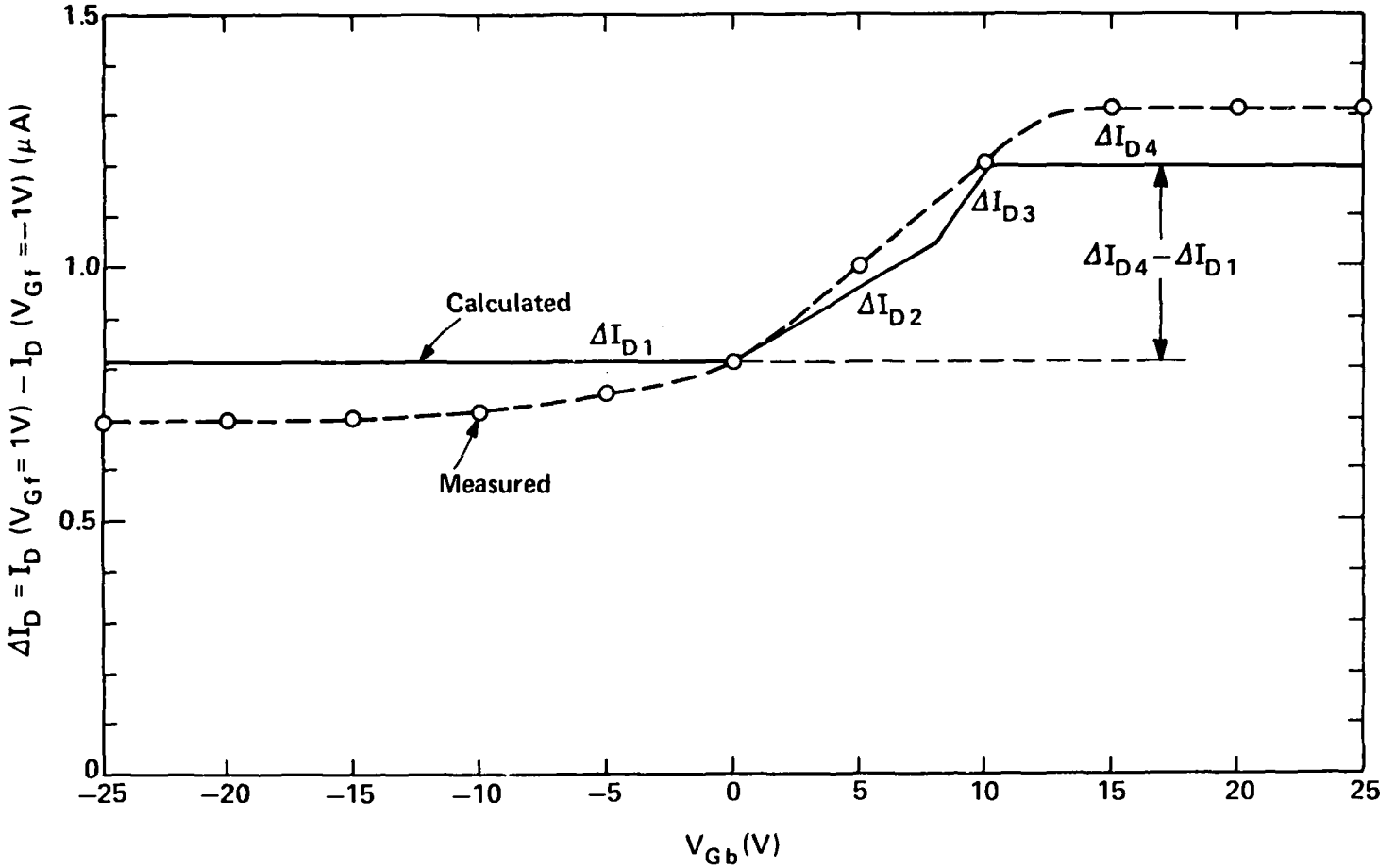
1.5
1.0
0.5
0
$\Delta I_D = I_D\ (V_{Gf} = 1V) - I_D\ (V_{Gf} = -1V)\ (\mu A)$
Calculated
Measured
ΔI_{D1}
ΔI_{D2}
ΔI_{D3}
ΔI_{D4}
$\Delta I_{D4} - \Delta I_{D1}$
−25
−20
−15
−10
−5
0
5
10
15
20
25
V_{Gb}(V)

Fig. 7

D. CURRENT-VOLTAGE CHARACTERISTICS OF THIN-FILM SOI MOSFETs IN STRONG INVERSION

I. INTRODUCTION

The fundamental advantages [1] of dielectric isolation have prompted the development of new silicon-on-insulator (SOI) technologies. Many methods to achieve thin-film SOI structures have been reported. Common ones are the recrystallization of polysilicon films deposited on silicon dioxide by laser annealing [2] or by graphite-strip heating [3] and the implantation of oxygen into single-crystal silicon [4]. MOSFETs fabricated in these thin SOI films have current-voltage characteristics that differ from those of conventional bulk MOSFETs because of the charge coupling between the front (conventional) and back (silicon substrate) gates. This coupling, which occurs when the silicon film is completely depleted, renders the front-channel (steady-state) current dependent on the back-gate bias [5]-[8].

We recently analyzed this charge coupling and modeled the resulting modulation of the (front-gate) threshold voltage V_{Tf} by the back-gate bias V_{Gb} [8]. We demonstrated that V_{Tf} varies linearly with V_{Gb} until inversion or accumulation charge at the back silicon surface blocks the field penetration from the back insulator. The charge coupling influences the current-voltage characteristics more significantly when the drain voltage V_D is high because the back surface near the drain remains depleted for a wider range of V_{Gb}. A complete model of the thin-film SOI MOSFET must therefore account for this influence.

Tihanyi and Schlotterer [9] analyzed the charge coupling in SOS MOSFETs, implicitly assuming that the silicon-sapphire interface is depleted and that the sapphire is thick enough that the electric field in it is negligibly small. Although these assumptions are typically valid for SOS MOSFETs, they are not valid for SOI (Si on SiO_2) MOSFETs because the back insulator is thin.

Barth et al. [7] derived rigorous analytic expressions for the drain current of MISIM-FETs accounting for the influence of the back gate. These expressions show that the front channel conductance of typical SOI MOSFETs is strongly dependent on the back-gate bias. Although the derivation was based on the depletion approximation and included assumptions of constant mobility and uniform doping, the complexity of the model limits its utility in giving physical insight and in aiding the design of SOI devices and circuits. Furthermore it was not adequately supported by experimental data.

In this paper we present a simple analytic model for the strong-inversion steady-state current-voltage characteristics of four-terminal thin-film SOI MOSFETs. The dependence of the drain current I_D on V_{Gf}, the front-gate voltage, V_{Gb}, and V_D for all regions of operation is explicitly shown in the derived expressions. Simplification of the model is achieved by recognizing, based on physical insight, that the inversion charge density anywhere in the channel can be approximated well by a linear function of the surface potential for a typical device. We assume a constant carrier mobility in the channel and a uniform doping density in the silicon film, but we include comprehensive discussions of the limitations implied by these assumptions. Because of the linearity, the model yields expressions for I_D that are simpler than those of bulk MOSFETs. The physical model can be useful in the engineering design of SOI devices and may imply optimal back-gate biases in particular SOI integrated circuits. It can also provide the basis for MOSFET models needed in computer-aided analysis of SOI circuits

Results of extensive current-voltage measurements of laser-recrystallized SOI MOSFETs are discussed and shown to support the model. Theoretical-experimental plots of $I_D(V_{Gf},V_{Gb},V_D)$ show good agreement until mobility degradation at high V_{Gf} causes discrepancies. The carrier mobility, which can

be modeled similarly to that in the bulk MOSFET in the linear region, is strongly dependent on the back surface charge condition in the saturation region. The mobility degradation is most severe when the back surface is accumulated.

The model reveals that, for given values of V_{Gf} and V_D, I_D decreases as V_{Gb} is varied to change the charge condition of the back surface from depletion everywhere between the source and drain regions to accumulation everywhere. This decrease occurs because the front inversion charge density decreases as V_{Gb} raises the electric field in the silicon film. Heavy accumulation at the back surface, for high V_D, suppresses I_D significantly because the high electric field degrades the mobility in addition to decreasing the inversion charge density. Also because of the change in the electric field, the drain saturation voltage decreases (linearly with V_{Gb}) as the back surface is biased from depletion to accumulation.

II. ANALYSIS

The device we analyze is the four-terminal n-channel enhancement-mode SOI MOSFET illustrated in Fig. 1. It is fabricated in a thin silicon film on an insulating layer of silicon dioxide, which has been formed on a silicon substrate. The front (conventional metal or polysilicon) and back (silicon substrate) gates compete for charge in the film body, which is manifested as the dependence of I_D on V_{Gb}. Although the analysis refers directly to the device structure in Fig. 1, it can be applied to any MISFET device, e.g., the SOS MOSFET.

In the derivation of expressions for $I_D(V_{Gf},V_{Gb},V_D)$, we use the common assumptions used for the bulk MOSFET in strong inversion [10]: constant mobility, long channel (gradual-channel approximation), uniform doping, and

negligible diffusion current. For a strongly inverted n-channel MOSFET, the current in the (front) channel ($0 < y < L$) is [10]

$$I_D = Z\,\mu_{nf}\,|Q_n(y)|\,\frac{d\psi_{sf}(y)}{dy} \tag{1}$$

where $Q_n(y)$ is the inversion (electron) charge density, $\psi_{sf}(y)$ is the front surface potential (band bending) [8], and μ_{nf} is the electron mobility in the channel. Integration of (1) from source (y=0) to drain (y=L) yields

$$I_D = \frac{Z}{L}\,\mu_{nf}\int_{2\phi_B}^{2\phi_B + V_D} |Q_n(y)|\,d\psi_{sf}(y) \tag{2}$$

where the limits $\psi_{sf}(0) = 2\phi_B$ and $\psi_{sf}(L) = 2\phi_B + V_D$ are the commonly assumed strong-inversion conditions [10].

If the silicon film is completely depleted at arbitrary y, then $Q_n(y)$ is obtained from the one-dimensional charge-coupling analysis [8] that combines Poisson's equation in the depleted silicon film with Gauss' theorem at the front and back Si-SiO_2 interfaces:

$$|Q_n(y)| = C_{of}\left[V_{Gf} - V_{FB}^f - \left(1 + \frac{C_b}{C_{of}}\right)\psi_{sf}(y) + \frac{C_b}{C_{of}}\,\psi_{sb}(y) + \frac{Q_b}{2C_{of}}\right] \tag{3}$$

where

$$\psi_{sb}(y) = \frac{C_{ob}}{C_{ob} + C_b}\left[V_{Gb} - V_{FB}^b + \frac{C_b}{C_{ob}}\,\psi_{sf}(y) + \frac{Q_b}{2C_{ob}} + \frac{Q_{cb}(y)}{C_{ob}}\right] \tag{4}$$

is the back surface potential. In (3) and (4), V_{FB}^f and V_{FB}^b are the conventionally defined [10] front- and back-gate flatland voltages, C_{of} and C_{ob} are the front and back oxide capacitances, $C_b = \varepsilon_s/t_b$ is the depletion

capacitance of the silicon film, $Q_b = -qN_A t_b$ is the depletion areal charge density, and Q_{cb} is the back-surface carrier charge density. In the derivation [8] of (3) and (4) we assumed, with justification, that the accumulation or inversion layer is much thinner than the silicon film thickness t_b and that the potential drop across the layer is negligible. We also neglected the potential drop in the silicon substrate (back gate) and the possible charging of surface-states at the back Si-SiO_2 interface, both of which shift the flatband voltage of the back gate but are relatively unimportant [8] with regard to I_D.

If the silicon film is sufficiently thick $[t_b > x_{d(max)} = (4\varepsilon_s\phi_B/qN_A)^{1/2}]$, it can be only partially depleted, which renders (3) and (4) not strictly valid. At points where this is the case, $Q_n[\psi_{sf}(y)]$ is given by the bulk MOSFET theory [10], and I_D in (2) is derived by appropriately using it or (3) and (4) as determined by $\psi_{sf}(y)$ [7]. Because $Q_n[\psi_{sf}(y)]$ is nonlinear where the film is not completely depleted, this derivation yields extremely complicated results Simpler but sufficiently accurate results for typical SOI MOSFETs are obtained by using the linear $Q_n[\psi_{sf}(y)]$ given by (3) and (4) irrespective of whether or not a neutral region exists under part of the channel. We discuss in Appendix A the physical basis for this approximation and show that it typically results in less than 5% error in I_D provided the film is completely depleted at the drain, which usually obtains in normal operation. Thus we develop our $I_D(V_{Gf},V_{Gb},V_D)$ model based on (3) and (4), i. e., $t_b < x_{d(max)}$, but we note that it is generally applicable.

Combining (2), (3), and (4), we obtain simplified expressions for I_D in terms of V_{Gf}, V_{Gb}, and V_D. We first define the values of V_{Gb} corresponding to the onsets of back-surface accumulation and inversion at the source and drain,

and then derive current expressions for each of the possible charge conditions at the back surface. We do not analyze the case in which the back surface is inverted; it is generally avoided to keep the leakage current low.

At sufficiently low values of V_{Gb}, the back surface is accumulated everywhere from source to drain. As V_{Gb} is increased, eventually, at $V_{Gb} = V_{Gb}^{A}(L)$, the back surface at the drain becomes depleted as implied by (4). From (4) with $\psi_{sf}(L) = V_D + 2\phi_B$, $\psi_{sb}(L) = 0$, and $Q_{cb}(L) = 0$,

$$V_{Gb}^{A}(L) = V_{Gb}^{A} - \frac{C_b}{C_{ob}} V_D \tag{5}$$

where

$$V_{Gb}^{A} \triangleq V_{FB}^{b} - \frac{C_b}{C_{ob}} 2\phi_B - \frac{Q_b}{2C_{ob}} \tag{6}$$

is the back-gate voltage coresponding to the onset of back-surface accumulation when $\psi_{sf} = 2\phi_B$ [8]. If the device is saturated, V_D in (5) must be replaced by $V_{D(sat)}^{A}$, which will be defined in Subsection II-A. As V_{Gb} is increased above $V_{Gb}^{A}(L)$, the depleted portion of the back surface expands toward the souce until, at $V_{Gb} = V_{Gb}^{A}$, the back surface is completely depleted. As V_{Gb} is increased above V_{Gb}^{A}, the back surface remains depleted until V_{Gb} reaches V_{Gb}^{I} [8], at which the back surface becomes inverted. From (4) we find that the minimum value of V_{Gb} required to invert the back surface is defined when $\psi_{sf}(0) = \psi_{sb}(0) = 2\phi_B$ and $Q_{cb}(0) = 0$:

$$V_{Gb}^{I} = V_{FB}^{b} + 2\phi_B - \frac{Q_b}{2C_{ob}} \quad . \tag{7}$$

A. Back Surface Accumulated from Source to Drain [$V_{Gb} < V_{Gb}^{A}(L)$]

When the back surface is everywhere accumulated, $\psi_{sb}(y)$ is virtually pinned at zero. Then combining (2) and (3), we get

$$I_D = I_D^A \triangleq \frac{Z}{L} \mu_{nf} C_{of} \left[(V_{Gf} - V_{Tf}^A) V_D - (1 + \frac{C_b}{C_{of}}) \frac{V_D^2}{2} \right] \tag{8}$$

where V_{Tf}^A is the (front-gate) threshold voltage ($\psi_{sf} = 2\phi_B$) when the back surface is accumulated [8]:

$$V_{Tf}^A \triangleq V_{FB}^f + (1 + \frac{C_b}{C_{of}}) 2\phi_B - \frac{Q_b}{2C_{of}} \quad . \tag{9}$$

As is evident in (8), I_D^A does not depend on V_{Gb} because the accumulated charge prohibits modulation by V_{Gb} of the electric field in the silicon film.

The drain voltage $V_{D(sat)}$ at which the drain current saturates is obtained from

$$\left. \frac{\partial I_D}{\partial V_D} \right|_{V_D = V_{D(sat)}} = 0 \quad . \tag{10}$$

Combining (8) and (10), we obtain

$$V_{D(sat)} = V_{D(sat)}^A \triangleq \frac{V_{Gf} - V_{Tf}^A}{1 + C_b/C_{of}} \quad . \tag{11}$$

The saturated drain current $I_{D(sat)}$ is obtained by evaluating (8) at $V_D = V_{D(sat)}^A$:

$$I_{D(sat)} = I_{D(sat)}^A \triangleq \frac{Z}{L} \frac{\mu_{nf} C_{of}}{2(1 + C_b/C_{of})} (V_{Gf} - V_{Tf}^A)^2 \quad . \tag{12}$$

We note that although (8) and (12) resemble corresponding approximate expressions for the bulk MOSFET [10], they are exact for the thin-film SOI MOSFET. They are simplified in this case because Q_n in (3) varies linearly with ψ_{sf}.

B. Back Surface Depleted from Source to Drain $[V_{Gb}^A < V_{Gb} < V_{Gb}^I]$

When the back surface is everywhere depleted, $Q_{cb}(y) = 0$, and (2), (3) and (4) yield

$$I_D = I_D^D \triangleq \frac{Z}{L} \mu_{nf} C_{of} \left[(V_{Gf} - V_{Tf}) V_D - (1 + \frac{C_{bb}}{C_{of}}) \frac{V_D^2}{2} \right] \tag{13}$$

where the effective body capacitance $C_{bb} \triangleq \frac{C_{ob} C_b}{C_{ob} + C_b}$ is the series combination of C_b and C_{ob}, and V_{Tf} is the (front-gate) threshold voltage when the back surface is depleted [8]:

$$V_{Tf} = V_{Tf}^A - \frac{C_{bb}}{C_{of}} (V_{Gb} - V_{Gb}^A) \quad . \tag{14}$$

In this case, as we see from (13) and (14), I_D increases with increasing V_{Gb} because V_{Tf} decreases.

Using (10) and (13), we obtain

$$V_{D(sat)} = V_{D(sat)}^D \triangleq \frac{V_{Gf} - V_{Tf}}{1 + C_{bb}/C_{of}} \quad , \tag{15}$$

which when inserted into (13) gives

$$I_{D(sat)} = I_{D(sat)}^D \triangleq \frac{Z}{L} \frac{\mu_{nf} C_{of}}{2(1 + C_{bb}/C_{of})} (V_{Gf} - V_{Tf})^2 \quad . \tag{16}$$

Note that the resulting expressions for this case are identical to those for the previous case [Subsection II-A] but with V_{Tf}^A and C_b replaced by V_{Tf} in (14) and C_{bb} respectively.

C. Back Surface Accumulated Near Source and Depleted Near Drain $[V_{Gb}^A(L) < V_{Gb} < V_{Gb}^A]$

When V_D is high, the back surface can be depleted near the drain even though it remains accumulated near the source. If such a transition in the charge condition of the back surface occurs at $y = y_t$, (2) must be rewritten as

$$I_D = \frac{Z}{L}\mu_{nf}\left[\int_{2\phi_B}^{\psi_{sf}(y_t)} |Q_n(y)|_{\psi_{sb}(y)=0} d\psi_{sf}(y) + \int_{\psi_{sf}(y_t)}^{2\phi_B+V_D} |Q_n(y)|_{Q_{cb}(y)=0} d\psi_{sf}(y)\right] \quad ; \tag{17}$$

$\psi_{sf}(y_t)$ is given by (4) with $\psi_{sb}(y_t) \simeq 0$ and $Q_{cb}(y_t) \simeq 0$:

$$\psi_{sf}(y_t) \simeq 2\phi_B + \frac{C_{ob}}{C_b}(V_{Gb}^A - V_{Gb}) \quad . \tag{18}$$

Combining (17) and (18), yields

$$I_D = I_D^{AD} \triangleq \frac{Z}{L}\mu_{nf}C_{of}\left[(V_{Gf} - V_{Tf}^A)V_D - (1 + \frac{C_{bb}}{C_{of}})\frac{V_D^2}{2} - \frac{C_{bb}}{C_{of}}V_D(V_{Gb}^A - V_{Gb}) + \frac{C_{bb}}{2C_{of}}\frac{C_{ob}}{C_b}(V_{Gb}^A - V_{Gb})^2\right] \tag{19}$$

Note that I_D^{AD} increases with increasing V_{Gb} because y_t decreases, i.e., more of the back surface becomes depleted, and hence the dependence defined in Subsection II-B becomes more prevalent.

From (10) and (19), we get

$$V_{D(sat)} = V_{D(sat)}^{AD} \triangleq \frac{V_{Gf} - V_{Tf}^A - \frac{C_{bb}}{C_{of}}(V_{Gb}^A - V_{Gb})}{1 + C_{bb}/C_{of}} \tag{20}$$

and

$$I_{D(sat)} = I_{D(sat)}^{AD} \triangleq \frac{Z}{L}\frac{\mu_{nf}C_{of}}{2(1 + C_{bb}/C_{of})}\left[(V_{Gf} - V_{Tf}^A)^2 - 2\frac{C_{bb}}{C_{of}}(V_{Gf} - V_{Tf}^A)(V_{Gb}^A - V_{Gb})\right.$$

$$\left. + \frac{C_{ob}}{C_{of}}\frac{C_{bb}}{C_{bf}}(V_{Gb}^A - V_{Gb})^2\right] \tag{21}$$

where $C_{bf} \triangleq \frac{C_{of}\,C_b}{C_{of} + C_b}$ is the series combination of C_b and C_{of}. Because $V_{D(sat)}$ is defined by the back-surface charge condition at the drain, (20) is identical to (15). We note that the results of this subsection reduce to those of Subsections II-A and II-B when V_{Gb} equals $V_{Gb}^A(L)$ and V_{Gb}^A respectively.

III. EXPERIMENTAL SUPPORT AND DISCUSSION

To provide experimental support for the analysis, we measured current-voltage characteristics of four-terminal SOI MOSFETs (n-channel) fabricated at Texas Instruments, Inc. [11]. The silicon film in which they were fabricated is 0.5-μm-thick and was laser-recrystallized after being deposited on a 1-

μm-thick SiO_2 layer, which had been thermally grown on a silicon substrate (p-type, 6-8 Ω-cm). The film was doped by ion implantation of boron that yielded based on SUPREM-II calculations [11], $N_A \simeq 2 \times 10^{16}$ cm^{-3} near the front surface and $N_A \simeq 10^{15}$ cm^{-3} at the back surface The front gate is n^+ polysilicon, and the gate oxide is 600-A-thick ($C_{of} \simeq 5.8 \times 10^{-8}$ F/cm^2). The devices are large (Z = L = 40 μm), and hence small-geometry effects are negligible.

These devices differ in three ways from the device on which the analysis in Section II is based. First, they have grain boundaries in the (poly)silicon film body, which at relatively low V_{Gf} affect the channel conductance [12]. At high enough V_{Gf} (>2 V) however, the grain-boundary effects are negligible. Second, the doping density in the film body is not uniform. Although this nonuniformity enhances the $V_{Tf}(V_{Gb})$ dependence [8], it does not significantly affect the current-voltage characteristics well above threshold as indicated in Section II. Third, for V_{Gb} sufficiently negative, e.g , when the back surface is accumulated, the film body is not completely depleted for low V_D, especially near the source. To account for incomplete depletion analytically is quite tedious as shown in [7], but, as we demonstrate in Appendix A, our simplified model is valid for these devices.

We plot in Fig. 2 the measured and calculated $I_D(V_D)$ characteristics of a representative device with V_{Gf} = 4 V and 6 V and V_{Gb} = 0 V and -80 V. The values of V_{Gb} were selected, based on measured $I_D(V_{Gb})$ characteristics, to deplete and accumulate, respectively, the entire back surface. We found from $I_D(V_{Gb})$ in the linear and saturation regions that $V_{Gb}^I \simeq 0$ V and $V_{Gb}^A(L) > -80$ V respectively. For the calculation of I_D, the threshold voltages [$V_{Tf}^A \simeq 0.3$ V, $V_{Tf}(V_{Gb} = 0\ V) \simeq 0.1$ V] and the (maximum) electron mobility ($\mu_{nf} \simeq 420$ $cm^2/V\text{-sec}$) were determined from the measured $I_D(V_{Gf})$ in

the linear region. At V_{Gf} = 4 V, we have good agreement between the measured and calculated results, except for the small "kink effect" at high V_D [9]. However at V_{Gf} = 6 V, the measured I_D is somewhat lower than the calculated I_D, especially for low V_D and at V_{Gb} = -80 V. This slight discrepancy can be explained by analyzing the dependences of μ_{nf} on the terminal voltages, which we do in Appendix B.

In Appendix B we show that the effective mobility in the linear region, μ_{lin}, is virtually independent of V_{Gb}, and $\mu_{lin}(V_{Gf})$ can be described well using an empirical mobility model [13] developed for the bulk MOSFET. However when the device is saturated, the effective mobility μ_{sat}, which is an average value across the channel, is strongly dependent on V_{Gb}. The mobility near the drain is higher than that near the source because $|Q_n(L)| < |Q_n(0)|$ and hence the effective normal electric field E_{eff} in (B.2) is lower. Consequently μ_{sat} is higher than μ_{lin} and depends on V_{Gb} because $E_{eff}(L)$ does. Based on the analysis in Appendix B, we estimate that at V_{Gf} = 8 V, $\mu_{sat}(V_{Gb} \simeq V_{Gb}^I)$ is about 15% lower than the maximum mobility (420 cm^2/V-sec) whereas $\mu_{sat}[V_{Gb} < V_{Gb}^A(L)]$ is about 22% lower than the maximum value; μ_{lin}, independent of V_{Gb}, is about 25% lower than the maximum mobility These differences are large enough to cause the discrepancy in Fig. 2 noted above and those to be noted below. The mobility degradation is most severe for low V_D and/or when the back surface is accumulated.

The drain conductance, g_d (= $\partial I_D/\partial V_D$), can be generally expressed, based on (8), (13), and (19), as

$$g_d = \frac{Z}{L} \mu_{nf} C_{of} \left[V_{Gf} - V_{Tf} - (1 + \frac{C_{body}}{C_{of}}) V_D \right] \tag{22}$$

where V_{Tf} is given by (9) or (14) depending on V_{Gb}, and where the effective

body capacitance C_{body} varies from C_b to C_{bb} as the back-surface charge condition is changed from accumulation to depletion. In contrast to the bulk MOSFET, C_{body} is a constant independent of V_D when the back-surface charge condition is uniform. Thus g_d decreases linearly with increasing V_D and the slope is determined by V_{Gb}, which defines C_{body}. We plot in Fig. 3 measured and calculated $g_d(V_D)$ for V_{Gf} = 4 V and 6 V and for V_{Gb} = 0 V and -80 V. We have good agreement between theory and experiment except for V_{Gf} = 6 V and V_D < 1 V where the measured g_d is considerably lower due to the mobility degradation. The influence of V_{Gb} on the slope of the plots is apparent from the data. Note that for $V_{Gb} < V_{Gb}^A$, $C_{body} = C_b$ when V_D is low enough that $V_{Gb} < V_{Gb}^A(L)$; otherwise, for higher V_D, $C_{body} = C_{bb}$. Hence for such intermediate-V_{Gb} cases, the $g_d(V_D)$ characteristic will show a change of slope at the value of V_D defined by $V_{Gb}^A(L) = V_{Gb}$.

Measured dependences of $I_{D(sat)}$ on V_{Gf} ($=V_D$) are plotted with the calculated dependences in Fig. 4 for V_{Gb} = 0 V, -20 V, and -80 V. We have good agreement between theory and experiment except for the high-V_{Gf} portion of the V_{Gb} = -80 V curve, where the mobility degradation again reduces the current considerably. The theory, based on constant μ_{nf}, predicts about a 30% decrease in $I_{D(sat)}$ at V_{Gf} = 8 V when V_{Gb} decreases from 0 V to -80V. Actually, because of the mobility degradation the measured current decreases by 35%. The V_{Gb} = -20 V curve is plotted to show the $I_{D(sat)}(V_{Gf})$ characteristic for a nonuniform back-surface charge condition. The plot coincides with the V_{Gb} = -80 V curve at low V_{Gf} until the back surface becomes depleted near the drain at $V_{Gf} \approx 3$ V. For larger V_{Gf} values, the drain current was calculated from $I_{D(sat)}^{AD}$ in (19) where $V_{Gb}^A \approx -6$ V was determined from the $I_{D(sat)}(V_{Gb})$ measurement using

$$\left.\frac{I_{D(sat)}}{I^{A}_{D(sat)}}\right|_{V_{Gb}=V^{A}_{Gb}} = \frac{1 + C_b/C_{of}}{1 + C_{bb}/C_{of}} \tag{23}$$

The relationship (23), which follows from (12) and (16), provides a theoretical basis for determining V^{A}_{Gb} from $I_{D(sat)}(V_{Gb})$ measured at low V_{Gf} such that μ_{nf} has negligible dependence on V_{Gb}. The use of (23) is exemplary of the utility of our simplified model.

The dependence of $I_{D(sat)}$ on V_{Gb} is illustrated in more detail in Fig. 5. For a given value of V_{Gf}, we see that $I_{D(sat)}$ decreases with decreasing V_{Gb} until it saturates when the back surface becomes completely accumulated [at $V_{Gb} = V^{A}_{Gb}(L)$]. Note that $V^{A}_{Gb}(L)$ decreases (becomes more negative) with increasing V_{Gf} as predicted by (5) and (11). The slight discrepancies between the measured and calculated $I_{D(sat)}$ at low V_{Gb} and high V_{Gf} are due to the mobility degradation discussed previously. The discrepancies in $V^{A}_{Gb}(L)$ are probably due to surface states at the back Si-SiO_2 interface [8], which tend to stretch-out the curves.

The dependence of $V_{D(sat)}$ on V_{Gf} and V_{Gb} is shown in Fig. 6. As predicted by (11) and (15), $V_{D(sat)}$ increases linearly with increasing V_{Gf} unlike the bulk MOSFET characteristic, and the slope is again determined by V_{Gb}. Two methods were used to measure $V_{D(sat)}$ to better support the analysis. First, from the $g_d(V_D)$ plots in Fig. 3, $V_{D(sat)}$ was taken as the intercept of the linear extrapolation on the V_D axis. Second, $V_{D(sat)}$ was taken as the value of V_D at which I_D is 99% of $I_{D(sat)}$ in Fig. 4. Both measured values agree well with the theoretical predictions; the influence of V_{Gb} is modeled well.

The SOI MOSFET transconductance, g_m $(=\partial I_D/\partial V_{Gf})$, differs considerably from that of the bulk counterpart in the saturation region. From (12), (16), and (21),

$$g_{m(sat)} = \frac{Z}{L} \frac{\mu_{nf} C_{of}}{(1 + C_{body}/C_{of})} (V_{Gf} - V_{Tf}) \quad (24)$$

varies linearly with V_{Gf}, unlike in the bulk MOSFET, and depends on V_{Gb} through V_{Tf} [8] and C_{body} defined previously with reference to (22). For high V_{Gf}, the device comes out of saturation, and from (8), (13), and (19),

$$g_m = \frac{Z}{L} \mu_{nf} C_{of} V_D \quad (25)$$

like in the bulk MOSFET. Calculated and measured values of $g_m(V_{Gf})$ at V_D = 4 V for V_{Gb} = 0 V and -80 V are plotted in Fig. 7. For low V_{Gf}, (24) applies and the influence of V_{Gb} on the slope of the characteristic is evident. For high V_{Gf}, g_m is independent of V_{Gb} as predictd by (25). The measured g_m in this region is 20-25% lower than the predicted g_m, which is consistent with the previously estimated mobility degradation. The plots support our notion that the μ_{sat} degradation due to high V_{Gf} is much more severe when the back surface is accumulated (V_{Gf} = 3-5V) and that the μ_{in} degradation is almost independent of V_{Gb} (V_{Gf} = 6-8 V).

As intimated by our theoretical-experimental analysis, the drain current of an SOI MOSFET can be either higher or lower than that of the bulk counterpart depending on V_{Gb}. Typically the conductance of the SOI MOSFET is higher than that of the bulk MOSFET when the back surface is depleted, and lower when the back surface is accumulated. The optimal V_{Gb} bias, at which I_D is maximized without increased leakage current, is theoretically V_{Gb}^A (when $t_b < x_{d(max)}$). At this bias, when the device is ON, I_D is high because the body capacitance (C_{bb}) is low, and when the device is OFF, the leakage current is minimized. Increasing V_{Gb} above V_{Gb}^A might increase the OFF leakage whereas lowering V_{Gb} reduces the ON current.

Reducing the silicon film body thickness, which is necessary for fine lithography, results in strong charge-coupling and hence more significant influence of V_{Gb} on the (front-channel) current-voltage characteristics This influence can be used advantageously for some applications. For example, an SOI MOSFET in a low-doped silicon film, in which the carrier mobility is high, can have an acceptable threshold voltage if V_{Gb} is properly selected [8].

From our analysis we see that the dependence of I_D on V_{Gb} is described by an effective silicon film body capacitance C_{body}, which decreases from C_b to C_{bb} as V_{Gb} alters the back-surface charge condition from accumulation to depletion. This capacitance, which is determined by the thicknesses of the silicon film and the back insulator, is independent of N_A as long as the film is completely depleted. Thus, except for the threshold voltage, the current-voltage characteristics of a completely depleted SOI MOSFET are virtually insensitive to the actual doping density profile $N_A(x)$.

It is common in the fabrication of n-channel SOI MOSFETs to implant boron deep into the silicon film to avoid inversion at the back surface. This implantation produces a highly doped region near the back surface that prevents complete depletion of the silicon film at low V_D (linear region). At high V_D (~5 V typically) however, even this highly doped region can be depleted near the drain, rendering the front channel conductance dependent on V_{Gb}. Since the highly doped region at the back surface is tantamount to an accumulation layer [8], I_D for this case can be modeled similarly to I_D^{AD}. Heavy deep boron implantation will suppress I_D because, in addition to increasing V_{Tf} [8], it tends to prevent depletion at the back surface and hence results in higher body capacitance

IV. SUMMARY

The dependence of the inversion charge density [$Q_n(y)$] on the terminal voltages of strongly inverted thin-film SOI MOSFETs has been modeled using a one-dimensional charge-coupling analysis [8], and simple closed-form expressions for drain current in all regions of operation have been derived. The model was simplified, without significant loss of accuracy, by recognizing that Q_n is approximated well by a linear function of the surface potential, which describes Q_n exactly when the silicon film is completely depleted. The I_D expressions, which are simpler than those for bulk MOSFETs when the back surface charge condition is uniform, clearly show the dependence of the current-voltage characteristics on the back-gate bias V_{Gb} and on the device parameters, e.g., the silicon film thickness and the doping density.

The analysis was supported by measurements of current-voltage characteristics of thin-film SOI MOSFETs fabricated in laser-recrystallized silicon. These measurements included the dependences of drain current (I_D, $I_{D(sat)}$), of conductances (g_d, g_m), and of saturation voltage ($V_{D(sat)}$) on the terminal voltages (V_{Gf}, V_{Gb}, V_D), and agreed well with the theoretical predictions. Some discrepancies were noted, but were attributed to the degradation of carrier mobility at high V_{Gf}, especially for low V_D and/or when the back surface is accumulated. The average mobility in the saturated device (μ_{sat}) has a strong dependence on V_{Gb}, which enhances the influence of V_{Gb} on I_D.

The drain current of the thin-film SOI MOSFET can be either higher or lower than that of the bulk MOSFET, for a given threshold voltage and mobility, depending on the back-surface charge condition as determined by V_{Gb} and the back Si-SiO_2 properties. We note that the high (saturated) current drive capability of the SOI MOSFET relative to the bulk counterpart that has

been reported [14] and attributed to high carrier mobility is quite possibly due to the low effective body capacitance (C_{bb}) that obtains when the back surface is depleted. With the leakage current minimized, the drain current will be maximized when V_{Gb} is biased at V_{Gb}^{A}, i.e., at the onset of back-surface accumulation at the source. At this bias, the back surface is depleted when the device is ON, whereas when the device is OFF the back surface is accumulated and the leakage current is suppressed.

APPENDIX A

Accuracy of the Simplified Model

The simplified $I_D(V_{Gf},V_{Gb},V_D)$ model developed in Section II is based on the linear $Q_n(\psi_{sf})$ relationship given by (3) and (4), which is strictly valid only when the silicon film is completely depleted. If $t_b > x_{d(max)}$, a neutral region can exist near the source. Over this region $Q_n(\psi_{sf})$ is described by the bulk MOSFET theory [10]:

$$|Q_n(y)| = C_{of}\left\{V_{Gf} - V_{FB}^f - \psi_{sf}(y) - \frac{1}{C_{of}}[2\varepsilon_s qN_A\psi_{sf}(y)]^{1/2}\right\} \quad . \qquad (A.1)$$

In this Appendix we show that using (3) and (4) instead of (A.1) results in negligible error in our model for typical SOI MOSFETs.

This error is illustrated in Fig. A.1 where we plot $Q_n(\psi_{sf})$ defined by (A.1) and by (3) and (4). The curved portion of the plot, which is described by (A.1), depicts the typical case in which $x_{d(max)} < t_b < 2x_{d(max)}$ but the silicon film is completely depleted at the drain. The straight lines follow from (3) and (4) at the three onset values of V_{Gb} defined in Section II. The dashed portions of the lines indicate where discrepancies in $Q_n(\psi_{sf})$ occur. The corresponding error in I_D [described by (2)] is proportional to the area between the $Q_n(\psi_{sf})$ curve and the appropriate (depending on V_{Gb}) dashed line. Note that the error is maximum when the back surface is accumulated everywhere [$V_{Gb} < V_{Gb}^A(L)$].

We have evaluated this maximum error for $N_A \leq 2 \times 10^{16}$ cm^{-3}, $t_b \leq 1$ μm, and $t_{of} \leq 600$Å by comparing I_D predicted by our simplified model with that obtained by the more rigorous analysis [7] using (A.1) as described in Section II. For these ranges of parameter values, which cover most of the

contemporary SOI MOSFETs, we found that the error never exceeded about 5% when the silicon film was completely depleted at the drain. The error is smaller for lower N_A and thinner t_{of}. With reference to Fig. A.1, we note that the accuracy of the simplified model is ensured because the slope of the nonlinear $Q_n(\psi_{sf})$ curve $[C_{of} + C_d = C_{of} + (\varepsilon_s q N_A / 2\psi_{sf})^{1/2}]$ does not differ appreciably from $C_{of} + C_b$ for typical devices. Thus the model is sufficiently accurate for all thin-film devices that cannot be modeled as a bulk MOSFET.

APPENDIX B

Dependence of Carrier Mobility on Terminal Voltages

The position-dependent carrier mobility in a strongly inverted long-channel MOSFET can be characterized empirically as [13]

$$\mu_{nf}(y) = \mu_{max}\left[\frac{E_c}{E_{eff}(y)}\right]^{c_1} \qquad \text{for } E_{eff}(y) > E_c \tag{B.1}$$

where μ_{max}, E_c, and c_1 are fitting parameters that depend on the gate oxidation process and the device properties, and

$$E_{eff}(y) = E_{sf}(y) + \frac{|Q_n(y)|}{2\varepsilon_s} \quad . \tag{B.2}$$

In (B.2), $E_{sf}(y)$ is the normal electric field at the interface between the front inversion layer and the depletion region. It is described by solving Poisson's equation in the depleted silicon film [8]:

$$E_{sf}(y) = \frac{-Q_b}{2\varepsilon_s} + \frac{\psi_{sf}(y) - \psi_{sb}(y)}{t_b} \quad . \tag{B.3}$$

Combining (B.1), (B.2), and (B.3) with the $Q_n[\psi_{sf}(y),\psi_{sb}(y)]$ relationship described by (3) and (4), we can characterize $\mu_{nf}(y)$ in terms of $Q_n(y)$.

For the device described in Section III, we plot in Fig. B.1 the measured and calculated linear-region mobility $\mu_{lin}(V_{Gf})$ for V_{Gb} = 0 V ($\simeq V_{Gb}^{I}$) and -80 V [$< V_{Gb}^{A}(L)$]. In the calculations we used $Q_n(y) \simeq Q_n(0) \simeq C_{of}(V_{Gf}-V_{Tf})$, and we assumed an average value $N_A = 10^{16}$ cm^{-3} for the nonuniform doping density. The fitting parameters μ_{max} = 420 cm^2/V-sec, c_1 = 0.4, and E_c = 1 25 x 10^5 V/cm in (B.1) were determined from the log-log plot of the measured μ_{lin} versus the calculated E_{eff}. We see good agreement in Fig. B.1 between the measured and calculated plots when V_{Gf} > 2 V where the grain boundaries in the film have negligible effects. Note that μ_{lin} is virtually independent of V_{Gb} because E_{sf} in (B.3), which conveys the main V_{Gb} dependence, is low and hence does not strongly affect E_{eff}.

For high V_D however, $E_{sf}(y)$ is high near the drain, and its strong dependence on V_{Gb} is thus reflected by $E_{eff}(y)$ and $\mu_{nf}(y)$. We plot in Fig. B.2 the calculated $\mu_{nf}(y)/\mu_{max}$ of the measured device in the saturation region for V_{Gf} = 8 V and V_{Gb} = 0 V and -80 V. The same fitting parameters and $Q_n(y) \simeq Q_n(0)(1-y/L)^{1/2}$, which can be obtained by integrating (1), were used in the calculations. Unweighted averaging across the channel of $\mu_{nf}(y)$ in Fig. B.2 defines the effective mobility μ_{sat} ($I_{D(sat)} \tilde{\propto} \mu_{sat}$) and its appreciable dependence on V_{Gb}. Note that this dependence is due mainly to the influence of V_{Gb} on $\mu_{nf}(y)$ near the drain.

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FIGURE CAPTIONS

Fig. 1. Four-terminal n-channel SOI MOSFET structure.

Fig. 2. Measured (points) and calculated (curves) current-voltage characteristics of the typical SOI MOSFET described in Section III.

Fig. 3. Measured (points) and calculated (lines) drain conductance versus the terminal voltages of the SOI MOSFET. The discrepancies between the theoretical and experimental results at low V_D are due to mobility degradation.

Fig. 4. Measured (points) and calculated (curves) saturated drain current versus the gate voltages of the SOI MOSFET. The measurements were made with the drain terminal connected to the front gate. The discrepancy for high V_{Gf} and V_{Gb} = -80 V is due to mobility degradation.

Fig. 5. Measured (points) and calculated (curves) dependences of $I_{D(sat)}$ on V_{Gb}.

Fig. 6. Measured (points) and calculated (lines) drain saturation voltage versus the gate voltages of the SOI MOSFET. The triangular data points were estimated from the $g_d(V_D)$ plots in Fig. 3; the circular data points were obtained by taking the value of V_D at which I_D is 99% of $I_{D(sat)}$ in Fig. 4. Note that V_{Tf} is 0.1 V and 0.3 V for V_{Gb} equal to 0 V and -80 V respectively.

Fig. 7. Measured (points) and calculated (lines) transconductance at V_D = 4 V versus the gate voltages of the SOI MOSFET. The discrepancies for high V_{Gf} are due to mobility degradation.

Fig. A.1. Illustration of the dependence of Q_n on ψ_{sf}. The curved characteristic is given by (A.1); the straight lines are from (3) and (4). The slopes of the lines are indicated. The threshold voltages $V_{Tf}^{I} = V_{FB}^{f} + 2\phi_B - Q_b/2C_{of}$ and $V_{TfO} = V_{FB}^{f} + 2\phi_B + qN_A x_{d(max)}/C_{of}$ are described in [8].

Fig. B.1. Measured (points) and calculated (curves) linear-region (electron) mobilitiy versus the gate voltages of the SOI MOSFET. The measured values were obtained from the $I_D(V_{Gf})$ characteristic at V_D = 50 mV.

Fig. B.2. Calculated mobility variation along the channel of the saturated device at V_{Gf} = 8 V and V_{Gb} = 0 V and -80 V. The maximum mobility μ_{max} = 420 cm^2/V-sec obtains at low V_{Gf} as shown in Fig. B.1.

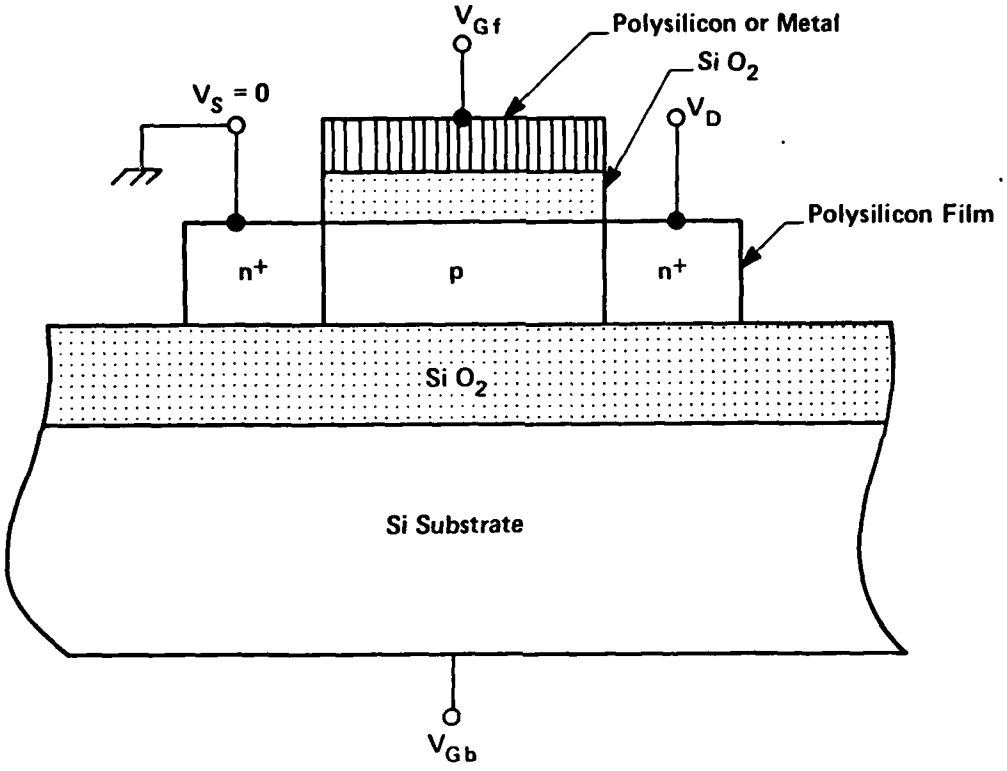
V_{Gf}
Polysilicon or Metal
Si O_2
$V_S = 0$
V_D
Polysilicon Film
n^+
p
n^+
Si O_2
Si Substrate
V_{Gb}

Fig. 1

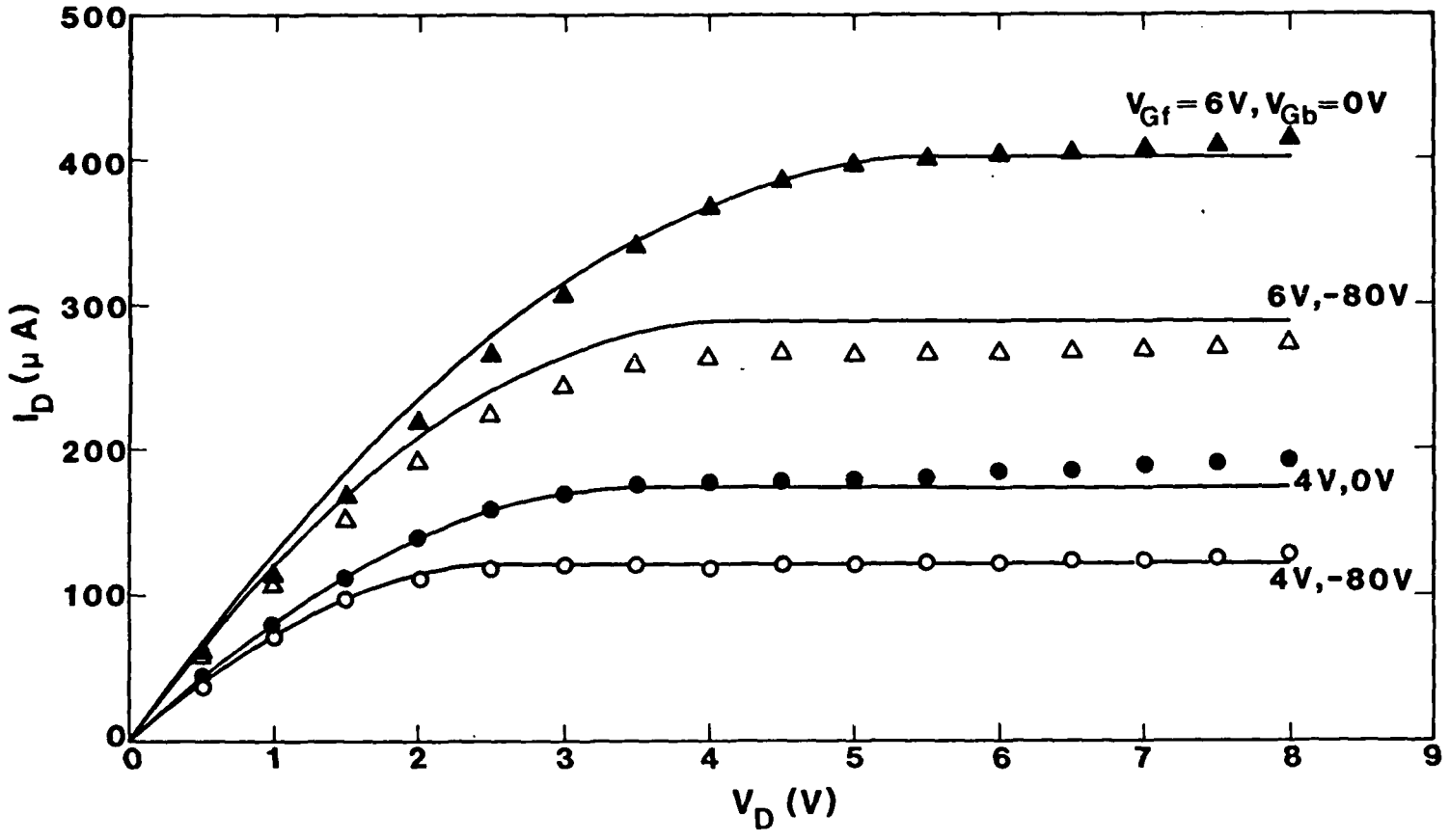
500
400
300
200
100
0
I_D (μA)
0
1
2
3
4
5
6
7
8
9
V_D (V)
V_{Gf} = 6V, V_{Gb} = 0V
6V,-80V
4V,0V
4V,-80V

Fig. 2

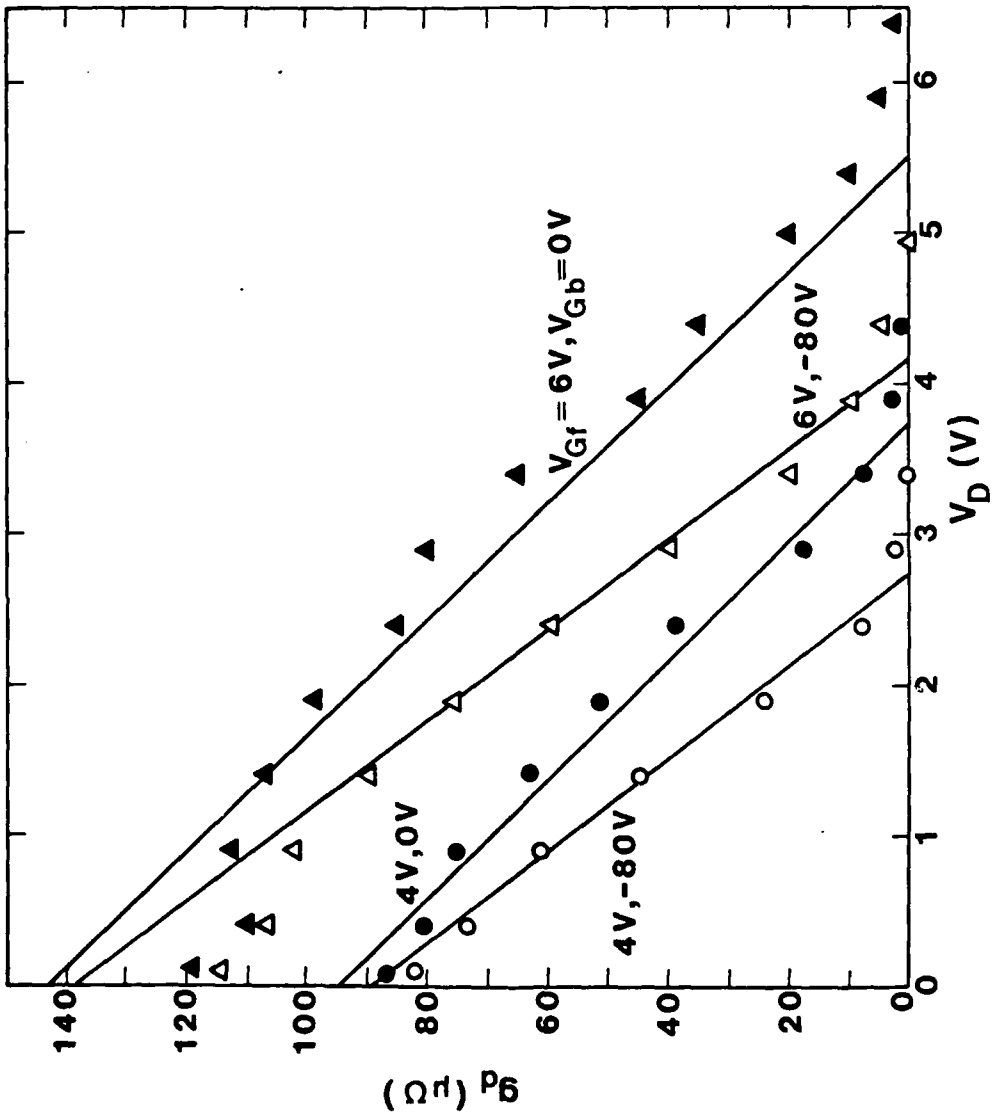
V_{Gf}=6V,V_{Gb}=0V
6V,-80V
4V,0V
4V,-80V
g_d (μΩ)
V_D (V)
0
20
40
60
80
100
120
140
0
1
2
3
4
5
6

Fig. 3

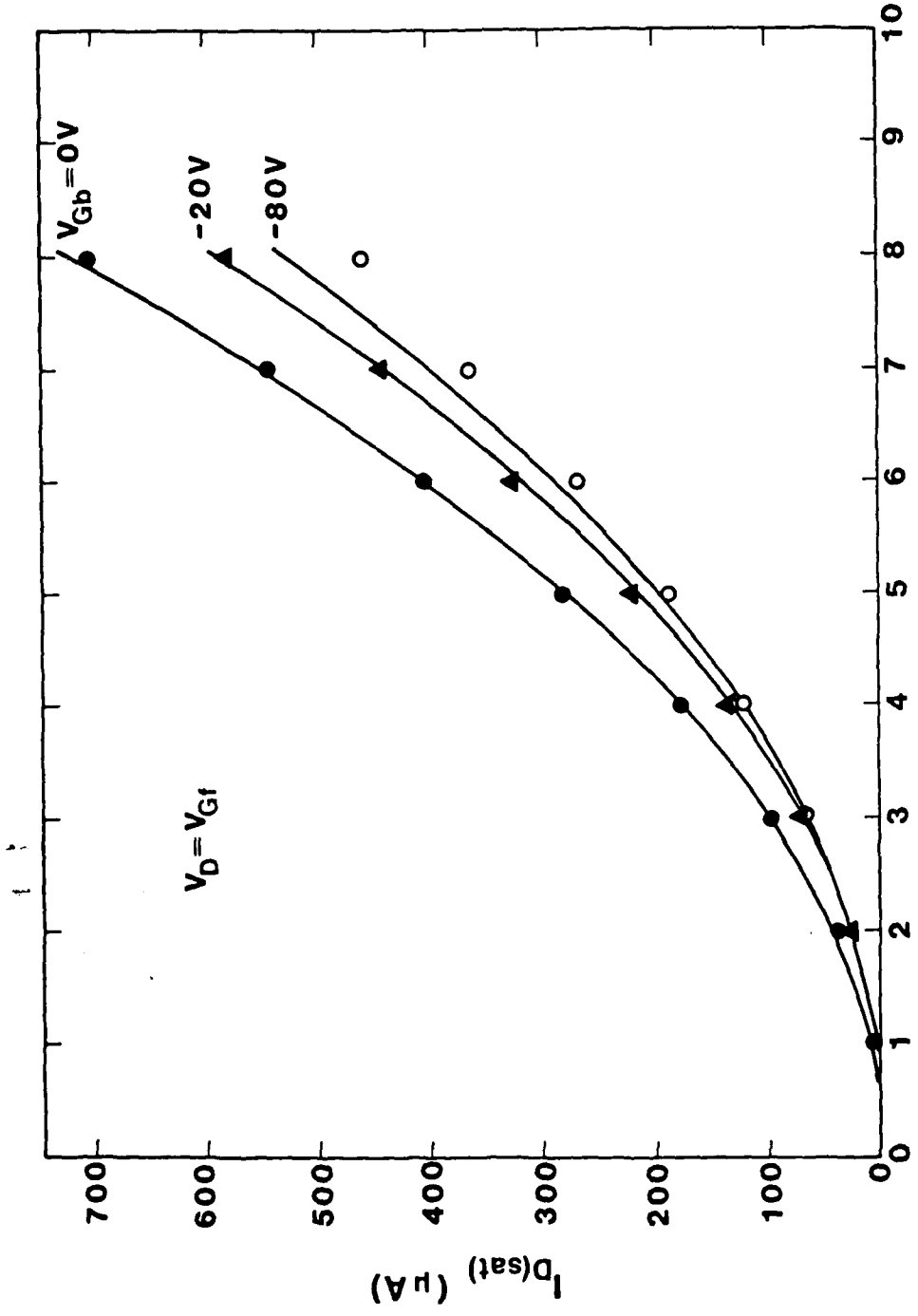
V_{Gb}=0V
-20V
-80V
V_D=V_{Gf}
$I_{D(sat)}$ (μA)
V_{Gf} (V)
0
100
200
300
400
500
600
700
1
2
3
4
5
6
7
8
9
10

Fig. 4

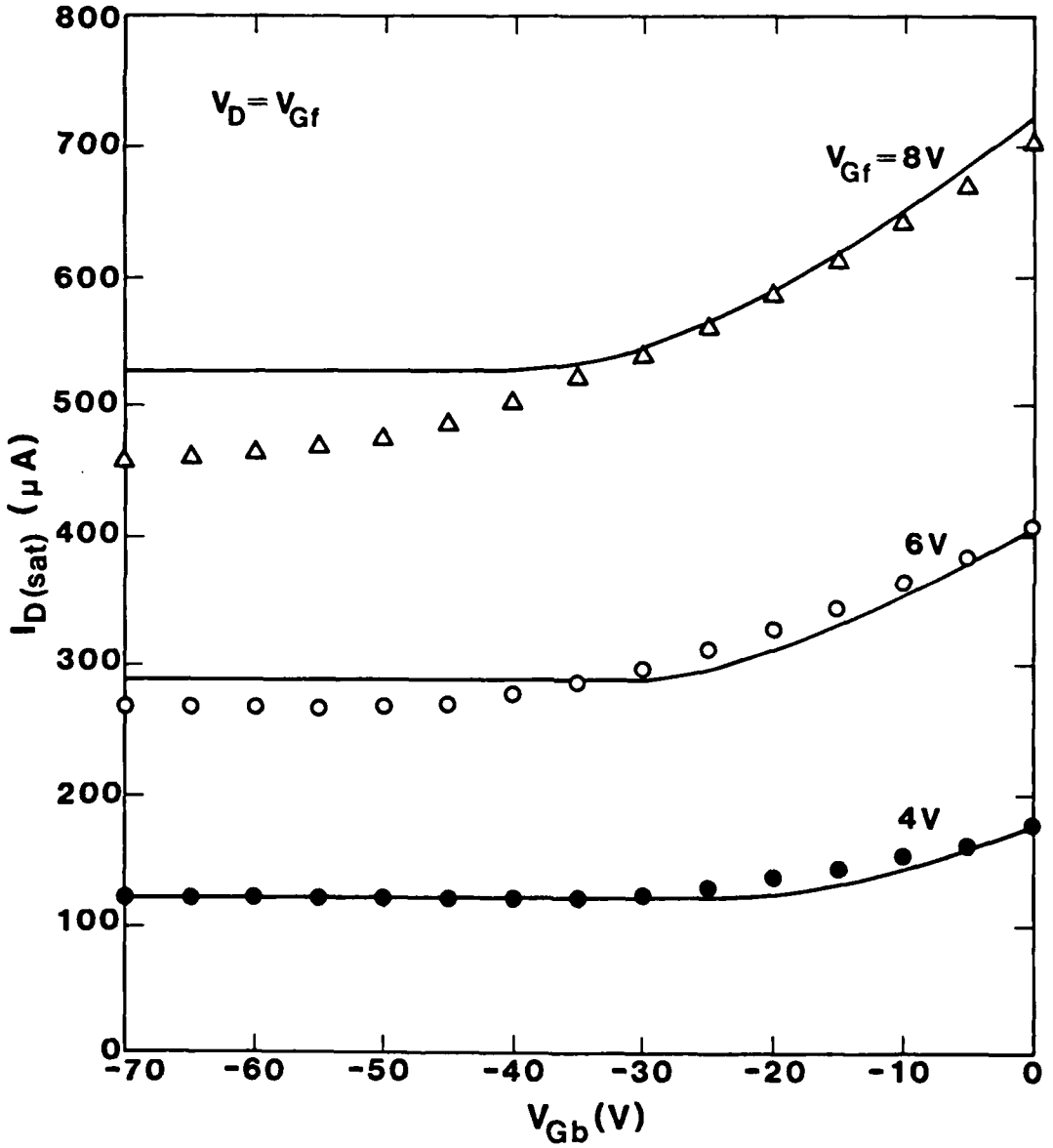
800
700
600
500
400
300
200
100
0
$V_D = V_{Gf}$
$V_{Gf} = 8V$
6V
4V
$I_{D(sat)}$ (μA)
-70
-60
-50
-40
-30
-20
-10
0
V_{Gb}(V)

Fig. 5

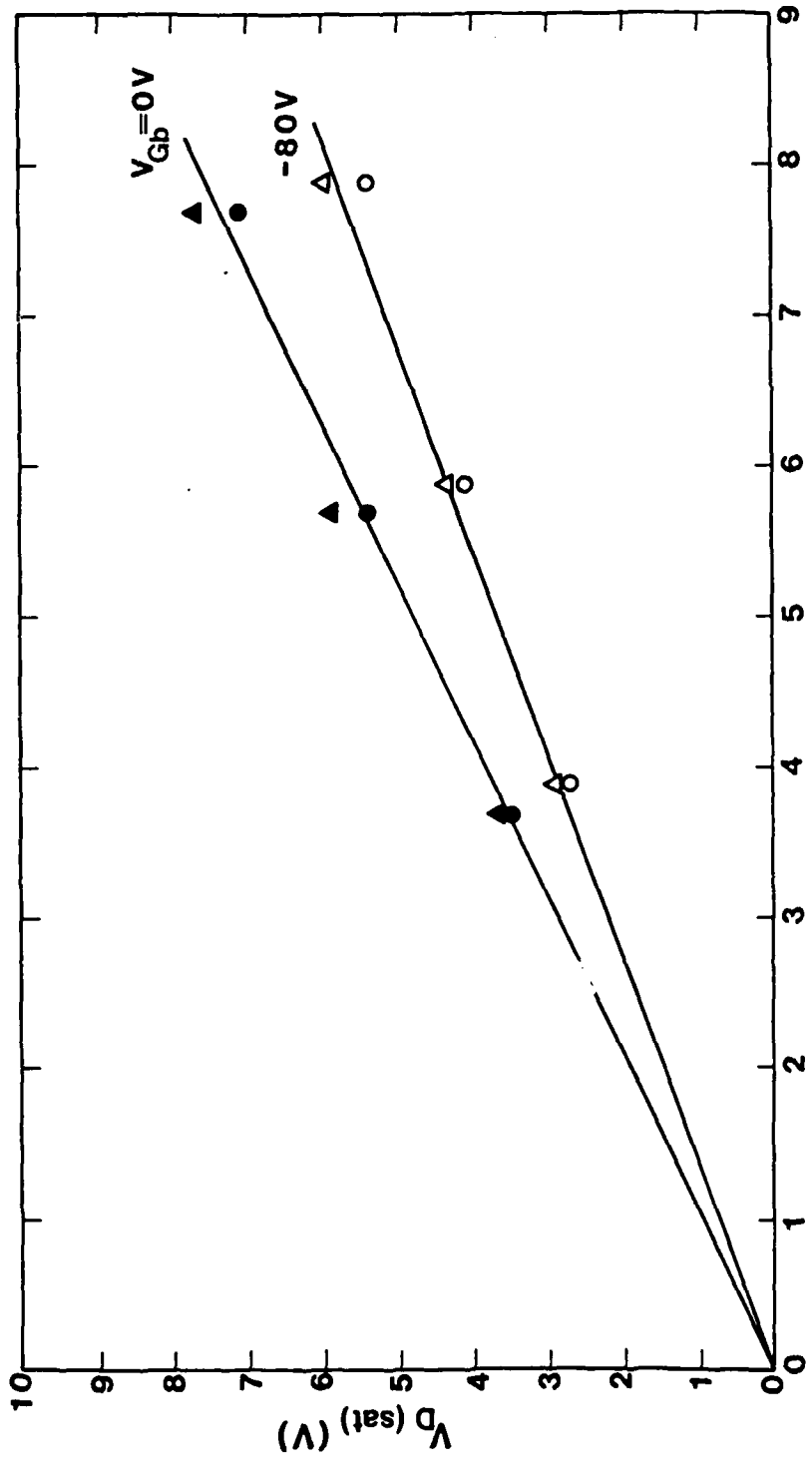

Fig. 6

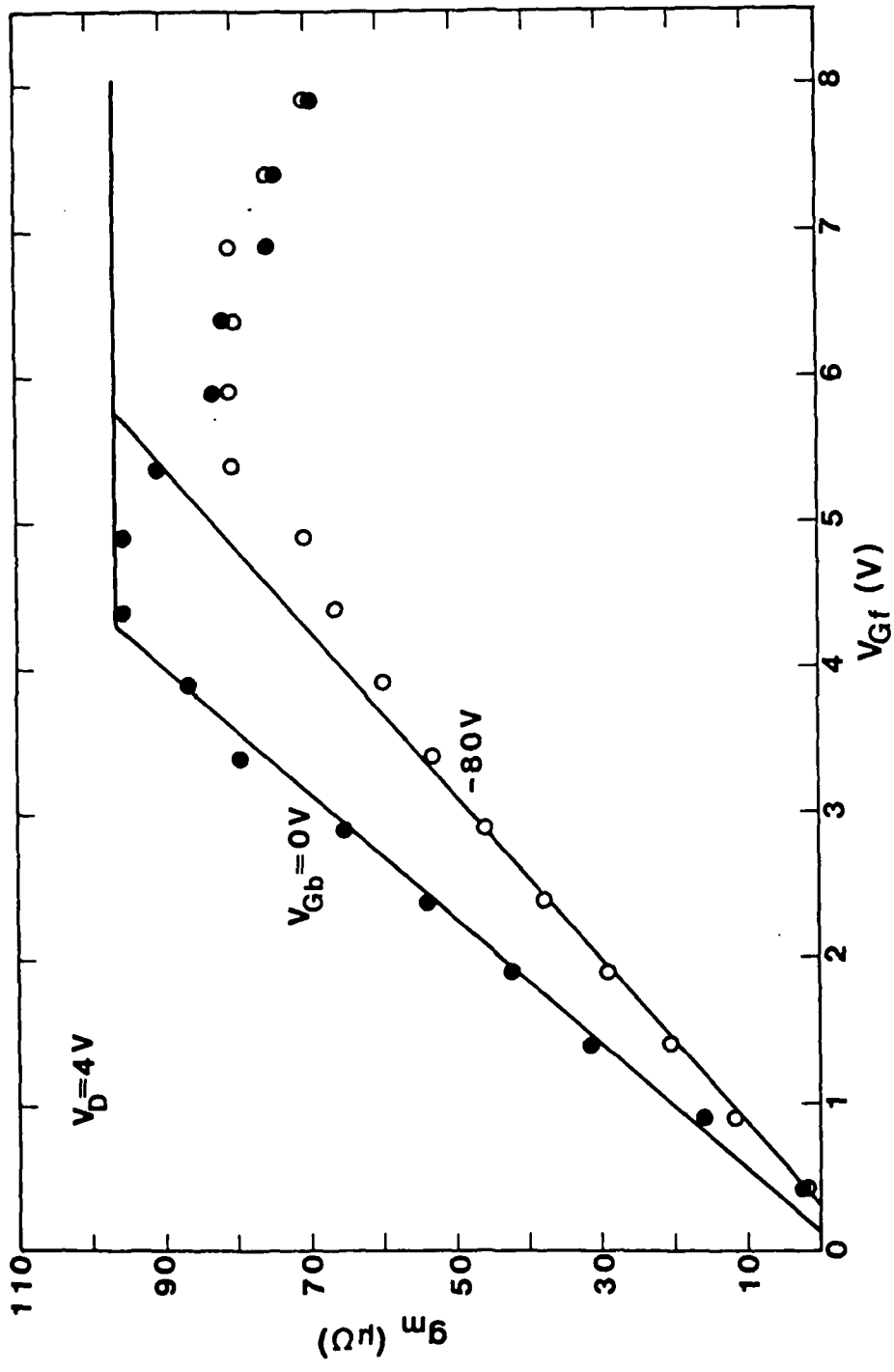

Fig. 7

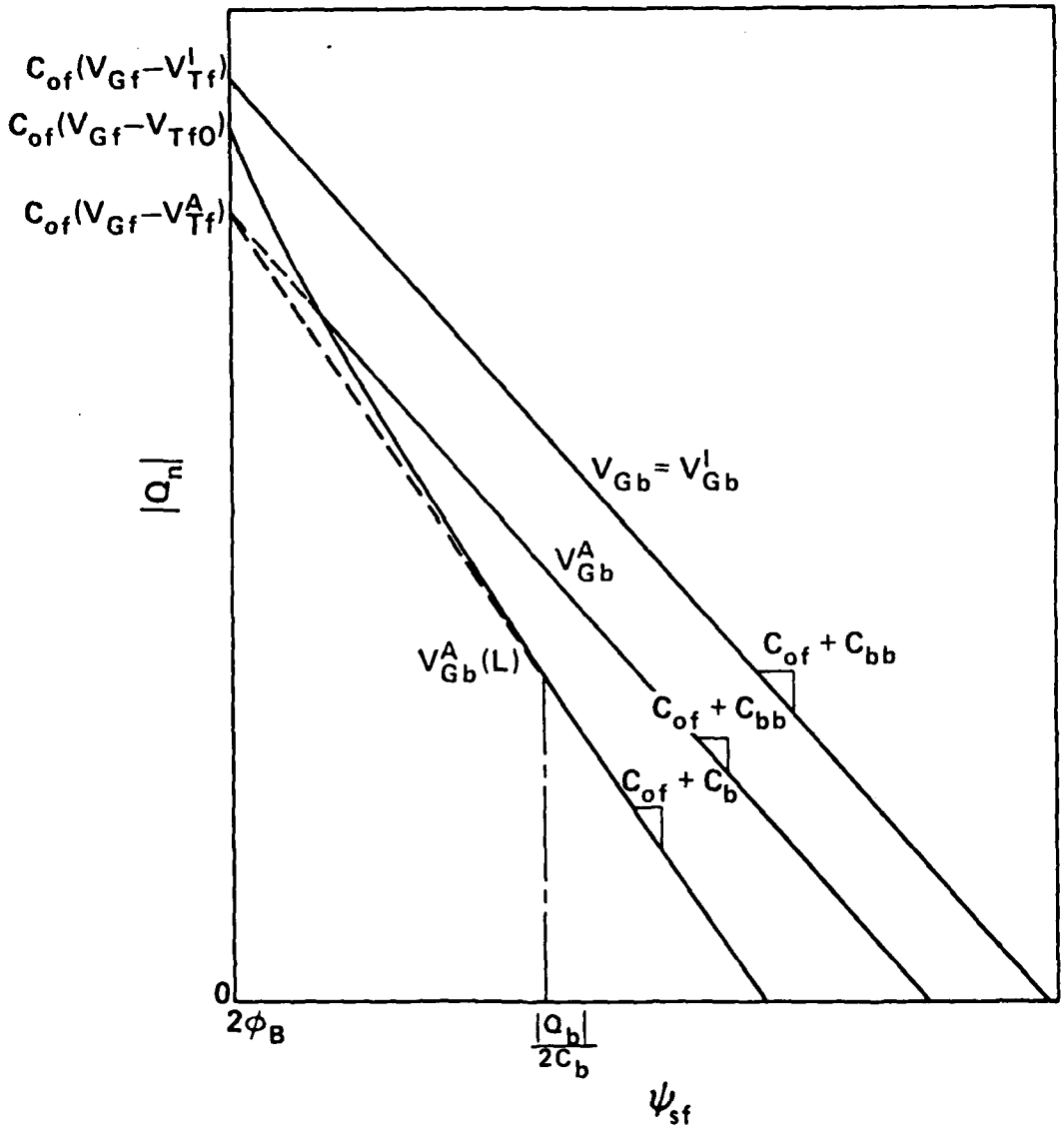
$C_{of}(V_{Gf}-V^{I}_{Tf})$
$C_{of}(V_{Gf}-V_{Tf0})$
$C_{of}(V_{Gf}-V^{A}_{Tf})$
$|Q_n|$
$V_{Gb}=V^{I}_{Gb}$
V^{A}_{Gb}
$V^{A}_{Gb}(L)$
$C_{of}+C_{bb}$
$C_{of}+C_{bb}$
$C_{of}+C_{b}$
0
$2\phi_B$
$\frac{|Q_b|}{2C_b}$
ψ_{sf}

Fig. A.1

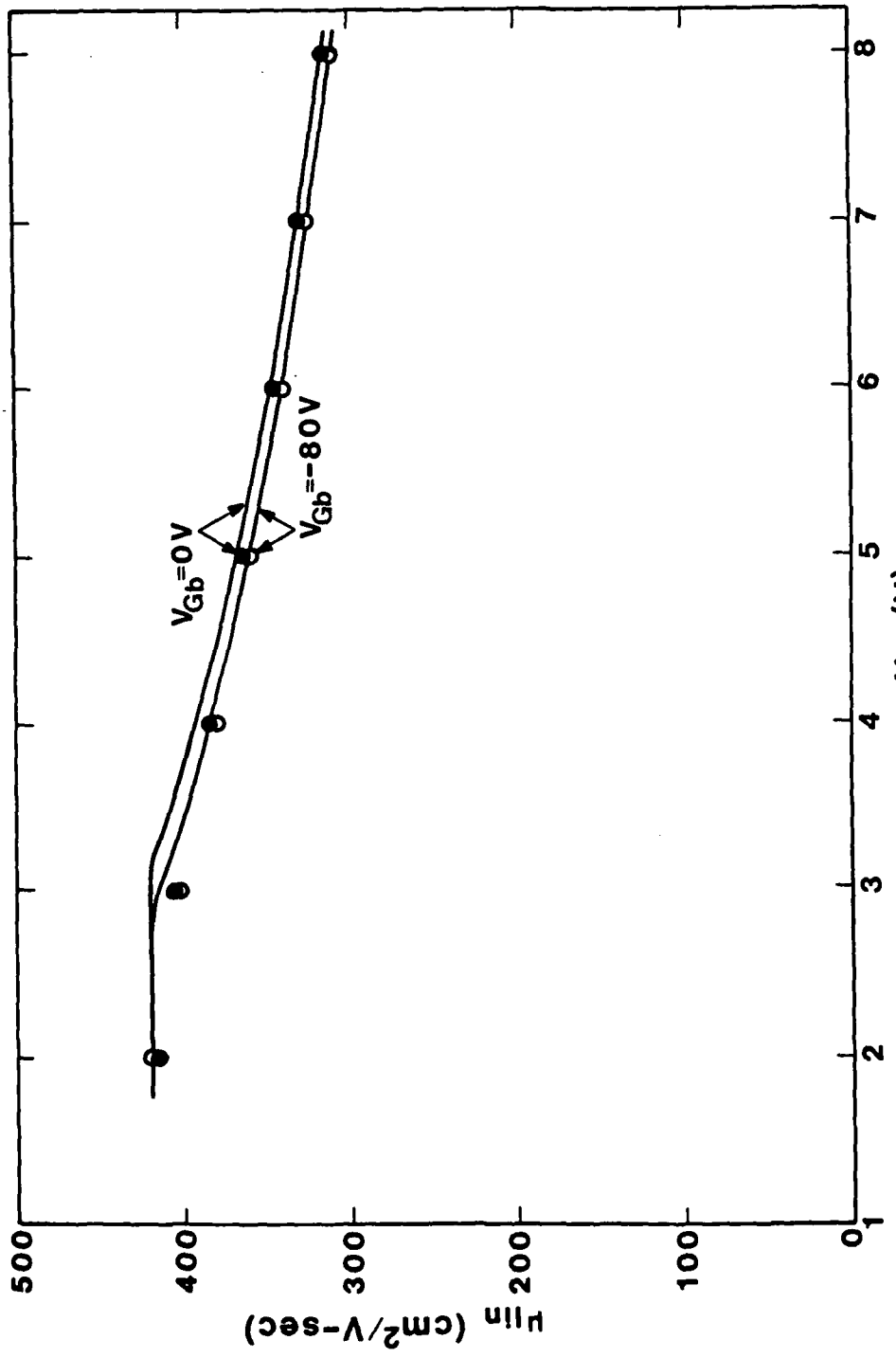
μ_{lin} (cm^2/V-sec)
500
400
300
200
100
0
1
2
3
4
5
6
7
8
V_{Gf} (V)
V_{Gb}=0V
V_{Gb}=-80V

Fig. B.1

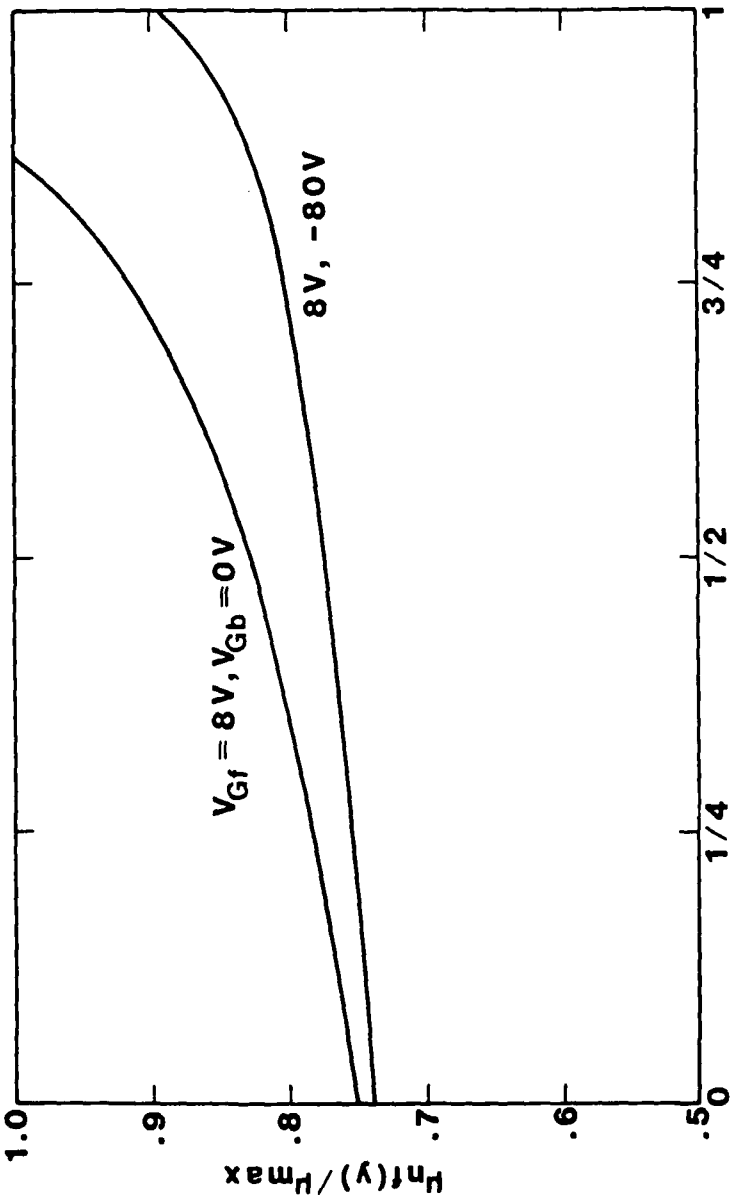

Fig. B.2

E. EFFECTS OF GRAIN BOUNDARIES ON THE CHANNEL CONDUCTANCE OF SOI MOSFETs

I. Introduction

Recent work [1],[2] has demonstrated that zone-melting recrystallization of polycrystalline silicon (polysilicon) films deposited on silicon-dioxide (hereinafter termed SOI) produces dramatic improvement in the quality of the films. Consequently SOI technologies are now being seriously considered, in competition with silicon-on-sapphire (SOS), as means of fabricating monolithic integrated circuits comprising dielectrically isolated devices, which enable higher packing densities, faster speeds, and increased radiation tolerance [3]. Furthermore SOI technologies might facilitate the fabrication of non-planar, "three-dimensional" integrated circuits [4] in which these benefits are exploited.

Most of the previous research and development of SOI has emphasized either the technology, i.e., the recrystallization process by laser [1] or graphite-strip [2] heating, or the recrystallized silicon [5], i.e., its characteristic defects and grain boundaries. Little work [6]-[11] has been done on the characterization or modeling of devices fabricated in SOI films, which is essential if SOI integrated circuits are to be optimally developed.

Such characterization of the SOI MOSFET must include a description of the charge coupling between the front and back gates, which defines the threshold voltage [12], and must account for the influence of grain boundaries on channel conduction, which is the subject of this paper. These boundaries can, depending on the gate bias, be effective scattering centers for carriers in the channel. Hence, as we describe, the grain boundaries can define an effective field-effect carrier mobility that differs from the intragrain mobility and an apparent threshold voltage that reflects an actual "carrier mobility threshold." Previous numerical analyses [6], [11], although based on

simplified models, yield similar results, but without the physical insight provided herein. An earlier analytic model [10], although crude and not generally applicable, does provide some insight with regard to the field effect at a grain boundary.

We derive in this paper a theoretical description of the linear-region (strong-inversion) drain current of the SOI MOSFET, which reveals the physical influence of grain boundaries in the channel, assumed to be perpendicular to the carrier flow. The corresponding channel conductance is described in terms of the (front) gate voltage, the actual threshold voltage [12], the device parameters, and the grain and grain-boundary properties. To stress the influence of the grain boundaries, we neglect small-geometry effects [13].

The model comprises the following physics: (a) the quantum-mechanical description [14] of the carrier distribution in the inversion layer, which implies an average carrier density and its dependence on the gate voltage that can be modeled based on the classical solution [15]; (b) the two-dimensional potential variation near a grain boundary in the channel, which when approximated by coupled one-dimensional solutions of Poisson's equation defines the grain-boundary barrier height resulting from carrier trapping [16]; and (c) the description of the carrier transport through the grain boundary, assumed to be predominantly thermionic emission over the potential barrier [17]. To obtain closed-form expressions for the channel conductance, which give physical insight and facilitate the development of SOI MOSFET models suitable for computer-aided circuit analysis, simplifying assumptions are made and justified.

The resulting channel-conductance model shows an <u>effective</u> turn-on characteristic controlled by the grain boundaries that occurs beyond the strong-inversion threshold. Henceforth the carrier mobility threshold

voltage, which exceeds the actual one, and the effective carrier mobility, which is typically higher than the actual (intragrain) one, are defined. For sufficiently high gate voltage, the grain-boundary potential barrier is low enough that the channel conductance is not significantly influenced by the boundaries. Thus the intragrain mobility, which can be affected by surface scattering [18] controls the conductance at high gate voltages.

To support the analysis and to stress its practicality, we compare model predictions with measured current-voltage-temperature characteristics of laser-recrystallized SOI MOSFETs fabricated at Texas Instruments [19]. The theoretical-experimental agreement is good, and in addition to indicating properties of the grain boundaries in these devices, it exemplifies how the mobility threshold voltage and the effective carrier mobility can be easily misinterpreted as the actual threshold voltage and mobility when conventional MOSFET theory is used as the basis for interpreting electrical measurements of SOI MOSFETs. Such misinterpretations can obscure essential criteria for achieving optimal designs of SOI devices and integrated circuits. For example, our physical analysis reveals that in particular cases grain boundaries can actually benefit the SOI MOSFET performance by producing an unusually high transconductance. This suggests, in contrast to the general belief, that optimal designs may not require elimination of all grain boundaries.

II. Analysis

We assume, based on studies [16], [17] of majority-carrier transport through silicon grain boundaries at room temperature, that thermionic emission of carriers over the grain-boundary potential barrier Ψ_B underlies the predominant influence of the boundary on the channel conductance of SOI

MOSFETs, and that Ψ_B results from carrier trapping at localized grain-boundary states. The trapping and Ψ_B are characterized by a two-dimensional solution of Poisson's equation in the channel. Before we discuss this solution and the corresponding thermionic-emission current, we must consider the intragrain carrier distribution in the channel and its dependence on the gate bias, which define Ψ_B. We refer to the four-terminal n-channel SOI MOSFET illustrated in Fig. 1, and we assume that the grain boundaries in the channel are perpendicular to the electron flow. We restrict our analysis to cases in which the polysilicon film is not completely depleted between the front and back surfaces. The charge-coupling effects [12] that occur otherwise will be incorporated in a future publication.

A. Intragrain Electron Distribution in Channel

Because the inversion layer thickness x_i is very narrow (on the order of the electron de Broglie wavelength), the true electron distribution $n(x)$ in the channel (away from grain boundaries) must be described quantum-mechanically [14]. This description follows from a self-consistent solution of the Schrodinger equation and Poisson's equation. The result differs markedly from the classical solution [15] based on Poisson's equation and Maxwell-Boltzmann statistics: x_i is narrower and $n(x)$ is more uniform [14]. However the inversion-layer areal charge density,

$$-Q_n = q\int_0^{x_i} n(x)dx \tag{1}$$

where $x = 0$ represents the $Si\text{-}SiO_2$ interface, is predicted well by the classical solution.

The analyses suggest a simplification in the description of n(x) and its dependence on the (front) gate voltage V_{Gf}. We define an average electron density $\bar{n}$ over the effective portion of the inversion layer, $0 \leq x \leq x_{i(eff)}$, as revealed by the quantum-mechanical solution, but we use the classical solution, $n^{cl}(x)$, to convey the V_{Gf} dependence. We find that $x_{i(eff)}$ is described well by

$$q \int_0^{x_{i(eff)}} n^{cl}(x)dx \simeq -0.9\ Q_n^{cl} \qquad (2)$$

where Q_n^{cl} ($\simeq Q_n$) is given by (1) with n(x) replaced by $n^{cl}(x)$; that is, about 90% of the inversion-layer charge is contained within a region in which $n \simeq \bar{n}$ and in which virtually all the channel current flows. Then we define $\bar{n}$ by

$$q\bar{n}x_{i(eff)} = -0.9\ Q_n^{cl} \quad . \qquad (3)$$

Numerical evaluations of $x_{i(eff)}$ reveal that it is not strongly dependent on V_{Gf}, that it decreases with increasing film doping density N_A, and that typically it is quite narrow. For example, when $N_A = 10^{16}$ cm^{-3}, $x_{i(eff)} \simeq 120$ Å. Corresponding caluclations of $\bar{n}$ defined by (3) are plotted versus $(V_{Gf} - V_{Tf})$ in Fig. 2 for different values of N_A and for an oxide thickness t_{of} of 600 Å; V_{Tf} is the threshold voltage [12] that corresponds to the onset of strong inversion [$n^{cl}(0) = N_A$]. As implied by (3), Fig. 2 shows that $\bar{n}$ increases with increasing V_{Gf} and with increasing N_A. We find that $x_{i(eff)}$ and $\bar{n}$ as defined by (2) and (3) in terms of the classical solution

[15] are generally consistent with the actual electron distribution given by the quantum-mechanical solution [14].

B. Grain-Boundary Potential Barrier in Channel

For strong-inversion conditions within the grains, electron trapping at localized grain-boundary states produces potential barriers that affect the electron transport along the channel. The barrier formation is similar to that at grain boundaries in bulk polysilicon [16],[20], except in the channel Ψ_B is influenced by V_{Gf} as described by the two-dimensional form of Poisson's equation.

We consider the potential variation near a grain boundary in the channel as shown in Fig. 3. We assume that away from the grain boundary ($y > y_d$) the electric field is vertical (in the x-direction), and $n(x)$ is well approximated by $\bar{n}$ over the effective inversion layer, $0 < x < x_{i(eff)}$, as discussed in the preceding subsection. In this region (I), Poisson's equation simplifies to

$$\left.\frac{\partial^2 \Psi}{\partial x^2}\right|_I \simeq \frac{q}{\varepsilon_s}(\bar{n} + N_A) \tag{4}$$

where Ψ is the electrostatic potential. In the vicinity of the grain boundary ($y < y_d$), a horizontal (y-direction) component of the electric field is produced by the electrons trapped at the grain boundary. We assume that the trapping nearly depletes this region (II) of free electrons; hence

$$\left.\frac{\partial^2 \Psi}{\partial x^2}\right|_{II} + \left.\frac{\partial^2 \Psi}{\partial y^2}\right|_{II} \simeq \frac{q}{\varepsilon_s} N_A \quad . \tag{5}$$

We note that this depletion approximation [16], [17] is valid provided Ψ_B is sufficiently high: high enough in fact, we assume, that the grain boundaries significantly affect the channel conductance. We discuss the validity of this assumption in Subsection II-C.

Assuming that, analogous to the gradual-channel approximation [15], the trapped electrons at the grain boundary typically create only a small perturbation on the x-component of electric field, we can write

$$\left| \left. \frac{\partial^2 \psi}{\partial x^2} \right|_I - \left. \frac{\partial^2 \psi}{\partial x^2} \right|_{II} \right| \ll \left| \left. \frac{\partial^2 \psi}{\partial y^2} \right|_{II} \right| \tag{6}$$

where the partial derivatives are evaluated anywhere in the regions indicated. We justify this assumption by noting that the subsequent solution we obtain is consistent with it when $(V_{Gf} - V_{Tf}) > \Psi_B$, which is usually true for strong-inversion conditions. Hence (6) implies an approximate solution to the two-dimensional problem defined by (4) and (5), which is obtained by coupling two one-dimensional solutions.

The corresponding approximation for Ψ_B derives from the combination of (4)-(6), which yields

$$\left. \frac{\partial^2 \psi}{\partial y^2} \right|_{II} \simeq - \frac{q}{\epsilon_s} \bar{n} \tag{7}$$

with the boundary conditions

$$\psi(x,y = y_d) = \psi_I(x) \tag{8}$$

and

$$\left.\frac{\partial \psi}{\partial y}\right|_{y=y_d} = 0 \quad . \tag{9}$$

In (8) $\psi_I(x)$ is the intragrain (region I) potential variation in the channel, which is given by the one-dimensional solution of Poisson's equation and the Schrodinger equation [14]. We now identify y_d as the grain-boundary depletion-region width, and we note that our analysis applies only when the grains are not completely depleted. The solution to (7)-(9) is

$$\left.\psi(x,y)\right|_{II} \simeq - \frac{q\bar{n}}{2\epsilon_s}(y-y_d)^2 + \psi_I(x) \quad , \tag{10}$$

and hence

$$\psi_B = \psi_I(x) - \left.\psi(x,0)\right|_{II} \simeq \frac{q\bar{n}y_d^2}{2\epsilon_s} \quad . \tag{11}$$

To complete the description of ψ_B, we must express y_d in terms of known parameters. This expression is implied by the conservation of charge in the vicinity of the grain boundary:

$$Q_{GB} = - 2q\bar{n}y_d \quad , \tag{12}$$

which equates the areal density of charge trapped at the grain boundary, Q_{GB}, to the electron charge density removed to form the (two) adjacent depletion regions. In writing (12) we have implicitly assumed that the electrons are

trapped within $x_{i(eff)}$, which is commensurate with our previous assumptions. The trapped charge density depends on the distribution in the energy gap of localized grain-boundary states (acceptor-type since $Q_{GB} < 0$) [17]. It is reasonable to approximate this distribution by a delta function [16], [17], [20], [21] yielding N_{ST} states (traps) per unit area at an energy level E_T. Then

$$Q_{GB} = \frac{-qN_{ST}}{1 + \frac{1}{2}\exp\left\{\frac{[E_T - E_F]_{y=0}}{kT}\right\}} \tag{13}$$

where E_F is the Fermi level and the factor of 1/2 reflects the (spin) degeneracy of the localized states. The position of E_F relative to E_T is defined by ψ_B and the electron density in region I, i.e., $\bar{n}$:

$$[E_T - E_F]_{y=0} \simeq [E_T - E_i] + q\psi_B - \frac{kT}{q}\ln\left(\frac{\bar{n}}{n_i}\right) \tag{14}$$

where E_i is the intrinsic Fermi level (virtually at midgap) and n_i is the intrinsic carrier density in silicon.

Thus (11)-(14) implicitly describe ψ_B in terms of the grain-boundary parameters N_{ST} and $(E_T - E_i)$, and of $\bar{n}$, which depends on V_{Gf} and the MOSFET properties as described in Subsection II-A. Numerical calculations of ψ_B are plotted versus $(V_{Gf} - V_{Tf})$ in Fig. 4 for $N_A = 10^{16}$ cm^{-3}, $t_{of} = 600$ Å, two representative values of N_{ST}, 10^{11} and 10^{12} cm^{-2}, and three positions of E_T in the energy gap. In all cases, for V_{Gf} sufficiently high, ψ_B decreases with increasing V_{Gf}. This can be explained by noting that under these conditions virtually all the grain-boundary states (within $x_{i(eff)}$) are filled, and hence $Q_{GB} \simeq -qN_{ST}$ is independent of V_{Gf}. Therefore since $\bar{n}$ increases with V_{Gf}

(see Fig. 2), y_d concomitantly decreases as described by (12), which implies through (11) that Ψ_B also decreases:

$$\Psi_B \simeq \frac{qN_{ST}^2}{8\varepsilon_s \bar{n}} \quad . \tag{15}$$

However when V_{Gf} is low, Ψ_B is nearly insensitive to V_{Gf}. This is because the grain-boundary states are not completely filled, and hence E_F is near E_T, which virtually fixes Ψ_B as described by (14).

We note in Fig. 4 that for $N_{ST} = 10^{11}$ cm^{-2}, Ψ_B is less than 10 mV when $(V_{Gf} - V_{Tf})$ exceeds about 0.1 V. Thus although our depletion approximation is invalid for these conditions, we surmise that Ψ_B is low enough that the grain boundaries do not significantly affect the channel conductance. However for $N_{ST} = 10^{12}$ cm^{-3}, Ψ_B is high enough, even when $(V_{Gf} - V_{Tf})$ is relatively large, to validate the depletion approximation and to strongly influence the channel conductance as we describe in the next subsection.

C. Channel Conductance

The physical basis for the influence of grain boundaries on the channel conductance is the interaction between electrons flowing from source to drain and the potential barriers at the boundaries. Although quantum-mechanical tunneling of electrons through the barrier may be significant at low temperatures [21] and diffusion of electrons is important when the barrier is low [11], we assume (at room temperature) that thermionic emission of electrons over the barrier Ψ_B is the predominant grain boundary transport mechanism [17]. Then if the drain voltage V_D is low enough (linear region) that the voltage drop across a grain boundary V_{gb} is much smaller than 2kT/q, and if $\Psi_B > kT/q$, the emitted current density is [16]

$$J_{gb} \simeq \frac{qA^*T}{kN_C} \exp\left(\frac{-q\psi_B}{kT}\right) \bar{n}\, V_{gb} \qquad (16)$$

where A^* is the effective Richardson constant [15] for electrons ($\simeq 250$ $A/cm^2/K^2$) and N_C is the effective density of states in the conduction band ($\simeq 2.9 \times 10^{19}$ cm^{-3} at 300° K).

Since the current in the channel is continuous from source to drain, the drain current I_D can be expressed by the integral of (16) over the (effective) cross-sectional area of the channel:

$$I_D = Z\, x_{i(eff)}\, J_{gb} \qquad (17)$$

where Z is the channel width. The combination of (16) and (17) gives I_D as a function of V_{gb}. To obtain I_D as a function of V_D, we simply equate the sum of the voltage drops along the channel to V_D. If we assume that the channel comprises N_g grains of equal length y_g separated by $(N_g - 1)$ identical grain boundaries (see Fig. 3), then

$$V_D = (N_g - 1)V_{gb} + N_g V_g \qquad (18)$$

where V_g is the voltage drop across a grain, which based on conventional MOSFET theory [15] is

$$V_g \simeq \frac{y_g - 2y_d}{Z\mu_{ng}C_{of}(V_{Gf} - V_{Tf})}\, I_D \qquad (19)$$

for strong-inversion conditions in the linear region. In (19) C_{of} is the

(front) gate oxide capacitance and μ_{ng} is the intragrain electron mobility, the dependence of which on V_{Gf} and on device parameters can be given empirically [18].

Combining (16)-(19), we obtain $I_D(V_{Gf},V_D)$ for the SOI MOSFET under strong-inversion conditions ($V_{Gf} > V_{Tf}$) in the linear region ($V_D < (N_g - 1)\ 2kT/q$). If we assume that $y_g >> y_d$, which is valid in typical SOI MOSFETs, then our result simplifies to

$$I_D \simeq \frac{\frac{Z}{L}\mu_{ng}C_{of}(V_{Gf} - V_{Tf})V_D}{1 + \frac{(N_g-1)kN_C\mu_{ng}}{0.9LA^*T}\exp(\frac{q\psi_B}{kT})} \tag{20}$$

where $L = N_g y_g$ is the channel length. In writing (20) we have used (3) and the strong-inversion condition that

$$-Q_n \simeq C_{of}(V_{Gf} - V_{Tf}) \quad , \tag{21}$$

which also underlies (19).

The influence of the grain boundaries on I_D is reflected by the second term in the denominator of (20), which depends of V_{Gf} through $\psi_B[\bar{n}(V_{Gf} - V_{Tf})]$ as described in Subsections II-A (Fig. 2) and II-B (Fig. 4). If the number of grains N_g constituting the channel is one, vis-a-vis, if there are no grain boundaries in the channel, then (20) reduces to the corresponding result of conventional MOSFET theory [15]. Furthermore if ψ_B is sufficiently low, because of low N_{ST} and/or high V_{Gf} (see Fig. 4), then the same result obtains. We note that (20), which because of the model assumptions is

strictly valid only when $\Psi_B > kT/q$, will correctly give the conventional current at high V_{Gf} only if the pre-exponential coefficient is much less than unity. With this insight then, (20) facilitates a self-consistency check for our model assumptions (5) and (16). We find that when the grain boundaries are influential, Ψ_B is generally high enough that the assumptions are valid.

In deriving (20) we have neglected thermionic field emission (tunneling) through Ψ_B, and we have ignored the possible existence of a significant grain-boundary scattering potential barrier [21] through which the electrons must tunnel to traverse the boundary. The tunneling can be predominant at low temperatures, but at room temperature and above it is generally insignificant [17], [21]. We also neglected diffusion of electrons through Ψ_B, which is important only when Ψ_B is low [11]. When Ψ_B is high enough that the grain boundaries significantly affect I_D, the diffusion can be ignored.

To illustrate the grain-boundary effects described by (20), we plot in Figs. 5 and 6 calculations of the linear-region channel conductance ($g \triangleq I_D/V_D$) versus ($V_{Gf} - V_{Tf}$) for several values of N_g and N_{ST}. In Fig. 5 we let N_g vary from one to 200 grains, and we use typical values for the remaining parameters: $N_{ST} = 10^{12}$ cm^{-2} at $E_T = E_i$; $N_A = 10^{16}$ cm^{-3}, $t_{of} = 600$ Å, $Z = L = 40$ μm; we also specify a (front) fixed oxide charge density $Q_{ff} = q(10^{11}$ cm$^{-2})$, which defines μ_{ng} and its dependence on V_{Gf} [18]. We see that as N_g increases, g decreases and the plots become inflected, in general accord with recent measurements of laser-annealed SOI MOSFETs [7]. The plots show <u>apparent</u> threshold voltages that are higher than V_{Tf} and transconductances ($g_m \triangleq \partial I_D/\partial V_{Gf} = V_D \partial g/\partial V_{Gf}$) that imply <u>effective</u> electron mobilities (via the conventional MOSFET theory [15]) which can differ from μ_{ng}. The apparent threshold voltage is actually a "carrier mobility threshold voltage" (V_μ) at which $\bar{n}$ becomes high enough that Ψ_B begins to

diminish with increasing V_{Gf} (see Fig. 4) as described by (15). For $V_{Gf} >> V_{\mu}$, ψ_B is too low to significantly affect I_D; that is, the ψ_B term in (20) is negligible, and g_m is defined by μ_{ng}. Note however in Fig. 5 that the plots for N_g very large become erroneous when $V_{Gf} >> V_{\mu}$ because, as we discussed previously, the pre-exponential coefficient in (20) is not much less than unity. When $V_{Gf} > V_{\mu}$, g_m is typically higher than that corresponding to μ_{ng}. We stress that the high effective electron mobility implied by g_m is defined predominantly by the properties of the grain boundaries. Measured $I_D(V_{Gf},V_D)$ characteristics of SOI MOSFETs can thus be misleading because of the nonlinear effects of grain boundaries as we discuss in the next section.

Additional calculations reveal that V_{μ} depends on N_A and t_{of}; it decreases with increasing N_A and it increases with increasing t_{of}. These dependences reflect, for a given $(V_{Gf} - V_{Tf})$, the dependences of $\bar{n}$, which controls ψ_B, on N_A shown in Fig. 2 and on t_{of} implied by $-Q_n \quad C_{of}$.

The plots of g versus $(V_{Gf} - V_{Tf})$ in Fig. 6 for N_{ST} ranging from 10^{11} to 2×10^{12} cm^{-2} were calculated from (20) for the same device parameter values used to derive the plots in Fig. 5. We let $N_g = 2$ (one grain boundary) to simplify the physical interpretation of the results. The same type of inflection seen in Fig. 5 is noted in Fig. 6 for $N_{ST} > 10^{11}$ cm^{-2}. For the device considered, if N_{ST} is much lower than 10^{12} cm^{-2}, the grain boundary is virtually ineffective; whereas if N_{ST} is higher than 10^{12} cm^{-2}, the grain boundary severely affects (lowers) the channel conductance. Similar calculations have been made for different values of E_T. In this case of the n-channel MOSFET, we find that as E_T approaches the conduction-band edge, ψ_B diminishes and the grain boundary becomes ineffective. As E_T moves toward midgap and below, the grain-boundary effect materializes as indicated in Fig. 6. This dependence on E_T reflects the electron occupancy of the grain-

boundary states, which has been described elsewhere [20]. These results for a monoenergetic trap density could be used to infer corresponding results for different trap distributions in the energy gap.

III. Experimental Results and Discussion

To support the analysis in Section II and to identify critical aspects of it with regard to SOI device and integrated circuit design, we measured linear-region $I_D(V_{Gf},V_D,T)$ characteristics of four-terminal SOI MOSFETs (n-channel) fabricated at Texas Instruments [19]. The polysilicon film is 0.5 μm thick and was laser-recrystallized after being deposited via LPCVD on a 1-μm-thick layer of silicon-dioxide, which had been thermally grown on a silicon substrate. The film was doped by ion implantation of boron that yielded $N_A \approx 2 \times 10^{16}$ cm^{-3} near the front surface and $N_A \sim 10^{15}$ cm^{-3} at the back surface [19]. The front gate is n^+ polysilicon and $C_{of} \approx 5.8 \times 10^{-8}$ F/cm^2 ($t_{of} \approx 600$ A). Large devices ($Z = L = 40$ μm) were selected to preclude small-geometry effects [13].

To avoid complications due to the charge coupling between the front and back gates [12], a high negative voltage (- 40 V) was applied to the back gate to ensure accumulation at the back Si-SiO_2 interface and to fix V_{Tf}. The $I_D(V_{Gf})$ dependence was measured with $V_D = 50$ mV at three temperatures (24° C, 70° C, and 100° C). The corresponding channel conductance characteristics $g(V_{Gf},T)$ of a particular device, which typify the characteristics of identically processed devices, are plotted in Fig. 7. The basic shape of these plots is the same as that of the theoretical curves in Figs. 5 and 6, which implies qualitative support for our analysis. (The theoretical and experimental curves should not be compared quantitatively because the parameter values used in the calculations are not necessarily the actual values.)

The support for (20) is demonstrated by examination of the measured $g(V_{Gf},T)$ characteristics within particular ranges of V_{Gf}. For high V_{Gf} ($>> V_\mu$), g is defined by the numerator of (20); the grain-boundary effect is negligible. Thus as in the case of conventional MOSFETs [15], the carrier mobility (μ_{ng}) follows from the slope of $g(V_{Gf})$, i.e., from g_m, and the threshold voltage (V_{Tf}) is given by the linear extrapolation of the characteristic to the V_{Gf} axis. From Fig. 7 we thereby get $V_{Tf} \simeq 0.10$ V and $\mu_{ng} \simeq 380$ $cm^2/V/sec$ at 24° C. This value of μ_{ng} is low, and hence implies excessive scattering at the polysilicon surface, due possibly to high Q_{ff} [18]. (Quantitative theoretical-experimental studies, which will be reported in a future publication, indicate $Q_{ff} \simeq q(3 \times 10^{11}\ cm^{-2})$.) The low μ_{ng} does not reflect decreased transconductance due to a high surface electric field [18], which we observed only at values of V_{Gf} higher than those in Fig. 7. These interpretations are supported by the temperature dependence of g in the high-V_{Gf} region. We see in Fig. 7 a <u>weak</u> dependence of V_{Tf} on T and a <u>negative</u> temperature coefficient for μ_{ng}, which are consistent with the g(T) characteristics of conventional silicon MOSFETs [7], [22].

It is obvious now in Fig. 7 that V_{Tf} is considerably less than the electron mobility threshold voltage V_μ. Thus there is a significant range of V_{Gf} ($V_{Tf} < V_{Gf} < V_\mu$) in which the grain boundaries suppress I_D. In this case the ψ_B term in (20) is much greater than unity, i.e., $V_{gb} >> V_g$, and hence $g \propto \exp(-q\psi_B/kT)$. As long as $V_{Gf} < V_\mu$, ψ_B is high and does not vary significantly with V_{Gf} (see Fig. 4). The <u>positive</u> temperature coefficient for g thus predicted is consistent with the measured conductance plotted in Fig. 7 in this region.

When $V_{Gf} > V_\mu$, ψ_B decreases with increasing V_{Gf} (see Fig. 4), and hence g increases. To analytically describe this increase and to estimate V_μ, we use

the approximate $\psi_B(\bar{n})$ dependence in (15) and the strong-inversion relationship (21). The combination of (15), (20), and (21) yields a $g(V_{Gf})$ characteristic that exhibits an inflection point where g_m is maximum. The theoretical and experimental plots in Figs. 5-7 imply that this maximum is broad. Therefore we approximate the actual characteristic by the linear function

$$g \simeq \frac{Z}{L}\mu_{n(eff)}C_{of}(V_{Gf} - V_{\mu}) \quad . \tag{22}$$

which is tangent to the actual $g(V_{Gf})$ curve at the inflection point. This function then analytically defines V_{μ} and the effective field-effect electron mobility $\mu_{n(eff)}$ due to the grain boundaries.

The value of V_{Gf} at the inflection point is defined by equating to zero the second derivative of (20) with respect to V_{Gf}, using (3), (15), and (21). We find that at this value, the denominator of (20) is two. Thus (22) describes the tangent to $g(V_{Gf})$ at the point where the ψ_B term in the denominator of (20) is unity. This tangent yields (for $N_g > 1$)

$$V_{\mu} \simeq V_{Tf} + \frac{\dfrac{q^3 x_{i(eff)} N_{ST}^2}{8kT\epsilon_s C_{of}}}{2 + \ln\left[\dfrac{0.9A^*TL}{kN_C\mu_{ng}(N_g-1)}\right]} \tag{23}$$

and

$$\mu_{n(eff)} \simeq \frac{\mu_{ng}}{4}\left\{2 + \ln\left[\frac{0.9A^*TL}{kN_C\mu_{ng}(N_g-1)}\right]\right\} \quad . \tag{24}$$

We note that the weak dependence of $x_{i(eff)}$ on V_{Gf} has been ignored in the derivation of (23) and (24). Thus V_μ in (23) is evaluated by assuming a representative value for $x_{i(eff)}$, which depends on N_A as discussed in Subsection II-A. We stress that (23) and (24), which are based on analytic simplifications of our more general analysis described in Section II, are merely estimates of V_μ and $\mu_{n(eff)}$. However they are useful in describing the functional dependences of g and g_m on device parameters and temperature, and hence will facilitate SOI MOSFET design and computer-aided SOI circuit analysis.

We see from (24) that the effective electron mobility is typically higher than μ_{ng} depending on L, N_g, and T. The measured $g(V_{Gf})$ characteristics plotted in Fig. 7 when interpreted using (22) yield $\mu_{n(eff)} \approx 530$ $cm^2/V/sec$ at 24° C, which is considerably higher than μ_{ng} The negative temperature coefficient for $\mu_{n(eff)}$ implied by the data in Fig. 7 is consistent with (24), which shows that the temperature dependence is defined primarily by that of μ_{ng}. Using the measured value of $\mu_{n(eff)}$ mentioned above and (24), we find that $N_g \approx 50$ grains. Since $L = 40$ μm, this implies a crude estimate of about 1 μm for the average grain size (y_g), which is not unreasonable for the laser-recrystallized polysilicon film [19]. We note finally that the dependence of $\mu_{n(eff)}$ on L suggested by (24) is consistent with measurements [8] of (effective) electron mobility in laser-recrystallized MOSFETs having different channel lengths. For a given y_g ($=L/N_g$ with $N_g > 1$), $\mu_{n(eff)}$ increases as L is reduced from many times y_g toward y_g.

The electron mobility threshold voltage as described in (23) is strongly dependent on N_{ST} and T, as well as on N_A through V_{Tf} [12] and $x_{i(eff)}$. The inverse dependence of $x_{i(eff)}$ on N_A described in Subsection II-A implies that the difference between V_μ and V_{Tf} decreases as N_A increases. The predicted

direct dependence on N_{ST} is consistent with observed decreases in the (apparent) threshold voltage of polysilicon MOSFETs resulting from hydrogenation [23], which is known to reduce N_{ST}. The inverse dependence of V_{μ} on T suggested by (23) is corroborated by the measured $g(V_{Gf},T)$ data plotted in Fig. 7. At 24° C, the measurements when interpreted using (22) imply $V_{\mu} \approx 0.55$ V, whereas $V_{Tf} \approx 0.10$ V. The difference between V_{μ} and V_{Tf}, based on (23), indicates that $N_{ST} \approx 1 \times 10^{12}$ cm^{-2} (where the traps are near midgap).

We conclude this section by stressing two significant conclusions drawn from it. First, because (22), which is of the same form as the linear-region conductance expression for the conventional MOSFET [15], empirically describes well an appreciable region of the $g(V_{Gf})$ characteristic for the SOI MOSFET, V_{μ} and $\mu_{n(eff)}$ can be easily misinterpreted as V_{Tf} and μ_{ng}. Such misinterpretations, which evidently have been made in some previous work, can lead to misconceptions regarding SOI and can impede the development of optimal SOI devices and integrated circuits. Second, even though grain boundaries are effective in defining the channel conductance of SOI MOSFETs, the transconductance can be higher than that of the conventional counterpart; the grain boundaries are actually beneficial in this regard. Thus perhaps optimal designs of SOI MOSFETs may not require complete elimination of grain boundaries.

IV. Summary

A physical model that describes the effects of grain boundaries on channel conductance in SOI MOSFETs has been developed and supported experimentally. These effects originate when electrons (n-channel MOSFET) are trapped at localized grain-boundary states, thereby creating potential

barriers that influence the flow of electrons from source to drain. The electron trapping depends on the degree of inversion in the channel and hence on the gate voltage. For sufficiently high V_{Gf}, Ψ_B is low enough that the grain boundaries are inconsequential with regard to g and g_m. However for lower V_{Gf}, the grain boundaries can predominantly control g and g_m and can define an effective turn-on (linear-region) characteristic that occurs well beyond the strong-inversion threshold as illustrated in Figs. 5 and 6.

The effective turn-on characteristic, described generally by (20) and approximated by (22), is actually a reflection of the "carrier mobility turn-on", which is controlled by the grain boundaries. It defines the electron mobility threshold voltage V_μ, which exceeds V_{Tf}, and the effective electron mobility $\mu_{n(eff)}$, which is typically higher than the actual (intragrain) mobility μ_{ng}. Evidently measurements of V_μ and $\mu_{n(eff)}$ have been previously misinterpreted as determinations of V_{Tf} and μ_{ng}. Subsequent erroneous conclusions regarding SOI can inhibit the development of optimal SOI devices and integrated circuits, which, based on our analysis, possibly need not nor should not be completely void of grain boundaries.

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AD-A136 975 THEORETICAL-EXPERIMENTAL ANALYSIS OF THE EFFECTS OF GRAIN BOUNDARIES ON T..(U) FLORIDA UNIV GAINESVILLE DEPT OF ELECTRICAL ENGINEERING J G FOSSUM NOV 83 2/2

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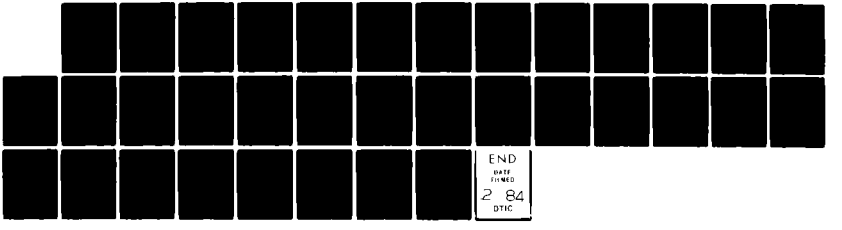

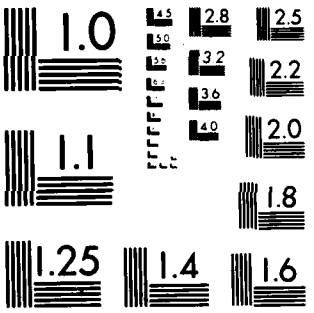

FIGURE CAPTIONS

Figure 1. Cross-section of four-terminal SOI MOSFET (n-channel). The terminal voltages are referenced to the source voltage (V_S=0).

Figure 2. Calculated average electron density in channel versus (front) gate voltage for several film doping densities.

Figure 3. Cross-section of effective inversion layer showing typical grain and grain boundaries, which are assumed to be perpendicular to the electron flow.

Figure 4. Calculated grain boundary potential barrier versus (front) gate voltage for two representative grain-boundary trap densities and three energy levels. We note that the low values of Ψ_B calculated for $N_{ST} = 10^{11}$ cm^{-2} are probably inaccurate because of the invalidity of the depletion approximation (5). Nevertheless the curve is useful because it indicates when Ψ_B is low enough that the grain-boundary effect on channel conduction is insignificant.

Figure 5. Calculated linear-region channel conductance versus (front) gate voltage for several numbers of grains constituting the channel. The broken portions of the curves for N_g=20, 100, and 200 are inaccurate because of the invalidity of (20) as discussed in Subsection II-C. The N_g = 1 curve is inaccurate for V_{Gf} near V_{Tf} because of the invalidity of the strong-inversion relationship (21).

Figure 6. Calculated linear-region channel conductance versus (front) gate voltage for several grain-boundary trap densities.

Figure 7. Measured linear-region channel conductance versus (front) gate voltage of n-channel SOI MOSFET in laser-recrystallized polysilicon [19] at three temperatures. The threshold voltage is fixed by the back-gate voltage [12], which was set at -40V to ensure accumulation at the back Si-SiO_2 interface.

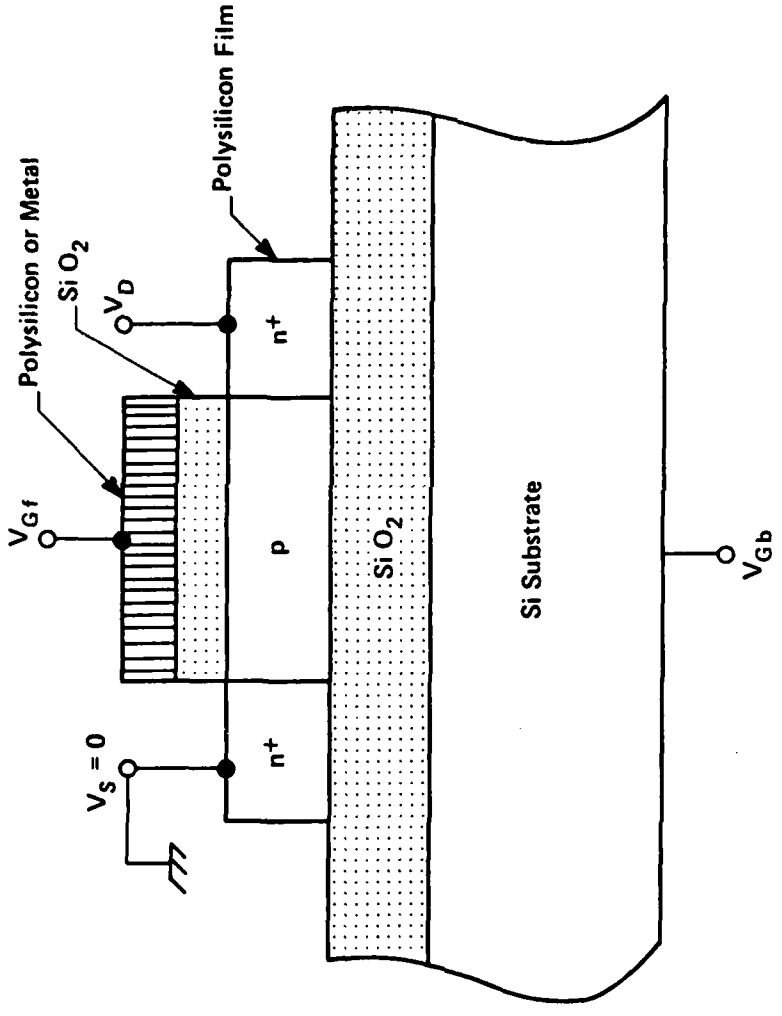
Polysilicon Film
Polysilicon or Metal
Si O2
VD
n+
VGf
p
Si O2
Si Substrate
VGb
VS = 0
n+

Fig. 1

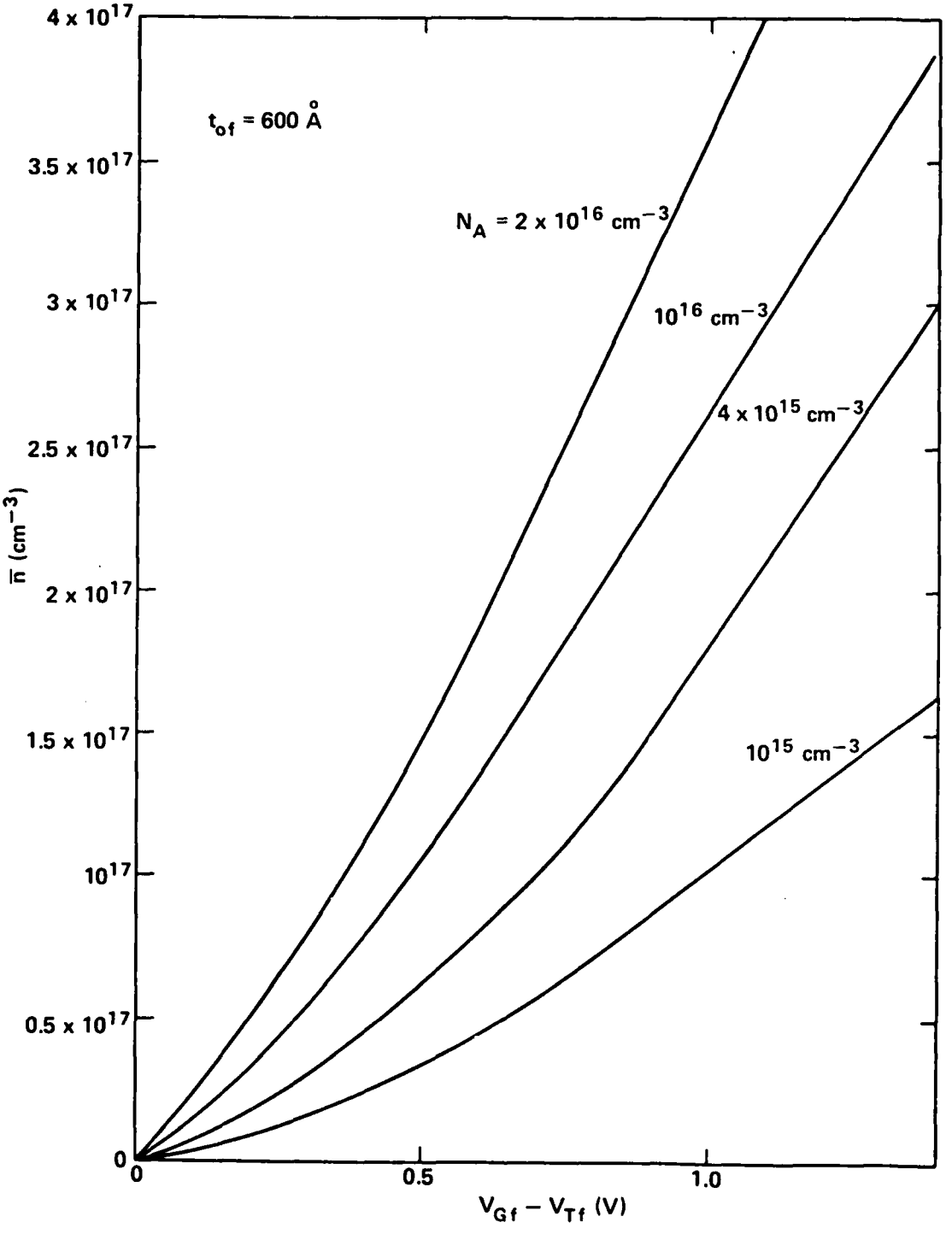
4 x 10^17
3.5 x 10^17
3 x 10^17
2.5 x 10^17
2 x 10^17
1.5 x 10^17
10^17
0.5 x 10^17
0
0
0.5
1.0
n̄ (cm^-3)
V_Gf − V_Tf (V)
t_of = 600 Å
N_A = 2 x 10^16 cm^-3
10^16 cm^-3
4 x 10^15 cm^-3
10^15 cm^-3

Fig. 2

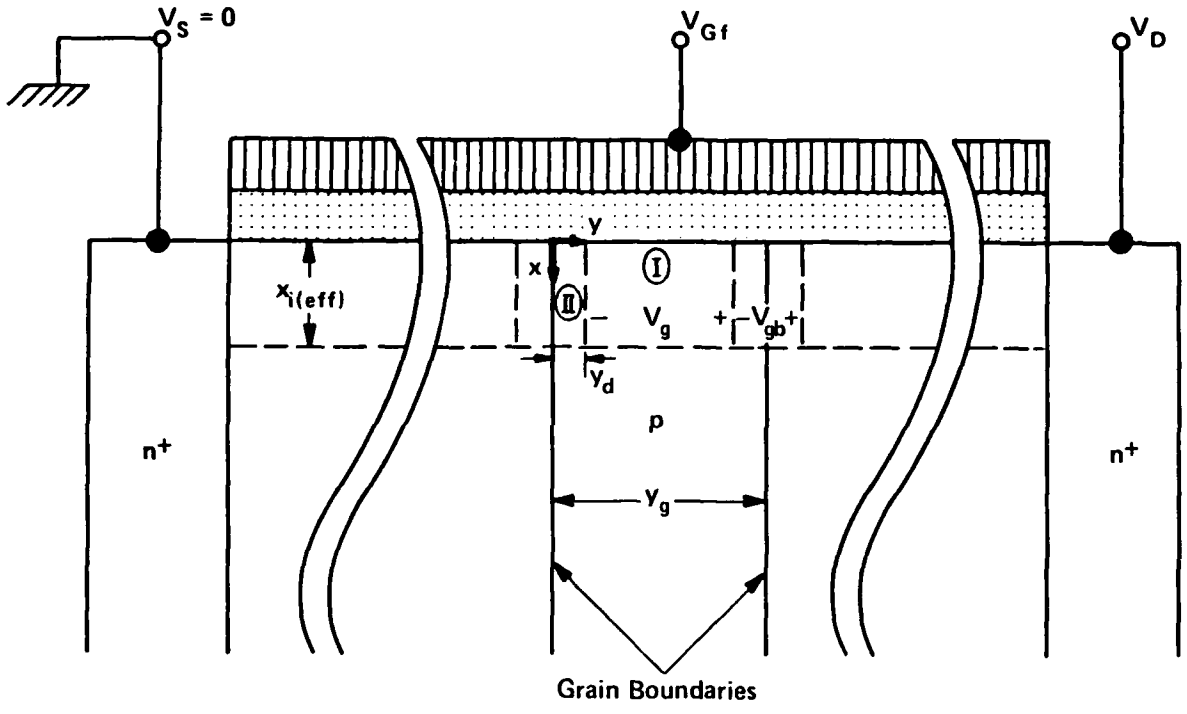

Fig. 3

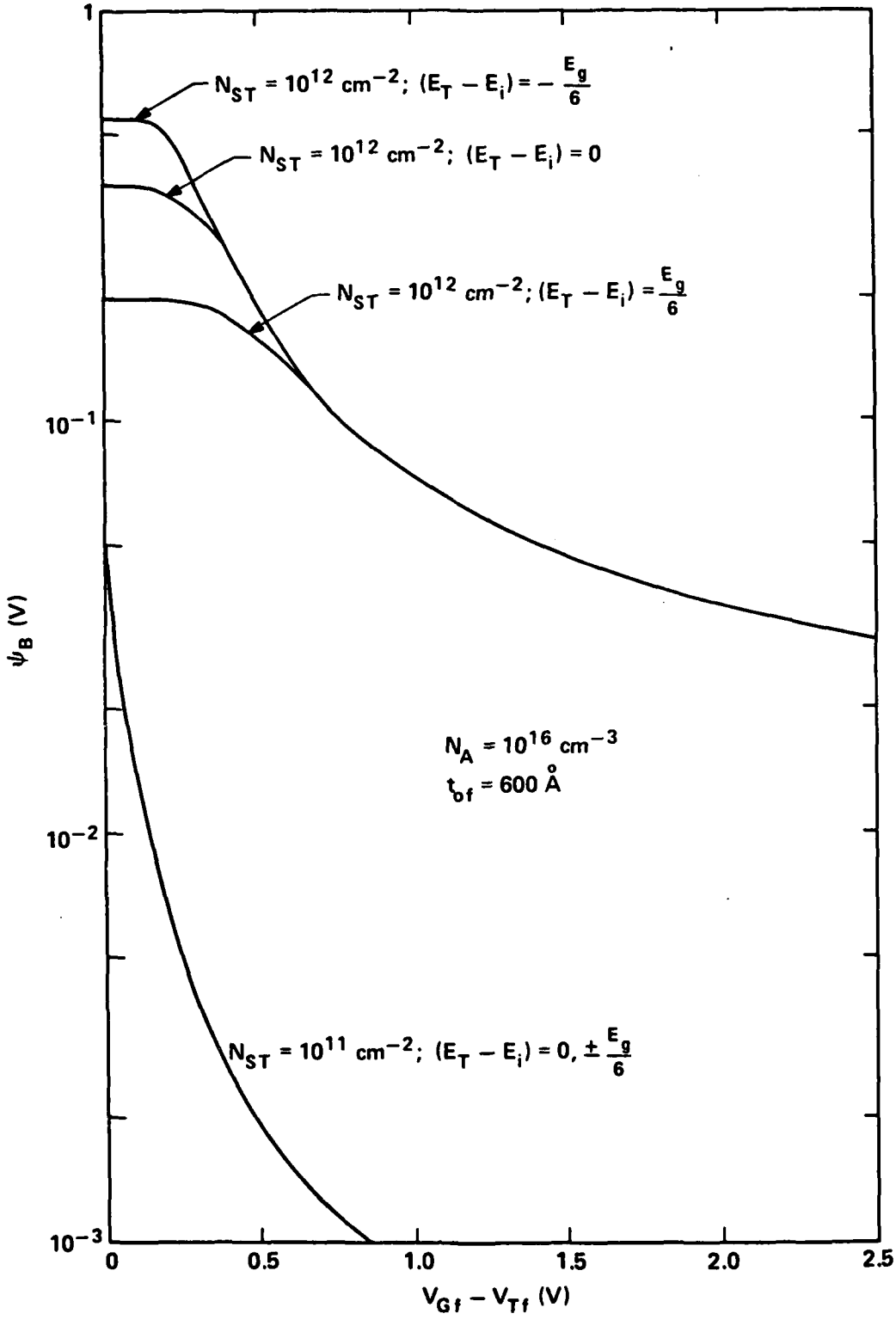
1
10^{-1}
10^{-2}
10^{-3}
ψ_B (V)
$N_{ST} = 10^{12}$ cm^{-2}; $(E_T - E_i) = -\frac{E_g}{6}$
$N_{ST} = 10^{12}$ cm^{-2}; $(E_T - E_i) = 0$
$N_{ST} = 10^{12}$ cm^{-2}; $(E_T - E_i) = \frac{E_g}{6}$
$N_A = 10^{16}$ cm^{-3}
$t_{of} = 600$ Å
$N_{ST} = 10^{11}$ cm^{-2}; $(E_T - E_i) = 0, \pm \frac{E_g}{6}$
0
0.5
1.0
1.5
2.0
2.5
$V_{Gf} - V_{Tf}$ (V)

Fig. 4

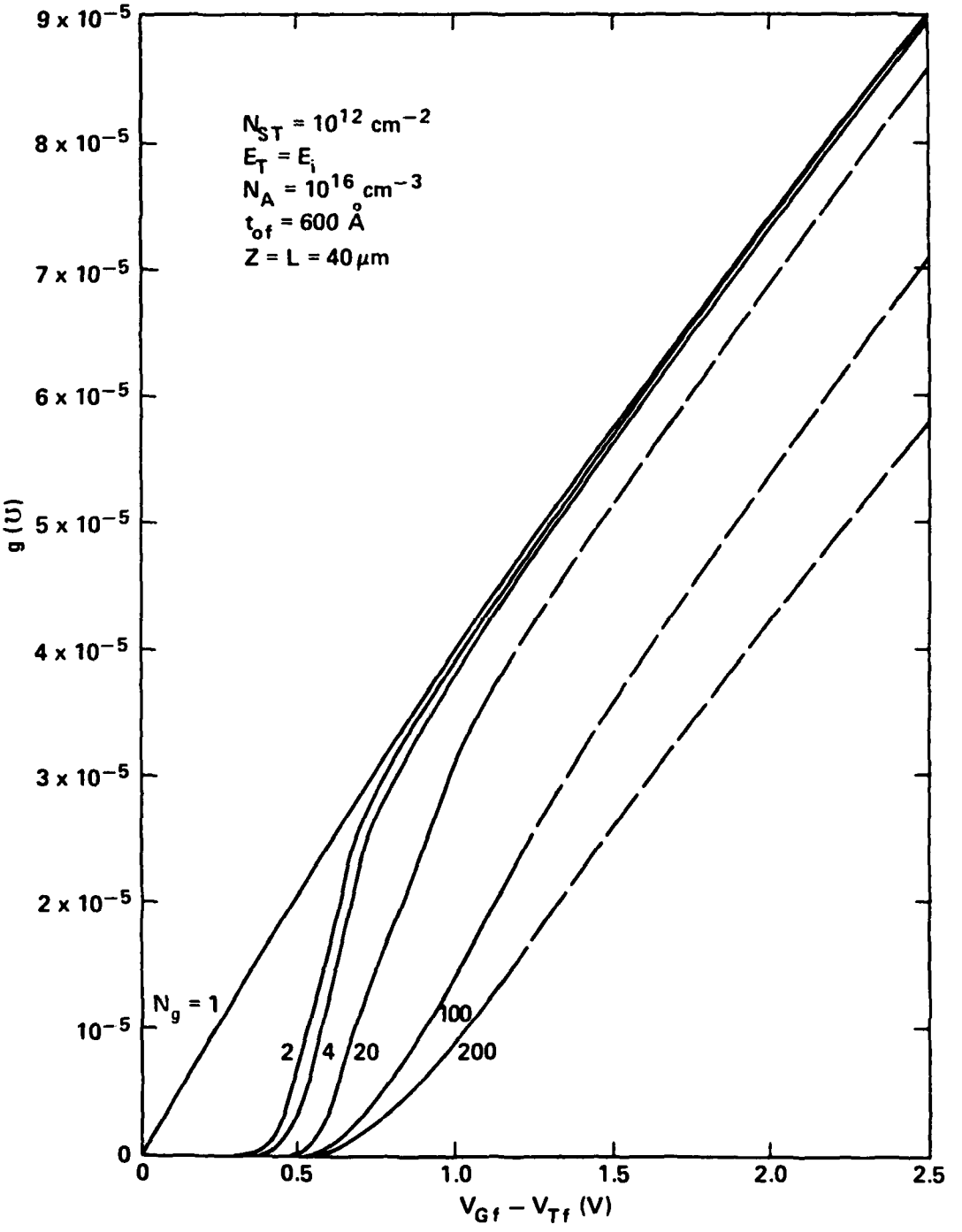
$N_{ST} = 10^{12}$ cm^{-2}
$E_T = E_i$
$N_A = 10^{16}$ cm^{-3}
t_{of} = 600 Å
Z = L = 40 μm
N_g = 1
2
4
20
100
200
g (U)
$V_{Gf} - V_{Tf}$ (V)
9 x 10^{-5}
8 x 10^{-5}
7 x 10^{-5}
6 x 10^{-5}
5 x 10^{-5}
4 x 10^{-5}
3 x 10^{-5}
2 x 10^{-5}
10^{-5}
0
0.5
1.0
1.5
2.0
2.5

Fig. 5

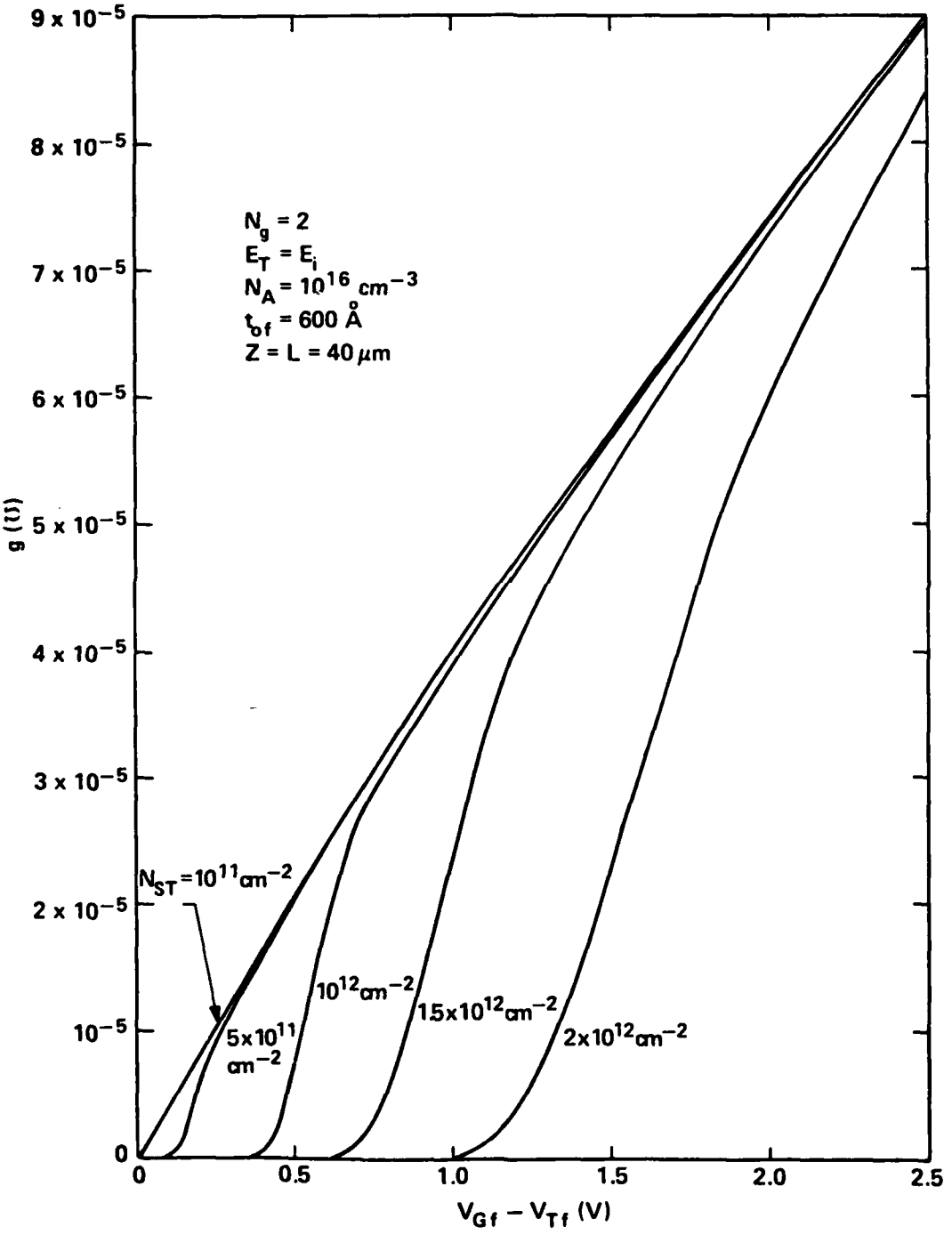
9 x 10⁻⁵
8 x 10⁻⁵
7 x 10⁻⁵
6 x 10⁻⁵
5 x 10⁻⁵
4 x 10⁻⁵
3 x 10⁻⁵
2 x 10⁻⁵
10⁻⁵
0
g (Ω)
N_g = 2
E_T = E_i
N_A = 10^16 cm⁻³
t_of = 600 Å
Z = L = 40 μm
N_ST=10^11cm⁻²
5x10^11 cm⁻²
10^12cm⁻²
1.5x10^12cm⁻²
2x10^12cm⁻²
0
0.5
1.0
1.5
2.0
2.5
V_Gf − V_Tf (V)

Fig. 6

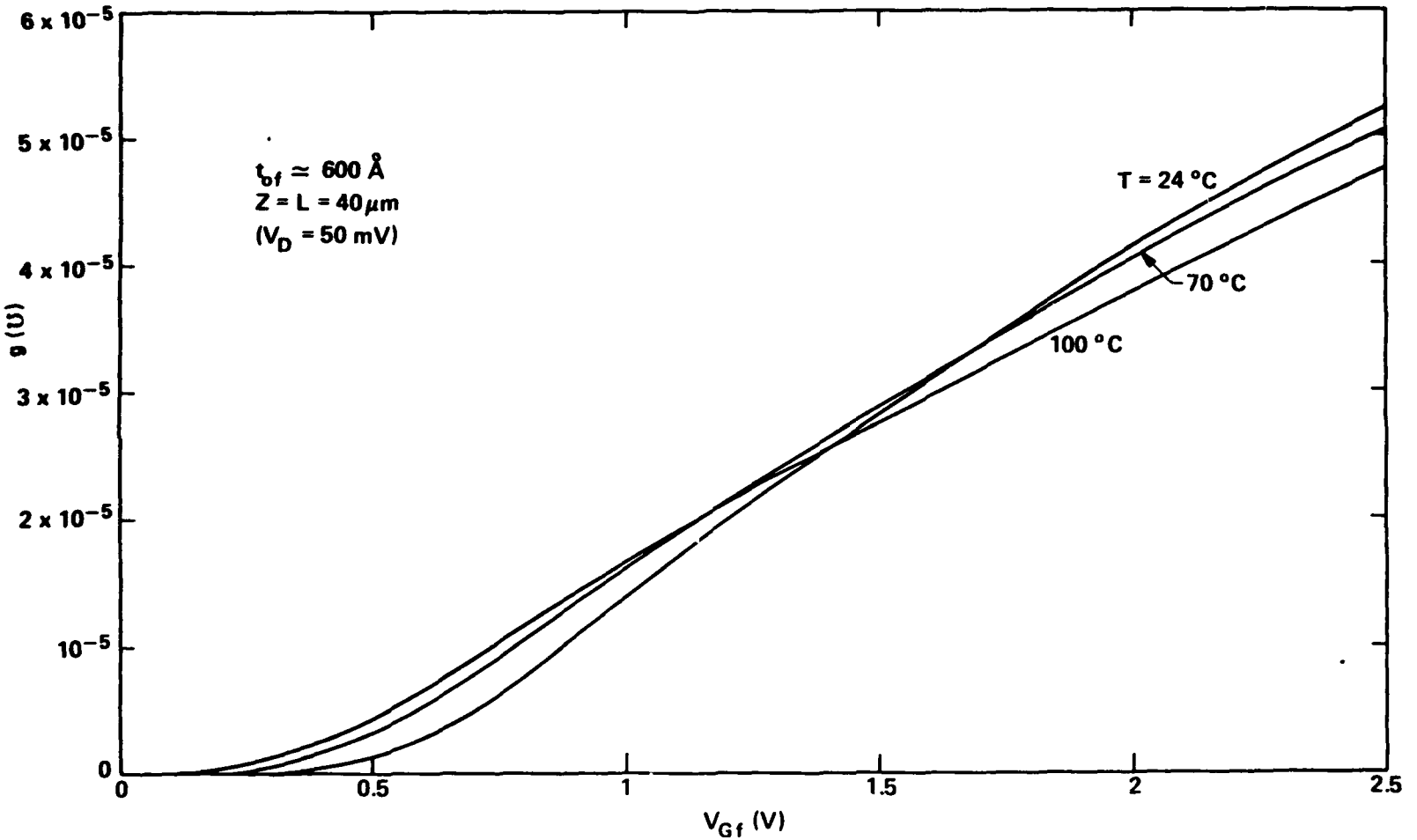
6 x 10⁻⁵
5 x 10⁻⁵
4 x 10⁻⁵
3 x 10⁻⁵
2 x 10⁻⁵
10⁻⁵
0
g (U)
t_of ≃ 600 Å
Z = L = 40 μm
(V_D = 50 mV)
T = 24 °C
70 °C
100 °C
0
0.5
1
1.5
2
2.5
V_Gf (V)

Fig. 7

F. MODERATE INVERSION IN SOI MOSFETs WITH GRAIN BOUNDARIES

The potential improvement of integrated circuits (VLSI) afforded by dielectric isolation has prompted the development of new silicon-on-insulator (SOI) technologies that yield useful thin films of (recrystallized) polysilicon deposited on silicon dioxide [1]. SOI MOSFETs fabricated in these films have two important dissimilarities with respect to their bulk-silicon counterparts: the charge coupling between the front (conventional) and back (silicon substrate) gates [2], [3], and the presence of grain boundaries in the channel region [4], [5]. As a consequence of the grain boundaries there is an effective turn-on characteristic [5] of the linear-region channel conductance that occurs beyond the strong-inversion threshold and henceforth defines the "carrier mobility threshold voltage" (V_μ) and the "effective field-effect carrier mobility" in the channel, which typically is higher than the actual (intragrain) mobility.

We recently presented a physical model [5] for the effects of grain boundaries on the linear-region (front) channel conductance ($g = I_D/V_D$) of SOI MOSFETs. The model assumptions are: (a) the carrier transport through a grain boundary is predominantly by thermionic emission over the potential barrier ψ_B; (b) the grain boundaries are perpendicular to the carrier flow in the channel; (c) the channel comprises N_g grains of equal length separated by (N_g-1) identical grain boundaries; and (d) the strong-inversion approximations are applicable, e.g., $-Q_n \simeq C_{of}(V_{Gf}-V_{Tf})$ where Q_n is the (intragrain) inversion-layer (n-channel) charge density, V_{Gf} is the front-gate voltage, C_{of} is the front-gate oxide capacitance, and V_{Tf} is the front-gate threshold voltage [3], which is defined as the value of V_{Gf} that causes the front band bending ψ_{sf} to be twice the Fermi potential [$\phi_B = (kT/q)\ln(N_A/n_i)$] in the silicon film.

In this paper we extend this model [5] to account for lower-V_{Gf}, or "sub-mobility-threshold" ($V_{Gf} < V_{\mu}$) regions of operation. We find that, irrespective of the inversion level, the drain current I_D varies nearly exponentially with V_{Gf}, and that the gate-voltage swing S needed to reduce I_D by one order-of-magnitude is strongly dependent on the properties of the grain boundaries. These results are supported experimentally, and, as we show, theoretical-experimental comparisons can be used to estimate key parameters of the grain boundaries and of the Si-SiO_2 interface. This moderate-inversion model extension supplements and corroborates well our previous strong-inversion analysis of the grain-boundary effects in SOI MOSFETs.

Following our analysis in [5] but removing the strong-inversion assumption, we obtain

$$g(V_{Gf}) = \frac{I_D}{V_D} = \frac{\frac{Z}{L}\mu_{ng}\left|Q_n(V_{Gf})\right|}{1 + \frac{(N_g-1)\mu_{ng}kN_c}{0.9A^*TL}\exp\left[\frac{q\psi_B(V_{Gf})}{kT}\right]} \qquad (1)$$

where μ_{ng} is the <u>intragrain</u> electron mobility in the channel; the other symbols in (1) have their usual meaning and/or are defined in [5]. If we neglect the charge-coupling effects [2], [3], then for all inversion conditions [6],

$$Q_n = Q_s - Q_b \qquad (2)$$

where

$$Q_s = -Q_r\left[\frac{q\psi_{sf}}{kT} - 1 + \left(\frac{n_i}{N_A}\right)^2 \exp\left(\frac{q\psi_{sf}}{kT}\right)\right]^{1/2} \qquad (3)$$

is the (areal) charge density in the silicon and

$$Q_b = -Q_r\left[\frac{q\psi_{sf}}{kT} - 1\right]^{1/2} \qquad (4)$$

is the depletion-region charge density. In (3) and (4), $Q_r = [2kT\varepsilon_s N_A]^{1/2}$ where N_A is the (uniform) doping density in the silicon film. The relationship between ψ_{sf} and V_{Gf} is defined by

$$V_{Gf} - V_{FB}^f = \psi_{sf} - \frac{Q_s}{C_{of}} + \frac{qN_{sf}}{C_{of}}\psi_{sf}$$

where V_{FB}^f is the front-gate flatband voltage, which includes a contribution from fast surface states at the Si-SiO_2 interface, the density N_{sf} ($cm^{-2}eV^{-1}$) of which is assumed to be uniform in the energy gap. The $Q_n(V_{Gf})$ dependence in (1) is now defined by (2)-(5).

The grain-boundary potential barrier $\psi_B(V_{Gf})$ in (1) is characterized as described in [5] with an effective inversion-layer thickness of 80Å implied by N_A. The barrier results from electron trapping at localized grain-boundary states in the channel and hence depends on the intragrain inversion level and on the grain-boundary trap density N_{ST} and the trap (assumed to be monoenergetic) energy level E_T. We described in [5] how ψ_B decreases as V_{Gf} and the electron density in the channel increase when the grain-boundary traps are completely filled. For low V_{Gf}, provided the grains are not completely depleted, ψ_B is nearly constant and maximum when the traps are predominantly empty, i.e., when the Fermi level is near E_T.

To support the model and to estimate critical parameters of it, we measured at various temperatures $g(V_{Gf})$ characteristics of four-terminal SOI

MOSFETs (n-channel) fabricated at Texas Instruments, Inc. [7]. The polysilicon film is 0.5-μm-thick and was laser-recrystallized after being deposited via LPCVD on a 1-μm-thick layer of silicon dioxide, which had been thermally grown on a silicon substrate. The film was doped by ion implantation of boron that yielded, based on SUPREM-II calculations [7], $N_A \approx 2 \times 10^{16}$ cm^{-3} near the front surface and $N_A \sim 10^{15}$ cm^{-3} at the back surface. The front gate is n^+ polysilicon and the gate oxide is 600-A-thick ($C_{of} \approx 5.8 \times 10^{-8}$ F/cm^2). Large devices (Z = L = 40 μm) were selected to avoid small-geometry effects.

To eliminate complications due to the charge coupling between the front and the back gates [3], a high negative voltage (-40 V) was applied to the back gate to ensure accumulation at the back Si-SiO_2 interface and to fix V_{Tf}. The $g(V_{Gf})$ characteristics were measured with a low drain voltage of 50 mV. We previously reported [5] good agreement between the experimental results and the theoretical predictions for high V_{Gf} ($> V_\mu$), i.e., strong inversion. We also estimated, for a typical device, that the threshold voltage defined by the linear extrapolation of the measured $g(V_{Gf})$ when the grain boundaries are insignificant ($V_{Gf} >> V_\mu$) is $V'_{Tf} \approx 0.1$ V, and that the electron mobility defined by the slope of the extrapolation is $\mu_{ng} \approx 380$ cm^2/V-sec. From $g(V_{Gf})$ that is affected by the grain boundaries ($V_{Gf} \gtrsim V_\mu$), we measured, based on our model, $V_\mu \approx 0.5$ V, $N_{ST} \approx 10^{12}$ cm^{-2} (for E_T assumed to be at midgap), and $N_g \approx 50$. Note that typically $V'_{Tf} \approx V_{Tf} + nkT/q$ with $n \approx 3$-5 depending on N_A and C_{of} [6]. Thus our strong-inversion measurements [5] imply $V_{Tf} \approx 0$, which is consistent with calculations based on (2)-(5).

We plot in Fig. 1 the $g(V_{Gf})$ characteristic of a typical device measured at room temperature. Note especially the lower-V_{Gf} ($< V_\mu$) data, which show a

nearly exponential dependence on V_{Gf}. For comparison we also show in Fig. 1 theoretical $g(V_{Gf})$ curves that were numerically derived from (1) using the parameter values given above and $N_A = 2 \times 10^{16}$ cm^{-3}. We varied E_T and let $N_{sf} = 0$, which from $V_{Tf} \approx 0$ and (5) implies $V_{FB}^f \approx -1.9$ V. The calculated $g(V_{Gf})$ characteristics also are nearly exponential for low V_{Gf}, even though the inversion level is <u>not</u> weak. (In weak inversion, the conductance of single-crystal MOSFETs is exponentially dependent on the gate voltage because Q_n is [6],[8].) This dependence is due primarily to the $\exp(q\psi_B/kT)$ term in (1) as implied by the strong dependence of S (i.e., the inverse slope) on E_T. As E_T moves from midgap ($\approx E_i$) toward the conduction band, S increases; when $(E_T-E_i) \approx 0.2$ eV, the measured S is modeled well. Thus the energy level of the grain-boundary traps significantly affects the channel conductance below the electron mobility threshold ($V_{Gf} < V_\mu$).

We illustrate in Fig. 2 the effect of N_{sf} on the $g(V_{Gf})$ characteristic. The theoretical curves plotted were derived using the same parameter values for Fig. 1 and $(E_T-E_i) = 0.2$ eV. For each value of N_{sf}, V_{FB}^f was calculated from (5) using $V_{Tf} \approx 0$. Increasing N_{sf} tends to suppress the conductance for intermediate values ($\sim V_\mu$) of V_{Gf}, but does not significantly affect S. By comparing the calculated curves with the measured data, we crudely estimate that $N_{sf} \sim 10^{11}$ cm^{-2}eV^{-1}.

Measurements at different temperatures (T = 24°C, 70°C, and 100°C) indicate that, for intermediate V_{Gf}, both $g(V_{Gf})$ and S increase with increasing T. As T increases from 24°C to 100°C, S increases from 0.25 V to 0.34 V and, at $V_{Gf} = V_\mu \approx 0.5$ V, g increases from 1.3×10^{-6} ℧ to 4.5×10^{-6} ℧. These changes are consistent with (1) in which, for relatively low V_{Gf}, the $\exp(q\psi_B/kT)$ term defines the predominant dependence on temperature.

To conclude, we have extended our previous model [5] that describes the effects of the grain boundaries on the linear-region (strong-inversion) channel conductance of SOI MOSFETs to account for moderate-inversion conditions that obtain in the "sub-mobility threshold" region ($V_{Gf} < V_{\mu}$) of operation. We have shown good agreement between theory and experiment, which corroborated the model and enabled estimations of key device and material parameters. In the "sub-mobility threshold" region, the drain current, which is controlled by the grain boundaries, varies nearly exponentially with gate voltage and the gate-voltage swing needed to reduce the drain current by one order-of-magnitude depends strongly on the properties of the grain boundaries, especially the grain-boundary trap level, and on the properties of the Si-SiO_2 interface, i.e., the fast surface-state density.

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5. J. G. Fossum and A. Ortiz-Conde, "Effects of Grain Boundaries on the Channel Conductance of SOI MOSFETs", IEEE Trans. Electron Devices, vol. ED-30, Aug. 1983; also in J. G. Fossum, A. Ortiz, H.-K. Lim, and H.-W. Lam, "Effects of Grain Boundaries on Channel Conduction in Thin-Film SOI MOSFETs", SPIE Technical Symposium, Los Angeles, California (SPIE Proc., vol. 385), Jan. 1983.

6. Y. Tsividis, "Moderate Inversion in MOS Devices", Solid-State Electron., vol. 25, pp. 1099-1104, 1982.

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FIGURE CAPTIONS

Fig. 1. Measured (points) and calculated (curves) linear-region (V_D = 50 mV) conductance versus front-gate voltage of an n-channel SOI MOSFET in laser-recrystallized polysilicon at room temperature. The measurements were made with the back gate biased at -40 V. The calculations were done for different grain-boundary trap energy levels as indicated and with the fast surface-state density at the front Si-SiO_2 interface equal to zero. Note that $V_{Tf} \approx 0$ V.

Fig. 2. Measured (points) and calculated (curves) linear-region (V_D = 50 mV) conductance versus front-gate voltage of an n-channel SOI MOSFET in laser-recrystallized polysilicon at room temperature. The measurements were made wtih the back gate biased at -40 V. The calculations were done for different fast surface-state densities at the front Si-SiO_2 interface as indicated and with the grain-boundary trap energy level at 0.2 eV above midgap.

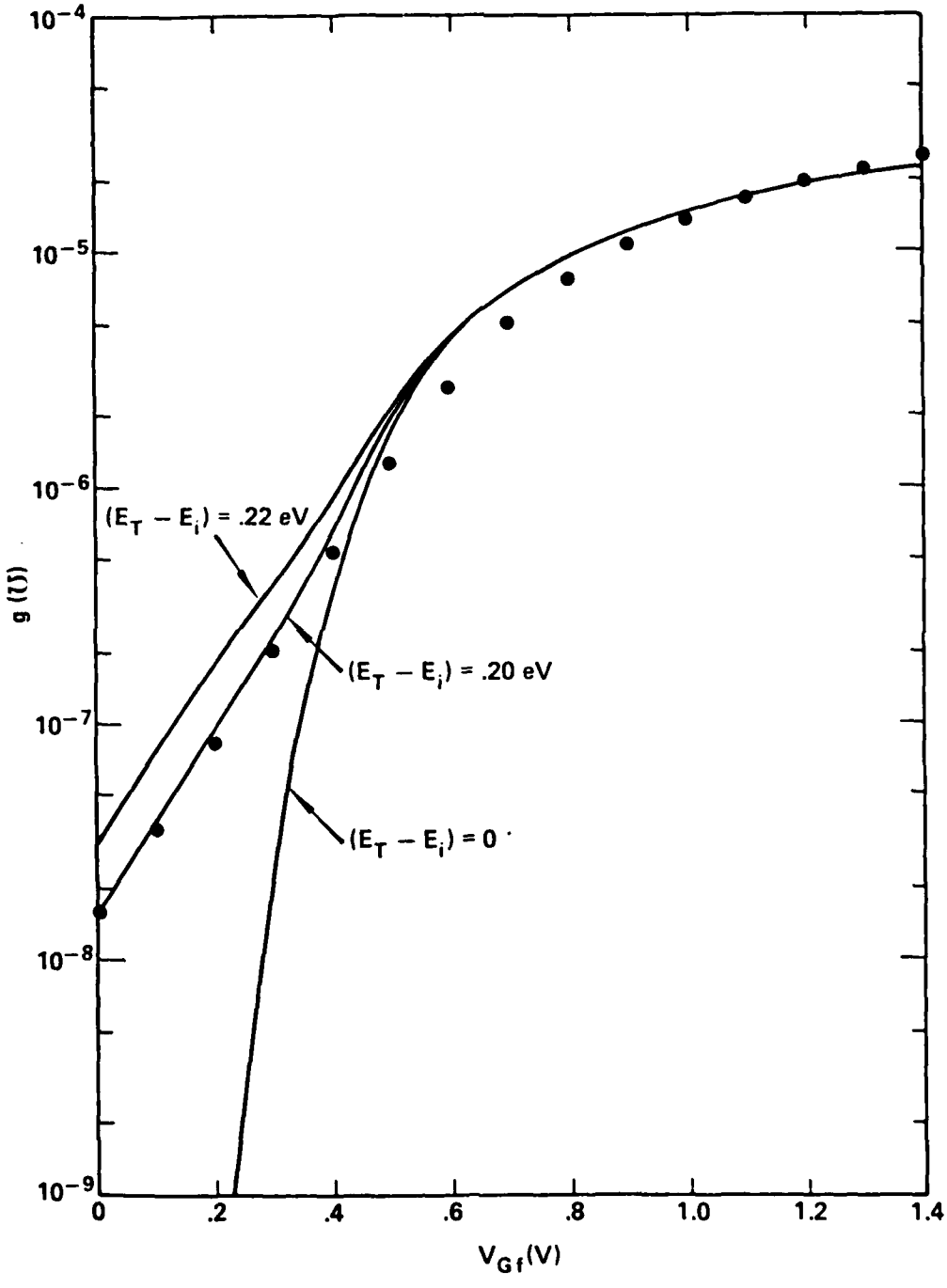
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
g (f)
$(E_T - E_i)$ = .22 eV
$(E_T - E_i)$ = .20 eV
$(E_T - E_i)$ = 0
0
.2
.4
.6
.8
1.0
1.2
1.4
V_{Gf}(V)

Fig. 1

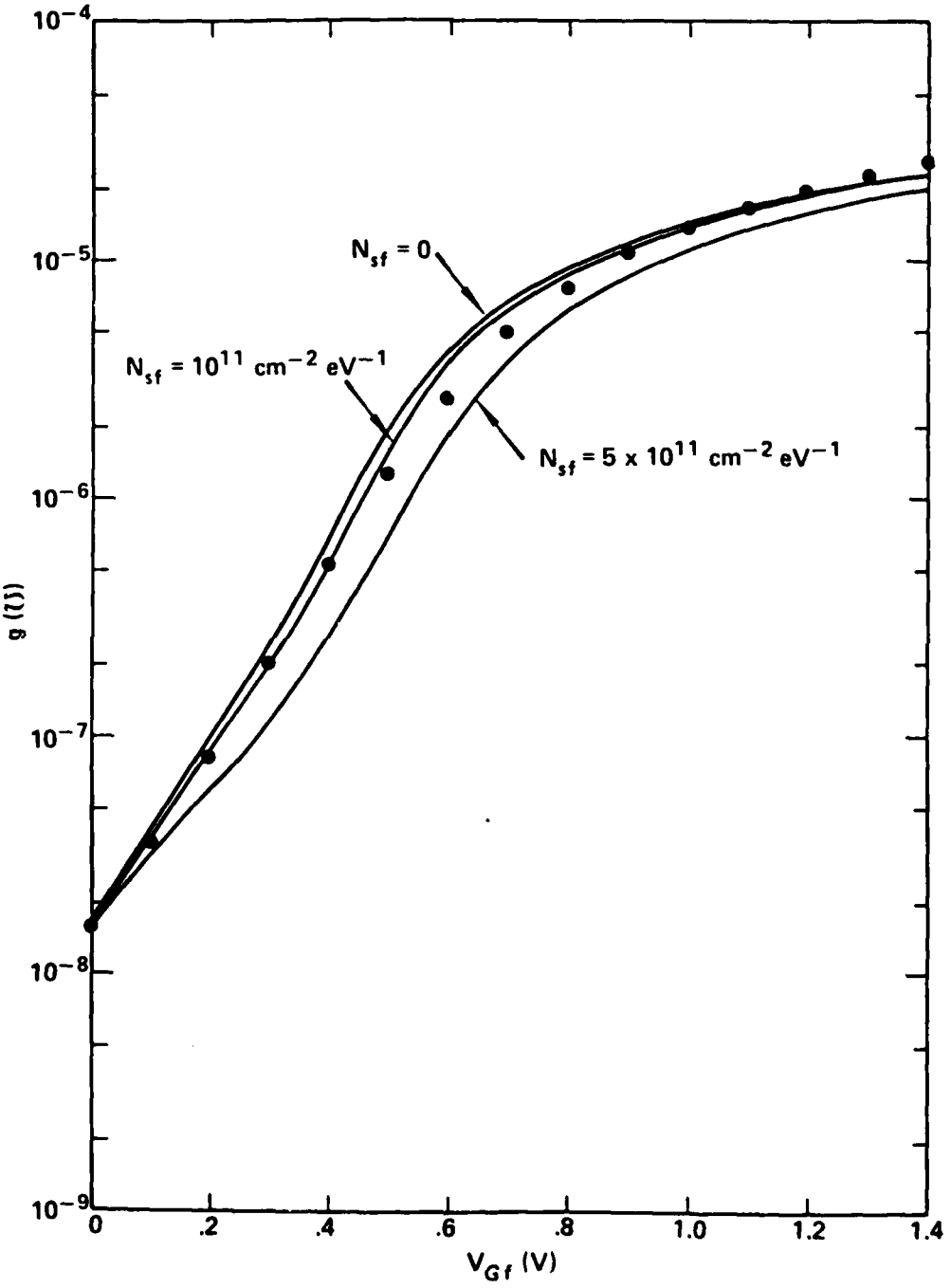
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
g (Ω)
$N_{sf} = 0$
$N_{sf} = 10^{11}$ cm^{-2} eV^{-1}
$N_{sf} = 5 \times 10^{11}$ cm^{-2} eV^{-1}
0
.2
.4
.6
.8
1.0
1.2
1.4
V_{Gf} (V)

Fig. 2

G. LINEAR-REGION CONDUCTANCE OF THIN-FILM SOI MOSFETs WITH GRAIN BOUNDARIES

The potential improvement of integrated circuits (VLSI) afforded by dielectric isolation has prompted the development of new silicon-on-insulator (SOI) technologies that yield useful thin films of (recrystallized) polysilicon deposited on silicon dioxide [1]. MOSFETs fabricated in these films differ from their bulk-silicon counterparts because of the charge coupling between the front (conventional) and back (silicon substrate) gates [2], [3] and because of grain boundaries in the channel region [4], [5]. These peculiarities influence the threshold voltage and the effective carrier mobility in the channel, measurements of which are generally used to infer the SOI material quality, and hence must be properly characterized to ensure optimal development of SOI devices and circuits.

We recently presented a physical model [5] for the effects of grain boundaries (perpendicular to the carrier flow in the channel) on the linear-region channel (drain) conductance ($g = I_D/V_D$) of SOI MOSFETs. The model accounts for the quantum-mechanical carrier distribution in the channel, the two-dimensional potential variation near a grain boundary due to carrier trapping, and the thermionic emission of carriers over the grain-boundary potential barrier Ψ_B, which can restrict the current. For an n-channel enhancement-mode MOSFET, we derived [5]

$$g \simeq \frac{\frac{Z}{L}\mu_{ng}C_{of}(V_{Gf}-V_{Tf})}{1+\frac{(N_g-1)kN_C\mu_{ng}}{0.9LA^*T}\exp(-\frac{q\Psi_B}{kT})} \tag{1}$$

where V_{Gf} is the front-gate voltage, V_{Tf} is the (front-gate) threshold voltage, N_g is the number of (identical) grains constituting the channel length L, and μ_{ng} is the intragrain electron mobility [6]. The other parameters in (1) have their usual meanings and/or are defined in [5]. The

implicit dependence of Ψ_B in (1) on $(V_{Gf}-V_{Tf})$ [5] reflects the reduction in Ψ_B that occurs as V_{Gf} and the electron density in the channel increase when the grain-boundary traps are completely filled with electrons. Thus for sufficiently high V_{Gf}, Ψ_B is low enough that the grain-boundary scattering is negligible; g is then given by the familiar numerator of (1).

The model (1) does not completely account for the charge coupling between the two gates, which defines a dependence of V_{Tf} on the back-gate voltage V_{Gb} [3]. It is directly applicable only when the polysilicon film is not completely depleted, that is, if the film is sufficiently thick or if the back silicon surface is accumulated [3]. In this case, the $g(V_{Gf})$ dependence predicted by (1) is exemplified by the curve in Fig. 1 labeled V_{Gb} = -30 V. This curve, and the others in Fig. 1, depict measured linear-region (V_D = 50 mV) $g(V_{Gf},V_{Gb})$ characteristics at room temperature of an n-channel SOI MOSFET fabricated at Texas Instruments, Inc. [7].

We measured several of these devices at different temperatures and found good correlation with (1). The polysilicon film in which they were fabricated is 0.5-μm-thick and was laser-recrystallized (with a scanning CW Ar^+ laser system) after being deposited via LPCVD on a 1-μm-thick layer of silicon dioxide, which had been thermally grown on a silicon substrate (p-type, 6-8 Ω-cm). The film was doped by ion implantation of boron that yielded, based on SUPREME-II calculations [7], $N_A \approx 2 \times 10^{16}$ cm^{-3} near the front surface and $N_A \approx 10^{15}$ cm^{-3} at the back surface. The front gate is n^+ polysilicon, and the gate oxide is 600-Å-thick ($C_{of} \approx 5.8 \times 10^{-8}$ F/cm^2). The devices are large (Z = L = 40 μm), and hence small-geometry effects are absent.

Three distinct portions of the $g(V_{Gf}, V_{Gb} = -30V)$ curve in Fig. 1 can be described based on (1). For low V_{Gf} ($< V_\mu$), Ψ_B is high and is nearly independent of V_{Gf}. The grain boundaries therefore severely inhibit channel

conduction even though $V_{Gf} > V_{Tf}$; g is very low. For intermediate V_{Gf} ($> V_\mu$), Ψ_B decreases with increasing V_{Gf}. In this region, (1) can be approximated by [5]

$$g \simeq \frac{Z}{L} \mu_{n(eff)} C_{of} (V_{Gf} - V_\mu) \qquad (2)$$

where the apparent ("mobility") threshold voltage V_μ and the effective electron mobility $\mu_{n(eff)}$ are defined by the grain boundaries, i.e., by N_g and by the trap density N_{ST} and energy level E_T. For high V_{Gf} ($>> V_\mu$), Ψ_B is low. The grain boundaries are ineffective, and g is described by the numerator of (1).

By comparing the measured $g(V_{Gf}, V_{Gb} = -30V)$ characteristic with (1) and (2), we can evaluate the device parameters involved, and then by checking the values for consistency, further support our model. The high-V_{Gf} (> 2.5 V) portion of the characteristic shown in Fig. 1 appears to be linear, which implies that the surface field effects on μ_{ng} [6] are insignificant for V_{Gf} in this range. Thus the extrapolation of this line, modeled by the numerator of (1), yields $\mu_{ng} \simeq 390$ cm^2/V-sec and $V_{Tf} \simeq 0.1$ V. Because the back surface is accumulated and the depletion-region width at the front surface is less than the silicon film thickness, $V_{Tf} \simeq V_{Tf0}$ [3], the threshold voltage predicted by the bulk-MOSFET theory. Since $N_A \simeq 2 \times 10^{16}$ cm^{-3} throughout the depletion region, the measured V_{Tf} thus implies that the fixed charge density at the front interface is $Q_{ff} \simeq q(3 \times 10^{11}$ cm$^{-2})$. Additional support for our model is now provided by the fact that the values of Q_{ff}, N_A, and μ_{ng} are crudely consistent with empirical relationships [6] that describe the observed dependence of mobility on fixed charge and doping density in silicon MOSFETs.

From the intermediate-V_{Gf} portion of the $g(V_{Gf}, V_{Gb} = -30\ V)$ characteristic in Fig. 1, modeled by (2), we find $V_\mu \simeq 0.6$ V and $\mu_{n(eff)} \simeq 550\ cm^2/V\text{-sec}$. These values, based on our grain-boundary model [5], suggest that $N_g \simeq 50$ grains and $N_{ST} \simeq 1 \times 10^{12}\ cm^{-2}$ for E_T near midgap. These crude estimates for the grain-boundary properties are not inconsistent with the typical qualities of the laser-recrystallized polysilicon films used to fabricate the devices [7]. Note that $V_\mu > V_{Tf}$, which is always true when $N_g > 1$ [4], [5], and that $\mu_{n(eff)} > \mu_{ng}$, which is typical [4], [5].

Consider now the measured $g(V_{Gf})$ characteristics in Fig. 1 for higher values of V_{Gb}, that is, for the cases in which the back surface is depleted or inverted. When the polysilicon film is completely depleted (at threshold), increasing V_{Gb} decreases V_{Tf} until the back surface becomes strongly inverted [2], [3]. Thus in the high-V_{Gf} region, in accord with the numerator of (1), the $g(V_{Gf})$ characteristic shifts to the left as V_{Gb} increases by about the corresponding change in V_{Tf}. The shift is not exactly described by $V_{Tf}(V_{Gb})$ [3] because of a weak dependence of μ_{ng} on V_{Gb} [8], which results from the modulation of the effective field in the channel [6] by V_{Gb}. Nonetheless, the $g(V_{Gf},V_{Gb})$ characteristics in the high-V_{Gf} region provide a basis for measuring the $V_{Tf}(V_{Gb})$ dependence. Using these characteristics and the method of measurement described in [3], we obtain $(V_{Tf0} - V_{Tf}^I) \simeq 0.16$ V where V_{Tf}^I is the threshold voltage when the back surface is inverted, i.e., when $V_{Gb} > V_{Gb}^I \sim 5$ V. Based on our analysis of the charge coupling for a uniform doping density [3], this threshold voltage shift corresponds to $N_A \simeq 9 \times 10^{15}\ cm^{-3}$, which is about the average of the actual density [7].

As described in [5], Ψ_B in (1) depends on $(V_{Gf}-V_{Tf})$. Thus putting the $V_{Tf}(V_{Gb})$ dependence [3] directly into (1) would yield $g(V_{Gf})$ characteristics for different values of V_{Gb} that are everywhere parallel and separated by the

change in V_{Tf} defined by the change in V_{Gb}. In (2), V_μ would vary by this same change, and $\mu_{n(eff)}$ would be unaffected by V_{Gb}. It is obvious from the measured curves plotted in Fig. 1 that this modification of (1) is invalid. With reference to (2), V_μ appears to be nearly insensitive to V_{Gb} and $\mu_{n(eff)}$ increases with V_{Gb} up to the onset of strong inversion at the back surface ($V_{Gb} = V_{Gb}^I \sim 5$ V) where back-channel conduction begins to contribute to g. The data in Fig. 1 show that $\mu_{n(eff)}$ increases from 550 to 680 cm^2/V-sec as V_{Gb} increases from -30 to +5 V.

These results imply that when the back surface is not inverted, Ψ_B is nearly independent of V_{Gb}, irrespective of the fact the electron density in the channel, which defines Ψ_B in (1) [5], is modulated by V_{Gb} when the polysilicon film is completely depleted [3]. This can be explained physically as follows. As the charge condition of the back surface changes from accumulation to inversion due to increasing V_{Gb}, the intragrain band bending Ψ_{sb} at the back surface increases from about zero to $2\phi_B$ (ϕ_B is the Fermi potential of the film). However the corresponding change in the band bending Ψ_{sb}^{GB} at a grain boundary is typically much less than $2\phi_B$ because of compensation due to the variation in Ψ_{Bb}, the grain-boundary potential barrier at the back surface. At the onset of accumulation, hole trapping at the grain boundary yields $\Psi_{Bb} = -\Psi_B^A$; hence $\Psi_{sb}^{GB} = \Psi_{sb} - \Psi_{Bb} \simeq \Psi_B^A$. At the onset of strong inversion, electron trapping yields $\Psi_{Bb} = +\Psi_B^I$; thus $\Psi_{sb}^{GB} \simeq 2\phi_B - \Psi_B^I$. Consequently if $\Psi_B^A + \Psi_B^I \sim 2\phi_B$, which is typical [5], Ψ_{sb}^{GB} does not vary appreciably with V_{Gb}. Hence at the front surface, $\Psi_{sf}^{GB} \simeq 2\phi_B - \Psi_B$ is nearly insensitive to V_{Gb}, and so is Ψ_B. However, once the back surface is strongly inverted, Ψ_{Bb} begins to diminish with increasing V_{Gb}, and hence Ψ_{sb}^{GB} approaches $2\phi_B$, which renders Ψ_B dependent on V_{Gb}. The $g(V_{Gf},V_{Gb})$ characteristic is further complicated by the back-channel contribution to it, which can be

modeled analogously to (1). These complications are evident in the V_{Gb} = 15 V curve in Fig. 1.

With this physical insight, we can modify (1) to describe completely the $g(V_{Gf},V_{Gb})$ characteristic for $V_{Gf} > V_{Tf}$ and $V_{Gb} < V_{Gb}^{I}$. In the modified version of (1), V_{Tf} in the numerator is given by the $V_{Tf}(V_{Gb})$ dependence derived in [3], and $\Psi_B(V_{Gf}-V_{Tf})$ in the denominator is defined by letting V_{Tf} be its maximum value, e.g., V_{TfO}, corresponding to accumulation at the back surface. These changes then bring (1) into agreement with the measured data in Fig. 1.

To further corroborate the modified model, we measured $g(V_{Gf},V_{Gb})$ characteristics of thin-film p-channel SOI MOSFETs that contain no grain boundaries. The film was created by implanting a buried oxide layer in a silicon substrate [7]. Typical results, plotted in Fig. 2, show that the $g(V_{Gf})$ curves for different values of V_{Gb} are everywhere parallel, reflecting directly the $V_{Tf}(V_{Gb})$ dependence [3]. Comparison of Figs. 1 and 2 then clearly distinguishes the charge-coupling effects from the grain-boundary effects apparent in Fig. 1. These results confirm our theory that grain boundaries, in addition to defining V_{μ} and $\mu_{n(eff)}$, cause the convergence of the $g(V_{Gf},V_{Gb})$ curves at low V_{Gf} ($\simeq V_{\mu}$). Measurement of $g(V_{Gf},V_{Gb})$, when interpreted based on our modified model, then not only indicates the presence of grain boundaries in the channel region, but also provides estimates of N_g and N_{ST}.

In summary, we have generalized our previously reported model [5] for the linear-region conductance of SOI MOSFETs by accounting for the charge coupling between the front and back gates and the concomitant dependence of g on V_{Gb}. The model, characterized by a generalized interpretation of (1) and illustrated with experimental support in Figs. 1 and 2, reveals that the

$g(V_{Gf})$ characteristic can be strongly influenced by grain boundaries (N_g, N_{ST}) and by V_{Gb} even when the back surface is not inverted (conducting). With reference to our discussions of the three distinct portions of the $g(V_{Gf},V_{Gb})$ characteristics and the underlying parameters, $V_{Tf}(V_{Gb})$ [3], $V_\mu(N_g,N_{ST})$, $\mu_{ng}(V_{Gf},V_{Gb})$ [6], [8], and $\mu_{n(eff)}(V_{Gb},N_g,N_{ST})$, we stress the necessity of careful interpretation of measured conductance curves to assess the quality of SOI material and devices. To avoid misleading conclusions in this regard, sound physical modeling of the devices is essential.

We note finally, with reference in particular to the intermediate-V_{Gf} region of the $g(V_{Gf},V_{Gb})$ characteristics, that the influence of grain boundaries as well as the back-gate voltage can be beneficial to the SOI MOSFET. For example, we see in Fig. 1 that the grain boundaries define an effective transconductance $[(Z/L)\mu_{n(eff)}C_{of}V_D]$ that is higher than that defined by the actual mobility; i.e., $\mu_{n(eff)} > \mu_{ng}$. Furthermore this improvement is enhanced by increasing V_{Gb} (up to V_{Gb}^I), i.e., depleting the back surface, with no significant increase in leakage since V_μ is not strongly dependent on V_{Gb}. This implies an optimal back-gate bias ($V_{Gb} \simeq V_{Gb}^I$) that was previously identified [3] for reasons associated with the intragrain charge coupling between the two gates.

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FIGURE CAPTIONS

Fig. 1. Measured linear-region (V_D = 50 mV) conductance versus front- and back-gate voltages of a laser-recrystallized thin-film n-channel SOI MOSFET (with grain boundaries). The variation of V_{Gb} from -30 V to +15 V alters the charge condition of the back surface from accumulation to strong inversion. For V_{Gb} = -30 V, the actual (V_{TfO}) and apparent (V_{μ}) threshold voltages are indicated.

Fig. 2. Measured linear-region (V_D = 50 mV) conductance versus front- and back-gate voltages of an implanted-oxide thin-film p-channel SOI MOSFET (without grain boundaries). The gate oxide thickness is 500 A and Z/L = 128μm/4μm. The silicon film and the underlying (implanted) oxide are each about 0.5-μm-thick.

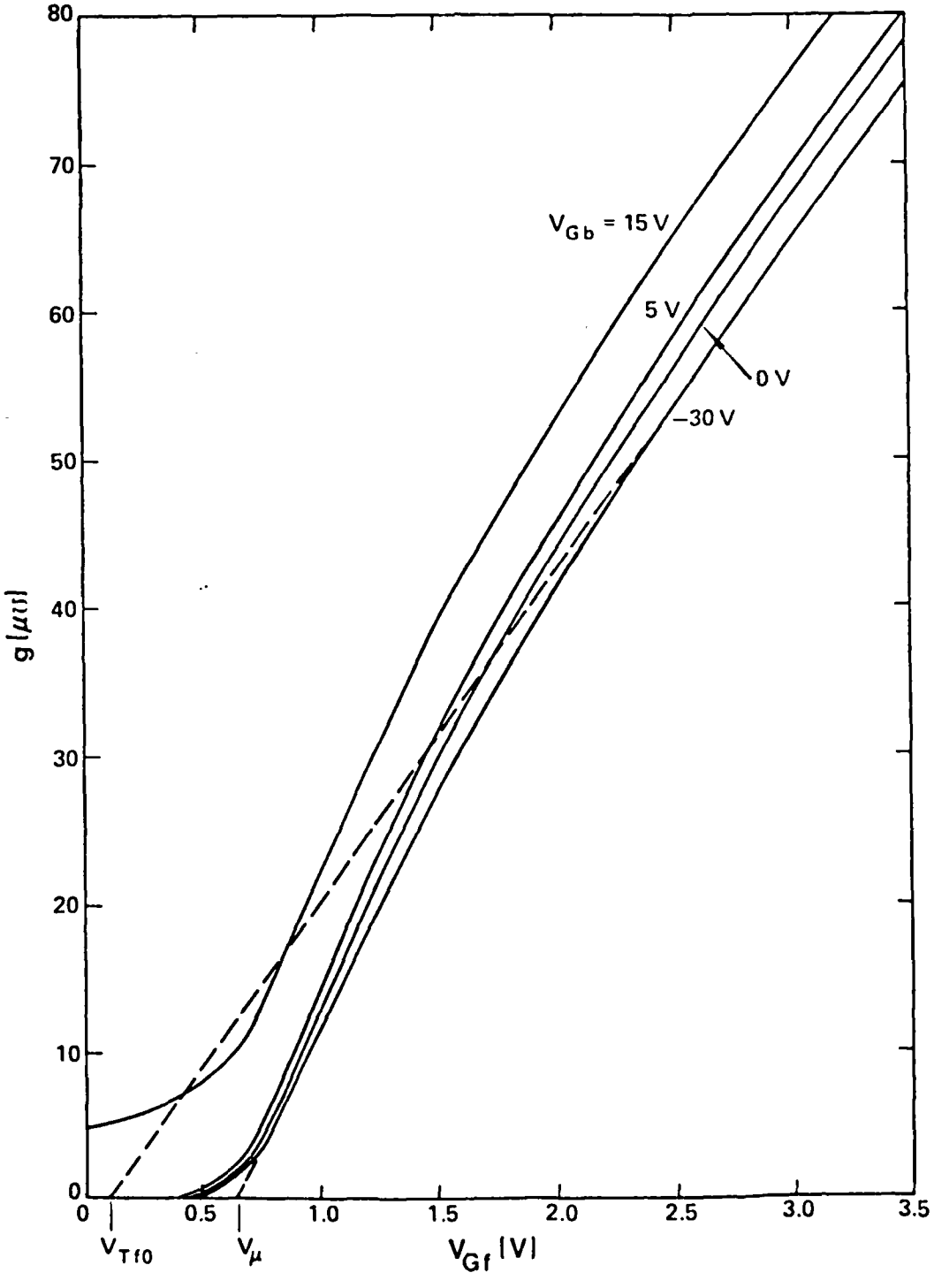
80
70
60
50
40
30
20
10
0
g [μS]
V_{Gb} = 15 V
5 V
0 V
−30 V
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
V_{Tf0}
V_{μ}
V_{Gf} [V]

Fig. 1

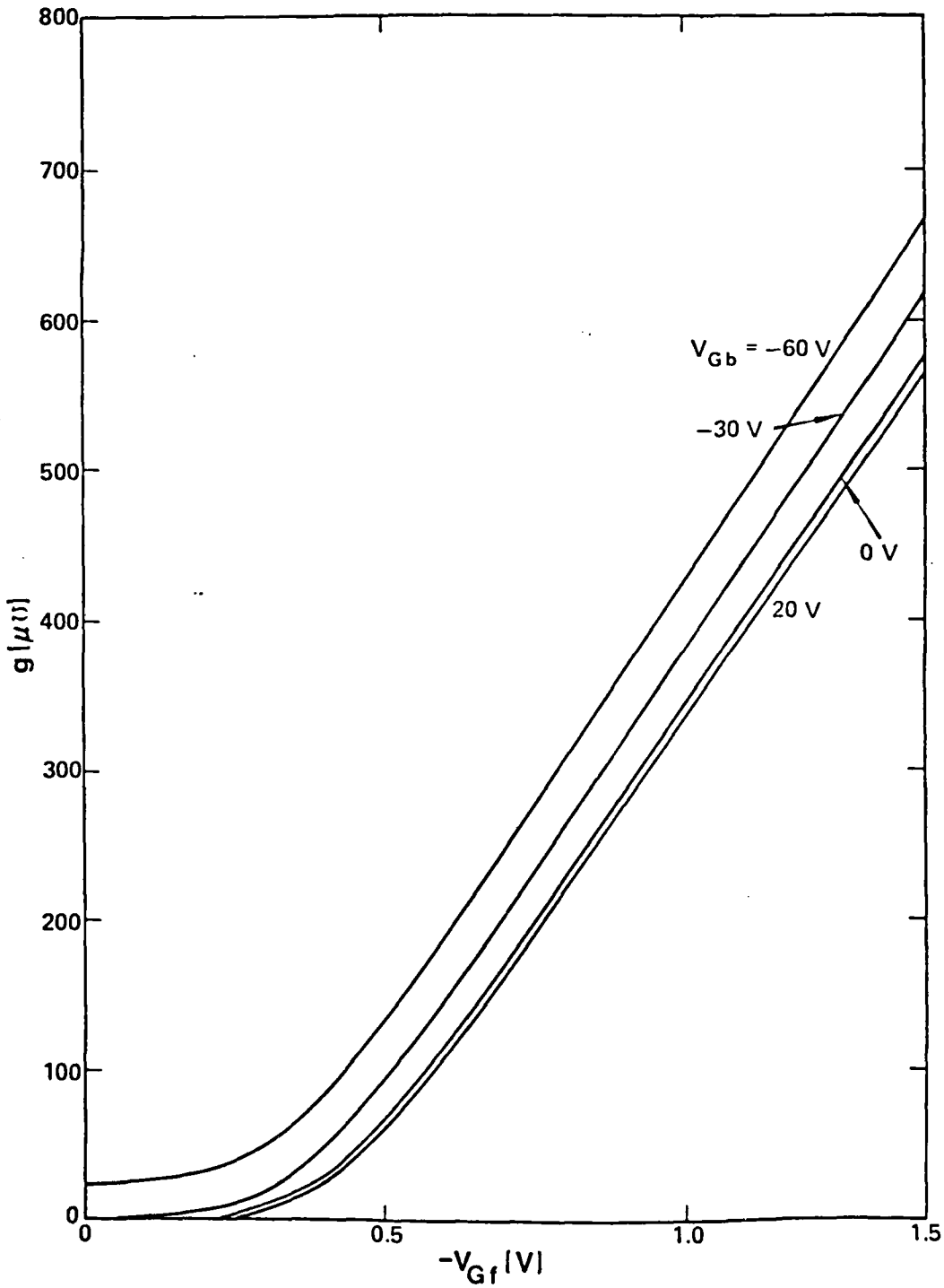
800
700
600
500
400
300
200
100
0
g [μS]
0
0.5
1.0
1.5
-V_Gf [V]
V_Gb = −60 V
−30 V
0 V
20 V

Fig. 2

H. EXTENSIONS AND APPLICATIONS OF ANALYSES

I. Grain-Boundary Orientation

The studies in Sections E-G of grain-boundary effects in SOI MOSFETs are based on the assumption that the grain boundaries are perpendicular to the carrier flow in the channel. This particular orientation maximizes the grain-boundary effect on the channel conductance as described by (20) in Section E. We have generalized the analysis to account for arbitrary orientations of the grain boundaries. This generalization is of interest because of the possibility of controlling, to some extent, the predominant grain-boundary orientation in devices constituting an IC in recrystallized SOI, and because it implies a range of MOSFET properties that could affect SOI wafer yields.

To exemplify the results of the generalization, we consider a (n-) channel region having one grain boundary running from source to drain at an angle θ from the perpendicular plane; i.e., $\theta = 0°$ if, as in Sections E-G, the grain boundary is perpendicular to the carrier flow. For this case, the drain current in the linear region is

$$I_D \simeq I_{Df} + I_{Db} \tag{1}$$

where I_{Df} is the component associated with the grain-boundary-free width (Z_f) of the channel:

$$I_{Df} = \frac{Z_f}{L} \mu_{ng} C_{of} (V_{Gf} - V_{Tf}) V_D \quad ; \tag{2}$$

and I_{Db} is the component associated with the width (Z_b) of the channel containing the grain boundary:

$$I_{Db} \simeq \frac{\frac{Z}{L}\mu_{ng}C_{of}(V_{Gf} - V_{Tf})V_D}{1 + \frac{kN_C\mu_{ng}}{0.9LA^*T}\exp(\frac{q\psi_B}{kT})\cos(\theta)} \quad . \tag{3}$$

Note that $Z = Z_f + Z_b$ and that $Z_b = L\cot(\theta)$. The $\cos(\theta)$ term is (3) accounts for the grain-boundary orientation and differentiates it from (20) in Section E.

II. Current-Voltage Characteristics

The analyses in Section E-G are applicable only in the linear region of operation, i.e., when the grain-boundary potential barrier heights are all equal and little voltage is dropped across the grain boundaries. We are presently extending the analysis to describe the effects of grain boundaries on $I_D(V_D,V_{Gf})$ in all regions of operation. This analysis is complicated because of the nonlinear characteristics of the grain boundaries and because a large V_D, which produces a variation in the degree of inversion along the channel, results in a grain-boundary position dependence for the potential barrier heights.

Although the grain-boundary effects tend to diminish as the gate voltage increases, grain boundaries near the drain can be influential even at high gate voltages (well above threshold) if the drain voltage is also high. For these conditions, the inversion is weaker near the drain, and hence the potential barriers at grain boundaries there are higher, rendering them more effective (in inhibiting carrier flow) than those near the source. For example in the saturation region, the drain current is reduced considerably by grain boundaries near the drain having properties (deep-level traps) like those in beam-crystallized SOI. However the transconductance is increased;

the saturation drain voltage is unaffected. The model thus accounts for the position (and orientation) of the grain boundaries in the channel, as well as their properties, and it necessarily accounts for all (weak-to-strong) inversion conditions in all (linear-to-saturation) regions of operation.

III. Transient Effects

The potential high speed of ICs comprising SOI (Si on SiO_2) MOSFETs is generally attributed to reduced parasitic junction capacitances resulting from the dielectric isolation. There is however another reason that thin-film SOI MOSFETs can be significantly faster than their bulk-silicon counterparts. Because the film body floats, an overshoot in the transient drain current $I_D(t)$ occurs when the device is abruptly turned on. This overshoot hastens the charging of the load capacitance, especially in low-voltage circuits, and hence tends to reduce the propagation delay t_{pd}.

We are theoretically and experimentally analyzing $I_D(t)$ and its dependence on the back-gate (substrate) voltage V_{Gb}, and decribing how it affects t_{pd} in an SOI circuit. Because the (source-drain) transit time of carriers in the channel is negligibly short, t_{pd} can be defined mainly by the overshoot in $I_D(t)$, which occurs because majority carriers in the floating film body cannot be removed instantaneously. The magnitude of the overshoot depends on the charge condition of the film at the instant the gate is pulsed on, and the decay in $I_D(t)$ depends on the mechanism of carrier removal (recombination) from the film. This mechanism is activated by a forward bias induced on the source-body junction. The resulting recombination current can be strongly dependent on V_{Gb}. The charge condition of the film, i.e., the number of majority carriers, prior to the turn-on also depends on V_{Gb}, as well as the off-time, vis-a-vis, frequency. This dependence follows from the

influence of V_{Gb} on the carrier generation rate associated with the reverse-biased source-body junction, which defines the transient discharging of the film in the off-state. Because of this dependence, and because the steady-off-state depletion-region charge is defined by V_{Gb}, the magnitude of the overshoot in $I_D(t)$ is affected by V_{Gb}. We henceforth will describe $I_D(t)$ and t_{pd} in terms of V_{Gb} and effective carrier generation and recombination lifetimes in the off- and on-states respectively.

Physical insight regarding $I_D(t)$ provided by the analysis enables characterization of the predominant mechanisms that control transient and steady-state leakage currents in SOI MOSFETs and implies design criteria to exploit potential speed benefits in SOI ICs. The transient analysis, when combined with the steady-state analyses described in the previous sections of this report, will facilitate the development of large-signal models for the SOI MOSFET. We intend to take this approach to develop a charge model for the transistor and use it in SPICE to simulate SOI devices and circuits. The initial application would be computer-aided analysis and design of stacked CMOS structures, which form the basis for three-dimensional ICs.

I. PUBLICATIONS AND PRESENTATIONS

The following papers and talks resulted from work supported in the first year of the contract. Corresponding sections of this report are noted in parentheses.

Publications

J. G. Fossum, A. Ortiz, H.-K. Lim, and H.-W. Lam, "Effects of Grain Boundaries on Channel Conduction in Thin-Film Polysilicon-on-Silicon-Dioxide Metal-Oxide-Semiconductor Field-Effect Transistors (SOI MOSFETs)", Proc. SPIE, vol. 385, pp. 65-75, Jan. 1983.

J. G. Fossum, H.-K. Lim, and A. Ortiz-Conde, "Linear-Region Conductance of Thin-Film SOI MOSFETs with Grain Boundaries", IEEE Electron Device Lett., vol. EDL-4, pp. 239-242, July 1983. (Section G)

J. G. Fossum and A. Ortiz-Conde, "Effects of Grain Boundaries on the Channel Conductance of SOI MOSFETs", IEEE Trans. Electron Devices, vol. ED-30, pp. 933-940, Aug. 1983. (Section E)

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H.-K. Lim and J. G. Fossum, "Threshold Voltage of Thin-Film Silicon-on-Insulator (SOI) MOSFETs", IEEE Trans. Electron Devices, vol. ED-30, Oct. 1983. (Section C)

H.-K. Lim and J. G. Fossum, "Current-Voltage Characteristics of Thin-Film SOI MOSFETs in Strong Inversion", IEEE Trans. Electron Devices, vol. ED-31, 1984. (Section D)

Presentations (by J. G. Fossum)

"Effects of Grain Boundaries on Channel Conduction in Thin-Film SOI MOSFETs", SPIE Technical Symposium, Los Angeles, CA, Jan. 1983.

"Effects of Grain Boundaries on Channel Conduction in Thin-Film SOI MOSFETs", Electrical Engineering Seminar, Stanford University, Stanford, CA, Jan. 1983;
also, Technical Seminar, Texas Instruments, Inc., Dallas, TX, Jan. 1983.

"Theoretical-Experimental Analysis of the Effects of Grain Boundaries on the Electrical Properties of SOI MOSFETs", NRL Contract Review Meeting, Naval Research Laboratory, Washington, D.C., May 1983;
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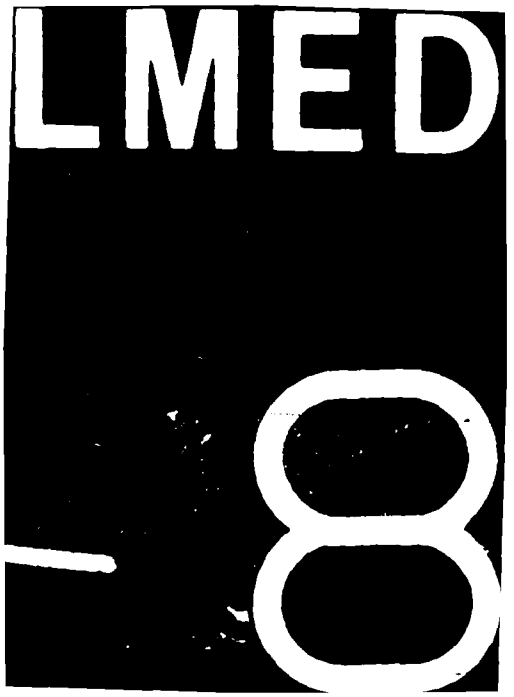
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