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HONEYWELL CORPORATE TECHNOLOGY CENTER BLOOMINGTON MN
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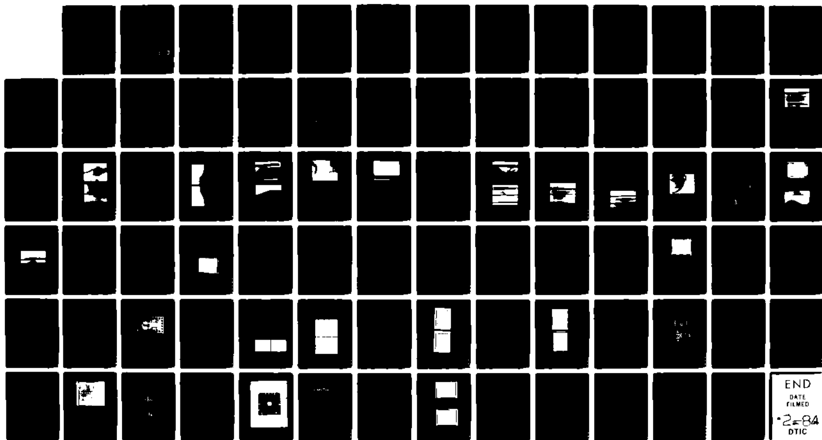

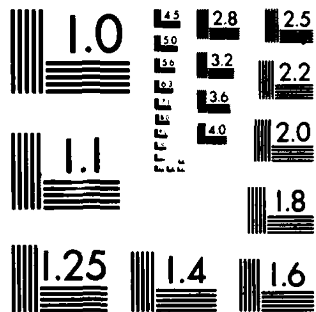

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GaAs GIGABIT MONOLITHIC OPTOELECTRONIC TRANSMITTER

Final Report

Honeywell Corporate Technology Center
10701 Lyndale Avenue South
Bloomington, Minnesota 55420

October, 1983
Final Report for July, 1981—August, 1983

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The objective of this program was to develop the Technologies required to monolithically integrate a high performance AlGaAs laser diode with high-speed digital GaAs circuitry. This objective was met with the demonstration of a fully integrated optoelectronic transmitter consisting of a Transverse junction stripe (TJS) laser diode, a power driver transistor, and a 4:1 multiplexer. This demonstration is the first major step in the development of high speed optical interconnects for future digital systems operating a gigabit/second data rates.

Other significant accomplishments which were achieved during this period were:

- Drove a discrete TJS laser (fabricated at Honeywell) at 1 Gb/s with the GaAs Mux/driver IC.

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- Demonstrated TJS lasers with threshold currents (I_{TH}) less than 35 mA.
- Demonstrated the first TJS laser-in-a-well (I_{TH} = 42 mA).
- Developed the Undercut Mirror Process.
- Demonstrated the first integratable TJS laser-in-a-well with Undercut Mirror (I_{TH} = 52 mA).
- Operated the 4:1 Mux at GHz rates.
  - Above 1.8 GHz clock rate with DC inputs
  - 1.2 Gb/s with high speed inputs (test system limited).
- Demonstrated a planarization technique that produced mirror smooth surfaces for digital IC fabrication.
- Developed a custom package for the optical transmitter.

Summary

Integrated Optoelectronic Circuits (IOECs) are being developed to meet the needs of future digital systems operating at multiple Gb/s data rates. These systems will require extremely broadband, low dispersion, low loss data buses for chip-to-chip, board-to-board and system-to-system interconnection. Long distance fiber optic communication links will also require Gb/s capabilities for the transmission of multiplexed signals over one channel. Optical interconnects and fiber optic links consisting of an integrated optoelectronic transmitter, optical fiber and integrated optoelectronic receiver are possibly the best solution to meet these needs. However, due to the different and often conflicting requirements for the fabrication of high performance lasers and electronics, only very elementary integrated laser/driver structures (less than six transistors) have been reported.

Honeywell has developed a unique concept for optoelectronic integration termed "laser-in-a-well" which presents a simple solution to the problems which have plagued other integration schemes. During the 24 month span of this contract, the laser-in-a-well concept was used to develop the processes required for integrating AlGaAs lasers with small to medium-scale digital GaAs electronics.

This study was culminated with the first operational IOEC which contains a semiconductor laser diode and small scale (36 gates) GaAs circuitry. The transmitter consisted of a transverse junction stripe (TJS) laser, a field effect transistor (FET) power driver, and a 4:1 multiplexer (developed with Honeywell funding). All elements were fabricated on a semi-insulating substrate. The multiplexer (Mux) and driver active regions are formed by selective ion implantation while the TJS laser is fabricated in epitaxial layers grown by liquid phase epitaxy (LPE) in a well that is etched into the substrate.

The fully monolithically integrated laser/Mux IC was tested to a clock rate of 160 MHz. In this report, the results of this program to date are presented. The development of the processing for the laser diode and the GaAs electronics and the operation of the individual elements are described. We also report on the successful integration of the components and suggest some areas for future investigation.

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Section 1
Introduction

Medium-scale integration-level gallium arsenide integrated circuits (GaAs ICs) have been shown to operate at multiple gigabit/second (Gb/s) data rates. Future high-speed digital systems fabricated with these chips will require extremely broadband/low dispersion/low cost data buses for board-to-board and system-to-system interconnection. Even chip-to-chip electrical interconnects will be difficult at speeds above a few Gb/s due to the problems in controlling impedances during packaging. Long distance data communication links will also require Gb/s capabilities for the transmission of time multiplexed signals over one channel. Optical interconnects and fiber optic links may be the best solution to these problems. The optical fibers can have bandwidths of hundreds of GHz and loss less than 1 dB/km. Semiconductor laser diodes and optical detectors have been demonstrated at data rates greater than 8 Gb/s[1].

In order to realize the full performance available from an optical system, it is desirable to have the optoelectronic components monolithically integrated with the electronics. This eliminates the excess capacitance and inductance associated with bonding pads and wires and removes the need for a broadband impedance match. The result is a smaller, more rugged, and higher performance circuit when compared to the hybrid counterpart.

The first integrated optoelectronic circuit was reported by the California Institute of Technology where an aluminum gallium arsenide (AlGaAs) laser was combined with a GaAs Gunn diode.[2] Since then, work on optoelectronic integration has been reported by several laboratories. Some of the integrated components which have been reported include laser/FETs,[3,4] pin detector/FETs[5] and an optical repeater[6].

1. R. Tell and S.T. Eng, "8 Gbit/s Optical Transmission with TJS GaAlAs Laser and p-i-n Detection," Electron Lett., Vol. 16, pp. 497-498: June, 1980.
2. C.P. Lee, S. Margalit, I. Ury, and A. Yariv, "Integration of an Injection Laser with a Gunn Oscillator on a Semi-insulating GaAs Substrate," Appl. Phys. Lett., Vol. 32, pp. 806-807: June, 1978.
3. I. Ury, S. Margalit, M. Yust, and A. Yariv, "Monolithic Integration of an Injection Laser and a Metal Semiconductor Field Effect Transistor," Appl. Phys. Lett., Vol. 34, pp. 430-431: Apr. 1979.
4. T. Fukuzawa, N. Nakamura, H. Hirao, T. Kuroda, and J. Umeda, "Monolithic Integration of a GaAlAs Injection Laser with a Schottky-gate Field Effect Transistor," Appl. Phys. Lett., Vol. 36, pp. 181-183: Feb. 1980.
5. R.F. Leheny, R.E. Nahory, M.A. Pollack, A.A. Bullman, E.D. Beebe, J.C. DeWinter, and R.J. Martin, "Integrated $In_{0.53}Ga_{0.47}As$ p-i-n FET Photoreceiver," Elect. Lett., Vol. 16, pp. 353-354, May, 1980.
6. M. Yust, N. Bar-Chaim, S.H. Izadpanah, S. Margalit, I. Ury, D. Wilt, and A. Yariv, "A Monolithically Integrated Optical Repeater," Appl. Phys. Lett., Vol. 35, pp. 795-797: Nov. 1979.

Although programs aimed at the integration of optoelectronic elements with electronic circuits are underway at numerous laboratories throughout the world, only very elementry structures (less than 7 components) have been reported until now. The slow development of these components is due in large part to the different and often incompatible processing requirements for high-performance AlGaAs heterostructure lasers and GaAs electronics.

Honeywell developed the "laser-in-a-well" technology to overcome the difficulties suffered by other integration techniques.

In this report, we describe the program which led to the successful integration of a semiconductor laser diode with a 36 gate GaAs circuit. A schematic representation of the integrated optoelectronic transmitter is shown in Figure 1. It contains a semicondutor laser, a driver FET (field effect transistor) and a 4:1 time multiplexer. These elements are described in the following sections.

STATEMENT OF THE PROBLEM

The materials and processing required for semiconductor lasers and electronics are different and often incompatible. This has been primarily responsible for the relatively slow development of integrated optoelectronic structures. Therefore, it is important that a method be developed for combining the two dissimilar technologies using materials and processes which do not place prohibitive restrictions on the performance or geometry of the optical and electronic devices.

The requirements for the efficient operation of semiconductor laser diodes necessitate that the devices be fabricated in hetero-epitaxial layers. The different bandgap materials which form the heterostructure provide excellent minority carrier and optical confinement in the narrow active layer.

In contrast to the laser diode, GaAs MESFET (metal-semiconductor FET) circuits contain majority carrier devices which, to obtain the best high-speed performance, should not be fabricated in the layers used for laser diodes in order to avoid introducing unwanted parasitics. In addition, the extremely narrow metal lines in high-speed GaAs gates require that the substrate material have a high-quality, planar surface during processing.

The recent published results have shown that monolithic integration of electrical and optical components is possible, but these reports have not demonstrated the feasibility of integrating a laser diode with medium-scale, high-speed circuits. The limiting factors in the reported devices relate to (1) the fabrication of the laser and the driver circuit in epitaxial layers using designs which compromise the performance of one or both components; (2) the use of nonplanar laser structures which limit the resolution and reproducibility necessary for high-speed GaAs gates; and (3) the restrictions placed on chip area by the use of lasers designed to have two cleaved mirrors.

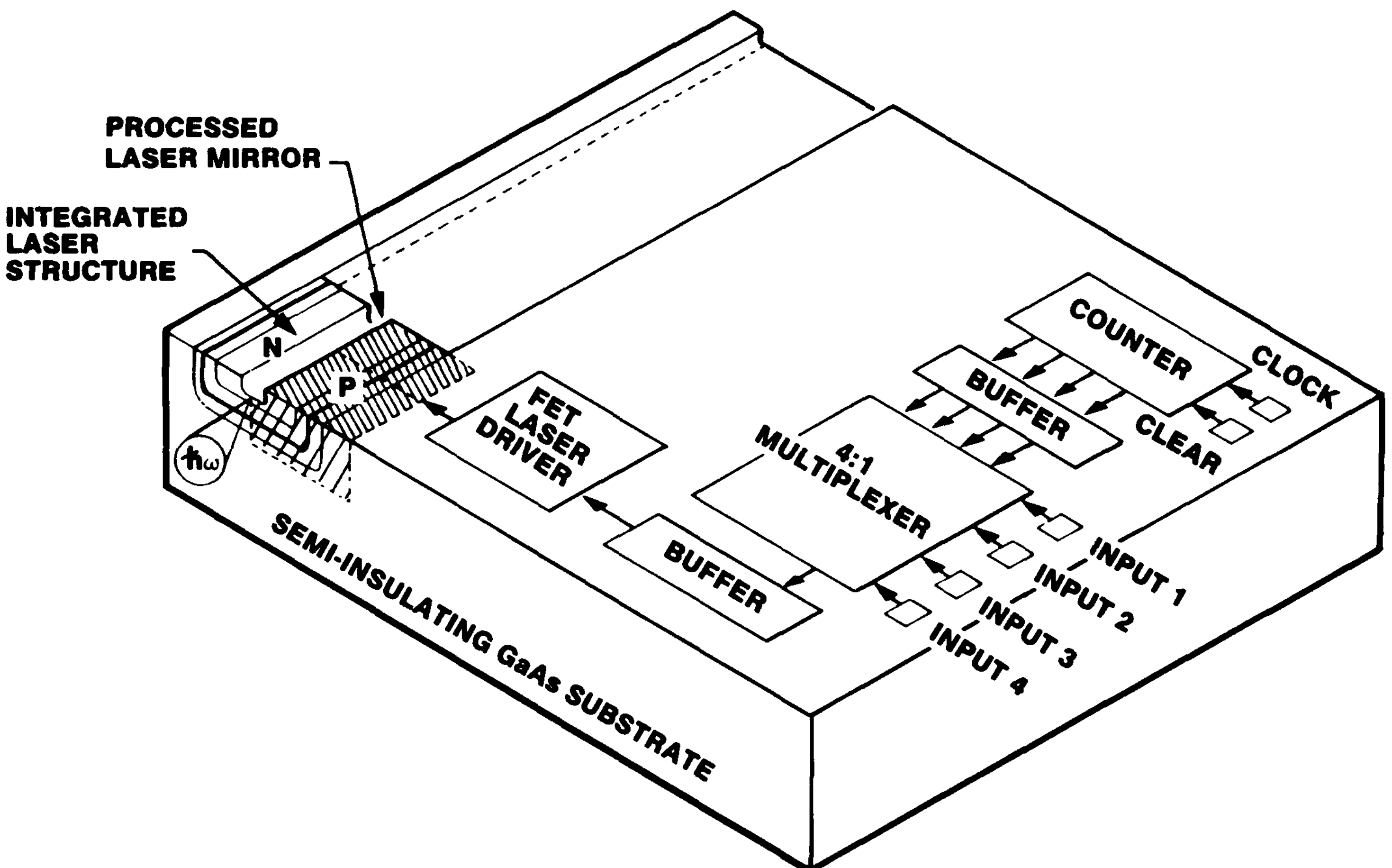

Figure 1. Block Diagram of Honeywell's Integrated Optoelectronic Transmitter. Approach is based on our "laser-in-a-well" concept for monolithic integration of lasers and medium-scale GaAs MESFET circuitry.

Honeywell's laser-in-a-well design concept was developed to address all of the issues mentioned above. The details of this unique process are presented in the following section.

PROGRAM OBJECTIVE

The overall objective of the completed program was to fabricate a monolithic optoelectronic transmitter consisting of an AlGaAs/GaAs laser diode and a GaAs multiplexer and driver. The system was designed to combine four 250-Mb/s electrical signals for transmission by the laser at 1 Gb/s. This goal was to be achieved by first developing processes compatible with both the high-performance lasers and the digital electronics and then combining these elements using the laser-in-a-well concept.

PROGRAM OVERVIEW

In this program, Honeywell used the laser-in-a-well design concept and high-speed GaAs MESFET technology to produce the first monolithic optoelectronic transmitter containing a laser, power driver, and small-scale digital electronics. The development of the monolithic optoelectronic transmitter involved three major tasks:

(1) Development of an integratable laser-in-a-well.

(2) Development of the digital GaAs multiplexer/driver electronics.

(3) Integration of the laser and the electronics.

Each of these major tasks involved several subtasks:

(1) Laser-in-a-well development:

- Controlled LPE growth of hetero-epitaxial layers in wide wells on semi-insulating GaAs substrates. This includes strict control of layer thickness, doping and composition.

- Restoration of the planar surface of the substrate following the epitaxial growth in the wells.

- Processing of an on-chip laser facet to remove any restriction on the size of the adjacent electronics.

- Evaluation of both the optical and high-speed operation of the laser.

(2) Electronics development:

- Design, layout, and fabrication of a set of photolithographic masks including different driver and multiplexer designs. The multiplexer development was a Honeywell funded task.

- Fabrication of the GaAs IC test set using the first set of masks.

- Evaluation of the operating characteristics of the different designs of drivers and multiplexers.

(3) Laser/electronics integration:

- Fabrication of laser/driver/multiplexer ICs from the first mask set and properly prepared substrates.

- Mask modifications.

- Operation and evaluation of the monolothic transmitter.

Section 2
Integratable TJS Laser

The laser-in-a-well requires a planar laser structure which can be fabricated in layers grown on semi-insulating GaAs. For this reason, we developed the Transverse Junction Stripe (TJS) laser as described in a later section. Many other features of the TJS laser make it ideal for use in a high-speed optoelectronic system. These include:

- Reported operation of a discrete TJS laser at 8 Gb/s.[1]
- Stable single longitudinal mode and fundamental transverse mode operation over a wide range of currents and temperatures.
- Predicted median room-temperature lifetimes up to 10^6 hours.[7]
- Extremely low lasing thresholds ($<$30mA).

A flow diagram of the steps required to fabricate an integratable TJS laser are shown in Figure 2. The laser process, the laser-in-a-well, LPE (liquid phase epitaxy) crystal growth, the zinc diffusion, and the Undercut Mirror Process are described in this section.

LASER PROCESS DESCRIPTION

Figure 3 is a cross-sectional view of a TJS laser. It is fabricated in epitaxial layers of GaAs and AlGaAs which are grown on a semi-insulating GaAs substrate. The layers which are successively grown on the semi-insulating substrate are: n-$Al_{0.4}Ga_{0.6}As$, n-GaAs, n-$Al_{0.4}Ga_{0.6}As$, n-GaAs. The typical carrier density and thickness of the middle GaAs layer that forms the active region is $2.5 \times 10^{18}cm^{-3}$ and 0.25μm, respectively. The transverse p-n homojunction is formed in the active layer by selectively diffusing zinc into the structure. The sample is then placed in a high temperature furnace (900°C) and the zinc is driven down through the layers to the substrate, forming p-n junctions in each of the four layers. By adjusting the diffusion process, a p^+-p-n region can be formed which improves the device performance by virtue of additional optical and carrier confinement. Both ohmic contacts are formed to the top GaAs layer. The current flow is effectively concentrated through the narrow band-gap active region by etching away the p-n junction in the top GaAs layer and by the wide band-gap of the two AlGaAs layers.

The standard TJS laser on a planar GaAs substrate is easily modified to be integratable by growing the epilayers in a well, etched into a semi-insulating substrate (laser-in-a-well) and by processing an on-chip laser mirror facet as a final step. Such a laser is shown schematically in Figure 4. The description of each of these processing steps is given below.

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7. S. Nita, N. Namizaki, S. Takamiya, and W. Susaki, "Single Mode, Junction-up TJS Lasers with Estimated Lifetime of 10^6 Hours," IEEE Quantum Electron., Vol. QE-15, pp. 1208-1209: Nov. 1979

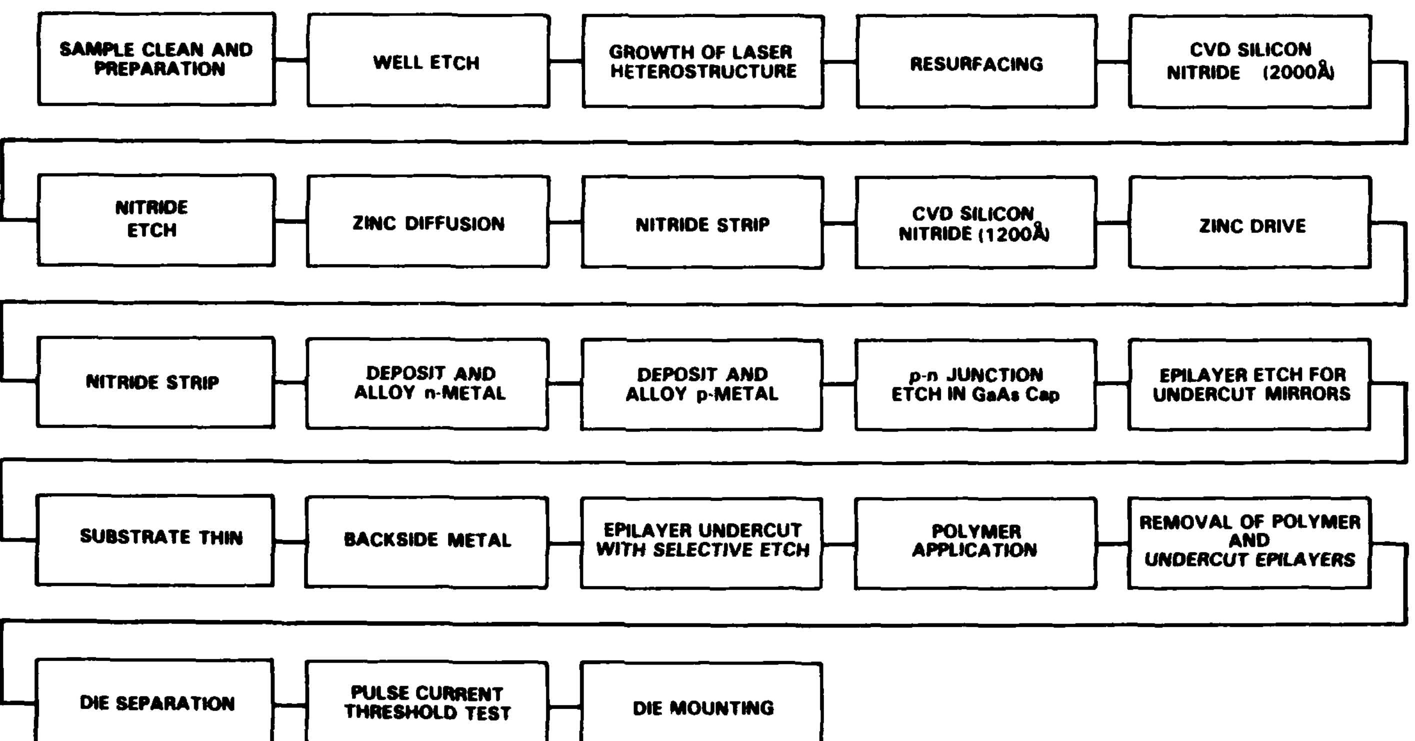

Figure 2. Process Flow Chart for Integratable TJS Laser.

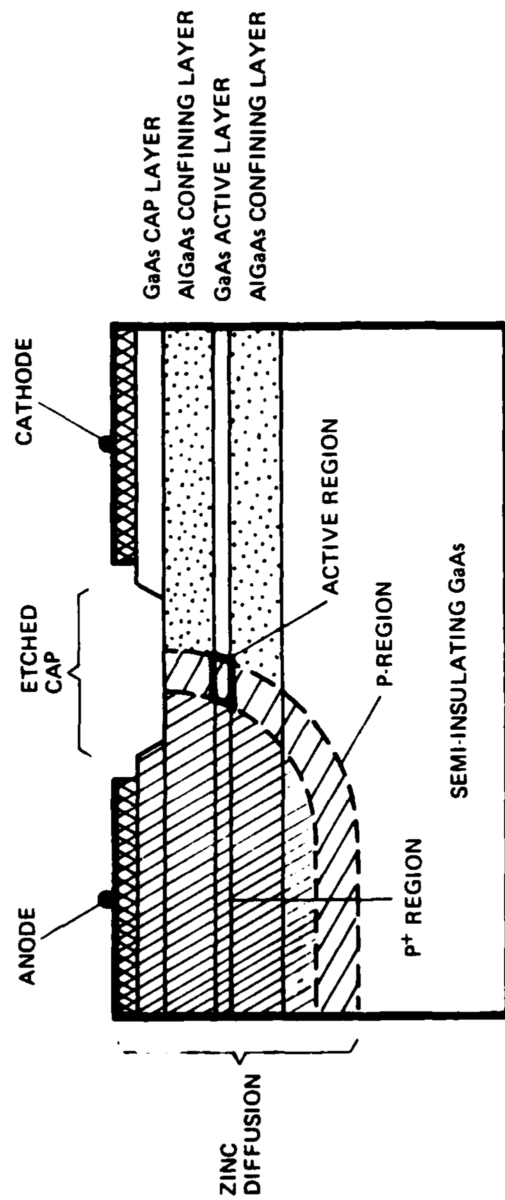

Figure 3. Schematic Cross Section of TJS Structure on Semi-Insulating Substrate.

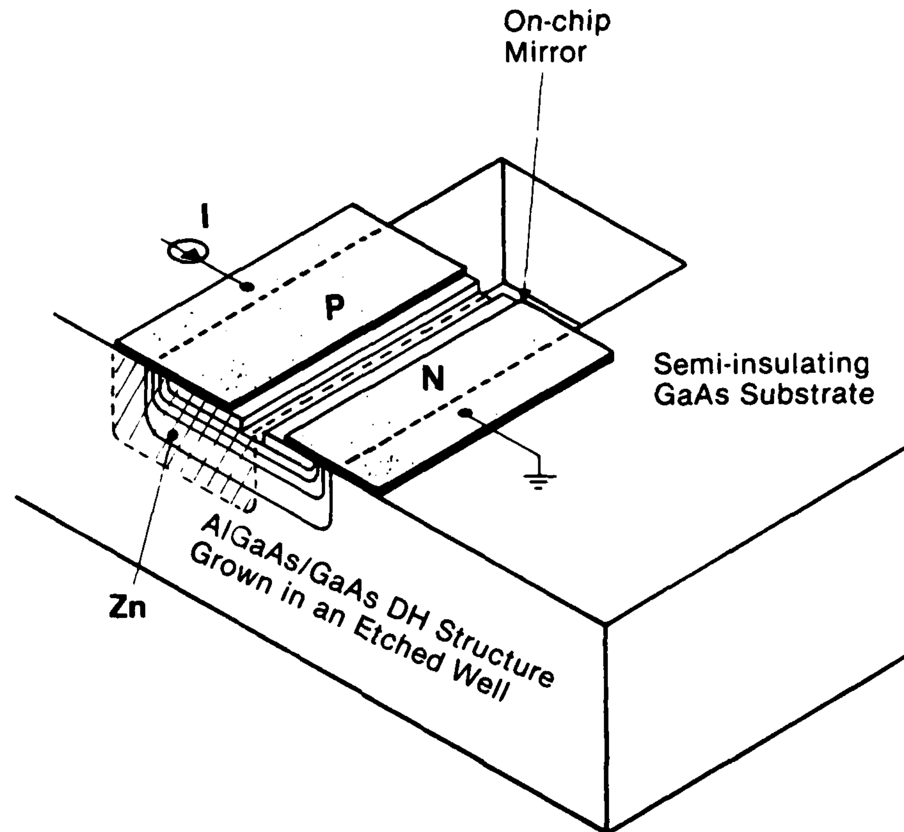

Figure 4. Schematic Representation of Integratable TJS Laser Grown in an Etched Well. The on-chip mirror facet is formed by the undercut mirror process.

LASER-IN-A-WELL

The basis for the Honeywell approach to IOECs is a materials preparation method termed "laser-in-a-well." This technique presents a simple solution to the problems that have plagued other integration schemes. The materials preparation for this integration method is illustrated in Figure 5. First, wells are etched in a semi-insulating GaAs substrate (Figure 5a), and subsequently, the appropriate epitaxial layers for the optical component are grown (total thickness less than well depth) over the entire substrate (Figure 5b). The wafer is then planarized by a chemo-mechanical process which removes the epitaxial layers from the unetched regions, exposing the substrate while preserving the grown layers in the wells. The resulting planar surface consists of semi-insulating substrate for MESFET fabrication (by direct ion implantation) and regions of epitaxial layers on the semi-insulating substrate for the optical components (Figure 5c). The advantages of this scheme include: 1) the wafer has a near-planar surface to take advantage of existing planar technology and to simplify processing steps; 2) all the components are at the surface, which facilitates

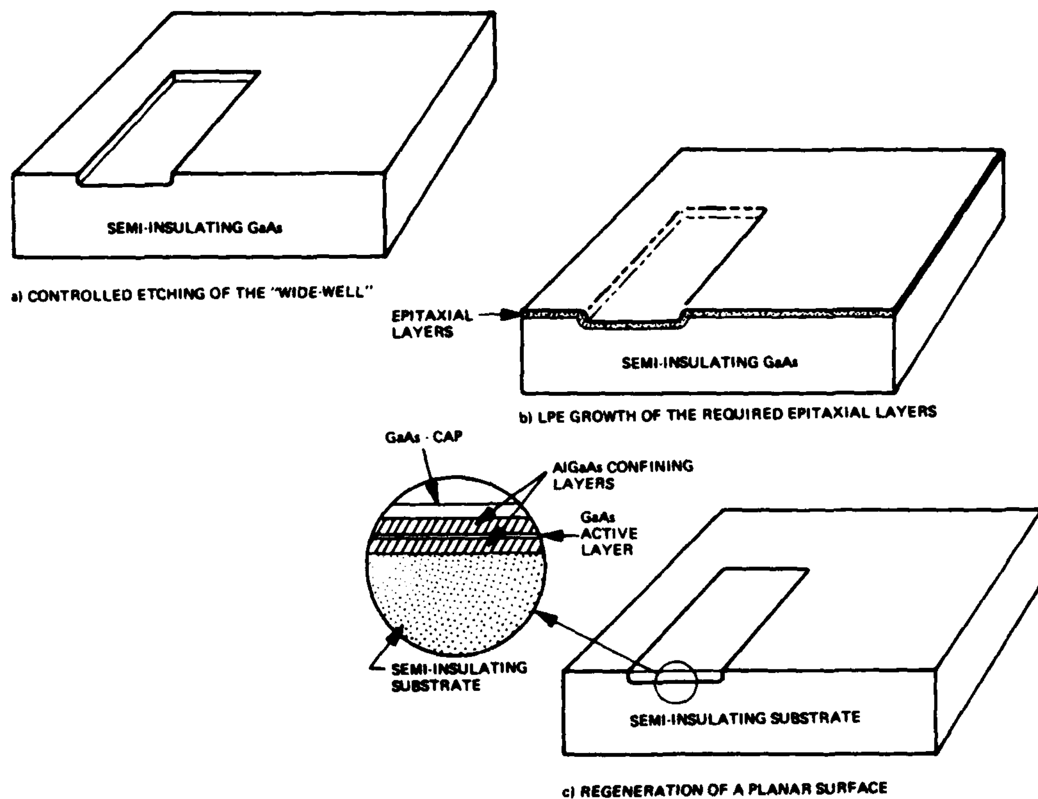

Figure 5. Schematic of the Materials Preparation for Honeywell's "Laser-in-a-Well". Insert shows the resulting epitaxial layer structure in the well. The final wafer surface is planar and, except for the epitaxial region, available for MESFET circuitry.

testing, contacting, etc.; 3) there is no restriction on the size or complexity of the GaAs electronics because the epilayers cover only a limited area of the chip; 4) this approach permits separate but parallel development programs for the electronics and the integratable optoelectronic elements on semi-insulating substrates.

This approach to integration has been successfully employed on wafers up to one square inch to fabricate AlGaAs TJS lasers grown in wells. In the next subsection, the crystal growth (liquid phase epitaxy) is described. The steps for resurfacing are described in the Laser Process Development section.

CRYSTAL GROWTH

High performance semiconductor laser diodes must be fabricated using high quality heterostructures. In order to obtain the planar structures for the monolithic transmitter, these layers must be controllably grown in wells etched into large substrates. Finally, it must be possible to remove the layers grown outside of the wells, leaving a smooth surface for producing 1μm linewidths by photolithography. The majority of the crystal growth development during this program was aimed at achieving these three requirements: high quality epitaxial layers, controlled growth in the etched wells, and good morphology of the layers grown outside of the wells.

The crystal growth technique used during the course of the contract was liquid phase epitaxy (LPE). Although LPE has a number of serious drawbacks for optoelectronic integration, it was the most straightforward crystal growth technique with which to demonstrate the feasibility of optoelectronic integration.

As a part of the task of crystal growth, we investigated the effects of growth in etched wells. The important features were: 1) the ability to control layer thicknesses in the well, 2) the shape of the grown layers at the edge in the well, 3) the morphology both in and out of the well, and 4) the uniformity of the layer thicknesses across the wafer. There are three variables which were investigated: 1) the shape and size of the well, 2) the exposed crystal planes after etching, and 3) the depth of the well. The results of these studies are described in Section 3, the Crystal Growth subsection.

ZINC DIFFUSION

The selective zinc diffusion and subsequent zinc drive are the most crucial processing steps in the fabrication of a TJS laser. This is because the zinc produces the p-n homojunctions, the lateral optical cavity, and lateral electrical confinement if done properly. If done improperly, it produces large amounts of electrical and optical loss, introduces other detrimental dopants, and damages the wafer surface.

As shown in Figure 3 the zinc provides the laser with its p-n junction. The zinc also produces a p-p^+ junction. These two junctions are instrumental in providing electrical carrier confinement as well as optical waveguiding. The separation of the two junctions defines the width of the active region and greatly impacts such device characteristics as threshold current, series resistance, single-mode operation and modulation characteristics.

The zinc level in the active region and the active region width are dependent on the zinc diffusion mask and the zinc diffusion/drive schedule. During the optoelectronic integration program, the processing steps were developed to fabricate TJS lasers on one square inch substrates. This sequence required the deposition of pyrolitic CVD (chemical vapor deposited) silicon nitride (700°C deposition), zinc diffusion in a

sealed quartz ampoule (700°C, 1 hr), deposition of a new film of CVD nitride, and a 900°C zinc drive. Further details of the zinc diffusion process are given in the section on Laser Process Development.

UNDERCUT MIRROR

To avoid placing any restriction on the size of the electronic circuitry due to the length of the laser, an on-chip laser mirror must be fabricated. In the literature, there are numerous reports of lasers with etched facets[8,9,10]. These facets were formed using either wet-chemical processing or dry processing. In each case, however, it was reported that the laser threshold for a laser with a processed mirror was higher than a comparable laser with two cleaved mirrors. Therefore, it was considered essential to develop a technique for producing a cleaved mirror in the middle of the GaAs wafer. Honeywell developed the Undercut Mirror technique for this purpose.

The Undercut Mirror requires two photolithographic steps and two etching steps. In the first lithographic step, the laser and a small dove-tail shaped region at the end of the laser stripe are masked with photoresist. The lasers are then placed in a solution which non-selectively etches away the exposed GaAs and AlGaAs epilayers from around the protected end regions, uncovering the GaAs substrates. In the second step, the lasers are placed in a solution which selectively etches just the exposed GaAs substrate, (not the AlGaAs epilayers) undercutting the protected region at each end of the laser stripe and producing a wing of epitaxial material which hangs out over an etched valley. This is shown schematically in Figure 6. Breaking off the undercut epilayers produces a flat, cleaved facet at the end of the laser.

The undercut mirror process developed at Honeywell is similar to the "micro-cleaved mirror" process reported by the California Institute of Technology[11] and at Fujitsu[12]. All three of these processes were developed independently. However, Honeywell has developed a unique method for breaking off the undercut epilayers. The complete undercut mirror process will be described further in the following section.

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9. J.L. Merz, R.A. Logan, and A.M. Sergent, "GaAs Integrated Optical Circuits by Wet Chemical Etching," IEEE J. Quantum Electron., Vol. QE-15, pp. 72-81: Feb. 1979.

10. K. Iga and B.I. Miller, "C.W. Operation of GaInAsP/InP Laser with Chemically Etched Mirror," Electron. Lett., Vol. 16, pp. 830-832: Oct. 1980.

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12. O. Wada, S. Yamakoshi, T. Fujii, S. Hiyamizu, and T. Sukarai, "AlGaAs/GaAs Microcleaved Fact (MCF) Laser Monolithically Integrated with Photodiode," Electron. Lett., Vol. 18, pp. 189-190: March, 1982.

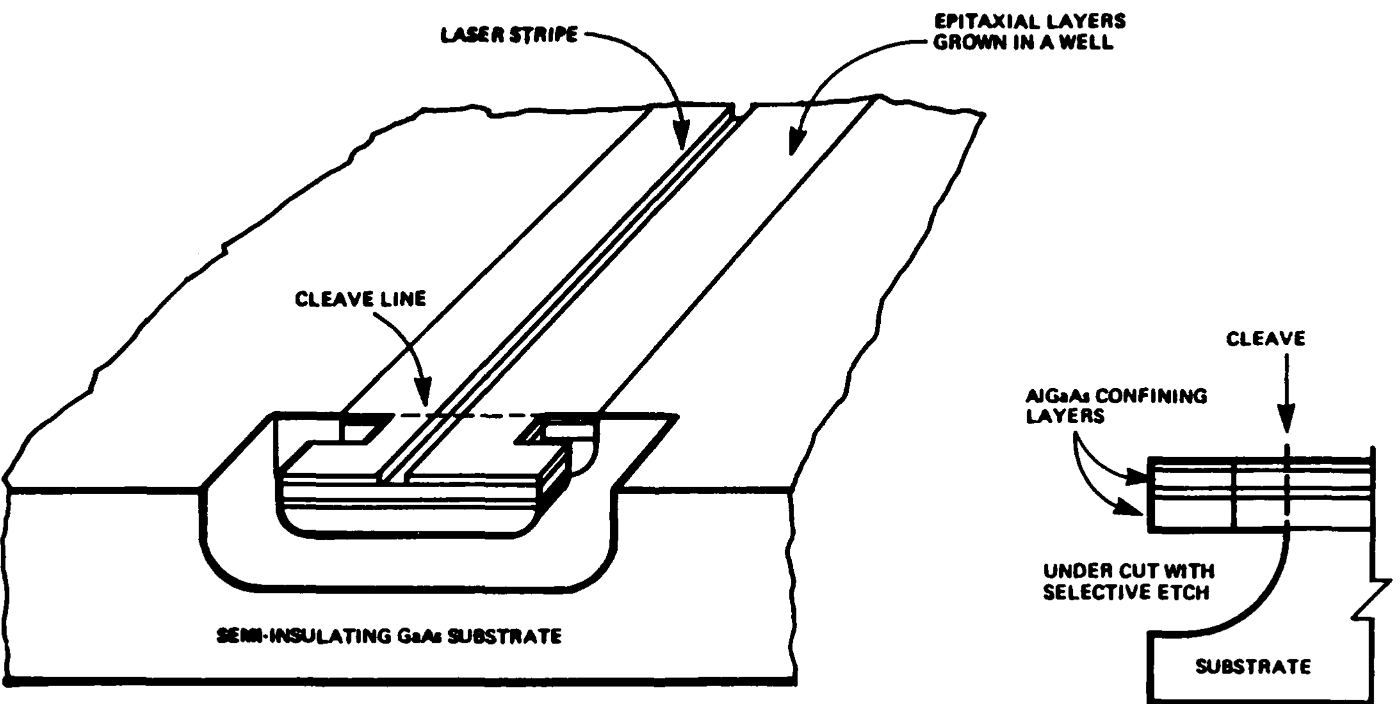


Figure 6. Artist's Conception of the Undercut Mirror Process. The small wing at the end of the laser stripe is formed by chemically etching under the AlGaAs. Breaking off this wing forms a smooth, cleaved mirror facet.

Section 3
Laser Process Development

When the Integrated Optoelectronic Transmitter Program began, the TJS lasers at Honeywell were being fabricated on 0.5 × 0.5 square inch substrates on which the epilayers had been grown by liquid phase epitaxy (LPE). The best pulsed lasing threshold was approximately 60 mA and no TJS laser had operated continuously (CW). It had been demonstrated that epilayers could be grown in wells and that small areas of the wafers could then be resurfaced, but there had been no lasers fabricated in wells, and there was no method for resurfacing large wafers for integration. There also was no method for producing the on-chip mirror.

The development of an integratable transverse junction stripe (TJS) laser involved tasks in three areas: 1) developing a process for reproducibly fabricating low-threshold, TJS lasers on planar (not in a well), semi-insulating substrates; 2) optimizing the processing required for the fabrication of a TJS laser-in-a-well; and 3) developing a high yield fabrication process to produce the laser mirror facet anywhere on a GaAs wafer. All processing had to be compatible with the fabrication of GaAs electronics.

By the end of the program, TJS lasers having pulsed threshold currents as low as 32 mA and CW thresholds as low as 38 mA had been fabricated on planar substrates. Lasers which had threshold currents as low as 38 mA had been produced in wells and a TJS laser-in-a-well with one undercut mirror operated CW with a 50 mA threshold.

In the following subsections, the development of the major processes for integratable TJS lasers are described in detail. These processes include the LPE crystal growth, the resurfacing of the substrate after crystal growth, the zinc diffusion and zinc drive.

CRYSTAL GROWTH

The requirements on the crystal growth for optoelectronic integration are to produce, in etched wells, heterostructures of controlled alloy composition, thickness, uniformity, and carrier concentration which are suitable for fabrication of high performance lasers. These layers must be grown on substrates large enough to permit IC processing. In addition, the growth must not degrade the semi-insulating nature of the substrate and the morphology must be good enough to permit resurfacing of the substrate.

There were three major areas of investigation for crystal growth during the course of this program: 1) growth conditions, 2) growth in wells and 3) growth on integration wafers. The work in these three areas is described below.

Growth Conditions

Prior to the start of this program, the maximum substrate size in our AlGaAs LPE furnace was 0.5 × 0.5 square inch. These wafers suffered from edge growth and pinholes which greatly reduced the amount of usable wafer area. In order to increase the amount of processable area as well as improve the quality of fine-line photolithography, a new LPE boat which could handle one square inch substrates was designed and fabricated. At approximately the same time, a load lock was placed on the furnace and the gas plumbing was improved to reduce the probability of leaks.

The semi-insulating substrate on which the TJS laser is fabricated can be degraded by exposing it to high temperatures (>800°C). For this reason, the temperature at which the LPE growth was performed was lowered from around 812°C to 750°C to protect the semi-insulating nature of the substrate. A typical time temperature cycle for one LPE run is shown in Figure 7. The layers are grown from melts which are capped and supercooled approximately 5°C.

A cleaved and stained cross section of a TJS structure grown by LPE is shown in Figure 8. The target layer thicknesses and doping concentrations are given in Table 1.

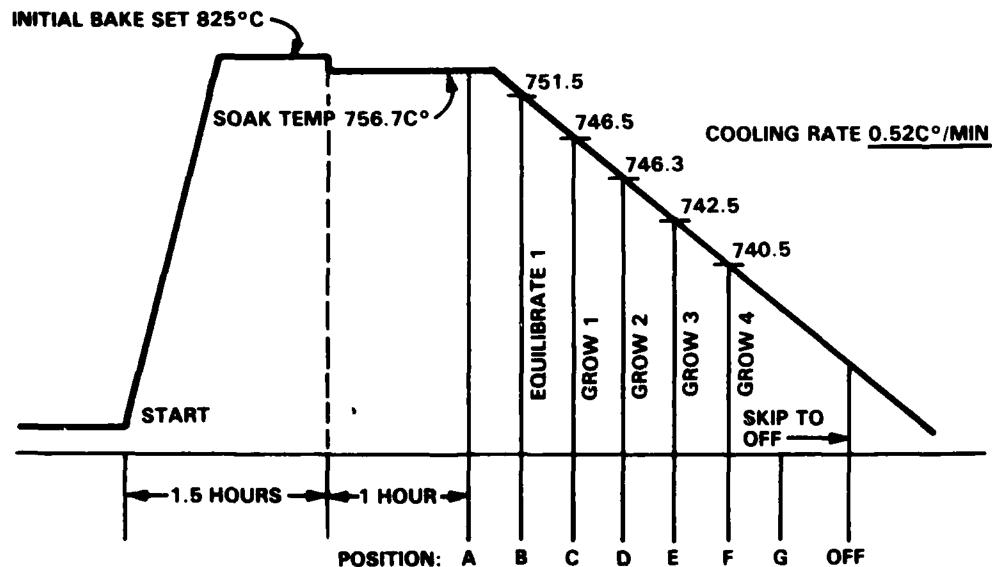


Figure 7. Typical Time-Temperature Growth Cycle of the Four-Layer TJS Laser. The structure is grown using ramp cooling and a precursor wafer for equilibrating the melts.

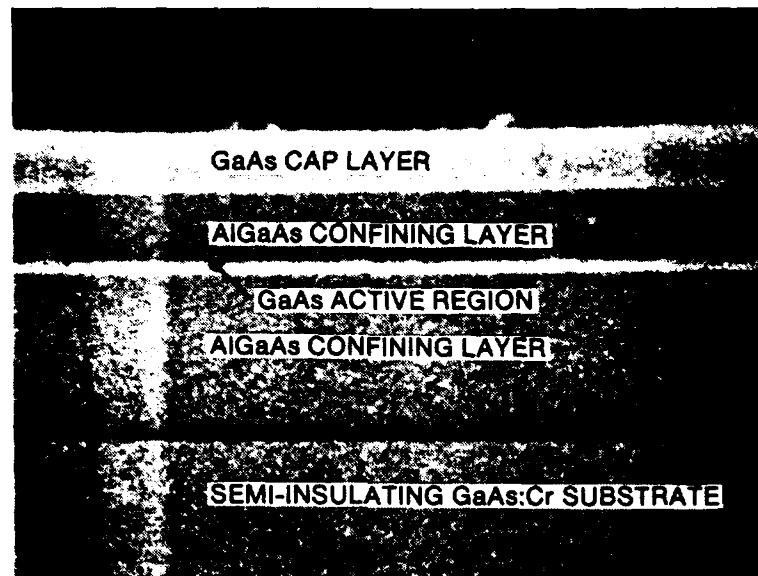


Figure 8. Stained Cross Section of a TJS Structure Grown by LPE. Magnification is 5900 ×.

Table 1. TJS Layers: Thickness and Doping

Layer #	Composition	Thickness (μm)	Doping (cm^{-3})
1	$Al_{0.4}Ga_{0.6}As$	3.0	n − 2 × 10^{16}
2	GaAs	0.25	n − 2.5 × 10^{18}
3	$Al_{0.4}Ga_{0.6}As$	1.5	n − 2 × 10^{16}
4	GaAs	1.0	n − 2 × 10^{18}

The thickness and doping level of the active region are the only critical values in the structure. The layer thickness and uniformity across the one square inch substrate is controlled using capped melts and a small amount of supercooling (5°C).

The doping level in the active region is important because of the effect it has on the efficiency of injecting electrons into the zinc diffused active region and on the formation of the optical waveguide. In a good TJS laser, steps in the real part of the index of refraction occur at the p-n junction and the p-p^{+} junction, forming an optical waveguide in the lateral direction. However, unless the electrons from the n-side of the junction are injected into the p-type region and recombine, it is not possible to take advantage of this guide. If the doping in the n-type active region is less than about 1.5 × 10^{18}cm^{-3}, then holes are injected from the heavily zinc doped p-region

into the n-side and anti-guiding occurs at the p-n junction (the light actually spreads out of the optical cavity). Lasing can only occur if the gain guiding produced by the injected carriers (the same guiding mechanism as in a proton bombarded stripe laser) overcomes the anti-guiding. This will occur at a current much higher than for a laser with refractive index guiding at the p-n junction.

At one point in our development of the TJS laser, the n-type doping levels in the active region were between $6 \times 10^{17} cm^{-3}$ and $1.2 \times 10^{18} cm^{-3}$. These lasers showed high threshold currents (80-100mA). Lasing on the n-side of the junction was confirmed by measuring the spectral output of the lasers fabricated from these wafers. The spectral peak of the light output was at approximately 8600Å rather than 8900Å, indicating that the lasing was originating in GaAs doped n-type. The doping in the active region was raised above $2.0 \times 10^{18} cm^{-3}$ and the threshold current dropped below 55 mA.

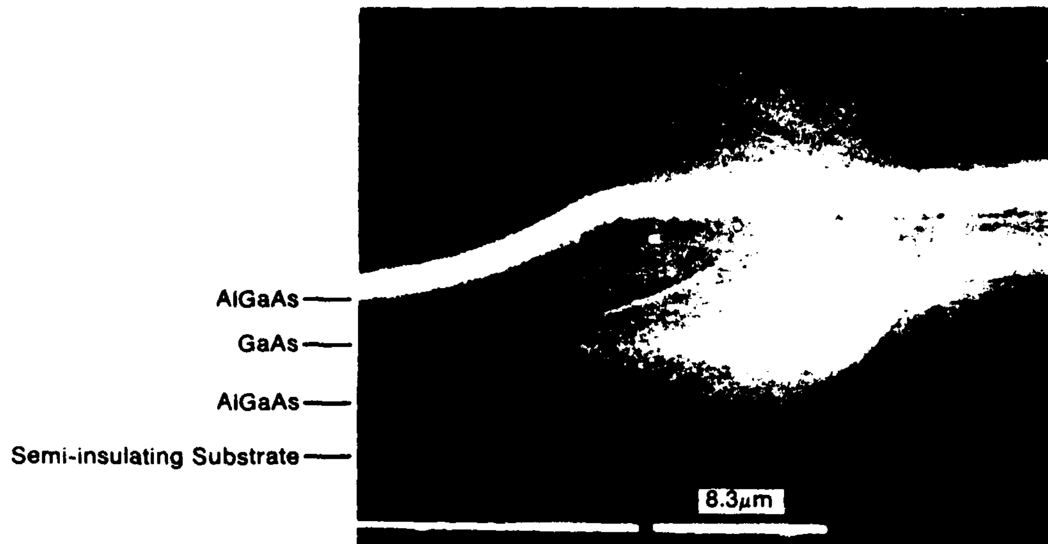
Epi-in-a-Well

To achieve the monolithic transmitter requires the ability to grow AlGaAs/GaAs heteroepitaxial structures. To obtain the planar structures for the transmitter design required that the epitaxial layers be grown in an etched groove and that the surface be made planar after growth.

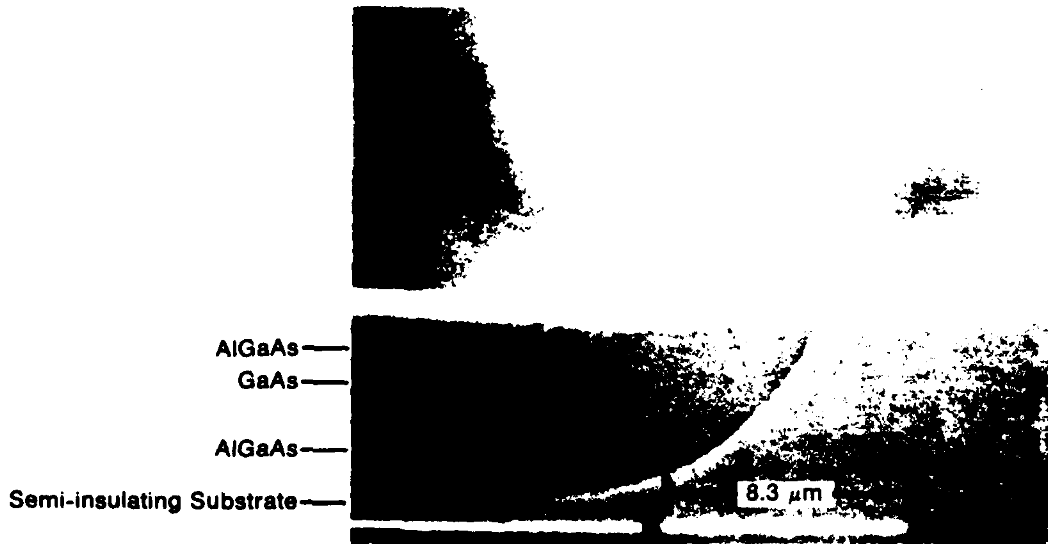
Prior to the start of this contract, Honeywell had grown LPE heterostructures of AlGaAs and GaAs in wide wells (400 micron) as shown in Figure 9a. We had also demonstrated the feasibility of the resurfacing process as shown in Figure 9b. Although it is quite easy to imagine techniques which would not require the resurfacing process after LPE, it is also very difficult to execute these ideas. For example, silicon nitride has been used previously as a growth mask in LPE. However, if only very small areas are open, the growth rate and morphology are extremely difficult to control. Also, if only a small area is masked, the growth near the edge of the mask is typically much faster than in adjacent regions resulting in nonuniform layers. Some of these ideas for the selective growth of LPE material were investigated under a different contract (Sandia Document No. 73-G277) but no major improvements were noted. For the contract for which this report is written, therefore, our approach was to shift the burden of integration away from the growth area to the device processing area.

The three major considerations for growth in a well are: 1) edge effects, 2) thickness control, and 3) effects on morphology. The size of the well must be large enough to accommodate the optoelectronic device and isolate the active region of the device from edge effects.

The ideal well-shape for integration would be a long rectangle, approximately 400μm wide and as long as the wafer. The initial work on LPE growth in wells was done on these long wells. The orientation of the wells was selected to be parallel (or perpendicular) to the (110) crystal planes so that the wafer could be cleaved parallel or perpendicular to the wells. The well depth was between 10 and 12μm.



a) As Grown Structure



b) After Polishing. Note the Planar Surface.

Figure 9. Cleaved and Stained Cross Section of a Double Heterostructure Grown in an Etched Well.

Using an anisotropic etch consisting of 1:8:1 solution of sulfuric acid:hydrogen peroxide:water, two different side wall profiles are possible, depending on the orientation of the etch stripes. Wafers have been prepared with each of these profiles and LPE was grown on each. Cleaved and stained cross-sections of each of these growths are shown in the photos of Figure 10. The dove-tail profile yields the preferred growth characteristics since the transition at the well edge is abrupt and there is a minimum of lateral edge growth. Also, the distinct edge characteristic of the dove-tail profile simplifies the subsequent photolithographic steps (alignment) during the resurfacing process.

After the epi-in-a-well was grown, the thicknesses of the layers inside the wells were found to be about 20 percent thinner than those outside the well. This was easily corrected with an adjustment in the growth cycle.

Growth for Integration

Two aspects of growth in wells had to be addressed for the integrated transmitter program. The first was that the epimaterial had to be confined to small areas on the wafer surface and, therefore, long rectangular wells could not be used. The second was that the crystal growth had a detrimental effect on the morphology of the semi-insulating substrate.

In order to produce a confined area of epimaterial, it would be necessary to expose different etch planes on the various sides of the well. For example, if a small rectangular well is etched in the substrate, two of the sides would have a V-groove profile and the other two would have a dove-tail profile.

To avoid the problems which were found when resurfacing over a V-groove, a special well shape was used. If the etch mask on the GaAs surface is aligned at 45° to the (110) planes, then the etch profile is almost vertical as shown by the cleaved cross section in Figure 11. A cleaved and stained cross-section of the crystal growth on these profiles is shown in Figure 12. There is more lateral edge growth than for the dove-tail profile, but less than for the V-groove profile. Therefore, this shape was found to be easier to resurface than the V-groove samples.

On the integration mask set, the wells were hexagonal in shape. Two opposite sides of the well were aligned in the (110) dove-tail direction. The other four sides of the well were aligned at 45° to these end lines.

Two problems with the materials growth were corrected during the integration portion of the problem. The first was a problem with the morphology of the semi-insulating GaAs surface after the epilayers had been removed by chemical resurfacing. The second was the number of pinholes in the top GaAs layer (cap layer).

On the initial wafers grown for integration runs, long rectangular pits were noticed in the surface of the substrate (Figure 13) after the first-grown AlGaAs layer was chemically removed. The shape of the pits was indicative of thermal damage.

a) The Etched Sidewalls of the Substrate formed a V-Groove

b) The Etched Sidewalls of the Substrate formed a Dove-tail.

Figure 10. Comparison of the Epitaxial Growth Characteristics at the Edge of the Etched Well. *Magnification* is 1800 ×.

Figure 11. Cleaved Cross Section of GaAs Etched at 45 degrees to the (110) Direction. The profile is nearly vertical. The photoresist etch mask is hanging over the etched region.

Figure 12. Cleaved and Stained Cross Section of LPE Growth in Wells Formed by Etching at 45 Degrees to the (110) Direction. The well profile is more vertical than for a V-groove profile.

Figure 13. Defects on Semi-Insulating Substrate Caused by Thermal Damage and Pinholes. Thermal damage leaves long straight streaks. Pinholes cause deeper spots.

The origin of the pits is as follows. Elevated temperatures prior to growth "damage" small sections on the substrate surface. When the substrate goes under the first melt (Al,Ga,As), meltback occurs at the selectively damaged spots on the wafer while growth occurs on the remainder of the surface. The localized meltback is short lived and the pits fill in as the first layer (AlGaAs) is grown. The pits are visible after resurfacing because a selective etch (see resurfacing section) removes the AlGaAs layer from the GaAs substrate revealing the "filled in" pits.

This problem was completely eliminated by modifying the growth apparatus so that a second GaAs wafer covered the substrate during the furnace heat-up prior to the growth of the first layer. Since the cover-chip was introduced, no thermal damage has been noted.

The second major materials problem which was corrected was that of pinholes which appeared in the GaAs cap layer. These pinholes did not affect the resurfacing but they did affect the zinc diffusion profile. Figure 14 shows a featureless resurfaced area in the center of the photo and a well region with high pinhole density on the left (200x). By increasing the super-cooling for growth of the cap layer, the problem was nearly eliminated.

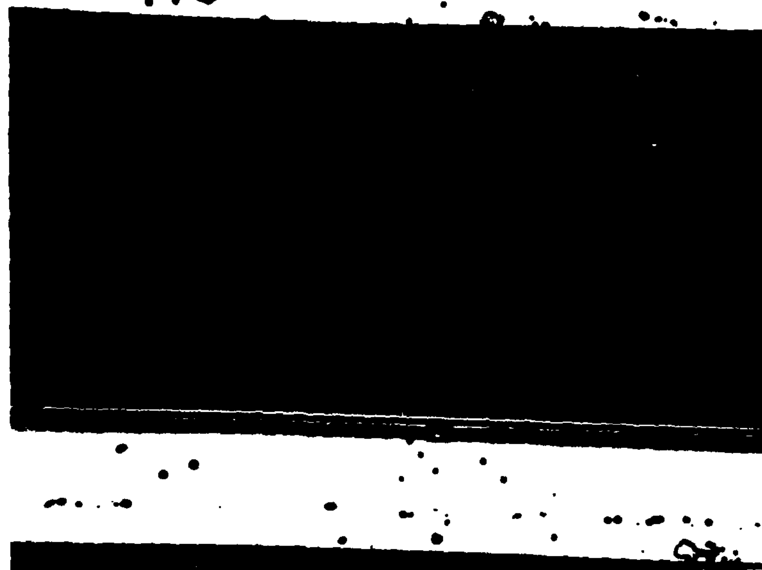


Figure 14. Microphotograph Illustrating the Effectiveness of the Resurfacing Process. The photo shows featureless resurfaced region between two wells with numerous pinholes in the epilayer.

RESURFACING

In order to use contact photolithography to successfully fabricate GaAs circuitry having 1 micron linewidth, the starting wafer must be extremely flat. Providing flat wafers which also contain the epimaterial required for laser fabrication is the major advantage of Honeywell's laser-in-a-well concept. The most critical processing step for the laser-in-a-well is the resurfacing of the wafer after the epilayers have been grown in the well. A method for planarizing the wafer has been developed which yields a high quality surface over a one inch wafer.

Resurfacing is the selective removal of the epitaxial layers grown outside the well, preparing the semi-insulating substrate for MESFET fabrication by selective ion implantation, while preserving the layers inside the well. The resurfaced area should be nearly coplanar with the surface of the epitaxial layers in the wells. The transition region between the epilayers in the well and the resurfaced area should be sufficiently smooth so as not to interfere with standard processing procedures such as metal interconnects.

The resurfacing is accomplished by masking the well regions with photoresist and then selectively etching off the epilayers outside the well one at a time using selective etches. The GaAs cap layer and active layer were removed by polishing the substrates on a soft pad with a 150:1 solution of H_2O_2:NH_4OH. The solution used to selectively remove the $Al_{0.4}Ga_{0.6}As$ layers was 113 g KI, 65g I_2, 100 ml H_2O.

The availability of a selective etch for both GaAs and AlGaAs permits the resurfacing layer by layer. This additional flexibility reduces the constraint on epi-layer uniformity. This is especially helpful since the layers grown by LPE are always thicker near the well edges. Hence the morphology of the resurfaced area is dependent only on the interface between the substrate and the first epitaxial layer rather than the overall morphology of all the grown layers. This was a major step in advancing the resurfacing technology.

The greatest problem faced during resurfacing was caused by pinholes in the epimaterial. This was because the pinhole would allow the GaAs selective etch to reach the substrate before the last AlGaAs layer had been removed. The result was that a pit would be etched in the substrate where ever the pinholes occured. It was found that, by controlling the amount of time allowed for any GaAs etch step, the depth of the pits could be minimized. Then, a final polish of the exposed substrate using the H_2O_2:NH_4OH solution was used to completely smooth out the surface. This is the resurfacing sequence which was used on the successful integration run.

ZINC DIFFUSION AND DRIVE

As stated in the Zinc Diffusion subsection of the previous section, the process of diffusing the zinc dopant into the AlGaAs heterostructure is the most important step in the fabrication of the TJS laser. The zinc diffusion and drive consists of four major steps:

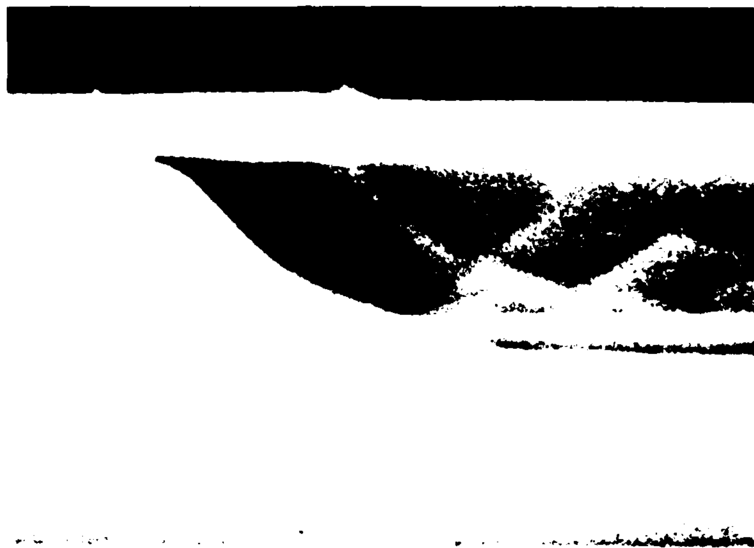
- Deposition and patterning of the zinc diffusion mask.
- Closed-ampoule zinc diffusion.
- Application of anneal cap.
- High temperature zinc drive.

In this subsection the development of these steps is described.

Silicon nitride is known to be a good mask against zinc diffusion. During this contract, zinc masks formed by the sputter deposition of silicon nitride were compared to those formed by pyrolitic CVD (chemical vapor deposited) nitride.

We found numerous problems with the sputter deposited nitride. At first, there was an adhesion problem which caused the nitride to peel at the diffusion temperature (700°C). Once the adhesion problem was solved, however, we still found it impossible to obtain a good zinc diffusion with the sputtered nitride. At 700°C, the stress at the nitride/GaAs interface caused by the thermal mismatch of these two materials caused an enhanced diffusion along the interface.

In comparison, there is no detectable interface diffusion when pyrolitic CVD nitride is used because it is deposited at 700°C. Therefore there is almost no stress during the diffusion. Figure 15a and 15b are cleaved and strained cross-sections of zinc diffusions into TJS lasers. In 15a, sputtered nitride was used and the enhanced side diffusion is obvious. In 15b, CVD nitride was used, resulting in a well behaved diffusion front.



a) Enhanced surface diffusion caused by the stress of the Sputtered Silicon Nitride Mask.

b) Well-behaved diffusion with a CVD Silicon Nitride Mask.

Figure 15. Cleaved and Stained Cross Sections of the Zinc Diffusion Profile.

The CVD nitride was tested for its effectiveness in preventing the zinc from converting the underlying semi-insulating GaAs on resurfaced wafers. It was found that at least 1100Å of nitride was required to protect the surface for a 90 minute zinc diffusion at 700°C. For the integration runs, 2000Å of nitride was specified.

The zinc diffusions were performed in closed quartz ampoules. During the development of the TJS laser, the ampoules were 7.5 cm long and had a 1.5 cm ID. The ampoules were cleaned in a solution of 1 part HF:1 part H_3NOH: 5 parts H_2O, rinsed in deionized water and vacuum baked at 800°C.

$ZnAs_2$ was used as a zinc source. Approximately 9 mg of $ZnAs_2$ was loaded into the ampoule along with the TJS sample. The ampoules were pumped down to 1-2 x 10^{-6} Torr and sealed off.

During the initial stages of the program the diffusion was performed in a small clam-shell furnace. The flat zone in this furnace was measured to be only 4 cm. The nonuniformity in temperature across the ampoule led to surface damage on the sample, irregular diffusion profiles, and Zn deposits on the GaAs surface. Figure 16 is a cleaved cross-section of a zinc-damaged wafer. The result was a low yield of laser and high lasing thresholds (80-100 mA).

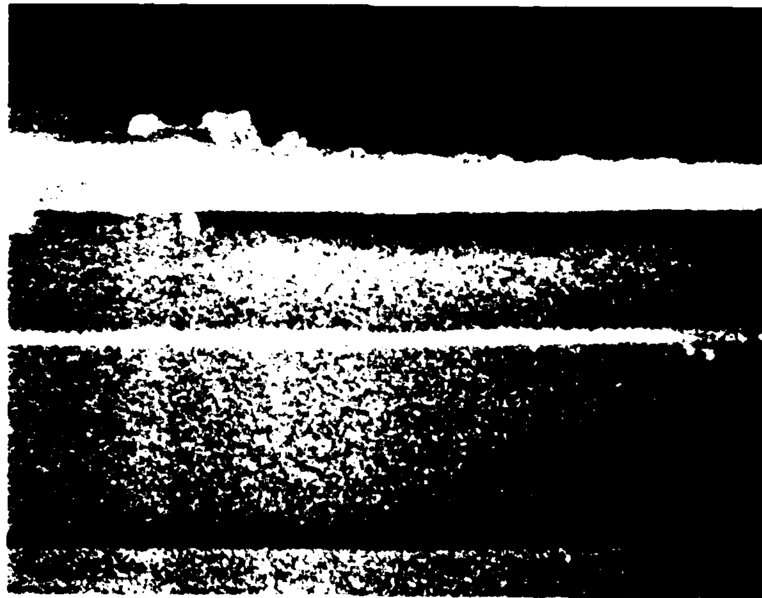


Figure 16. Cleaved Cross Section of TJS Structure Damaged during Zinc Diffusion. Pitting of the GaAs cap layer occured during the diffusion. Deposits of Zinc and Arsenic occurred during the cool-down.

To correct this problem a controlled 3-zone furnace was used which had a flat zone (± 0.5°C) of 25 cm. The furnace was controlled during a diffusion to achieve even heating of the ampoule and prevent temperature overshoot and cooling which would result in sample surface damage.

A study was carried out on the effect on threshold caused by the diffusion temperature. Diffusions were performed at 650°C and 700°C. The diffusion coefficients for GaAs and $Al_{0.4}Ga_{0.6}As$ (D_{GaAs} and D_{AlGaAs}) were measured and are given in Table 2 as a function of temperature.

Table 2. Zinc Diffusion Coefficients ($\mu m/\sqrt{hr}$)

	650°C	700°C
GaAs	0.9	1.8
$Al_{0.4}Ga_{0.6}As$	2.7	5.7

The duration of a diffusion was determined by the thickness of the GaAs cap layer (t_{GaAs}) and the top AlGaAs confining layer (t_{AlGaAs}). It was found to be advantageous to have the diffusion stop 0.3 μm above the active layer. Therefore the diffusion time was

$$T(\min) = \left(\frac{t_{GaAs}}{D_{GaAs}} + \frac{t_{AlGaAs} - 0.3}{D_{AlGaAs}} \right)^2 \cdot 60$$

This formula was found to give consistently good results as shown by the diffusion in Figure 17.

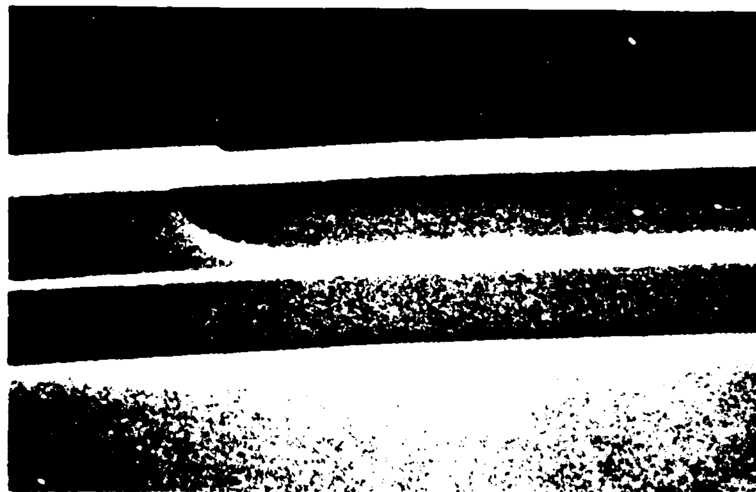


Figure 17. Cleaved Cross Section of Zinc Diffusion into TJS Structure. The diffusion was stopped 0.3μm above the active layer.

The studies of threshold current versus diffusion temperature showed no clear cut difference between 650°C and 700°C. Therefore, the 700°C diffusion was chosen because 650°C diffusion takes about four times longer.

After the diffusion, the zinc mask is stripped off and a new CVD nitride is deposited. This nitride protects the wafer surface during the high temperature drive step.

The drive step diffuses the zinc through the layers and into the substrate. The diffusion properties of zinc separates the p-n junction and p-p+ junction by a controlled amount to form the optical cavity in the active layer. The two junctions are highlighted in the stained cross-section of Figure 18. Drives were performed at 800°C, 850°C, 870°C, and 900°C for between one and three hours. It was found that two hours at 900°C gave the lowest lasing threshold.

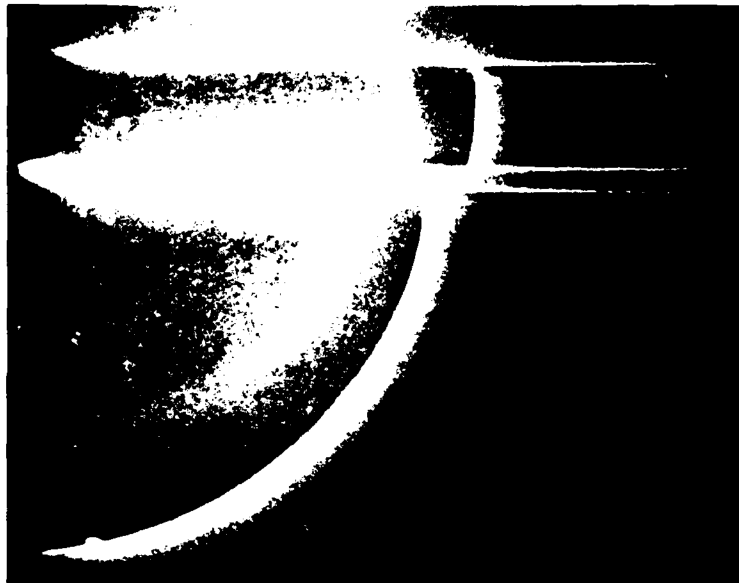


Figure 18. Cleaved and Stained Cross Section of Zinc Diffusion in a TJS Structure after the Drive Step. The two diffusion fronts indicate the position of the p-n junction (on the right) and the p-p$^+$ junction (on the left).

There was a concern, however, about the effect of a two hour, 900°C drive on the quality of the exposed semi-insulating substrate for integration wafers. It was found that the CVD nitride cap was an excellent protective layer and little or no degradation of the surface occured.

The two hour, 900°C anneal produced lasers with threshold current between 32 and 40 mA. After this was demonstrated no further work was done to achieve lower thresholds. The integration wafers were diffused at 700°C and the drive was two hours at 900°C.

UNDERCUT MIRROR PROCESS

The Undercut Mirror Process was developed at Honeywell as a method for obtaining cleaved laser mirrors in the middle of a GaAs wafer. This process is similar to the microcleave mirror process reported by the California Institute of Technology[11] and Fujitsu Laboratories.[12]

The Undercut Mirror Process was first demonstrated a Honeywell using our well established proton bombardment-defined stripe (PBS) lasers. These lasers have a 6-micron-stripe width (2-3 times wider than TJS).

The essential features of the Undercut Mirror Process on PBS lasers are illustrated by the photographs in Figures 19, 20, and 21. After the laser stripes have been defined by proton bombardment and the metal contact applied to the top surface of the wafer, the wafer is coated with photoresist and small "dove-tails" are defined at the ends of the stripes. A solution of sulfuric acid:hydrogen peroxide:water is used to etch through the exposed material down to the GaAs substrate. Figure 19 is a top view of the wafer after the etch step. The laser stripes running horizontally are easily seen as are the dove-tails. For this wafer, a mask was used which had two different dove-tail shapes. The light region in the photo is the gold contact and the darker region is the exposed GaAs epilayers. It should be noted that the action of the etch and the orientation of the wafer produces a notch at the outer edge of the wing. This is very important in protecting the active layer during the next etch step.

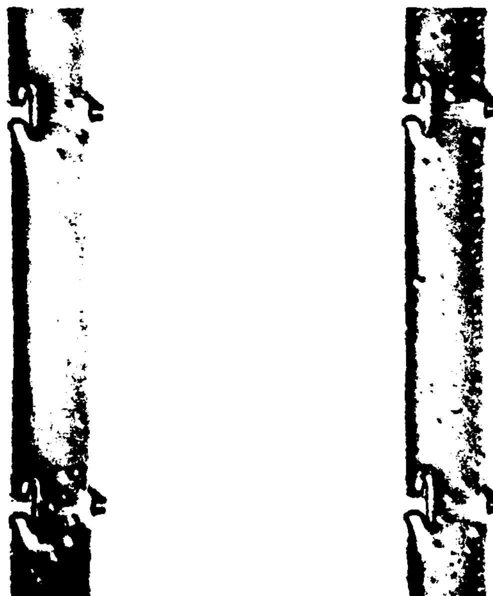


Figure 19. Microphotograph of Dove-tails Formed at the Ends of Proton-Bombarded Stripe Lasers by Etching the Epitaxial Layers. Two differently shaped dove-tails were used on this mask. (1cm = 50μm).

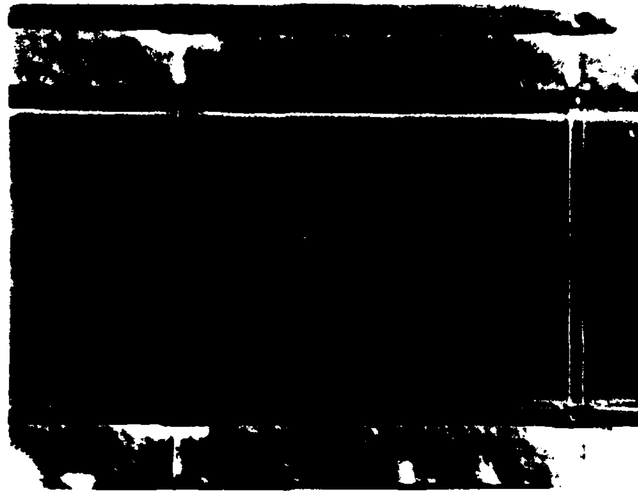


Figure 20. Photomicrograph of Dove-tails Covered by Photoresist during Undercut Mirror Process. Undercutting is monitored by observing the substrate through the resist.

Figure 21. Scanning Electron Microscope Photograph showing an Undercut Dove-tail of Epimaterial on a Proton-Bombarded Stripe Laser. The edges of the laser stripe can be seen at the top of the photo. (1cm = 6μm)

A thick photoresist is applied to the sample and stripes are opened in the resist which uncover the exposed substrate in front of the etched dove-tail, but the dove-tails remain covered as shown in Figure 20. Resist also remains in the notch at the outer edge of each dove-tail. This resist guarantees that the GaAs active layer will not be etched out between the two AlGaAs layers during the undercut process.

The wafer is then placed in a solution which selectively etches GaAs but not AlGaAs. The etch forms a long trough which undercuts the wings of epimaterial. The progress of the undercutting is monitored by watching the sideways etching of the GaAs substrate from the top through the photoresist. When the undercutting has progressed back to the narrowest point in the dove-tail, the etching is stopped and the resist is removed. Figure 21 is a front-on view of one of the undercut dove-tails. At this point, the only remaining step is to break off the undercut epimaterial, forming a cleaved surface. In the original PBS laser work, the epilayers were snapped off using ultrasonic vibrations. A photograph of a cleaved facet is shown in Figure 22.

Figure 22. Scanning Electron Microscope Photograph of Undercut Mirror after the Dove-tail was Cleaved Off. The laser epilayers are obvious on the flat mirror.

A power-current curve for a PBS laser with one undercut mirror and one cleaved mirror is shown in Figure 23. This laser had a threshold current of approximately 90 mA. A comparable laser with two cleaved mirrors had an 80 mA threshold. The slight difference is believed to be due either to small irregularities in the cleaved surface across the 6 micron active region, or to excess scattering loss at the mirror because the cleaved surface is only 10 μm wide while the lateral optical field of a PBS laser with 6 μm stripes would be 12-15 μm wide.

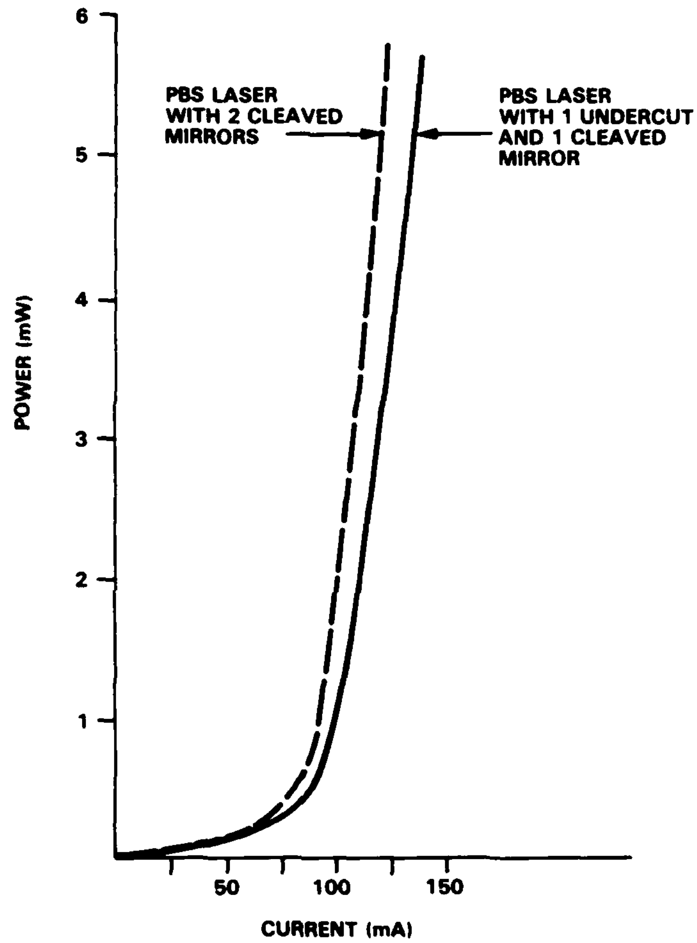


Figure 23. Comparison of the Power versus Current Photo of Proton-Bombarded Stripe (PBS) Lasers with and without an Undercut Mirror

There were two major concerns with the use of ultrasonic vibration to break off the epilayers. The first was a question of how this process would affect the surrounding electronic circuits on an integrated chip. The second was the yield of the process.

This led to a comparison of ultrasonic vibration to another method for removing the dove-tails. It was found that ultrasonic vibration was extremely difficult to control and produced a relatively poor yield. Typically, the wings would not break off flush with the edge of the trough but, instead, part of the wing was left still sticking out from the laser stripe. This would not be suitable for a laser mirror.

The use of a thick polymer film (Durepoly) was found to be the answer to the problem. The wafer was coated with the polymer suspended in a solvent. After the solvent dries, a polymer film coats the wafer and encases the dove-tails. The film is then peeled off, breaking the dove-tails off at the same time. This method produces suitable cleaves nearly 100 percent of the time. A view of one undercut and cleaved mirror is shown in Figure 22.

The only drawback to this method was that the film would sometimes remove the metal contacts if they had poor adhesion to the GaAs or if there were cracks in the metal which allowed the polymer to seep in underneath. However, we felt these problems could be avoided in the integrated structure. Therefore, this was the technique which was chosen for the integration process.

Due to structural dissimilarities between the TJS laser and the PBS laser, some modification in the previous fabrication procedure was required. Because the TJS laser is fabricated using a selective zinc diffusion to form the laser stripe, the solution which etches through the epitaxial layers is required to remove n-type and p-type material at the same rate. The solution is also required to be fairly anisotropic (etching down into the sample much faster than etching sideways). Most etching solutions do not meet these criteria and do not produce acceptable results. After an etch study using different solutions based on sulfuric acid, hydrochloric acid, or ammonium hydroxide, the solution 5 parts sulfuric acid:1 part hydrogen perioxide:4 parts water was found to produce excellent results. Discrete TJS lasers with undercut mirrors were fabricated using the techniques described above. The power-current curve of one of these lasers is in the following section. This laser was delivered to NRL as part of this contract.

Section 4
TJS Laser Evaluation

In the previous section, the processes involved in fabricating integratable TJS lasers were described. In this section, the results which were obtained using those processes are presented.

ELECTRICAL CHARACTERISTICS

The TJS laser is a diode in which the main current-carrying junction is formed by a zinc diffusion into heavily doped GaAs. A typical current versus voltage trace of a low-threshold TJS laser is shown in Figure 24. The turn-on voltage is approximately 1.3 volts and the series resistance is about 8 ohms. For this laser, when the current though the device was at lasing threshold (40 mA), the voltage across the device was 1.85 volts.

In reverse bias, the low threshold lasers breakdown sharply at 8-10 volts. Lasers having a soft breakdown at lower voltages usually had higher thresholds. This is probably indicative of a poor zinc diffusion or a pinhole near the zinc diffused stripe.

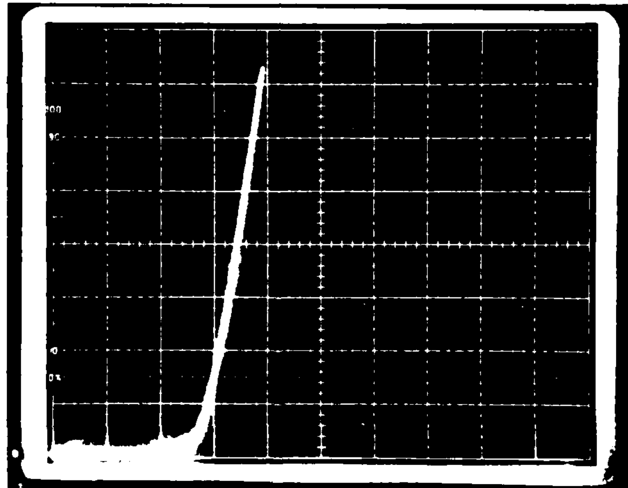


Figure 24. Current versus Voltage Curve for a TJS Laser Diode. The vertical scale is 5mA/division and the horizontal, 0.5V/division.

TJS LASER THRESHOLD CURRENTS

The development of the integratable TJS laser involved three tasks: 1) Determine a process for obtaining low threshold lasers on planar substrates, 2) Optimize the process for the laser-in-a-well, and 3) Produce integratable laser-in-a-well with an on-chip mirror. The results of these tasks are presented in this subsection.

Prior to the start of this contract, the threshold currents of typical TJS lasers fabricated at Honeywell was in the range of 80-100 mA. Following an extensive effort to improve the zinc diffusion process, the thresholds were lowered to between 50 and 55 mA for lasers with 2 cleaved mirrors. Figure 25 shows the power versus current for a laser which is 280 microns long. The threshold is approximately 51 mA. This im-

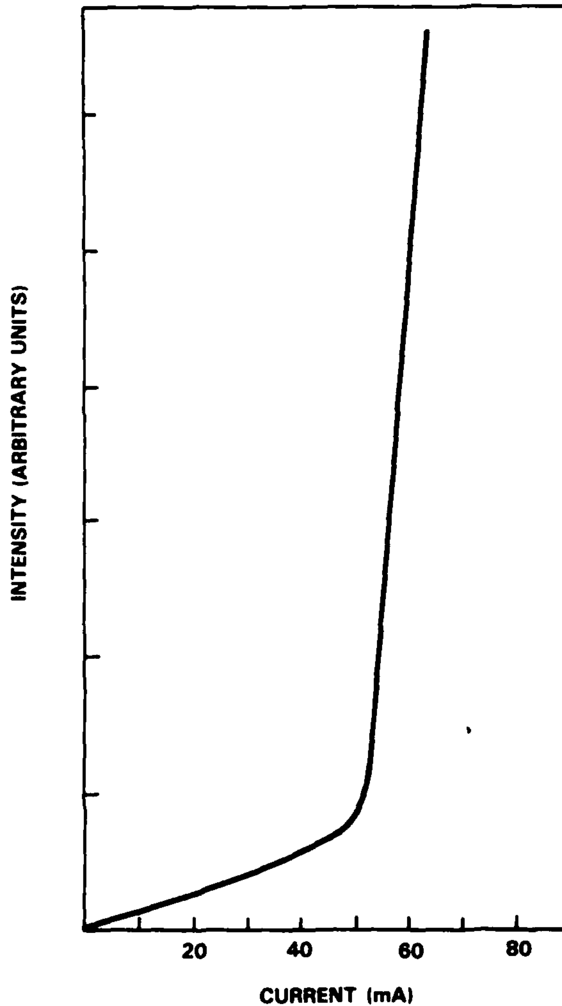


Figure 25. Power versus Current Curve for TJS Laser after 850°C Drive Step

provement was due to the use of a new furnace for the zinc diffusion and to the increase in the doping level in the active region. The laser had a 700°C Zn diffusion and a two hour 850°C drive.

The new furnace provides far more uniformity and control during the diffusion than was previously available. With the added control over the diffusion, a study of the effects of the anneal step was undertaken. Table 3 is a chart of typical threshold currents for lasers fabricated from the same wafer with the same Zn diffusion but different drive cycles.

Table 3. Drive/Time Temperature Effect on Threshold Current (mA)

Drive Time	Drive Temp (°C)		
	850	870	900
1 hr	55-60	—	40-45
2 hr	45-50	42-45	35-40
3 hr	50-55	45-50	—

In general, the 900°C drive gave the lowest threshold currents.

This wafer also had over 80% yield of lasers. In Figure 26 are the power-vs-current plots of four lasers chosen randomly from the 900°C, two hour sample. The pulsed current thresholds ranged from 32 mA to 38 mA. When mounted on a heatsink, the CW threshold currents were 38-40 mA.

Two of the lasers from the two hour, 900°C sample were mounted on heat sinks and their optical properties were measured in a spectrometer. Figure 27 is the spectrum of a TJS laser with a 38 mA threshold that is driven at 42 mA. The laser output is a single mode centered at 8914 Å Figure 28 is the spectrum of a 41 mA threshold laser at 48 mA. Its main peak is at 8905 Å but there is a small peak at 8901 Å This demonstrates that the TJS lasers are not yet optimized but they were still useful for the integrated optoelectronic transmitter. Both of these lasers were delivered to NRL.

LASER-IN-A-WELL

The initial work on fabricating lasers in wells was performed in wells that were 400 μm wide and ran the full length of the wafer. The first laser-in-a-well had an 80 mA threshold. However, after the improvements in the process of the planar lasers were included in the process of the laser-in-a-well, excellent lasers were fabricated. Figure 29 shows a comparison of a TJS laser fabricated on a planar semi-insulating

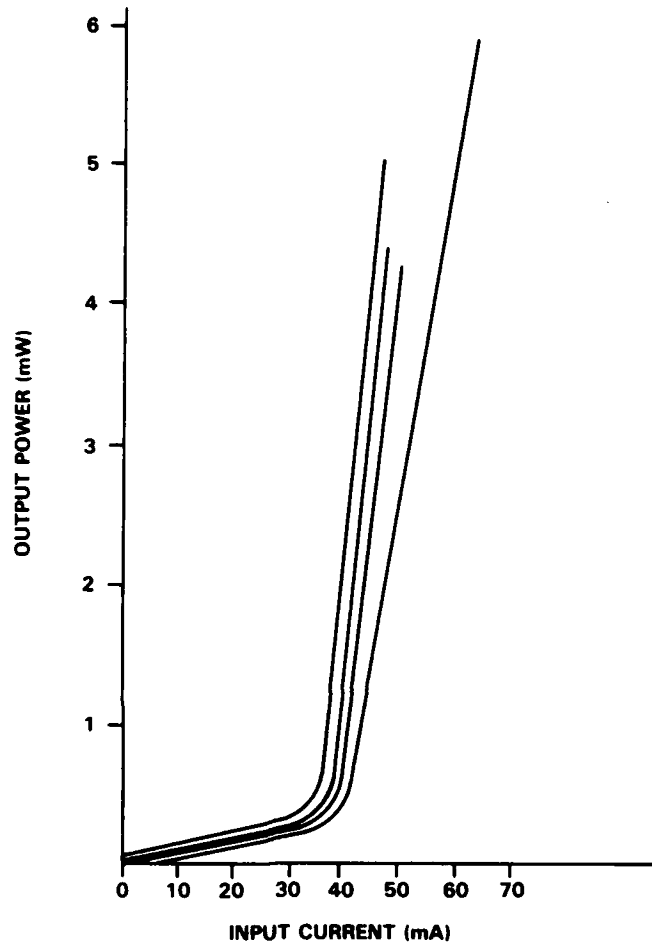


Figure 26. Output Power versus Input Current for Four Low Threshold Current TJS Lasers

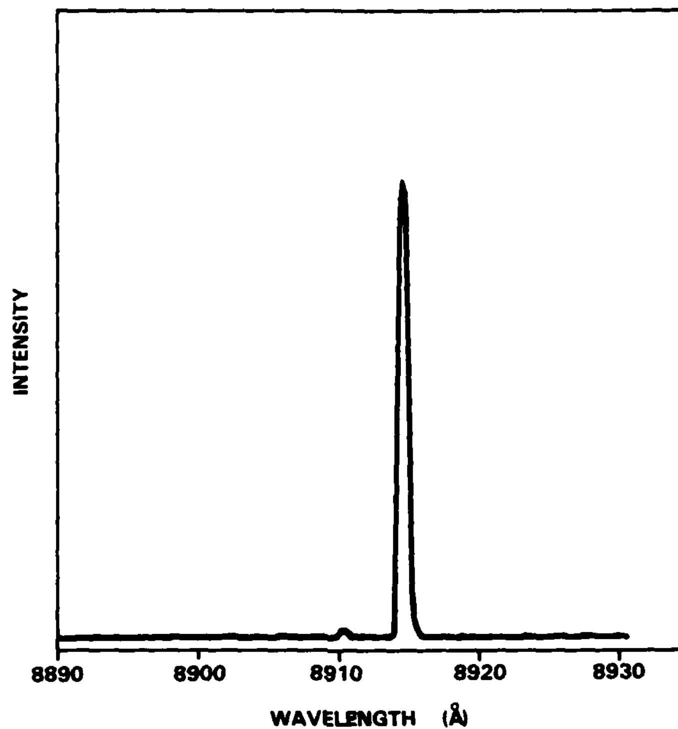


Figure 27. ***Spectrum of a Single Mode TJS Laser.*** The laser had a 38mA threshold and was biased at 42mA.

substrate with one fabricated in a well. Both lasers received the same processing steps. The lasers have nearly identical differential quantum efficiencies (slopes). The threshold currents are nearly identical with the small difference most probably due to a slight variation in the active layer thickness.

LASER-IN-A-WELL WITH UNDERCUT MIRROR

The Undercut Mirror Process has been used to fabricate fully integratable TJS lasers. Figure 30 is the CW threshold current for one of these lasers. Its threshold current is about 52 mA. Its optical spectrum shows that this laser is not single mode. This may have been due to non-uniformity of the epitaxial layers caused by a large number of pinholes in this wafer. This laser was delivered to NRL.

DYNAMIC PROPERTIES

One of the main reasons that Honeywell chose to develop the TJS laser for integration was that it has extremely good high-speed properties. Some of the low threshold lasers have been tested with very narrow electrical pulses. Figure 31 shows a sampling scope trace of a TJS laser fabricated at Honeywell (I_{th} = 40 mA) biased above

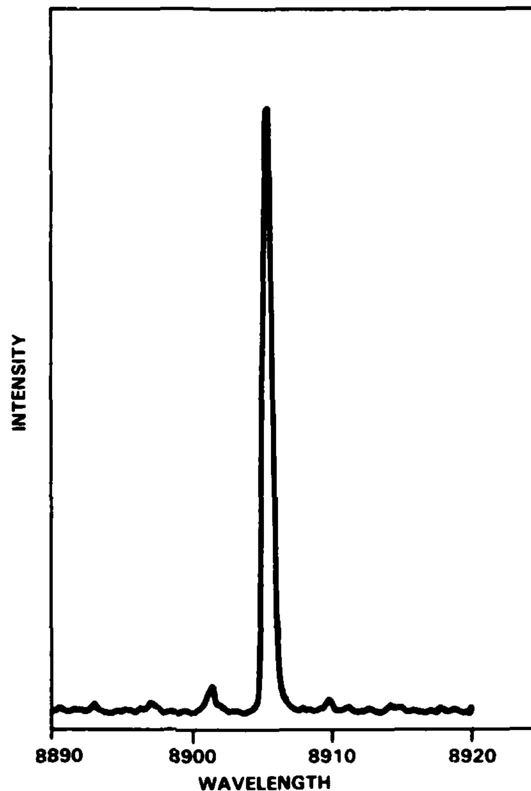


Figure 28. Emission Spectrum of a TJS Laser Showing Extra Side Modes. The laser had a 42mA threshold and was biased at 48mA.

threshold and driven with an additional 200-psec wide pulse. The rise and fall times of the optical detector are about 100 psec each. The resulting pulse as detected has a 300-psec FWHM, which indicates that the rise and fall time of the laser is faster than 100 ps, making 3 GHz modulation definitely viable.

These lasers were also tested with a digital input. As described in the next section, one of these discrete lasers was driven at 1 Gb/s by the Mux/driver IC.

In summary, we demonstrated planar TJS lasers with CW threshold as low as 38 mA and integratable lasers with CW thresholds as low as 52 mA. The process is, however, far from optimized and is not yet completely reproducible. It was, however, good enough to demonstrate an integrated optoelectronic transmitter which was the prime objective of the program.

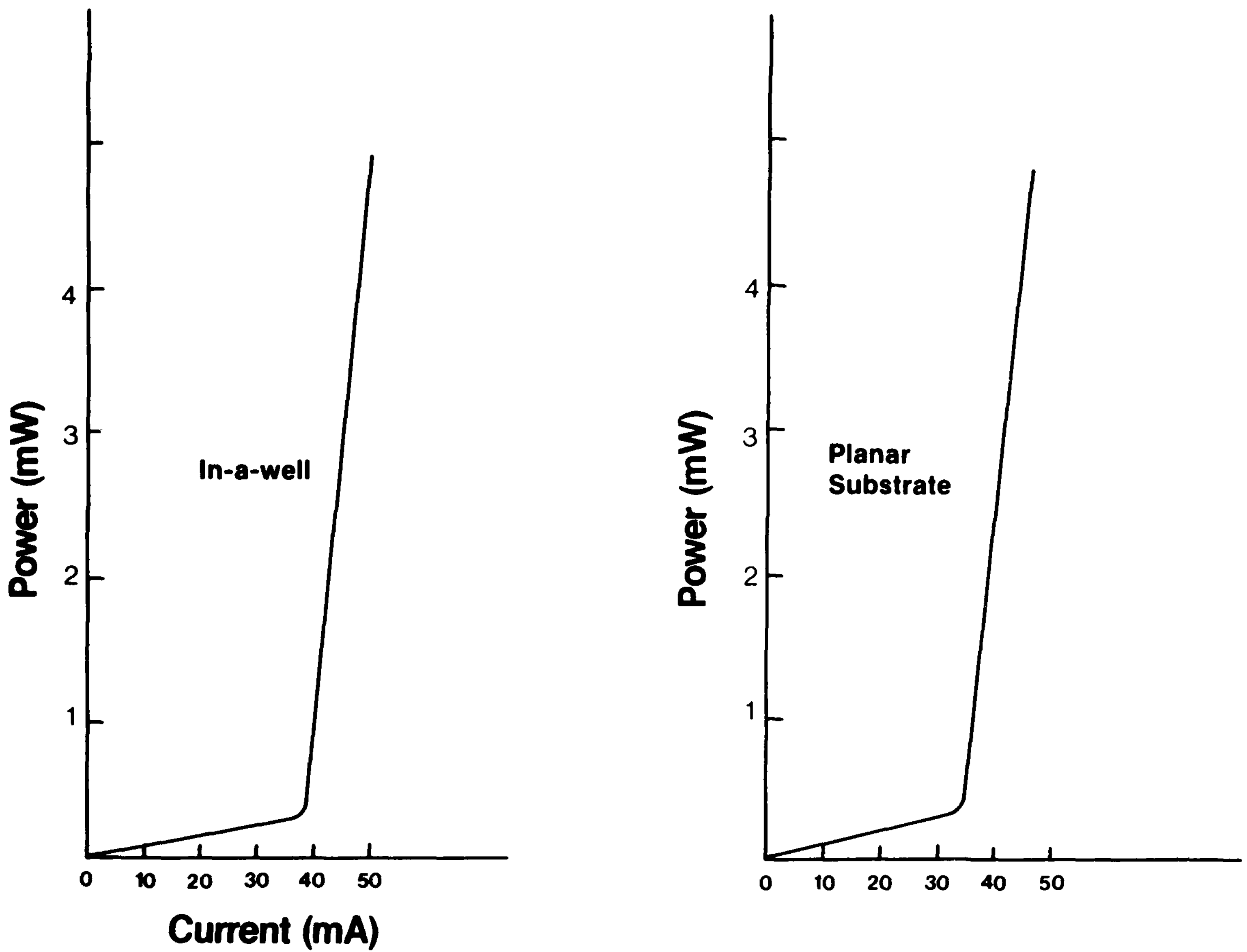


Figure 29. Comparison of Power versus Current for TJS Laser-in-a-Well and Planar TJS Laser

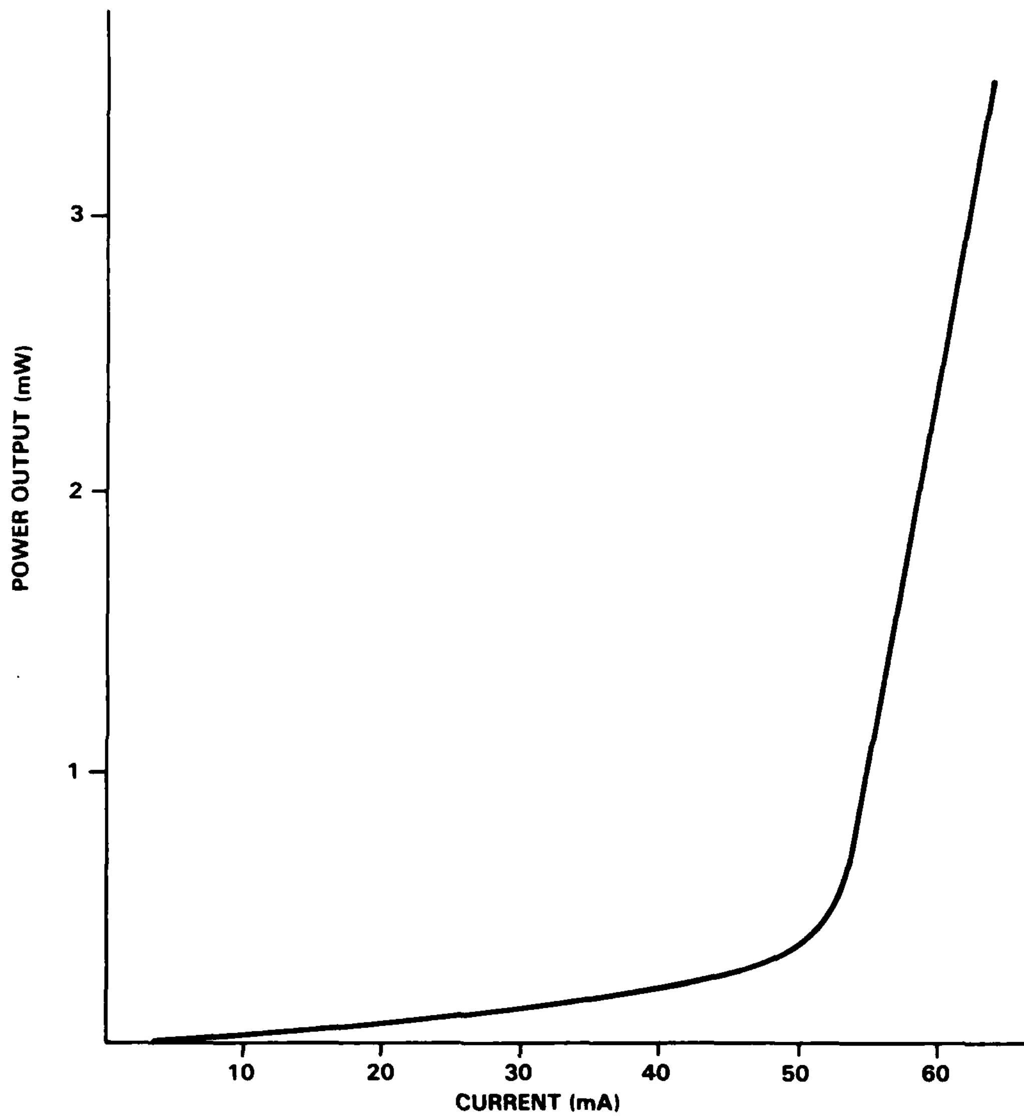


Figure 30. Power versus Current Plot for a TJS Laser-in-a-Well with One Undercut Mirror

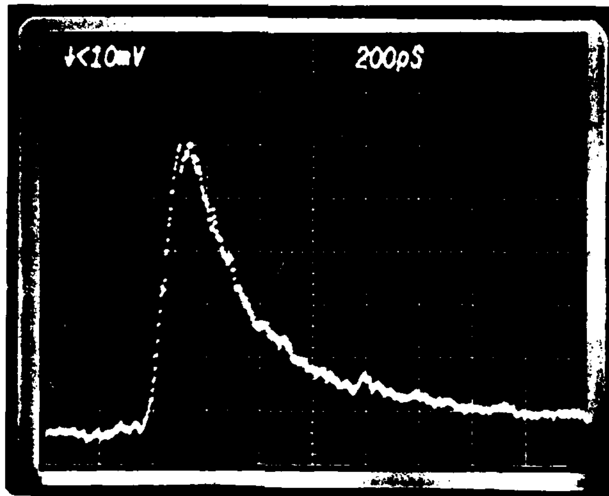


Figure 31. Detected Optical Response of a Biased TJS Laser to a 200-psec Electrical Pulse. The 300 psec FWHM indicates 3 Gb/s is possible.

Section 5
GaAs Electronics

The development of the GaAs circuit for the laser/multiplexer IC was a Honeywell funded task. Within this section is a description of the 4:1 multiplexer (Mux) including a unique buffered NOR gate and the power driver FETs. The operating characteristics are then presented.

Prior to the start of this contract, a mask set for the fabrication of GaAs circuits using SDFL (Schottky Diode FET logic) gates was designed. This test set contained a seven-stage ring oscillator (7 gates for fan-outs of 1, 14 gates for fan-outs of 2), a divide-by-4 counter (18 gates) and a 4:1 multiplexer (28 gates). The divide-by-4 counters operated at input rates well over 1 GHz and gate delays of 107 psec were obtained in the ring oscillators with fan-outs of 1. The multiplexer, however, could be operated at only a few MHz. These results indicated that much of the gate design and processing was applicable to circuits which operate above 1 Gb/s. The Mux design shown in Figure 32, however, was found to be faulty after considerable modeling using SPICE circuit simulation.

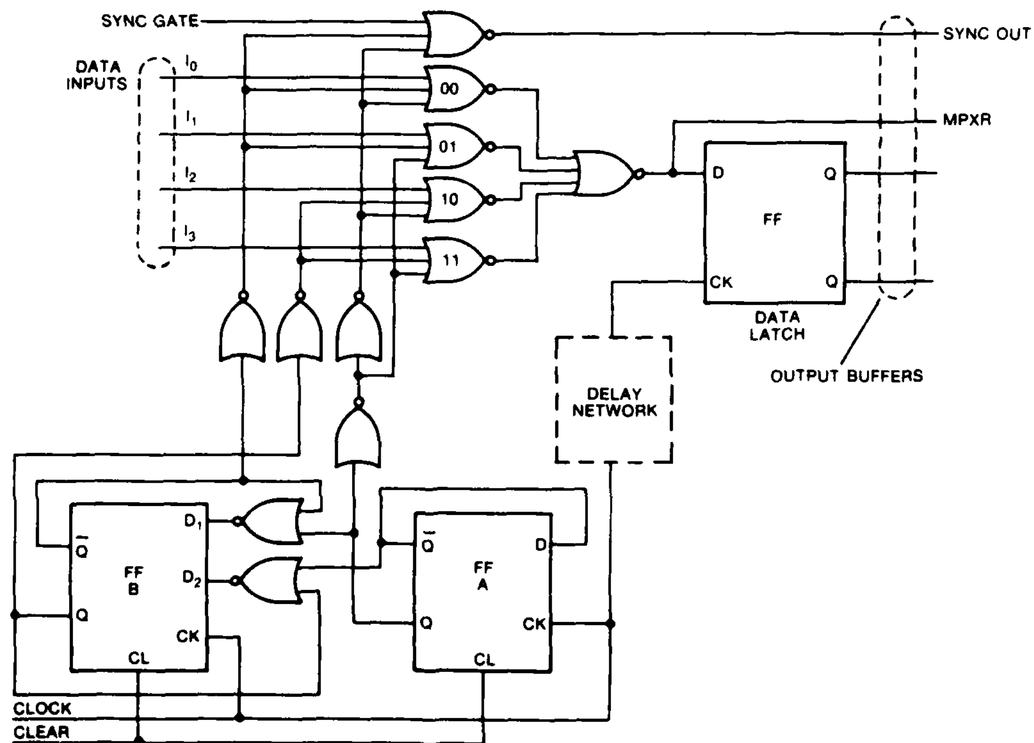


Figure 32. Logic Diagram of the Original 4:1 Multiplexer

A new multiplexer was designed which included a unique NOR gate as described below. SPICE simulation predicted that the new circuits would operate above 1.5 Gb/s.

BUFFERED NOR GATE

The gate delay for a fan-out of one with the SDFL design used in the old multiplexer was 107 psec. However, a fan-out of 2 produced approximately a 170 psec delay and the delay for a fan-out of 3 was estimated to be well over 200 psec. The original Mux design contained fan-outs of 3 and even higher in the output buffers. The result was a circuit which operated correctly only at low data rates. Large fan-outs in SDFL circuits also cause the gate input-voltage error margin to be greatly reduced.

To overcome these problems, we modified the standard unbuffered SDFL gate (Figure 33) into a buffered SDFL gate with a push-pull output driver (Figure 34). This gate structure contains a source follower plus a switched pull down FET. The source follower has excellent current supply capability and is relatively insensitive to loading as has been demonstrated in BFL (buffered FET logic) gates. Because the logic is performed by diodes and the level shifting occurs at the input to the gate, a source follower alone is not enough for SDFL. The pull down current available for a given gate is dependent on the input states of the gates loading it, but the parasitic capacitance is not. The switched pull down is added to eliminate this problem. Since it is switched off when the output is high, it does not add more loading or draw power. When turned on it helps to pull down the output node and interconnect lines independent of the input states of the loading gates.

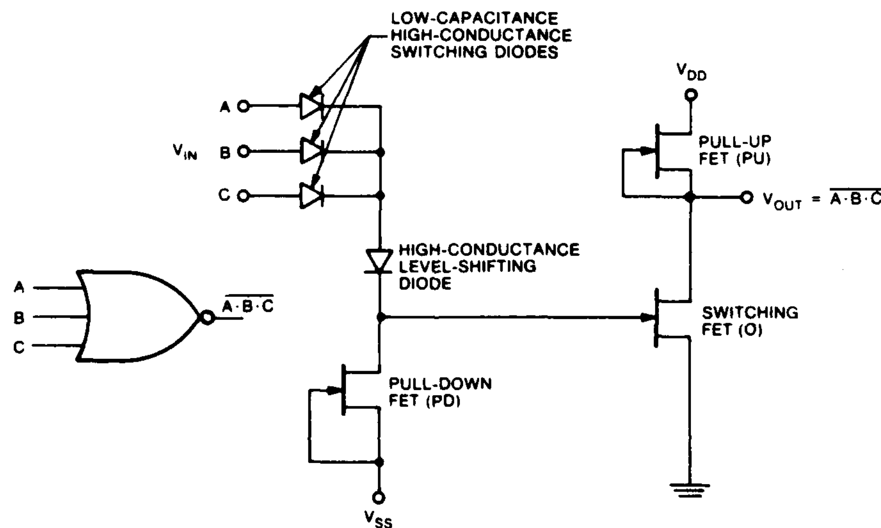


Figure 33. Unbuffered SDFL NOR Gate Schematic

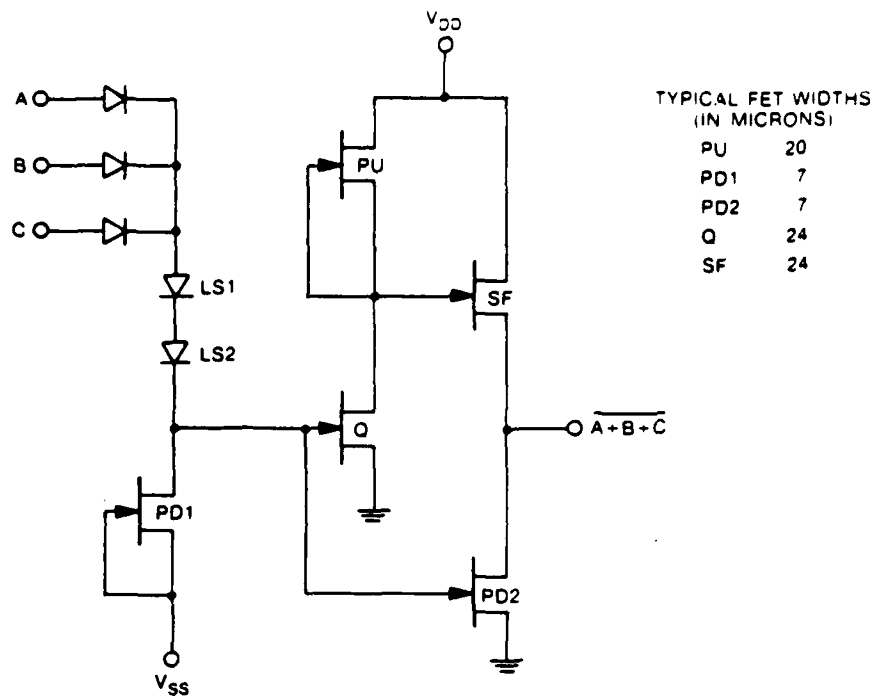


Figure 34. Circuit Diagram for Unique Buffered SDFL NOR Gate with Push-Pull Output

This gate has a gate delay which is nearly independent of fan-out from 1 to 3. Simulations of the new gates predicts a 30 percent increase in speed in cases of heavy capacitive loading.

This push-pull output integrates well into a circuit with unbuffered SDFL. Figure 35 shows a layout for a buffered SDFL gate. It can be seen that the two additional FETs on the right fit easily into the structure. This gate has high gain and an excellent noise margin. The measured transfer curve worst case noise has a margin of 1.0V. A large noise margin is extremely important in obtaining reproducibly high yield on substrates which have gone through extra heat steps and processing for optoelectronic integration.

MULTIPLEXER CIRCUIT DESCRIPTION

The logic diagram of the 4:1 multiplexer used for integration with the TJS laser is shown in Figure 36. The Mux was fabricated using a combination of buffered and unbuffered SDFL gates. There are a total of 36 NOR gates containing about 140 MESFETs. The "B" denotes those gates which are buffered because of larger fanouts or loading. When buffered gates are not needed, unbuffered gates are used to reduce the overall power consumption. A Gray-code counter containing two D-type flip-flops was used for data selection.

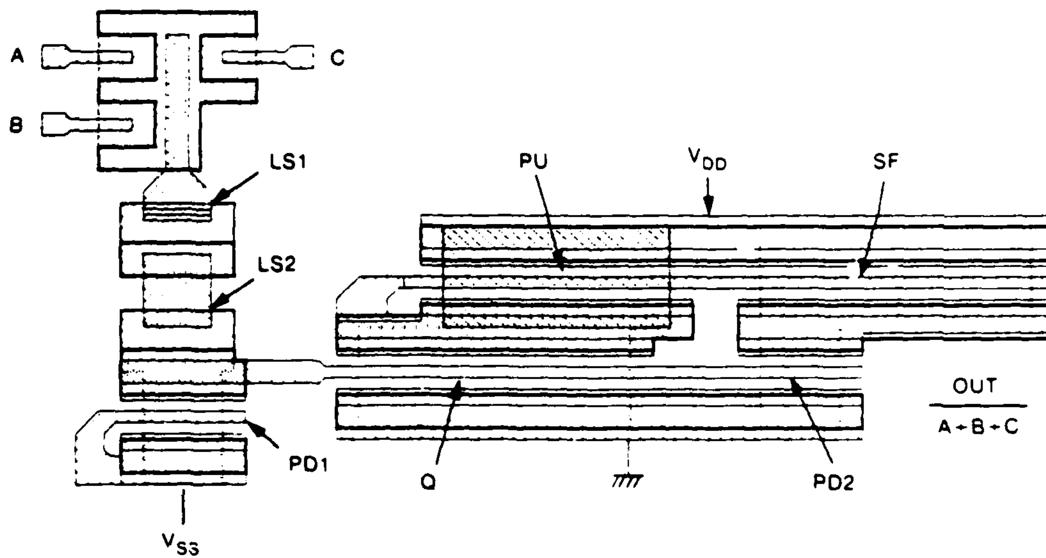


Figure 35. **Layout for a Buffered SDFL NOR Gate.** The cell size is 40 x 80 microns.

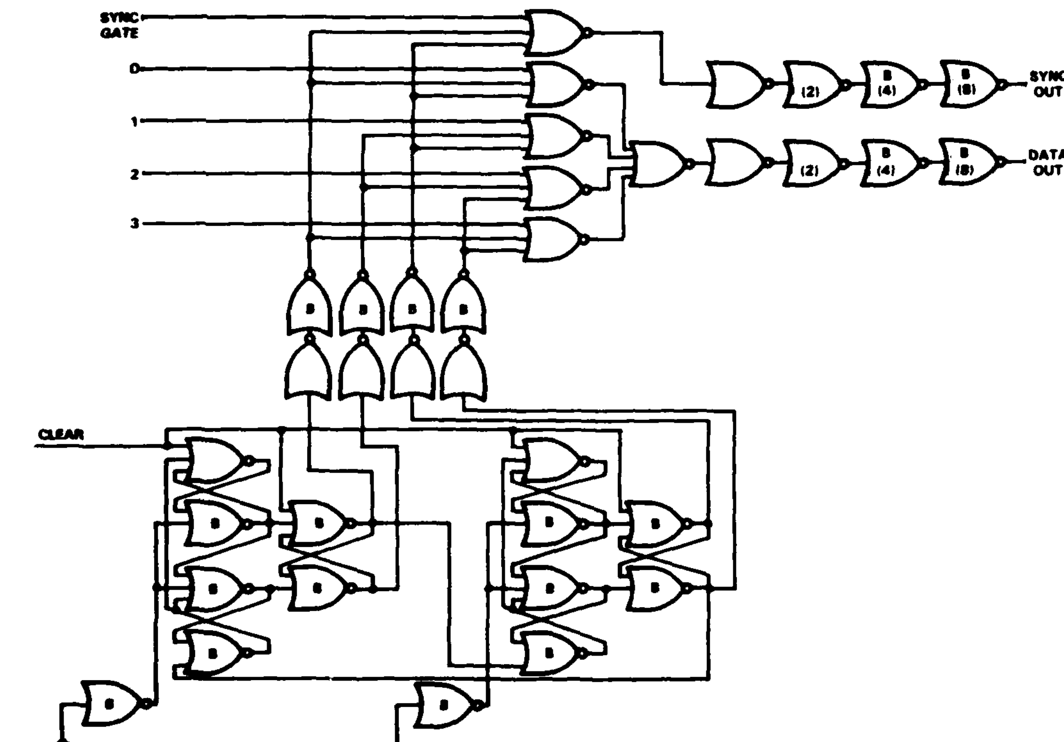


Figure 36. Logic Diagram of 4:1 Multiplexer using Mixed Buffered and Unbuffered NOR Gates. "B" within gate signifies buffered; number in parenthesis signifies the gate size referenced to a standard gate.

The circuits were fabricated using selective ion implantation into unintentionally doped LEC (liquid encapsulated Czochralsky) GaAs substrates. Ohmic contacts were formed using AuGeNi and the Schottky barrier/first level metal was TiW/Au patterned using a dielectric assisted liftoff process. The MESFET gate lengths were nominally 1μm. The interlevel dielectric was plasma enhanced CVD silicon oxynitride, and the second level metal was TiW/Au patterned using ion beam milling. A photomicrograph of the circuit is shown in Figure 37.

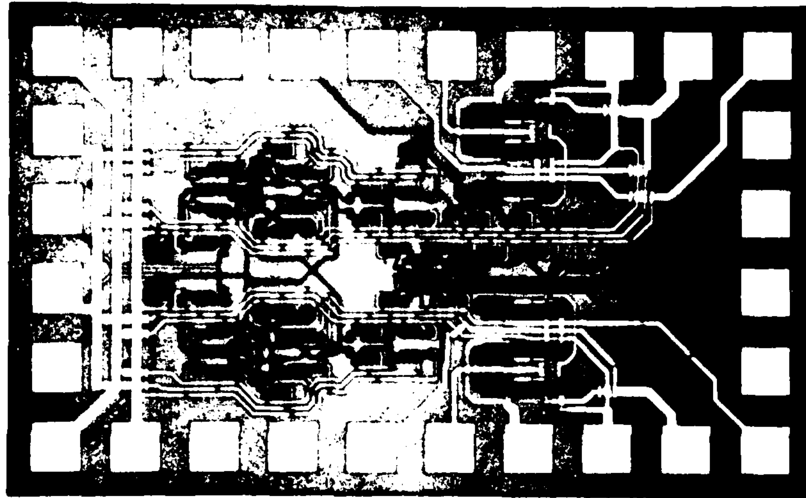


Figure 37. Photomicrograph of Honeywell's 4:1 Multiplexer.

DRIVER CIRCUIT DESCRIPTION

There are two different MESFET power driver circuits on the transmitter mask set. The schematics for these two devices are shown in Figure 38. In Figure 38a, the laser is connected in series with 4 FETs which are hooked in parallel. In operation, two of the FETs provide a constant bias to the laser while the other two FETs are the pulse current sources. In this circuit, the bias current to the laser is limited by the maximum current that the bias FETs can handle.

In Figure 38b, the 4 FETs are connected in parallel with the laser. In this configuration, a constant current is supplied to the laser/FET circuit. The bias FET can make adjustments to the bias current which flows through the laser and the pulsed FETs pull current away from the laser. Therefore, the laser is normally-on and the pulse FETs act to turn the laser off. There is no limit to the bias current which can be supplied to the laser in this configuration because the bias does not pass through an on-chip FET.

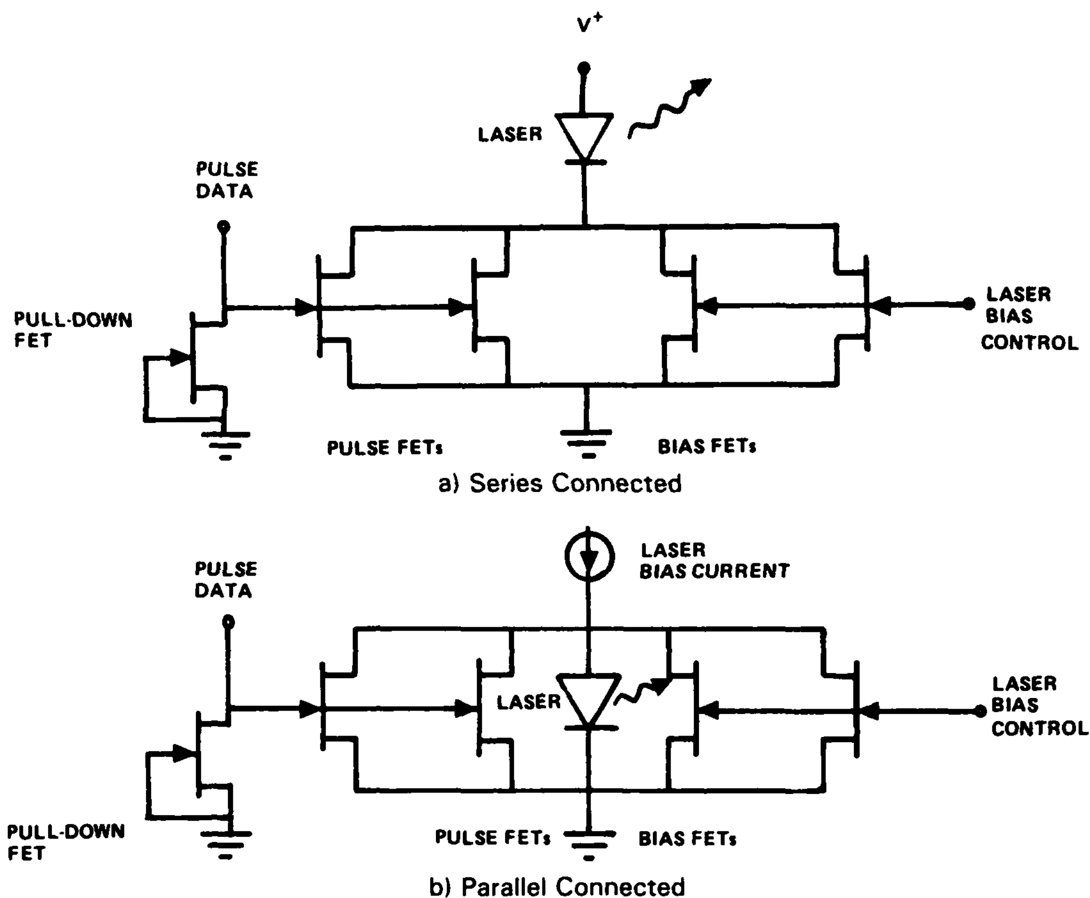


Figure 38. Schematics of FET Laser Driver Circuits

Both driver types were designed using the same models and design rules employed in the high-speed multiplexer. The gate of each FET is 1 micron long and 260 microns wide. This permitted the operation of the driver circuit at 1 Gb/s.

CIRCUIT EVALUATION

The validity of the 4:1 multiplexer design and the usefulness of the buffered NOR gate were demonstrated with the successful operation of multiplexer IC's at clock rates well over 1 Gb/s. In addition, easing the photolithographic alignment tolerances and improvements in fabrication techniques resulted in typical device yields of 50 percent. Figure 39 shows the results of testing the multiplexers from a 2-inch wafer on the probe station. Each block contains two different types of multiplexers. Approximately, a 50 percent yield was obtained for each type of Mux operated at 1.1 GHz clock rate. The lower right hand portion of the wafer was used for end point detection of one etch step. If the Muxs in that region are not counted, the yield is over 55 percent.

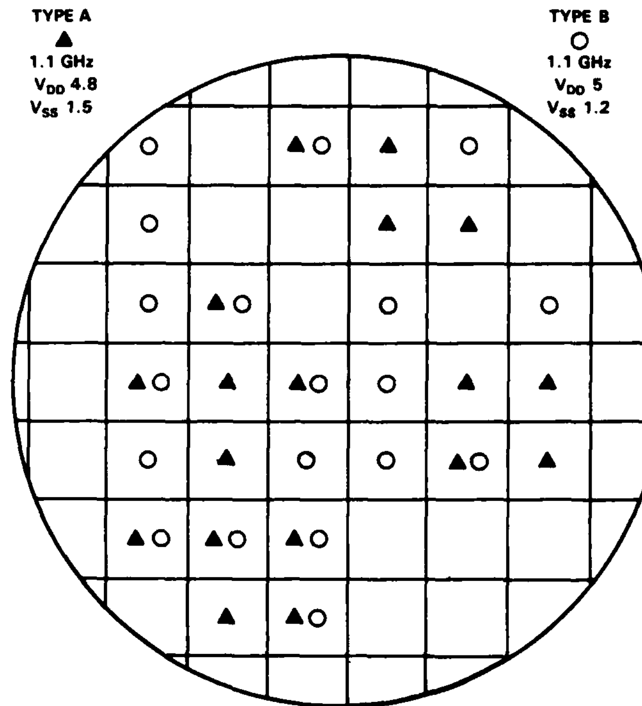


Figure 39. Multiplexer Yield Measured on a Two-inch Round Wafer. Each box contains two types of multiplexers. Each type was measured to have a 50 percent yield when operated at a 1.1 gigahertz clock rate.

The 4:1 multiplexers have operated up to 1.9 Gb/s in a microstrip test fixture with replaceable chip carriers. A description of the package is in Section 6. Figure 40 shows the output at 1.8 Gb/s for the two input combinations; 1:0:1:0 and 1:0:1:1. In the figure the signal has been attenuated by 10 dB at the sampling scope input. A 1.5 volt swing is developed across the 50 ohm load. The Mux output is the top trace

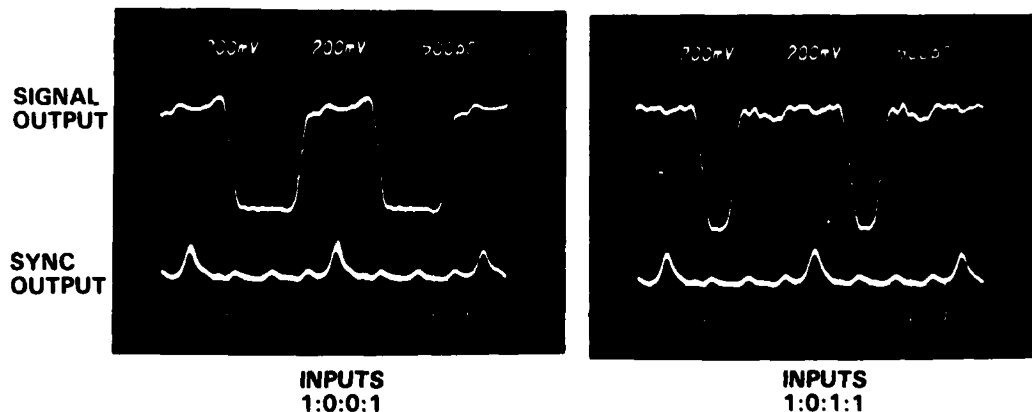


Figure 40. Oscilloscope Traces of the Response of a 4:1 Multiplexer to Two Different Sets of Electrical Inputs. The clock rate was 1.8 gigahertz.

in each of the photos while the Mux sync signal is the lower trace. The sync signal goes high when input line 1 is being sampled.

Packaged 4:1 multiplexers fabricated with the integration mask set have been tested with high-speed data into two of the four input lines. The other two lines were held at constant voltages. The two high-speed data streams were the output and the inverse of a 16-bit word generator with a maximum bit rate of 300 Mb/s. Figure 41 shows the oscilloscope trace of the Mux output (upper trace) and the Mux sync output (lower trace) for two test words at 275 Mb/s (1.1 Gb/s output). For this trace, Table 4 lists the input words to the Mux.

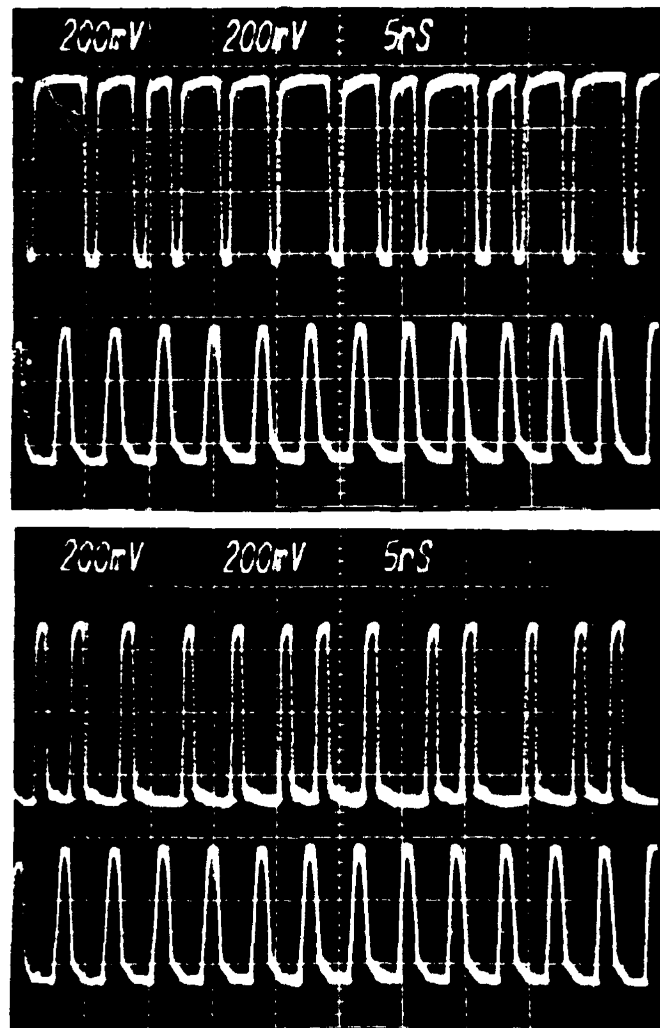


Figure 41. Output Waveforms (Upper Trace) and Sync-Out of a 4:1 Multiplexer for Two Different Inputs at 250 Mb/s at a Clock Frequency of One Gigahertz

Table 4. Input data to 4:1 Mux

Input 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Input 2	1	0	0	1	1	1	0	1	1	1	1	1	0	1
Input 3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Input 4	0	1	1	0	0	0	1	0	1	1	1	0	1	0

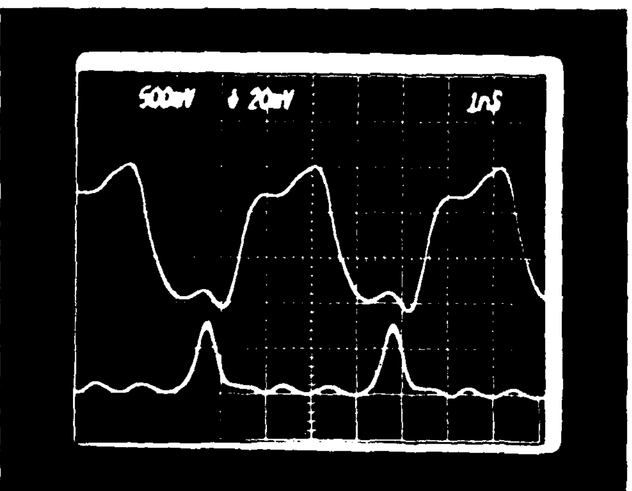
These multiplexers have operated flawlessly at the maximum input rate of the word generator (300 Mb/s) to give an output data rate of 1.2 Gb/s.

The driver circuits also operated at 1 Gb/s. Figure 42 shows the output for a packaged Mux/driver IC operating at 1 GHz clock rate for the two input combination 1:1:0:0 and 1:0:1:0. In order to obtain the electrical output from the driver circuit, it was necessary to supply an external bias. The bias circuit shown in Figure 43 was built for this purpose. The attenuation through this circuit was measured to be about 10 dB at 1 GHz.

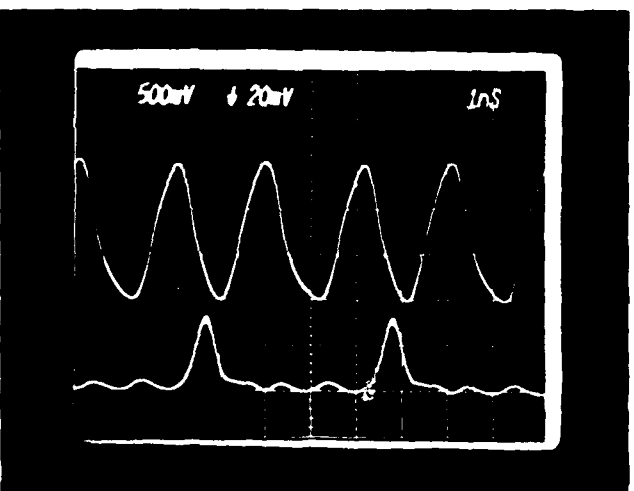
The Mux/driver IC has also been used to pulse one of the TJS lasers fabricated at Honeywell at 1 Gb/s. The laser was connected in parallel with the driver FET and a constant current was supplied as shown in Figure 44.

The response of a high speed detector for the input combinations 1:1:0:0 and 1:0:1:0 are shown in Figure 45. The Mux sync output is also shown and indicates a 1 GHz clock rate.

In separate experiments, the current handling capabilities of the driver FETs were measured. It was found that the bias FETs could handle 60 mA and the two pulse FETs could handle 20-30 mA each. Because a 40 mA current pulse to the laser is much more than desirable, one of the pulse FETs was removed from the IC which was used to drive the discrete laser. This Mux/driver was delivered to NRL.



a) Inputs 1:1:0:0



b) Inputs 1:0:1:0

Figure 42. ***Oscilloscope Traces of the Response of the Packaged Mux/Driver IC to Two Different Sets of Electrical Inputs.*** The clock rate was 1 gigahertz.

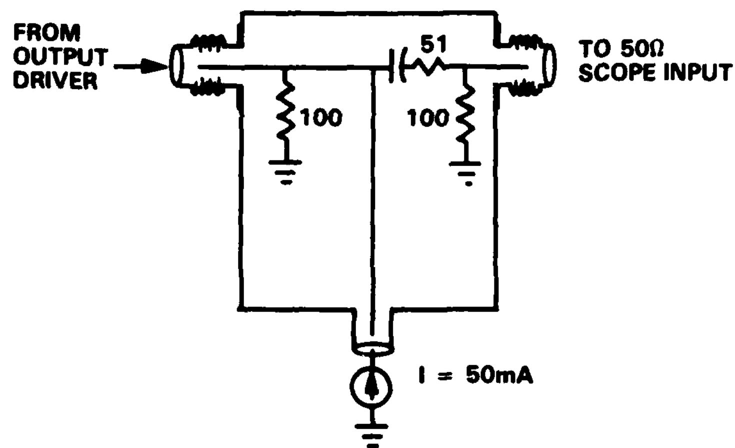


Figure 43. Schematic Diagram of Bias Box used to Test the Electrical Output of the Mux/Driver IC

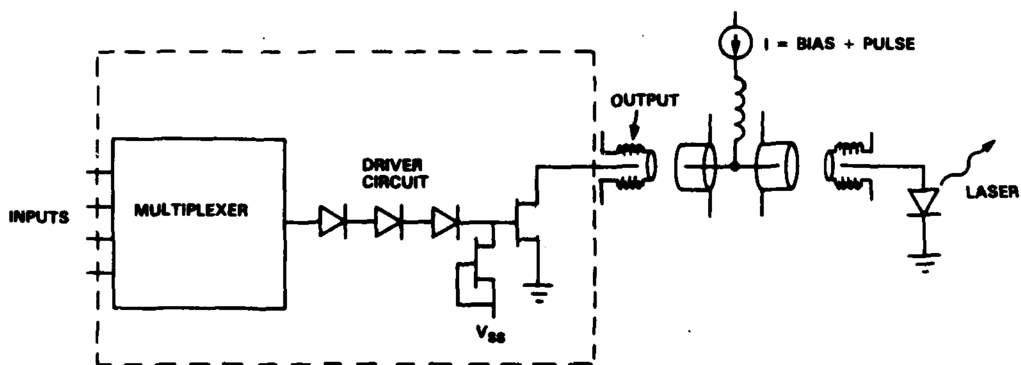
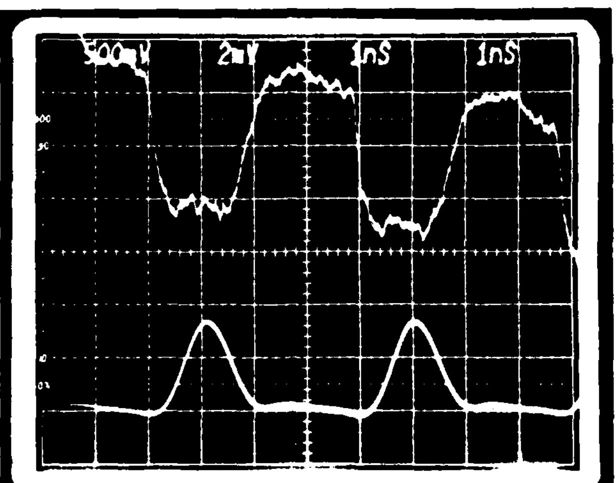
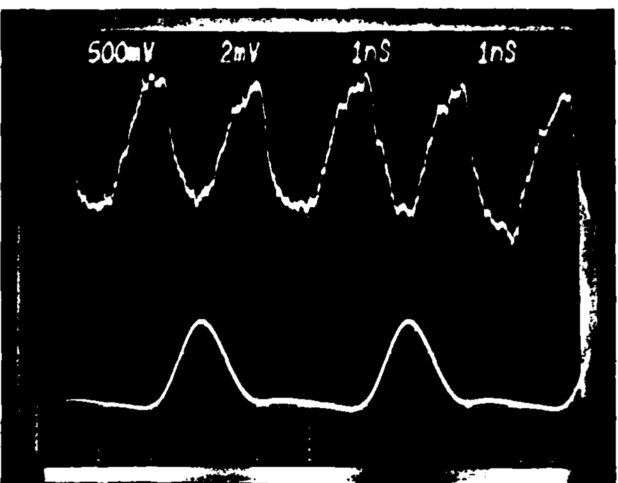


Figure 44. Schematic Representation of the Connection of the Bias Current Source and the Discrete TJS Laser to the Mux/Driver Circuit



a) Inputs 0:1:1:0



b) Inputs 0:1:0:1

Figure 45. Detected Response of a Discrete TJS Laser Driven by the Mux/Driver IC to Two Different Sets of Inputs Voltages. The clock rate was one gigahertz.

Section 6
Monolithic Optoelectronic Transmitter

The goal of this program was to integrate an AlGaAs laser diode with small-scale, digital GaAs electronics using processes which were compatible with both technologies. One of the criteria for the integration technique was that the processing required for the GaAs electronics would require no modifications due to the presence of the laser. Thus it would be possible to use all of the processing steps which were being developed for Honeywell's internally funded programs.

The laser-in-a-well integration concept was developed to meet this need. In the preceding sections, the laser-in-a-well was described. The processing and operating characteristics for the GaAs electronics and the TJS laser were also presented. In this section, we describe the design, fabrication, and packaging of the laser/Mux IC. The evaluation of the different fabrication runs is also presented.

TRANSMITTER IC DESIGN

Figure 46 is the CALMA plot of one transmitter chip on the mask set used in the integration runs. The transmitter die is approximately 1.8×1.8 mm^2. The 4:1 Mux and its associated circuitry are contained within the area surrounded by bonding pads in the lower half of the chip. The gates of all the MESFETs are 1μm long and are formed by contact photolithography.

The four FETs that make up the driver circuit are divided into two pulse FETs and two bias FETs. The gates of all four FETs are 1μm long and 260μm wide. The sources and drains of all the driver FETs are connected in parallel. The gates of the bias FETs go to a separate bonding pad. The gates of the pulse FETs are connected through three level shifting diodes to the Mux output at one of the internal probe pads. In this way, the operation of the Mux can be checked separately on a probe station during the processing.

The electronics required eight mask levels (fiducials, 2 implants, ohmic metal, Schottky metal, via holes, 2nd level metals, and pads).

The well containing the integratable TJS laser is in the upper left hand corner of the CALMA plot. A magnified view of this portion of the die is shown in Figure 47. In the original design, the wells were rectangular (200μm $\times$ 500μm). The wells were modified to be more diamond shape in order to obtain vertically etched sidewalls at 45° to the (110) planes. (See Section 3.)

Including the laser in the circuit requires five extra photolithographic masks: well etch, zinc diffusion, capping layer etch, epilayer etch for mirror fabrication, and Undercut Mirror mask. The laser uses the same metals as the electronics to form contacts. The lasers were connected electrically in parallel with the driver FETs. This permitted a large bias current to be applied to the laser.

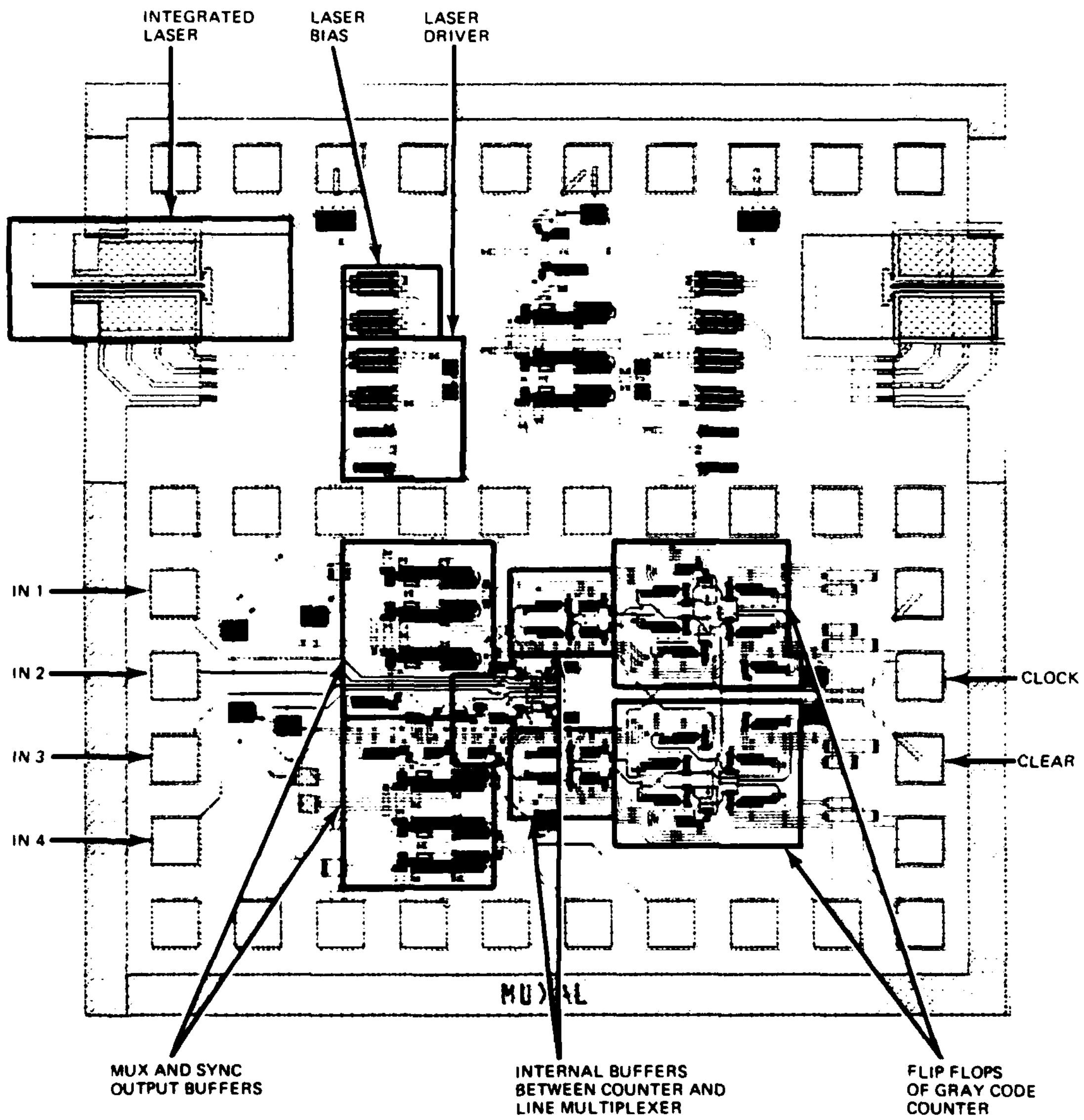


Figure 46. CALMA Layout of Monolithic Laser/Multiplexer IC

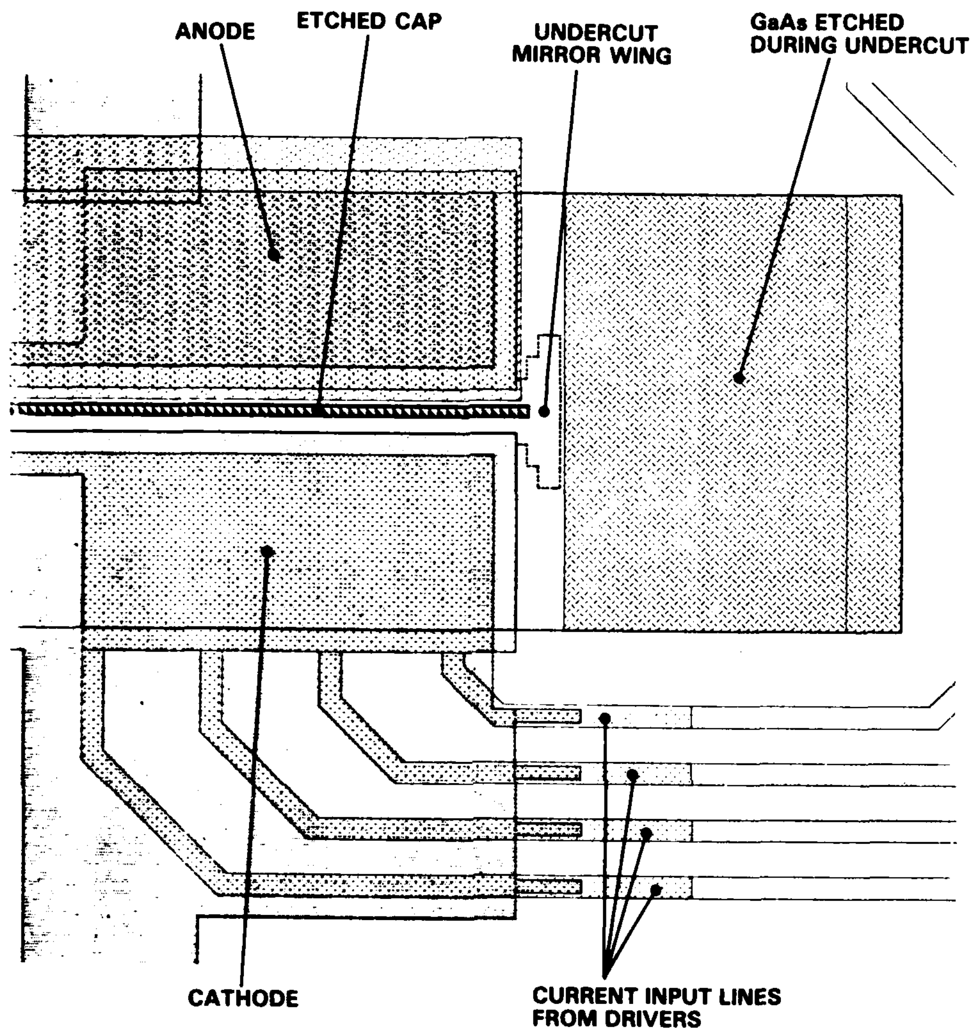


Figure 47. CALMA Layout of Integrable Transverse Junction Stripe Laser

The orientation of the laser stripe was chosen based on the preliminary development of the Undercut Mirror. It was found to be advantageous if the etched notch was formed in the long side of the dove-tail which was perpendicular to the laser stripe. This means that the laser stripe is oriented in the same direction as the FET gate widths.

The zinc diffusion and electrical contact to the lasers stuck out into the streets between adjacent chips. This permitted one laser mirror to be formed by cleaving between the chips. The other mirror was formed on-chip using the Undercut Mirror Process. The final laser length was about 250μm after processing.

PROCESSING SEQUENCE

In Sections 2 and 5, the processing steps required to fabricate the integratable TJS laser and the digital GaAs electronics were described. In this subsection, we detail the processing sequence for the monolithically integrated transmitter.

The integration processing sequence consists of three major sections:

- Laser-in-a-Well Processing
- GaAs Electronics Processing
- Laser Etch Steps and Dicing.

The major tasks in each of these sections is given in Table 5.

Table 5. Laser/Mux Integration Processing Steps

- Laser-in-a-Well Processing:
  - Wells etched in semi-insulating substrate
  - AlGaAs/GaAs epitaxial layers grown by liquid phase epitaxy
  - Epilayers outside of wells removed, exposing the semi-insulating substrate
  - Selective zinc diffusion to form TJS laser (700°C, 1 hour)
  - Zinc drive (900°C, 2 hours)
  - Semi-insulating GaAs surface polished
- GaAs Electronics Processing:
  - Nitride deposition
  - Ion implantation
  - Implant anneal
  - Ohmic contact metallization
  - Schottky contact metallization (p-ohmic)
  - Interlevel dielectric deposition
  - Via holes
  - Interconnect metallization
  - Passivating nitride
  - Mux evaluation
- Laser Etch Steps and Dicing:
  - TJS laser cap etch
  - Epi-etch for mirrors
  - Wafer thinning (150μm)
  - Backside metallization
  - Undercut etching
  - Die separation and cleaning
  - Laser evaluation
  - Mounting

In the laser-in-a-well processing section, the initial laser processing is performed. The AlGaAs double heterostructure is grown in wells etched into a one square inch semi-insulating substrate. After the resurfacing, the zinc is diffused and then driven into the TJS laser. The final surface polish removes 1-2μm of semi-insulating GaAs substrate. This step was included in the process after it was determined that the high temperature zinc steps changed the semi-insulating nature of the GaAs substrate, resulting in some surface leakage. Later in the program, better methods (CVD silicon nitride) were found for protecting the substrates during the zinc drive step. The surface polish was kept in the process sequence because it was not known just how well the CVD nitride maintains the uniformity of the surface.

One goal of the laser-in-a-well integration technique is that no modifications would be required for the GaAs electronics processing. Except for the use of one square inch substrates rather than two-inch round substrates, this goal was met. The n-ohmic metal for the FETs is also used as the n-ohmic metal for the laser. The Schottky metal for the FETs is used as the p-metal for the laser. We have not had any difficulty using the Schottky-metal as a p-type contact to the TJS laser because the surface concentration of zinc is near $1 \times 10^{20} cm^{-3}$.

Following the completion of the GaAs electronics processing, the wafers are placed on an automated probe station and are tested for working multiplexers. If there are working Muxs, the wafers continue on to the final laser processing.

The etch steps were placed at the end of the processing in order to avoid problems with non-planar substrates, and to prevent any degradation of the lasers due to exposure to the GaAs processes. It should be noted that the last photolithographic step and undercut etch take place after the sample has been thinned to about 150 μm. This is accomplished by attaching the thinned wafer to a glass cover-slip prior to spinning-on the resist. The wafer thinning step is required not only for heat sinking for the laser, but also to allow a good cleave for one laser mirror. A photo of a processed laser/Mux chip is shown in Figure 48.

After the transmitters are separated into individual chips, the lasers on chips with working multiplexers are pulse tested and their threshold currents measured. Those ICs with working lasers and Muxs proceed on to bonding.

Die bonding was attempted with thermally conductive epoxy, An-Sn (gold-tin) alloy solder, and In (indium) solder. The In solder was the best by far. However questions exist concerning the use of indium underneath a thinned IC. There is the possibility that the subsequent wirebonding will force the edges of the chip into the soft indium and break the die. By using only a thin layer of In, we have been able to avoid this problem for the most part.

After the chip is attached to the copper heat sink, the laser is once again tested, but this time with DC current. If the laser operates CW, the wire bonding of the chip to the carrier is performed. Because the laser is connected in parallel with the driver FETs, the gates of the bias FETs are connected to V_{ss} in order to cut-off any current flow through the FET.

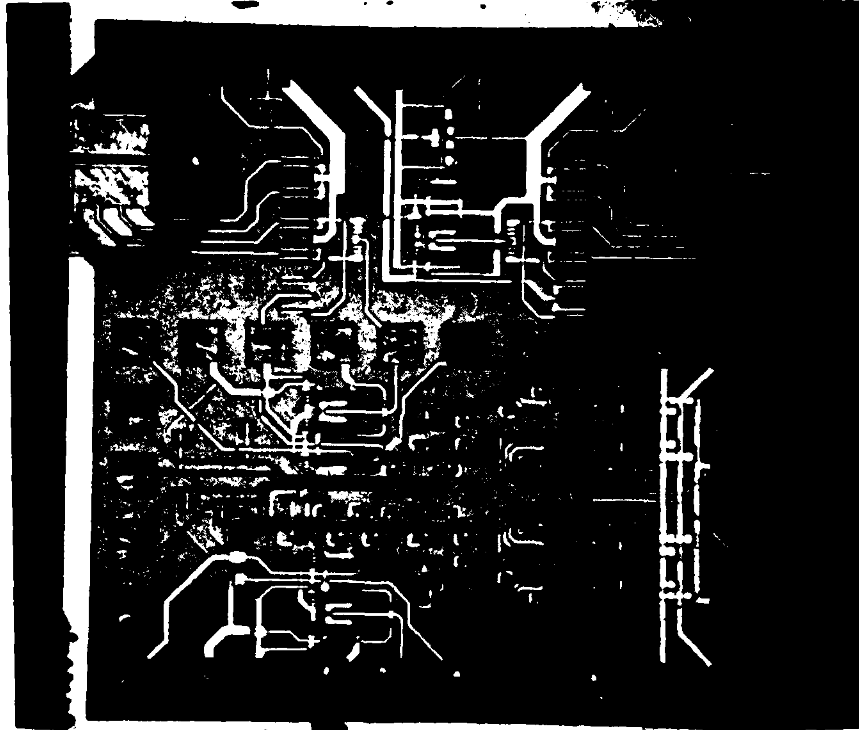


Figure 48. Photomicrograph of the Completed Laser/Multiplexer IC. The die is 1.8 × 1.8 mm square.

PACKAGING

A useful package for an IOEC (integrated optoelectronic circuit) must fulfill a number of stringent requirements: electrical, optical, and thermal. The electrical interface between the IOEC and its package is similar to that of any other high-speed GaAs IC.

Proper impedance matching, shielding and filtering are required for Gb/s operation. A controlled impedance chip carrier is required and the access for an optical fiber to the optoelectronic component must be provided. In addition, the package must supply adequate heat sinking for the IOEC in order to keep the laser threshold low. Honeywell has developed a method of packaging the laser/Mux that was based on a sucessful package for the 4:1 multiplexer.

Figure 49 shows an exploded view of the components in the laser/Mux package. The self-contained module consists of a machined aluminum housing with a hermetically sealable top cover. The data, clock, sync and power lines are connected by SMA jacks.

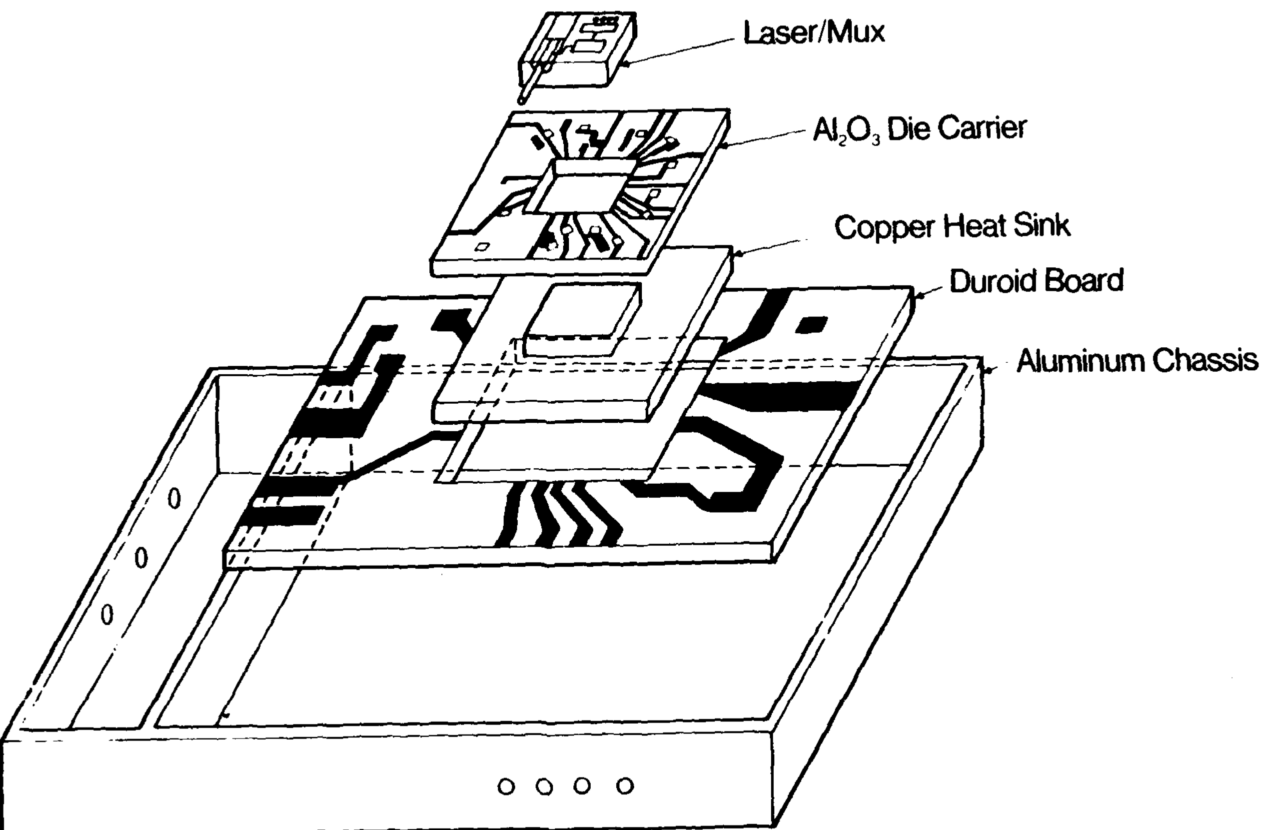


Figure 49. Exploded View of the Components in the Laser/Multiplexer Package

Figure 50 shows a photograph of the chip carrier for the laser/Mux. The cross-sectional representation of the housing and chip carrier assembly is shown schematically in Figure 51. All data, clock, sync, and power lines pass to the chip carrier on a gold-plated copper microstrip line patterned on a Duroid motherboard. The motherboard has been reflow-soldered to the bottom of the aluminum housing.

The laser/Mux IC, terminating resistors, and supply bypass capacitors are located in the chip carrier assembly area. The carrier consists of a metallized Al_2O_3 ceramic which is Au-Ge soldered to a Ni-Au metallized Cu heat sink. The top side of the ceramic is TiW-Au-Ni-Au metallized. The IC is then In soldered to the Cu heat sink. The heat sink sticks up through a rectangular opening which has been laser-machined through the Al_2O_3 ceramic. Contact to ground for terminating resistors and bypass capacitors is made by plated through holes in the laser-machined, Al_2O_3 metallization. The interconnection from the die carrier to the motherboard is accomplished by parallel gap welding using Au ribbon.

Microstrip lines are used on both the alumnina chip carrier and Duroid motherboard. All inputs and outputs use 50-ohm microstrip lines fabricated on the chip carrier. These lines taper slightly near the chip area. The termination for clock, data and sync-in signals consist of 50-ohm resistors attached from the microstrip lines to ground. The 50-ohm microstrip lines change width from the Duroid motherboard to the alumina carrier with a resulting excess capacitance at the interface. This is compensated for by an appropriate tapering of each line as it approaches the interface. The microstrip lines on the alumina also taper near the ICs, so that the large number of lines fit along the small IC opening. The resulting reduction in capacitance is useful in compensating the input capacitance of the ICs.

The major difficulty with this design for packging IOECs is that no method for aligning or attaching the optical fiber has been built into the chip carriers. At the present time, a very cumbersome method is used to position and hold the fiber. The fiber is threaded through a glass capillary tube which is held in a micromanipulator. The capillary tube is inserted through an extra hole drilled through the aluminum box. The fiber is then positioned manually using the micromanipulator. Care must be taken to avoid either damaging the face of the laser or breaking any wire bonds on the chip carrier.

EVALUATION

The evaluation of the laser/Mux ICs includes not ony those tests which were performed on packaged chips, but also the in-process tests. Also in this section is a listing of the results for all the substrates which started the laser/Mux integration process.

In all, the epitaxial layers for the TJS laser were grown on 31 wafers with etched wells. Of these 31 wafers, 14 made it through the growth and initial laser processing. The causes for the loss of the other 17 wafers were breakage (3), bad LPE morphology (7), poor zinc diffusion (2), and conversion of the semi-insulating substrate during processing (5).

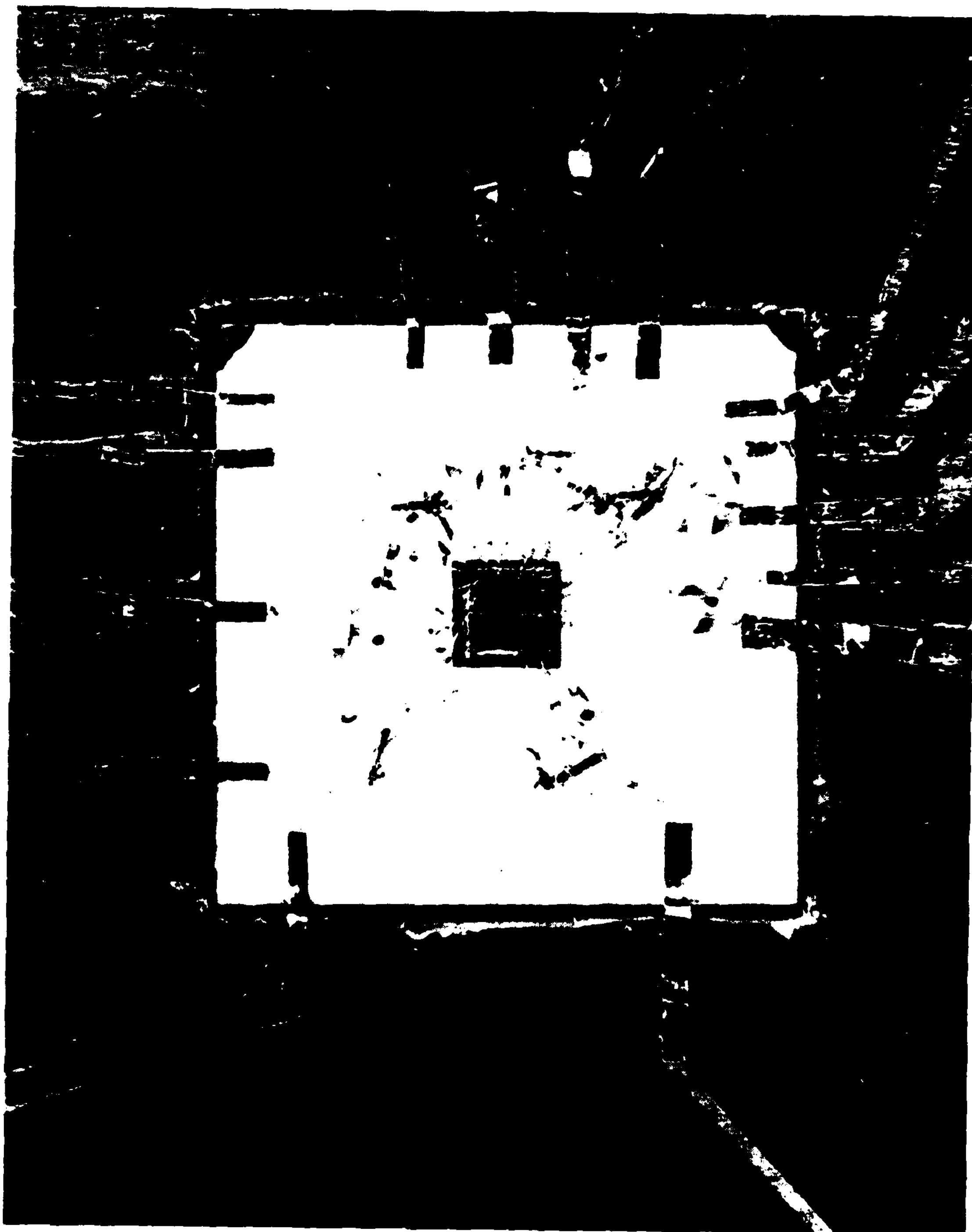


Figure 50. Photograph of the Laser/Multiplexer Chip Carrier

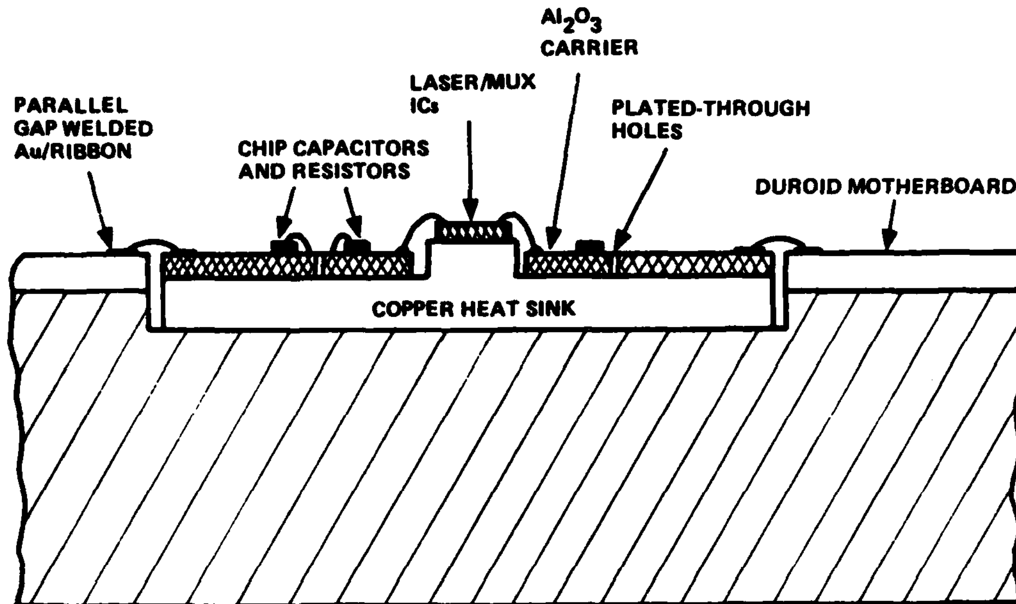


Figure 51. Detail of the Laser/Multiplexer Chip Carrier Assembly

The 14 wafers that completed the initial laser fabrication steps were sent through GaAs electronics processing in four runs. Of these 14 wafers, only 7 were fully processed and probe tested for working Muxs. The other 7 were lost due to breakage (2), wrong implant dose (2) and poor lithography due to bad resurfacing (3).

Of the 7 wafers carried through electronics processing, only the two from Run #4 had working multiplexers when tested on the probe station. These two samples were the source of the successful laser/multiplexers.

Two wafers from Run #1 were completely processed even though the semi-insulating surface was badly pitted due to thermal damage during the LPE growth (See Section 3). These samples had no working multiplexers, but 7 stage ring oscillators operated with 107 psec gate delays.

The one wafer from Run #2 that made it through GaAs processing was found to have excessive surface leakage due to insufficient protection of the substrate during the high temperature zinc drive and implant anneal steps. Both wafers from Run #3 were eliminated by excessive surface current. These samples came from a poor boule of semi-insulating GaAs substrates which converted badly at temperatures above 800°C.

The two wafers from Run #4 gave nearly identical results. 6 out of 24 Muxs on each wafer were completely operational at a 500 MHz clock rate on the probe station (25 percent yield). Two or three other Muxs had minor problems such as single input lines that were stuck high or low.

After the final laser processing steps, the lasers were tested with pulsed current. Eleven out of twelve devices lased. However, the threshold currents were 60-90 mA, which was higher than previously achieved. The cause seemed to be in the LPE growth. In an effort to minimize pinholes on these wafers, the layers were grown from a 2-phase melt which led to thin AlGaAs confining layers. Therefore, there was absorption of the laser light in the cap and in the substrate. As a result, for only one packaged transmitter did the laser still work when the electronics were also turned on. The other devices did not reach threshold due to the extra heat generated by the electronics.

The packaged laser/Mux IC has been tested at a 160 MHz clock rate. Figure 52 is an oscilloscope trace of the detected output of the laser/Mux transmitter chip. The lower of the two traces is the sync output from the multiplexer. This line goes high each time that input-line 1 is sampled. The upper trace is the detected output from the laser (inverted by the detector). The four input lines to the multiplexer were 0:1:1:1 and the clock rate was 160 MHz. The detector had a 1 nsec rise time and the oscilloscope amplifier had a 250 MHz bandwidth. This accounted for the relatively long rise and fall times shown in the photo. Before high speed testing could be done, however, the chip was inadvertantly damaged.

The photo in Figure 53 is the detected output of a transmitter IC which would not lase when the GaAs digital circuit was operating. The laser in this case operated as a light emitting diode (LED) and did not respond well to the 160 MHz pulsing from the Mux/driver circuit.

In summary, we successfully operated the first integrated optoelectronic circuit containing a laser and digital GaAs electronics. Therefore, we achieved the goal of developing the processing technology required to combine these very different components.

The maximum operating speed of the laser/Mux chip was not measured. However, the testing of the discrete components leads us to believe that 1Gb/s would have been reached if the chip had not been damaged.

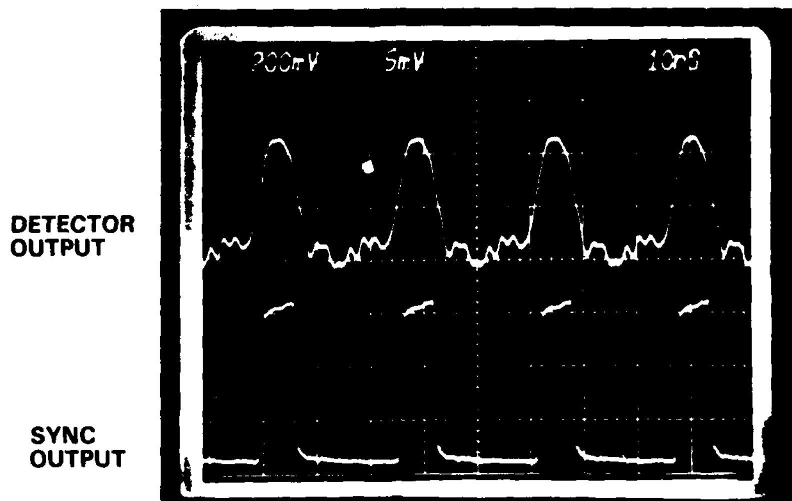


Figure 52. Detected Output of an Integrated Laser/Multiplexer Transmitter IC. The inputs were 0:1:1:1 and the output was inverted by the detector. The clock rate was 160 MHz.

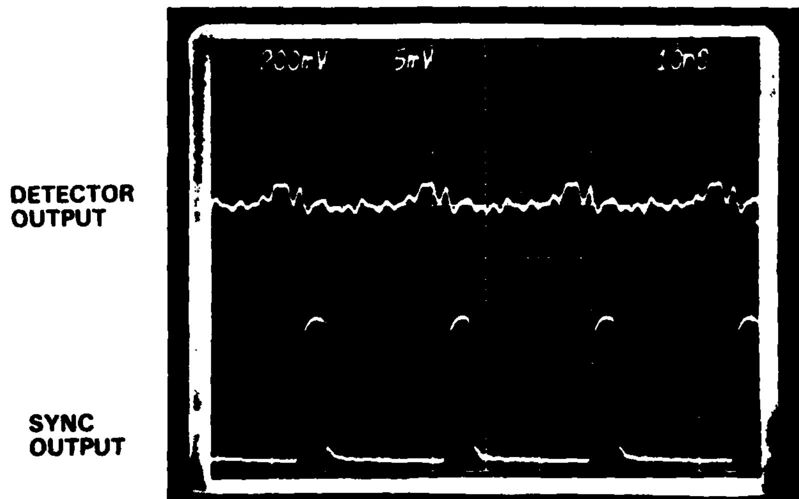


Figure 53. Detected Output of a Transmitter IC which did not Lase. The inputs were 1:1:1:0 and the clock rate was 160 MHz.

Section 7
Discussion of Problem Areas

Within the course of this program, there were a number of significant successes:

- Demonstrated the first integrated optoelectronic circuit which combined an AlGaAs laser with small-scale digital GaAs circuitry.
- Demonstrated the process for integrable low-threshold-current TJS lasers.
- Developed the Undercut Mirror process and applied it to TJS lasers in wells.
- Developed a technique for resurfacing the wafers after LPE growth to permit 1μm lithography.

There were a number of deficiencies, however, which were noted in the design, process development, and overall performance of the components. These shortcomings as well as an assessment of yield and process compatibility are described in this section.

DEFICIENCIES

The greatest threat to the success of the program was the development of the TJS laser. Although a process for low threshold TJS lasers was demonstrated, this task took much longer than originally planned. Thus, there was insufficient time available to completely adapt this procedure into the integration process. The result was that the layers grown during the final fabrication runs were too thin and the lasers had higher threshold currents than we had previously demonstrated.

Because the room-temperature threshold currents of the lasers on the transmitter ICs were high to begin with, most of the devices did not lase when the heat generated by the 1.5 watts dissipated by the multiplexer increased the chip temperature about 20°C. A portion of this temperature increase might have been avoided if more effort had been placed on the package development. However, the thermal considerations for the package were not studied.

Another deficiency with both the package and the chip layout was that alignment and attachment of an optical fiber was not given enough consideration. Difficulty arises from the fact that the input pads to the multiplexer are on the same edge of the chip as the laser's emitting region. The wirebonds, microstrip lines, and terminating resistors tend to be in the emission path for the laser. We attempted to overcome this problem by rotating the laser/Mux IC by about 15 degrees during mounting so that the electrical interconnects did not shadow the output. This was not an acceptable solution.

The most serious drawback to the development of a reproducible technique for optoelectronic integration was the use of liquid phase epitaxy as a crystal growth technique. Typical GaAs electronic processing is performed on 2-or 3-inch round substrates. LPE limits the size of substrates to one square inch. In addition, selec-

tive epitaxy cannot easily be performed with LPE. Therefore, the double heterostructure must be grown over the entire wafer and then be removed from the regions outside the wells. The pinholes that are always present in the LPE layers lead to pits in the substrate during the resurfacing steps and ultimately lower the yield.

YIELD AND PROCESS COMPATIBILITY

As enumerated in Section 6, the laser/Mux process has thus far been extremely low yield. Out of 31 wafer starts, only one device was successfully operated. This result is due in part to the long, complex process sequence which contains 13 mask levels and many non-standard steps. However, the greatest cause for wafer rejection was that some of the most critical processes were developed after most of the wafers had already been processed. For example, wafer rejection due to poor zinc diffusion, bad surface morphology, and surface conversion were eliminated before run #4. Only one wafer out of the final 10 was rejected for bad LPE morphology and only one wafer out of the final 15 was broken during processing.

At the end of the program, the remaining low-yield processes appeared to be: 1) reproducibly obtaining the correct epi-layers for the TJS laser, and 2) implanting the MESFET channel regions with the proper dosage to achieve FET threshold voltages between 0.9 and 1.6 volts.

The 25 percent yield of multiplexers on the final two wafers demonstrated that the processing for the TJS laser could be made compatible with the requirements for the GaAs electronics. However, the effects of the laser processing on the performance of the GaAs circuits was never quantified.

The 25 percent yield was lower than should have been achieved on these wafers. However, most of the non-working Muxs could be attributed to the condition of the photo-masks during the run. The two final wafers were produced by contact photolithography, and the photo-masks were well used by the time of run #4. The result was that many of the non-working multiplexers contained observable defects in the metal patterns caused by damage on the masks.

During the program, both semi-insulating chrome-doped substrates and undoped substrates were used. No working GaAs circuits were successfully fabricated on the Cr-doped substrates because the necessary implant dose could not be calibrated due to non-uniformities in the activation of the implant species. Therefore, the undoped LEC (liquid encapsulated Czochrolsky) substrates were preferred during this program. However, the high defect density of present LEC material may greatly decrease the lifetime of the integrated lasers, making these substrates incompatible with the requirements of the laser diodes.

In the next section is a short discussion of some of the issues which must be addressed in any future program if large integrated optoelectronic circuits are to become viable.

Section 8
Areas of Future Investigation

During this program, we demonstrated the feasibility of fabricating an AlGaAs laser with a complex digital GaAs circuit. However, the development of a predictable, flexible, high-yield procedure for the integration of optoelectronic components with a large variety of GaAs circuits requires that several issues mentioned below be addressed:

- The development of the laser/Mux IC has been slowed by a number of yield-limiting processes. To fabricate larger, more complex IOECs in the future, these low-yield processes must be modified so that we can move beyond the laboratory feasibility stage to a producible design.
- Although we have proven that the epitaxial crystal growth and laser processing does not result in surface conversion, it is not known how these additional processes affect device uniformity, circuit noise margins, and ultimately yield. Any changes in the substrate characteristics would be detrimental, especially if enhancement-mode circuits were to be used.
- It is not known if LEC GaAs substrates are suitable for optoelectronic components. The high etch-pit density might cause a low yield of lasers with long lifetime.
- It is desirable to produce laser diodes that can be integrated using a high yield process, have extremely low threshold currents at elevated temperatures, and have multiple Gb/s modulation capabilities. It is not known if all of these characteristics can be achieved in a single laser or if trade-offs will be required.
- The laser fabrication processes must be scaled-up to handle three-inch substrates in order to accomodate the state-of-the-art projection lithographic techniques. The epitaxial growth on three-inch substrates by MOCVD (metal-organic chemical vapor deposition) and the Zn diffusion steps will require major revisions to handle large substrates.

It will also be necessary to design and fabricate the complementary receiver circuit to the optoelectronic transmitter. Including a GaAs optical detector on the same chip as a GaAs circuit will be easier than integrating a laser on the substrate. However, the circuit design for the high speed amplifier will be much more difficult than the driver circuit for the laser.

Finally, a large effort must go into the development of packaging techniques for IOECs. The package must provide impedance matching for the electrical inputs and outputs, accomodate optical fiber coupling, and provide good heat sinking for circuits that tend to dissipate a few watts of power. Very few of these issues have yet been addressed in any optoelectronic integration program, but providing adequate solutions will be essential if these chips are to be used in real systems.

Section 9
Conclusion

During the first phase of our Integrated Optoelectronic Circuits (IOEC) program, Honeywell successfully fabricated and tested the first IOEC that contained a laser diode driven by a complex digital GaAs circuit. This IOEC was also the first reported in which the electronics was formed by selective ion implantation into the semi-insulating substrate.

Other significant accomplishments which were achieved during this period were:

- Drove a discrete TJS laser (fabricated at Honeywell) at 1 Gb/s with the GaAs Mux/driver IC.
- Demonstrated TJS lasers with threshold currents (I_{TH}) less than 35 mA.
- Demonstrated the first TJS Laser-in-a-well (I_{TH} = 42 mA).
- Developed the Undercut Mirror Process.
- Demonstrated the first integratable TJS Laser-in-a-well with Undercut Mirror (I_{TH} = 52 mA).
- Operated the 4:1 Mux at GHz rates
  - Above 1.8 GHz clock rate with DC inputs
  - 1.2 Gb/s with high speed inputs (test system limited).
- Demonstrated a planarization technique that produced mirror smooth surfaces for digital IC fabrication.
- Developed a custom package for the optical transmitter.

In future work on IOECs, the biggest question is whether long-lived semiconductor lasers can be fabricated on LEC grown GaAs substrates. Once this question is answered, the greatest amount of effort will need to be expended on eliminating the yield limiting steps in the fabrication process and on developing an adequate package for the chips.

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