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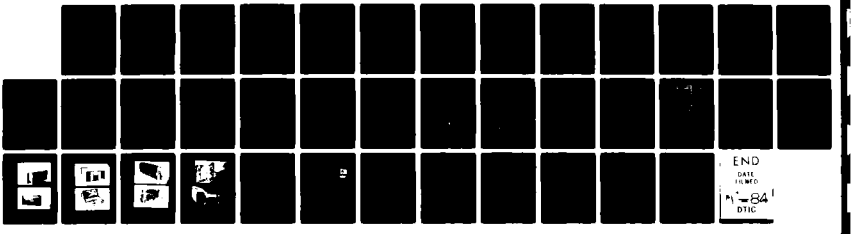

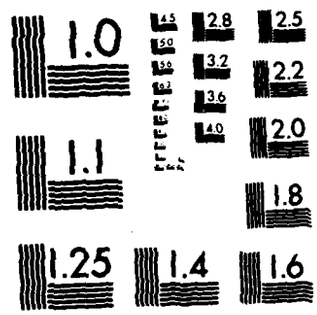

DNA 6271F

ACQUISITION SYSTEM FOR DIGITAL DATA RECORDING

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3251 Hanover Street
Palo Alto, California 94304

28 February 1982

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This report describes the development of a multi-channel data acquisition system for the digital recording of analog signals using charge-coupled-device (CCD) technology. The original brassboard design provides eight channels of fully independent analog recording at 160 MHz input sampling rate in a single 8-3/4-inch-high rack-mount chassis. Included in this report are evaluations of the general technological problems directly associated with fast data-acquisition systems using CCDs and also with items such as clock driver technology, triggering and control techniques, digitizing techniques, and

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20. ABSTRACT (Continued)

output data-handling procedures.

A secondary goal was to generate a working eight channel DAS capable of sufficiently high performance. Because of problems encountered in the actual layout and construction, this was not realized. However, the workability of the basic DAS design and its compatibility with future ultra-fast CCD development was indicated.

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SECTION 1
INTRODUCTION

The Lockheed Palo Alto Research Laboratory (LPARL) has carried on a program supported by the Defense Nuclear Agency (DNA) for the design, construction, and test at brassboard level of a multi-channel data-acquisition system (DAS) for the digital recording of analog signals using charge-coupled-device (CCD) technology. The original brassboard design provides eight channels of fully independent analog recording at 160 MHz input sampling rate in a single 8-3/4-inch-high rack-mount chassis.

The primary motivation for this program has been to evaluate the technological problems associated with the technique, not only problems directly associated with the CCD, but also with such items as

- o Clock driver technology
- o Triggering and control techniques
- o Digitizing techniques
- o Output data-handling procedures

It has been evident that if the problems in these areas could be solved in ways that would permit the realization of the theoretical intrinsic speed of CCD devices, data acquisition systems based on CCDs could compete favorably with digital oscilloscopes in providing high bandwidths for the recording of fast non-repetitive signals. One would then be able to profit from other capabilities offered by CCD systems, such as

- o Post triggering capability the digital trigger delay
- o The possibility of extremely long time windows in comparison to conventional oscilloscope sweep times of corresponding resolution

Since CCD technology is relatively new, the opportunity to influence the course of future CCD device technology development has been an important consideration. A very significant synergism has already developed between the DNA program and an ongoing LPARL Independent Research Program to develop and test technology for an ultra-high-speed CCD. In particular, clocking technology exchange has been very fruitful, and there are very attractive possibilities for using the new CCD device with the present DAS as a test vehicle.

This report describes the development of the DAS, including the investigations of CCD properties and clocking technique carried out prior to the brassboard design.

SECTION 2
TECHNOLOGY DEVELOPMENT

2.1 REQUIREMENTS FOR CCD DAS DESIGN INFORMATION

The design information required prior to defining the final brassboard design objectives consisted of two major parts. First, it was necessary to find and characterize the best available CCD for the application. Secondly, clock drive and control facilities adapted to the CCD and the application were required. These areas will be discussed in turn in the following sections.

2.2 CCD CHARACTERIZATION

Excluding laboratory prototype units as being too expensive and of dubious reproducibility, the best CCD we found available commerically was the Fairchild FCCD321A, a dual-channel unit with 455 stages per channel, rated at 20 MHz clock frequency. The unit is of the so-called 1-1/2-phase type, having a two-phase structure with one clock phase run at a DC level. The two halves of the unit have separately-driven clock lines with a common DC phase. By running the two sides at opposite clock phases and making use of input gating provided on the chip, it is possible to run the device as a 40-megasample single-input unit with successive samples alternating between the two sides.

2.2.1 High-Frequency Properties of the FCCD321A

Using a breadboard driver and control system based on the technology described below in Section 2.3, the properties of the FCCD321A were explored at clock frequencies ranging from 80 MHz to a few tens of kHz. Figure 1 shows data typifying most of the phenomena observed in operation of the FCCD321A at high frequencies.

These data were clocked into the register at 50 MHz and clocked out at 3.125 Mhz, with the signal input a series of 10-ns rise-time pulses. The trace shows the contents of approximately the first third of the register from the entry end, about 150 cells out of 455. The last pulse on the trace,

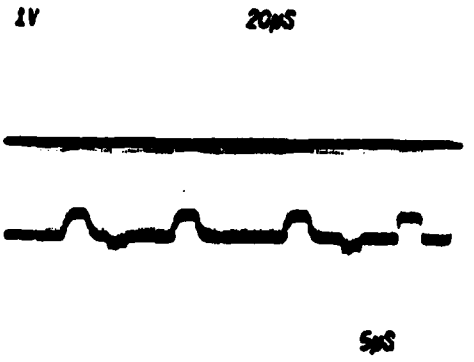

Figure 1 FCCD321A Performance at 50 MHz

therefore, had been clocked only some 16 or 18 cells into the register before the transition from 50-MHz to 3.125-MHz clocking took place. In consequence, there is little rise-time degradation visible on that pulse. Substantial rise-time increases are visible on the earlier pulses, however, and at the opposite end of the register (not shown) the signal bandwidth has dropped to just a few megahertz.

The sharp-edged, irregular negative pulses that appear on the trace are not associated with the signal, but appear at fixed intervals throughout the register, and are observed with very similar patterns at precisely the same locations in all CCDs of this type that we have tested. They are observable only in fast/slow switched clock frequency operation, and increase in amplitude with increasing clock frequency. From a number of lines of argument, we believe they represent regions of poor coupling of the clock fields in the CCD cell to the signal charge in the channel, probably associated with the necessary changes in cell geometry as the register is passed around a corner in the chip layout. In these regions, a kind of "puddle" of charge forms in the cell, with insufficient driving field to transfer at the high clock rate. When the clock rate is slowed down, the "puddles" have time to empty, by diffusion or other slower means, and in consequence deposit their contents immediately into the signal stream.

In first order, the effects of these corner defects of the register are readily removed from the signal by subtracting a background trace, cell by cell. From the rise-time effects observed in data such as that of Figure 1, however, it is apparent that these defects are major contributors to the degradation of signal bandwidth through the register. The effect is visible on close inspection of Figure 1--the rise-time increment between pairs of signal pulses separated by a defect is anomalously large in comparison to that between pulses not so separated. This is the result of the statistical nature of the charge separation at each clock cycle between propagating signal charge and the trapped charge in the defect.

When studies such as those described above were carried out at various frequencies, it was found that the maximum signal bandwidth of the FCCD321A occurs at clock frequencies very close to 20 MHz. At this frequency, the

risetime degradation through the entire register is very small, of the order of one clock cycle or less in duration, giving a signal bandwidth close to the Nyquist limit. Using both halves of the dual register in time multiplex, a sampling rate of 40 megasamples/sec is therefore a usable limit for one of these devices. Such operation was verified experimentally, including measurements confirming the efficiency of demultiplexing into the two channels using the input gating facilities of the chip itself.

2.2.2 Low-frequency Characteristics of the FCCD321A

The principal additional parameter of the CCD needed for the design of fast/slow data-acquisition applications is the register leakage rate, which sets the lower limit on frequency of readout. It was found that room-temperature leakage rates of the FCCD321A are typically full scale in 120 ms or so, corresponding to leakages of about 0.5 pA per cell. If one allows 20% of the saturation range for leakage drift, this implies a maximum readout period of the order of 50 or 60 microseconds per sample on each half of the device, well within the range of conversion time obtainable from inexpensive integrated circuit analog-to-digital converters (ADCs).

It should be remarked here that leakage pattern noise, which is a problem in start/stop operation of CCDs is largely averaged out in fast/slow operation, since the clock is never entirely stopped.

If multiple channels are required, either for multiple input signals or for bandwidth expansion using signal demultiplexing techniques, the measured minimum readout rates do place limits on the use of a single minicomputer as the digital storage element for an array of CCDs. For example, using the 5-microsecond minimum I/O cycle of our laboratory minicomputers, two 160-MHz demultiplexed channels would be about the maximum practicable without using substantially more complex direct memory access techniques. As will be seen below, this conclusion had a strong effect on the architecture of the brassboard DAS.

2.3 CLOCK DRIVER TECHNOLOGY

Because of the capacitive load presented by the CCD clock bus to the driver, and the careful waveform control required over a very wide frequency range, high-speed clocking of CCDs presents substantial problems in the

design of appropriate drive circuits. The initial objectives for this project required the investigation of the properties of CCDs at frequencies of the order of 100 MHz, well above the design maximum clocking frequency of the FCCD321A CCD.

2.3.1 80-MHz Driver Breadboard

In order to drive the capacitance of the clock inputs of the FCCD321A at such frequencies, substantial high-frequency power capability is necessary. The clock capacitance of the device under operating conditions was measured to be an unexpectedly high 75 pf, more than double the data-sheet specification.

The driver circuits built for this part of the investigation were based on the Siliconix VMP family of RF power field-effect transistors (FETs), and are diagrammed in Figure 2. The design is fully balanced, allowing both sections of the FCCD321A to be driven with minimum RF return current from the common DC phase line of the chip. As is evident, careful compensation and neutralization were required to achieve the necessary bandwidth. To reduce the very substantial power dissipation in the driver, the output stage used broad-band inductive bias elements. This circuit was capable of producing 15-V peak-to-peak output (each side to ground) at up to 80 MHz while driving 75-pf dummy loads.

2.3.2 20-MHz Driver Circuit

For driving the CCD array planned for the brassboard DAS system, it was desired to simplify the driving circuits as much as possible, since each analog channel would require eight clock inputs at 20 MHz. For this purpose the circuit of Figure 3, based on type 75361 MOS memory drivers, was tested. It was found that selected 75361's with proper input drive could produce the clock waveforms illustrated in Figure 4, very nearly optimum for the CCD. To provide a margin of safety, the brassboard layout provides socketing for enough 75361's to allow paralleling two drivers onto one clock line in order to reduce the dissipation in each driver.

2.3.3 Very-high-frequency Clock Drivers

It is clear from our experimental work that the extension of CCD driver technology to still higher frequencies is not a trivial matter.

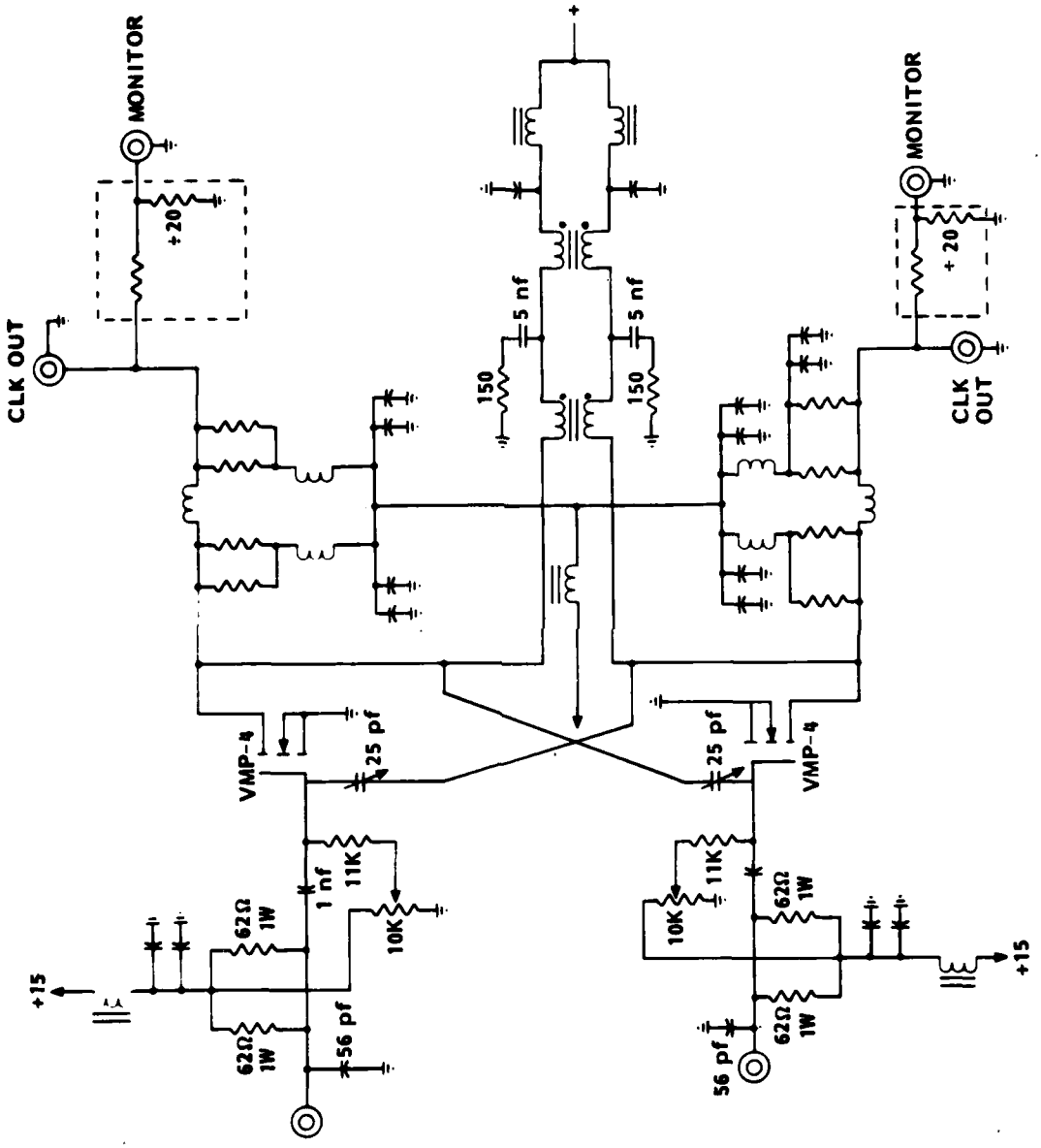

Figure 2a 80-MHz Clock Driver Circuit

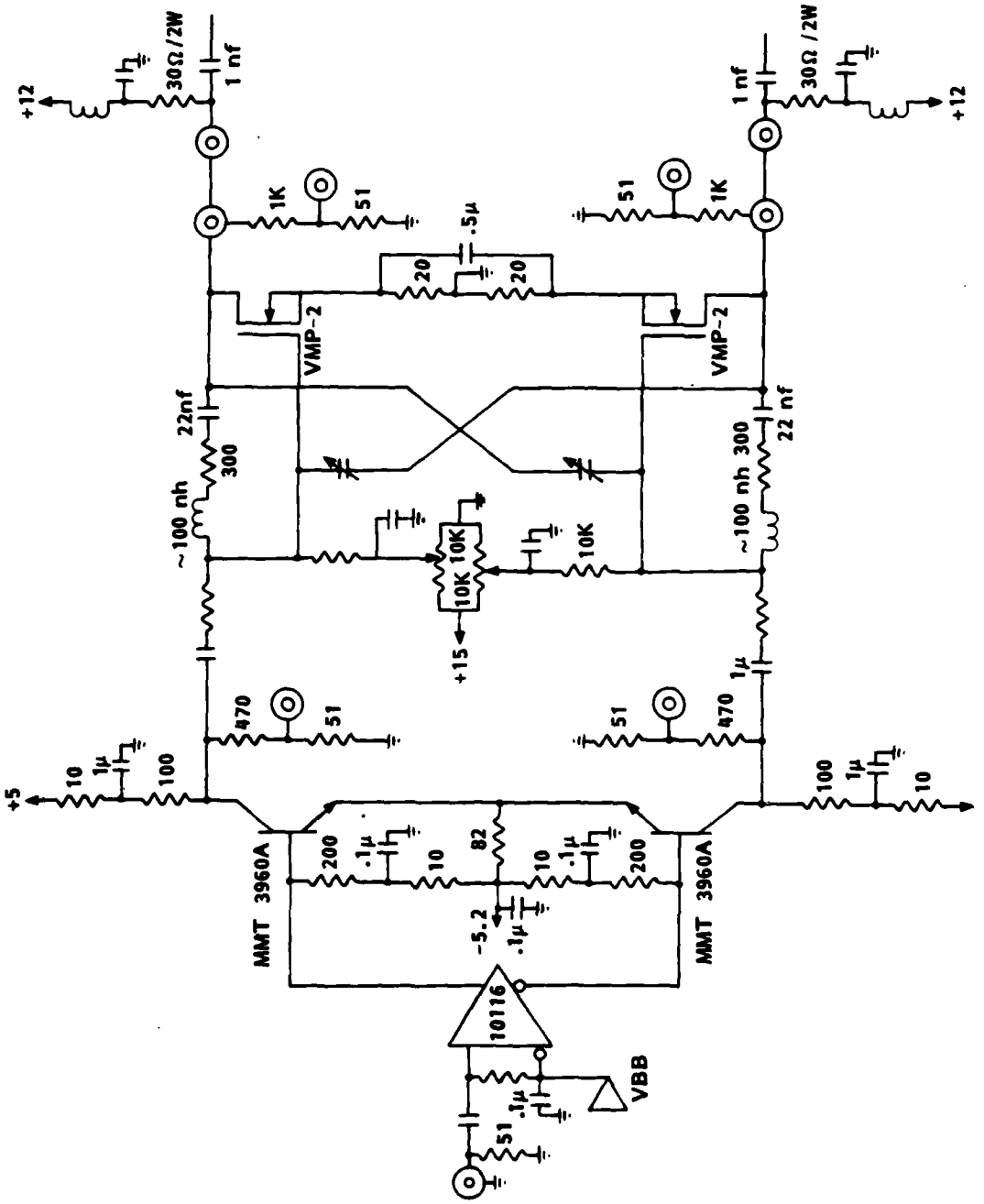

Figure 2b 80-Mlz Clock Pre-Driver Circuit

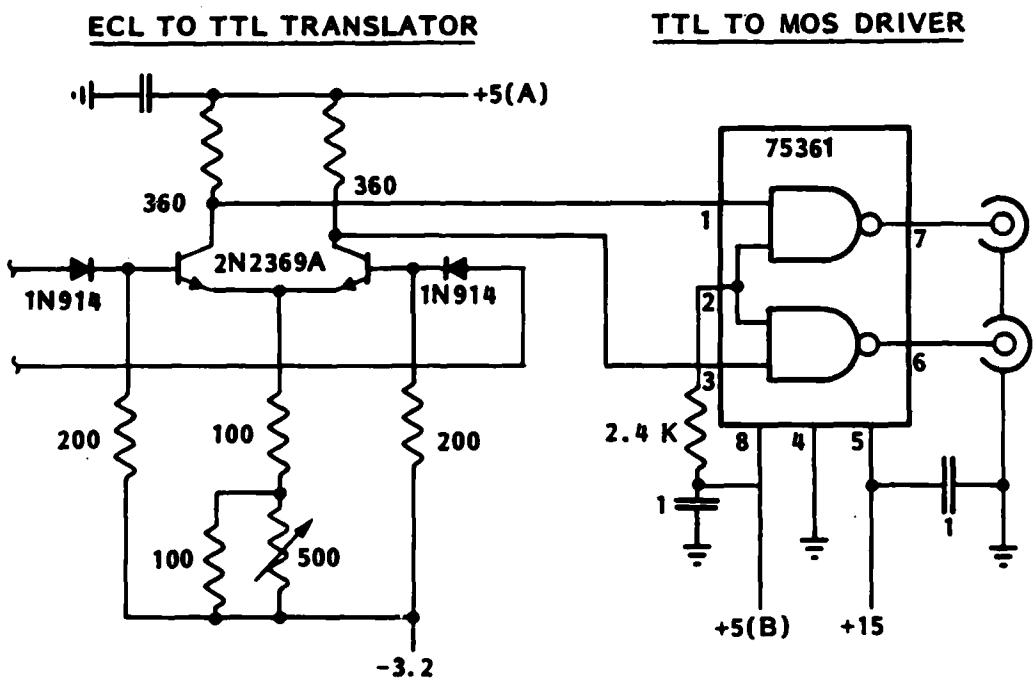

Figure 3 20-MHz Clock Driver Circuit

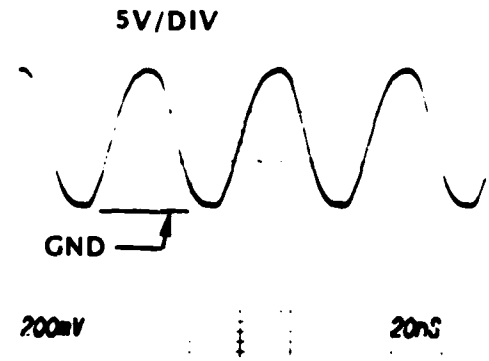

Figure 4 Clock Waveform at CCD Input Using 20-MHz Clock Driver Circuit

Using the approaches outlined in Section 2.1.1, even allowing for substantial reductions in clock bus capacitance and drive voltage requirements in CCDs designed for higher frequencies, the power level required becomes formidable. We therefore devoted some effort to the development of a clock driver concept capable of fast/slow switching that would show more favorable frequency-scaling properties.

The concept developed is illustrated in Figure 5. In essence, the circuit is a tuned amplifier, with the tank circuit containing a series step-recovery diode (SRD). With a relatively modest DC forward bias current, the SRD can be maintained entirely within its high-conductivity operating region even with relatively large circulating RF currents passing through it. This is so because stored charge in the junction built up over charge storage lifetimes of typically hundreds of nanoseconds is available to provide the conductivity during the reverse half-cycles of the RF, while the forward half-cycles return to the junction most of the charge extracted during the reverse half-cycles. During the high-speed writing of data into the CCD, then, the Q of the tank circuit greatly reduces the required input power from the driving transistor.

When the time for the transition to low-frequency readout of the data arrives, an avalanche transistor, fired in synchronism with the master clock, can be used to remove the stored charge from the SRD. By the proper adjustment of the timing, the SRD may be made to snap into its high-impedance mode at the peak of the voltage waveform on the tank, when the inductor current is zero. This "catches" and stops the oscillation with all of the charge resident on the capacitance of the CCD clock bus. Low-frequency, low-power auxiliary circuits can then take over the task of the low-speed readout of the CCD data.

While no experimental version of this circuit has yet been built, previous work in this laboratory has demonstrated that the key timing requirement for the snap-off can be met with stability of the order of 1 psec. The limitations on frequency scaling of this curcuit are therefore expected to lie in the achievable tank Q and in the deviations of the impedance of the CCD clock lines from pure capacitance at higher frequencies.

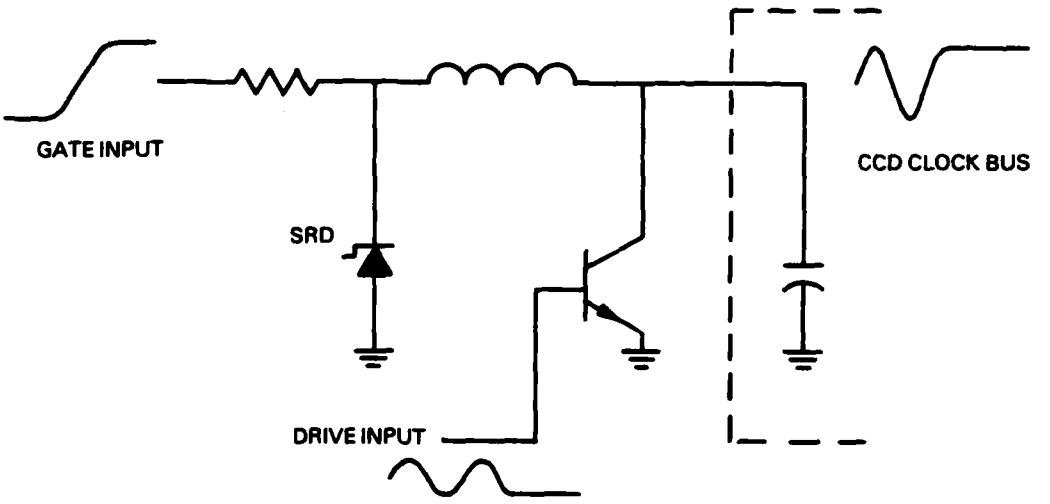

Figure 5 Simplified Schematic of Tuned "Catcher" - Type Clock Driver Circuit

Figures 6 and 7 show more detailed circuit diagrams of the catcher concept, in versions which catch the tank voltage at high and low levels, respectively, as required for a two-phase CCD drive. These figures show the SRD, tuning inductor L, equivalent CCD bus capacitance, and drive transistor on the right in each case, and the avalanche transistor (Q1) on the left. As is indicated, the same avalanche transistor would be used for both phases, simplifying triggering.

The added circuitry in each figure serves to shift the operating biases of the SRD and the driver transistor from values suited to high-frequency tuned operation to those required for low-frequency operation with resistive biasing. Referring to Figure 6, the Gate 2 input to transistor Q3 serves to switch the forward bias of the SRD off for the low-frequency mode. In Figure 7, a similar function is provided by Gate 4 and transistors Q7 and Q8.

In Figure 6 again, Gate 1 and Q2 serve to bypass bias current from R2 during high-frequency operation, so that Q4 is biased through D2 and L1 at approximately half the peak-to-peak level of the bus waveform. After snap-off occurs, Q2 is turned off, so that R2 becomes the load resistor for Q4. In Figure 7, high-frequency-mode bias is supplied via D4 and L2, while low-frequency operation is biased via R3. Gate 3 and transistors Q5 and Q6 serve to switch between these two modes. Note that the switching time requirements on the gates are not at all severe, since the full duration of the avalanche current pulse is available before the resistive bias is needed.

Diodes D1 and D3 serve as clippers, to bypass any excess avalanche current to the supply buses and minimize overvoltage transients during the snapoff process. Finally, we comment that all diodes except the SRDs should be fast Schottky types. Aside from the tuning inductors, the remaining component values are relatively non-critical.

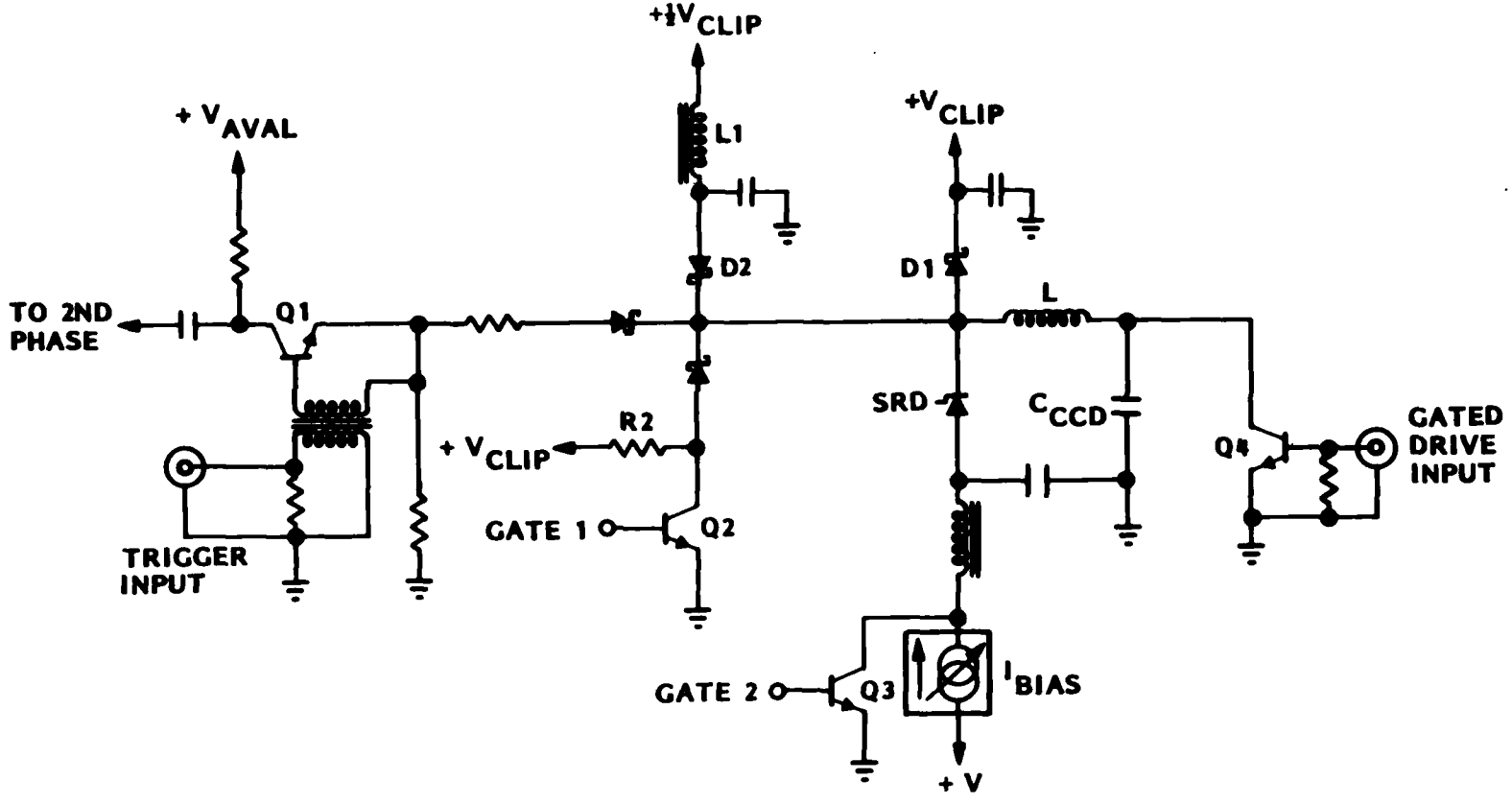

Figure 6 Tuned Driver Circuit Phase 1 - First Slow Clock Phase is High

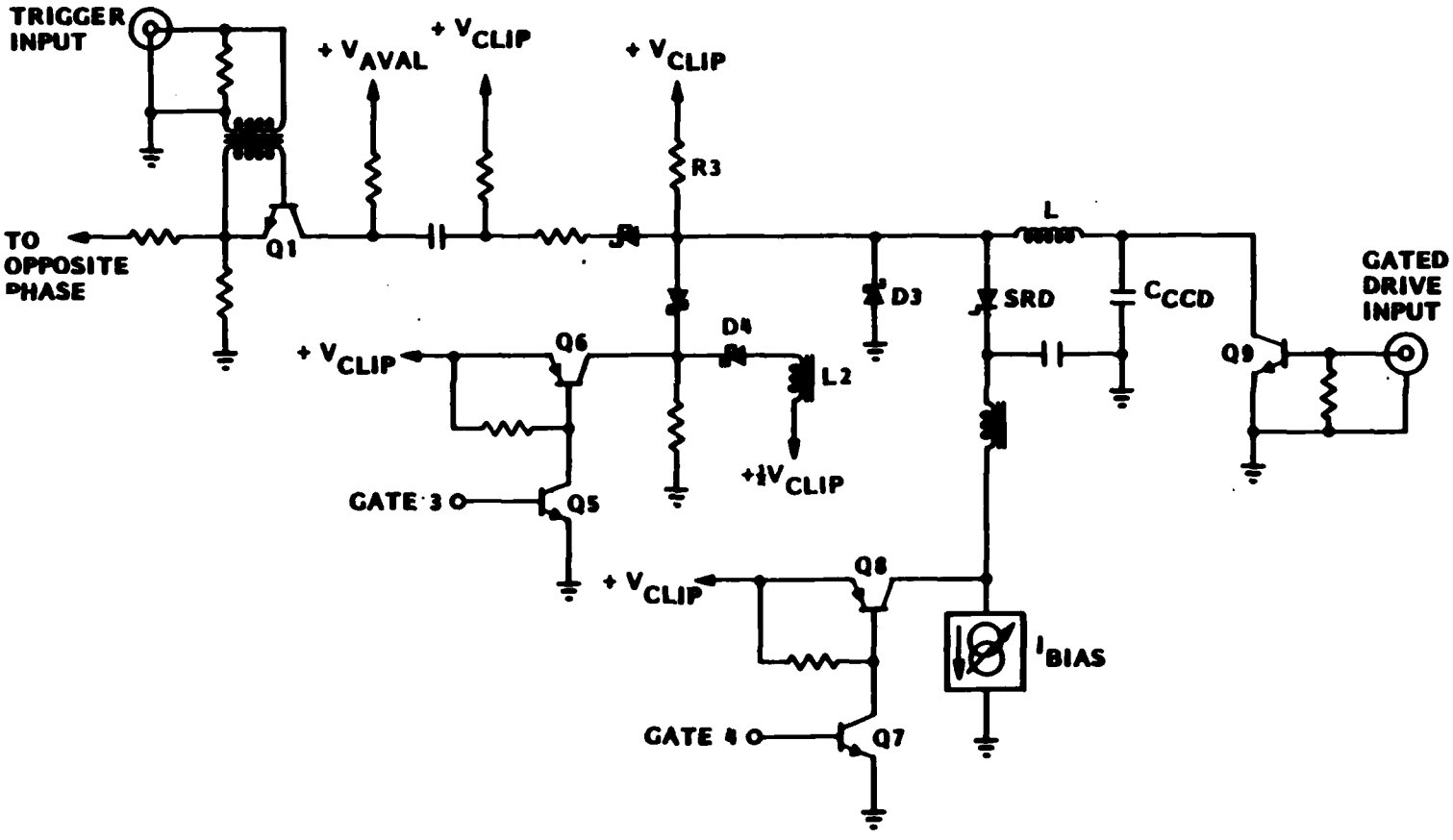

Figure 7 Tuned Driver Circuit Phase 2 - First Slow Clock Phase is Low

SECTION 3
SYSTEM DESIGN AND CONSTRUCTION

3.1 DESIGN PARAMETERS AND SYSTEM ARCHITECTURE

We give here a brief recapitulation of the critical factors which determined the system design. The major choice was that the requisite analog sampling rate be achieved by demultiplexing the input signal into an array of commercially available CCDs as shown in the block diagram of Figure 8. A nominal 160-MHz sampling rate is achieved using four Fairchild FCCD321A dual 455-element registers at a basic clock rate of 20 MHz, which we have determined is the maximum practical drive rate for these chips.

The minimum readout rate is determined by the maximum charge-retention time of the chip, and is about 40 kHz for the entire register. To allow independent readout of any number of channels onto a single digital data bus without loss of data, and without saturating standard microcomputer technology, individual integrated-circuit (IC) analog-to-digital converters (ADCs) are used for each dual CCD register chip, multiplexed between the two channels of the chip, and the results stored in memory within the DAS module for later readout on the bus. This is also illustrated in Figure 8.

A more detailed block diagram of a single DAS module is given in Figure 9, showing signal and control flow, major components of the controller and memory systems, and the interface to the main-frame data bus. While the high-speed clock and trigger control system is hard-wired,and necessarily quite closely tailored to the drive requirements of the CCDs the low-speed controller is PROM-driven, using a standard microprogram sequencer. This allows great flexibility combined with considerable sophistication of operation built into the firmware of the module. Among the features of the firmware are automatic baseline acquisition and a calibration mode, both controllable from the external computer bus.

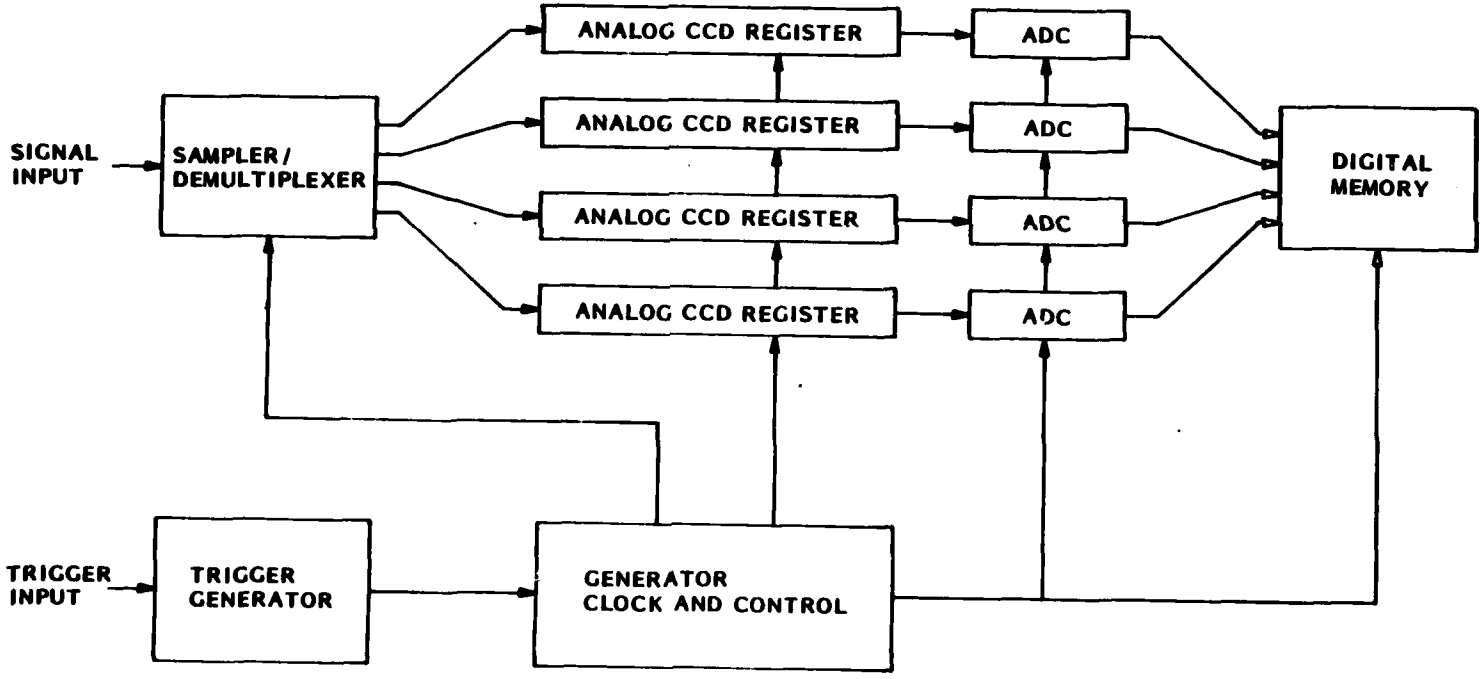

Figure 8 Module Block Diagram

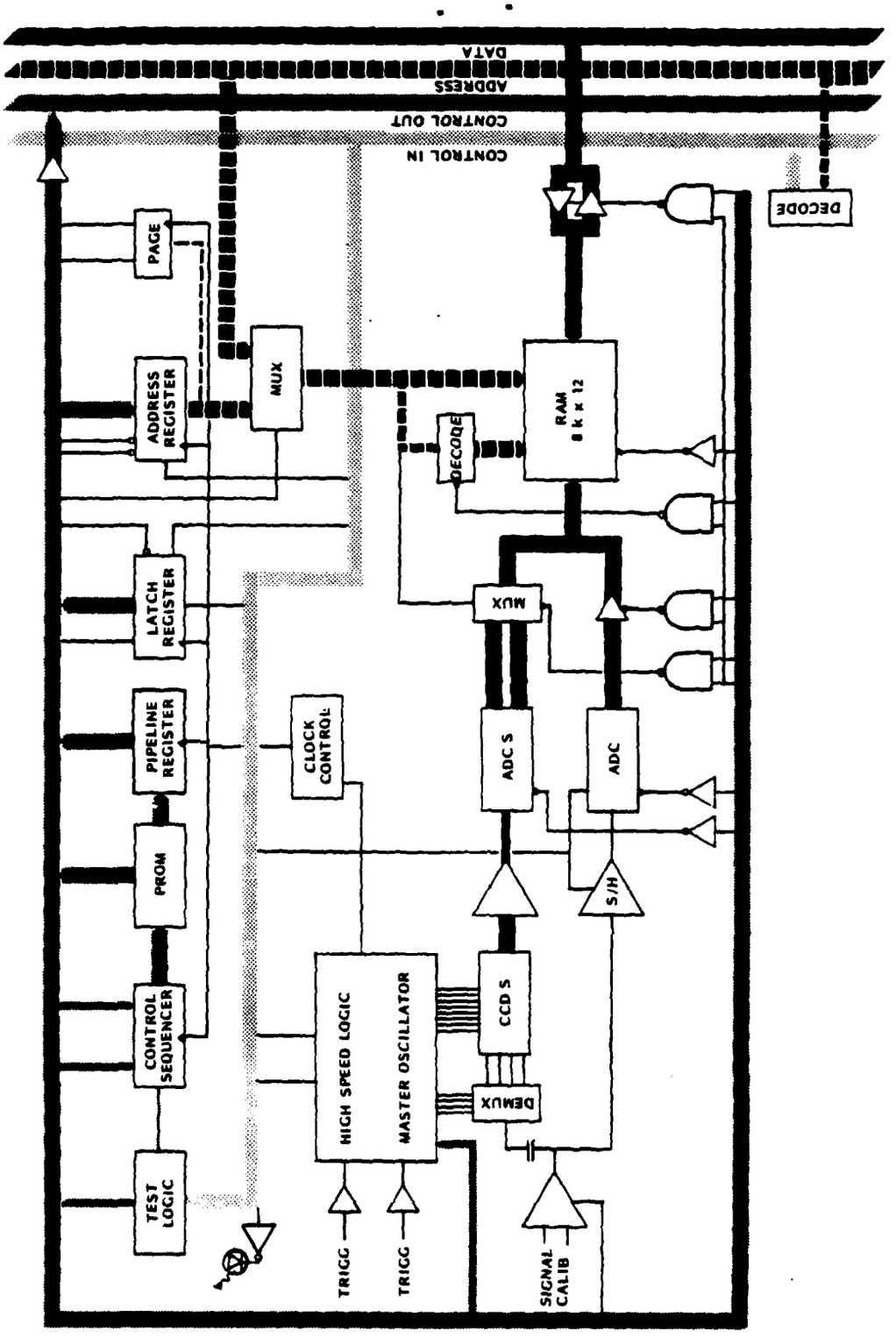

Figure 9 Detailed Block Diagram

Communication with the external control and data-processing computer is via a data and control bus permitting direct read and write of the DAS module memory by the external computer. A 16-bit address bus is used, the three most-significant bits of which are used to address one of eight modules in the DAS mainframe, the remainder serving as module memory address lines.

Two 16-bit I/O ports of a minicomputer are used in our particular interface implementation. One output port is dedicated to the address bus. Since the DAS data bus is 12 bits wide, four bits of the second output port may be used for command and handshaking functions while still allowing a full 12-bit write to the DAS.

The system design parameters are summarized in the following table:

- o 160-MHz maximum sampling rate
- o 22.75 microsecond maximum time window at full rate
- o > 8-bit data word
- o 10-bit data word
- o Post-trigger capability
- o Main-frame capacity 8 modules
- o Firmware automatic baseline subtraction and calibration modes

3.2 PROGRESS IN LAYOUT AND CONSTRUCTION

As stated in the introduction, the primary goal of the program has been to evaluate the general technological problems associated with fast data-acquisition systems utilizing CCDs. A secondary goal, not actually realized, was to generate a working 8-channel DAS capable of sufficiently high performance to have useful applications in the field. Because of problems encountered in the actual layout and construction of the 8-channel system, it was not possible to complete the system within the program cost without compromising the primary goal and settling for much lower performance parameters. This would have generated a completed system with perhaps some limited utility, but would not have made any significant contribution to the ultimate goal of a really satisfactory fast DAS. For this reason it was decided to retain the original performance parameters and to work towards a solution of the attendant problems introduced into system layout and construction.

The physical layout of the DAS system is detailed in the next sequence of figures. The main-frame, containing power supplies, cooling fan, and a small computer interface board, is designed to occupy 8 3/4 inches of standard rack space. Aside from a narrow panel containing the main power switch and three manual control buttons, the entire width of the main-frame is devoted to eight DAS module slots. This is illustrated in Figure 10. In Figure 10a, one module is shown partly inserted into its slot, while Figure 10b shows the main-frame with modules removed. The module connectors and interface bus are visible at the rear.

Figure 11 shows the rear of the chassis, first fully assembled (Fig. 11a), and then with the 5-volt power supply laid back for access to the bus structure (Fig. 11b). Note the ribbon cable daisy-chain construction of the bus.

Figures 12a and b show the two sides of the first module in its present state of construction, with the covers removed. Our original single-CCD breadboard has been mounted in the location designed for the main analog board for testing of the remaining sections of the module. All boards are mounted on standoffs to the central septum plate that forms an interstage shield and the mechanical backbone of the module.

Figure 13 shows detail of the left front section of the module, including the high-speed control board and the input signal conditioning board mounted on the front panel. Figure 14 shows the final version of the analog board, with one of the four CCD sections complete, and the high-speed demultiplexer installed in the center. The remaining three CCD sections fit in the three remaining quadrants of the board.

As is evident from the Figures, both sides of the module are fairly well filled by boards. Because of the module width restrictions arising from the DNA-requested 8-slot main-frame format, there is not sufficient room to put standard wire-wrap boards on both sides of the module septum. For this reason, insulation-displacement-contact (IDC) integrated-circuit sockets were used, a fairly recent introduction by the 3M Company. Among the advantages of these sockets is a compactness of construction that allows the resulting boards to fit easily within the available space.

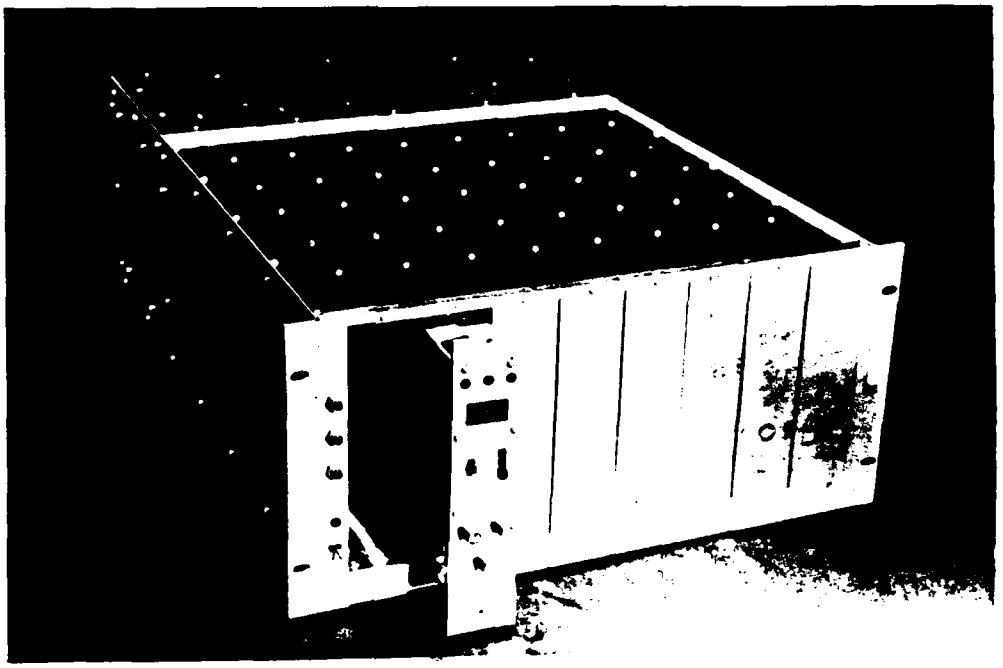

Figure 10a DAS Mainframe with One Module Installed

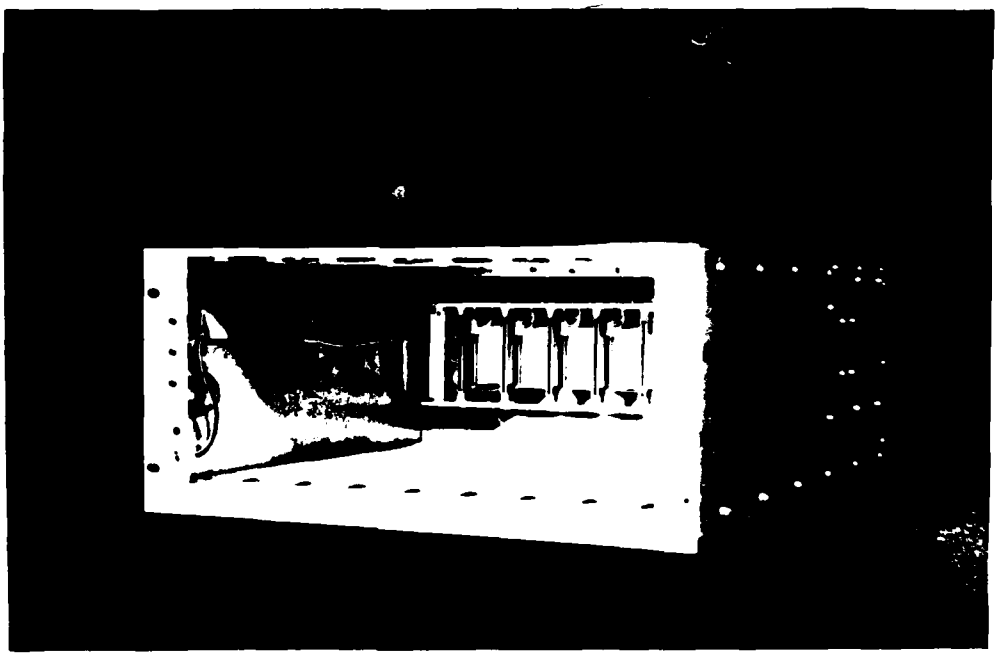

Figure 10b DAS Mainframe Front View

Figure 11a DAS Mainframe Rear View

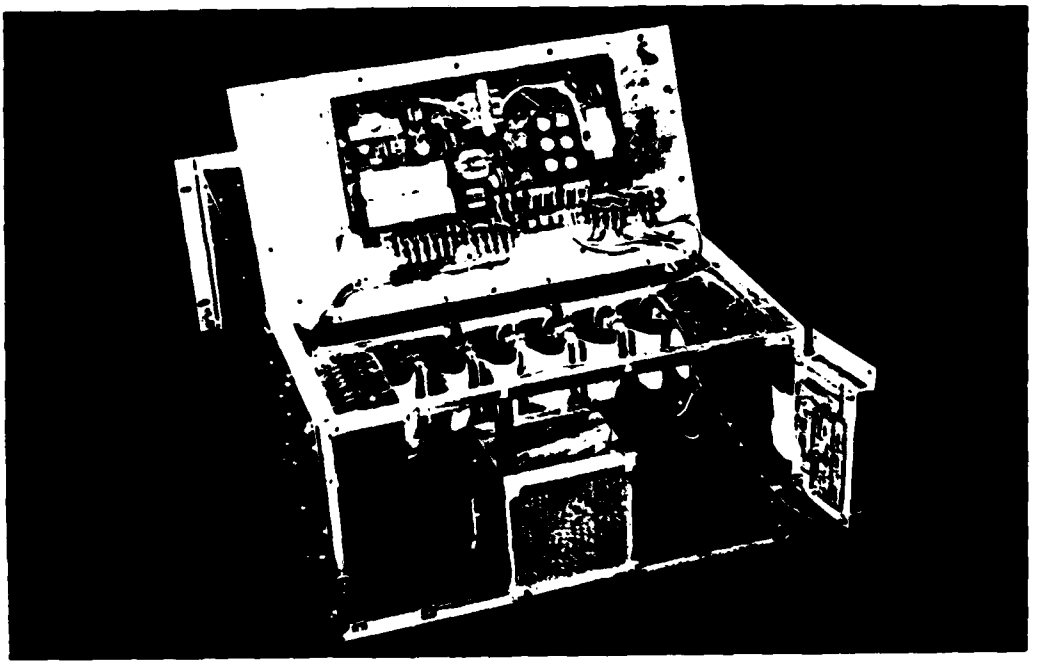

Figure 11b Rear Access to DAS Mainframe

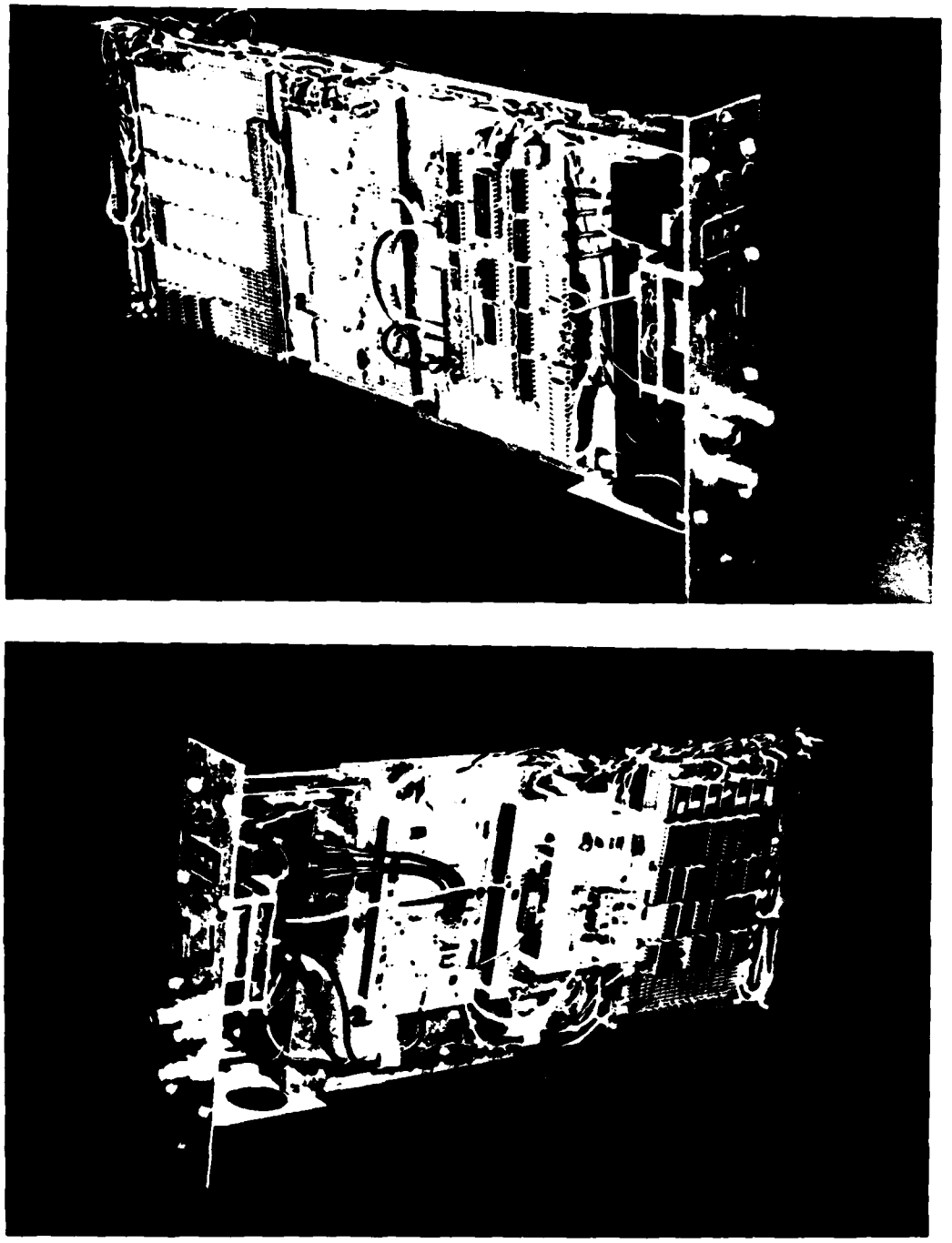

Figure 12 Present Condition of First Module

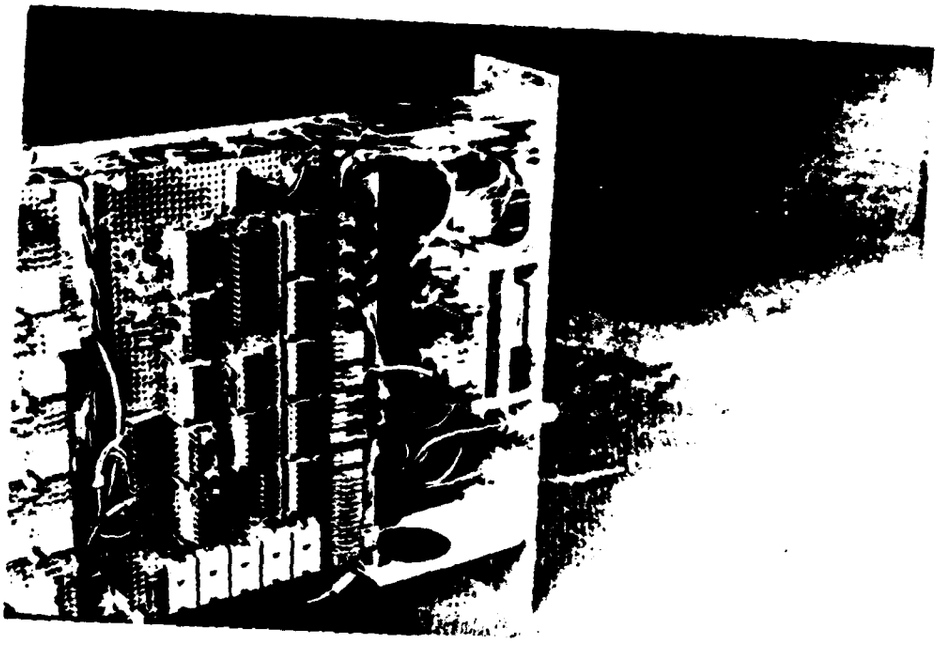

Figure 13 Detail of Input and High-Speed Controller Sections

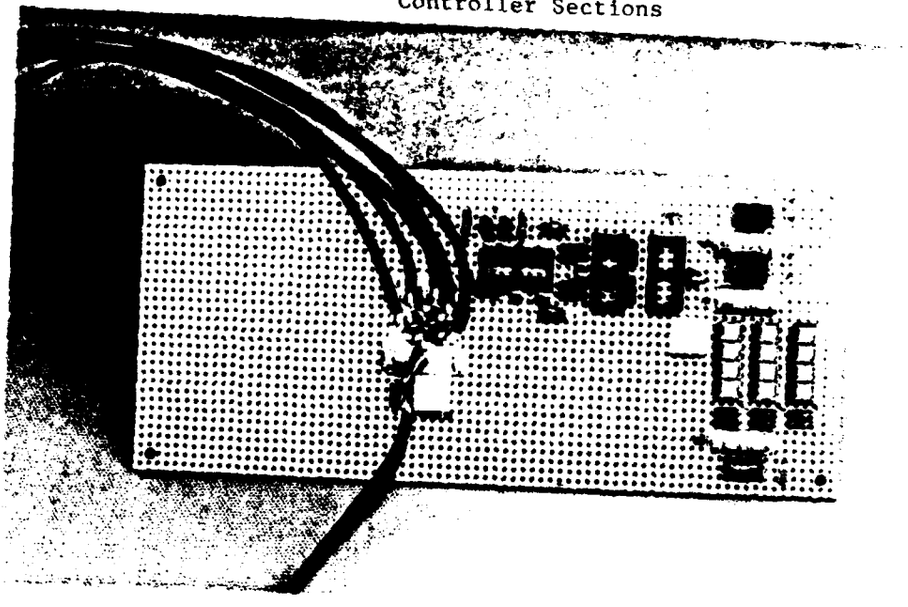

Figure 14 Partially Completed Analog Board

3.2.1 The Socket Reliability Problem

Of the various types of construction one might consider for a brassboard system of this level of complexity, the insulation-displacement contact (IDC) is unique in its combination of compactness, ease of construction, and--most importantly--ease of modification. We have found that in some circuit configurations, especially highly bus-oriented systems, construc using IDC systems may approach a factor of 5 greater speed than a similar wire-wrapped circuit. We also find that the continuous wire runs characteristic of the IDC system are considerably easier to document than the many short wires of the wire-wrap approach.

Figure 15 shows two types of IDC systems. In Figure 15a, we see the two-piece contact structure of the 3M Scotchflex IDC socket. The IDC forks are carried on contact tails molded into carrier strips. The sockets are assembled by pushing the contact tails through 0.043-inch holes on 0.1-inch centers in the circuit board and into receptacles in the under side of the socket body, on the other side of the board. The resulting system is extremely convenient to use.

Unfortunately, we find that the contact within the original 3M socket body is made of too soft a material, so that the circuit through the socket body becomes intermittent rather easily. As a result, these sockets may be suitable for small breadboarding applications, but they present an intolerable reliability problem for any application requiring more than a few sockets. We are not alone in this conclusion. The manufacturer has recently revised the socket body and contact material in response to similar complaints from other customers.

It should be emphasized that we have had no problems whatever with the insulation-displacement fork contacts themselves. Therefore, the arguments for the use of IDC contacts remain the same: compactness, ease of documentation, rapid modification, ease and low cost of construction. In view of the 3M socket upgrade, the most economical approach to correcting the present DAS reliability problem is to replace the existing socket bodies directly with the upgraded 3M sockets. We have verified that this can be done easily without disturbing the existing wiring, thereby minimizing the cost of the repair.

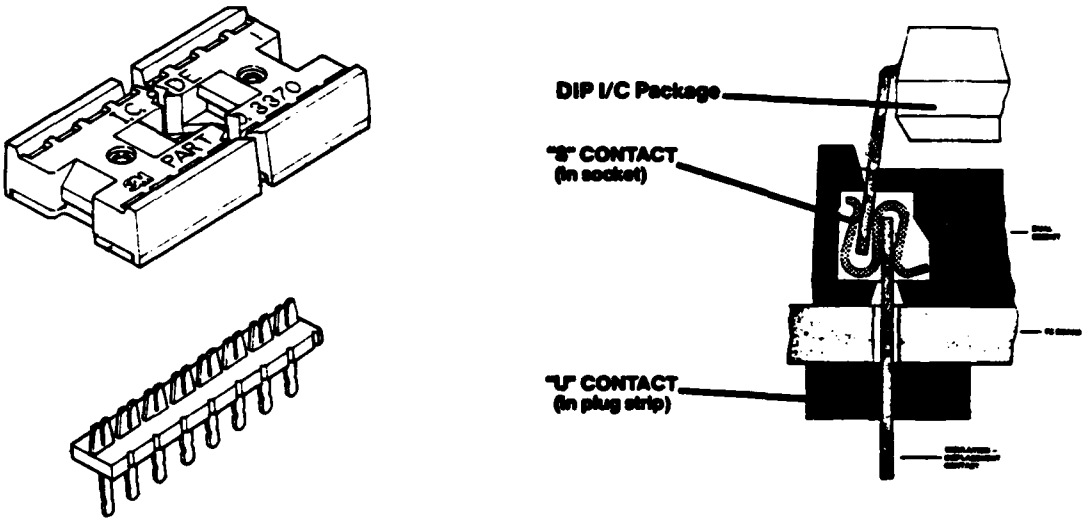

Figure 15a 3M Insulation-Displacement Sockets

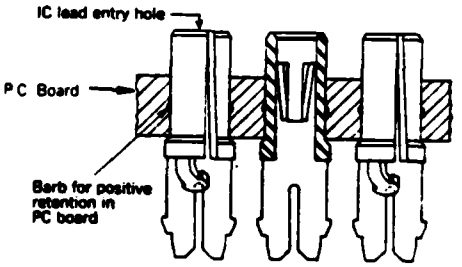

Figure 15b Robinson-Nugent Insulation-Displacement Contacts

For applications in the field, it may ultimately prove desirable to take further steps to increase the reliability of the socket contacts. This could be accomplished by replacing the Scotchflex sockets with Robinson-Nugent press-in IDC contacts, which are of high-quality one-piece construction, with hard beryllium-copper IDC forks and integral IC socket contacts. These contacts are illustrated in Figure 15b.

3.2.2 Present Status of Construction and Checkout

The construction status of the DAS may be summarized as follows:

- o The main chassis is complete and operational, including the computer interface bus and bus control board.
- o Sheet metal parts for all eight modules have been fabricated.
- o Module 1 has been completely constructed except for the final version of the analog board, which has been laid out and one CCD section constructed.
- o With the exception of the final version of the analog board, boards have been completed and wired for Module 2. but have not been installed on the module chassis. Some wiring corrections made during the checkout of Module 1 have not yet been made to the Module 2 boards.

Checkout of the main-frame of the DAS is complete, and checkout of one module is approximately 75% complete. The sub-systems checked include

- o The input amplifier and gain control
- o High-speed logic board
- o Controller board functions and controls--minor corrections to the PROM-resident firmware remain to be made and checked
- o Memory address register functions

Addtional checkout is required for the following subsystems:

- o Memory read/write functions
- o ADC board
- o Analog board

3.3 SUMMARY AND FUTURE POSSIBILITIES

The progress achieved to date has indicated the workability of the basic DAS design and its compatibility with future ultra-fast CCD development.

To provide an operating instrument and a useful basis for future development, it would be necessary to complete at least one module using the improved 3M sockets. After completion of the socket replacement, a short experimental test series would be carried out using the existing single-chip CCD breadboard as a substitute for the analog board. This series would be the first opportunity to obtain really reliable data on the system performance ultimately obtainable, and would permit making any necessary changes to the design of the analog board before finishing construction. We would then complete the analog board with any required corrections, and carry out tests of the full system.

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