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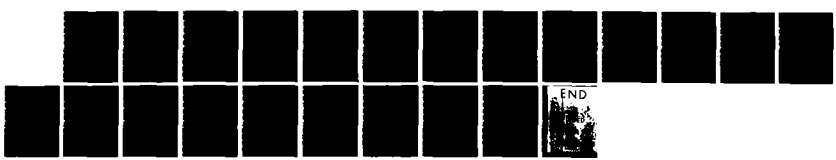

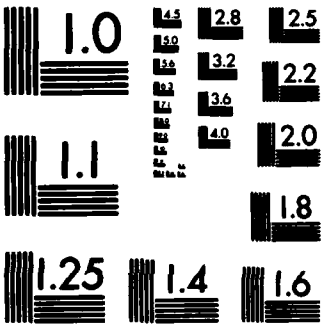

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The objective of this project was to fabricate multiple heterostructure bipolar transistors in semi-insulating GaAs substrates. During the first year of effort, molecular beam epitaxial growth of doped aluminum-gallium arsenide (AlGaAs) gallium arsenide (GaAs) heterojunctions was carried out. GaAs layers were doped n-type with silicon from the background (1E16) up to 2E18 and p-type with beryllium up to 1E19. N-type AlGaAs was grown up to 30% aluminum composition and doped with silicon to 1.5E18. Tools were developed for lateral structuring of transisitors such as beryllium ion implantation, reactive sputtering and thermal annealing. Single devices were grown, fabricated by mesa etching and tested. Current-voltage characteristics shows evidence of excess recombination current.

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Annual Technical Report. Grant No. AFOSR-82-0344

Development of a Planar Heterojunction Bipolar Transistor for Very High Speed Logic

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ABSTRACT

The objective of this project was to fabricate multiple heterostructure bipolar transistors in semi-insulating GaAs substrates. During the first year of effort, molecular beam epitaxial growth of doped aluminum-gallium arsenide (AlGaAs) gallium arsenide (GaAs) heterojunctions was carried out. GaAs layers were doped n-type with silicon from the background (1E16) up to 2E18 and p-type with beryllium up to 1E19. N-type AlGaAs was grown up to 30% aluminum composition and doped with silicon to 1.5E18. Tools were developed for lateral structuring of transistors such as beryllium ion implantation, reactive sputtering and thermal annealing. Single devices were grown, fabricated by mesa etching and tested. Current-voltage characteristics shows evidence of excess recombination current.

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1. RESEARCH WORK STATEMENT

In this research project, efforts are being directed toward the fabrication of heterojunction bipolar transistors in the (Aℓ,Ga)As/GaAs and the (In,Ga)P/GaAs material systems. Emphasis has been placed on growth and characterization of the above heterojunctions by Molecular Beam Epitaxy and on the development of techniques for horizontal patterning and definition of single and multiple transistor structures on semi-insulating GaAs substrates. Transistors are to be characterized for dc and, if successful, dynamic or ac performance. Specific details relating to these general tasks are outlined below.

1.1 MBE Growth on Non-Integrated HBT Structures

This first objective consists of a learning phase, where the more familiar (Aℓ,Ga)As/GaAs material system is used to fabricate discrete single heterojunction bipolar transistor structures. Conventional mesa-etch techniques will be used for isolation and exposure of the base region for contacting. Characteristics of the wide-gap emitter junction will be determined, and transistor action will be evaluated. These initial studies will help to provide insight into HBT fabrication requirements and will provide an initial baseline against which the results of subsequently fabricated more complex devices and material systems can be gauged.

1.2 MBE Growth of InGaP on GaAs

The second objective will be to investigate MBE growth of InGaP on GaAs and GaAs on InGaP. This will include:

a) Pre-MBE Substrate Preparation. The effects of various surface treatments such as chem-mechanical polishing, chemical etching, and in-situ anneal-

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ing on subsequent epitaxial deposition will be systematically studied. It is expected that procedures similar to those already developed for GaAs/GaAs or GaAs/(Aℓ,Ga)As growth will be applicable.

b) MBE Growth Parameters. The influence of substrate temperature and P_2 flux on the epitaxial InGaP layer quality will be determined. This includes specifically a determination of the interrelation between Ga and In source temperatures to yield the correct Ga:In flux ratio for lattice matching. At a later stage, coaxial sources will be developed, possibly also mixed sources. In-situ RED patterns can be of value in monitoring initial nucleation and post-nucleation structural changes. Photoluminescence measurements can be used to determine composition and evaluate interface strain (related to peak width) Auger analysis and sputter-Auger profiling can also be employed to determine composition of the film.

c) Electrical Properties. Conductivity and Hall effect measurements at temperatures from above room temperature down to at least liquid nitrogen temperature will be performed to evaluate the quality of deposits. Both isotype and anisotype heterointerfaces will be evaluated by: (1) I-V measurements vs. temperature; (2) C-V measurements, either through self-capacitance of the heterojunction or by profiling through the interface from an adjacent p-n junction or Schottky barrier.

1.3 Horizontal Definition of Transistor Structures

The third objective will be to fabricate heterojunction and double-heterojunction bipolar transistor structures on semi-insulating GaAs substrates while evaluating a variety of techniques for horizontal isolation and patterning of transistor islands. Some parts of this task can be carried out in parallel with the MBE growth task. This task includes:

a) Ion Implantation into InGaP and GaAs. Both p-type doping of InGaP and isolation by bombardment with protons or B^+ or O^+ will be evaluated. Beryllium as a p-type doping species is expected to be effective in achieving high levels of net acceptors in (In,Ga)P. Investigation of the electrical isolation achievable by ion implantation will involve study and electrical characterization through appropriate test structures. The effect of: (1) damage species; (2) implant conditions (energy, dose, temperature); (3) post-implant annealing will be explored. Annealing caps such as Si_3N_4 will be evaluated for activation efficiency of the Be-dopant. Conductivity and hole mobility will be measured.

b) Low Resistivity Contacts for Base and Emitter. While familiar metal systems such as Au-Ge/Ni/Au and Au-Zn are known to provide adequate contact resistance on n+ and p+ GaAs respectively, the advantages of a self-aligned structure which could come from a single contact metallization are great. Therefore, alternatives such as grading and lower bandgap surface layers may be explored as time permits.

c) Selective Epitaxy. The applicability of epitaxial growth in localized surface areas for isolation amd patterning of transistor structures will be determined. Growth of InGaP on GaAs or GaAs on InGaP will be attempted in selected surface regions using Si_3N_4 or polycrystalline Ge as a growth-masking material. Patterning of the work materials will be accomplished by plasma etching. The morphology and electrical characteristics of these locally-grown layers and their interfaces will be evaluated and optimized experimentally. Methods for surface protection (such as polycrystalline As) will be developed if needed.

d) Fabrication of HBT Test Structures. Heterojunction bipolar transistors will be defined in the MBE-grown epitaxial films by conventional methods

(photolithography, mesa etching) for the purpose of providing transistor-like structures for testing. These devices will be used to evaluate (1) injection vs. interface recombination currents (HJ emitters); or (2) band edge discontinuities and interface charges (collectors).

1.4 Device Characterization and Optimization

Demonstration devices that are fabricated by the first three tasks will be fully characterized for all dc parameters. The injection efficiency, the common-base current gain α, and common emitter current gain β, will be measured as a function of temperature, bias conditions, and doping levels in the emitter and base. Critical evaluation of the comparative advantages and disadvantages of both (Aℓ,Ga)As/GaAs and (In,Ga)P/GaAs material systems and their device performance will be carried out. Other material systems might also be evaluated, but only if the (In,Ga)P performance would suggest the need for further exploration. Both single and double HBTs will be fabricated and characterized if possible.

2. Status of Research

In the following sections, work which was initiated during the first year of this project is described and reviewed. Some of the most significant areas of accomplishment include the following: 1) MBE growth of (Aℓ,Ga)As, (In,Ga)P* and the ion implantation of Be were performed for the first time in the UCSB/ECE Solid-State Lab in accordance with the goals of the project. 2) A capability for DC sputtering of metals, RF and reactive sputtering of dielectric materials such as SiO_2 and Si_3N_4 in a clean vacuum system was established. 3) A very flexible and versatile annealing system was designed, equipment was obtained through project funding, and construction of the system was initiated.

2.1 MBE Growth of (Aℓ,Ga)As and HBT Device Design (B. Hancock)

At the beginning of this contract, the growth of undoped GaAs was well established in our laboratory. Typical growth conditions are a substrate temperature of 560°C, a growth rate of 0.5 micron/hour, and an atomic flux ratio of 3 from a dimeric arsenic source. This generally results, for our system, in a background concentration of approximately 1E16 n-type. This relatively high background probably comes from germanium, which is also grown in our system.

A structure was designed to be used as our first device goal. It is shown in Fig. 1, with the associated band diagram in Fig. 2. The n+ substrate serves as the external emitter contract. The first, heavily-doped, graded layer serves to make the contact to the wide-gap emitter layer ohmic. The

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* Because the initial studies of (In,Ga)P/GaAs heterojunction growth by MBE were supported on another grant, the current status of this work will be reported in a separate section (5). This work is being discussed in this report because of its relevance to the objectives of the AFOSR project.

undoped graded layer, bounded on both sides by heavily-doped layers, eliminates the heterojunction spike which would greatly reduce the injection efficiency. The base is heavily doped to reduce series resistance. An undoped collector region is included to improve the breakdown properties, followed by a heavily doped region to facilitate ohmic contact. Finally, there is a contact layer, described later, to further improve the quality of the collector contact. The wide-gap region under the base contact must be doped p-type forming a junction with a higher turn-on voltage. This prevents injection into this region, which would lower the gain to the ratio of collecor area to emitter area. The most likely technology for this doping is ion implantation.

In order to build such structures, several problems had to be addressed. p-type doping of GaAs with beryllium was established. Layers with doping from 1E16 to 1E19/cm^3 were grown on semi-insulating substrates and evaluated by Hall measurement. Ohmic contacts were successfully made with Au:5%Zn, alloyed at 420°C for 2 minutes. On the most heavily-doped layers, unalloyed Au made an excellent contact.

GaAs layers were doped with silicon from the background level of 1E16 up to 2E18. These layers were evaluated by C-V measurement.

We have attempted the use of a GaAs:Ge alloy of approximately 30% Ge for ohmic contact to n-type GaAs. This alloy has a band gap of about 0.4 eV and is easily grown epitaxially on the GaAs. Unalloyed gold makes an excellent ohmic contact to this material. Unfortunately, the heterojunction between the alloy and GaAs shows some nonlinear behavior. This could be eliminated by use of a graded transition.

We have grown AlGaAs layers at a variety of compositions up to 40% with substrate temperatures from 620 to 650°C. The morphology has been very good, though there is some slight roughening, as observed by others.

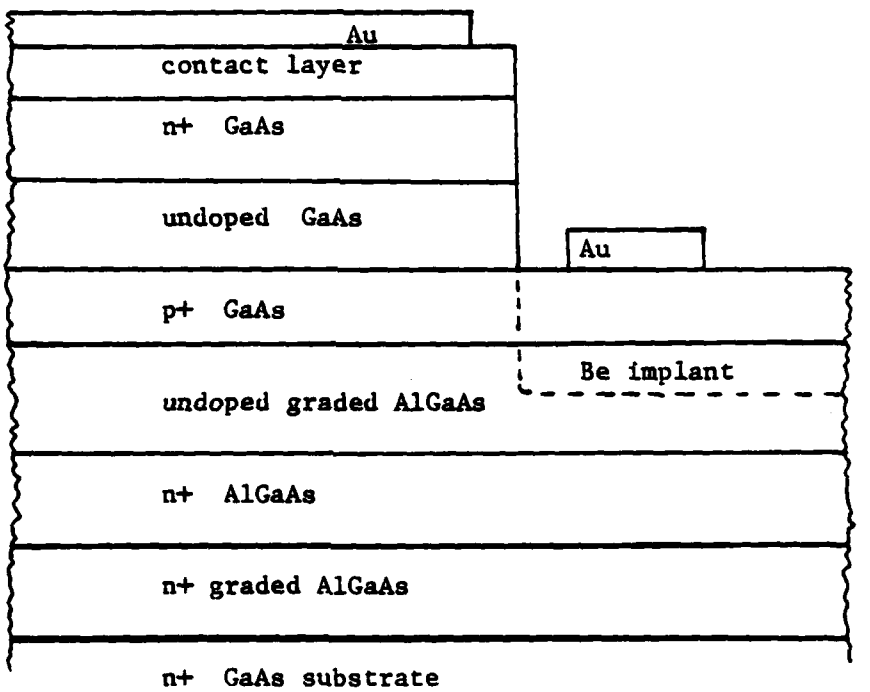

Figure 1. Inverted heterostructure bipolar transistor. Emitter-base junction is graded from 30% aluminum to GaAs which is p+ doped with beryllium.

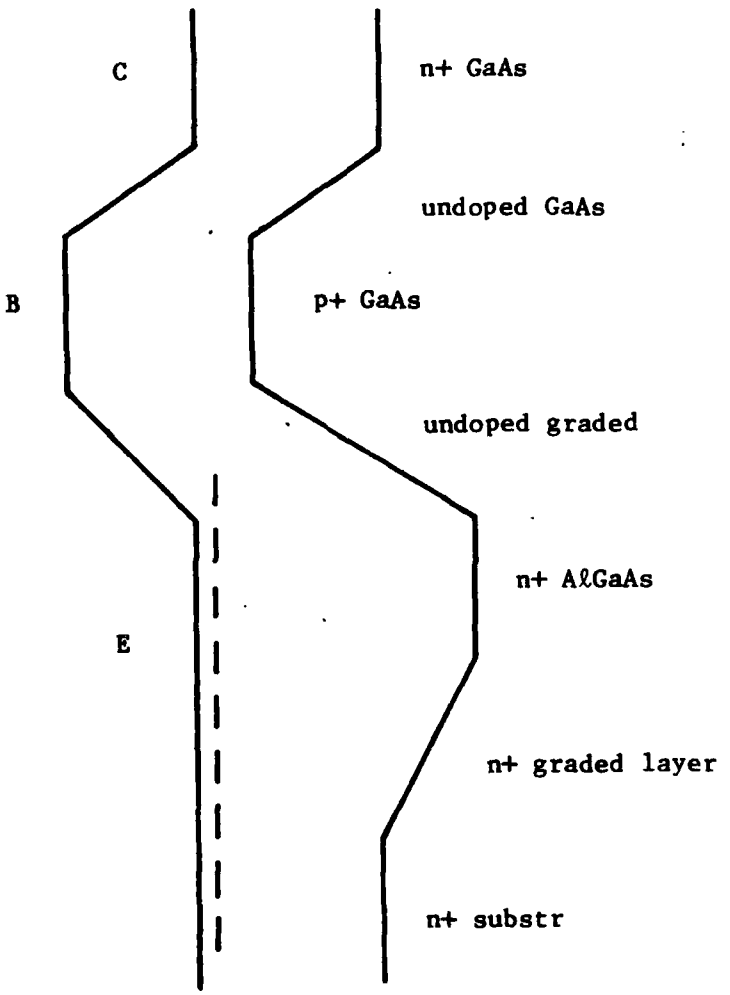

Figure 2. Energy band diagram of transistor structure shown in Fig. 1.

Undoped AlGaAs grown on p-type substrates was observed to be p-type with hole concentrations of 3E15. Photoluminescence confirmed that this is caused by outdiffusion of zinc from the substrate. Diffusion of beryllium out from the base, which is also rapid, is a potential problem. In the inverted structure we have chosen (see Fig. 1), the substrate temperature can be lowered after the growth of the emitter layer in order to avoid excess diffusion into the emitter.

Undoped AlGaAs grown on n-type substrates was semi-insulating, and silicon doping at low concentrations was ineffective. This is probably caused by a deep acceptor-like trap level. Silicon doping at high concentration was less efficient than for GaAs. This may result from the fact that, as reported by others, the silicon level in AlGaAs is deep, reaching 150 meV for 36% aluminum. Nevertheless, we have succeeded in doping AlGaAs n-type up to 1.5E18.

In order to contact the base, it is necessary to etch away the collector, stopping within the narrow base layer. This requires well controlled etching. We have found that sulfuric acid : hydrogen peroxide : water in the ratio of 4:1:35 is a good nonselective etch with good reproducibility. This has given us the necessary control.

Device Results

We have fabricated only a few devices. The most recent show the best results. The collector-base and emitter-base junctions show good characteristics with very sharp breakdowns. Both junctions show photocollection. Because these devices have not been ion implanted, the maximum alpha we can expect is 0.28. However, we only observe an alpha of 0.1. Examining the I-V curves for the emitter-base junction, we find an ideality factor of 1.5. This

suggests recombination in the emitter depletion region, possibly through the deep levels in the AℓGaAs that affect the doping.

Future Plans

By examining the collector and base currents as a function of emitter-base voltage and temperature we should be able to separate injection current from recombination current. We will use this as a tool to evaluate the effects of growth conditions on the injection efficiency. This can also be used to look for outdiffusion of beryllium from the base.

As an alternative to the GaAs:Ge alloy we will also try using a thin germanium contact layer. With the same gold metallization used for the base contact, we can form the traditional alloyed Au:Ge contact. Use of the same metallization may allow a self-aligned base contact if the collector mesa can be made to undercut. This should further reduce the base resistance.

2.2 Ion Implantation Technology (J. Blokker)

The development of the implantation of beryllium into GaAs for contacts to the p-type region of the base in our HJBJT's requires several significant steps. Not only must the ion implanter be adapted for a beryllium source but a suitable form of annealing of the implanted GaAs samples must be developed. This section will describe the progress of the last year and the plans for the future in achieving this goal.

10/82 to 12/82 - Ion Implanter

A beryllium implantation was achieved by the installation of a cold cathode source which has a beryllium sleeve along the outlet hole of the plasma beam. The beryllium is eroded by the plasma and accelerated by the ion

implanter making it easy to tune in a beryllium beam with the mass selecting magnet. To refit the ion implanter to the cold cathode, a new power supply needed to be installed requiring rearrangement of most of the gas supply tanks. Since previous modifications had been made on the electrical system, rewiring of some control leads to the power supplies was also necessary. The result of this effort was a beryllium beam of six microamperes.

Development of Annealing Techniques

The annealing of GaAs poses special problems because of the higher vapor pressure of arsenic than gallium. At the temperature of a typical annealing (850°C), the outgassing of arsenic causes the decomposition of the GaAs crystal. This can be avoided by a number of techniques. The most common technique is using silicon nitride as an encapsulation layer to prevent the outgassing of arsenic and the diffusion of gallium away from the surface of the crystal.

12/82 to 4/83 - Cleaning of the Sputtering System for Silicon Nitride

A system where a previous attempt at sputtering silicon nitride was tried, was taken over for our purposes. The first five months working on this system were spent in cleaning and finding leaks. The entire diffusion and roughing pump setup was taken apart and cleaned. All the metal parts were cleaned in an acid bath and all the O-rings were changed. As a result the final pumpdown pressure of this system reached 3.7 e-7 torr.

4/83 to 6/83 - Development of Sputtering System

During this period a sample holder and shutter were designed and built for the sputtering system. Five samples can be held in each run and each sample can be exposed to two sputter guns and a substrate heater.

6/83 to 9/83 - Aluminum and Silicon Dioxide Sputtering

First, DC sputtering of aluminum was tried to test out the magnetron sputtering sources and the substrate holder. Various argon pressures and input power levels were tried to determine the conditions for the most uniform films. It was found that very low power levels were best because higher power would cause large (1 to 5 micron) balls of aluminum to be spit from the sputter gun making the films unsuitable for use in most micro circuits.

Next, RF sputtering of silicon dioxide was evaluated using a target of quartz in the sputter gun. The new challenge in this setup was the use of the RF generator and matching network. This generator was borrowed from an older system in our lab making it more difficult to use than was expected. After setting up a forward and reflected power meter it was found that most of the power from the generator was used in the fields of the matching network and in heating up the cable. Cutting the connecting cable as short as possible was helpful, but didn't solve the problem. If 500 watts of forward power is received by the gun, 400 watts are reflected making only 100 watts available for formation of the plasma.

Working with these power levels, it was found that the lower the pressure, the denser the silicon dioxide film. This has been explained in the literature as due to the resputtering of the deposited film. Since the deposited insulating film on the sample is in a plasma, and electrons in the plasma move faster than the positive ions, the surface is bombarded by more electrons and charges to a negative potential. The pressure of the gas determines the mean-free-path between collisions of the ions. As a result the lower the pressure the higher the velocity of the ions that hit the surface of the negatively charged film. These high velocity ions redistribute and pack the deposited film into a denser form.

It was found that the best pressure for the deposition of silicon dioxide was at 2×10^{-3} torr. This result was tested first by trying to scratch off the film, then by measuring the etch rate in buffered HF. The best films could not be scratched off and were close to thermally grown oxides in their etch rate. Thicknesses and deposition rates were determined by ellipsometry.

9/83 to 12/83 Silicon Nitride Sputtering

The deposition of silicon nitride films was a much more difficult task. Using a target of pure silicon in a nitrogen plasma, a reaction of the sputtered silicon with the nitrogen can take place to form silicon nitride. It would be best if this reaction occurred at the lowest possible pressure so as to take advantage of the resputtering of the surface to make a denser film. Many samples were run but it was found that at low pressures, micron size blobs of silicon were spit from the target. As the pressure of the plasma was raised the density of the blobs decreased, but the etch rate of the films increased beyond acceptable levels indicating low density and possibly oxygen contamination.

This problem was solved by adding argon to the plasma. The spitting of silicon seemed to be due to arcing between the anode and cathode or due to an unstable plasma at lower pressures. By adding argon, the plasma was much more stable, and the silicon spots on the samples disappeared. It was found that the best results were with 3.4 microns of argon and 0.6 microns of nitrogen. These samples would only etch slowly in buffered HF and had a refractive index of 2.0, the known refractive index of silicon nitride, when measured by ellipsometry.

All tests up to this point were done on silicon samples which behave much differently than GaAs. Adherence of the silicon nitride film to GaAs is known

to be a significant problem. This has been attributed to a difference in thermal expansion of the GaAs and to gallium oxide on the surface of the sample. A substrate heater was added to the system to heat the samples to 300°C for 30 minutes under vacuum to drive off adsorbed gases and to help reduce the oxide surface layer. Also, depositing 1000 angstroms of silicon nitride and then 2000 angstroms of silicon dioxide on top of the GaAs samples is a good recipe for reducing the adhesion problem.

Future Plans for the Development of Annealing

There are many different procedures that have been used for the annealing of beryllium implanted GaAs. Besides the use of a silicon nitride encapsulating layer, capless annealing with an over pressure of arsenic has had great success. Flash annealing of capped and uncapped layers is a popular new technique also. We have designed an annealing system that has great flexibility in being able to test all of these techniques.

At the present time we have most of the necessary parts to construct this annealing system and are in the process of putting it all together. Beryllium implantation and annealing in GaAs samples should begin in early 1984.

3. Publications

No publications or presentations have been prepared or delivered during the first year of this project.

4. Personnel

Prof. Stephen I. Long is the principal investigator. Prof. Herbert Kroemer is the co-principal investigator. Graduate research assistants J. Blokker and B. Hancock are supported by and are the main student contributors to this effort. ECE department staff D. Zak and G. Hauser provided assistance in the solid-state laboratory for development of equipment and facilities.

5. MBE Growth of (In,Ga)P on GaAs (M. Mondry)

Some initial MBE growth studies on InGaP/GaAs heterojunctions were begun at UCSB in 1983 under separate funding.* Because the goals of this MICRO project are complementary and supportive of the AFOSR funded effort, the current status of the (In,Ga)P/GaAs growth activity will also be reported here. This effort has been aimed at resolving the problem of determining the proper flux ratios for the UCSB system. Much attention has been focused at the importance of the precise control of the Ga/In flux ratio with various methods utilized.[1,2] However, in the growths performed, the anticipated problems of nonuniformity of the Ga/In composition over the substrate and the preferential desorption of In from the surface have not been encountered as inferred from the results of photoluminescence studies. The main difficulty has been establishing the proper P_2 to total group III flux ratio for growth at high substrate temperatures (500°-580°C). It has been shown that the high substrate temperature is essential for the growth of undoped material with good electrical properties. Previous work[3-8] though has not directed itself toward refining this issue since only ambiguous system background pressures have been quoted with no indication that phosphorus beam flux measurements were attempted. The problem is compounded by the fact that the low resistivity layers were grown with a P_4 source[8] while the UCSB system possesses a P_2 source in the form of GaP.

Anticipating that the growth kinetics of (GaIn)P would be similar to that of GaP which the UCSB system has been used to study extensively, the P_2 to total Group III flux ratio was chosen for a desired substrate temperature

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* Jointly funded by a "MICRO" grant from Univerity of California, Hewlett-Packard Corp., Rockwell International and Xerox Corp. Prof. H. Kroemer is the principal investigator.

corresponding to the optimum growth conditions determined for GaP.[9] It has been found for the various flux ratios used that the substrate temperature is limited to a lower range than desired (450°-500°C). The electrical properties of the layers range from insulating to very high resistivity which is expected for the growth of (GaIn)P in this temperature range according to the reports of Blood et al. The high resistivity is attributed to the high dislocation density which has been confirmed by morphology studies. Photoluminescence work performed on the layers yield a Ga/In composition in agreement with the composition calculated from the calibrated flux measurements. It is concluded from these efforts that optimum growth conditions for (GaIn)P are more similar to that of InP which requires a substantially higher P_2 flux (10^{-5} torr) for quality growth of InP at 580°C.[10] The requirement of such a large flux might present a problem of phosphorus depletion of the GaP source but this can be overcome by the careful monitoring of the Ga composition of the layers once the basic growth conditions are established here.

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