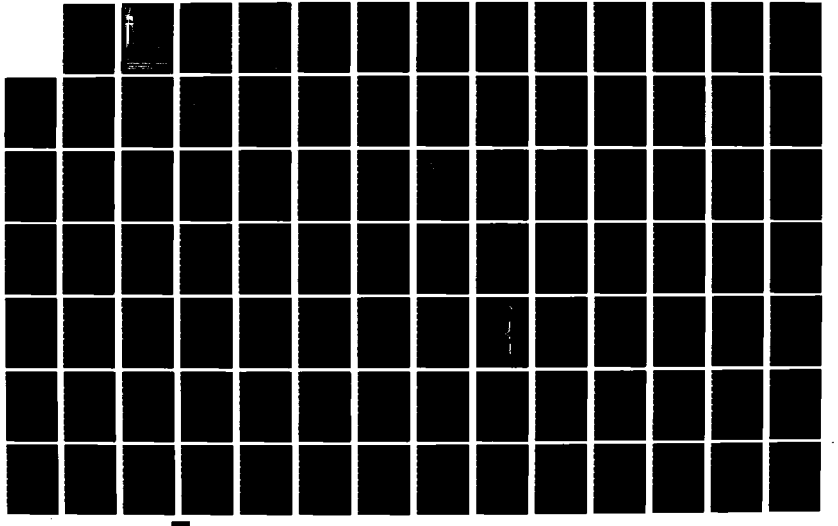
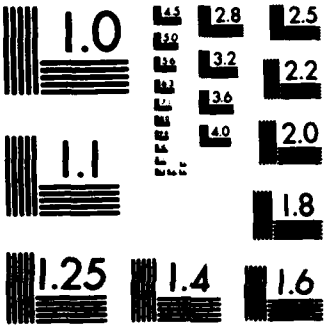
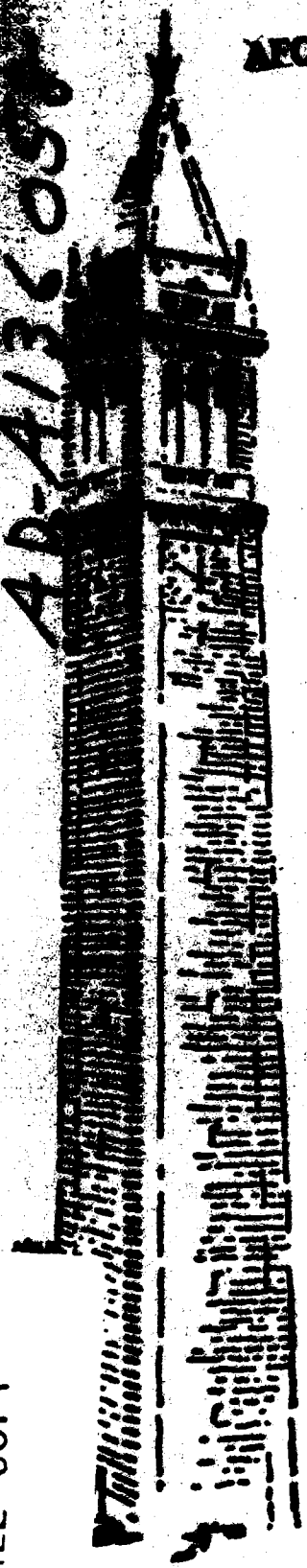
AD-A136 058 JOINT SERVICES ELECTRONICS PROGRAM(U) CALIFORNIA UNIV 1/2
BERKELEY ELECTRONICS RESEARCH LAB D J ANGELAKOS
30 SEP 83 UCB/ERL-83/1 AFOSR-TR-83-1076
UNCLASSIFIED F49620-79-C-0178 F/G 9/5 NL







Report No. UCB/ERL 83/1

JOINT SERVICES ELECTRONICS PROGRAM

ANNUAL PROGRESS REPORT
(Contract F49620-79-C-0178)
(1 September 1982 - 31 August 1983)

D. J. Angelakos

30 September 1983

Approved for public release;
distribution unlimited.

Prepared for

Air Force Office of Scientific Research (NE)
Bolling Air Force Base
Washington, D.C. 20332

ELECTRONICS RESEARCH LABORATORY
College of Engineering
University of California, Berkeley, CA 94720

JOINT SERVICES ELECTRONICS PROGRAM

ANNUAL PROGRESS REPORT (CONTRACT F49620-79-C-0178)

(1 September 1982 - 31 August 1983)

by

D. J. Angelakos

Report No. UCB/ERL 83/1

30 September 1983

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley 94720

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: AFOSR-TR- 83-1076	2. GOVT ACCESSION NO.: AD-A136 058
	3. RECIPIENT'S CATALOG NUMBER:
4. TITLE (and Subtitle): JOINT SERVICES ELECTRONICS PROGRAM Progress Report	5. TYPE OF REPORT & PERIOD COVERED: ANNUAL 1 September '82-31 August '83
	6. PERFORMING ORG. REPORT NUMBER: UCB/ERL 83/1
7. AUTHOR(s): D. J. Angelakos	8. CONTRACT OR GRANT NUMBER(s): F49620-79-C-0178
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Electronics Research Laboratory, University of California, Berkeley, CA 94720	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 61102F 2305/A9
11. CONTROLLING OFFICE NAME AND ADDRESS: Air Force Office of Scientific Research (AFSC) Bolling AFB, DC 20332	12. REPORT DATE: 30 September 1983
	13. NUMBER OF PAGES:
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office):	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE:

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Electromagnetics, solid state electronics: materials and devices, quantum electronics, information and control systems, circuits.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

An annual report of the JSEP (Joint Services Electronics Program) in Electromagnetics, Solid State Electronics, Materials and Devices, Quantum Electronics and Information Sciences is presented. In addition, results of the research to date are summarized and significant accomplishments are indicated.

UNCLASSIFIED

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

1. INTRODUCTION

During the period 1 May 1983 through 30 April 1984, the Electronics Research Laboratory (ERL), University of California, Berkeley, is receiving support for its basic program from the Joint Services Electronics Program (JSEP), sponsored by the Departments of the Air Force (Air Force Office of Scientific Research), Army (Army Research Office), and Navy (Office of Naval Research), under contract F49620-79-C-0178.

This annual report is an updating report; hence it covers the period 1 September 1982 through 31 August 1983. *Significant Accomplishments*, where applicable, appear in the project reports (section A). In particular, the three most significant accomplishments, as determined by the Director, are summarized as:

i. Project **QE-85-1** — Analysis of Integrated-Optics Networks Applied to Semiconductor Lasers.

The interferometric principle of mode control, tuning, or wavelength switching of semiconductor lasers has been firmly demonstrated. Several configurations are possible for this, with an open-ended Michelson interferometer, two versions of a multi-cavity interferometer, and a coupled-waveguide version demonstrated. Stability performance comparable to that of distributed feedback (DFB) or distributed Bragg reflector (DBR) lasers has resulted, with optimization of either stability or tuning analyzed by the scattering-matrix approach.

Two new sets of results not yet published are worth mentioning. First, a continuous wavelength tuning range of 4.5 Å and a quasi-continuous wavelength change over a range of 9.0 Å have been achieved in the integrated-etalon interferometer (IEI) laser under separate pumping. Second, a new multiple-cavity laser, the multiple-twisted (MT) double heterostructure (DH) laser consisting of waveguide segments fabricated on an alternate channeled and terraced substrate has been tested. The MTDH laser showed a mode-stable temperature range 140°C and 25°C in another laser. For both the IEI and the MTDH laser operating in the stable range, a mode-suppression ratio (dominant/side mode) in excess of 100:1 was obtained.

ii. Project **SSM-85-2** — Studies of MBE Growth Kinetics and High-Energy Ion Implantation in Compound Semiconductors.

Our material studies have shown that, using 11 MeV arsenic and 4 MeV boron implantation into Si, buried dopant layers can be fabricated with high electrical conductivity. Ion-beam-induced annealing has been proven to be beneficial to the regrowth of amorphous Si. The damage profile due to implantation amorphization can be understood from the computer calculations of energy deposition profile. The top 2 microns of the surface Si has a lifetime of approximately 2 to 3 microseconds, a value comparable with that of the unimplanted wafer.

Bipolar and NMOS transistors have been fabricated with the high-energy implants. Device performance of both types indicates that the surface layer after implantation is of device quality. The device

structures imply that three dimensional usage of the semiconductor is possible with this high-energy implantation technique.

iii. Project ISS-85-1 — Large-Scale and Nonlinear Circuits Study

Several approaches to solving problems of two layer channel routing have been made.

The first approach is a new method for routing two-layer printed circuit boards with fixed geometry, i.e. alternate columns of pins and vias. Circuit components are mounted on top of the board, and conductor wires are to be laid on the board such that circuit connections can be properly made. The proposed approach gives 100 per cent routability. The method consists of three steps, namely: partitioning of multi-pin nets into 2-pin subnets, via assignment, and routing on the two layers. In comparison with the traditional undirectional routing, the method offers more flexibility and it requires usually about half as many vias. A computer program based on the presented algorithms was written. Its implementation includes testing examples.

The second approach to the 2-layer channel-routing problem allows horizontal and vertical connections on both layers. An order graph similar to the traditional vertical constraint graph is used in the algorithm. The main advantage is that the method is general and is immune to cyclic constraints. Furthermore, the channel width does not have a lower bound equal to the maximum density.

The report contains:

A. 1982-1984 JSEP Projects: as of 31 August 1983

B. Consolidated List of JSEP Published Papers and Memorandums through 31 August 1983

During this time period 1 September 1982 - 31 August 1983, there are currently an additional 17 Journal papers being processed: in *press*, in *review*, *submitted* and being *prepared*. Further, there have been 26 Conference papers presented (or to be presented).

2. RESEARCH PROJECTS

A. *1982-1983 JSEP Projects: as of 31 August 1983*

Project No.	Title and Faculty Investigator
I. *ELECTROMAGNETICS*	
EM-85-1	Conformal Time Domain Finite Difference Methods of Solving Scattering Problems — K. K. Mei and D. J. Angelakos
EM-85-2	Millimeter Wavelength Electromagnetic Structures — S. E. Schwarz, K. K. Mei, and D. J. Angelakos
II. *QUANTUM ELECTRONICS*	
QE-85-1	Analysis of Integrated-Optics Networks Applied to Semiconductor Lasers — J. R. Whinnery and S. Wang
QE-85-2	Electro-Optical Interactions in Quantum-Well Structures: Applications to Detection and Millimeter Mixing — T. K. Gustafson, S. E. Schwarz, and R. M. White
III. *SOLID STATE ELECTRONICS*	
A. *Materials*	
SSM-85-1	Materials Issues in VLSI Interconnectors — N. W. Cheung, C. M. Hu, and W. G. Oldham
SSM-85-2	Studies of MBE Growth Kinetics and High-Energy Ion Implantation in Compound Semiconductors — N. W. Cheung and S. Wang
B. *Devices*	
SSD-85-1	Problems in E-Beam and Optical Lithography — A. R. Neureuther and W. G. Oldham
SSD-85-2	Study of the Effects Limiting Realization of Far-Submicron Superconductive Electronic Structures — T. Van Duzer
SSD-85-3	Studies in Room-Temperature and Cryogenic Heterodyne Detection — T. K. Gustafson and T. Van Duzer
SSD-85-4	Research on Electronic Systems Composed of Polymer Films and Planar Silicon Devices — D. W. Hess, R. S. Muller, and R. M. White

Project No.	Title and Faculty Investigator
SSD-85-5	Wide-Dynamic-Range Signal Processing Using Monolithic Integrated Circuit Technology — R. G. Meyer, R. W. Brodersen, and P. R. Gray
SSD-85-6	High-Field Transport in MOS Devices — C. Hu and P. Ko

IV. *INFORMATION SYSTEMS*

ISS-85-1	Large-Scale and Nonlinear Circuits Study — L. O. Chua and E. S. Kuh
ISS-85-2	Control in Distributed Systems — P. Varaiya and J. Walrand
ISS-85-3	Robust, Adaptive Control and Computer-Aided Design — C. Desoer, S. Sastry and E. Polak
ISS-85-4	Optimization Based Computer-Aided Design of Integrated Circuits — A. Sangiovanni-Vincentelli and R. G. Meyer

B. *Consolidated List of JSEP Published Papers and Memorandums through 31 August 1982*

A. 1982-1983 JSEP PROJECTS

AS OF 31 AUGUST, 1983

University of California — Electronics Research Laboratory

Joint Services Electronics Program — August 15, 1983

I. Basic Research in Electromagnetics — Coordinator: Professor K. K. Mei

Basic research in electromagnetics at ERL presently consists of two parts. One is the development and application of computational techniques to electromagnetics, and the other is the basic research int theory and experimentation of electromagnetics. These two research activities are described in the following.

Computations in Electromagnetics

Research in electromagnetic theory was traditionally done within the regime of applied mathematics. Since the advent of high speed digital computers, we have seen more and more emphasis on the computational research being done in applied electromagnetics. In the early 1960's the main thrust of electromagnetic related computation was in integral equation approaches[1]. The integral equation was a natural choice in radiation problems because the radiation conditions at infinity could easily be satisfied by using proper Green's functions. Although the integral equation method is not too well adapted to problems involving fat bodies and dielectric bodies, early investigators were still quite happy with it, because even with its limitations it was possible to solve many problems which were hitherto unsolvable. As more and mmore problems were solved, researchers began to look for alernatives to the integral equation approach, which might be better than the integral equation method in solving fat, dielectric or even inhomogeneous bodies. This effort is represented by the unimoment method which was developed by K. K. Mei and his associates at ERL[2], and the several publications that follow[3,4] indeed show that the differential equation approach can be very efficient in regions where the integral equation method is clumsy and impractical. This method is currently being used to investigate the scattering by buried dielectric obstacles, a project now supported outside the JSEP.

We have already succeeded in using the unimoment method to solve scattering by dielectric bodies[5], and it is apparent that it should work even better when applied to a single fat metal scatterer. We have also completed two-body scattering involving two metal scatterers[6,7,8].

With the support of AROD the unimoment method has been successfully applied to scattering by submerged targets[9] and to partially buried targets[10]. Other applications of our computational skills are considerable, but our intention is to develop new basic techniques rather than to solve problems. Our new direction is to approach Maxwell's equations in time domain.

The direct time domain solutions of Maxwell's equations were first attempted by Yee[11]. In recent years, even though Yee's method has been extensively applied to scattering problems involving complex-shaped targets[12,13], the basic approach has not been improved. Basically, Yee's method is a finite difference time domain (FDTD) technique, which applied finite difference both in space and time. The disadvantage of this method is that the space mesh must be right rectangular, thus a circle must be composed of small rectangles. This is both theoretically and practically unsatisfying.

Our approach to the time domain problem is to use complete quadratics in space mesh, so that the mesh can conform with the contour of the scatterer. In addition, we have also tried a new "radiation condition" on the technique which shows great promise in terminating the mesh close to the scatterer. We have excellent success in trying our new approach to simple scattering problems in two dimensions. We are very hopeful that this new development will open a new door in electromagnetics.

With our computational skill expand it becomse more and more difficult for us to validate the computed results. Our research also includes measurement of scattering by buried objects.

Electromagnetics at Submillimeter Wavelengths

Radio, microwave, submillimeter wave and light are all electromagnetic waves. The only difference between them is the frequency. However, both in theory and application they are dealt with quite differently. For example, the guided transmission of radio is mostly by coaxial lines, of microwave by metal waveguides, and of light by beams or dielectric waveguides. There are borderline frequencies where different transmission methods can be used. That indeed is the case at submillimeter waves to low infrared waves.

Under the previous sponsorship of JSEP we investigated both metal and dielectric structures such as antenna and wave guides at low infrared frequencies. It has turned out that the metal guide, while lossy, is an excellent device to concentrate electromagnetic power to a very small region, much less than a wavelength. The bulk of any submillimeter device has to consist of dielectric material as antennas and guides. Hence, our effort for the next period will emphasize the application of dielectric guiding structures and couplers at mm waves.

References

(1) Mei, K. K. "On the integral equations of thin wire antennas," *IEEE Trans. on Antennas and Propagation*, Vol. AP-13, no. 3, May 1965, pp. 374-378.

(2) Mei, K. K., "Unimoment method of solving antenna and scattering problems," *IEEE Trans. on Antennas and Propagation*, Vol. AP-22, no. 6, Nov. 1974, pp. 760-766.

(3) Stovall, R. and K. K. Mei, "Application of a unimoment method to a biconical antenna with inhomogeneous dielectric loading," *IEEE Trans. on Antennas and Propagation*, Vol. AP-24, no. 1, January 1976.

(4) Chang, S. K. and K. K. Mei, "Application of the unimoment method to a biconical antenna with inhomogeneous dielectric loading," *IEEE Trans. on Antennas and Propagation*, Vol. AP-23, no. 3, May 1975, pp. 335, 342.

(5) Morgan, M., "Numerical computation of electromagnetic scattering by inhomogeneous dielectric bodies of revolution," Ph.D. Dissertation, University of California, Berkeley, 1976.

(6) Hunka, J. F. and K. K. Mei, "Numerical computation of electromagnetic scattering by two bodies of revolution," USNC/URSI Meeting, November 1978, Boulder, Colorado.

(7) Hunka, J. F., "Scattering by two bodies of revolution," Ph.D. Dissertation, University of California, Berkeley, 1979.

(8) Mei, K. K., J. F. Hunka and S. K. Chang, "Recent developments of the unimoment method," presented at the International Symposium on Recent Developments in Classical Scattering, Columbus, Ohio, June 1979. Also to be published in *Recent Developments in Classical Scattering*, edited by V. K. Varaden, Academic Press.

(9) Chang, S. K. and K. K. Mei, "Mulitpole expansion technique for electromagnetic scattering by buried objects," *Electromagnetics*, Vol. 1, no. 1, pp. 73-89, Jan.-Mar. 1981.

(10) Chang, H. O. and K. K. Mei, "Scattering of EM waves by buried or partly buried body of revolution," *IEEE Antennas and Propagation International Symposium*, Los Angeles, pp. 653-656, June 1981.

(11) Yee, K. S., "Numerical solution of initial boundary value problems involving a Maxwell's equation in isotropic media," *IEEE Trans. on Antennas and Propagation*, Vol. AP=14, pp. 302-307, May 1966.

(12) Taflove, T., and M. E. Brodwin, "Numerical solution of steady state electromagnecit scattering problems using the time-dependent Maxwell's equations," *IEEE Trans. Microwave Theory and Tech.*, Vol. MTT-23, pp. 623-63 August 1975.

(13) Merewether, D. E., "Transient currents induced on a metallic body of revolution by an electromagnetic pulse," *IEEE Trans. Electromagnetic Compatibility*, Vol. EMC-13, pp. 41-44, May 1971.

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: EM-84-1 **Last Year's No.(s):** EM-83-1

Title: Conformal Time Domain Finite Difference Methods of Solving Scattering Problems

Senior Principal Investigator(s): K. K. Mei (415) 642-4106
D. J. Angelakos 642-7200

Scientific Objectives

The objectives of this research are (1) to complete our effort in measuring scattering from buried targets, and (2) to advance our computational capability to the new time domain technique. The first objective is associated with our previous computation effort, which successfully computed scattering by buried targets, and we are doing the experiment to verify the results. The second objective is to further our current success in the research of the time domain finite element method (TDFE), which has great potential in computation in view of the recent trend in computer development.

State of the Art

The controlled measurement of scattering by buried targets has never been attempted, because there was no theoretical data to calibrate the experiment. With our newly developed program using the Unimoment Method, such data are now readily available. Verification of calculations with experimentation is a recognized engineering tradition and our research in the measurements is consistent with that tradition. The details of the experiment are given in subsequent sections.

The time domain computation of electromagnetic wave scattering was first presented by Yee (1) in 1966. This method uses a field lattice shown in Fig. 1. Later work on more complex targets by Taflove (2) and Merewether (3) uses the same lattice scheme. The disadvantage of the method is that the lattice is necessarily rectangular in shape, so it cannot conform to the shape of the scatterers with curved surfaces.

The advantage of the method is that it solves hyperbolic a partial differential equation in a time marching computation procedure, which does not solve any matrix. Furthermore, the computations are limited to local space time data and the usage of memory is almost in sequential order, thus it is possible to use relatively slow access memory, such as the virtual memory systems offered by many minicomputers.

Our objective is to advance the state of the art to conformal mesh and take advantage of the recent trend in minicomputer development in low cost, large capacity computers.

Progress and Publications Since Last Major Proposal

The proposed projects on measurement and conformal time domain analysis are new. Nothing has yet been published on these subjects.

Publications in previous proposed tasks since September 30, 1982 include the following:

Under JSEP Sponsorship

(1) "Radiation and Scattering from Partially Buried Vertical Wires," C. C. Lin and K. K. Mei, *Electromagnetics*, 2, 4, 309-334 (Oct.-Dec. 1982).

(2) "Bistatic Scattering from Objects with Constrained Circuit Flow," D. J. Angelakos and R. K. Najim, *Electromagnetics*, 2, 4, 355-362 (Oct.-Dec. 1982).

(3) "Unimoment Method for Electromagnetic Wave Scattering," K. K. Mei and T. M. Kvam, Workshop on Research Techniques in Wave Propagation and Scattering," Ohio State University, Columbus, Ohio (Oct. 18-21, 1982).

(4) "Conformal Time Domain Finite Difference Method," K. K. Mei, A. Cangellaris, and D. J. Angelakos, to be presented URSI Electromagnetic Symposium, Santiago De Compostela, Spain (Aug. 23-26, 1983).

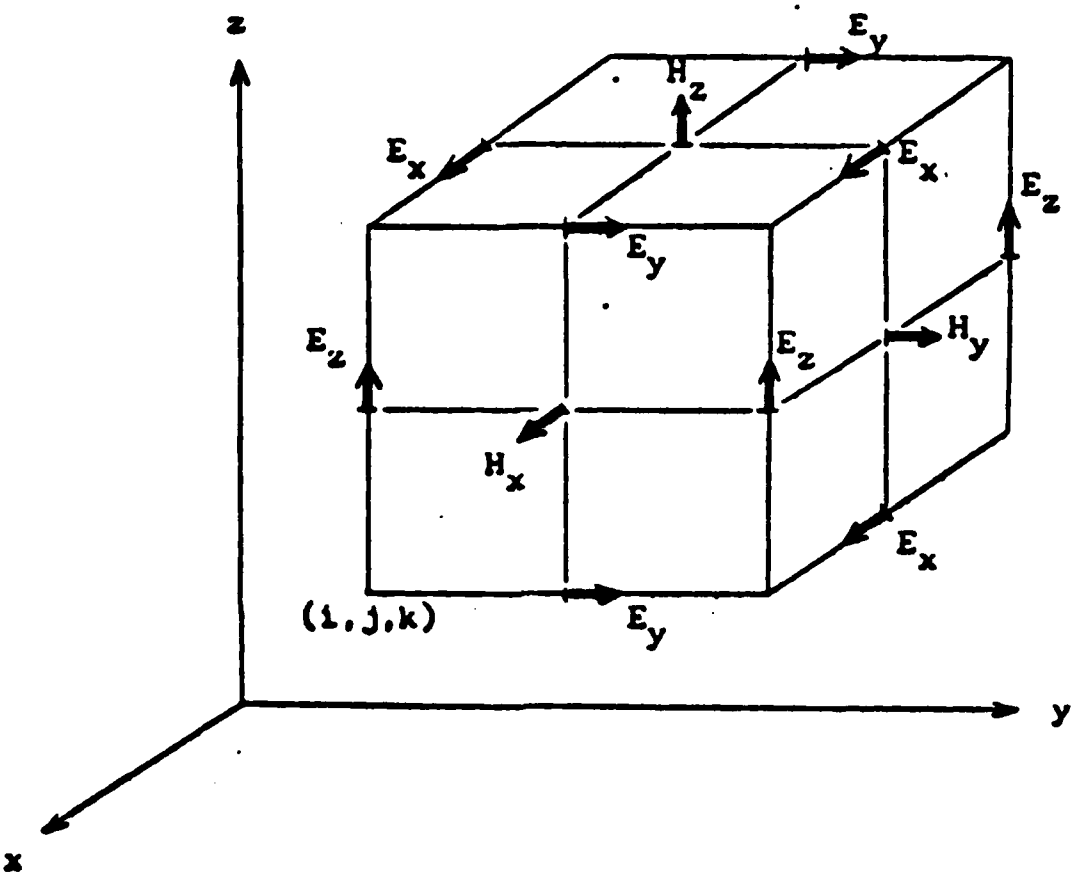


Fig. 1 POSITIONS OF THE FIELD COMPONENTS ABOUT A UNIT CELL OF THE YEE LATTICE

Under Other Sponsorship - Related

(5) "Scattering by Buried and Partially Buried Objects," H. Chang and K. K. Mei, to be published in *IEEE Trans. on Geoscience and Remote Sensing*.

Measurement of Electromagnetic Scattering by Submerged Targets

Our computational capability has actually developed beyond the point where verification of the results by classical methods is still available. The computations of scattering by submerged targets can only be verified by experimentation. We have already set up an experiment which will do just that. The experiment involves two parts. Part I is to measure the dielectric parameter of the earth. Part II is to measure the scattering electric field close to the air-ground boundary near the target. The following sections describe the details of the experiment which will be in operation very shortly.

(a) Ground preparation and construction

Since the computations are done for idealized uniform ground, the earth near the target must be as uniform as possible and be isolated from the weather. This is done by digging a 10' X 10' X 6' (deep) pit and refilling it with sifted agricultural soil. The pit is then covered with a wood and plastic shelter. A movable carriage is mounted on a rail 9 feet above the ground surface and the antennas and probes are mounted on the carriage. The relative position between the illuminating antenna and the probe is fixed, as shown in Fig. 2. If the ground were truly uniform the probe should measure constant field as it moves over the ground.

(b) Ground parameter measurement

The most important ground parameter for verification of the computation is the dielectric constant, and that for application is the water constant of the soil. We plan to determine those two parameters in the following ways:

(i) soil water content

The soil water content may be determined from the resistance of buried gypsum blocks which are frequently used in agriculture. The resistances are measured by a 1,000 Hz wheatstone bridge, and the samples are weighed before and after they are baked, to determine water content. The resistance can then be calibrated versus percentage water content of the soil. After proper calibration we only need to measure the block resistance to determine the water content of the soil.

(ii) Dielectric parameter

An isolated pair of source and probe antennas are mounted above the ground. The received amplitude and phase at the probe when the ground is covered with a flat sheet of aluminum is considered to be 1 and 180° respectively. When the conducting sheet is removed, the amplitude and phase of the received signal can be determined. The received amplitude ρ and φ can be used to calculate the ground reflective index $n = n_r + jn_i$, by

$$n_r = \frac{1-|\rho|^2}{1+|\rho|^2 = 2\rho_r}$$

$$n_i = \frac{-2\rho_i}{1+|\rho|^2 = 2\rho_r}$$

where,

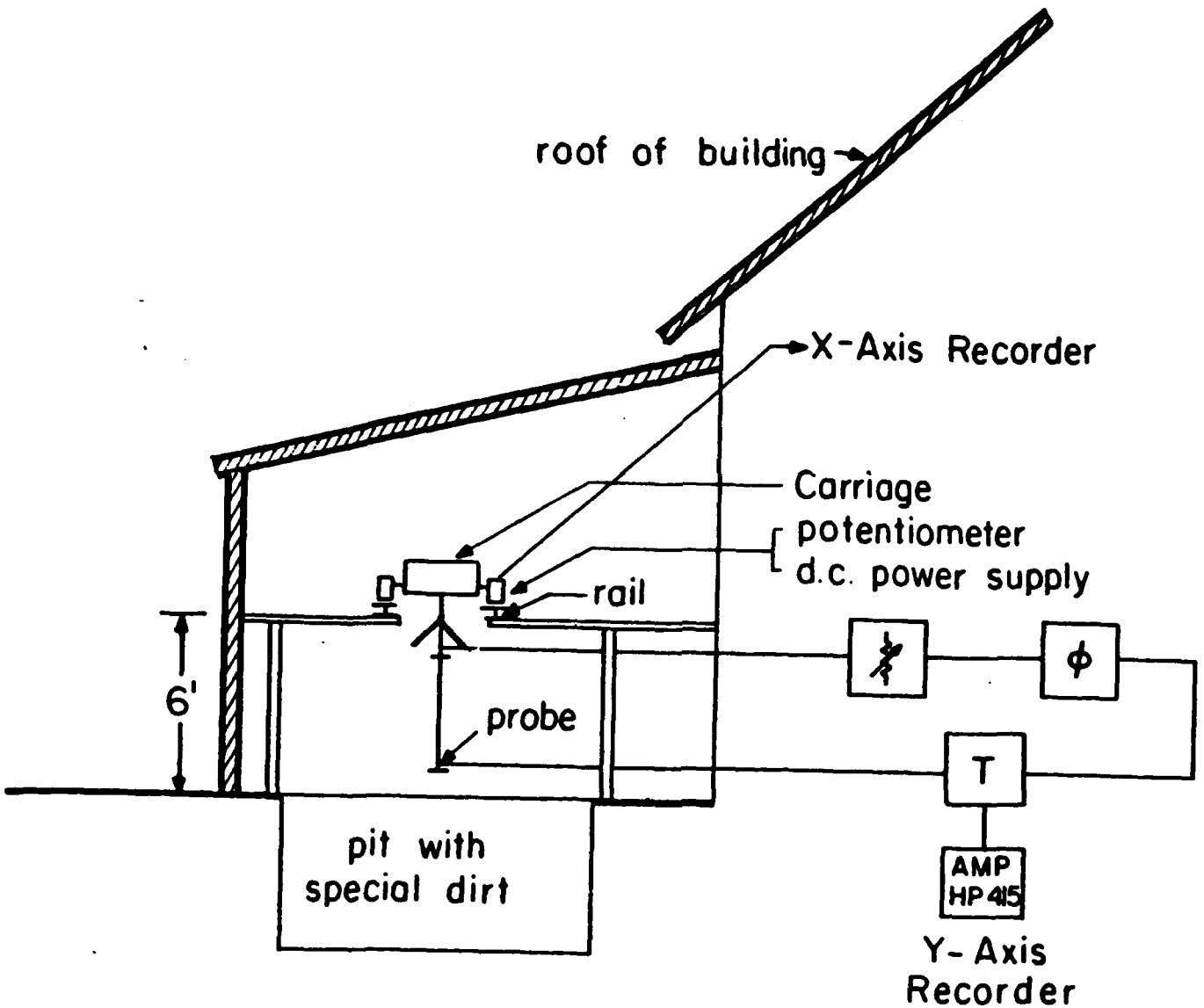


Figure 2. Schematics of measurements of scattering from buried targets.

$$\rho = \rho_r + j\rho_i$$

$$|\rho|^2 = \rho_r^2 + \rho_i^2$$

Thus, the real and imaginary parts of the reflective index may be obtained from the complex reflection coefficient.

(b) Scattered Field Measurement

Computations indicate that the scattered electric field of a buried dielectric finite cylinder of $\varepsilon_r = 2.67$ and 1.1 diameter and 5.5 cm thick, is about 5% of the incident field at about 1 inch above the ground. The incident field is defined as the field at the same position when the scatterer is replaced by the background material. The measurement scheme is to null out the incident field by mixing the received signal of the probe with the source signal by a hybrid junction, such as shown in Fig. 2. The position of the antenna is measured by the potentiometer mounted on a wheel of the carriage. The measurement will be done twice. First the ground without the target will be measured and the signals recorded digitally in a MINK 11 minicomputer. Next, the measurement is repeated with the target in place. The difference between the two measurements is the scattered field.

The measurement set-up is almost completed and the testing is about to begin soon.

Conformal Time Domain Finite Element Method

We have already made significant progress in time domain computations. Our scheme is to break away from the Yee's lattice and have each electric field component defined at every node point. The magnetic fields are defined at nodes inside an electric field cell such as shown in Fig. 3. The time steps of the magnetic fields are in between the electric fields, same as Yee's approach. The magnetic fields are obtained from the Maxwell's equation,

$$\mu \frac{\partial \bar{H}}{\partial t} = \Delta \times \bar{E} \tag{1}$$

which can be numerically expressed as:

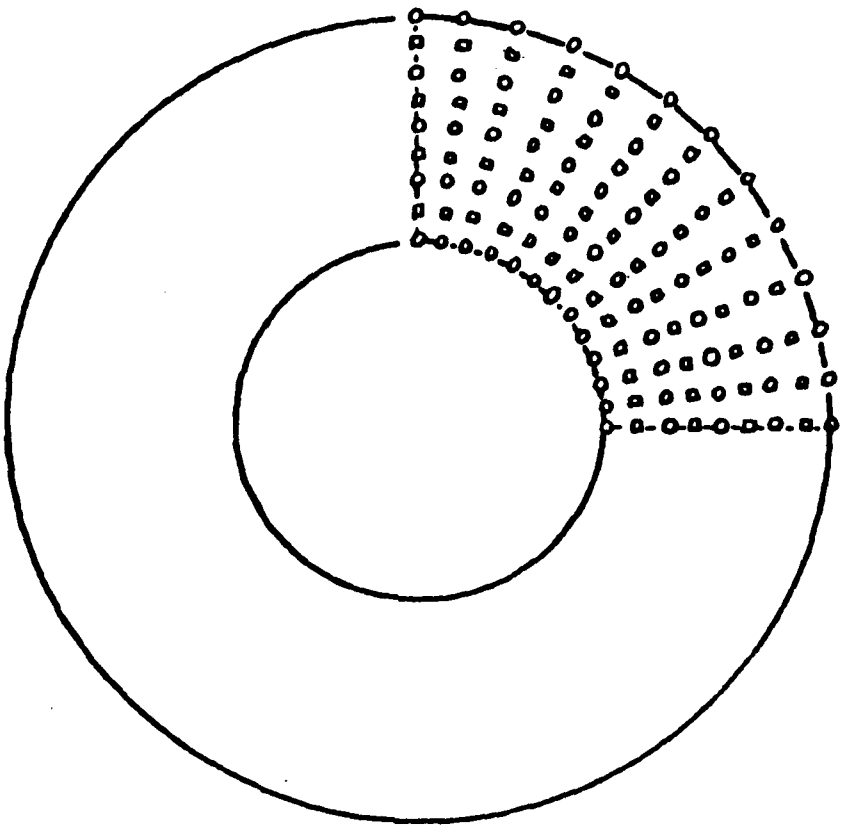
$$\mu H_x^{n+1/2} = \left(\frac{\partial E_z^n}{\partial y} - \frac{\partial E_y^n}{\partial z} \right) \Delta t + \mu H_x^{n-1/2} \tag{2}$$

and similar formulas for H_y and H_z.

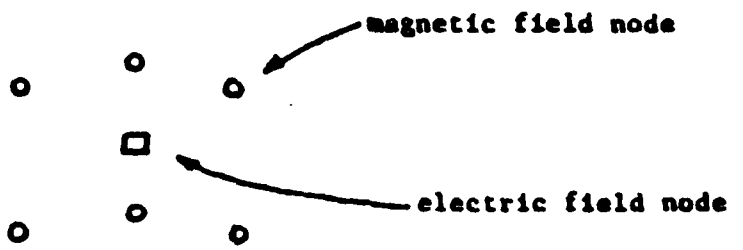
The space derivatives in (2) are performed analytically on the interpolated values of $\bar{E}$. If we use conforming elements or complete interpolating polynomials, we may have great freedom in locating the nodes of the fields and thus be able to have conforming mesh. We have used this new technique to calculate two dimensional scattering and have obtained results comparable to the time domain integral equation method (4) which is known to be stable and accurate but much more expensive to use. Some typical results are shown in Fig. 4.

Our initial success in the conformal time domain finite element technique has encouraged us to consider the objective of solving arbitrary 3-D targets, which have been hitherto untractable except for very small volume targets. It is our belief that using the time domain finite element method we shall be able to solve problems beyond the capability of the present main frame machine by using the new minicomputers at a considerable amount of cost saving.

In addition to solving scattering problems, the time domain analysis can also be used to analyze a guided wave system. We may excite a waveguide by a



(a) A conformal mesh for a conducting circle.



(b) A typical cell of magnetic field

Fig. 3. A node configuration of the conformal TDFD method.

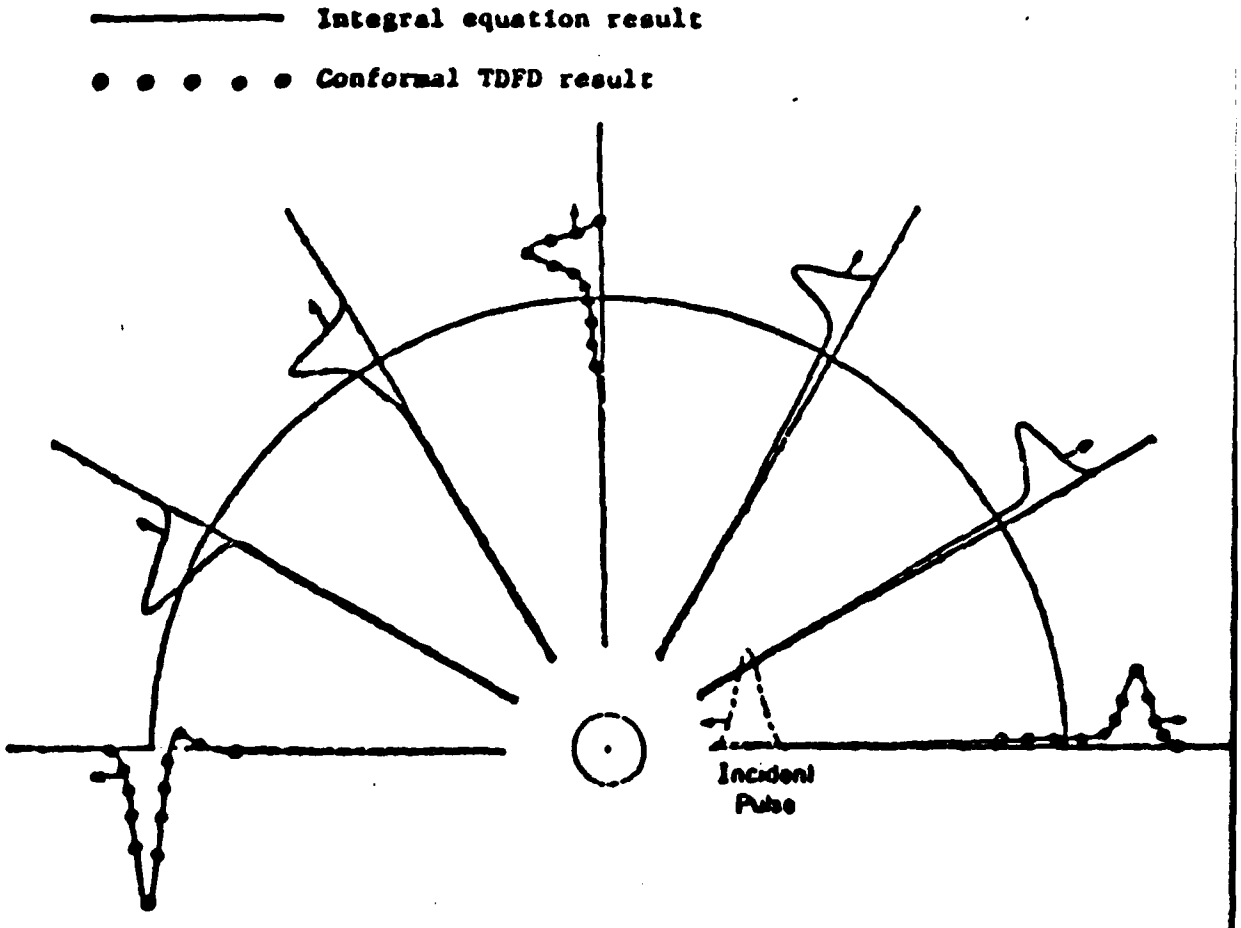


Fig. 4 TM approximate impulse response of circular cylinder.

Gaussian pulse and obtain a time domain solution of the field along the transmission structure. The space-time Fourier transform of the field shall provide the $\omega-\beta$ diagram of the structure. This analysis demands large storage space but has the advantage of being a deterministic computation, without search or iteration processes. However, the time domain analysis is expected to be more advantageous on a present day minicomputer which contains a virtual memory system.

The time domain analysis of a guided wave can easily be extended to the analysis of cavities or resonators. We shall use this analysis technique in the design of mm wave antennas and couplers, which are described in .

Proposed Research Program

A. Measurement of Electromagnetic Scattering by Buried Objects

The proposed program on measurement of scattering by buried objects includes the following:

(1) Completion of the test facilities now under construction.

(2) Compilation of ground parameters as a function of ground resistance at 1,000 Hz.

(3) The profile of the ground parameter.

(4) Measurement of the scattered field.

(5) Investigation of converting the facility to measure time domain scattering.

B. Conformal Time Domain Finite Difference and Finite Element Methods

The proposed program on time domain computation includes the following:

(1) To investigate different conforming mesh techniques such as: polynomial interpolation, rational function interpolation, lagrange interpolation techniques.

(2) To investigate different approximations to radiation conditions such as: Enquist and Majda's method, De Mur's method, the Poynting vector methods.

(3) To investigate scattering by 2-D dielectric bodies of arbitrary shape.

(4) To investigate scattering by 3-D metal bodies of arbitrary shape.

References

(1) Yee, K. S., "Numerical solution of initial boundary value problems involving a Maxwell's equation in isotropic media," *IEEE Trans. on Antennas and Propagation*, AP-14, 302-307 (May 1966).

(2) Taflove, T. and M. E. Brodwin, "Numerical solution of steady state electromagnetic scattering problems using time-dependent Maxwell's equations," *IEEE Trans. Microwave Theory and Tech.*, MTT-23, 623-630 (August 1975).

(3) Merewether, D. E., "Transient currents induced on a metallic body of revolution by an electromagnetic pulse," *IEEE Trans. Electromagnetic Compatibility*, EMC-13, 41-44 (May 1971).

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: EM-84-2 **Last Year's No.(s):** EM-83-2

Title: Millimeter Wavelength Electromagnetic Structures

Senior Principal Investigator(s):

S. E. Schwarz	(415) 642-5684
K. K. Mei	642-4106
D. J. Angelakos	642-7200

Scientific Objective

In order to exploit the frequency range above 30 GHz, it is necessary to use electromagnetic structures with dimensions on the order of 1 mm or less. For such structures, planar microfabrication is very advantageous. The requisite small dimensions are easily fabricated; it is convenient to integrate various components into planar circuits; production costs can be low. However, planar electromagnetic structures are less familiar than conventional waveguides; hence there are many unsolved problems of analysis and design. Some of these problems are as follows. (a) Design of planar components to perform each of the common functions of conventional components based on hollow waveguide structures. (b) Reduction of ohmic and radiation losses. (c) Provision of adjustable elements that can be used for tuning and optimization.

In recent work under JSEP and other support (1,2) we have developed planar bandpass filters and resonators for use in integrated millimeter-wave receivers. These components are based on use of coplanar waveguides, which is suitable because of its low radiation loss. The present resonator design is shown in Fig. 1. Its Q, as measured in 1-GHz simulation, is about 195, primarily a result of radiation loss. When the resonator is scaled to 100 GHz its Q is expected to decrease to about 50, because of ohmic loss.

It would be desirable to achieve high values of resonator Q. Higher Q would result in better frequency stability and also in lower noise. One way to accomplish this would be to add to the circuit a low-loss dielectric resonator. It is therefore necessary to find an efficient means of coupling such a resonator to the planar circuit. Some means of tuning the resonator should be provided.

State of the Art

The proposed work is related to an ongoing effort in high-frequency devices and integrated circuits. This work involves development of GaAs mixers, planar oscillators, waveguides, resonators, and tuning elements, and assembly of these components into receivers and other systems.

Work directed toward millimeter-wave receivers has been carried on in several laboratories (3,4,5,). Good progress has been made with planar Schottky diode mixers (3) and with planar antennas (4), waveguides, and filters (1), but a fully integrated planar receiver has not yet been built at this writing. In the field of planar millimeter-wave oscillators, attention has been directed primarily to designs based on microstrip (7,8). However, microstrip is not truly planar (since one electrode is on the reverse side of the circuit). We plan to pursue designs based on fully planar guiding structures, such as coplanar waveguides. The use of dielectric resonators for stabilization has been studied by various workers (9,10,11). Our concern will be to apply this technique to fully planar oscillators, using designs consistent with planar microfabrication techniques.

Plans for complete planar receiver systems are well advanced. A block diagram of such a system is shown in Fig. 2. For design and testing purposes, simulation in the range 1-10 GHz is used. An anechoic chamber, network analyzer, and other test apparatus are in use for this purpose. Extensive microfabrication facilities are also in use for deposition of mm-wave electromagnetic structures with photolithography. The resulting structures are tested at 70 GHz, where sources, calibrated detectors, and associated waveguide components are available.

As of this writing we have tested waveguides, bandpass filters, and antennas for 70 GHz receivers. (There is nothing special about 70 GHz except that we

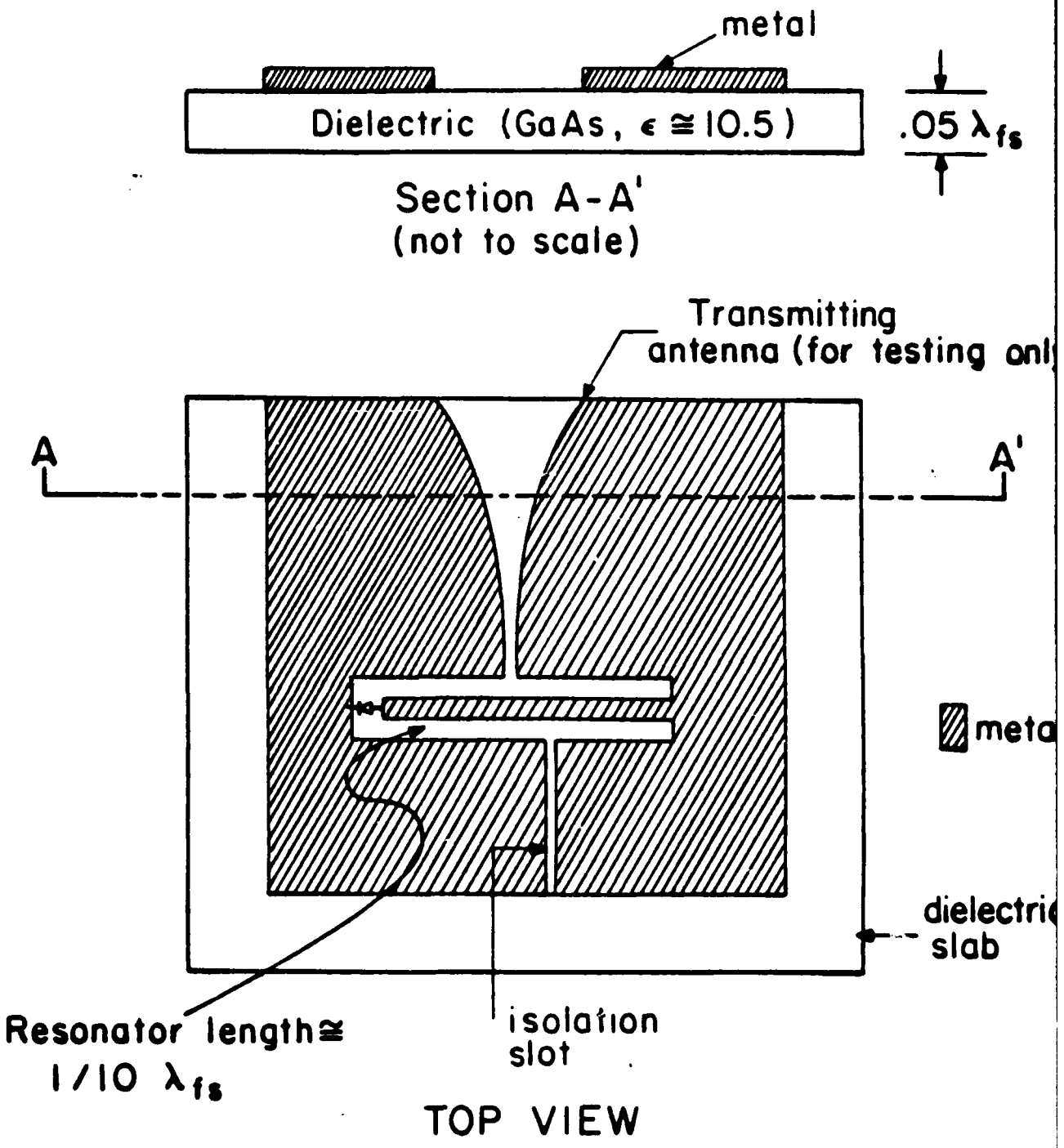


Fig. 1. The present resonator consists of a short-circuited length of coplanar waveguide deposited on the surface of a thin dielectric. The transmitting antenna is used to extract output radiation for analysis. The isolation slot is required in order to apply dc bias to the Gunn diode.

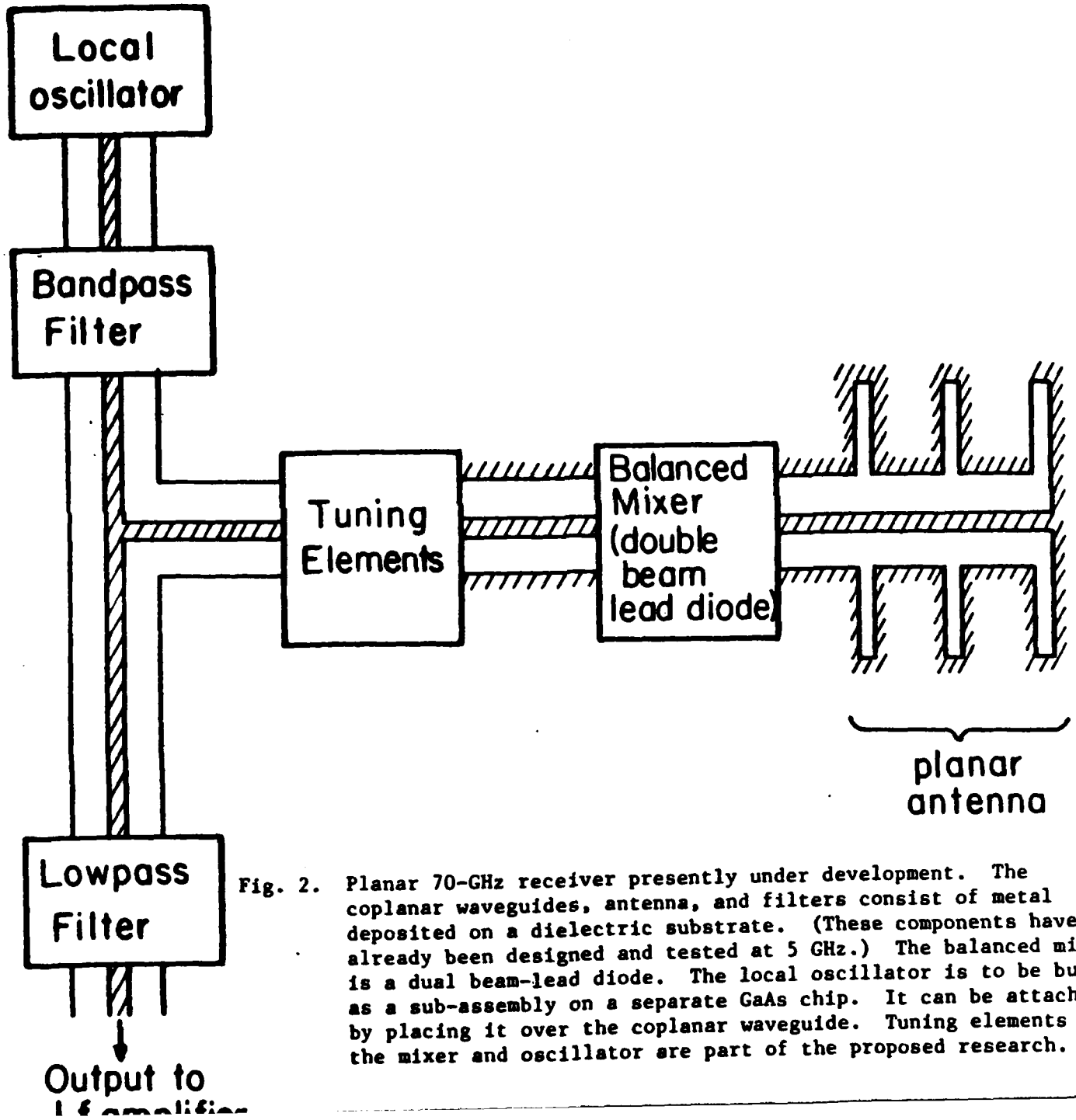


Fig. 2. Planar 70-GHz receiver presently under development. The coplanar waveguides, antenna, and filters consist of metal deposited on a dielectric substrate. (These components have already been designed and tested at 5 GHz.) The balanced mixer is a dual beam-lead diode. The local oscillator is to be built as a sub-assembly on a separate GaAs chip. It can be attached by placing it over the coplanar waveguide. Tuning elements for the mixer and oscillator are part of the proposed research.

are well-instrumented at that frequency. The same devices can be scaled to 95 GHz.) Designs are being completed for a complete receiver, including a Gunn local oscillator. Although we have some confidence that this receiver will function successfully, it uses "first generation" components, some of which are less than ideal. The proposed research is intended to provide an improved oscillator. Similar improvements can probably be introduced in other elements of the system.

Progress & Publications Since Last Major Proposal

Acknowledging JSEP Support

D. B. Rutledge and S. E. Schwarz, "Planar Multimode Detector Arrays for Infrared and Millimeter-Wave Applications," *IEEE J. Quantum Electronics*, QE-17, 407-414 (March 1981).

C. Yao, S. E. Schwarz and B. J. Blumenstock, "Monolithic Integration of a Dielectric Millimeter-Wave Antenna and Mixer Diode: an Embryonic Millimeter-Wave IC," *IEEE Trans. Microwave Theory and Techniques*, vol. MTT-30, 1241-1247 (August 1982).

N-L. Wang and S. E. Schwarz, "Planar Oscillators for Monolithic Integration," *Int'l. J. of Infrared and Millimeter Waves*, vol. 3, 771-782 (November 1982).

T. Wang and S. E. Schwarz, "Design of Dielectric Ridge Waveguides for Millimeter-Wave Integrated Circuits," *IEEE Trans. Microwave Theory and Techniques*, MTT—31, 128-134 (February 1983).

D. F. Williams and S. E. Schwarz, "Design and Performance of Coplanar Waveguide Bandpass Filters," to appear in *IEEE Trans. Microwave Theory and Techniques*.

Theses:

"Submillimeter Integrated-Circuit Antennas and Detectors," David B. Rutledge, Ph.D. Thesis, University of California, Berkeley, 1980.

Abstract

Integrated-circuit techniques promise to make possible reliable submillimeter devices and arrays. This thesis discusses three different integrated-circuit antennas. The first is an evaporated V-antenna in a sandwich of crystal-quartz substrates. This was the first evaporated submillimeter antenna to have a predictable pattern, and it has been succesfully tested in a plasma interferometer at 119 μm. The second is a dielectric-waveguide antenna, made by anisotropic etching of silicon. This antenna has been integrated with a Schottky diode. The final antenna is a multi-mode, tunable array of 400 microbolometers. This approach gives efficient coupling between a source and the detectors. The array achieves a D* of 2 x $10^8 cmHz^{1/2}W^{-1}$ at 1.4 mm with a modulation frequency of 1 MHz.

"Monolithic Integration of a Dielectric Millimeter-Wave Antenna and Mixer Diode," Chingchi Yao, Ph.D. Thesis, University of California, Berkeley, 1981.

Abstract

A monolithic silicon integrated circuit consisting of a mixer diode and an all-dielectric receiving antenna has been built and tested at 85 GHz. Radiation is coupled into the device optically with a coupling loss of 2.7 dB. No external metal structure is required for coupling. The design can be used efficiently at considerably higher frequencies, and can be elaborated into more complex integrated circuits. From measurements of video responsivity the losses of various parts of the device are estimated. A simple theory of conversion efficiency is found to agree well with experiments; this theory is then used to predict the performance of improved versions of the device. It is shown that acceptable conversion efficiencies can be obtained with a more advanced diode fabrication technology using epitaxial Si or GaAs. Integrated millimeter-wave receivers of this kind should be suitable for short-path terrestrial communications, in applications where compactness and low cost are required.

Under Other Sponsorship (related)

G. S. Lee, "Superconductor-Insulator-Superconductor Reflection Parametric Amplifier," *Appl. Phys. Lett.*, 41, 291-293 (August 1982).

G. S. Lee and S. E. Schwarz, "Numerical Studies of Mutual Locking of Resistively and Capacitively Shunted Josephson Junctions," submitted to *Appl. Phys. Lett.*

Significant Accomplishments

The significant accomplishments are described in the "Scientific Objective", and in greater detail in the publication list.

Proposed Research Program

It is proposed to carry out research on millimeter (and submillimeter) wavelength components and in particular on those of coplanar geometries. The overall objective is to understand the interrelationship of the various components in order to facilitate the design of planar millimeter/submillimeter wavelength systems.

The proposed research will proceed in various steps which, of course, are dependent on each other. In particular, it is proposed that the coplanar structures which we have studied will be combined with cylindrical dielectric resonators with various cross sections in order to improve the resonance characteristics of the structure. The problems of coupling between the coplanar structure, the driving coplanar waveguide and its coplanar resonator will be analyzed using not only known techniques which may be limited, but especially the time domain numerical method as explained in EM-85-1. Obtaining a grasp of the behavior of the hybrid structure will naturally lead into the problem of methods of tuning. The effects of dielectric losses, radiation by the open resonator and coupling losses are not fully understood. This may involve tuning of the open dielectric structure by mechanical penetration, by close coupling of other dielectric objects, by displacement of the resonator, etc. Emphasis must be placed on the somewhat unusual structures consistent with planar microfabrication technology. There is considerable information on open dielectric resonators -- a good list appears at the end of reference (11). However, the basic problem of the coupling of these resonators to planar structures such as coplanar waveguides has not been investigated in detail.

As the research progresses, partial systems will be fabricated and tested by simulation at 5 GHz. At this frequency measurements are easy, and the large-scale structures are easily adjusted and optimized. When the basic characteristics become known we can proceed to measurements on microfabricated 70-95 GHz structures. This will determine the effects of skin-effect losses that appear at high frequencies.

Progress of this research will enable us to make substantial contributions to the art of planar millimeter-wave systems such as indicated in Figs. 2 and 3. The interrelationship of the various components must then be determined -- on a theoretical basis or in an experimental way, or a combination of both.

Adjustable tuning structures for planar millimeter-wave systems will be investigated theoretically and experimentally. For example, bonding wires can be placed across slots to short-circuit them, thus providing an adjustable reactance. We propose to investigate the modelling of such bonding-wire shorts at millimeter frequencies in order to assess reactance and ohmic and radiation loss.

References

(1) D. F. Williams and S. E. Schwarz, "Design and Performance of Coplanar Waveguide Bandpass Filters," to appear in *IEEE Trans. Microwave Theory and Techniques.*

(2) N-L. Wang and S. E. Schwarz, "Planar Oscillators for Monolithic Integration," *Journal of Infrared and Millimeter Waves*, vol. 3, 771-782, November 1982.

(3) B. J. Clifton, G. D. Alley, R. A. Murphy and I. H. Mroczkowski, "High-Performance Quasi-Optical GaAs Monolithic Mixer at 110 GHz," *IEEE Trans. Electron Devices*, ED-28, 155-157 (February 1981).

(4) L. Yuan, J. Paul and P. Yen, "140-GHz Quasi-Optical Planar Mixers," 1982 International Microwave Symposium, paper S-5.

(5) S. E. Schwarz and D. B. Rutledge, "Moving Toward NMM Wave Integrated Circuits, *Microwave Journal*, 47-52 (June 1980).

(6) D. B. Rutledge, D. P. Neikirk, D. P. Kasilingam, "Integrated-Circuit Antennas," to appear in *Infrared and Millimeter Waves*, K. J. Button, ed., Vol VI.

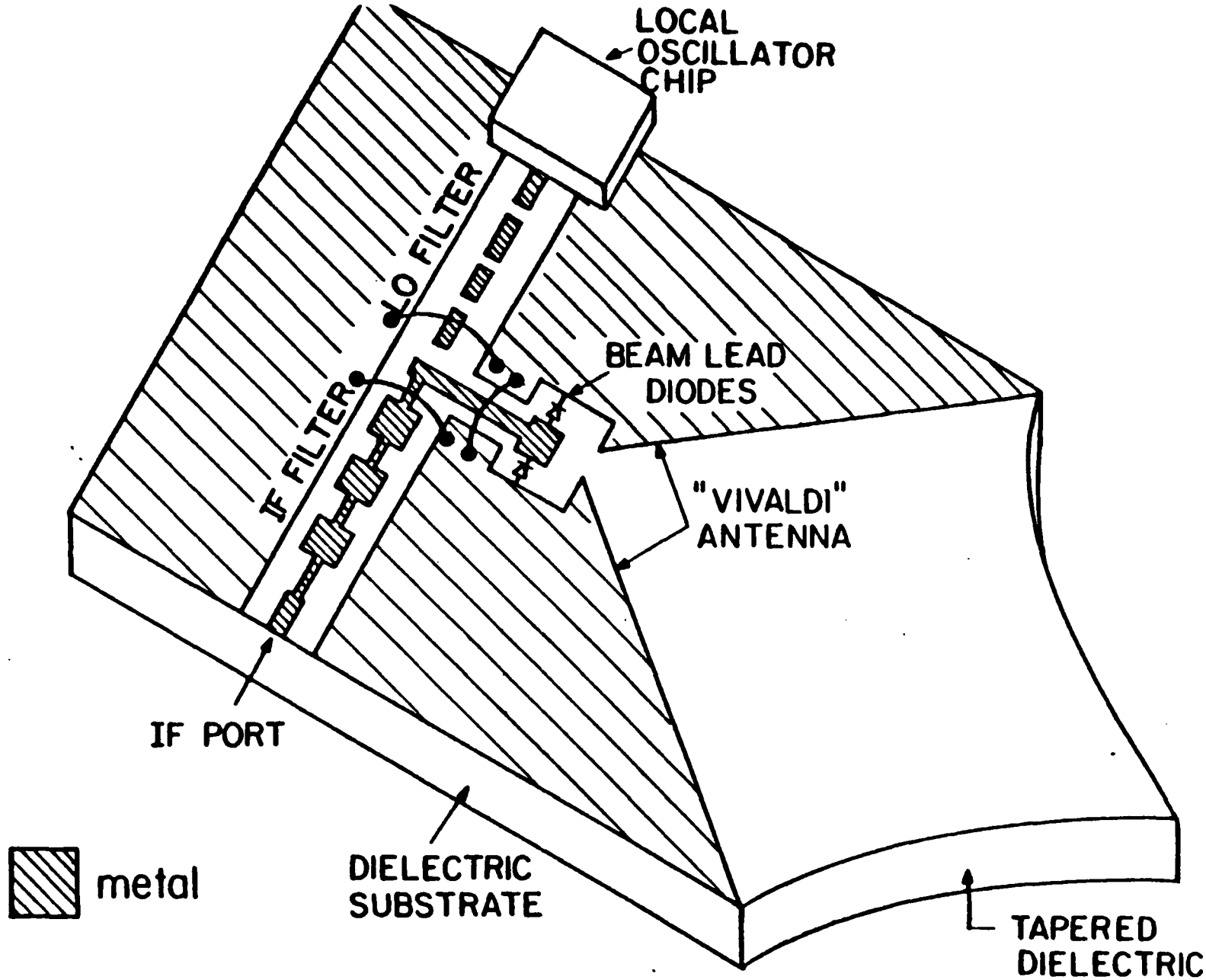
(7) G. B. Morgan, "A Microstrip IMPATT Diode Oscillator for 100 GHz," Sixth International Conference on Infrared and Millimeter Waves, paper M-5-2 (1981).

(8) D. C. Smith, T. J. Simmons and M. R. B. Jones, "A Comparison of the Performance of Millimeter-Wave Semiconductor Oscillator Devices and Circuits," International Microwave Symposium, paper D-1 (1983).

(9) T. Makino and A. Hashima, "A Highly Stabilized MIC Gunn Oscillator Using a Dielectric Resonator," *IEEE Trans. Microwave Theory and Techniques*, MTT-27, 633-638 (July 1979).

(10) Aps Khanna and Y. Garault, Determination of Loaded, Unloaded and External Quality Factors of a Dielectric Resonator Coupled to a Microstrip Line," *IEEE Trans. Microwave Theory and Techniques*, MTT-31, 261-266 (March 1983).

(11) Tsuji, Shigesawa, Takigama, "On the Complex Resonance Frequency of Open Dielectric Resonators," *IEEE Trans. Microwave Theory and Techniques*, vol. MTT-31, 392-396 (May 1983).



EM-84-2 - p. 5a

BROAD BAND RECEIVER WITH BALANCED MIXER

Fig. 3. The metallization is on the bottom side of the LO chip. That means TiO_2-filled tuning cavity is on the top, where we can probe it for tuning.

University of California, Berkeley — Electronics Research Laboratory

Joint Services Electronics Program — August 15, 1983

II. Basic Research in Quantum Electronics — Coordinator Professor J. R. Whinnery

General

We propose to perform research in quantum electronics in the following areas: (1) composite semiconductor laser structures in which integrated-optics circuit elements are combined with the active region for purposes of frequency control, wavelength tuning, power combining, or short-pulse formation; (2) layered, quantum-well structures of III-V alloy semiconductors for high bandwidth optical and millimeter-wave devices.

Semiconductor lasers have proven their dominance for optical communication and information processing applications, but many extensions and improvements are possible. Recent research in our laboratory has shown the increased spectral purity and frequency stability with temperature possible through the use of auxiliary circuits coupled to or joined to the lasing region. These circuits also provided the opportunity for significant wavelength tuning or frequency switching. Further improvements in these directions are possible and will be pursued. The coupling networks developed in the above work may also be utilized for power combining and a comparison of this technique with that of laser arrays is proposed. There are also possibilities for use of the networks for short-pulse formation with semiconductor lasers, say by passive mode locking using a ring configuration, or by nonlinear coupling effects between adjacent guiding regions. The scattering-matrix formulation has proven invaluable in the analysis of these several network applications.

Recent millimeter-wave work in our laboratories has involved fabrication and study of GaAs Schottky diode arrays, planar 70 GHz Gunn oscillators, and a variety of transmission lines and elements for use with monolithic integrated circuits for the millimeter-wave range. Quantum-well structures are promising for many of these devices, not only because of the increased mobility, with the corresponding increases in cut-off frequency and efficiency, but also because of the advantage of their inherently planar form over the "vertical" form of conventional millimeter-wave components. In particular, modulation should be possible with lower voltages. The quantum-well structures are also of use for integrated-optics devices. We have demonstrated a very fast detector for visible wavelengths using a metal-insulator-metal-insulator-metal (M-I-S-I-M) structure with silicon as the semiconductor. It is proposed to study extensions of this with a quantum-well material used as the mesa. This should give peak response corresponding to the two-dimensional exciton levels, and could be tailored by modulation-doping of the wells. The quantum-well structures are to be grown in the Berkeley MBE unit, or in some cases obtained commercially.

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: QE-84-1 **Last Year's No.(s):** QE-83-1

Title: Analysis of Integrated-Optics Networks Applied to Semiconductor Lasers

Senior Principal Investigator(s): J. R. Whinnery (415) 642-1030
S. Wang 642-4134

Scientific Objective

The potentiality of semiconductor lasers may be appreciably extended by the interconnection or coupling of various integrated-optics networks to the active regions of the lasers. At the same time there are problems including radiation and mode conversion at the junctions, frequency pulling and increased loss. A great deal has been accomplished in minimizing the problems and to accomplish desired objectives of frequency stabilization, wavelength tuning and spectral improvement. The objective of this research is to continue these improvements and to extend into the nonlinear and short-pulse range of applications. Stress will be placed on the understanding of the interaction phenomena, both from a materials and optical network point of view.

State of the Art

Tremendous advances have been made in semiconductor laser technology during the last decade, all of this opening up new directions for the future. The frequency range has been extended both into the infrared and also into the visible (1). Operating lifetime continues to increase. Spectral purity -- important for high-data-rate systems and also for scientific uses -- has been improved by resonators incorporating distributed Bragg reflectors (DBR) (2), and by a variety of techniques for controlling transverse modes (3). Power output has been increased from a few milliwatts to several times this for a single laser (4), and more by arrays of coupled lasers (5-7). Picosecond and subpicosecond operation has been demonstrated by mode locking (8-10) and by several pulse excitations (11).

Of the recent advances, very important has been the coupling of active resonators to other active or passive ones on the same substrate by a variety of techniques. These have had important uses in mode control, wavelength stability with temperature, tuning, and wavelength switching. Much of the pioneering work, with the basic analysis, has been done in our laboratories (12-15) and will be detailed in the section on *Recent Progress*, but much important related work with multiple resonators or coupled resonators is being carried on in other laboratories (16-18). There is much more to be done in this area, as will be explained in the section on *Proposed Research*.

The networks mentioned above also have application to power-combining techniques. Most power combining to date has used arrays of parallel lasers, with power combining taking place in the radiation pattern. The first work added power only incoherently, but recent arrays have provided coupling, either by direct coupling or through evanescent fields, to maintain phase coherence (6,7,19). Such arrays represent a significant development, but for many applications additional flexibility would be provided by combining by means of waveguide networks, as is typically done for microwave devices (20).

The coupling networks may also have application to the short-pulse operation of semiconductor lasers. The first mode locking of semiconductor lasers was done actively, with an external cavity (8). Passive mode locking followed (9) with later extensions to the subpicosecond regime (10). It has been difficult to obtain saturable absorbers with long operating lifetimes, so recently much emphasis has shifted to the generation of short pulses in semiconductor lasers by controlled transient techniques. In the meantime, the technique of colliding pulse mode locking for dye lasers in the ring configuration has been shown to provide ultra-short, stable pulses (26), and various analyses have indicated that the key element is the interference grating produced by the colliding pulses in the saturable absorber. We have already demonstrated semiconductor ring lasers (21) so are in a position to look at this possibility. There is also much

interest in the interaction of the short pulses with semiconductors following generation. Our work to date has been largely with the photoconductive effect, and the dispersion of the switched pulses following generation.

Progress and Publications Since Last Proposal

A. Under Combined Sponsorship

The stress in this project has been on the application of integrated-optics networks to semiconductors lasers, using the scattering matrix as the primary method for analyzing the interconnections. Especial important progress has been made in the interferometric and coupled-guide lasers. Interferometric techniques were first used with gas lasers (22), and of the several arrangements used, the open-ended Michelson interferometer (OEMI) and the multi-cavity interferometer were found especially adaptable to injection lasers. In the former, a y-junction acts as a beam splitter, coupling to the side arm of the interferometer. The radiation modes form the open arms of the common guide 1. In the multi-cavity arrangement, reflections separating the cavities may take place in a waveguide, or at etched or cleaved facets. The scattering-matrix analysis shows that longitudinal modes of the composite resonators may be divided into two groups, coincident resonant modes (CRM), and non-resonant modes (NRM).

An OEMI laser made by Fattah and Wang (13) showed nearly single longitudinal mode oscillations even though it was gain-guided, and was locked to one CRM for approximately 7°C during which it changed at a rate of 0.67 Å/°C. Moreover, the possibility of wavelength tuning or wavelength switching was demonstrated. With separate, variable, pumping in the interferometer arm to change refractive index by change of carrier concentration, one OEMI laser showed continuous wavelength change of 2.5 Å, and another a sudden wavelength jump of 30 Å.

For the multi-cavity lasers, one version of Choi and Wang (14) utilized an internal-reflection interferometer (IRI) and another of Antreasyan and Wang (15) an integrated-etalon interferometer (IEI). In the IRI version, lateral guiding was achieved by a channeled-substrate structure with a slight thickness variation in the active region, and internal reflections provided by notches in the waveguide channel. In the IEI version, a buried heterostructure provided lateral guiding. The laser was made of three segments with one curved section of radius 150 μm, joined at both ends to straight sections. The IRI laser had a wavelength locking range of 7°C and the IEI a range of 23°C. Additional increases in these ranges are possible by reducing cavity length.

Although emphasis has been on the coupling of passive cavities to active ones for the purposes of mode control and tuning as described, it is clear that many of the junctions and coupling techniques could be used to couple multiple active cavities for the purpose of combining powers from individual lasers.

Papers Under Joint Sponsorship

S. Wang, H. K. Choi and I. H. A. Fattah, "Studies of Semiconductor Lasers of the Interferometric and Ring Types," *IEEE J. Quant. Elect.*, vol. QE-18, p. 610 (1982).

H. K. Choi and S. Wang, "Semiconductor Internal-Reflection-Interference Laser," *Appl. Phys. Lett.*, vol. 40, p. 571 (1982).

A. Antreasyan and S. Wang, "Semiconductor Integrated Etalon Interference

Laser with a Curved Resonator," *Appl. Phys. Lett.*, vol. 42, p. 562 (1983).

B. Related Work Under Other Sponsorship

An alternative approach for interferometric lasers over those described above uses distributed coupling between an active and a passive waveguide. Optimization of the effective reflectance was carried out by means of the scattering matrix. Experimental demonstration of single-longitudinal-mode operation and good temperature stability was achieved with coupled guides made by six layers of GaAlAs grown on an etched substrate with narrow mesa (23).

Coupling between single-mode fibers has been found useful for a variety of purposes (24) and may in some cases be used as an external coupling for some of the functions described above. The difficult technique of etching and positioning such fibers for controlled coupling was consequently developed (25).

Extensive work in generating subpicosecond pulses by colliding-pulse mode locking (26) of ring dye lasers has continued, including analysis of the role of the interference grating on stability and pulse formation in this configuration (27,28). The short pulses have been used for studies of excitation and recombination effects in photoconductive switches on GaAs and InP (29). Detailed analyses of the dispersive effects of the electrical pulses generated by the switching process have also been made (30,31).

Selected papers describing this related work include items 13, 23, 25 and 27-31 of the Reference list.

Significant Accomplishments

The interferometric principle of mode control, tuning, or wavelength switching of semiconductor lasers has been firmly demonstrated. Several configurations are possible for this, with an open-ended Michelson interferometer, two versions of a multi-cavity interferometer, and a coupled-waveguide version demonstrated. Stability performance comparable to that of DFB or DBR lasers has resulted, with optimization of either stability or tuning analyzed by the scattering-matrix approach.

Two new sets of results not yet published are worth mentioning. First, a continuous wavelength tuning range of 4.5 Å (Fig. 1) and a quasi-continuous wavelength change over a range of .90 Å (Fig. 2) have been achieved in the IEI laser under separate pumping (32). Second, a new multiple-cavity laser, the multiple-twisted (MT) DH laser (Fig. 3), consisting of waveguide segments fabricated on an alternate channeled and terraced substrate has been tested (33). The MTDH laser showed a mode-stable temperature range 140°C and 25°C in another laser (Fig. 4). For both the IEI and the MTDH laser operating in the stable range, a mode-suppression ratio (dominant/side mode) in excess of 100: 1 was obtained.

Proposed Research Program

Because of the success of the several coupling mechanisms between active and passive semiconductor lasers, additional work will be done on these devices. Analysis by means of the scattering-matrix has given guidelines for optimization, either for mode stability, tuning or wavelength switching. There are many possible embodiments, however, and in addition to the four basic types tested so far (OEMI, IEI, IRI, MTDH and coupled waveguide types), modifications of these will be built, and parameters varied. We have so far stressed the issues of mode stability and wavelength tuning (12-15), but it may be interesting to look more carefully at optimization for wavelength switching in view of potential systems

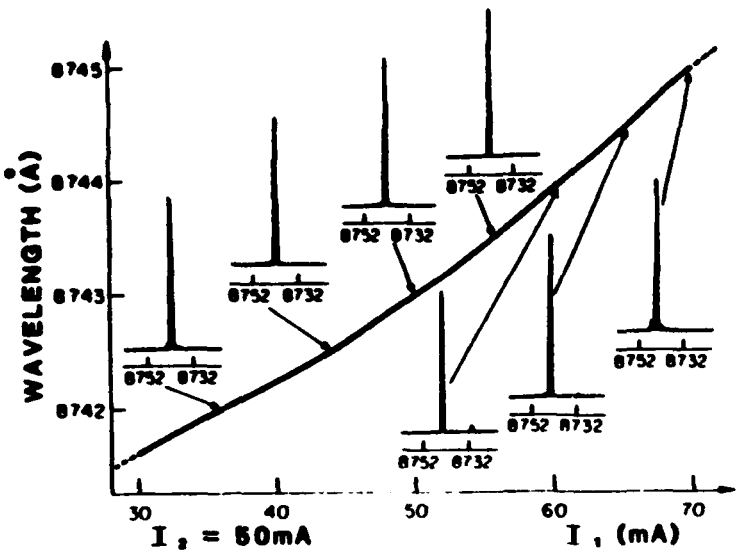

WAVELENGTH (Å)
8745
8744
8743
8742
8752 8732
30
40
50
60
70
I₂ = 50mA
I₁ (mA)

Fig. 1

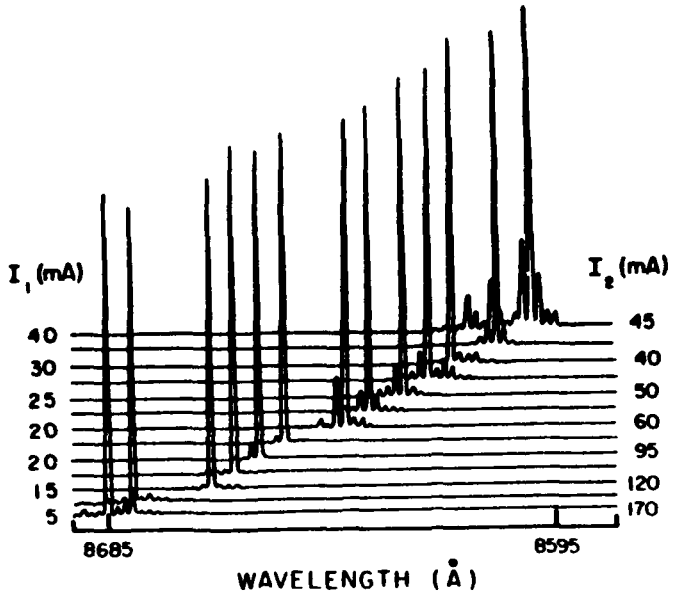
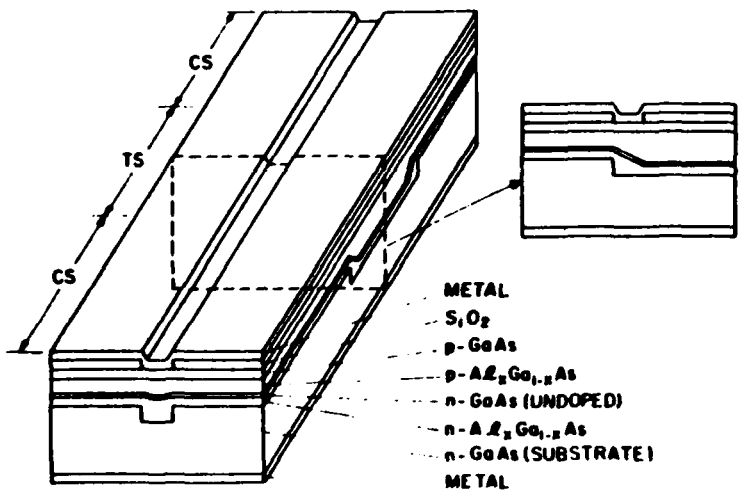
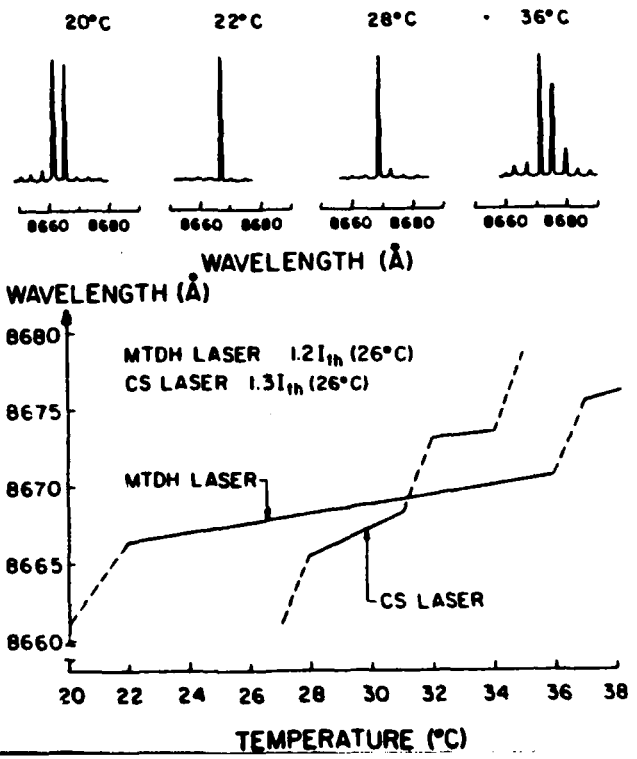

I₁ (mA)
I₂ (mA)
40
30
25
20
20
15
5
45
40
50
60
95
120
170
8685
8595
WAVELENGTH (Å)

Fig. 2


CS
TS
CS
METAL
SiO₂
p-GaAs
p-AlxGa1-xAs
n-GaAs (UNDOPED)
n-AlxGa1-xAs
n-GaAs (SUBSTRATE)
METAL


20°C
22°C
28°C
36°C
8660 8680
WAVELENGTH (Å)
WAVELENGTH (Å)
8680
8675
8670
8665
8660
MTDH LASER 1.2Ith (26°C)
CS LASER 1.3Ith (26°C)
MTDH LASER
CS LASER
20 22 24 26 28 30 32 34 36 38
TEMPERATURE (°C)

advantages of frequency-shift keying (FSK) systems (34).

The coupling of two active waveguides will be tried, using one of the networks developed for coupling of active and passive guides. The coupled waveguide approach, with coupling of two active guides to a central passive guide is one reasonable possibility. The Y junction developed for the OEMI laser (13) is another. For fabrication of these, plasma-etch capabilities for GaAs are being developed with the help of the Hewlett-Packard Company.

In the use of the coupling networks for picosecond pulse studies, the first experiments will be on pulse sharpening by nonlinear effects between coupled waveguides in GaAs. The configuration is similar to that used for the interferometric coupled waveguide laser (23); analysis has predicted a strong pulse sharpening effect (35). Tests will be with picosecond pulses from a synchronously pumped dye laser operating in the infrared. We also wish to design a ring configuration, colliding-pulse mode-locked semiconductor laser using the networks described, and the earlier experience with ring lasers (21). The biggest problem for this appears to be the selection of a suitable and durable saturable absorber. Studies of interaction between the picosecond pulses and the semiconductor, including the issue of dispersion, will continue (29-31).

References

(1) See for example *IEEE J. Quant. Elect.* vol. QE-17, no. 2 (February 1981), Special Issue on Quaternary Compound Semiconductor Materials and Devices

(2) M. K. Shams and S. Wang, *Appl. Phys. Lett.*, vol. 33, p. 170 (1978).

(3) S. Wang, C. Y. Chen, A. S. H. Liao, L. Figueroa, *IEEE J. Quant. Elect.*, vol. QE-17, p. 453 (1981).

(4) D. Botez and G. J. Herskowitz, *IEEE Proc.*, vol. 68, p. 689 (1980).

(5) E. M. Phillip-Rutz, *Appl. Phys. Lett.*, vol. 26, p. 15 (1975).

(6) W. T. Tsang, R. A. Logan and R. P. Solathe, *Appl. Phys. Lett.*, vol. 34, p. 162 (1979).

(7) B. F. Levine, R. A. Logan, W. T. Tsang, C. G. Bethea and F. R. Merritt, "Optically Integrated Coherently Coupled $Al_xGA_{1-x}As$ Lasers," *Appl. Phys. Lett.*, vol. 42, 339 (1983).

(8) P. T. Ho, L. A. Glasser, E. P. Ippen and H. A. Haus, *Appl. Phys. Lett.*, vol. 33, p. 241 (1978).

(9) E. P. Ippen, D. J. Eidenberger and R. W. Dixon, *Appl. Phys. Lett.*, vol. 37, p. 267 (1980).

(10) J. P. Vanderziel, W. T. Tsang, R. A. Logan, R. M. Mikulyak and W. M. Augustynaik, *Appl. Phys. Lett.*, vol. 39, p. 525 (1981).

(11) J. C. Au Yeung and A. R. Johnston, *SPIE Proceedings*, vol. 322, "Picosecond Lasers and Applications," p. 25 (1982).

(12) S. Wang, H. K. Choi and I. H. A. Fattah, *IEEE J. Quant. Elect.*, vol. QE-18, p. 610 (1982).

(13) I. H. A. Fattah and S. Wang, *Appl. Phys. Lett.*, vol. 41, p. 112 (1982).

(14) H. K. Choi and S. Wang, *Appl. Phys. Lett.*, vol. 40, p. 571 (1982).

(15) A. Antreasyan and S. Wang, *Appl. Phys. Lett.*, vol. 42, p. 562 (1983).

(16) W. T. Tsang, N. A. Olsson and R. A. Logan, *Appl. Phys. Lett.*, vol. 42, p. 650 (1983).

(17) B. F. Levine, R. A. Logan, W. T. Tsang C. G. Bethea and F. R. Merritt, "Optically Integrated Coherently Coupled $Al_xGa_{1-x}As$ Lasers," *Appl. Phys. Lett.*, vol. 42, 339 (1983).

(18) C. Lin and C. A. Burrus, Meeting on Optical Fiber Communications, New Orleans, LA February 28 - March 2 (1983).

(19) J. Katz, S. Margolit and A. Yariv, *Appl. Phys. Lett.*, vol. 42, p. 554 (1983).

(20) K. J. Russell, *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-27, p. 472 (1979).

(21) A. S. H. Liao and S. Wang, *Appl. Phys. Lett.*, vol. 36, p. 801 (1980).

(22) P. W. Smith, *Proc. IEEE*, vol. 60, p. 422 (1972)

(23) K. Kitayama, I. H. A. Fattah and S. Wang, submitted to *Appl. Phys. Lett.*, (1983); paper Th02, Conference on Lasers and Electro-optics, Baltimore, Md., May 17-20 (1983).

(24) M. J. F. Digonnet and H. J. Shaw, *IEEE J. Quant. Elect.*, vol. QE-18, p. 746 (1982).

(25) J. C. Lamb, "External Coupling Networks for Semiconductor Lasers," M.S. Report, EECS Department, University of California, Berkeley, June 1983.

(26) R. L. Fork, C. V. Shank, R. Yen and C. Hirlimann, *IEEE J. Quant. Elect.*, vol. QE-19, p. 500 (1983).

(27) K. K. Li, G. Arjavalingam, A. Dienes and J. R. Whinnery, *IEEE J. Quant. Elect.*, vol. QE-19, p. 539 (1983).

(28) G. Arjavalingam, "Study of Linear and Ring Configurations for the Passive Mode Locking of Dye Lasers," Ph.D. Thesis, EECS Department, University of California, Berkeley, June 1983.

(29) K. K. Li, J. R. Whinnery and A. Dienes, *SPIE Proceedings*, "Picosecond Lasers and Applications," vol. 322, p. 124 (1982).

(30) K. K. Li, G. Arjavalingam, A. Dienes and J. R. Whinnery, *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-30, p. 1270 (1982).

(31) G. Hosnain, G. Arjavalingam, A. Dienes and J. R. Whinnery, *SPIE Proceedings*, "Picosecond Optoelectronics," San Diego, Aug. 24, 1983.

(32) A. Antreasyan and S. Wang, accepted for publication in *Appl. Phys. Lett.*, vol. 43, September (1983).

(33) T. Sugino and S. Wang, accepted for publication in *Appl. Phys. Lettl*, vol. 43, September (1983).

(34) P. R. Prucnol, "Frequency-shift Key Modulation for Fiber-Optic Communications," NSF Grantee-User's Meeting on Optical Communication Systems, M.I.T., June 1, 1983.

(35) K. Kitayama and S. Wang, *Appl. Phys. Lett.*, vol. 43, p. 17, June 1, (1983).

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: QE-84-2 **Last Year's No.(s)** QE-83-2

Title: Electro-Optical Interactions in Quantum-Well Structures: Applications to Detection and Millimeter Mixing

Senior Principal Investigator(s):

T. K. Gustafson	(415) 642-3139
S. E. Schwarz	642-5684
R. M. White	642-0540

Scientific Objective

We would like to exploit and investigate layered structures of III-V alloy semiconductors with particular interests in high bandwidth electro-optic and millimeter-wave devices. Various characteristics, such as the high mobility and the lateral carrier confinement offered by these quantum-well structures provide advantages difficult to achieve otherwise for such applications as high speed optical detectors and phototransistors, frequency multiplexed detection, millimeter-wave mixers, oscillators, and modulators. In addition, other unique aspects of such structures such as the two-dimensional exciton and the discrete quantum mechanical transitions between the valence and conduction bands of the quantum well provide an opportunity for fundamental optical interaction studies.

The interplay between the millimeter-wave investigations and the optical studies proposed is particularly interesting with regard to potential applications involving millimeter frequency modulation, multiplexing, and detection of optical signals.

State of the Art

Recent progress by various workers (1-5), has led to the development of novel quantum-well devices. These are layered structures of III-V alloy semiconductors, designed in such a way as to provide current conduction through undoped GaAs layers with high mobility. For example in Fig. 1, the undoped GaAs acquires a thin layer of free electron gas at its border with the Si-doped AlGaAs. This gas is confined in a thin sheet by a conduction-band minimum known as a quantum well. The two-dimensional structure of this well also quantizes the electron states vertically so that discrete optical interband transitions are a possibility, as well as two dimensional exciton states.

A variety of millimeter and optical devices and spectroscopic investigations utilizing such quantum-well structures have been reported. In particular, high-electron-mobility transistors (HEMTs), especially for digital applications, be useful as analog devices in the millimeter range. For instance, they may be useful as low-noise amplifiers or as local oscillators in receivers. Their high mobility should allow relaxation of the small fabrication tolerances normally needed for millimeter-wave amplifiers.

Multiquantum-well lasers grown by molecular beam epitaxy have been fabricated and tested (6,7) and a low threshold has been reported, principally because of the decreased free carrier loss available from such lasers, as well as the quantized transitions. Picosecond superlattice (quantum-well) spectroscopy (utilizing a pulse probe technique) has been utilized to observe the two-dimensional aspects of the quantum well, such as the exciton levels the density of states, and the transient gain (9).

Recently C. Y. Chen et al. reported an ultrahigh speed modulation-doped heterostructure field-effect photodetector with a demonstrated 27 psec response time (10). A particular advantage was the high mobility of the carriers within the thin layer (66,000 cm^2/vs). Interestingly enough no optical gain on the picosecond time scale was reported for this particular configuration because, presumably, a steady state was not reached.

Our laboratory is actively engaged in research in millimeter-wave and optical devices and integrated circuits. This work involves not only semiconductor devices, but also electromagnetic structures. Our millimeter-wave efforts presently involve the fabrication of GaAs Schottky diode arrays for 70-GHz imaging; planar 70-GHz Gunn oscillators using vertical leads; as well as a variety of planar transmission lines and antennas for use in mm-wave integrated

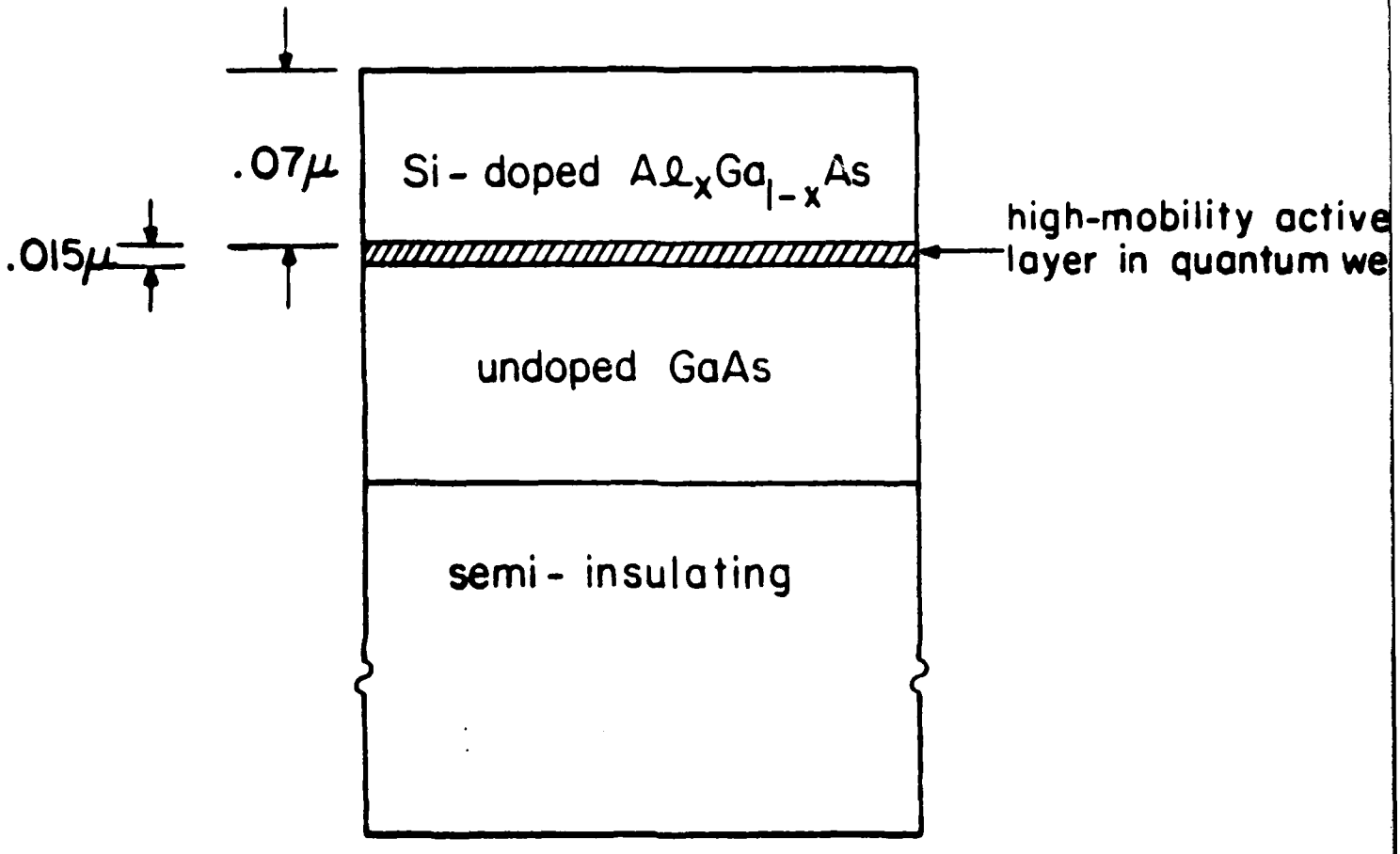


Fig. 1. Three-layer quantum-well structure.

circuits. Considerable 70-GHz test apparatus is available. Lower-microwave-frequency apparatus is also available for use in simulation and design. A 200 keV proton-implanter is available.

We have been interested in a surface lateral structure of the form of an M-I-S-I-M (11), which we have established displays field effect photoresistor characteristics for continuous wave illumination. It is felt that the gain arises from the larger barrier height for holes with respect to that for the electrons at the M-I-S interface acting as the source (12). If this turns out to be the case, the gain should be limited by a single transit time of the device, since the transit time of the M-I-S junction which limits the gain is much shorter. Thus one would expect the cutoff frequency for gain to be much higher than that for the modulation-doped structure fabricated by Chen at al (10). This presence of gain for short times is presently being checked with a silicon device utiliuzing pictosecond optical pulse illumination.

Both the increased mobility and the current confinement offered by the quantum-well structure would be advantageous for this lateral detector, which operates by absorption within the quantum well.

We expect that the necessary layered III-V compound structures can be made with the molecular-beam-epitaxy apparatus of Professor Shyh Wang in our laboratory. Alternatively, the material, which is relatively common since it is the same as that used in HEMTs, will be obtained from outside laboratories engaged in HEMT research.

Progress and Publications Since Last Major Proposal

Publications Acknowledging JSEP Support:

(1) "Planar Multimode Detector Arrays for Infrared and Millimeter-Wave Applications," by D. B. Rutledge and S. E. Schwarz, *IEEE J. Quantum Electronics*, QE-17, 407-414 (March 1981).

(2) "A High-Speed Si Lateral Photodetector Fabricated over an Etched Interdigital Mesa," by C. W. Chen and T. K. Gustafson, *Appl. Phys. Lett.*, 87, 1014 (1980).

(3) "Characteristics of an Avalanche Phototransistor Fabricated on a Si Surface," C. W. Chen and T. K. Gustafson, *Appl. Phys. Lett.*, 39, 161 (1981).

(4) "A Phototransistor With Concentric Electrodes on the Silicon Surface," *IEEE Electron Device Letters*, EDL-2, 200 (1981).

(5) :Monolithic Integration of a Dielectric Millimeter-Wave Antenna and Mixer Diode: An Embryonic Millimeter-Wave IC," C. Yao, S. E. Schwarz and B. J. Blumenstock, *IEEE Trans. Microwave Theory and Tech.*, MTT-30, 1241-1247 (August 1982).

(6) "Planar Oscillators for Monolithic Integration," N-L. Wang and S. E. Schwarz, *Int'l. J. of Infrared and Millimeter Waves*, 3, 771-782 (November 1982).

(7) "Design of Dielectric Ridge Waveguides for Millimeter-Wave Integrated Circuits," T. Wang and S. E. Schwarz, *IEEE Trans. Microwave Theory and Tech.*, MTT-31, 128-134 (February 1983).

(8) "Design and Performance of Coplanar Waveguide Bandpass Filters," D. F. Williams and S. E. Schwarz, to appear in *IEEE Trans. Microwave Theory and Tech.*

Theses:

"High Speed Photodetectors with Interdigital Mesa Structures on Si Surfaces," Ph.D. Thesis, D. C. Chen, May 1981.

"High-speed Surface Lateral M-I-S-I-M Photodetector," Ph.D. Thesis, S. Thaniyavarn, May 1983 (partial support).

Under Other Sponsorship (Related):

(1) "Superconductor-Insulator-Superconductor Reflection Parametric Amplifier," G. S. Lee, *Appl. Phys. Lett.*, 41, 219-293

(2) Numerical Studies of Mutual Locking of Resistively and Capacitively Shunted Josephson Junctions,", G. S. Lee and S. E. Schwarz, submitted to *Appl. Phys. Lett.*

(3) "Relation of Stimulated and Spontaneous Transitions in Tunneling Structures to the Elastic Current-Voltage Characteristic, S. R. Whiteley, L. Z. Xie, R. Hemphill and T. K. Gustafson, *Appl. Phys. Lett*, 41, 868 (1982).

(4) "Stationary State Model for Normal Metal Tunnel Junction Phenomena," S. R. Whiteley and T. Kenneth Gustafson, *IEEE J. Quantum Electronics*, QE-18, 1387 (1982).

(5) "Surface Metal-Oxide-Silicon-Oxide-Metal Picosecond Photodetector," S. Thaniyavarn and T. K. Gustafson, in *Picosecond Phenomena III*, (Ed. K. B. Eisenthal, R. M. Hochstrasser, W. Kaiser and A. Laubereau), page 137.

(6) S. Thaniyavarn and T. K. Gustafson, "Metal/Tunnel-Barrier/Semiconductor/Tunnel-Barrier/Metal Fast Photodetector," *Appl. Phys. Lett.*, 40, 255 (1982).

Significant Accomplishments

1) Reference 1, the development of planar multimode detector arrays as well as Reference 2, the monolithic integration of a dielectric millimeter-wave antenna and a mixer diode.

2) The development of a mesa detector as described in Reference 2, and in C. W. Chen's thesis.

3) In Reference 5, the description and data relating to the development of a lateral M-I-S-I-M photodetector, which relates directly to the effort proposed herein.

Proposed Research Program.

We wish to explore fundamental characteristics and applications of the quantum-well principle in the millimeter and optical region of the spectrum. Aside from the aspect of high mobility, quantum-well devices are promising for millimeter-wave structures because of their inherently planar form. Most high-frequency semiconductor devices are "vertical" (i.e. they involve conduction normal to the semiconductor surface). However, for high-frequency devices integrated circuit planar fabrication technology must be used, and fabrication of vertical devices is relatively inconvenient. The quantum-well principle has a significant advantage in that it confines current conduction to a thin sheet parallel to the surface. This allows us to avoid earlier problems with "lateral" devices, for which current flow was unconfined and operation was confused by the existence of many current paths of different lengths.

(a) Millimeter-Wave Devices

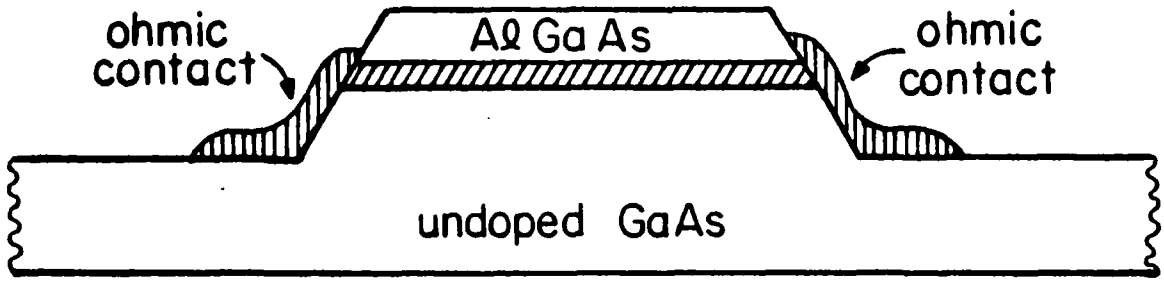


Fig. 2. Planar quantum-well Gunn oscillator

We propose an investigation of the planar Gunn oscillator configuration shown in Fig. 2. Here the high-mobility active layer forms a conduction path between two ohmic contacts. (The path is not short-circuited through the AlGaAs because the latter is depleted due to band-bending.) This structure is much easier to fabricate than a vertical device, and the current path is confined in the vertical direction. If desired, current paths can also be confined in the horizontal plane by proton implantation. A top view of this version of the device is shown in Fig. 3. In this case, motion of the electrons is highly linear, which should lead to predictable, efficient operation. The high mobility of the active layer will tend to increase the average carrier velocity (although not proportionally, owing to velocity saturation). This is beneficial as it increases the oscillation. High mobility will also reduce ohmic loss, thus increasing efficiency and reducing heat dissipation.

Since the current-carrying layer is very thin, the device must be wide (perhaps one centimeter) in order to obtain useful amounts of output power. This suggests that the active paths be placed between the conductors of a planar transmission line. This would yield a very convenient planar oscillator structure.

At high frequencies it can be difficult to impose amplitude or frequency modulation on the output of an oscillator. In the proposed planar oscillator this can be done by borrowing from the HEMT principle, as shown in Fig. 4. A Schottky contact above the active layer is reverse-biased, thus depleting the quantum well. This structure will provide very effective control of the oscillator output, with very little modulation power being needed. Small voltages applied to the control electrode can be used to modulate the oscillator output. (What mixture of AM and FM will result remains to be determined.) Larger voltages can be used to turn the device on and off entirely.

Wafers of quantum-well material will be fabricated by MBE in our laboratory or obtained from outside sources. Initially a comparatively large, low-frequency Gunn oscillator will be fabricated and tested. The experimental observations will be studied and compared with theory in order to learn the effects of (a) high mobility, (b) 2-dimensional geometry, and (c) one-dimensional geometry. A control electrode will be added in order to investigate the modulation properties of the device.

After study of these experimental results, we plan to design a millimeter-wave version of the Gunn device. This will probably take the form of a travelling-wave oscillator as described above. Tunability and noise studies of this device will be made. Modulation experiments will be carried out by providing control electrodes for the traveling-wave oscillator.

(b) Optical Devices

We would like to propose optical experiments involving the M-I-S-I-M structure which we have been investigating in silicon. The structure envisioned would have a form similar to Fig. 1 except that an insulating la I) would be deposited (or grown) on the mesa edges as shown in Fig. 5. The mesa semiconductor material (S) would ideally be a multi-quantum-well structure and the band diagram across the mesa following the well would ideally appear as in Fig. 6. The wells could be modulation-doped. A bias in general would be applied to sweep the carriers towards the electrodes.

The optical sensitivity of such a detector as a function of wavelength would be of initial interest. Since there is confinement of the electrons in the vertical direction one would expect to observe a peak response corresponding to the two-dimensional exciton levels and to transitions corresponding to a "particle

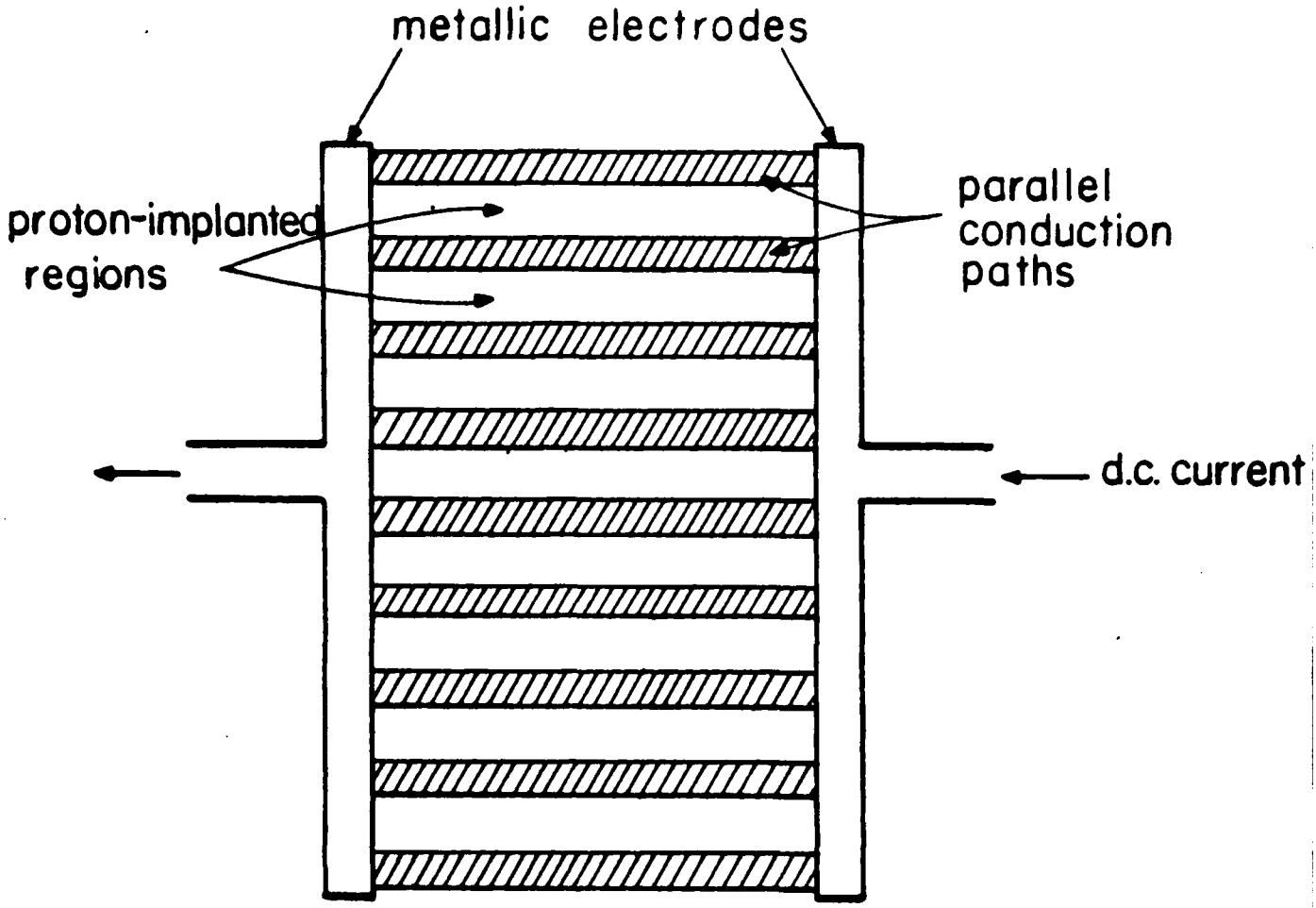


Fig. 3. Parallel Gunn oscillators with linear current paths.

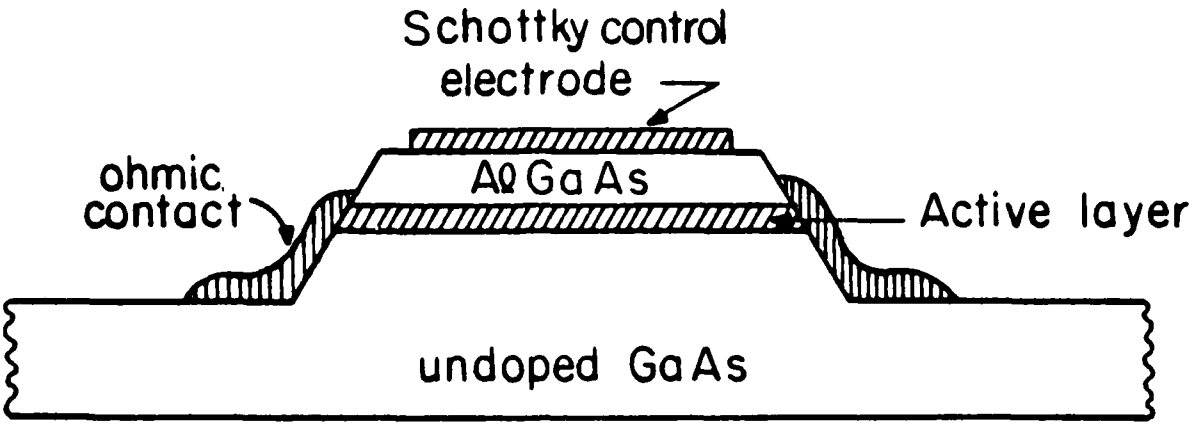


Fig. 4. Planar Gunn oscillator with control electrode.

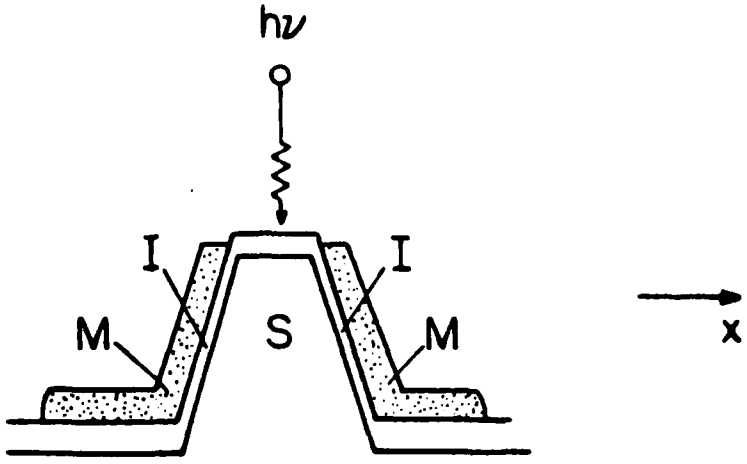


Fig. 5. The M-I-S-I-M photodetector fabricated on a quantum well.

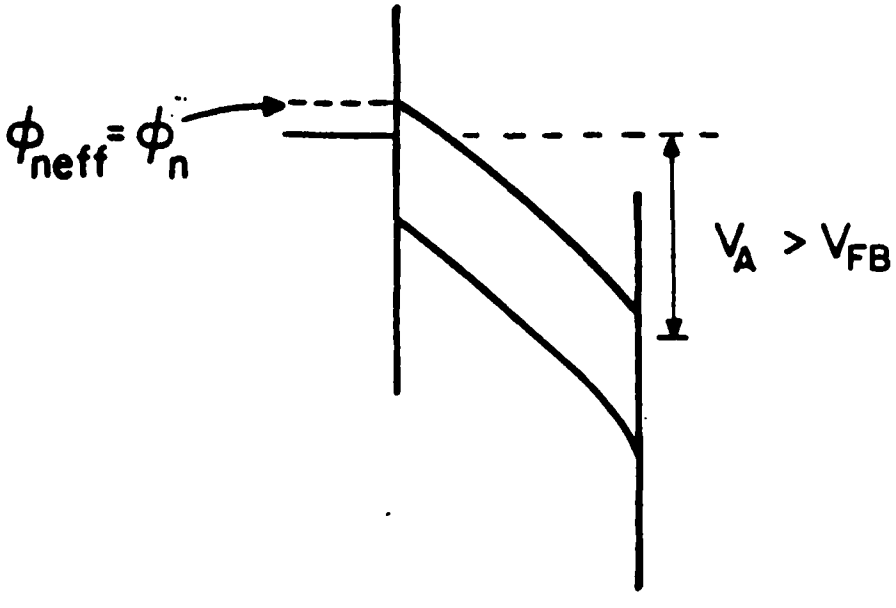


Fig. 6. Ideal band diagram across (x-direction) the mesa of the detector of Fig. 4 along the quantum well.

in a box". The multi-quantum well would allow one to establish a reasonable absorption of the radiation. For shorter wavelengths one would expect continuum absorption in the gallium aluminum arsenide.

There are several investigations which would be of interest. Initially the d.c. dark current voltage characteristics would be obtained. For illumination with a tunable dye laser across the band-gap of the wells we would like to study the photo response as a function of applied bias and illumination intensity. This should result in:

a) the establishment of a gain for photo excitations

b) the zero illumination limit of saturated carrier flow in the GaAs quantum well

c) the avalanche breakdown threshold

d) the presence or absence of an exciton resonance response.

Picosecond illumination with a mode-locked dye laser would be utilized to investigate and establish a response time superior to an M-I-S-I-M lateral detector not utilizing a quantum well for two reasons:

(1) the high mobility of carriers in the quantum well

(2) the limitation of the absorption of the radiation to the quantum well near the absorption edge.

Many other interesting devices are possible, if arbitrarily-layered material structures can be mode. The ideas presented above are based on the use of "standard" quantum-well material, which is fairly widespread. If sufficient success with MBE is achieved in our laboratory, we plan to extend our work to other novel devices based on different epitaxial heterostructure profiles.

References

(1) R. Dingle, H. L. Stormer, A. C. Gossard and W. Wiegeman, *Appl. Phys. Lett*, 33, 655 (1978).

(2) T. Mimura, S. Hiyamizu, T. Fujii and K. Nanbu, *Japan J. Appl. Phys.*, 19, L225-L227 (May 1980).

(3) T. Mimura, S. Hiyamizu, K. Joshin and K. Hikosaka, *Japan J. Appl. Phys.*, 20, L317-L319 (May 1981).

(4) T. Mimura, K. Joshin, S. Hiyamizu, K. Hikosaka and M. Abe, *Japan J. Appl. Phys.*, 20, L598-L600 (Aug. 1981).

(5) M. Abe et al., *IEEE Trans. Elec. Dev.*, ED-29, 7, 1088-1095 (July 1982).

(6) D. R. Scifres, R. D. Burnham and W. Striefer, *Appl. Phys. Lett*, 41, 118 (1982).

(7) S. Yamahoshi, O. Wada, T. Fujii, S. Hiyamizu and T. Sakurai, International Electron Device Meeting, San Francisco, Dec. (1982), paper 13.3.

(8) C. V. Shank, lecture presented April 21, 1983, University of California, Berkeley.

(9) C. Y. Chen, A. Y. Cho, C. G. Betheas, P. A. Garbinski, Y. M. Pang, B. F. Levine and K. Ogawa, *Appl. Phys. Lett.*, 42, 1041 (1983).

(10) Ph.D. Thesis, S. Thaniyavarn, University of California, Berkeley (1982).

Interaction with Other Units

EM-85-2 and QE-84-2.

University of California — Electronics Research Laboratory

Joint Services Electronics Program — August 15, 1983

III. A. Basic Research in Solid State Electronics—Materials — Coordinator: Professor S. Wang

General

We propose to perform research in solid state electals in the following areas:

(1) Use of silicides and regrown silicon as materials for interconnects, gate electrodes, and/or active layers and feasibility study of three-dimensional packing of devices to advance VLSI MOS technology,

(2) Use of MBE growth process and high-energy ion implantation for fabricating multiple levels of GaAs-based devices with low defect density,

(3) Studies of interface problems of compound semiconductors.

Two important aspects to the advancement of microelectronics are interface and interconnect problems. Even for silicon integrated circuits for which the technology is well advanced, important materials issues remain to be answered. One issue concerns the selection of a common material for the gate electrode and for the interconnect between devices. Recent work in our laboratory has shown that silicides and regrown silicon are very promising as an alternative to poly-silicon which is widely used at present. Another relatd issue concerns the electorde-dielectric interface. Problems of particular interest are possible thin-film reactions and carrier transport across the oxide. A research program on the above topics as well as on a novel device structure as a feasibility test of three-dimensional packing of devices is presented under SSM-1 entitled "Materials Issues in VLSI Interconnections."

It is conceivable that fabrication of future submicron electronic devices will involve a combination of several growth and procesing steps. In our laboratory, using the Riber 1000 MBE system, we have been able to grow GaAs and (GaAl)As films showing excellent surface morphology and photoluminescence spectrum. Also bipolar and NMOS transistors have been fabricated with high-energy ion implants into silicon. Device performance of both types indicates that the surface layer after implantation is of device quality. Two basic components in a multi-level device architecture are electrical isolation and interconnects between devices. Besides, both the MBE grown layer and the ion implanted layer must have low defect density. A research program to study the growth kinetics of MBE process to minimize defect density and to investigate high-energy ion implantation in GaAs is presented in SSM-2 entitled "Studies of MBE Growth Kinetics and High-Energy Ion Implantation in Compound Semiconductors."

With the successful demonstration of ultra high-speed devices, such as the HEMT and the direct-coupled GaAs MESFET, the future of compound semiconductors as a viable complement to Si in VHS IC is indeed very bright. To explore the GaAs-based technology to its full potential, two basic problems, the semiconductor-insulator interface and the semiconductor-metal interface, need to be thoroughly studied and substantial improvements of interface properties have to be made. In our laboratory, we have nearly completed a high-

vacuum deposition chamber with e-beam evaporation capability. The new chamber separate from the MBE system will be used in exploratory experiments, for example, to co-deposit II and VI elements and to deposit reractory metals on MBE-grown films under high vacuum. A research program to study the interface of lattice-matched II-VI and III-V films and to investigate the metal-GaAs interface with refractory metals introduced as interdiffusion barrier is presented in SSM-supplement entitled "Studies of Interface Problems of Compound Semiconductors."

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: SSM-84-1 **Last Year's No.(s):** N.A.

Title: Materials Issues in VLSI Interconnections

Senior Principal Investigator(s):	N. W. Cheung	(415) 642-1615
	C. M. Hu	642-3393
	W. G. Oldham	642-2318

Scientific Objective

Future advances in MOS technology depend critically on the communication between on-chip devices, because of the delays incurred in signal propagation over ever-increasing line lengths. To maintain the phenomenal packing density and circuit efficiency, the conductor must also serve as MOS gate material. Compounds of metals and Si (i.e.,silicides) offer a better alternative to poly-Si for VLSI metallization. The silicides are highly conductive and they can be isolated from other electrically active regions with conformal grown or deposited oxide on the surface.

Another approach to solving the interconnectivity problem is simply to reduce line length. Given the need for higher complexity, it is attractive to consider three dimensional packing of devices to reduce device-device spacing. As a potentially higher payoff alternative, lateral **solid-phase** epitaxial growth of amorphous Si on insulators (e.g.,SiO_2 and Si_3N_4) offers the advantage of being a low-temperature process. We envision the regrown Si film can serve as the active layer, the gate electrode or even interconnects in multi-layered device structures.

The proposed study is to investigate the metallurgical and electrical properties of the silicides and the laterally regrown Si. Their impact on device performance and reliability will be emphasized. In particular, we will study their effects on the integrity of dielectrics both lying under and grown over these materials in terms of transport properties, charge trapping characteristics, interface traps, interface mobility, and time-dependent breakdown. The objective is to accumulate basic knowledge and to identify optimum processing parameters for this new metallization and recrystallization technologies. To demonstrate the feasibility of three-dimensional packing of devices, a merged CMOS static RAM cell and a dense dynamic RAM cell are proposed as test device structures.

State of the Art

As device dimensions continue to decrease due to the increasing level of integration, the technology of metallization on integrated circuits is becoming increasingly important. Most current approaches to improving circuit density and performance are based on some form of scaling. Given the need to shrink oxide thickness, to shrink conductor width and thickness, to increase chip size (and thus line length) while reducing circuit delays, there is clearly a need for lower resistivity conductor materials. Besides the general requirements of low contact resistance, the metallization materials for VLSI applications have to be compatible with multilevel metallization designs. The material must also be capable of withstanding higher temperature ($\geq 600^{\circ}C$) annealing to remove radiation damage because definition of micron and submicron linewidths usually requires the ion bombardment of plasma etching. At present, highly doped poly-Si has been widely used for interconnections because of its high temperature process compatibility.However, its resistivity is becoming objectionable as we go to narrower interconnect geometries. The large grains of poly-Si (due to doping and annealing) is also an undesirable feature for finer pattern definitions. Refractory metal silicides deposited on poly-Si films (polycides) have been proposed as an alternative to poly-Si [1,2]. The scheme utilizes both the high conductivity of a silicide and the stable poly-Si/SiO_2 interface. Success of using the silicide alone as the gate electrode has also been reported [3]. Silicides such as $MoSi_2$,$TaSi_2$,$TiSi_2$ and WSi_2 are potential candidates because they can be thermally oxidized and plasma etched with processing conditions similar to those of poly-Si [4].

In contrast to laser annealing or strip-heater annealing, the lateral solid-phase epitaxy process offers the distinct advantage of being a low temperature process (<900° C) . Thus, true three dimensional circuits are potentially possible, since localized melting is unnecessary. Dopant redistribution, thermal stresses, and reflow of CVD glasses will be minimized due to the low temperature annealing cycles. Vertical solid-phase epitaxial growth of deposited amorphous Si films on (100)Si at 550°C has been demonstrated by von Allmen et al. [5] and Saitoh et al. [6]. In the presence of interfacial contaminants, the growth mechanism is believed to be vertical growth of isolated epitaxial columns which subsequently grow laterally to consume the remaining amorphous Si. Layer-by-layer epitaxial growth at rates comparable to those found in implanted amorphous Si has also been observed by Hung et al. [7]. Recently, we have demonstrated the lateral regrowth of LPCVD amorphous Si over SiO_2 windows by solid-phase epitaxy[8]. The single-crystal lateral regrowth proceeds 3 to 4 microns from the oxide window edge; a result consistent with that of Kunii et al. [9,10]. Our TEM studies showed that the spatial extent of the lateral growth is limited by the random nucleation of poly-Si on SiO_2.

One area of special concern even for the scaled but otherwise conventional NMOS and CMOS technologies is the integrity of gate dielectrics. We have developed several techniques for the modeling and characterization of charge transport and trapping in oxides. We have developed the theory of current transport (tunneling) in oxide and verified it experimentally with oxides 34 to 400 A thick and voltages as low as 0.5V [11,12]. From C-V and bidirectional I-V measurements, we can determine the quantities and locations of trapped holes and electrons as well as the rates of electron trapping and interface-traps generation. Furthermore, we have correlated these traps with the degradations of surface mobility and the subthreshold-current slope, and the shift of the threshold voltage [13,14]. Some preliminary research has also be completed on the causes of the time-dependent breakdown phenomenon [15].

Proposed Research Program

We propose a coordinated fabrication/materials/device study.

(1) Material and Fabrication Studies

A) Silicide Fabrication

Presently, the dominant technique for the deposition of silicide films is sputtering. We propose to begin the materials and device studies using composite polysilicon/silicide structures with the silicide deposited by sputtering. For comparative studies, silicide films formed by CVD will be obtained initially from outside sources. The emphasis will be on low-temperature approaches, especially plasma-excited processes. If possible, a commercial reactor, or possibly a modified commercial reactor of the type now being developed for tungsten silicide will be obtained. We will also examine the feasibility of small hot-wall reactors similar to the very successful silicon nitride reactor we developed for growth of ultra-thin nitride dielectric films [16].

We will study the interaction of the gate electrode with the entire process sequence. We are especially concerned with the limits posed on process temperature and atmosphere subsequent to film deposition. We will investigate the ability to perform glass flow, both using low transition temperature boron-phosphorus glasses[17] and rapid annealing procedures . The ability to form buried contacts and control the spiking of shallow junctions is of major significance.

B) Silicide Thin-film Reactions

Since the stoichiometry of the deposited silicide depends on the fabrication parameters, the annealing cycles can create segregation of the disilicide and poly-Si phases(in case of excessive Si), or segregation of the disilicide and metal phases (in case of excessive metal). Both cases will affect the sheet resistivity and oxidation properties of the silicide layer. For excessive metal in the as-deposited composition, the metal can consume more Si from the poly-Si pad underneath to form a new layer of disilicide. The silicide/Si interface morphology formed by solid phase reaction is usually laterally nonuniform[18,19,20]. Due to the rapid diffusion along grain boundaries of the poly-Si, spikes of silicide can form with their apexes reaching the poly-Si/SiO_2 interface. In severe cases , the spikes can even create dielectric shorts for MOS structures. Hence, the thickness and grain size of the poly-Si pad will play an important role in the reliability and performance of MOS devices.

In this study, we proposed to investigate the dependence of various silicide reactions on annealing temperature, annealing ambient and as-deposited composition. The proposed research will seek to further the understanding of silicide oxidation mechanisms and the silicide reactions with metals, poly-Si and crystalline Si. The interfacial reactions will be probed by Rutherford Backscattering Spectrometry (RBS) [21] .Using this technique, depth profiles of the reaction components can be measured nondestructively and the analysis time is on the order of ten minutes per sample. The RBS analysis will be carried out at the 2 MeV Van de Graaff accelerator facilities of the Lawrence Berkeley Laboratory at UC-Berkeley. Changes in microstructures and phase segregation effects of the silicide films will be studied by Transmission Electron Microscopy (TEM) both in the plan-view and cross-sectional modes. The metallurgical studies will be correlated to the device related properties discussed in Section 2.

C) Electrical Properties of Silicide/Si Interfaces

To minimize the number of IC processing steps, it is preferable to use the same silicide for both contacts and interconnections.For contact applications, the silicide/Si contact resistance at the source and drain will depend on the presence of interfacial impurities such as native SiO_2. To circumvent this problem, we propose to use a slightly metal-rich silicide composition for contact applications. The excessive metal can react with the Si substrate by solid phase reactions to form a thin silicide layer and a relatively oxygen-free silicide/Si interface is obtained. At the Electronics Research Laboratory of UC-Berkeley, we have developed a self-aligned test structure to measure contact resistance with contact openings down to 1 micron in size. The 1-micron metal lines are usually defined by a lift-off process and this technique will be tested with the co-sputtered silicides. The contact resistance and its dependence on processing parameters (i.e., annealing conditions and interface dopant concentration) will be characterized by the Transmission Line Model [22] using four-point probe measurements. Schottky barriers heights of the silicide/Si interface will also be determined with Schottky diode structures.

D) Lateral Recrystallization of Si over SiO_2

In the Si regrowth over SiO_2 studies, we propose to extend the solid-phase technique to the lateral growth of recrystallized Si on SiO_2 and Si_3N_4. Contact holes will be opened in the dielectric films to provide the seed required for epitaxial growth. The amorphous Si film will be deposited by CVD or E-beam evaporation. The CVD process is preferable because HCl can be introduced in the gas stream to clean the Si substrate surface prior to amorphous Si deposition.

Both furnace annealing and halogen-lamp heating will be explored in the preliminary studies.

We will investigate the kinetics of random nucleation of poly-Si on dielectric films versus those of lateral epitaxial growth. Our preliminary results have shown that the former mechanism can be delayed by ion implantation of impurities at the vicinity of the amorphous Si/SiO_2 interface. Mechanisms of the delayed nucleation process due to interface ion-beam mixing will be studied in detail. Effects of the contact opening geometry on lateral epitaxy will be studied by a planar-seed structure and an indented- seed structure. Both structures were based on the birds-beak free local oxidation process developed here at Berkeley[23].

Material characterization of the regrown Si film will be performed using plan-view and cross-sectional electron microscopy ,and Hall measurements. Trace impurities in the film will also be analyzed by SIMS.

(2) Device Related Properties and Structures

A) Interface Carrier Transport and Dielectrics Reliability

Several device properties will be studied for devices fabricated on laterally regrown silicon and devices having refractory-metal/silicide gates. Surface mobility is one parameter to be monitored routinely. Gate materials, when properly deposited, should not have significant effects on mobility. Minor mobility degradation may result from scattering from excess interface traps or fixed charges. Severe degradation would be indicative of gross disturbances at the interface as described in Section 1. This discussion also applies to recrystallized silicon films. In the recrystallized films, mobility ranges from 20% lower (for laser recrystallization) to 5% higher (for strip heater recrystallization due to frozen-in strain) than in single-crystal substrates. The threshold voltage is often high in the early stage of developing a new regrowth technique, indicating high densities of interface traps. The small threshold voltage shifts sometimes observed as the results of using refractory-metal/silicide gates may be symptomatic of physical or chemical disturbances at the Si/SiO_2 interface and their cause will be investigated. Any observed changes in surface mobility or threshold voltage will be correlated with the results of metallurgical studies described in Section 1.

We propose to study the impacts of silicide gates and lateral epitaxy on the oxide breakdown voltage and time-dependent dielectric breakdown (TDDB), charge trapping, and the generation of interface traps. We will study both the oxides under the silicide gates and the regrown silicon film, and the oxides thermally grown on these materials.

We will employ the dielectrics characterization techniques (mostly developed in our laboratory and described in the State-of-the -Art section) to study the charge transport, charge trapping, and integrity of the oxides present under and grown over the silicide gates and the silicon films regrown by lateral epitaxy. The oxide properties will be correlated with the physical and chemical studies described in Section 1 for a more complete basic understanding of these material systems and optimized fabrication methods.

B) Three-Dimensional Packing of Devices

Multi-layered testing device structures using laterally regrown Si on insulators will be fabricated in this study. For example, a merged CMOS inverter [or

half of a static RAM cell] can be made with the load transistor on the regrown layer and the drive transistor in bulk Si, both sharing the common gate oxide. By aligning the n^- region of the p-channel device over the n^+ region of the n-channel device, the drain(or source) of one device will become the gate of the other.Due to the efficient sharing of gates and the elimination of n-well isolation for the p-channel device, the memory cell layout is smaller than any existing NMOS static RAMs. Considerable success with similar structures has been achieved both in the US and abroad even with the laser melting/recrystallization techniques. We expec the proposed low-temperature lateral epitaxial growth method to result in much greater manufacturability and be truly benign to any structures existing.

A more novel device structure that we propose to investigate is a dynamic RAM cell that achieves high density, superior refresh time, and practical immunity to alpha-induced soft errors. This DRAM cell has its address transistor in recrystallized silicon. The drain of this transistor physically contacts the bit line diffusion through an opening in the oxide. This opening serves, of course, as the seed of lateral solid-phase regrowth of the amorphous silicon. Good crystalline quality is only required up to the channel/source junction, which may only be 4 microns away from the opening, within the demonstrated capability of the proposed regrowth technique [8].Beyond this point, the recrystallized silicon may well be polycrystalline since it only serves as one plate of the storage capacitor. The other (ground) plate is made of a second layer of poly-Si.

References

[1] B.L. Crowder and S. Zirinsky, "1-Micron MOSFET VLSI Technology,Part VII: Metal Silicide Interconnection Technology -- A Future Perspective," *IEEE Tran. Electron Devices, Vol. ED-26*, p.369,1979.

[2] M.Y.Tsai,H.H. Chao,L.M.Ephrath, B.L. Crowder,A. Cramer,R.S. Bennett, C.J. Lucchese,and M.R. Wordeman, " One-Micron Polycide(WSi_2 on Poly-Si) MOSFET Technology", *J. Electrochem. Soc.,Vol.128*, pp. 2207-2214,1981.

[3] K.C. Saraswat, F. Mohammadi, and J.D. Meindl, "WSi_2 Gate MOS devices", *IEDM Digest, p.462,1979.*

[4] K.L.Wang,T.C. Holloway, R.F. Pinizzotto, Z.P. Sobczak,W.R. Hunter, and A.F. Tasch,Jr., "Composite $TiSi_2/n^+$ Poly-Si Low Resistivity Gate Electrode and Interconnect for VLSI Technology," *IEDM Digest,pp.58-61,1981.*

[5] M. von Allmen,S.S.Lau, J.W.Mayer, and W.F.Tseng, "Solid State Epitaxial Growth of Deposited Si Films," *Appl.Phys. Lett.,Vol.35*, pp.280-282,1979.

[6] S.Saitoh,T.Sugii,H.Ishiwara, and S. Furukawa, "Growth Conditions of Deposited Si Films in Solid Phase Epitaxy," *Japan J. Appl. Phys., Vol.20*, pp. L130-L132,1981.

[7] L.S.Hung,S.S.Lau,M.von Allmen,J.W.Mayer, B.M. Ullrich,J.E. Baker, P.Williams and W.F. Tseng, "Epitaxial Growth of Si Deposited on (100) Si," *Appl. Phys. Lett.,Vol.37*, pp.909-911 ,1980.

[8] Y.Y. Wang, C. Jiou, D.K. Sadana, N.W. Cheung, and M. Strathman, "Solid-Phase Lateral Epitaxy of LPCVD Amorphous Si over SiO_2 Windows," *paper presented at*

the ECS Meeting, San Francisco, CA ,1983.

[9] Y.Kunii,M.Tabe, and K.Kajiyama, "Solid-Phase Epitaxy of CVD Amorphous Si Film on Crystalline Si," *Jap. J. Appl. Phys., Vol.21* , pp. 1431-1436,1982.

[10] Y.Kunii,M.Tabe, and K. Kajiyama, "Solid-Phase Lateral Epitaxy of CVD Amorphous Si by Furnace Annealing," *J. Appl. Phys.,Vol. 54*, pp. 2847-2849,1983.

[11] C. Chang, R.W. Brodersen, and C. Hu, "Direct and Fowler-Nordheim Tunneling in Thin Gate Oxide MOS Structures," *INFOS, Apr. 1983*, To be published by North Holland Publishing Co.

[12] C. Chang, R.W. Brodersen, M.S. Liang, and C. Hu, "Direct Tunneling in Thin Gate-Oxide MOS Structures," *Device Research Conference, June 1983.*

[13] M.S. Liang, Y.T. Yeow, C. Chang, C. Hu, and R.W. Brodersen, "MOSFET Degradation due to Stressing of Thin Gate Oxide," *IEDM Digest*, pp.50-53,1982.

[14] C. Chang, M.S. Liang, C. Hu, and R.W. Brodersen, "Charge Tunneling and Impact on Thin Oxide Device Reliability," *Electrochemical Society Meeting, May 1983.*

[15] C. Chang, M. Liang, T.Y. Chiu, W. G. Oldham, "Charge Transport in Oxide, Nitrided Oxide, and Nitride Films," *IEEE VLSI Workshop, Hyannis Mass., May 1982.*

[16] S. Wong and W. G. Oldham, "Silicon Nitride formed by Plasma Anodization", *1983 VLSI Technology Symposium*, Maui, Sept 1983.

[17] C. Ramiller, "Boro-Phospho-Silicate Glasses for Low-Temperature Reflow", *Proceedings, Semicon West , May 1982 , pp29-37.*

[18] N.W. Cheung, M-A. Nicolet,M. Wittmer, C.A.Evans, and T.T. Sheng, " Growth Kinetics of Pd_2S from Evaporated and Sputter-Deposited Films," *Thin Solid Films, Vol. 79*, pp.51-60, 1981.

[19] S.S. Lau and N.W. Cheung, "Epitaxial Growth of the Nickel Disilicide Phase", *Thin Solid Films, Vol. 71*, pp.117-127, 1980.

[20] N.W. Cheung,P.J. Grunthaner, F.J. Grunthaner,J.W. Mayer, and B.M. Ullrich, "Metal-Semiconductor Interfacial Reactions: Ni/Si System", *J. Vac. Technol.,Vol. 18*, pp.917-923, 1981. [21] W.K. Chu,J.W.Mayer and M-A. Nicolet, *Backscattering Spectrometry, Academic Press, New York (1978).*

[22] H.H. Berger, "Models For Contacts to Planar Devices," *Solid State Electronics, Vol.23*, pp.145-158,1972.

[23] J. Hui, T. Y. Chiu, S. Wong, and W. G. Oldham, "Sealed-Interface Local Oxidation Technology", *IEEE Trans. Elec. Dev. ED-29*, pp554-560, 1982.

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: SSM-84-2 **Last Year's No.(s):** SSM-83-2 (in part)

Title: Studies of MBE Growth Kinetics and High-Energy Ion Implantation in Compound Semiconductors

Senior Principal Investigator(s): N. W. Cheung (415) 642-1615
S. Wang 642-4134

I Scientific Objective

Propagation delays and parasitic capacitive effects may ultimately limit the processing speed of very-high-speed integrated circuits (VHSIC) because of the ever-increasing line lengths and junction capacitance for isolation between on-chip devices. The advent of the MBE and MO-CVD growth technologies and the availability of semi-insulating (SI) GaAs and InP substrates make it attractive to consider the feasibility of three-dimensional packaging of compound-semiconductor devices. The objectives of the proposed research are to investigate the MBE growth process and the high-energy ion implantation for fabricating multiple layers of GaAs-based devices.

One basic component in a multi-layer device architecture is the electrical isolation between adjacent layers of device structures. A great deal of efforts have been reported in the literature to obtain semi-insulating bulk crystals with low etch pit density (EPD), and much work remains to be done to improve the crystal quality suitable for uae in large scale integration. We propose that MBE-grown GaAs films with Cr and isoelectronic doping be studied for their semi-insulating property and defect density.

To complement the MBE technique for fabricating three-dimensional device structures, we will explore the use of high energy implantation (MeV energy range) to modify the electrical properties of semiconductors.With conventional implantation energies (100 keV range), dopants can only penetrate a depth of approximately 1000 *angstrom* for III-V semiconductors.With the ions in the MeV energy range, the ions can penetrate microns deep into the semiconductor with a relatively low dopant concentration at the surface region(i.e., the formation of buried layers). We also believe that the higher electronic stopping component of the energy deposition mechanism will create less physical defects at the surface region because ion-lattice collisions will be significantly reduced. In this way, not only conventional device structures benefit, but three dimensional usage of the semiconductor will also be possible.

II State-of-the-Art

The recent advances in high-speed electronic and optoelectronic compound-semiconductor devices have provided fresh impetus to improving the quality of GaAs and InP bulk crystals. Although much progress has been made, much work remains to be done to control the doping concentration and to reduce the defect density in the bulk crystals so that the material is suitable for use as the substrate for large-scale device integration. In undoped SI ($P \approx 10^8 \Omega cm$) LEC-grown GaAs crystals, an etch-pit density (EPD) of $10^4/cm^2$ has been reported[1]. In (Cr,0)-doped SI ($P \approx 10^8 \Omega cm$) HB-grown GaAs crystals, an average EPD as low as $365/cm^2$ has been achieved. There is some definite correlation between EPD and doping concentration. Although LEC growth of dislocation-free InP crystals has been reported[3], the crystals are highly compensated.

The relatively poor quality of GaAs and InP substrates has not impeded the remarkable progress achieved in electronic and optoelectronic devices. The success in large part can be attributed to the high quality of MBE frown and MO-CVD grown films. Commercially available GaAs and InP substrates generally have a EPD in the range $10^3 - 10^4/cm^2$. Yet, ultra-high-speed electronic devices, such as the HEMT[4] and the direct-coupled GaAs MESFET[5], and extremely low-threshold lasers, such as the GRIN-SCH laser[6], have been realized. Undoubtedly, the defect density in MBE or Mo-CVD grown films is much reduced with respect to that in the substrate. However, a systematic study of the defect density in MBE grown films is lacking in terms of doping

concentration and degree of compensation. This is especially true for SI films.

High energy implantation has made possible some novel and perhaps important device structures. Doken et al. [7] have developed a bipolar process utilizing high energy As and B ions to implant p-Si substrates through thin oxide and LOCOS field oxide layers to form buried n^+ layer and channel stopping p^+ layer. Combs [8] has investigated a scaleable retrograde p-well CMOS technology by using a single high-energy boron implant to produce a self-aligned channel stop and an extremely shallow, low sheet resistance p-well. A Si power FET using multichannel p-type buried gates (the "Gridistor") has also been realized by Lecrosnier and Pelous [9]. These structures have been fabricated using beams with energies between 1 and 5 MeV. In our work the energy has been extended to 11 MeV. By increasing the energy range, we have extended the usable depth for three-dimensional device design and have minimized the nuclear damage at the surface regions of the semiconductor.

A survey of the literature shows that material characterization of MeV ion implantation effects in semiconductors have not be studied in detail. Maby [10] has investigated the distribution of B (up to 3 MeV) and defect states in Si. High-energy (1.2 MeV) implantation of Si into GaAs has been reported by Liu et al. [11], with good mobility and controllable profile.

III Progress and Publications

The Riber 1000 MBE growth system is now in full operation. A scanning Anger analyzer with depth profiling capability (purchased through JSEP funding) was installed in the analysis chamber and a quadrupole mass spectrometer (purchased through NSF funding) was installed in the growth chamber. The new mass spectrometer helped us to detect a tiny leak in the cryo-shroud which was re-welded. With a background pressure in the 1.5 x 10^{-10} range without LN cooling and in the 8 x 10^{-11} range with LN cooling, we have been ale to grow GaAs and (GaAl)As films of consistently high quality, showing excellent surface morphology and photoluminescent spectrum. Growth rate and doping concentration at different substrate and oven temperatures have also been calibrated.

At the same time, we have built our capabilities in material characterization. Through JSEP funding, apparatus for the DLTS and PL experiments have been purchased and tested. Computer programs have been set up to obtain doping profile from the measured C-V plot. Photoluminescence experiment has been performed at 77 eK with the MBE-grown GaAs and (GaAl)As films. The PL spectrum is much narrower (by a factor of about 10) from the MBE film than from the substrate. The measured mobility in both p and n layers is also consistent with the amount of doping in the layers.

We have completed several experiments of high energy implantations into Si. Silicon was chosen in these preliminary studies because it is an elemental semiconductor. Three-dimensional usage of the buried implanted layer in device structures has been demonstrated.

A) Implantation Range and Damage Profile

Arsenic has been implanted into p-type silicon at 11 MeV to form buried layers. These buried layers can be defined laterally using a sputtered tungsten mask that is 2 microns thick. The tungsten is patterned using a fluorine based plasma. The range (R_p) of 11 MeV arsenic is 4.4 microns with a straggle (ΔR_p) of .37 microns. For a dose of 1.9 x 10^{15} atoms/cm^2 at a beam current of 1.2 μ

amps the upper two microns of the silicon remains dislocation free after furnace annealing. Our cross-sectional TEM studies showed that substrate temperature during implantation affects the crystalline quality of the implanted layer significantly. Spreading resistance measurements gave a sheet resistance value of 50 ohm/square for the buried layer.

B) Masking

There are two main considerations for masking ion implantation in the megavolt regime. The first is the masking technology, and the second is the divergence of the beam in penetrating the substrate. The later will set a lower limit on the lateral definition of minimum device features. For conventional low energy ion implantation, silicon dioxide or high temperature resists are used to mask off the areas that are not to be implanted. For high energy implantation, the low atomic masses of silicon dioxide or resist will require an excessively thick masking layer. Instead, a heavy element that can be readily deposited and patterned offers a solution to this problem. Workers in the past have used gold. However, tungsten has advantages over gold in many respects. Gold which has poorer adhesion to silicon dioxide than tungsten requires an intermediate layer such as chromium while tungsten can be directly deposited onto silicon dioxide. A fluorine based plasma can define patterns in tungsten anisotropically. After implantation, the mask is readily removed in a heated solution of formic acid and hydrogen peroxide. Experimently, we have determined that for an 11 MeV arsenic beam with a particle current of 1 μ amp ,a gold mask will buckle while a tungsten mask remains intact.

C) Buried Interconnect

Using 11 MeV arsenic implantation ,buried interconnects have been fabricated in p-type silicon. Because the conducting medium is crystalline, the interconnect can have a lower resistivity than a polycrystalline interconnect with the same dopant density. For complex IC circuits this type of interconnection offers an independent layer of interconnection. The 11 MeV arsenic implant shows a pronounced dopant distribution tail toward the surface. Further work should be done with respect to the annealing conditions to minimize this tail.

D) Bipolar Transistor

To demonstrate the feasibility of making multi-layered device structures, a vertical npn bipolar transistor has been fabricated using 11 MeV arsenic implantation. A Beta value of 40 has been obtained without leakage between the emitter and the collector. Contact to the buried layer was obtained through a deep phosphorus diffusion that was performed before the high energy implant. A more sophisticated process would use a multi-energy implant to make contact to the buried collector. This type of processing could produce a very compact and easily fabricated self-isolating bipolar transistor.

E) MOS Structures

Recently there has been interest in fabricating both NMOS and CMOS in high resistivity epitaxial material grown on a highly doped substrate. Such structures offer enhanced breakdown characteristics and latchup protection. A high energy boron implant into a high resistivity substrate can produce the

same geometry without using epitaxial silicon. This nonepitaxy process offers advantages in simplicity and perhaps yield. High energy boron (4 MeV) has been implanted into lightly doped p-type silicon substrates. The boron has a range of 5.2 microns with a .2 micron straggle. NMOS transistors have been fabricated above this layer, and these transistors show good characteristics. The result indicates that the surface layer after implantation is of device quality.

Publications

[] P.F. Byrne, N.W. Cheung, and D.K. Sadana, "Damage Induced Through Megavolt Arsenic Implantation into Si," *Appl. Phys. Lett., Vol. 41*, pp. 537-539, 1982.

[] P.F. Byrne, N.W. Cheung, and D.K. Sadana, "Megavolt Arsenic Implantation into Silicon," *Thin Solid Films, Vol. 95*, pp.363-367,1982.

[] J.Washburn,C.S.Murty,D.Sadana,P.Byrne,R.Gronsky,N.W.Cheung and R.Kilaas, "The Crystalline To Amorphous Transformation in Si," *To be published in Proceedings of the Third International Conference* on Ion Beam Modification of Materials (Sept.1982).

[] P.F. Byrne, "High Energy Ion Implantation Effects in Si," *J. Appl. Phys., Vol.54*, pp.1146-1147, 1983.

[] P.F. Byrne, N.W. Cheung, D.K. Sadana, and D.L. Polla, "Electrical Characteristics of Silicon Implanted with 11 MeV Arsenic," *To be published in the Proceedings of Electrochemical Society Meeting* (San Francisco, CA, May 1983).

[] D.K. Sadana, J. Washburn, P.F. Byrne, and N.W. Cheung, "Damage and In Situ Annealing During Ion Implantation," *Defects in Semiconductors, Vol.4, (in press)*, (Proceedings of Materials Research Society Symposium, Boston,MA, Nov 1982).

[] P.F. Byrne and N.W. Cheung, "Megavolt Boron and Arsenic Implantation into Si," *paper accepted for Material Research Society Meeting (Boston, MA*, Nov 1983).

[] P.F. Byrne, N.W. Cheung, and D.K. Sadana, "Buried Layer Formation Through Megavolt Arsenic Implantation," *paper submitted to IEDM, 1983.*

Significant Accomplishments

Our material studies have shown that, using 11 MeV arsenic and 4 MeV boron implantation into Si, buried dopant layers can be fabricated with high electrical conductivity. Ion-beam induced annealing has been proven to be beneficial to the regrowth of amorphous Si.The damage profile due to implantation amorphization can be understood from the computer calculations of energy deposition profile. The top 2 microns of the surface Si has a lifetime of approximately 2 to 3 microseconds, a value comparable with that of the unimplanted wafer.

Bipolar and NMOS transistors have been fabricated with the high-energy implants. Device performance of both types indicates the surface layer after implantation is of device quality. The device structures imply that three dimensional usage of the semiconductor is possible with this high-energy implantation technique.

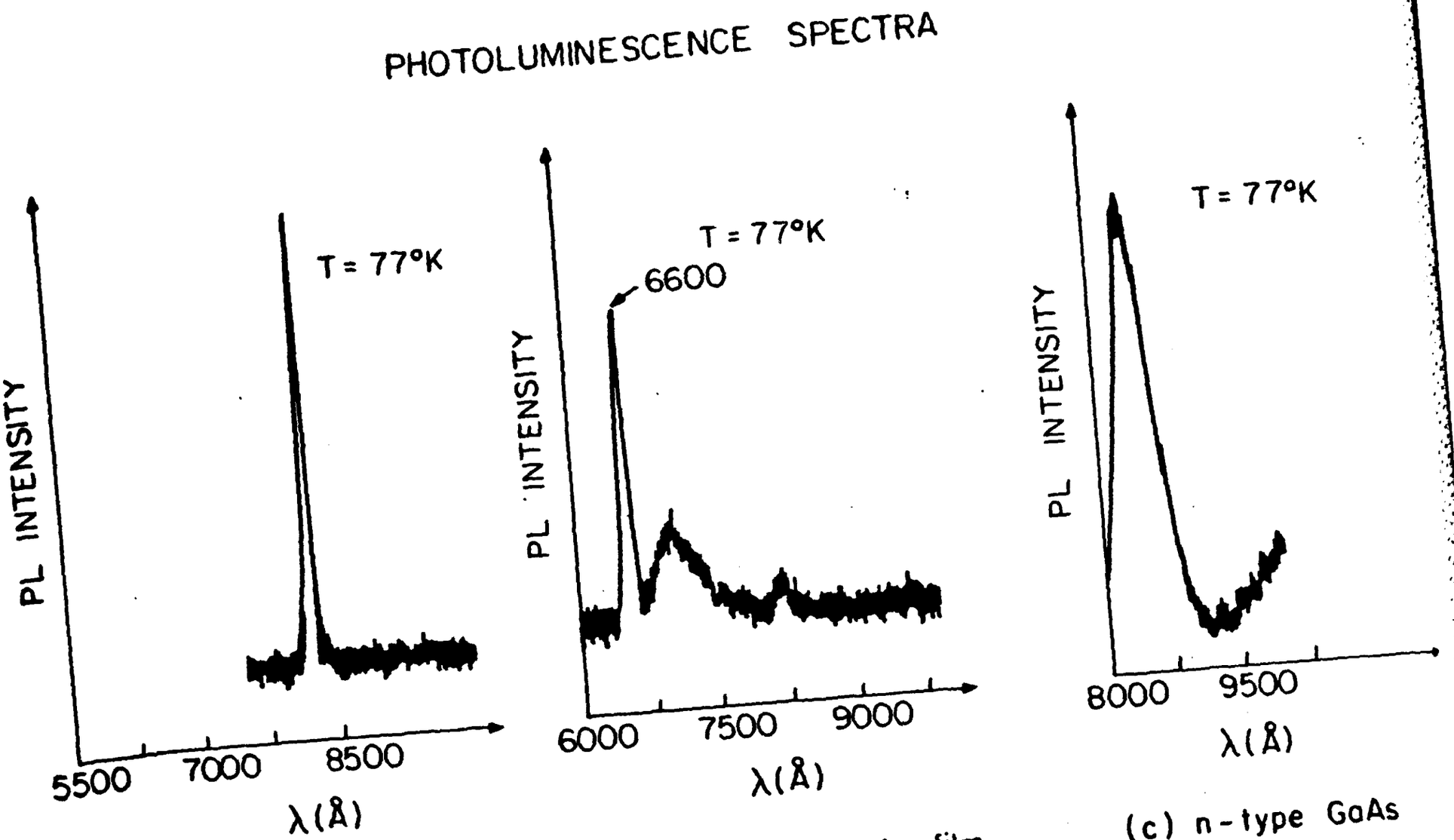


Fig. 1. Photoluminescence Spectra

IV The Proposed Research

With the MBE system in full operation, we are in a position to explore the potential use of the MBE process for device applications. We propose to study the growth kinetics and resistivity in Cr-doped MBE-grown GaAs and (GaAl)As films. The aim is to grow semi-insulating films for electrical isolation. Two recent developments are worth noting. First, doping of GaAs and InP bulk crystals with isoelectronic species seems to be effective in reducing or even suppressing dislocations and microprecipitates[12]. Second, x-ray diffraction study of GaAs/AlAs superlattice grown on (001) planes shows satellite reflections, indicating a terraced surface and interface structure[13]. Because of the accurate control of film thickness and composition, MBE grown films can be used as a sensitive tool to study the growth kinetics of the MBE process.

Using TEM, x-ray diffraction, PL, DLTS, and Hall measurements, the dependence of defect structure and electrical activation will be investigated as a function of Cr, donor, and isoelectronic doping concentrations. As mentioned earlier, dislocation-free bulk InP crystals have been grown along the <111> direction. It is well known that LPE growth kinetics varies with the crystal plane. Therefore, the study will be carried out with MBE films grown on different crystal planes.

With our initial success of using high energy implantation to process Si devices, we propose to extend its application to the study of III-V semiconductors. We envision the high energy implantation technique will create novel approaches to fabricate three-dimensional device structures.Implantation to form buried doped regions (e.g. Si, Se and Zn) and buried insulating regions(e.g. H and O) will be attempted.

Using cross-sectional TEM ,SIMS and Hall Effect measurements, the dependence of defect structures and electrical activity on the implantation conditions and annealing conditions will be investigated. Computer calculations of the energy deposition profile will be performed. Our goal is to acquire a basic understanding of the implantation damage mechanisms of III-V semiconductors in the MeV energy regime.

Implantation through superlattice structures grown by MBE will also be studied. Interface electrical properties of ion-beam mixing effects will provide more insight in structural imperfections of superlattices.

References

(1) T. Fukuda and T. Iizuka, "LEC GaAs Crystal Growth for Optoelectronic Integrated Circuits," paper PC1, Technical Digest, Post IOOC Conference Meeting, Kobe, Japan, July 2 (1983).

(2) S. Akai, K. Fujita, and N. Kito, "HB GaAs Crystal Growth for Integrated Optics," paper PC2, Technical Digest, Post IOOC Conference Meeting, Kobe, Japan, July 2 (1983).

(3) S. Shinoyama, "InP Crystal Growth for Integrated Optics," paper PC3, Technical Digest, Poast IOOC Conference Meeting, Kobe, Japan, July 2 (1983).

(4) M. Abe, T. Mimura, N. Yokoyama, and H. Ishikawa, "New Technology Towards GaAs LSI/VLSI for Computer Applications," *IEEE Trans. Electron. Dev.*, Vol. ED-29, p. 1088 (1982).

(5) R. A. Kiehl, P. G. Flahive, S. H. Wemple, and H. M. Cox, "Direct-Coupled GaAs Ring Oscillators with Self-Aligned Gates," *Electron. Dev. Lett.*, Vol. EDL-3, p.

35 (1982).

(6) W. T. Tsang, "Extremely Low Threshold (AlGa)As Graded-Index Waveguide Separate-Confinement Heterostructure Lasers Grown by Molecular Beam Epitaxy," *Appl. Phys. Lett.*, Vol. 40, p. 217 (1982).

(7) M. Doken, T. Unagami, K. Sakuma, and K. Kagiyama, "Novel Bipolar Process Utilizing MeV Energy Ion Implantation," *IEDM*, pp.586-589, 1981.

(8) S.R. Combs, "Scaleable Retrograde P-well CMOS Technology," *IEDM*, pp. 346-349, 1981.

(9) D.P. Lecrosnier and G.P. Pelous, "Ion-Implanted FET for Power Applications," *IEEE Tran. Electron Devices, Vol. ED-21*, pp.113-118,1974.

(10) E.W. Maby, " MeV Ion Implanted Boron Layers in Silicon," *Ph.D. Thesis, Massachusetts Institute of Technology*, 1979.

(11) S.G. Liu,E.C. Douglas, C.w. Magee, F. Kolondra, and S. Jain, "High-energy Implantation of Silicon into GaAs," *Appl. Phys. Lett., Vol. 37*, pp.79-81, 1980.

(12) G. Jacob, J. P. Farges, C. Shemalt, M. Duseaux, J. Hallais, W. J. Bartels, and P. J. Roksnoer, "Effects of Isoelectronic Species on Dislocations and Microprecipitates," *J. Cryst. Growth*, Vol. 57, p. 245 (1982).

(13) D. A. Neumann, H. Zabel, and H. Morkoc, "X-Ray Evidence for a Terraced GaAs/AlAs Superlattice," *Appl. Phys. Lett.*, Vol. 43, p. 59 (1983).

University of California, Berkeley — Electronics Research Laboratory

Joint Services Electronics Program — August 15, 1983

III. B. Basic Research in Solid State Electronics - Devices — Coordinator: Professor T. Van Duzer

General

Since 1960 solid-state device research and integrated circuit research have been carried out in a common facility in the Electronics Research Laboratory. We have long maintained and observed the obvious benefit; everyone enjoys a more complete, flexible experimental capability. Further, as a consequence of sharing experimental facilities, there has been a beneficial contact between research in apparently quite different fields. One result is a significant transfer of technique, accelerating progress in experimental technology for all concerned. More subtle results are the development of larger research goals in common.

The work in solid-state electronics has received new impetus with the construction of a major new microelectronics clean facility in the Electronics Research Laboratory. In addition to having high-grade clean areas, much new equipment has been added. For example, we have a new state-of-the-art mask fabricator which couples with our in-house CAD facilities to give the capability of rapid turn-around in research experimentation on devices and circuits. Well-controlled furnaces for silicon processing, a system for reactive etching, a scanning electron microscope that will allow inspections with extreme precision of wafer-size samples, a molecular-beam epitaxy system for gallium arsenide and other related materials, and an electron-beam lithography system capable of 0.1 μm fabrication and alignment, which has also been adapted to our CAD circuit layout system, as well as other supportive equipment, are parts of the new facilities available for solid-state device studies.

The proposals contained herein are all advanced device basic studies which use the common laboratory facilities in the experimental phase. They have in common the state-of-the-art techniques required for successful fabrication. The research proposals also have in common certain intermediate and long-term goals. In general the intermediate goals are the basic study and development of simple devices and processes which will point the way toward the long-term goal of more powerful, cheaper, denser circuits.

Processing studies have the broadest applicability of the various projects in the solid-state device area. The emphasis here is on photo- and electron-beam lithography with studies of the resists and exposure strategies. Earlier work in this laboratory has led to accurate modeling of certain resists and this will now be applied to a wider variety of resists and a broader range of processing parameters. Studies of alignment accuracy and proximity corrections for electron-beam lithography systems will continue. Of primary concern are the effects of resist thickness and development characteristics.

The availability of the LEBES electron-beam lithography system will make possible a study of the miniaturization of superconductive devices and circuits. Of particular importance is a study of the factors limiting miniaturization and speed of operation. Work will be directed first to several families of Josephson logic circuits to predict theoretically scaling possibilities and to confirm the calculations by fabricating the circuits and making high-speed tests. We have

studied one such family theoretically to date, with the result that a factor of three increase in speed and a factor of ten in circuit density appear possible by miniaturization.

Mixers for millimeter wave and higher frequencies continue to be subjects of importance. Basic understanding of the factors limiting conversion efficiency and noise minimization are developing. Superconductive devices with energy gaps on the order of a few millivolts have been shown to have promise as the most sensitive mixers for frequencies that should extend to about 600 GHz. Beyond that, nonlinearities based on other phenomena are needed and the metal-barrier-metal (MBM) tunnel junction appears to be a good candidate. We have made superconductive devices that employ contacts of metals on crystalline silicon; these have the potential of being efficient, rugged mixers that can operate at 10 K. Fundamental studies on the metal-semiconductor contact need to be continued and we propose mixer evaluation at 90 GHz. The same system will be used to study MBM devices at room temperature; the testing can be done at 90 GHz and the results applied to estimate the behavior at higher frequencies. Basic questions on losses in the junctions and factors affecting roll-off must be answered.

A potentially important process for forming piezoelectric films on silicon substrates to make them a part of integrated circuits is proposed. The films would be piezoelectric because of being formed in the presence of an electric field. Plasma-enhanced chemical vapor deposition and solution polymerization techniques will be used. It is believed that this approach will widen the number of piezoelectric polymers known. This project brings together the efforts of faculty in electrical and chemical engineering.

It is proposed to study techniques for analog signal processing with the maximum possible dynamic range. The project will encompass noise characterization, system design, new circuit topologies, and technology research. The high end of the dynamic range is limited by internally generated distortion mechanisms and the low end by noise. Work on this project has already identified the factors of importance at the high end and the continuing effort will be directed toward characterization and minimization of these effects. Studies in this project have led to predictions of the noise limitations in switched-capacitor filters, which have become of considerable importance in high-frequency communication applications.

Future scaling down the size of devices for VLSI applications will depend on the availability of understanding of high-field transport phenomena. This proposal has the objective of clarifying the physics of such effects. The effect of hot-electrons on the terminal characteristics will be related to studies of the physical phenomena, both of the generation and influence of hot electrons. The uniformity of field in the gate region of short-channel devices will be studied by measuring the light emission from that region as was recently demonstrated here. New approaches to minimization of hot electron effects and improvement of breakdown voltages in high-voltage devices will be explored.

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: SSD-84-1 **Last Year's No.(s):** SSD-83-1

Title: Problems in E-Beam and Optical Lithography

Senior Principal Investigator(s): A. R. Neureuther (415) 642-4590
W. G. Oldham 642-2318

Scientific Objective

This research is concerned with those critical properties of photo- and e-beam sensitive materials and the strategies for exposure and development which can significantly improve lithographic performance. Through careful resist characterization we have identified the key parameters of a number of positive photoresists. The understanding thus gained has led not only to accurate models for resist development, but also to more optimum methods of processing to extract the maximum performance. We propose to follow this very promising lead and study both a greater number of resists and their behavior over a wider range of processing parameters (including, for example, the use of positive resist in a negative operating mode). Our state-of-the-art in-situ resist development system will be further advanced to provide more detailed information on resist development mechanisms.

In electron beam lithography both simulation and experimental studies will be pursued. In such studies in the past we have identified optimal alignment and writing strategies, both for maximization of alignment accuracy, and for minimization of writing time. We will pursue this approach by means of simulation of electron scattering and resist line edge profile development. A number of new e-beam machines are appearing, with a variety of addressing and beam shaping approaches. One goal of this research is to assess how the particular characteristics of the various new equipment, especially the VHSIC machines, can be best utilized in proximity correction techniques. The primary concerns are how resist thickness and development characteristics will impact compensation techniques. Electron beam lithography will be used in the laboratory as a tool for exploring device problems. In linear IC circuits it will be used to assess lithography issues in obtaining matching device characteristics.

State of the Art

The processes and first order mechanisms of both e-beam and optical lithography are now reasonably well understood, and it is possible to accurately simulate a variety of processes(1-4). The simulator SAMPLE (1) is used widely for such purposes. Future advances in optical lithography will extend useful resolution to below 0.5um, largely based on improvements in resist technology and processing. Optical performance of both refracting and reflective systems is close to the diffraction limit, and slowly increasing with time(5). Resist performance, on the other hand, is less ideal and has greater potential for extending effective system performance. Both new approaches with existing materials (such as multi-layer resists (6), portable conformable masks (7), and contrast enhancement layers (8)), and new resist systems (such as the Ge-Se inorganic system (9), and the complex single-layer resists like MRS (10)) have been demonstrated to extend the useful range of existing tools into the submicron regime. It is important to be able to model these new processes and systems, and to be able to accurately simulate the complete process if lithographic performance is to be optimized. However there are a dearth of both models and model parameters. In fact our group at Berkeley, under JSEP support, is virtually the only group in the world presently producing new model data for resist systems(11-13). Our state-of-the-art resist characterization capability consists of an exposure bleaching apparatus and an in situ development thickness monitor based on interferometry (12). With these systems we have been able to accurately study the effects of process conditions such as bake temperature, developer type and concentration, and special treatments on lithographic performance(12,13). A new development model for positive resist has also resulted (12). Currently the system is being used to establish a model for KODAK 820

which has a beneficial surface induction effect(13).

There are very clear opportunities for using our resist measurement system and modeling approach to understand the new resist materials, determine fruitful directions for obtaining improved performance, and quantitatively predict the benefits/drawbacks of processing approaches. New models are needed for the advanced materials which use a minimal set of parameters to describe the physical mechanisms. In order to be able to accurately characterize the newer materials, some improvements in our characterization system are needed. In particular, the cell design can be improved for better signal-to-noise performance, and to allow measurements both from front and rear surfaces.

The development of new electron beam lithography hardware under the VHSIC project has raised many questions about writing strategies and proximity corrections. Under JSEP sponsorship we have developed the ability to evaluate alignment and exposure strategy (14-17), and have made available a widely used simulator for e-beam exposure and development(18-20). Many studies are available in the literature on e-beam strategy; however, several of the new machines have special characteristics whose virtues and vices need to be explored. One such characteristic is the paint brush approach where the width of the brush can be dynamically altered but at fixed dose. Another consideration is the potential impact of new lithography materials on the writing strategies of these machines. SAMPLE is well suited for generating the kinds of information needed to understand tradeoffs in the hardware and software. New approximate algebraic exposure models are needed to deal directly with the two dimensional pattern proximity effects. Such models necessarily depend on Monte Carlo studies for their "raw data", thus our Monte Carlo energy deposition program should continue to be developed.

Electron beam lithography is a very useful tool for achieving high resolution and high overlay accuracy. As such it is very useful in the exploration of device physics for high performance devices. In linear IC circuits it can be used to systematically explore the lithography contribution in matching device characteristics. This can be carried out with the aid of on chip measurement electronics.

Proposed Research Program

Engineering Models for Advanced Lithography Materials

The further development and application of our resist characterization system will be pursued along three major directions.

1) Modeling of Positive Photoresist and Extraction of Model Parameters

The present activity focussing on the understanding of positive photo resist will be continued. A new resist model was proposed and data were presented for a few typical photoresists in 1982 (12). The validity of the model needs to be further explored by examing both new resists and new developers. Recently we determined that the Kodak 820 resist shows a very persistent and reproducible surface development rate reduction. We have tentatively modified the model to account for the surface rate effect (13), but a great deal of data need to be taken over a wide range of process conditions to provide verification, yield model parameters, and suggest directions for better models. Furthermore, the dependence of the induction effect on process conditions must be well understood to be able to take full advantage of this potentially helpful effect.

As new developers, especially metal-ion-free solutions, become available, they will be characterized to both extract model parameters and discover unexpected behavior or sensitivities. The new "hot plate" bake technique for resist curing must be more thoroughly characterized. We expect, but have not yet been able to verify, a modified residual solvent distribution leading to a change in the depth dependence of surface inhibition. Very recently we have discovered an unusual sensitivity of development to post-cure solvent vapor exposure. This effect will be characterized and evaluated as a potential new "trick" in the processing arsenal.

2) Exploration of New Materials and Process Techniques

The exposure and development of new optical, e-beam, (and eventually x-ray and ion-beam) resists will characterized and modeled. The modification of resist properties with special thermal and chemical treatments will be studied. In particular, the modification of positive photoresist to cause it to operate in a negative mode (similar to the e-beam development reversal technique (21)) will be explored, and models generated to describe the behavior quantitatively. The new surface-controlled negative resists will be studied and modeled as alternatives.

New approaches for the measurement of development will be explored. Such resists as Ge-Se inorganic films require entirely different approaches, both because they are opaque in the visible, and because they are so thin. Furthermore they utilize a built-in anisotropy, which makes present isotropic models inappropriate. Thus to date we have been able to accurately model only the exposure of such systems (22).

Similarly, the development of e-beam resists will be characterized as needed to support the e-beam strategy activity. The behavior of special developers which minimize the effects of backscattered electrons, and possible treatments to control resist profiles can be determined. It is also our intention to develop appropriate apparatus and extend our characterization and modeling program as resists for x-ray and ion-beam lithography become available.

3) System and Data Reduction Improvements

The resist characterization system can be improved to allow more rapid and accurate characterization, as well as new modes of development. The photo-bleaching system requires minor modifications to increase the absolute precision and reproducibility of resist exposure (from about +/- 25% to +/- 5%). The development system needs both minor improvements, eg in the interferometer beam to reduce the spot size, and a more major modification of the basic development cell. By reducing the spot size, the susceptibility to errors from spin nonuniformities will be greatly reduced. Another development cell, in which the interferometer beam passes through the development fluid will allow development characterization on a wider variety of substrates. The effects of standing waves interacting with surface rate inhibition effects, for example, can be examined. The use of very high drying rates at elevated temperatures can be characterized with higher conductivity (opaque) substrates. Furthermore, standard 100mm Si substrates will be possible, allowing collaborative studies with industrial colleagues.

The data reduction and parameter extraction algorithms also require further development. A more automated procedure will be developed in which the development rate data are fit to the various models, and the model behavior is compared directly to the measured thickness versus time. At present, a good deal of intelligent intervention is required, and the extraction algorithms are not uniformly robust.

Electron beam lithography

Both simulation and experimental studies are proposed.

1) Simulation

The models in SAMPLE will be extended for studying proximity effects from two dimensional patterns. An approximate algebraic approach will be used to avoid the time consuming 3-d Monte Carlo simulation. This will be used in the study of intra-line proximity effects such as line end tapering to compensate for line end rounding. Inter-line proximity effects such as line tapering when nearing other features will also be explored. The important issues are to determine the best basis (incident or absorbed dose at which height) for making the proximity correction and the appropriate dose discretization level for an adjustable width beam.

2) Experimental Device Fabrication

In a collaborative effort with the IC design group, the LEBES system will be used to write certain critical levels of linear and digital prototype devices in the Berkeley Advanced CMOS process. The goal is to assess the sensitivity of high performance linear and digital devices to critical dimension variation and alignment accuracy. The possible improvement of device characteristics matching with electron beam lithography will be explored. The possibility of using special parameter-tolerant on-chip circuits for the measurement of matched device tolerances will be explored. The layout of these devices will be automated by means of the KIC system.

References

(1) W. G. Oldham, S. N. Nandgaonkar, A. R. Neureuther, and M. M. O'Toole, "A General Simulator for VLSI Lithography and Etching Processes: Part I - Application to Projection Lithography," *IEEE Trans. on Electron Devices*, Vol. ED-26, No. 4, pp. 717-722 April 1979.

(2) W. G. Oldham, A. R. Neureuther, C. Sung, J. L. Reynolds and S. N. Nandgaonkar, "A General Simulator for VLSI Lithography and Etching Processes: PartII-Application to Deposition and Etching," *IEEE Trans. on Electron Devices*, Vol. ED-27, No. 8, pp. 1455-1459, August 1980.

(3) A.R. Neureuther, "IC Process Modeling and Topography Design," *IEEE Proceedings*, Special Issue on VLSI Design: Problems and Tools, Vol. 71, No. 1, pp. 121-128, January, 1983.

(4) W. Leung, A.R. Neureuther and W.G. Oldham, "Edge Sharpening, Contrast Enhancement, and Feature Dependent Amplification in Inorganic Resist - A Simulation Study," *SPIE Vol. 394*, Optical Microlithography II, March 1983.

(5) M. G. Rosenfield, A. R. Neureuther and C. H. Ting, "The Use of Bias in Electron-Beam Lithography for Improved Linewidth Control," *J. Vac. Sci. and Technol.*, Vol. 19, No. 4, pp. 1242-1247, Nov/Dec 1981.

(6) M. G. Rosenfield and A. R. Neureuther, "Exploration of Electron-Beam Writing Strategies and Resist Development Effects," *IEEE Trans. on Electron Devices*, Vol.ED-28, No.11, pp 1289-1294, (November),1981.

(7) M. G. Rosenfield, "Simulation of Developed Resist Profiles for Electron Beam Lithography," MS Thesis, University of California, Berkeley, June 1981

(8) D.K. Kim, W.G. Oldham, and A.R. Neureuther, "Characterization of Resist Development: Models, Equipment and Experimental Results," Kodak Microelectronics Seminar, San Diego, CA., Oct. 20-21, 1982.

(9) D. K. Kim, W. G. Oldham, and A. R. Neureuther, "Characterization and Modeling of a Resist with Built-in Induction Effect", Kodak Microelectronics Seminar, San Diego, Ca., Oct 1983.

(10) M. Exterkamp, W. Wong, H. Damar, A.R. Neureuther and W.G. Oldham, "Resist Characterization: Procedures, Parameters, and Profiles," *SPIE Vol. 334*, Optical Microlithography, pp. 182-187, 1982.

(11) Y. C. Lin, I. Adesida, and A. R. Neureuther, "Monte Carlo Simulation of Registration Signals for Electron Beam Microfabrication," *Appl. Phys. Lett.*, Vol. 36. No. 8, pp. 672-674, 15 April 1980.

(12) Y. C. Lin, A. R. Neureuther, and I. Adesida, "Alignment Signals from Si Tapered Steps for Electron Beam Lithography," *J. A. Phys.*, Vol. 53, No. 2, pp. 899-911, February 1982.

(13) Y. C. Lin and A. R. Neureuther, "Alignment Signals from Resist-Coated Marks for Direct Wafer Writing," *IEEE Trans. on Electron Devices*, Vol.ED-28, No.11, pp 1397-1405, (November),1981.

(14) Y. C. Lin, A. R. Neureuther and W. G. Oldham, "Alignment Signals from Symmetrical Silicon Marks for Electron Beam Lithography," *Kodak Microelectronics Seminar, Interface 1981*, October 15-16, 1981, Dallas Texas.

(15) Y. C. Lin, "Alignment Signals from Electron Scattering Near an Edge for Electron Beam Microfabrication," PhD. Thesis, University of California, Berkeley, March 1981.

(16) W.G. Oldham, P. Jain, A.R. Neureuther, C. Ting and H. Binder, "Contrast in High-Performance Projection Optics," *Proceedings, Kodak Microelectronics Seminar, Interface 81*, Dallas, pp 75-80, October 1981 .

(17) W.G. Oldham and E. Hieke, "A High Resolution Negative Electron Resist by Image Reversal," *IEEE Electron Device Letters*, Vol. EDL-1, No. 10, pp. 217-219, October 1980

(18) P. Poenisch, "An Automatic Dual-Beam Resist Bleaching System and Exploration of Prebake Solvent Content Effects", MS. Dec 1981.

(19) M. Exterkamp, "A System to Characterize Positive Photoresist Development", M. S. June 1982.

(20) W. Wong, "Positive Photoresist Exposure Characterization", M. S. June 1983.

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: SSD-84-2 **Last Year's No.(s):** SSD-83-2

Title: Study of the Effects Limiting Realization of Far-Submicron Superconductive Electronic Structures

Senior Principal Investigator(s): T. Van Duzer **(415)** 642-3306

Scientific Objective

The objective of this work is to investigate the fundamental factors that limit the speed and miniaturization of superconductive devices and circuits.

State of the Art

There is currently interest in two areas that appear destined to overlap as they come to fruition. Electron-beam lithography has made possible the fabrication of devices and circuits having feature sizes on the order of 0.1 μm and smaller. A parallel development is the demonstration of the potential of superconductive devices for performance important to future systems. Improved device performance is often obtained by miniaturization; the extent to which this approach can be applied and the goals that can be achieved need study. There are characteristic lengths, the "penetration depth" and the "coherence length" which may set limits. The former is the 1/e distance of decrease of magnetic flux density into a superconductor. The latter is roughly the size of a Cooper pair which, in thin films, is largely dominated by the mean free path of the electrons. Other basic limitations include the maximum current in a thin-film line, the maximum current density in a Josephson junction, and the superconductor gap voltage. At the circuit level the flux quantum plays an important role. Superconductor loops that appear in the interferometers used in logic and memory circuits must have inductance that is some fraction of the ratio of the flux quantum (2.07×10^{-15} Wb) to the critical current of a Josephson junction in the loop. This sets a minimum on the inductance and, therefore, on the size of loop that can be used. We will examine possible ways to circumvent the limitation, such as using very thin films so that the inertia of the momentum-locked electron-pair fluid makes a significant contribution to the effective inductance.

No systematic studies of miniaturization have yet appeared in the literature. There have been scattered examples of fabrication of very small tunnel junctions and other Josephson devices with far-submicron features. Also, there have been occasional brief speculations about how the speed of Josephson logic circuits will scale with feature size.

Progress and Publications Since Last Major Proposal

Work has proceeded on both experimental and theoretical fronts. The experimental work includes both facilities development and device fabrication. An electron-beam lithography system (Perkin Elmer ETEC LEBES system) has been purchased and the acceptance tests completed. With this machine, we are able to write 0.1 μm lines and achieve level-to-level registration of 0.1 μm. We have written and tested successfully the necessary program to generate, with our in-house CAD circuit-layout system, tapes that can drive the LEBES system. It will therefore be quick and convenient to lay out circuits for fabrication by electron-beam lithography. We have also written a program for correction of proximity effects present in electron-beam lithography. With other sponsorship (ONR) we have developed a complete lead-alloy process for fabrication of superconductive integrated circuits. The process is modeled after that developed by IBM. Under that sponsorship, circuits have been demonstrated that employ some new concepts in A/D signal conversion. We have made functioning circuits containing more than 60 junctions. Work is beginning on making chips containing circuits for the miniaturization project. The circuits are made using 5 μm diameter junctions. Measurements will be made on such circuits as benchmarks for comparisons with the later miniaturized circuits.

On the theoretical side, we have completed a computer study of the optimization of a typical logic chip containing the IBM current injection logic (CIL) circuit family. The chip is considered divided into logic cells separated by sets of transmission lines. The aims of the calculation are to find the maximum number of gates on a given size chip and the minimum gate delay that can be achieved by circuit miniaturization and optimization.

There are a number of constraints to consider in miniaturization. The following must be satisfied by CIL logic:

(1) $I_m Z_0 < V_g$, where I_m is the critical current of the device, Z_0 is the characteristic impedance of the transmission line, and V_g is the gap voltage (V_g = 2.5 mV for lead technology). This condition insures adequate output signal when a CIL gate switches.

(2) Critical current I_m of a gate must be $\geq$ 40 - 50 μA to insure against noise switching.

(3) Critical current density of a junction J_c must be $\leq 10^4$ A/cm^2 due to the unsuitability of junctions with higher J_c's for latching-logic applications. (2. and 3. limit the minimum junction size.)

(4) LI_m, where L is the gate inductance, must remain constant under scaling to keep gains and margins constant.

The total logic delay t_D of a CIL gate has four components, ($t_D = t_0 + t_r + t_s + t_p$). The turn-on delay t_0 depends only on the capacitance C and I_m: for a given overdrive $t_0 \alpha (C/I_m)^{1/2}$. Since the capacitance of a junction is a very slowly varying function of the critical current density J_c, t_0 is approximately proportional to $[J_c]^{-1/2}$. The risetime t_r is proportional to the time constant CZ_0. For a given operating voltage V < V_g, $Z_0 \alpha [I_m]^{-1}$ (constraint no. 1). Therefore, t_r is proportional to $[J_c]^{-1}$. Each fan out causes a delay L_s/Z_0 where L_s is the crossing inductance of an interferometer control line. For a series fan out of n, $t_s = nL_s/Z_0$ i s the crossing delay. The transmission delay is $t_p = l\tau_p$, where l is a typical path and τ_p is the delay per unit length of the transmission line. For a superconducting transmission line $\tau_p \approx c^{-1}[\varepsilon(1+2\lambda/d_0)]^{1/2}$ where ε is the dielectric constant of the insulator, d_0 is the thickness of the insulator, and λ the penetration depth.

To optimize the performance of the circuits, the junction should be made with the highest possible J_c. At the limit of 10^4 A/cm^2, an interferometer with I_m = 50 μA would have junction size of 0.12 μm^2. Other considerations must be taken into account in optimizing scaled circuits. These considerations cause minimum junction sizes to be larger than indicated above. The line width of the interferometers and control lines should be made as small as possible, since the inductance per unit length of superconducting strip line is inversely proportional to their width.

The determination of other parameters is not as straightforward, since it involves trade-offs between various aspects of circuit performance. Increasing the width of the transmission lines would lower their characteristic impedance and allow a higher I_m (constraint no. 1), which implies a lower loop inductance L (constraint no. 4) and the size of the device is reduced. However, this increase causes greater mismatch between transmission lines and control lines, which requires larger space-consuming capacitors to correct, and of course, wider lines take up more space on the chip. A thinner insulator (smaller d_0) lowers the transmission line impedance but also lowers the propagation speed, and increasing the dielectric constant produces similar results.

The study of the CIL family optimization indicates that it should be possible to decrease the average gate delay (including transmission time and using an average fan-out of 2) from the value of 40 ps applicable for the present IBM design that uses 2.5 μm minimum feature size, to 12 ps, or a speed improvement of a factor of about three. The number of gates per chip would also increase by a factor of eight to 8000 gates for a chip of 6.35 mm by 6.35 mm. The minimum feature size in the optimum design is 0.2 μm for the control lines for the interferometers.

Recent Publications with JSEP Support

"Silicon-Coupled Josephson Junctions and Super-Schottky Diodes with Coplanar Electrodes," R. C. Ruby and T. Van Duzer, *IEEE Trans. on Electron Devices*, vol. ED-28, pp. 1394-1397, November 1981.

"Vertical Silicon Membranes for Super-Schottky Diodes," N. F. Raley, Y. Sugiyama and T. Van Duzer, *IEEE Trans. Magn.*, vol. MAG-19, pp. 507-511, May 1983. Also presented at Applied Superconductivity Conference, Knoxville, November 30 - December 3, 1982.

"(100) Silicon Etch-Rate Dependence on Boron Concentration in Ethylenediamine-Pyrocatechol-Water Solutions," Presented at Meeting of Electrochemical Society, San Francisco, May 8 - 13, 1983 and to be published in *J. Electrochemical Society*.

"Miniaturization of Josephson Current-Injection Logic (CIL) Circuits," H. Ko and T. Van Duzer, accepted for publication in *Proc. International Conference on Computer Design: VLSI in Computers*, New York, October 31-November 3, 1983.

Recent Publications without JSEP Support

"Digital Applications of Josephson Junctions," T. Van Duzer, *Proc. Symposium on Processing and Devices*, Stanford University, May 1, 1982.

"A Symmetrical Three-Junction Superconducting Quantum-Interference Device," S. H. Dhong, R. E. Jewett, J. W. Spargo and T. Van Duzer, *J. Appl. Phys.*, vol. 54, pp. 445-448, January 1983.

"Fabrication and Properties of High-J_c Lead-Alloy Junction," Y. Tarutani and T. Van Duzer, *IEEE Trans. Electron Devices*, vol. ED-30, pp. 34-39, January 1983.

"Josephson Analog-to-Digital Converter Using Self-Gating-AND Circuits as Comparators," S. H. Dhong, R. E. Jewett and T. Van Duzer, *IEEE Trans. Magn.*, vol. MAG-19, pp. 1282-1285, May 1983. Also presented at the Applied Superconductivity Conference, Knoxville, November 30 - December 1, 1982.

"A Pipelined Gray Code-to-Natural Binary Decoder for Use in a Josephson A/D Converter," J. W. Spargo, R. E. Jewett and T. Van Duzer, *IEEE Trans. Magn.*, vol. MAG-19, pp. 1255-1258, May 1983. Also presented at the Applied Superconductivity Conference, Knoxville, November 30 -December 1, 1982.

Government Scientific Contacts

The principal investigator for this project instigated the formation of a biennial workshop on Josephson digital circuits, was its first chairman for the meeting held in 1979, and continues to function in the leadership of the conference. This workshop brings together governmental, academic, and industrial groups in the U.S. that are working in this field. He is also a member of the board of directors of the Applied Superconductivity Conference. Both of these relationships bring him extensive interactions with scientific personnel from the Office of Naval Research, the Naval Research Laboratory, the National Bureau of Standards, and other governmental agencies.

Significant Accomplishments

During the last grant period the LEBES electron-beam lithography system was installed and the acceptance tests were satisfactorily performed. A program was written and demonstrated that made possible the use of our in-house CAD system for circuit layout for generating tapes that control the positioning of the electron beam. With this system we will be able to make rapid design changes in the circuits to be fabricated using the LEBES system. A program was written that will permit corrections in the electron-beam exposures to take account of proximity effects.

We have completed a computer study that shows how to optimize feature sizes in miniaturized current-injection-logic (CIL) circuits, the family now in use in the IBM project. The study shows the speed and circuit density improvements that can be expected in miniaturizing the CIL family. Compared with the present circuits that use 2.5 μm minimum feature size, the circuits with 0.2 μm minimum features will increase speed by a factor of three and the circuit density by a factor of eight.

Proposed Research Program

We will continue the computer studies of miniaturization of logic circuits of the type completed for the CIL family. The high level of interest in both the U.S. and Japan has led to the invention of several different logic families. These show a greater potentiality for improved density and performance by miniaturization than does the CIL family. These other types of circuits are combinations of resistors and Josephson junctions and do not contain interferometers, which are limited in their potentiality for miniaturization.

We will first make circuits in each of the several different logic families using feature sizes achievable with photolithography. Speed measurements will be made for comparison with scaled-down circuits. The scaling will be done in two stages; in the first, the minimum feature size will be about 0.7 μm which is easy for electron-beam lithography and is substantially smaller than present sizes. Speed measurements on these circuits will give the first experimental evaluation of our scaling calculations. Subsequently we will fabricate and test circuits having 0.2 μm minimum features. It is to be expected that a substantial effort will be required for successful fabrication of circuits of this size. If successful, these will be, by far, the smallest Josephson logic circuits demonstrated by anyone. They should also have the lowest speed-power products. We expect that it will be necessary to develop procedures for fabrication that are qualitatively different from those used for the somewhat larger circuits.

In addition to the innovations in fabrication required for these small circuits, there will be important questions of physics. There is evidence that for circuits that operate as fast as we expect for those of the smaller size, the model presently used in dynamic simulations may be inadequate. In dynamic

simulations that will be made to compare with measurements, it may be necessary to use a more precise model of the Josephson junction. Also, feature sizes may become comparable with penetration depth or coherence length and these complications will have to be taken into account in evaluation of the experimental results.

Interaction With Other Work Units

This program of miniaturization forms a part of a larger effort on various aspects of Josephson devices and circuits. One part of the effort is the development of a new concept in A/D conversion using the peculiar properties of Josephson circuits. A multi-layer process similar to those used in semiconductor integrated circuits has been established in our laboratory using lead-alloy superconductors. The miniaturization project draws heavily on the tools developed in the A/D project for simulation and fabrication. We will also be developing a niobium-based circuit fabrication process for superconductive integrated circuits during the coming 12 - 18 months and this technology will be transferred to the miniaturization project as it becomes functional.

Our work on Josephson devices and their frequent need for submicron dimensions has given our group a high degree of familiarity with electron lithography and we have published several papers in that field. This expertise will be supported by the microfabrication interests of Professors A. R. Neureuther and W. G. Oldham, as well as the large body of knowledge in our integrated circuits group (SSD-85-1).

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: SSD-84-3 **Last Year's No.(s):** N.A.

Title: Studies on Room-Temperature and Cryogenic Heterodyne Detection

Senior Principal Investigator(s): T. K. Gustafson (415) 642-3139
T. Van Duzer 642-3306

Scientific Objective

The object of this project is to gain fundamental understanding of the factors determining the conversion efficiencies and noise temperatures of metal-barrier-metal (MBM) room-temperature tunneling devices and cryogenic semiconductor-coupled super-Schottky and Josephson devices.

State of the Art

Superconductive devices have strong nonlinearities on the scale of their millivolt energy gaps, and make excellent detectors and mixers that can be expected to operate at frequencies as high as about 600 GHz (about 0.5 mm wavelength). For higher frequencies (far-submillimeter and far-infrared wavelengths), the MBM devices with their nonlinearities on a scale of a few volts become equally effective and have the advantage that they can be operated at room-temperature.

At frequencies corresponding to the infrared or higher, quasi-optical coupling techniques are being studied for coupling radiation into MBM junctions; however, up to the present time quantitative measurements of the power coupled and hence conversion loss, noise temperature etc. have been lacking. The most accurate measurements of such parameters have been made by Slayman at 36 GHz (1), a frequency that was convenient for parametrizing the detection and mixing characteristics, but not high enough for the MBM to be competitive with the Schottky diode or with superconducting junctions. However, even at 36 GHz the noise temperature of the MBM as a heterodyne mixer was found to be of the order of 1000^{o}K, which was within a factor of two or three of commercially available room temperature Shottky diodes. The conversion loss, on the other hand, was of the order of 22 dB as compared to the 5 dB typical of a Schottky diode. This is presumably a reflection of the low nonlinearity of the MBM device.

Tinkham (2) has posed some interesting questions in regards to mixing with a variety of devices and raised the question of a nonlinearity-bandwidth product which is conserved. He established this result and other related results on the basis of a Schottky tunnel diode but argued that it should be true of the MBM as well. In this manner he also argued that for many practical situations it would be appropriate to treat the current as arising from a tunneling process, be it an MBM or a Schottky device.

In separate recent work, Daniel et al. (3) and Evenson et al. (4) have reported a 2.3 dB/decade roll-off in the signal-to-noise ratio of both the MBM and Schottky devices as heterodyne mixers. We have attributed this to propagational loss of the mode propagating within the junction of the detector (5), although this has by no means been clearly established. If this is indeed the case, it could be decreased by cooling of the junctions to decrease phonon collisions.

These three aspects: quantitative measurements (similar to those carried out by Slayman), verification of Tinkham's theoretical work, and an investigation of the 2.3 dB/decade measured roll-off as a function of temperature, would be interesting to pursue at 90 GHz. This would provide quantitative data and experimental verification of the theory, which could be utilized in the design of mixers and detectors at higher frequencies for which such data is not available and is much more difficult to obtain directly.

For mixers and detectors at 90 GHz, in order to attain noise temperatures below several thousand degrees Kelvin, the proposed frequency of concentration in this project, cryogenic devices must be used. The lowest noise temperature in this frequency range was attained with an SIS at 115 GHz (68 K) (6).

There is considerable activity presently in studying mixing with superconductor-insulator-superconductor (SIS) tunnel junctions with results reaching quantum limits and in which conversion gain is sometimes seen (7). Cooling of Schottky diodes has been shown to be beneficial in improving the noise temperature of the diode and its conversion efficiency for temperatures down to about 40 K. At lower temperatures, the useful nonlinearity, which derives from thermal excitation over the barrier, is, however, lost because of the linear and symmetric tunneling current that becomes relatively more important. In the super-Schottky diode, the normal-metal contact is replaced by a superconductor and an exponential I-V characteristic in the millivolt range results from the energy gap of the superconductor; its shape is retained down to the lowest temperatures and the sensitivity factor $S = k_B T/e$ has been measured to be as high as 11,600 (compared with a maximum of 300 for cooled Schottky diodes). In earlier mixing studies with super-Schottky diodes, excellent diode noise temperatures were achieved and with very good system noise temperatures at 10 GHz (8). The high series resistance of the semiconductor substrate leads to large parasitic losses as frequency is raised in the configuration employed in that study. Studies of mixing with the Josephson effect in point contact devices showed SSB gain of 1.4 and mixer noise temperature of 54 K at 36 GHz. Also work at 115 GHz demonstrated mixer noise temperature of 120 K and conversion efficiency of 1.0 using point contacts (7). The conversion efficiency in Josephson mixing increases with a high product of junction critical current and normal-state resistance ($I_c R_n$) and reasonably good values were achieved by careful adjustment of point contacts. The method of operation demands nonhysteretic I-V characteristics so Josephson tunnel junctions are precluded except with heavy shunting, which degrades the $I_c R_n$ product. Our semiconductor-coupled Josephson junctions have had both nonhysteretic characteristics and high $I_c R_n$ products.

During the previous contract period, a 90 GHz system was assembled and tests are presently in progress to measure the video detection properties of one configuration of a super-Schottky diode with coplanar superconductive electrodes. Considerable understanding has been developed concerning the optimum design for such a diode.

Progress and Publications Since Last Major Proposal

To investigate the nonlinearity of tunneling junctions at high frequencies, as well as the quasi-optical coupling scheme, we have devised a harmonic heterodyne mixing experiment which uses conveniently available sources in our laboratory, and provides a high frequency output which can be monitored on a spectrum analyzer. This involves the heterodyne mixing of the output of a water vapor laser with a frequency of 11 THz and the output of a carbon dioxide laser with a frequency of 32 THz (Fig. 1). The output frequency $\omega_{IF} = 3\omega_{H_2O} - \omega_{CO_2}$ should be at approximately 20 GHz. Preliminary calculations have been carried out in three stages. First the input coupling has been analyzed, following this the conversion efficiency has been obtained, and finally the output coupling to the spectrum analyzer deduced.

The configuration for this equipment is shown in Fig. 2a and the profile of our "edge-MBM" structure is shown in Fig. 2b. As shown in Fig. 2a, one observes that the quasi-optical coupling involves a bevelled edge on the silicon substrate structure. This allows "phase-matching" of the incident radiation field to the surface waves on the antenna structure and hence a coupling to the junction current. A coplanar waveguide is used to couple the 20 GHz radiation to a coaxial cable through a taper for impedance matching purposes.

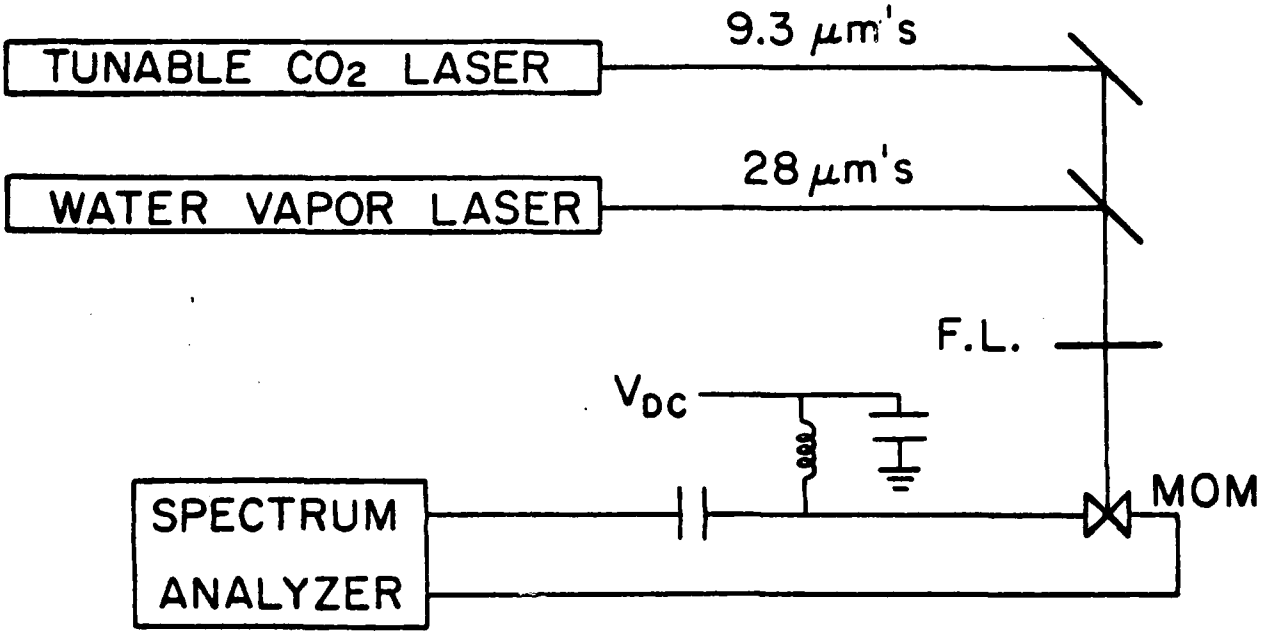
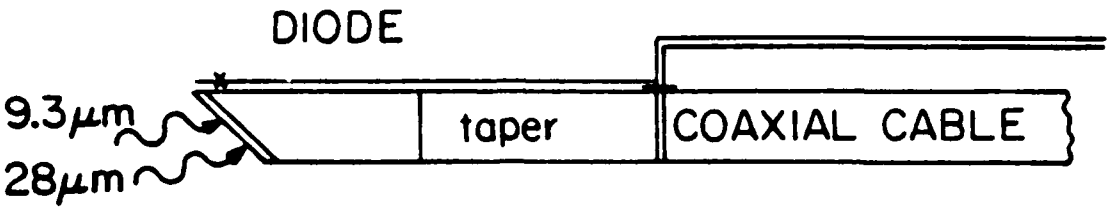
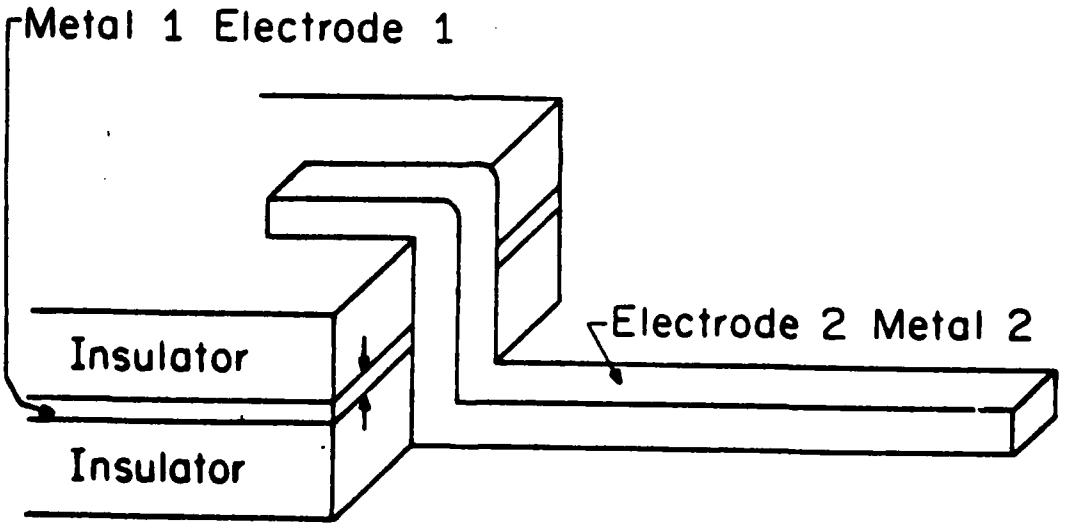


Fig. (1). Configuration of the quasi-optical harmonic mixing using a water vapor laser and a Co_2 laser resulting in a 20 GHz i.f. frequency.



(2a)



(2b)

Fig. (2). Profile of the junction configuration for the harmonic mixing experiment of Fig. (1). (a) physical layout of the MBM diode, strip line, and silicon substrate; (b) profile of the edge MBM showing the two metal electrodes. The barrier is an oxide between these two.

We have accomplished the fabrication of the diode structures on the bevelled silicon substrate. We are presently discussing the necessity of imbedding the antenna structure within the substrate to obtain a proper termination of the antenna. We are also in the process of setting up and testing the lasers, spectrum analyzer and post detection processing equipment. The rather detailed numerical estimates indicate that at a minimum, one should observe a -83 dBm signal for such an experiment.

Most of our effort with regard to low temperature work during the last period was devoted to studies of the fabrication of the families of Josephson and super-Schottky devices that employ crystalline silicon. One class of device is formed by etching a pit bounded by (111) planes in a (100) silicon wafer to form a thin (≈ 100 nm) membrane as the floor of the pit. The etching is stopped at the desired thickness of membrane by boron previously diffused in from the back side. We have developed a two-step process in which a thicker membrane ($\approx 2\mu m$) is formed first; then it is measured by determining the energy required to pass electrons through it and, with that knowledge, the small etch pit is made in the thick membrane. By this procedure, we can make membranes of 50 to 150 nm in thickness and areas controlled down to about 1 μm^2 to achieve the desired device resistance for convenient RF matching. The measurement of the membrane thickness by electron-beam transmission was done in a scanning electron microscope; the energies for transmission were determined for remaining portions of broken membranes and correlated with direct measurements of the edges. The resulting calibration allows nondestructive determination of thickness in the range of 100 nm to several microns. In order to do the second etching step it is necessary to out-diffuse the heavy ($> 7 \times 10^{19}\ cm^{-3}$) concentration of boron to prepare for the shallow diffusion used as a stop for the thin membrane etching. Damage to the silicon surface occurs during out-diffusion; an extensive study of out-diffusion was required to control the process. Also, knowledge of the dependence of etch rate on boron concentration was not available in the literature, and understanding of the electrochemical reasons for this dependence was not adequate. We conducted a systematic study which has led to a major paper that should be of use to the many different projects that are now using boron-stopped silicon etching for various applications. The work on thickness measurement and out-diffusion will be prepared for publication soon.

Our knowledge of silicon etching was also applied to form a new device configuration in which anisotropic etching of a (110) surface of silicon with a thin protective strip leads to the formation of a vertical membrane which can have a height of at least 1 μm and thickness of less than 0.1 μm. There are various ways of doping and electrode deposition that can produce either super-Schottky diodes or Josephson junctions. To date we have made super-Schottky devices and are in the process of testing these as video detectors at 90 GHz.

One of the tasks done during the last period was to assemble and calibrate a 90 GHz millimeter-wave system with the components required to make measurements of video detection responsivity and NEP and also noise temperature and conversion efficiency in heterodyne detection for low-noise devices. Room-temperature devices (e.g., MBMs) require measurements made with sine-wave sources for both local oscillator and signal; it will be necessary to supplement our system with an additional 90 GHz source.

Recent Publications with JSEP Support

"Metal-Barrier-Metal Junctions for Room Temperature Millimeter-Wave Mixing

and Detection," C. W. Slayman and T. K. Gustafson, *Proc. IEEE MTT-S*, 338-340 (1981); also *International Microwave Symposium Digest*, June 15-19, Los Angeles (1981).

"A Phototransistor with Concentric Electrodes on the Si Substrate," C. W. Chen and T. K. Gustafson, *IEEE Electron Device Lett.*, EDL-2, 200 (1981).

"Junction Surface Detectors and Mixers for Integrated Optics," *Proc. National Science Foundation Grantee-User's Meeting*, Boston (June 1983), to appear (partial JSEP support).

"Optical Interactions Between Confined Surface Electromagnetic Waves and Tunneling Transitions in Junction Devices," T. K. Gustafson, R. Hemphill, J. Wummer and S. R. Whiteley, *Proc. of the SPIE Technical Symposium East* held April 4 - 8, 1983, arlington, VA (to be published).

"Silicon-Coupled Josephson Junctions and Super-Schottky Diodes with Coplanar Electrodes," R. C. Ruby and T. Van Duzer, *IEEE Trans. on Electron Devices*, ED-28, 1394-1397 (November 1981).

"Vertical Silicon Membranes for Super-Schottky Diodes," N. F. Raley, Y. Sugiyama and T. Van Duzer, *IEEE Trans. Magn.*, MAG-19, 507-511 (May 1983). Also presented at Applied Superconductivity Conference, Knoxville, November 30 -December 3, 1982.

"(100) Silicon Etch-Rate Dependence on Boron Concentration in Ethylenediamine-Pyrocatechol-Water Solutions," presented at Meeting of Electrochemical Society, San Francisco, May 8- 13, 1983, and to be published in *J. Electrochemical Society*.

"Miniaturization of Josephson Current-Injection Logic (CIL) Circuits," H. Ko and T. Van Duzer, accepted for publication in *Proc. International Conference on Computer Design: VLSI in Computers*, New York October 31 - November 3, 1983.

Recent Publications without JSEP Support

"Stimulated Emission of Surface Plasmons in Metal-Insulator-Degenerate p-type Semiconductor Structures," S. R. Whiteley, L. Z. Xie, R. Hemphill and T. K. Gustafson, to appear in *Applied Phys. Lett*, (Sept. 1983).

"Relation of Stimulated and Spontaneous Transitions in Tunneling Structures to the Elastic Current-Voltage Characteristic," S. R. Whiteley, L. Z. Xie, R. Hemphill and T. K. Gustafson, *Appl. Phys. Lett.*, 41, 868 (1982).

"Stationary State Model for Normal Metal Tunnel Junction Phenomena," S. R. Whiteley and T. K. Gustafson, *IEEE J. Quantum Electronics*, QE-18, 1387 (1982).

"Metal/Tunnel-Barrier/Semiconductor/Tunnel-Barrier/Metal Fast Photodetector," S. Thaniyavarn and T. K. Gustafson, *Appl. Phys. Lett.*, 40, 255 1982).

"Sequence Frequency Three-Wave Mixing Emissions in a Birefringent Fiber," K. Kitayama, M. Ohaski and T. K. Gustafson, submitted to *IEEE J. Quantum Electronics (in review)*.

"Digital Applications of Josephson Junctions," T. Van Duzer, *Proc. Symposium on*

Processing and Devices, Stanford University (May 1, 1982).

"A Symmetrical Three-Junction Superconducting Quantum-Interference Device," S. H. Dhong, R. E. Jewett, J. W. Spargo and T. Van Duzer, *J. Appl. Phys.*, 445-448 (January 1983).

"Fabrication and Properties of High-J_c Lead-Alloy Junction," Y. Tarutani and T. Van Duzer, *IEEE Trans. Electron Devices*, ED-30, 34-39 (January 1983).

"Josephson Analog-to-Digital Converter Using Self-Gating-AND Circuits as Comparators," S. H. Dhong, R. E. Jewett and T. Van Duzer, *IEEE Trans. Magn.*, MAG-19, 1255-1258 (May 1983). Also presented at the Applied Superconductivity Conference, Knoxville, November 30 - December 1, 1982.

"A Pipelined Gray Code-to-Natural Binary Decoder for Use in a Josephson A/D Converter," J. W. Spargo, R. E. Jewett and T. Van Duzer, *IEEE Trans. Magn.*, MAG-19, 1255-1258 (May 1983). Also presented at the Applied Superconductivity Conference, Knoxville, November 30 - December 1, 1982.

Government Scientific Contacts

T. K. Gustafson has been actively involved in the NSF-sponsored Grantee-User's Meetings (under Mr. E. Schutzman) which are held yearly. These involve mutual discussion among governmental, university and business of problems related to optical communications and a publication of the proceedings of the conference. In addition, he has been involved through grants and contracts with NASA and the Jet Propulsion Laboratory.

T. Van Duzer instigated the formation of a biennial workshop on Josephson digital circuits, was its first chairman for the meeting held in 1979, and continues to function in the leadership of the conference. This workshop brings together governmental, academic, and industrial groups in the U.S. that are working and supporting work in superconductive electronics. He is also a member of the board of directors of the Applied Superconductivity Conference. Both of these relationships bring him extensive interactions with scientific personnel from the Office of Naval Research, the Naval Research Laboratory, the National Bureau of Standards, and other government agencies.

Significant Accomplishments

The efforts discussed in the first reference under "Publications with JSEP Support" describe the most quantitative measurements made on MBM junctions to date. These showed that if the coupling at higher frequencies can be accomplished, then reasonable detectors and mixers are to be expected. This, coupled with the propagational losses discussed in the fourth reference, are particularly significant since they relate directly to sensitivities and noise performance expected at higher frequencies.

The development of the edge MBM junction on an etched silicon substrate is expected to provide a new approach to quasi-optical coupling utilizing what we have termed length confinement coupling to the surface electromagnetic modes of the junction structure. Significant progress has been made in theoretically analyzing and understanding the basic concepts of this coupling in our fabricated structures.

The assembly and careful calibration of the 90 GHz system that was done makes available an important test system which will be used to evaluate the detection and mixing properties of various devices. This system employs a dewar that can be magnetically shielded and is located in an

electromagnetically shielded room, a necessity for very low noise measurements.

Many of the problems of fabrication have been solved for the super-Schottky diodes and Josephson junctions employing crystalline silicon. The work has produced data and theoretical understanding of properties of boron-doped silicon that will be useful not only in the present project, but also for the community using silicon for other purposes. A new device configuration has been made and its detection properties are being studied.

Proposed Research Program

The intention of the combined effort is to make common use of existing apparatus to study two different device families for heterodyne detection at the important frequency of 90 GHz. A common structure will be constructed for matching the waveguide to the detector device, and the RF system would be common except that the signal source for the MBM measurement would be a modulated and filtered portion of the Gunn oscillator, whereas noise sources will be used for the cryogenic devices. The commonality of test facilities should lead to a good deal of interaction of the research assistants working on the two device types, as well as efficiency of the research.

90 GHz provides an excellent frequency choice for future MBM work. This is midway between our quasi-optical coupling exeriments, which we plan to continue, and the 35 GHz experiments of Slayman, which yielded important quantitative data on noise temperature and conversion loss, as well as sensitivity. It is low enough so that excellent coupling efficiency measurements can be conveniently made and yet high enough so that one might expect to begin observing a frequency roll-off due to metallic losses within the junction competing with the tunneling transitions, as far as coherent detection is concerned. The thermal contribution is temperature sensitive and thus it is possible that this could be measured and the theoretical basis of the 2.3 dB/decade roll-off checked accurately using 90 GHz results.

Many of the fabrication problems of silicon-coupled super-Schottky and Josephson devices have been solved. Contact resistance between the superconductor and silicon is still larger than expected from theory. Diffusions of high doping levels of boron in silicon lead to the formation of a Si-B layer on the surface with a boron glass on top. The latter can be easily removed chemically, but the Si-B layer must be oxidized and then removed. A rather complete study of the Si-B layer has been done under other sponsorship and it now seems possible to oxidize it at low temperatures without disturbing the dopant in the silicon. Alternatively, we will use implantation instead of diffusion; this will avoid the growth of the Si-B layer but may have other, as yet unknown, problems. With the contact resistance problem solved, we will make devices of coplanar and etch-pit types. We will correlate the mixing results with the existing theories involving Josephson and single-particle tunneling to determine whether our understanding of the models for the devices is correct. The work will also show whether the devices are competitive with the SIS tunneling devices that are now under investigation in our own and other laboratories. If comparable electrically, the silicon-coupled devices should be advantageous from the viewpoint of ruggedness. The structure also should be adaptable to high-T_c superconductors so that operation would be possible at 10 K, where small refrigerators are available.

Interaction with Other Work Units

Interactions will occur with other units in connection with sharing fabrication expertise, tunneling and superconductivity experience, and regarding

millimeter-wave mixing. Our fabrication work is done in the ERL microfabrication facility and there is considerable sharing of fabrication techniques among the research assistants of the various groups. A high level of theoretical expertise in tunneling exists in Professor T. K. Gustafson's group for other projects. The cryogenic work proposed here is part of a larger effort in superconductive electronics, including work on digital circuits especially aimed toward A/D conversion and basic physics studies on devices coupled by crystalline silicon. Work on millimeter-wave mixing is in progress in Professor S. E. Schwarz's group as well as in Professor P. L. Richard's group in the Physics Department and in the Radio Astronomy Department. There is a continuing strong level of interaction among the research assistants of the various groups.

References

(1) C. W. Slayman, "Metal-Barrier-Metal Junctions for Millimeter Wave Mixing and Detection," Ph.D. Thesis, University of California, Berkeley (1980) (unpublished).

(2) M. T. Tinkham, "Fundamental Considerations Limiting Tunnel Diode Mixers and Detectors" (unpublished).

(3) H. U. Daniel and M. Steiner, *Appl. Phys. Lett.*, 25, 7 (1981).

(4) R. E. Drulinger, K. M. Evenson, D. A. Jennings, R. F. Peterson, J. C. Berquist, Lee Burkins and H. U. Daniel, *Appl. Phys. Lett.*, 42, 137 (1983).

(5) Final Report, NASA Grant NAG-3-88.

(6) S-K. Pan, M. J. Feldman, A. R. Kerr and P. Timbie, "A Low-Noise 115 GHz Receiver using Superconducting Tunnel Junctions," submitted for publication June 1983.

(7) P. L. Richards and T-M. Shen, "Superconductive Devices for Millimeter Wave Detection, Mixing, and Amplification," *IEEE Trans. Electron Devices*, ED-27, 1909-1920 (October 1980).

(8) F. L. Vernon, Jr., M. F. Millea, M. F. Bottjer, A. H. Silver, R. J. Pederson and M. McColl, "The Super-Schottky Diode," *IEEE Trans. Microwave Theory and Tech.*, MTT-25, 286-294 (April 1977).

University of California, Berkeley — **Electronics Research Laboratory**

Joint Services Electronics Program — **August 15, 1983**

Work Unit No.: SSD-84-4 — **Last Year's No.(s):** SSD-83-4

Title: Research on Electronic Systems Composed of Polymer Films and Planar Silicon Devices

Senior Principal Investigator(s):		
	D. W. Hess	(415) 642-4862
	R. S. Muller	642-0614
	R. M. White	642-0540

Scientific Objective

We propose to investigate several novel processes for forming piezoelectric polymer films on silicon substrates. The objective of this research is to develop techniques that form polymer films with good piezoelectric activity by depositing the films in the presence of an electrical field. Plasma enhanced chemical vapor deposition and solution polymerization techniques will be carried out using vinylidene fluoride monomer to polymerize films directly on silicon substrates. We expect that depositing films in the presence of an electrical field will yield polyvinylidene fluoride films with high piezoelectric activity and superior thermal stability relative to those formed by conventional means. In addition, this type of field-enhanced deposition may be expected to form piezoelectric films of other polymers such as polyacrylonitrile that previously have not shown significant piezoelectric activity.

State of the Art

Semi-crystalline polymers with aligned dipoles such as polyvinylidene fluoride have been shown to display good piezoelectric properties (1). Thus far, the best polyvinylidene fluoride films are extruded; the films are then stretched and poled. We propose to deposit thinner films than can be formed by extrusion directly on silicon. By depositing the films in the presence of an electric field we will attempt to align dipoles during polymerization, yielding piezoelectric thin films directly on silicon substrates. This type of processing eliminates the stretching and poling operations currently needed (2).

Progress to Date

Three important experimental systems have been assembled to characterize piezoelectric polymer films. The first system is a laser interferometer. This interferometer is similar to a Michelson interferometer, but uses optical heterodyning to provide a linear, sensitive output signal capable of detecting 0.1 Angstrom mechanical displacements. Data taken from this system will be used to determine piezoelectric activity of polymer films.

The second experimental system is a multistate Thermally Stimulated Discharge Spectrometer (3). This spectrometer measures the activation energy of each charge trapping mechanism in addition to giving the amount and type of polarization.

Finally, an apparatus for measuring the pyroelectric properties of polymer films has been developed. A polymer sample is placed in an environmental chamber and the temperature is ramped up or down at a fixed rate. The reversible current produced as the temperature changes is used to calculate one of the pyroelectric coefficients of the sample. It has been shown that pyroelectric activity is often related to piezoelectric activity of the polymer sample (4).

Significant Accomplishments

We have developed analytical tools capable of measuring the piezoelectric, pyroelectric, and charge-trapping mechanisms in polymer films. A plasma enhanced chemical vapor deposition reactor has been fabricated that can be used to deposit polymer films. Finally, an apparatus for corona poling polymer films has been built.

Proposed Research

The goal of this research is to develop techniques suitable for the production of piezoelectric polymer transducers with high piezoelectric activity and long term stability. Simultaneous film formation and poling appears to offer a

novel fabrication method for forming such films.

Molecular dipole orientation is considered a primary cause of piezoelectricity in polymer films (5). During film deposition, the molecules forming a film are in their most fluid state and thus most easily aligned. We will examine several types of film deposition techniques that can be carried out in the presence of an electric field.

The first such technique is solvent casting. Films can be solvent cast with a solvent that evaporates slowly while an electrical field is applied normal to the surface of the film. The electric field will be applied using closely spaced electrodes or by charging the surface of the film via a corona discharge. It may be possible to initiate a solution polymerization of liquid monomer directly on a substrate while in the presence of an electric field. Finally, plasma enhanced chemical vapor deposition can be used to form polymer films while an electric field aligns molecular dipoles. The electric field in plasma deposition can be from the plasma itself (sheath potential) or it can be a DC field that comes from a second set of electrodes placed downstream from the glow discharge (6).

Piezoelectric activity will be determined using the interferometer previously described. This will be done by electrically driving the piezoelectric film with a known voltage and measuring the resulting mechanical movement using the interferometer. In addition to measuring the magnitude of piezoelectric constants, the phase difference between the driving voltage and the resulting mechanical displacement can be used to calculate piezoelectric relaxation as a function of frequency.

Additional analytical techniques will be used to characterize the polymer films. Molecular and crystalline structure and composition will be investigated using infrared and x-ray spectroscopy. Charge storage mechanisms will be studied using the previously described thermally-stimulated discharge system.

We will also develop a mathematical model that is based on general continuum mechanics that form a foundation for describing nonlinear and dissipative materials in the thermoelastic system (7). We have modified this work to include electrical effects, and plan to continue this work to model nonlinear piezoelectric materials.

References

(1) R. G. Kepler, *Ann. Rev. Phys. Chem.*, 29, 497 (1978).

(2) R. Hayakawa and Y. Wada, *Adv. Polymer Sci.*, 11, 1 (1973).

(3) J. van Turnhout, *Thermally Stimulated Discharge of Polymer Electrets*, Elsevier Publishing Co., Amsterdam, 1975, Chapter 9.

(4) G. M. Sessler, *Topics in Applied Physics*, 33, (1980).

(5) A. J. Lovinger, in *Development in Crystalline Polymers*, ed. by D. C. Bassett, Applied Science Publishers, 1982, p. 195.

(6) M. Shen and A. T. Bell, *Plasma Polymerization*, ACS Symposium Series, 108 (1977).

(7) P. M. Naghdi, *Energy*, 5, 771-781 (1980).

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: SSD-84-5 **Last Year's No.(s):** SSD-83-3

Title: Wide-Dynamic-Range Signal Processing Using Monolithic Integrated Circuit Technology

Senior Principal Investigator(s):	R. G. Meyer	(415) 642-8026
	R. W. Brodersen	642-1779
	P. R. Gray	642-5179

Scientific Objective

To investigate new techniques for signal processing with maximum dynamic range using monolithic integrated-circuit technology. The project will encompass noise characterization, system design, new circuit topologies and a coordinated program of technology research.

State of the Art

Monolithic integrated-circuit technology has profoundly affected the field of signal processing. Functions such as A/D and D/A conversion[1], filtering[2], and digital signal recovery[3] are examples where monolithic technology has become the preferred method of realization in many systems. These functions are crucial components in systems such as radar, sonar and communication networks. A key problem limiting the performance of such systems is the effective dynamic range of the signal processors. In a recent example[4] a complete analog-digital interface for a monolithic data acquisition system achieved a dynamic range of 86 dB at a sampling rate of 32 Hz. Future improvements in the performance of such systems will require basic research on thermal noise in switches and operational amplifiers and the sources of nonlinearity in filters, sample-and-hold circuits and data converters.

Progress and Publications Since last Major Proposal

Our earlier work on the fabrication, characterization and modeling of generalized multi-layer monolithic structures allowed us to realize a unique monolithic process incorporating high-frequency JFET structures with independently-accessible gates. Extensive characterization on a range of devices has been undertaken and verified the advantages of these structures for a wide range of high-frequency signal processing areas. In particular, it appears possible to advance the state of the art significantly in the realization of high-frequency monolithic filters and real-time signal processing. Experimental high-frequency filters using this process are currently in fabrication. These filters incorporate very-wide-band operational amplifiers (unity gain beyond 100 MHz) made possible by the unique JFET structures described previously. This project will continue with further work in combining advanced fabrication techniques and new system concepts with the ultimate goal being the realization of unique methods of high-speed signal processing using arbitrary combinations of analog and digital techniques.

A second aspect of our work has involved new techniques to achieve maximum possible dynamic range in bipolar and MOS analog amplifiers and signal-processing circuits. Our work in this area has focussed initially on methods of achieving maximum dynamic range in switched-capacitor filters. In such devices, the fundamental limit on dynamic range results from thermal noise in the MOS switch transistors used in the filter structure, but monolithic switched-capacitor filters produced to date have not approached this limit because of the dominant effects of flicker noise in the MOS transistors making up the operational amplifiers[2,5]. Our research has resulted in a new differential chopper-stabilized technique which removes this 1/f noise, resulting in experimental fifth-order filter prototypes with dynamic range in excess of 105 dB. This is more than 15 dB higher than previously reported performance obtained from such filters[6]. We expect to continue this work with the objective of exploring the maximum theoretical dynamic ranges achievable, and formulating detailed theories of the noise performance of such filters.

Significant Accomplishments

(1) A new high-frequency bipolar monolithic process has been devised and extensively characterized for both low-frequency and high-frequency parameters. This research has led to new circuit configurations for high-frequency monolithic filters, switches and amplifiers which are currently being fabricated.

(2) A new chopper stabilized differential filtering technique was developed, and a monolithic prototype fabricated. This prototype has been extensively characterized, demonstrating dynamic range and power supply rejection performance well beyond any previously published levels. An extensive theoretical analysis of the sources of noise in switched capacitor filters has been carried out, resulting in a better understanding of the fundamental limitations on dynamic range as a function of energy storage element values. These results have been subsequently applied to the bandpass case, with important conclusions regarding the dynamic range of high-Q bandpass filter structures.

(3) During the past period we have made considerable progress in research on new methods for the design and implementation of high-frequency switched-capacitor filters for communications. We have designed and fabricated a sixth order bandpass switched capacitor filter with center frequency of 250kHz, bandwidth of 10kHz, and clock rate of 4MHz. The unique circuit approach incorporates fully differential signal paths, identical resonators, and cascode differential CMOS operational amplifiers.

(4) We have devised new topologies for switched capacitor filters in NMOS technology, which utilize positive feedback to overcome the limited gain achievable in NMOS single-stage amplifiers. A sixth order elliptic filter with center frequency at 250kHz was fabricated and tested. The effects of intermodulation at high signal levels in amplifiers of this type are now being investigated.

(5) Our research in high-frequency bipolar monolithic circuits has resulted in the realization of a new monolithic amplifier topology. A number of circuits have been fabricated incorporating unique dual-gate FET structures and giving bandwidths of 50MHz, gain of 66 dB and slew rates of 125v/μsec.

A. Publications under JSEP

K. C. Hsieh and P. R. Gray, "A low noise chopper stabilized differential switched capacitor filtering technique," *Digest of Technical Papers*, 1981 International Solid State Circuits Conference, New York, NY, February 1981.

P. R. Gray, R. W. Brodersen, D. A. Hodges, T. Choi, R. Kaneshiro and K. C. Hsieh, "Some practical aspects of switched capacitor filter design," *Digest of Technical Papers*, 1981 International Symposium on Circuits and Systems, Chicago, April 1981.

K. C. Hsieh, P. R. Gray, D. Senderowicz and D. G. Messerschmitt, "A low-noise switched capacitor filtering technique," *IEEE J. Solid-State Circuits*, December 1981.

S. K. Lui and R. G. Meyer, "High frequency-JFET-I^2L process," *IEEE Trans. on Electron Devices*, vol. ED-29, no. 8, August 1982.

P. R. Gray and R. G. Meyer, "MOS Operational Amplifier Design - A Tutorial

Overview," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 6, December 1982, pp. 969-982.

Proposed Research Program

Basic research on techniques for maximizing dynamic range in signal processing circuits will proceed in several directions. At the high end of the dynamic range the limitation on signal level is set by internally generated distortion. We have begun a program of research into distortion mechanisms in sampled-data systems and propose to extend and generalize this work

We have identified a number of distortion mechanisms in such systems and future work will be directed towards characterization and minimization of such effects. We have isolated one distortion mechanism in particular which is common to several classes of sampled-data systems. This is slew-limiting distortion which is a major limitation on the dynamic range of switched-capacitor filters, digital-to-analog converters and sample-and-hold amplifiers. The mechanism by which this distortion manifests itself is quite complex and will be the subject of research with the object of deriving analytical methods for its description and thus for its minimization. This is closely linked with topological considerations, particularly for switched-capacitor filters. As part of this research, we aim to devise new topologies for switched-capacitor filters with ranges as high as 100 dB. This will require basic research into other nonlinear mechanisms such as the influence of capacitive nonlinearities and voltage-dependent MOS clock feedthrough. Methods of analysis of such effects in sampled-data systems have not yet been derived and this is a prime goal of this project. Achievement of very wide dynamic range in sampled-data systems requires extremely high-performance amplifiers in critical locations. As part of this work we are investigating new topologies for low-noise fast-slewing monolithic amplifiers. Fully-differential Class AB topologies appear very promising in this regard. We expect to fabricate and test prototype amplifiers in our integrated-circuit facility as part of this research.

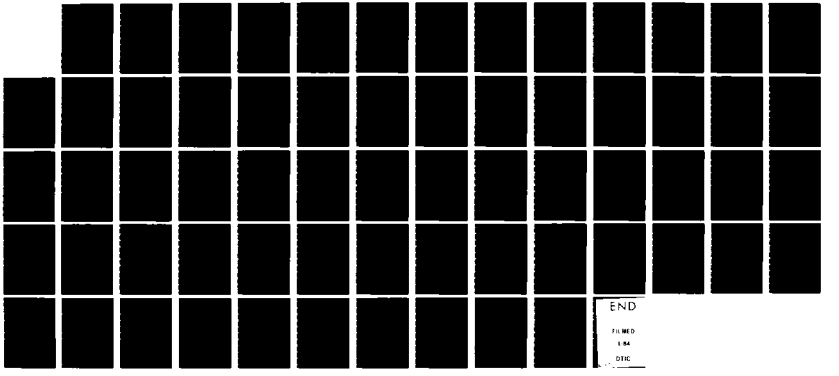
At the low signal end of the dynamic range, noise mechanisms determine the minimum usable signal level. We now are able to predict a priori the noise behavior of switched capacitor filters once the device noise parameters are known. We are now extrapolating these results to attempt to draw general conclusions regarding noise limitations in high-Q bandpass switched capacitor filter applications. These filters will become quite important in high frequency communications applications. We are currently fabricating a number of prototypes of such filters which will allow us to compare our theoretical results with experimental observations.

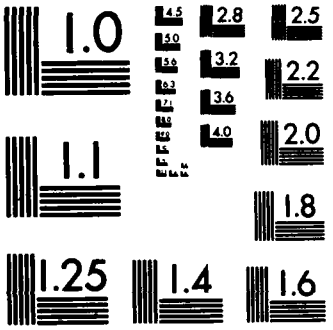
Another aspect of this research will focus on the problem of dynamic range in high-Q switched capacitor filters. We have determined that from a fundamental standpoint, high-Q switched capacitor filters must suffer in dynamic range relative to lowpass filters of the same bandwidth by a factor equal to the square root of the ratio of the center frequency to the bandwidth. For filters with Q on the order of 100, this is a severe limitation, giving typical dynamic range on the order of 70 dB as opposed to 90 dB for lowpass filters. We propose to study alternate filter architectures which achieve better dynamic range performance. The use of decimation through a cascade of lower Q filters appears to be a promising avenue for achieving better dynamic range.

References

(1) G. L. McCreary and P. R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 6, Dec. 1975, pp. 371-379.

AD-A136 058 JOINT SERVICES ELECTRONICS PROGRAM(U) CALIFORNIA UNIV 2/2
BERKELEY ELECTRONICS RESEARCH LAB D J ANGELAKOS
30 SEP 83 UCB/ERL-83/1 AFOSR-TR-83-1076
UNCLASSIFIED F49620-79-C-0178 F/G 9/5 NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

(2) D. J. Allstot, R. W. Brodersen and P. R. Gray, "MOS switched capacitor ladder filters," *IEEE J. Solid-State Circuits*, vol. SC-13, no. 6, Dec. 1978, pp. 806-814.

(3) R. R. Cordell, J. B. Forney, C. N. Dunn and W. G. Garrett, "A 50 MHz phase and frequency-locked loop," *IEEE J. Solid-State Circuits*, vol. SC-14, no. 6, Dec. 1979, 1003-1010.

(4) R. K. Hester, K. S. Tan and C. R. Hewes, "A monolithic data-acquisition channel," *Digest of Technical Papers*, 1983 International Solid-State Circuits Conference, N. Y., February 1983,pp. 122-123.

(5) D. Senderowicz, D. A. Hodges and P. R. Gray, "High-performance NMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-13, no. 6, Dec. 1978, pp. 760-766.

(6) P. R. Gray, D. Senderowicz, H. O'Hara and B. Warren, "A single-chip NMOS dual channel filter for PCM telephony applications," *IEEE J. Solid-State Circuits*, vol. SC-14, no. 6, Dec. 1979, pp. 981-991.

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: SSD-84-6 **Last Year's No.(s):** N.A.

Title: High-Field Transport in MOS Devices

Senior Principal Investigator(s): C. Hu (415) 642-3393
P. Ko 642-2302

Scientific Objectives

With the aggressive scaling of VLSI devices, it is increasingly apparent that the basic understanding of the high-field transport phenomena has lagged behind the progress in fabrication technologies. Both current designs, and more importantly, projections of future limits on device size, operating voltage, and reliability are principally based on (extrapolations of) empirical data. This proposal has the objective of clarifying the physics of such high field transport phenomena as the short-channel device I-V characteristics, the substrate current, the gate current, light emission from silicon MOSFET, and finally breakdown. From such knowledge, we will investigate the limits of device scaling and reliability. With the limitations of the present devices in mind we will investigate new approaches to minimize the hot-electron effects for low-voltage devices and to improve the breakdown voltages of high-voltage devices.

State of the Art

High-field transport is manifested in these "hot-electron" currents: the drain current, I_d; the substrate current (due to impact ionizations), I_{sub}; the gate current (due to channel hot-electron injection); and a less known current, I_{coll}. The substrate current, I_{sub} degrades circuit performance through substrate potential bouncing and can cause transistor snap-back and latch-up of CMOS circuits. The gate current, I_g, has been linked to oxide charge trapping and surface states generation which leads to V_T drift and reduction of drain current. For floating gate EPROMs, the gate current is the means for programming. I_{coll} is the leakage current through the drain of a nearby transistor or a nearby diode due to the collection from the substrate of minority carriers, whose origin was not understood until recently. This leakage current degrades the refresh time of DRAM and can upset logic circuits or static RAM in severe cases. To ensure the proper performance and reliability of scaled MOS ICs by minimizing these hot-electron currents (or adjusting I_g for EPROM programming) it is necessary to characterize them as functions of device geometry and technology (L_{eff}, W, X_{ox}, X_j, N_{sub}) and bias voltages (V_d, V_g, V_{sub}). The two prevalent approaches to solving this problem have been numerical simulations and experimental characterization. There is a glaring lack of effort to improve the basic understanding of these high-field transport phenomena.

Our research group has carried out a fruitful study of hot-electron effects and device breakdown models. The first major task of our research was the development of an accurate predictive theory for the electric field strength near the drain of the MOSFET under current-saturation conditions. At the outset of the work, any multidimensional field mapping approaches were ruled out as impractical for design procedures. A remarkably accurate method to account for two-dimensional effects on the electric field in the pinched-off region was proven experimentally in the work in our group by P.K. Ko (1). This theory provides the requisite accurate model for the channel electric field. Once the channel electric field is accurately known, the substrate current can be calculated using well-known expressions. The channel hot-electron emission (gate current) can be calculated using our lucky electron model (2). We have shown that I_{coll} (the substrate minority-carrier current) results from photogeneration of carriers (3,4). The light flux is generated by bremstralung in the high-field region of the channel and can be calculated with a simple theory (5). Recently, we have photographed the light emission from operating MOSFETs and used this technique to study the uniformity of the electric field along the width of the MOSFET channel (6). Thus we have conclusively disproved the old explanation of I_{coll} being a result of secondary impact ionization.

Since I_g, I_{sub}, and I_{coll} have the $e^{-A/E}$, $e^{-B/E}$ and $e^{-C/E}$ dependences respectively on the peak channel field E with A,B,C, being constants. The three currents have simple power law relationships among them (7,8). We also derived and experimentally proved a linear relationship between I_{sub} and (I_d - I_{dsat}) (9). These interrelationships or correlations among the hot-electron currents are of course independent of and without the need for any electric-field models. The most useful ones are those correlating a small current to a larger current, e.g., I_g to I_{sub} (7), correlating an unfamiliar current to a more familiar one, e.g., I_{coll} to I_{sub} (4) and I_{sub} to I_d (9). The I_g - I_{sub} correlation was recently proven in a 0.14 μm device (10).

We further applied these field and hot electron models to the study of MOSFET breakdown. A model of the parasitic bipolar transistor snap-back breakdown has been published (11). The I-V characteristics near and in the breakdown regime can be understood easily (9,12). Finally, a simple punchthrough model has been derived (13).

The key to both minimizing all the hot-electron effects and improving device breakdown is obviously to reduce the peak channel field. Several structures have been proposed to achieve this goal (14-16). They include the lightly-doped (or offset) drain, a return to the phosphorus-doped drain, an arsenic-plus-phosphorus drain (graded drain), and buried channel. Experimental proof of improvements and limited simulations have been published. However, there have been no simple quantitative models for these new structures, nor design guidelines, or comparative studies of trade-offs such that one can select and design the optimum structure.

Adequate breakdown voltages are of course more difficult to achieve for devices intended to operate at higher voltages. Conventional MOSFETs' breakdown voltages are around 20V or less. Many applications require devices with much higher breakdown voltages, for example 200V. Preferably, these devices are made with the simple planar MOS process so that they can be integrated with low-voltage logic circuitry. Applications include on-chip drivers for displays, servo-mechanisms, and use in telecommunication equipment.

There is a large number of very different device structures for high voltage transistors (17,18). Some use dielectric isolation, others use junction isolation. Some employ epitaxial substrates, some employ silicon-on-sapphire substrates, others employ bulk substrates. In addition, the methods of improving the drain breakdown voltage include deep drain-diffusion, field plate, guard-ring, ion-implantation, and combinations thereof. The very existence of such numerous and varied structures proves that the physics, trade-offs and potentials of these structures are not understood.

All high-voltage MOSFETs share a common drawback. A long, high-resistance region must be present between the source and the drain, thus increasing the channel resistance and reducing the current-carrying capability (limited by heat dissipation or by voltage drop) of the devices. In fact, we have shown that the on-state resistance increases as the cube of the breakdown (19,20). This severely limits the density as well as the applications of high-voltage IC's.

Proposed Research

1. Modeling the hot electron currents

We propose to continue our fruitful study of the hot-electron effects and models. We want to extend the gate current model and the I_g - I_{sub} correlation to the region where $V_d > V_g$. We would like to investigate the field uniformity in

the channel under various bias conditions and for several isolation technologies and transistor widths by photographing the light emission from the channel (6).

The physical mechanism of the light emission itself will be studied. Our hypothesis at the present time is bremstralung radiation. The threshold energy for an electron to cause an impact ionization in the inversion channel will be determined. Our preliminary data show that it is smaller than the threshold energy for bulk impact ionization.

2. Device degradation and breakdown

Our hot-electron study has modeled I_g as the indicator for the hot-electron susceptibility of the device but stopped short of studying the device degradations due to hot electrons. We propose to close this gap and study the device degradations experimentally and theoretically. Two areas will require special attention: 1) how localized (near drain) hot-electron emissions affect the terminal characteristics of the MOSFET, and 2) the possibility that when $V_d > V_g$, many more hot electrons reach the Si/SiO_2 interface (and cause charge trapping there) than the gate (and show up as gate current).

3. Improved device structures

Several structures have been proposed to combat the hot-electron effects and to improve the breakdown voltage (14-16). They all suppress the hot-electron creations and improve the breakdown voltages by reducing the *peak* channel field (at the drain). There have been no models for these new structures nor design guidelines, nor comparative studies of trade-offs such that one can select and design the optimum structure.

We propose to develop simple quantitative models for the peak electric fields in these improved structures by extending our existing field model (1). This will be done with the aid of experiments and simulations. Several other quantities are also of interest in the trade-off considerations. The loss in device conductance, the impact of deeper or graded junctions on dV_t/dL and punchthrough can be analyzed with existing theories with minor changes. We will validate the theories with extensive experimental studies. This study will not only help identify the best structure, but also, perhaps more importantly, guide the optimization of a structure once it is chosen. With the improved structures, the scaling of devices can be carried further than thought possible before. We will identify the new limits.

4. High-voltage MOSFET structures

In order to model and understand the large number of structures mentioned in the State of the Art section, we propose to develop simple field models for each of the building blocks that are the bases of all the different structures. For example, one such common building block is a field plate overlapping the edge of a planar junction. One approximate solution that we have derived for the electric field is

$$E(x) = 1.15E_0(x_1)e^{-0.36(x_1 - x)t_{ox}} \qquad x < x_1$$

$$= E_0(x) + 0.15E_0(x_1)e^{-0.06(x - x_1)t_{ox}} \qquad x > x_1$$

where $E_0(x)$ is the simple cylindrical-junction solution, x_1 is the location of the end of the field plate and t_{ox} is the oxide thickness. All of the constants are theoretically derived. This simple model has been verified with 2-D device simulations.

Once these building-block models are perfected, one need only to optimize quantities such as t_{ox}, x_1, etc. so that the peak field does not exceed a critical field for breakdown.

References

(1) P. K. Ko, R. S. Muller and C. Hu, "Aunified Model for Hot-Electron Currents in MOSFETs," *Tech. Digest, 1981 Int. Electr. Devices Meeting*, 600-601, Washington, DC (December 1981).

(2) C. Hu, "Lucky Electron Model of Channel Hot-Electron Emission," *Tech. Digest, 1979 Int. Electr. Devices Meeting*, 26-30, Washington, DC (December 1979).

(3) S. Tam, P. K. Ko, F. C. Hsu, C. Hu and R. S. Muller, "Hot-Electron Induced Excess Carriers in n-Channel MOSFETs," IEEE Solid-State Device Research Conference, Fort Collins, Co. (June 1982).

(4) S. Tam, F. C. Hsu, P. Ko, C. Hu and R. S. Muller, "Hot-Electron Induced Excess Carriers in MOSFETs, *IEEE Electron Devices Letters*, 376 (December 1982).

(5) S. Tam and C. Hu, to be published.

(6) S. Tam, P. Ko and C. Hu, "Light Emission and Field Uniformity in MOSFETs," submitted to *IEEE Electron Devices Letters*.

(7) S. Tam, P. Ko, C. Hu and R. S. Muller, "Correlation Between Substrate and Gate Currents in MOSFETs," *IEEE Trans. Electron Devices*, 1740-1744 (November 1982).

(8) C. Hu, S. Tam. F. C. Hsu, R. S. Muller and P. Ko, "Correlating the Channel, Substrate, Gate, and Minority-Carrier Currents in MOSFETs," 1983 IEEE ISSCC, 88-89 (February 1983).

(9) F. C.Hsu, R. S. Muller and C.Hu, "Characteristics of Short-Channel MOSFETs in the Breakdown Regime," *Digest of 1983 IEDM*, 282-285 (December 1982).

(10) S. Tam, F. C. Hsu, C. Hu, R. S. Muller and P. Ko, "Hot-Electron Currents in Very Short Channel MOSFETs," to appear in *IEEE Electron Devices Letters*, (July 1983).

(11) F. C. Hsu, P. K. Ko, S. Tam, C. Hu and R. S. Muller, "An Analytical Breakdown Model for Short-Channel MOSFETs," *IEEE Trans. Electron Devices*, 1735-1739 (November 1982).

(12) F. C. Hsu, R. S. Muller and C.Hu, "A Simplified Model of MOSFETs in the Breakdown Regime," to appear in *IEEE Trans. Electron Devices (June 1983)*.

(13) F. C. Hsu, R. S. Muller and C. Hu, "A Model of MOSFET Punchthrough Voltage," accepted by *IEEE Trans. Electron Devices*.

(14) P. J. Tsang, et al., *IEEE Trans. Electron Devices*, 590 (April 1982).

(15) H. Sunami, et al., *IEEE Trans. Electron Devices*, 601 (April 1982).

(16) E. Takeda, et al., *IEEE Trans. Electron Devices*, 611 (April 1982).

(17) B. J. Baliga, in *Silicon Integrated Circuits, Part B*, edited by Dawan Kahng, Academic Press (1981).

(18) S. Ochi, et al., *IEEE Trans. Electron Devices*, 399 (February 1980).

(19) C. Hu, "Optimum Doping Profile for Minimum Ohmic Resistance and High-Breakdown Voltage," *IEEE Trans. Electron Devices*, ED-26, 243-244 (March 1979)

(20) C. Hu and Y. Chen, "Optimum Doping Profile of Power MOSFET Epitaxial Layer," *IEEE Trans. Electron Devices*, EQ-29, 9860987 (June 1982).

(21) J. P. Russell, et al., to be published.

(22) B. J. Baliga, et al., *Digest of 19872 IEDM*, 264 (1982).

University of California — Electronics Research Laboratory

Joint Services Electronics Program — August 15, 1983

IV. Basic Research in Information Systems — Coordinator: C. A. Desoer

General

The integrated circuits revolution drives forward practically all sub areas of what used to be called "systems." The tremendous progress in computer hardware and software has created the need for better algorithms for a) simulation to study linear and nonlinear circuits, layout of chips, and behavior of control systems and of distributed control systems; and for b) optimization in order to achieve optimal designs. It has also created the need for better models to achieve more accurate and less expensive simulation, and also create better understanding of nonlinear circuit and system behavior, such understanding being a first step towards inventing more rational design methodologies. Finally the progress in communications and microprocessor has stimulated interestin distributed control: here the problem is to invent local control strategies and coordinate them in order to achieve overall system objectives.

The first topic includes a) general study of piecewise-linear circuit models and a study of dynamics of nonlinear circuits; b) study of the layout problem, in particular, the general placement problem, the global wiring problem and the detailed routing problem.

The second topic includes a) the robustness of the design of several configurations of linear and nonlinear control systems; b) the development of robust adaptive control strategies and c) the computer aided design of control systems subject to semi-infinite time- and frequency-domain inequality constraints.

The third topic concentrates on the computer-aided design of integrated ciruits with a) formulation of the optimization problem towards yield maximization; b) improved simulation algorithms of integrated circuits; c) improved device models to reflect process technology.

The fourth topic of control in distributed systems includes a) a study of the superprocess where, in addition, the user must select a control action which affects both his reward and his transition probability, b) a study of more realistic models where more than one resource is involved.

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: ISS-84-1 **Last Year's No.(s):** ISS-83-1 (in part)

Title: Large-Scale and Nonlinear Circuits Study

Senior Principal Investigator(s): L. O. Chua (415) 642-3209
E. S. Kuh 642-2689

Scientific Objective

Our objective is to continue our research efforts on *large scale* and *nonlinear circuits* which were initiated several years ago. The many tools and results that we have developed so far continue to serve as a foundation for our future research and will be used to attack several interrelated fundamental problems in this relatively unexplored but important area.

State of the Art

Network theory played a major role from the early 40's to the 60's in the development of the present day communication systems. The main thrust of network theory then was directed at the analysis and synthesis of linear circuits which can be characterized by a relatively small number of differential equations. Although in recent years many authors have published papers on nonlinear circuits and large-scale networks, the extent of the development of large-scale nonlinear circuits, both in theory and applications, is nowhere near the kind of maturity in classical network theory. The advances during the past decade in electronic devices and integrated circuits, coupled with the immense impact of computers on circuit analysis and design, have drastically changed the nature of the problems faced by circuit theorists. While analysis of circuits is still the key problem, it is more difficult in view of the size and complexity of the circuit and the inherent nonlinearity which exists in most electronic devices. Furthermore, the scope and significance of "circuit analysis" has been much broadened. Theory and techniques developed from large-scale networks and nonlinear circuit analysis can often be used in other types of large-scale network and system problems; for example, computer networks, power networks and complex control systems.

It should be noted that because of the nonlinearity, size and complexity of LSI and VLSI, the objectives and approaches in analysis are considerably different from those of the classical network theory. First, computation becomes a key element in the study of any nonlinear large circuit or system. The development of efficient algorithms is crucial. While theoretical results are essential, often one must also depend on heuristics. Second, the study of the structure of a large circuit and the property of interconnection is important. Frequently, large problems need to be divided into smaller sub-problems in order to facilitate analysis, data storage and computation. Third, design is usually accomplished by experience as a first step and improved on by repeated analysis. Fourth, such problems as reliability study, tolerance analysis, diagnosis and testing are important and should be kept in mind in the overall design process. The last item constitutes a new area of research which was not a part of classical network theory. All these indicate that there exist a large variety of problems of a circuit-theoretic nature which need to be studied.

Progress and Publications Since Last Major Proposal

Research on large-scale and nonlinear circuits during the period 1981-1983 has focused on the following three topics:

(1) Piecewise-linear analysis of general nonlinear networks.

(2) Qualitative analysis of nonlinear communications circuits.

(3) Circuit layout and routing.

Significant progress has been achieved in these areas and documented in several professional journals. The following is a brief summary of these papers.

(1) L. O. Chua and Y. S. Tang,, "Nonlinear oscillation via Volterra series," *IEEE Trans. on Circuits and Systems*, CAS-29, 150-168 (March 1982).

Summary. Using a novel approach, the amplitude and frequency of nearly sinusoidal nonlinear oscillators can be calculated by solving two algebraic nonlinear equations. These determining equations can be generated to within any desired accuracy using a recursive algorithm based on Volterra series.

Our method inherits many desirable features of the harmonic balance method, the describing function method, and the averaging method. Our technique is analogous to, but is much simpler than, the classic approach due to Krylov, Bogoliubov, and Mitropolsky. Unlike conventional techniques, however, our approach imposes no severe restriction on either the degree of nonlinearity, or the amplitude of oscillation. Moreover, the accuracy of the solution can be determined by a constructive algorithm.

(2) * P. J. Moylan, L. O. Chua and E. W. Szeto, "When is a device passive?" *International J. On Circuit Theory and Applications*, 10, 151-165 (April 1982)

Summary. *Passivity* is perhaps the most basic concept in circuit th[eory]. Unfortunately, the existing definitions of passivity are too restrictive [and] often contradict one another. In this paper, a new passivity definiti[on] is proposed which is applicable to *all* n-port and (n+1)-terminal devices -- including *time-varying*, *nonlinear* and *distributed* circuit elements. This definition generalizes and reconciles several recent conflicting definitions.

(3) * A. Bergen, L. O. Chua, A. Mees and E. Szeto, "Error bounds for general describing function problems," *IEEE trans. on Circuits and Systems*, CAS-29, 345-354 (June 1982).

Summary. The describing function method is widely used without much attention being paid to the error analysis so vital in any approximate method. One reason for this is the lack of a straightforward, user-oriented method for checking error bounds except when the nonlinear element characteristic is single-valued and of bounded slope. This paper attempts to eliminate that defect. A far wider range of nonlinear elements is now amenable to straightforward, usually graphical treatment; discontinuities, hysteresis and backlash characteristics are included. In addition, previous results for slope-bounded single-valued nonlinear characteristics may be substantially improved with a small additional computational effort.

(4) * Leon O. Chua and Robin L. P. Ying, "Finding all solutions of piecewise-linear equations," *International J. on Circuit Theory and Applications*, 10, 201-229 (1982).

Summary. A new algorithm is given for solving the d.c. piecewise-linear equations of nonlinear electronic circuits. The device models are assumed, with little loss of generality, to be made of 2-terminal piecewise-linear resistors and linear controlled sources. Unlike other methods, this algorithm guarantees that *all* solutions will be found in a finite number of steps. The method depends crucially on a recent development which allows a multi-dimensional piecewise-linear function to be represented in a closed canonical form. This highly compact representation requires only a minimum amount of computer storage and is responsible for the efficiency

---

*Under JSEP support.

of the algorithm.

(5) L. O. Chua, M. Hasler, J. Neirynck and Ph. Verburgh, "Dynamics of a piecewise-linear resonant circuit," *IEEE Trans. on Circuits and Systems*, CAS-29, 535-547 (August 1982).

Summary. The qualitative nature of the time evolution in a piecewise-linear lossy resonant circuit driven by a sinusoidal voltage source is investigated by computer-aided analysis using exact analytical formulas. A surprising wealth of different nonlinear phenomena is discovered. They are: stable and unstable harmonics, subharmonics, and even apparently completely disordered aperiodic "chaotic" motions. In the latter case, the hyperbolicity, strange attractor, and broadband frequency spectrum normally associated with chaotic motions have all been observed using nearly exact piecewise-linear solutions. These results represent the most reliable numerical confirmation to date of chaotic motions in a *real physical circuit*.

(6) * L. O. Chua and G. N. Lin, "The (p+q)-port transformer," *International J. of Circuit Theory and Applications*, 10, 335-339 (October 1982).

Summary. Two approaches for realizing a *(p+q)-port transformer* using operational amplifiers are presented. Unlike iron-core transformers, our realization is valid from d.c. to a relatively high frequency limited only by the op amp's frequency response. The stability and limitation of the two approaches are analyzed and compared. Examples are given to illustrate two unique and indispensable applications of the (p+q)-port transformer: *synthesis of nonlinear n-ports and nonlinear programming*.

(7) Y. S. Tang, A. I. Mees and L. O. Chua, "Hopf bifurcation via Volterra series," *IEEE Trans. on Automatic Control*, (January 1983).

Summary. The Hopf bifurcation theorem gives a method of predicting oscillations which appear in a nonlinear system when a parameter is varied. There are many different ways of proving the theorem and of using its results but the way which is probably the most useful to control and system theorists uses Nyquist loci in much the same way as the describing function method does. The main advantages of this method are dimensionality reduction, which eases the calculation and the ability to cope with higher order approximations than are used in the original Hopf theorem. This paper shows how such an approach to the Hopf bifurcation follows naturally and easily from Volterra series methods. Such use of Volterra series in nonlinear oscillations appears to be new. In many problems, the calculations involved are simplified when the Volterra series approach is taken, so the approach has practical merits as well as theoretical ones.

(8) * L. O. Chua and R. Ying, "Canonical piecewise-linear analysis," *IEEE Trans. on Circuits and Systems*, CAS-30, 3, 125-140 (March 1983).

Summary. Any continuous resistive nonlinear circuit can be approximated to any desired accuracy by a global piecewise-linear equation in the *canonical form*

$$\alpha + Bx + \sum_{i=1}^{n} c_i |\langle a_i, x\rangle - \beta_i| = 0.$$

---

*Under ISEP support.

All conventional circuit analysis methods (nodal, mesh, cut set, loop, hybrid, modified nodal, tableau) are shown to always yield an equation of this form, provided the only *nonlinear* elements are two-terminal resistors and controlled sources, each modeled by a one-dimensional piecewise-linear function.

The well-known Katzenelson algorithm when applied to this equation yields an efficient algorithm which requires only a minimal computer storage. In the important special case when the canonical equation has a lattice structure (which always occurs in the hybrid analysis), the algorithm is further refined to achieve a dramatic reduction in computation time.

(9) * M. Odyniec and L. O. Chua, "Josephson-junction circuit analysis via integral manifolds," *IEEE Trans. on Circuits and Systems*, CAS-30, 308-320 (May 1983).

Summary. Using a second-order circuit model the complex dynamical behavior of a typical Josephson-junction circuit is rigorously analyzed using integral manifolds. The key idea is to prove that under certain small-parameter assumptions, the nonautonomous circuit has a stable integral manifold. Moreover, this manifold is doubly periodic so that steady-state behavior of the Josephson-junction circuit reduces to the analysis of its dynamics on a torus. Well-known experimental phenomena, such as the existence of hysteresis in the dc Josephson circuit and voltage steps in the ac Josephson circuit, are rigorously derived and explained.

(10) * M. Marek-Sadowska and E. S. Kuh, "A new approach to routing of two-layer printed circuit board," *International J. on Circuit Theory and Applications*, 9, 331-341 (1981).

Summary. This paper presents a new method for routing two-layer printed circuit boards with fixed geometry, i.e. alternate columns of pins and vias. Circuit components are mounted on top of the board, and conductor wires are to be laid on the board such that circuit connections can be properly made. The proposed approach gives 100 per cent routability. The method consists of three steps, namely: partitioning of multi-pin nets into 2-pin subnets, via assignment, and routing on the two layers. In comparison with the traditional undirectional routing, the method offers more flexibility and it requires usually about half as many vias. A computer program based on the presented algorithms was written. Its implementation is presented along with testing examples.

(11) * M. Marek-Sadowska and E. S. Kuh, "General channel routing algorithm," *IEE Proc.*, 130, Pt. G, 3, 83-88 (June 1983).

Summary. A new approach to the 2-layer channel-routing problem is introduced. The method allows horizontal and vertical connections on both layers. An order graph similar to the traditional vertical constraint graph is used in the algorithm. The main advantage is that the method is general and is immune to cyclic constraints. Furthermore, the channel width does not have a lower bound equal to the maximum density.

---

*Under JSEP support.

(12) * C. P. Hsu, "General river routing algorithm," *Proc. 20th Design Automation Conf.*, 578-583 (1983).

Summary. A general and practical river routing algorithm is described. It is assumed that there is one layer for routing and terminals are on the boundaries of an arbitrarily shaped rectilinear routing region. All nets are two-terminal nets with pre-assigned (may be different) widths and no crossover between nets is allowed. The minimum separation between the edges of the two adjacent wires is input as the design rule. This algorithm assumes no grid on the plane and will always generate a solution if a solution exists. The number of corners is reduced by flipping of corners. An analysis to determine the minimum space required for a strait-type river routing problem is included.

Let B be the number of boundary segments and T be the total number of terminals. The time complexity is $O(T(B+T)^2)$ and the storage required is $O((B+T)^2)$. This algorithm is implemented as part of the design station under development at the University of California, Berkeley.

(13) * N. P. Chen, C. P. Hsu and E. S. Kuh, "The Berkeley building-block layout system for VLSI design," to appear *Proc. VLSI 1983*, Trondheim, Norway.

Summary. Automatic layout design of custom VLSI circuits depends on the building-block hierarchical approach in which macrocells of arbitrary shapes and sizes are given together with the net list. Our aim is to design an intelligent and practical automatic layout system which will interface with other design aids at Berkeley. The BBL system has a general purpose database, a smart global router which can dynamically adjust placement and efficient detailed routers, namely: the channel router and the switch-box router. The System incorporates several novel ideas and is based on a number of graph-theoretical algorithms. Experimental results indicate that the System is extremely effective.

(14) * C. K. Cheng and E. S. Kuh, "Partitioning and placement based on network optimization," to appear *Proc. ICCAD (1983)*.

Summary. A new constructive placement and partitioning method based on resistive network optimization has been developed. It allows fixed modules in the formulation, takes advantage of net-list sparsity and has a complexity of $O[n^{1.4}\log n]$.

(15) * M. Marek-Sadowska and J. T. Li, "Global router for gate array," to appear *Proc. ICCAD (1983)*.

Summary. The global routing problem in gate array layout design is analyzed. A new routing method which identifies unique connection patterns and routes other nets along certain meshes is developed with several advantages over the conventional approach.

(16) * C. P. Hsu, "Minimum-via two-layer two-dimensional routing," to appear *Proc. ICCAD (1983)*.

Summary. Based on a circle graph representation and related graph theoretical algorithms, a new approach to the two-layer two-dimensional routing problem is proposed. It considers both routing problem and via-minimization problem at the same time from a global point of view.

---

*Under JSEP support.

(17) * N. P. Chen, C. P. Hsu, E. S. Kuh, C. C. Chen and M. Takahashi, "BBL: A building-block layout system for custom chip design," to appear *Proc. ICCAD (1983)*.

Summary. BBL is an automatic layout system for placing and interconnecting macrocells of rectilinear shape and arbitrary sizes. The System includes a number of distinct features and has resulted in excellent layout design of custom chips.

This paper describes the Berkeley Building-Block Layout for automatic design of custom chips based on a hierarchical approach. The macrocells (blocks) are allowed to be of arbitrary rectilinear shape and sizes. Our ultimate aim is to design an intelligent and practical automatic layout system which will interface with other design aids at Berkeley.

Significant Accomplishments

The major results have been described in the preceding summaries.

Proposed Research Program

Research on the following topics is proposed for the next three years:

1. Canonical piecewise-linear circuit theory

One of the most significant discoveries we have made in our research during the last three years on piecewise-linear analysis is the following theorem:

Any continuous piecewise-linear function from $R^n \to R^1$ with a nondegenerate *linear partition* can be represented globally by the following canonical form:

$$f(x) = a + \langle b, x \rangle + \sum_{i=1}^{p} c_i \, | \langle a_i, x - \beta_i | \rangle$$

where x, b, a_i, i=1,2,...,p are vectors in R^n and <,> denotes the vector dot product. The significance of the above ***piecewise-linear equation*** is that it is a *global* analytical representation. Moreover, the only nonlinearities are ***absolute-value*** functions. This compact representation is far superior to the *conventional* piecewise-linear approach where a linear equation must be specified and stored in the computer *for each* region, along with its boundary. The enormous amount of data needed to be stored is in fact one of the most objectionable features of conventional piecewise-linear analysis. This objection which is particularly serious when the nonliner elements are n-dimensional (n > 2), is now overcome by resorting to our piecewise-linear equation.

More recently, we have proved the following general result:

Theorem. Let N denote any circuit made of ***linear***, possibly coupled, resistive elements (e.g. linear controlled sources, transformers, gyrators, etc.) and 2-terminal ***nonlinear*** resistors. We assume that the nonlinear resistors are either voltage or current-controlled and are approximated by *continuous piecewise-linear* functions. Hence the class of circuits we allow can be depicted as an n-port *N* with the nonlinear resistors extracted across the ports. Note that since *N* may contain any type of linear controlled sources, and since most device circuit models are made simply of 2-terminal nonlinear resistors and controlled sources, most practical resistive circuits are allowed.

---

* Under JSEP support.

Similarly, any *dynamic* piecewise-linear circuit having a state representation can be recast into an equivalent piecewise-linear state equation of the following canonical form:

$$\dot{x} = \alpha + Bx + \sum_{i=1}^{p} C_i \, | <alpha_i, x> - \beta_i |$$

The above results suggest the possibility for developing a *unified piecewise-linear circuit theory*. It is remarkable that such a general theory would involve only a single nonlinearity, namely, the *absolute-value function*.

So far, we have developed several efficient computational algorithms for solving these equations for *resistive* circuits. We propose to continue this research for solving *dynamic* piecewise-linear circuits.

From the *circuit-theoretic* point of view, we propose to attack the following basic problem:

Derive the *necessary* and *sufficient* conditions in terms of the coefficients a, B, C_i, α_i, and β_i in the above *canonical piecewise-linear state equation* so that the dynamic circuit has one of the following properties: (a) reciprocal, (b) passive, (c) locally passive, and (d) lossless. Necessary and sufficient conditions for *each* of these properties are known to be extremely difficult to derive for $n \geq 2$. Our initial research will therefore be restricted to *2nd* order dynamic piecewise-linear circuits.

2. Piecewise-linear synthesis

Since most resistive and dynamic nonlinear circuits can be modelled by a *canonical piecewise-linear* algebraic or state equation, it makes sense to develop *synthesis* techniques in terms of these equations. This problem is relevant to both *device modelling* and *nonlinear circuit design*.

In *device modelling*, we usually end up with a *nonlinear* state equation which can be *approximated* in canonical piecewise-linear form. The final task consists of synthesizing a circuit having this prescribed state equation. In this particular application, the circuit elements will be restricted to linear and piecewise-linear 2-terminal resistors, inductors, capacitors and controlled sources, since these are the elements that a general circuit simulator can be easily developed to handle.

In *nonlinear circuit design*, however, it is important to use only circuit elements that are commercially available. Hence, we will restrict our building blocks to linear resistors, inductors, capacitors, operational amplifiers, pn junction diodes, zener diodes, and 2-terminal *piecewise-linear* resistors. Only the last building block is not available as an off-the-shelf component. However, we have demonstrated that any prescribed *piecewise-linear* voltage-controlled or current-controlled v-i curve can be realized with *high precision* using only pn-junction diodes, operational amplifiers, in addition to the usual dc power supply.

One motivation in this research is to allow us to *optimize* the performance of dynamic nonlinear circuits. The performance to be optimized may include *minimising the nonlinear distortion*, *increasing the switching speed*, etc. For example, in many practical weakly linear feedback systems, it is possible to design a dynamic "nonlinear compensating circuit" to cancel out the nonlinearity. This linearization approach is necessary in systems with *delays* or *non-minimum phase* linear parts where stability constraints preclude the application of strong linear negative feedback. The dynamic nonlinear compensating circuit could be specified in terms of a canonical piecewise-linear state

equation, which in turn can be built using the synthesis technique to be developed in this research.

3. Nonlinear dynamics on integral manifolds

Josephson junction devices are used in many applications ranging from super-sensitive detectors to superfast computers. This remarkable 2-terminal device is imbued with extremely rich dynamics and displays a wide variety of exotic nonlinear phenomena. For example, when driven with dc current source, the device is found to oscillate at extremely high frequencies (GHz range). If we plot the *average value* V_{dc} of the high frequency voltage versus the dc current I_{dc}, the V_{dc} - I_{dc} characteristic is found to be hysteretic (double-valued). If we connect a sinusoidal current source in parallel with the dc current source and repeat the experiment, the resulting V_{dc} - I_{dc} characteristic changes dramatically. Here discontinuous *voltage steps* of varying width are observed at *rational number* multiples of some natural frequency. This puzzling voltage-step phenomenon had been given various intuitive and physical examinations. A rigorous explanation using a *first-order* circuit model has been given in our earlier publication. Unfortunately, this first-order model is *over-idealized* because it fails to include the effect of junction capacitance C which is always present in non-negligible amounts in the real device.

A more realistic Josephson junction circuit model leads to a *non-autonomous 2nd* order differential equation

$$C\frac{d^2\varphi}{dt^2} + \frac{1}{R}\frac{d\varphi}{dt} + I_o \sin\left(\frac{4\pi e}{h}\right)\varphi = I_{dc} + I_{ac} \sin \omega t$$

This equation can be transformed into the following dimensionless form:

$$\beta\ddot{x} + \dot{x} + \sin x = \alpha + \varepsilon \sin \omega\tau$$

This equation is also of practical interest in several unrelated areas. For example, phase-lock loop in communication systems, swing equation in power systems, pendulum with constant torque and viscous damping, synchronous motor, rotating disc, etc. are all described by the same equation.

We have been studying the dynamics associated with this equation since 1981. In spite of the simplicity of this equation, we have not completely understood its exceedingly rich and complicated dynamics -- especially when the parameter β is large.

Using the *method of integral manifolds*, we were able to prove that under certain small-parameter assumptions, solutions of the above equation are attracted to a doubly-periodic 2-dimensional surface. This surface is called an *integral manifold* because any trajectory originating from this surface must remain there forever. By identifying appropriate periodic boundaries, this surface can be represented by a *torus*. Consequently the steady state behavior of the 2nd order Josephson junction model can be derived by studying the corresponding motion on this torus. This important observation reduces a nonautonomous *second-order* differential equation on the plane to an equivalent nonautonomous *first-order* differential equation on the torus. Consequently the same tools we have used so successfully (which are applicable only for first-order differential equations) can now be used to analyze the complex *nonlinear dynamics* of the Josephson junction.

Using the integral manifolds as a tool, we were able to prove and explain a number of experimentally observed phenomena which have so far defied a rigorous analysis. For example, we have proved that when the excitation amplitude ε is small, some of the periodic solutions become "more stable" than

others. This phenomenon causes a drastic change in the average V-I characteristic of the device: namely, it changes from a *continuous* curve (in the autonomous case) to a "discontinuous" *step-wise* characteristic. We have also proved that if a periodic steady state solution remains stable then its period must be commensurate with that of excitation (i.e. every stable solution must be a subharmonic solution, although some subharmonic solutions may be unstable). It is possible to explain geometrically (in terms of the Poincaire map for torus) why subharmonic solutions behave in this manner and why some of them are "more stable" than others, as demonstrated by steps of unequal length in the measured average V-I characteristic.

We are convinced that the *method of integral manifolds* will become increasingly important in the study of *high-dimensional* nonlinear systems. We propose therefore to continue our investigation of the Josephson equation for large values of ε and β, using some appropriately chosen integral manifolds. We also propose to generalize the results we have obtained so far to the following more general system:

$$\dot{x} = y$$

$$\dot{y} = \alpha + f(x) + g(x)y + \beta h(\omega t)$$

where $f(x) = f(x+2\pi)$, $f(x) = -f(x)$, $g(x) = g(-x)$, and $h(t+\tau) = h(t)$. This equation represents an even more realistic model of the Josephson junction, as well as other physical systems. We believe that by some clever transformation and tricks, most, if not all, of the general properties that we have derived so far will remain valid for this equation.

4. Layout theory and algorithms

We propose to continue to investigate difficult problems in the field of custom chip layout. Emphasis will be placed on theoretical study and the development of efficient algorithms. The three specific areas are listed below:

(a) General Placement

The problem of module placement is central to automatic layout. A good placement is essential to a good layout design. The problem of general placement is like the bin packing problem, i.e., to place the modules of arbitrary rectangles into a minimum size rectangle with certain constraints. In addition, we must also consider the connectivity specification on modules and allow for space needed for wire interconnection. Thus a preamble to general placement is chip planning, i.e., to estimate the wiring space required. One possible approach for placement is to use the method of dissection of a square into rectangular modules. Another approach is to ignore the differences of module shape and size, and to consider only the information on connectivity. For the latter, existing methods include those based on a force directed placement procedure, minimization of a quadratic form, and iterative pair-wise exchanges. We believe that an innovative combination of various procedures will lead to a good solution to the general placement problem.

The special placement problem for gate-array design is also being studied. It deals with partitioning and placement of "point" modules on rectangular grids from a given net list and the boundary pad connectivity information. The problem can be formulated in terms of resistive network analog with specified voltage sources. The corresponding objective function based on connectivity and wire length for optimum placement is then the power dissipation in the resistive network. It can be shown that the objective function is $w = v^T Yv$ where v represents the node potential vector and Y the indefinite admittance matrix.

We propose to attack the problem using this approach, thus taking advantage of highly efficient circuit simulation programs based on sparse-matrix algorithms.

(b) Global Wiring

After placement is done, pins on different modules most be connected according to a net list specification. The global wiring problem represents the first of two steps in making the interconnections. The problem is similar to the multi-commodity flow problem in operations research. We have formulated an approach to the building-block layout problem by using the concept of "bottleneck." A graph representation of the bottlenecks can be introduced once the placement of modules is given. Nets must be assigned to streets in an optimal way to facilitate detailed routing, i.e., putting nets to specific tracks on streets. The problem is to find a minimum-distance tree which connects pins on different modules. Yet we must also consider the congestion of streets as nets are being assigned to streets. The problem can be stated in terms of a Steiner tree on graph with its edges appropriately weighted according to congestion and street length. The Steiner tree problem is NP complete. We have, however, developed a highly efficient heuristic algorithm based on a "3-point" method. The building-block routing system based on the above is being developed.

In the case of gate-array design the global routing problem is somewhat different because modules are fixed in location and are of uniform size. Thus streets or channels are fixed and regular, and the main constraint for global wiring is the channel capacity. Although a similar Steiner tree strategy can be used, we wish to attack the problem at a more fundamental level.

Let us assume that the whole chip is divided into a rectangular array of cells, each contains wiring grid lines and circuit pins. For global wiring, the interconnections and exact pin locations within each cell are ignored. The routing problem is to determine, for each net, a path of cells for which the net will pass through. Our goal is to route all the nets in such a way that the number of nets crossing the boundary of two adjacent cells does not exceed the available grid line (cross supply).

We are interested in obtaining theoretical results of this general problem on routability, i.e., if a solution exists, what is the nature of the routing path? If we make assumptions on the shape of the routing path, e.g., allowing a maximum of only one horizontal and one vertical connection for each routing path, is the problem NP complete? The general problem is most likely NP complete. However, we need to develop an efficient heuristic routing algorithm. Some obvious items which need to be considered are the number of pins within a cell, the pins pertaining to a given net, the total cross-supply of a cell, the regions which are defined by non-pass-through cells, and optimal connections to be made between neighboring regions, etc.

The global wiring problem for gate-array so formulated can hopefully answer such questions: If a solution to a difficult wiring problem exists, are there nets or portions of the connections that must be routed in a unique way? Can we say anything about the existence of solutions or, at least, distinct properties of solutions?

(c) Detailed Routing

The second step of the interconnection problem is detailed routing. In detailed routing each net is routed precisely on the available layers (usually 2) to complete all necessary interconnections. The channel routing algorithm mentioned earlier works quite well. A problem which occurs frequently is the

completion of 2-layer routing at an intersection of channels, i.e., a rectangular space with points to be connected on all four sides, called the switch-box or 2-dimensional routing problem. It appears that there exist fundamental limitations on the number of nets and terminals to be connected in relation to the space available. It is conceivable that the interval graph approach for one-dimensional routing could be extended to the two-dimensional case.

There are other problems in detailed routing which are important. Automatic routing programs may lead to less than 100 per cent completion. It is then necessary to complete the routing interactively. This calls for deletion of certain nets for rerouting. The problem can be formulated in terms of an n-path routing problem on a rectangular grid. At present there exist efficient 2-path routing algorithms. We propose to study the n-path problem and develop efficient interactive routing methods.

Another problem of interest is minimum-via routing. Vias which are used to connect layers should be kept to a minimum for many practical reasons. The problem of minimum-via routing can be divided into two sub-programs, namely: topological routing and geometric routing. The problem of topological routing is to determine a topological solution from the given net list, which has a minimum number of vias. If we map the topological solution onto a rectilinear plane, we have then the problem of geometrical routing. Geometric routing is to obtain a solution using as small an area as possible, which satisfies the design rules in terms of wire width and separation.

We have found that the problem of topological routing can be successfully attacked by means of a circle graph representation of the net intersection information. The minimum-via problem is then reduced to that of minimum-node deletion of a graph to obtain a bipartite subgraph. The method amounts to obtaining a global analysis directly from the given net list in contrast to the existing approaches of reducing vias from a given routing.

University of California, Berkeley | **Electronics Research Laboratory**

Joint Services Electronics Program | **August 15, 1983**

Work Unit No.: ISS-84-2 | **Last Year's No.(s):** ISS-83-2 (in part)

Title: Control in Distributed Systems

Senior Principal Investigator(s): P. Varaiya (415) 642-5270
J. Walrand 642-1529

Scientific Objective

Over the past decade, enormous attention has been devoted to the analysis and design of distributed systems. This attention has been informed by the disciplines of communication, control, and computer engineering. The disciplinary separation has led to differences in approach which can in part be explained by the different technologies that researchers are accepting as a basis, and in part by different methodological emphasis. In spite of this diversity, it is remarkable to observe a convergence of interest to the point where a few common generic problems have crystallized.

The commonality can be traced to the fact that a key issue in distributed systems is the management, on the basis of limited information, of scarce resources demanded by competing activities. In communication problems, for example, the scarce resource is bandwidth and the competing activities are users who wish to transmit messages. In a multi-programming environment an important aspect of the management problem is to allocate several devices (cpu, I/O equipment) among several processes.

In the special case of a single resource and several users the allocation problem can often be formulated as a so-called multi-armed bandit problem (see the bibliography and the references cited therein). We propose to extend the bandit model in two directions. First, we wish to study the case in which in addition to the "higher" level resource allocation decision, there is also, for each user, a "lower" level control variable which alters the dynamic behavior of each user. (In the standard bandit problem user dynamics are fixed.) Second, we wish to study the very important extension to the case where there is more than one resource. This case turns out to be considerably more difficult than the single-user case. The generalization is, however, very important since it immensely increases the applicability of the bandit model.

State of the Art

In the basic version of the multi-armed bandit problem there are N independent users and a single resource. Let $x_i(t)$ designate the state of the i^{th} user at time t. At each t one must assign the resource to one user. If user i has been selected, one gets an immediate reward $R(t) = R_i(x_i(t))$ and the user's state changes to $x_i(t+1)$ according to some **Markov** transition rule; the states of the remaining users remain frozen, $x_j(t+1) = x_j(t)$, $j \neq i$. The states of all users are observed and the decision problem is to assign the resource to users so as to maximize the present value of the reward sequence

$$E \sum_{t=1}^{\infty} \alpha^t R(t).$$

There is an extensive literature showing that the bandit problem and its variants can be used to model the decision problems in job scheduling, resource allocation, sequential random sampling, etc.

The bandit problem has received a great deal of attention since it was first formulated in the 1940s. The essential breakthrough came only in 1972 when Gittins and Jones (10) showed that to each user i is attached an index $\nu_i(x_i)$ which is a function only of its own state, and that the optimal policy is to assign the resource to the user with the largest current index. Call this the **index policy**.

This is a very important result since it decomposes the N-dimensional bandit problem into N one-dimensional problems.

Very recently, we have extended the index result to a much wider class of single resource problems by eliminating the condition of Markov dynamics (we allow the user process to be arbitrary), and by permitting partial observations (22). In addition, we have proposed new algorithms for computing the index. Finally, we have applied our results to propose a protocol for a local area network that minimizes the average delay (23).

The bandit problem serves as a versatile model for many resource allocation problems in distributed systems, and the index rule provides a conceptually and computationally attractive solution. The available theory has two limitations. First, it only applies to the case where there is a single resource. This is a major restriction since multiple resources are obviously very common. However, outside of some very special cases there is virtually no result for the multiple resource case. The main objective of this proposal is to treat this case. The second restriction of the theory is that it models users in a "passive" way. In the bandit model once a user is given the resource its state changes according to a fixed law, whereas if it does not have the resource its state is frozen. In many problems, however, the user can take several actions beyond having or not having a resource. To include this possibility the theory of the bandit problem needs to be extended considerably. We have made a promising advance in this direction via the concept of "superprocesses" introduced in (22).

Proposed Research Program

We will concentrate initially on two problems. First, we will study superprocesses. These are bandit problems with an additional degree of freedom: when a particular user is allocated a resource, the user must further select a "control action" that affects both the immediate reward and the user's state transition. A very important special case of superprocesses is the situation where new users arrive randomly. In communication networks, for example, these users represent new messages. In a multi-programming environment they represent new computing tasks. We will investigate this special case in much greater depth than has hitherto been possible.

Second, we will study the generalization of the bandit problem where there are two or more resources, otherwise the problem stays the same. This turns out to be considerably more difficult that the single resource case. The importance of this generalization cannot be overemphasized, and any significant result in this area will immediately have useful applications. We are hopeful of progress on this problem using the novel techniques of analysis introduced in (22).

References

(1) Glazebrook K.D., "Scheduling tasks with exponential service times on parallel processors," *Journal of Applied Probability* Vol 16 (1979), 685-689.

(2) Glazebrook K.D., "Stoppable families of alternative bandit processes," *Journal of Applied Probability* Vol 16 (1979), 843-854.

(3) Glazebrook K.D., "On randomized dynamic allocation indices for sequential design of experiments," *Journal of the Royal Statistical Society* Vol 42 (1980), 342-346.

(4) Glazebrook K.D., "On stochastic scheduling with precedence relations and switching costs," *Journal of Applied Probability* Vol 17 (1980), 1016-1024.

(5) Glazebrook K.D., "On the evaluation of suboptimal policies for families of alternative bandit processes," *Journal of Applied Probability* Vol 19 (1982), 716-722.

(6) Glazebrook K.D., "On a sufficient condition for superprocesses due to Whittle," *Journal of Applied Probability* Vol 19 (1982), 99-110.

(7) Gittins J.C. "Bandit processes and dynamic allocation indices," *Journal of the Royal Statistical Society* Vol 41 (1979), 148-177.

(8) Gittins J.C. and K.D. Glazebrook, "On Bayesian models in stochastic scheduling," *Journal of Applied Probability* Vol 14 (1977), 556-565.

(9) Gittins J.C. and K.D. Glazebrook, "On single machine scheduling with precedence relation and linear or discounted costs," *Operations Research* Vol 29 (1981), 161-173.

(10) Gittins J.C. and D.M. Jones, "A dynamic allocation index for the sequential design of experiments," in J. Gani, K. Sarkadi and I. Vince (eds) *Progress in Statistics* European Meeting of Statisticians 1972, Vol 1, North-Holland (1974), 241-266.

(11) Karatzas, I., "Gittins indices in the dynamic allocation problem for diffusion processes," Columbia University, Department of Mathematical Statistics, Preprint (1982), 40 pp.

(12) Kelly, F.P., "Multi-armed bandits with discount factor near one: the Bernoulli case," *The Annals of Statistics* Vol 9 (1981), 987-1001.

(13) Klimov G.P., "Time sharing service systems I," *Theory of Probability and Applications* Vol 19 (1974), 532-551.

(14) Klimov G.P., "Time sharing service systems II," *Theory of Probability and Applications* Vol 23 (1978), 314-321.

(15) Nash P. and J.C. Gittins, "A Hamiltonian approach to optimal stochastic resource allocation," *Advances in Applied Probability* Vol 9 (1977), 55-68.

(16) Rodman L., "On the many-armed bandit problem," *The Annals of Probabilty* Vol 6 (1978), 491-498.

(17) Wahrenberger D., C. Antle and L. Klimko, "Bayesian rules for the two-armed bandit problem," *Biometrika* Vol 64 (1977), 172-174

(18) Weitzman M.L., "Optimal search for the best alternative," *Econometrica* Vol 47 (1979), 641-654.

(19) Whittle P., "Multi-armed bandits and the Gittins index," *Journal of the Royal Statistical Society*, Vol 42 (1980), 143-149.

(20) Whittle P., "Arm-acquiring bandits," *The Annals of Probability* Vol 9 (1981), 284-292.

(21) Whittle, P., *Optimization over Time* Vol 1 (1982), John Wiley.

(22) Varaiya, P., J. Walrand and C. Buyukkoc, "Extensions of the multi-armed bandit problem," ERL Memo M83/14, University of California, Berkeley, March 8, 1983.

(23) Buyukkoc, C. and J. Walrand, "An optimal local area network design problem," preprint, University of California, Berkeley, June 1983.

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: ISS-84-3 **Last Year's No.(s):** ISS-83-3(in part)

Title: Robust, Adaptive Control and Computer-Aided Design

Senior Principal Investigator(s): C. Desoer (415) 642-0459
S. Sastry 642-1857
E. Polak 642-2644

Scientific Objective

We propose here a three pronged effort by Profs. C. A. Desoer, E. Polak and S. S. Sastry aided by graduate students on various aspects of robust control systems design in a computer aided design environment. The research is under three interrelated heads: (1) algebraic Methodologies for Control Systems design, both linear and non-linear, (2) robust adaptive control for poorly modelled and/or slowly time-varying control systems, (3) development of an interface theory between control systems design/optimization theory and optimization-based computer-aided design of both adaptive and non-adaptive control systems.

New theoretical advances under heads (1) and (2) are already being used to develop both new adaptive control theory in head (2) and design methodologies for our design package DELIGHT MIMO under head (3). We feel that a unified attack on these three problems will result in the development of new and computer-implementable methodologies of control systems design.

State of the Art

1. Robust Control Systems Design Methodologies

The basic understanding of the design possibilities and design limitations imposed by a given plant for a specific control configuration has made enormous progress in the last few years. We find it convenient to view these developments as follows:

a) the work of Youla et al. [You. 1] on the parametrization of compensation; of Desoer et al. (1980) [Des. 1] on the algebraic theory; of Desoer and M. J. Chen (1981) [Des. 2] and their design implications (CAD); of Desoer and Gustafson [Des. 3] on purely algebraic theory that both specify the achievable I/O maps and the corresponding compensator;
b) the fundamental work of Zames [Zam. 1,2] establishing some new design limitations imposed by the plant;
c) the work of Vidyasayar et al. [Vid. 1,2] proposing the best topological approach to the study of robustness;
d) the work of Doyle [Doy. 1,2] with the generalized theorem by Desoer-Chen [Des. 4] over a class of additive or multiplicative plant perturbation.
e) the extension of these ideas to ***nonlinear*** systems by Desoer and his students [An. 1, Des. 5,6,7] and by Vidyasagar [Vid. 3].

The approach to robustness used in the recent work of Chen and Desoer [Che. 3, in particular] is significantly different from the traditional approach based on additive or multiplicative perturbations as, say, in Doyle's or Sandell's work. By using factorization techniques and using the appropriate representation we can get rid of all the constraints imposed by the additive or by the multiplicative perturbation approach. This algebraic theory covers any possible perturbation. It is also satisfying to see that it touches base with the topology introduced on feedback systems by Vidyasagar et al. [Vid. 1].

2. Adaptive Control

Proceeding in parallel with the development in a robust control methodology discussed above has been progress in the field of adaptive control. Here one does not start the design process with a fixed nominal model for the plant, but parametrizes some of the uncertainties and imprecisions in the plant model. These parameters are identified on-line, i.e., during the operation of the plant; and used to improve the accuracy of the control systems design. Recent

activity in adaptive control methodologies has been triggered by two factors: (a) the realization that with the advent of inexpensive microprocessors, fairly complicated non-linear, line varying oontrol laws can be easily implemented and (b) the appearance in the literature ([Nar. 1,2], [Goo. 1], [Mar. 1], [Boy. 1]]) of proofs of stability (convergence) of a certain classes of adaptive control algorithms.

With the appearance of a firm theoretical foundation to base the analysis of adaptive control laws at least for single-input, single output control system recent attention has centered on the sensitivity and robustness of these laws to noise and high-frequency unmodelled dynamics (i.e., unparametrized) uncertainty) in the plant ([Roh. 1], [Isa. 1], [Mar. 3]). This work is essentially preliminary but addresses certain important issues which need to be resolved to formulate a viable adaptive control methodology

3. Computer Aided Control Systems Design

Over the last decade, the ability of the designer has been tremendously enhanced by the introduction of interactive computing packages. These packages enable the designer to define his problem graphically, simulate system responses and display the results graphically. With a ***computer aided-design*** environment in mind we have been developing a design package called DELIGHT.MIMO (see [Pol. 1-11]) of course, the package is applicable with equal ease to electronic circuit design and structural design. This package is described in [Nye 1,2]. Although DELIGHT.MIMO was primarily conceived for use in conjunction with semi-infinite optimization algorithms, it will include a good number of other currently used design tools, which will be usable either to provide an initial design for subsequent optimization or in stand alone fashion.

The introduction of semi-infinite optimization into control system design has created the need for an interface between control theory and optimization theory. The function of this interface theory is (i) to supply information as to the power of controller configurations, (ii) to supply efficient and computationally well conditioned controller parametrizations, (iii) to supply methods for the selection of initial values of the design vector and (iv) to supply methods for expressing performance requirements in a manner that is computationally well conditioned. Examples of results in this interface area are various stable control system parametrizations, see, e.g., [Des. 1, Per. 1, Vid. 1, Zam. 1], the expression of performance in terms of bounds on singular values, see e.g.,[Che. 1, Doy. 1, Doy 2, Doy. 3] the modifications of the Nyquist stability test {Pol. 42], the stability test for nonlinear systems in [Pol. 31], and the reduction of computational complexity, due to model uncertainty, in worst case design, by means of majorization of inequalities [Pol. 40]. Despite the existence of a few solid results, the interace area between control theory and optimization has barely been explored and remains the weakest link in the chain of optimization-based computer-aided design of control systems.

Progress and Publication Since Last Proposal

Dr. M. J. Chen was continuously supported by JSEP. The basis of his research with Professor Desoer was based on [Des. 1] -- where the co-author R. Saeks was also supported by JSEP at Texas Tech -- and on [Zam. 1]. With Dr. M. J. Chen we investigated the Q-parametrization method of design -- in which we achieved decoupling -- and the problems of robustness. The design studies were reported in [Des. 8] and [Che. 1,4]. The robustness results were reported in [Des. 3,4; Che. 2,3,4 and 5]

A recent work on nonlinear feedback control was partially supported [Des. 7].

The work partially supported by JSEP was directed towards the development of an optimization-based methodology for engineering design and was reported in [Nye. 1], and [Pol. 12], [Pol. 13], [Pol. 14], [Pol. 15], [Pol. 16] and [Pol.17]. Our work included the development of optimal design algorithms for problems with tolerancing and tuning requirements, Pol. 13; the development of superlinearly converging optimization algorithms for solving design problems with distributed constraints, [Pol. 14], [Pol. 15], [Pol. 16]; as well as general results in optimization algorithm theory which are pertinent to the construction of optimal design algorithms, [Pol.12], [Pol.17]. In addition, our work produced a major accomplishment in design software: the development of DELIGHT, Nye.1, an interactive software system for optimization-based engineering design.

Significant Accomplishments

1. The introduction of the Q-parametrization techniques of design.

2. The creation of a completely general robustness theory for linear systems having arbitrary configurations.

3. The generalization to nonlinear systems of the two-step stablization and compensation techniques that Zames proposed for linear systems.

4. The development of techniques for computer-aided design based on equality and inequality constraints, in particular semi infinite programming.

5. The development of optimization algorithm theory which are pertinent to the construction of CAD algorithm.

6. A new proof of convergence of adaptive control.

Proposed Research

1. Robust Control Systems Design Methodologies

We propose to investigate both for the linear and nonlinear case questions associated with the robustness of the design with respect to uncertainties in the plant sensor and actuation on the one hand, and to external disturbances on the other. In particular, we propose to study the relation between configuration and achievable performance; one preliminary study seems to indicate that in the linear case the two-input one-output controller dominates all other schemes, whether based on model reference or not.

We believe that the momentum achieved in this line of research presents many opportunities to develop theories that will guide the computer-aided-design of systems, studied in part 3 below.

2. Robust Adaptive Control Methodologies

In the area of adaptive control, we propose to investigate the following topics:

(1) Robustness and Sensitivity with few exceptions address stability and convergence of adaptive algorithms in the absence of noise, and high-frequency dynamics which are unstructured (i.e., non-parametrizable).

(2) Transient Behavior of Adaptive convergence establish only that the adaptive algorithm eventually, (asymptotically) converges to the desired configuration. In the transient phase, the algorithms in their present form are capable of undesirably high swings in parameter values. We propose to study modifications of the algorithms to improve transient behavior.

(3) Adaptive Control of Slowly Time-Varying Plants: One of the key applications in which adaptive control will hold an advantage over fixed formed non adaptive control is the control of slowly-varying plants. Such systems are encountered for instance in the control of high performance aircraft at varying altitude and air-speeds (the altitude and air-speed variation is slow compared to the control system.

(4) Multivariable Adaptive Control: Present work in multivariable adaptive control centers around a class of multivariable systems which can be diagonalized by dynamic feedback (see e.g., [Goo 1], [Eli. 1], and [Nar. 4]. Thus multivariable adaptive control has been developed as a small extension of the single input single-output theory. We propose to extend the theory to a larger class of systems using the algebraic techniques and insights developed in [Des. 1,2,3].

3. Computer Aided Control Systems Design

In keeping with the need for an interface between control theory and optimization we propose to do research on design parametrization and optimization initialization techniques for Computer Aided Design.

There are various known ways for parametrizing the design [Des. 3, Des. 4, Per. 1, Vid. 1, Zam. 1] of a control system. Each of these ways leads to a different semi-infinite optimization problem with different computational conditioning properties, with respect to existing semi-infinite optimization algorithms. In addition, each design parametrization has an associated, different design initialization problem which differs considerably in difficulty from parametrization to parametrization. Numerical conditioning (with respect to semi-infinite optimizaton) and design initialization aspects of control system design are still to be explored. We propose to carry out research to determine efficient design parametrization and initialization schemes.

Our proposal can be made more specific by examining the properties of two parametrization schemes for the design of a control system of the form shown in Fig. 1. We assume that in addition to stability, the designer is required to satisfy a number of time domain constraints of the form

$$\max_{t \in T} |y_k^j(t,x) - b_k^j(t)| \leq 0 \quad j = 1,2,\ldots,m, \;\; k \;,. \; k = 1,2, \tag{3.1}$$

and a number of frequency domain constraints involving either the largest or the smallest singular value of some transfer function matrix, e.g.,

$$\max_{w \in \Omega} \operatorname{smax}_{j,k} [H_{y_j u_k}(w,x)] - 1_{jk}(w) \leq 0 \quad \text{for } j = 1,2, \;\; k = 1,2, \tag{3.2}$$

where smax[H] denotes the maximum singular value of the matrix H.

To avoid numerical difficulties associated with polynomial matrix computations, we propose (in DELIGHT.MIMO) to carry out all the computations in terms of state space descriptions in terms of space descriptions together with algebraic system interconnection equations. First consider the parametrization implied by the diagram in Fig. 1. Calling the block F system 1, block C system 2 and block P system 3, we can describe the closed loop system by the equations:

$$\dot{z}_i = A_i(x)z_i + B_i(x)e_i$$

$$y_i = C_i(x)z_i + D_i(x)e_i \quad i = 1,2,3 \tag{3.3}$$

$$e_i = F_i y_i + G_i u_i$$

where the matrices A_3, B_3, C_3, D_3 are independent of x. Clearly, first derivatives of any time or frequency response with respect to x can be obtained quite easily from the above system. We assume that the A matrices in the compensator blocks are real, block diagonal, of the form

$$A_i = diag(S_{ij}), \quad j = 1,2,...k_i, \quad i = 1,2, \tag{3.4}$$

where

$$S_{i1} = a_i, \quad i = 1,2, \tag{3.5a}$$

and

$$S_{ij} = \begin{vmatrix} 0 & 1 \\ -b_{ij} & -c_{ij} \end{vmatrix} \quad \text{for } j = 2,3,....,k_i, \quad i = 1,2. \tag{3.5b}$$

The scalars a, b, c, become the components of the design vector x.

The advantages of this parametrization are as follows:

(i) it is easy to maintain control over the complexity of the controller blocks,

(ii) controller stability can be ensured by adding a set of simple linear inequalities in the coefficients of the a matrices,

(iii) it can be used with both stable and unstable plants.

The disadvantages of this parametrization are:

(i) To ensure stability of the closed loop system one must add a semi-infinite inequality corresponding to a modified form of the generalized Nyquist stability criterion, [Pol. 10], and

(ii) obtaining a reasonable initial choice for the blocks F and G involves either doing a preliminary linear quadratic design with observer, or some least squares fit to a desirable loop gain matrix PC, both fairly cumbersomer and not very reliable procedures.

It will be necessary to determine experimentally whether the need for a semi-infinite inequality to ensure closed loop system stability, based on the graphical test in [Pol. 10], adds much to the already considerable computational burden implied by the battery of semi-infinite inequalities already required for other reasons. In case the stability inequality, in the form given in [Pol. 10], is found to be computationally excessively burdensome, one will have to find alternative means for ensuring closed loop system stability.

To date, the problem of design vector initialization has received the scantest attention. Since the computing cost and even final design depend considerably on a good initial compensator choice, we propose to undertake a methodical study into means for initializing design.

Next we turn to the Q parametrization mentioned in Section 2. Since reliable numerical algorithms for state space problems exist we specify Q as

follows:

$$\dot{z}_q = A_q(x)z_q + B_q(x)e_q$$

$$y_q = C_q(x)z_q \tag{3.6}$$

In terms of Q, the controller dynamics are determined by $C=Q(I-PQ)^{-1}$, so that in state form, the controller dynamics are given by

$$\dot{z}_q = A_q(x)z_q + B_q(x)e_q$$

$$z_p = A_p z_p + B_p e_p$$

$$y_q = C_q(x)z_q \tag{3.7}$$

$$y_p = C_p z_p$$

$$e_q = u + y_p$$

$$e_p = y_q$$

The various other blocks needed to compute time and frequency domain responses can be obtained similarly from the dynamics of Q and the plant P.

The advantages of the Q parametrization are:

(i) assuming that A(x) is put in the form (3.4)-(3.5), stability of the closed loop system can be ensured by imposing simple linear inequalities on the coefficients of A(x) (because Q is stable if and only if the closed loop system is stable),

(ii) there is preliminary evidence that numerical methods described in [Van. 1] can be used to obtain an initial Q from an initial closed loop transfer function which may be quite easy to specify (e.g. diagonal structure).

The disadvantages of the Q parametrization are:

(i) it appears that it can only be used conveniently with proper, stable plants,

(ii) it does not guarantee that the resulting controller will be stale, and

(iii) it gives only indirect control over the complexity of the controller C.

As optimization-based design of control systems becomes more wide spread it will be necessary to find ways of combining the virtues of the various design parametrizations and of eliminating their disadvantages.

References

[Ana. 1] V. Anantharam and C. A. Desoer, "On Stabilization of nonlinear systems," Memo. No. UCB/ERL M82/49, May 1982.

[Boy. 1] *Boyd, S. and Sastry, S., "On parameter convergence in adaptive control," Prepint, University of California, Berkeley, June 1983.

---

* indicates JSEP support

[Che. 1] *M. J. Chen, C. A. Desoer, and G. F. Franklin, .
"Algorithmic design of single-input single-output systems
with two-input one-output controller," 20th IEEE CDC,
San Diego, p. 133-136, Dec. 1981.

[Che. 2] *M. J. Chen and C. A. Desoer,
"Necessary and sufficient conditions for robust
stability of linear distributed feedback systems,"
Proc. ISCAS, Rome, May 1982, also in *Int. Jour. Contr., 35*,
2, p. 255-267, 1982.

[Che. 3] *M. J. Chen and C. A. Desoer, "Algebraic theory
of robust stability of interconnected systems: necessary
and sufficient conditions," Proc. 21st IEEE CDC, Orlando, FL,
p. 1199-1202, Dec. 1982.

[Che. 4] *M. J. Chen, "Linear multivariable feedback
systems: robust stability, robust disturbance rejection
and design, Ph.D. Thesis, University of California, Berkeley, 1982.

[Che. 5] *M. J. Chen and C. A. Desoer, "The problem of
guaranteeing robust disturbance rejection in linear multivariable
feedback systems," Int. Jour. Contr., vol. 37, 2, p.305-314,
Feb. 1983.

[Des. 1] C. A. Desoer, R.-W. Liu, J. Murray, and R. Saeks,
"Feedback system design: the fractional approach to analysis
and synthesis," *IEEE Trans. Automat. Contr., Vol. AC-21*,
pp. 319-338, June 1980.

[Des. 2] *C. A. Desoer and M. J. Chen, "Design of
multivariable feedback systems with stable plants,"
IEEE Trans. Autom. Contr., Vol. AC-26, No. 2,
pp. 408-415, April 1981.

[Des. 3] C. A. Desoer and C. L. Gustafson, "Algebraic Theory
of multivariable systems," Memo. No. UCB/ERL M82/90,
December, 1982. [Des. 4] *M. J. Chen and C. A. Desoer, "Necessary
and
sufficient conditions for robust stability of linear distributed
feedback systems," Int. J. Contr. *35*, 2, pp. 255-267, 1982.

[Des. 5] C. A. Desoer and R. W. Liu, "Global parametrization
of feedback systems with nonlinear plant," *System and Control
Letters*, Vol. 1, No. 4, pp. 249-251, January 1981.

[Des. 6] *C. A. Desoer and C. A. Lin, "Two-step
compensation of nonlinear systems," *Systems and Control Letters*,
Vol. 3, No. 1, pp. 41-45, June 1983.

[Des. 7] C. A. Desoer and C. A. Lin, "Simultaneous
stabilization of nonlinear systems," Memo. No. M82/79,
November 1982.

---

* indicates JSEP support

[Doy. 1] J. C. Doyle and G. Stein, "Multivariable feedback design: Concepts of a classical/modern synthesis," *IEEE Trans. Automat. Contr.*, Vol. AC-26, No. 1, pp. 4-16, February 1981.

[Doy. 2] J. C. Doyle, "Analysis of feedback systems with structured uncertainties," Proc. IEEE, Vol. 129, Pr. D, No. 6, November 1982.

[Doy. 3] J. C. Doyle, J. E. Wall and G. Stein, "Performance and robustness analysis for structured uncertainty," Proceedings Conference on Decision and Control, 1982.

[Eli. 1] Elliott, K. and W. A. Wolorich, "A parameter adaptive control structure for linear multivariable systems," *IEEE Trans. Automat. Contr.*, Vol. AC-27 (1982), pp. 340-351.

[Goo. 1] Goodwin, G. E., Ramadge, P. J. and Caines, P. C., "Discrete time multivariable adaptive control," *IEEE Trans.* Automat. Contr., Vol. AC-25 (1980), pp. 449-456.

[Ioa. 1] Ioannou, P. A., *Robustness of Model Reference Adaptive Systems with Respect to Modelling Errors*, Ph.D. Dissertation, University of Illinois, Urbana, Champaign, August 1982.

[Mor. 1] Morse, A. S., "Global stability of parameter adaptive control systems," *IEEE Trans. Automat. Contr.*, Vol. AC-25 (1980) pp. 433-440.

[Nar. 1] Narendra, K. S., Valavani, L. S. "Stable adaptive controller design-direct control," *IEEE Trans. on Automat. Contr.*, Vol. AC-25 (1978), pp. 570-583.

[Nar. 2] Narendra, K. S., Lin, Y. H., Valavani, L. S., Stable adaptive controller design, Part II: Proof of stability," *IEEE Trans. Automat. Contr.*, Vol. AC-25, (1980), pp. 440-448.

[Nar. 3] Narendra, K. S. and Peterson, B. B., "Bounded error adaptive control," *IEEE Trans. Automat. Contr.*, Vol. AC-27 (1982), pp. 1161-1169.

[Nar. 4] Narendra, K. S. and Singh, R. P., "A globally stable adaptive controller for multivariable systems," Yale University Preprint, April 1982.

[Nye 1] *W. Nye, E. Polak, A. Sangiovanni-Vincentelli and A. Tits, "DELIGHT: an Optimization-Based Computer-Aided-Design System", Proc. IEEE Int. Symp. on Circuits and Systems, Chicago, Ill, April 24-27, 1981.

[Nye. 2] Nye, W., and Tits, A. L., "DELIGHT for beginners," University of California, Berkeley, Electronics Research Memo UCB/ERL M82/55, July 1982.

---

* indicates JSEP support

[Per. 1] Pernebo, L., "An algebraic theory for the design of controllers for linear multivariable systems - Parts I and II," *IEEE Trans. Automat. Contr.*, Vol. AC-26, No. 1, pp. 171-193, February 1981.

[Pol. 1] Polak, E., "On the use of optimization algorithms in the design of linear systems," Report No. UCB/ERL - M377, Electronics Research Laboratory, University of California, Berkeley, 1973.

[Pol. 2] Polak, E., Trahan, R., "An algorithm for computer aided design of control systems," *IEEE Conf. on Decision and Control*, 1976.

[Pol. 3] Polak, E., and Mayne, D. Q., "Algorithms for computer aided design of control systems by the method of inequalities," *Proc. 18th IEEE Conference on Decision and Control*, Fort Lauderdale, Florida, December 12-14, 1979.

[Pol. 4] Polak, E., "An implementable algorithm for the design centering, tolerancing and tuning problem," in *Computing Methods in Applied Science and Engineering*, R. Glowinski, J. L. Lions, ed., North Holland, Amsterdam, 1980, pp. 499-517.

[Pol. 5] Polak, E., and Mayne, D. Q., "On the solution of singular value inequalities over a continuum of frequencies," *IEEE Trans. on Automat. Contr.*, Vol. AC-26, No. 3, pp. 690-695, 1981.

[Pol. 6] Polak, E., and Mayne, D. Q., "Design of nonlinear feedback controllers," Proceedings, 20th IEEE CDC, Albuquerque, NM, December 10-12, 1980. *IEEE Trans. Automat. Contr.*, Vol. AC-26, No. 3, pp. 730-733, 1981.

[Pol. 7] Polak, E., and Wardi, Y., "A nondifferentiable optimization algorithm for the design of control systems subject to singular value inequalities over a frequency range," *Automatica*, Vol. 18, No. 3, pp. 267-283, 1982.

[Pol. 8] Polak, E. and Stimler, D. M., "Optimization-based design of SISO control systems with uncertain plant: problem formulation," Memo No. UCB/ERL M83/16, University of California, Berkeley, California, 1983.

[Pol. 9] Polak, E. and Mayne, D. Q., "Algorithm models for nondifferentiable optimization," University of California, Berkeley, Electronics Research Laboratory, Memo. No. UCB/ERL M82/34, May 10, 1982.

[Pol. 10] Polak, E., "A modified Nyquist stability criterion for use in computer-aided design," University of California, Berkeley, Electronics Research Laboratory, Memo. No. UCB/ERL M83/11, 1983; *IEEE Trans. Automat. Contr.*, in Press.

[Pol. 11] Polak, E., Siegel, P., Wuu, T., Nye, W., Mayne, D. Q., "DELIGHT.MIMO, an interactive, optimization-based multivariable

control system design package," *IEEE Control Systems Magazine*, Vol. 2, No. 4, pp. 9-15, 1982.

[Pol. 12] *E. Polak, D.Q. Mayne and Y. Wardi, "On the Extension of Constrained Optimization Algorithms from Differentiable to Nondifferentiable Problems", SIAM J. Cont. & Opt. Vol. 21, No.2, pp 179,204, 1983.

[Pol. 13] *E. Polak, "An implementable algorithm for the design centering, tolerancing and tuning problem", JOTA, Vol. 35, No. 3, Nov. 1981.

[Pol. 14] *E. Polak, "Semi-infinite optimization in engineering design", International Symposium on Semi-Infinite Programming, Univ. of Texas, Austin Texas, September 8-10, 1981

[Pol. 15] *E. Polak and A. Tits, " On globally stabilized quasi-newton methods of inequality constrained optimization problems", Proc. 10th IFIP Conference on System Modeling and Optimization, New York, August 31-September 4, 1981.

[Pol. 16] *E. Polak and A. Tits, " A Recursive Quadratic Programming Algorithm for Semi-Infinite Optimization Problems", J. Appl. Math. and Optimization, Vol. 8, pp 325-349, 1982.

[Pol. 17] *E. Polak and Y. Y. Wardi, "A study of minimizing sequences", University of California, Electronics Research Laboratory Memo UCB/ERL No. M82/22, March 22, 1982. submitted to SICOPT.

[Roh. 1] Rohrs, C. E., *Adaptive control in the presence of unmodelled dynamics*, Ph.D. Dissertation, M.I.T., November 1982.

[Van. 1] van Dooren, P., "The generalized eigenvalue problem in linear system theory," *IEEE Trans. Automat. Contr.*, Vol. AC-26 (1981), pp. 111-129.

[Vid. 1] M. Vidyasagar, H. Schneider, and B. A. Francis, "Algebraic and topological aspects of feedback stabilization," *IEEE Trans. Automat. Contr.*, Vol. AC-27, No. 4, pp. 880-894, August 1982.

[Vid. 2] M. Vidyasagar, and N. Viswanatham, "Algebraic design techniques for reliable stabilization," *IEEE Trans. Automat. Contr.*, Vol. AC-27, No. 5, pp. 895-903, October 1982.

[Vid. 3] M. Vidyasagar, Personal communication, June 1983.

[You. 1] D. C. Youla, H. A. Jabr, and J. J. Bongiorno,Jr., "Modern Wiener-Hopf design of optimal controllers, Part II: the multivariable case," *IEEE Trans. Automat. Contr.*, Vol. AC-21, pp. 319-338, June 1976.

[Zam. 1] G. Zames, "Feedback and optimal sensitivity: model reference transformation, multiplicative seminorms and

* indicates JSEP support

approximate inverse," *IEEE Trans. Automat. Contr.*, Vol. AC-26, No. 2, pp. 301-320, April 1981.

[Zam. 2] G. Zames and B. A. Francis, "Feedback, Minimax sensitivity, and optimal robustness," *IEEE Trans. Automat. Contr.*, Vol. AC-28, No. 5, pp. 585-600, May 1983.

University of California, Berkeley **Electronics Research Laboratory**

Joint Services Electronics Program **August 15, 1983**

Work Unit No.: ISS-84-4 **Last Year's No.(s):** N.A.

Title: Optimization Based Computer-Aided Design of Integrated Circuits

Senior Principal Investigator(s):	A. Sangiovanni-Vincentelli	(415)642-4882
	R. Meyer	642-8028

Scientific Objective

Our objective is the development of an interactive, optimization-based, computer-aided design methodology for the design of complex integrated circuits. Particular emphasis will be placed on statistical aspects of integrated circuit design such as yield maximization. To this end, we propose to develop a new formulation of the statistical design problem, new specialized, single and multi-objective optimization algorithms, circuit simulation techniques and device models.

The new formulation of the design problem must reflect the goal of maximizing the economic gain attributable to the design. The optimization algorithms to be developed must be capable of solving complex, nondifferentiable, semi-infinite optimization and trade-off problems which arise in integrated circuit design when tolerances and distributed constraints are taken into account. The simulation techniques have to be particularly fast since yield calculation requires many solutions of the circuit equations. In addition, optimization algorithms involve many iterations and, for each iteration, several yield calculations may be required. Furthermore, our simulation procedures must be capable of producing not only circuit responses, but also the derivatives of these responses with respect to design parameters since the most effective optimization algorithms are based on the sensitivity of the circuit responses to parameter variations. Device models must be developed in terms of production parameters by making use of the fact that the variation of many circuit parameters can be expressed in terms of variations of production parameters. By developing these models, the number of circuit analysis needed to calculate the yield can be reduced for circuits containing on the order of 100 devices by more than two orders of magnitude.

Finally, our theoretical work will be implemented and experimentally evaluated in an interactive-computer aided design facility which we are developing.

State of the Art

Formulation and Optimization Algorithms

There have been a number of mathematically distinct formulations of optimization problems intended to deal with the optimal design of circuits subjected to statistical fluctuations (see [BRA-80], [BRA-81]. In particular, two formulations have been widely used. One formulation holds circuit specifications fixed, and adjusts the nominal values of the design parameters subject to random fluctuations in order to maximize the expected value of the fraction of the operational circuits which meet specifications, the parametric yield. This is the "(parametric) yield maximization", or "design centering" formulation. Another formulation, "tolerance assignment", assumes that for most design parameters the amount of their random dispersion is not in fact fixed. Reducing the dispersion certainly increases yield, which tends to decrease effective circuit cost. But to reduce random dispersion requires the use of fabrication techniques which tend to increase circuit cost. Tolerance assignment attempts to find the set of parameter dispersion magnitudes which minimizes cost in this tradeoff. These formulations are limited in a number of ways. First, the yield that is considered in these formulations deals only with statistical fluctuations of the device parameters (parametric yield) and ignores spot-defect yield, a major factor in determining the overall yield; second, the objective function reflecting the manufacturing cost has not been carefully studied.

The property of yield which distinguishes it from the kinds of optimization criteria more commonly found in optimal circuit design, is that the yield is expressed in the form of a multidimensional integral. This integral if evaluated without special techniques would would make yield calculations very expensive. For later reference, the yield integral can be written as,

$$\int_{F(x_M)} f(x, x_M) dx$$

where x and x_M are vectors in the parameter space $!RR^n$, $f(x, x_M)$ is the probability density function of the random parameter vector X at point x, having mean x_M, and $F(x_M)$ is the feasible set, i.e. the set of points in $!RR^n$ such that the circuit satisfies a given set of performance constraints. The techniques which have been proposed for yield maximization generally fall into two categories - probabilistic, i.e., those that use some Monte Carlo technique, and deterministic, i.e., those that relax and modify the requirements on the design, so as to eliminate the need for Monte Carlo analysis and to reformulate the design problem in a simpler deterministic form [BRAY-81].

Among the major contributions in the deterministic class are the simplicial approximation technique of Director and Hachtel [DIR-77], the performance function polynomial approximation approach of Bandler and Abdel-Malek [BAN-77,BAN-78, ABD-80], the outer approximations algorithm approach proposed by Polak and Sangiovanni [POL-79], the extension of minmax optimization to statistical design by Madsen and Schjaer-Jacobsen [MAD-78], and the constrained optimization approach by Brayton et al [BRA-79]. Although the deterministic class is approaching maturity, the methods make restrictive assumptions, e.g. convexity of the set A in the case of simplicial approximation, they lack error bounds, and they all suffer a fatal degradation of efficiency as the number of parameters increases towards typical IC design problem values.

The algorithms developed in this research are expected to be more closely related to the techniques in the probabilistic class. The obstacle to routine application of proven mathematical programming techniques here is that the use of Monte Carlo methods introduces errors in the estimation of the yield and especially its derivatives which are roughly speaking proportional to $1/N$, where N is the number of samples, with an unacceptably large proportionality constant. The literature on Monte Carlo evaluation of integrals contains a number of techniques, called variance reduction techniques [SCH-66,MCG-73,HAM-75], for essentially reducing the proportionality constant.

A significant portion of the probabilistic literature presents techniques for yield estimation rather than yield maximization, giving scant or no attention to the problem of efficient computation of yield improvement directions. Rankin and Soin [RAN-81] describe the application of the well known control variate method of variance reduction to the estimation of circuit yield. Singhal and Pinel [PIN-77,SIN-80] describe a direct application of the importance sampling variance reduction technique. Neither methodology is particularly encouraging. Although the quadratic approximation technique of Hocevar et al [HOC-83] ignores the yield derivative problem, it is a very promising application of correlated sampling [COC-77,BEC-77].

Among the methods making respectable attempts to do yield maximization are a number using approximations of the feasible region A. Styblinski et al [OGR-80,STY-80,STY-81] use a series of one-dimensional orthogonal searches of the feasible set to enable a mixed Monte Carlo and direct integration approach, but its claims to efficiency are based an accelerated search process applicable only to linear circuits, and ignore discrepancies in the cost of each Monte Carlo trial. Spence et al [LEU-74,LEU-76,TAH-78, TAH-79, TAH-80,SOI-78,SOI-79,SOI-

80] have proposed a number of geometric approaches, including radial exploration, in which the feasible set is searched in randomly chosen directions, to estimate yield and compute a direction of yield improvement. However the methods assume uniform parameter distributions or linear problems, and are missing mathematical justification.

The more analytic approaches are of greater relevance to our work. Strasz and Styblinski [STR-80] have shown how yield gradients and second derivatives can be computed using the same Monte Carlo trials as are used to estimate the yield, and he bases a yield maximization method on these techniques. But as Hocevar et al [HOC-83] have shown, the errors in computing the yield derivatives are large compared to those in computing the yield itself, making the potential of the method questionable. Antreich and Koblitz [ANT-80,ANT-81,ANT-82] have derived a number of quadratic expressions for yield in the neighborhood of an arbitrary point in terms of first and second statistical moments with respect to a distribution centered at that point. The moments can be evaluated via Monte Carlo. However gaussian parameter distributions and constant dispersions are assumed, and special techniques must be employed to suppress the effects of error in the yield derivatives (quadratic coefficients), saddle-point behavior, and other errors. Finally, Kjellstrom and Taxen [KJE-69,KJE-75,KJE-76,KJE-81], guided by information theory concepts, explore the feasible set with samples from gaussian distributions updated with each iteration to maintain a constant probability of the samples falling in the feasible set. The methodology seems very promising but its details are poorly defined, and its performance in practical IC problems unknown.

Simulation

Electronic circuit simulation (e.g. [SAN-81, HAC-81, NASG-75]) is a well established design aid. In optimization-based design, circuit simulation is required for function and gradient evaluations.

When hundreds of simulations are required as in yield evaluation or when the circuit to be simulated is very large, as is the case of Very Large Scale Integrated (VLSI) circuits, "standard" simulation methods used in simulators such as SPICE2 and ASTAP, take too much cpu time or too much storage to be economically acceptable. New simulation methods are presently emerging which decompose a simulation into set of simpler tasks that can be carried out either independently or in some order.

Simulators based on nonlinear relaxation methods [CHA-75, NEW-79, LEL-82a, WHI-83, KLE-82] have been developed for the analysis of a special class of circuits of great importance for VLSI technology: MOS circuits. The numerical techniques, in part discovered by A. Sangiovanni-Vincentelli, one of the PIs, which are used in the simulators RELAX [LEL-82, WHI-83] (Waveform Relaxation) and SPLICE [KLE-82] (Iterated Timing Analysis), have been proven to be reliable and fast. In a number of test examples transient simulation has been carried out with up to two orders of magnitude speed improvement over standard simulators such as SPICE2.

Work needs to be done to extend the use of relaxation methods for dc and ac analysis. Initial experiments with SPLICE [KLE-83] show that it is possible to run one hundred iteration of a nonlinear relaxation method to find the dc operating point of a circuit. To build a circuit simulator with full analysis capabilities including ac and dc operating point, new relaxation techniques have to be developed. Aggregation methods seem a very promising technique.

The use of aggregation methods to speed up a relaxation process applied to the solution of the linear system:

$$x = Ax + b$$

was proposed by R.P. Fedorenko [FED-61, FED-64] in 1961, in connection with the solution of partial differential equations by finite difference methods: to obtain a closer approximation to the solution of the linear system, he introduced an auxiliary net, whose mesh size was an integer multiple of the original net. Another example can be found in a book by Leontief [LEO-51] with reference to a problem arising in input-output economics. Considering a linear model for a productive economy consisting of n industrial sectors, he constructed a reduced model by aggregating together groups of sectors, thus reducing the size of the linear system that described the economy.

More recently, a survey of aggregation methods was compiled by F. Chatelin and W.L. Miranker [CHA-80], who also showed that all the existing aggregation methods are nothing else but different implementations of the same mathematical idea; more precisely, aggregating a system corresponds to performing a projection on a suitable linear subspace: different aggregation methods correspond to different choices of subspaces.

In the same work, several numerical examples are reported, showing how effective aggregation methods can be in improving the performance of relaxation processes. However, the analysis carried out in that report also shows an obvious limitation of these methods as they have been implemented so far. In fact, the authors prove that the choice of the subspace plays a major role in the gain that can be obtained from an aggregation step: if we denote the projection operator by P, and if $\rho(A(I-P))$ is significantly less than $\rho(A)$, then the relaxation process will converge much faster after an aggregation step. This is due to the fact that, by solving the aggregated system, we annihilate the component of the error lying in the subspace generated by those eigenvectors of A corresponding to the eingenvalues of largest magnitude.

It is therefore obvious that we should choose carefully the subspace which to perform the projection onto; on the contrary, all the aggregation methods that we know of operate that choice either randomly or on the basis of heuristic considerations, without taking into account the structure of the specific matrix involved.

Device Modeling

In general, all the above-mentioned approaches to yield optimization assume that the device parameters are affected by independent statistical fluctuations. Since typical active devices require eight or more parameters for acceptably accurate representation, the computer simulation of even small circuits becomes impractical if all possible parameters are independently varied. In addition, this simulation would give a misleading estimate of the production spread of circuit performance since many device parameters are closely correlated in their product variations. Maly and Strojwas [MAL-82] propose the use of the process simulator FABRICS to generate the dependence of the parameters of a device on both layout and process parameters. This approach has been reported to be quite feasible in terms of computation time. However, we feel that the dependence of the device parameters on the process and layout parameters could be modeled explicitly with good accuracy, thus eliminating the need of an additional program in the design loop. In particular, R.G. Meyer, one of the PIs, has been able to derive such models for the bipolar technology. The models have been built and tested over a number of industrial designs.

Progress and Publications Since Last Major Proposal

A. Under JSEP

1. Existing semi-infinite optimization algorithms used in engineering design are very reliable. However, since they are only first order methods, they are rather slow. Now, engineering design via optimization involves a great deal of time-consuming simulation and hence, in conjunction with first order methods, can be quite expensive in computer time. Obviously, there is a great need for faster methods. Professor E. Polak, in collaboration with Professor D. Q. Mayne of Imperial College, London, and Andre Tits, a former graduate student now Assistant Professor at the University of Maryland, have made a considerable amount of progress in devising superlinearly converging algorithms for solving nonlinear semi-infinite optimization problems encountered in engineering design. Their work is reported in the following papers.

D. Q. Mayne and E. Polak, "A quadratically convergent algorithm for solving infinite dimensional inequalities," University of California, Berkeley, Electronics Research Laboratory Memo No. UCB/ERL M80/11, 1980. To appear in *J. of Appl. Math. and Optimization.*

E. Polak and A. Tits, "A recursive quadratic programming algorithm for semi-infinite optimization problems," International Symposium on Semi-infinite Programming, University of Texas, Austin, September 8-10, 1981, also to appear in *J. of Appl. Math. and Optimization.*

E. Polak and A. Tits, "On Globally stabilized quasi-newton methods for inequality constrained optimization problems", 10th IFIP Conference on System Modeling and Optimization, New York August 31-September 4, 1981.

D.Q. Mayne and E. Polak, "A superlinearly convergent algorithm for constrained optimization problems", *Mathematical Programming Study 16*, On Constrained Optimization, pp. 45-61, 1982.

2. We have made a great deal of progress in constructing an interactive computing system for optimization-based computer-aided-design. Our present package, DELIGHT, offers an extremely high level language for very rapid and easy optimization program writing; extreme modularity, which permits very simple assembly of algorithms and problems from blocks; easy interface to simulation and system definition packages such as SPICE; various interrupt and restart features; powerful graphics; etc. Recently we have developed a version of the DELIGHT system for integrated circuit design called DELIGHT.SPICE that has been successfully used in the design of complex integrated circuits in an industrial environment. Our progress to date on this system is described in:

W. Nye, E. Polak, A. Sangiovanni-Vincentelli and A. Tits, "DELIGHT: an optimization-based computer-aided-design system," University of California, Berkeley, Electronics Research Laboratory Memo UCB/ERL M81/19, 1981; *Proc. IEEE Int. Symp. on Circuits and Systems*, Chicago, Ill, April 24-27, 1981.

W. Nye, A. Sangiovanni-Vincentelli, J. Spoto and A. Tits, "DELIGHT.SPICE: An Optimization-Based System for the Design of Integrated Circuits", *Proceedings of the 1983 Int. Conf. on Custom Int. Circ.*, Rochester, May 1983.

3. In our earlier work on the deterministic approach to the design centering, tolerancing and tuning problems, we discovered that these problems are inherently nondifferentiable. An examination of the literature showed that

there was very little available by way of nondifferentiable optimization algorithms. It was therefore clear that the art of constructing nondifferentiable optimization algorithms would have to be considerably extended if these algorithms are to become a realistic tool in engineering design. Professor E. Polak, in collaboration with Professor D. Q. Mayne of Imperial College, London, and Y. Wardi, a graduate student, have studied the possibility of obtaining nondifferentiable optimization algorithms by extension of differentiable optimization algorithms. Their results are most encouraging and are reported in:

E. Polak, D. Q. Mayne and Y. Wardi, "On the extension of constrained optimization algorithms from differentiable to nondifferentiable problems," University of California, Berkeley, Electronics Research Laboratory Memo No. UCBERL M81/78, 1981, also to appear in *SIAM J. on Cont. and Opt.*

E. Polak and D.Q. Mayne, "Algorithm Models for Nondifferentiable Optimization", University of California, ERL Memo UCB/ERL No. M82/34, May 1982.

E. Polak, "Semi-infinite Optimization in Enginering Design", International Symposium on Semi-infinite Programming, Univ. of Texas, Austin, Texas, Sept. 8-10, 1981.

4. Professor Polak has shown that nondifferentiable, design centering, tolerancing and tuning problems can be decomposed into a sequence of differentiable optimization problems via outer approximations. As a result, the arsenal of computational tools available for their solution is much enlarged.

E. Polak, "An Implementable Algorithm for the Design Centering, Tolerancing and Tuning Problem", *J. on Opt. Th. and App.*, Vol. 35, N. 3, Nov. 1981.

5. Professor Polak in collaboration with Y. Wardi, a graduate student has presented a theory that enables one to make some sense in a number of optimization problems defined on function spaces, where either the problems themselves have no solutions or algorithms construct sequences in solving them that have no accumulation points in the spaces in which they are defined. The tools used to achieve this result are minimizing sequences.

E. Polak and Y. Wardi, " A Study of Minimizing Sequences", University of California, Berkeley, ERL Memo M82/22, March 1982.

6. Professor A. Sangiovanni-Vincentelli has co-authored three survey papers dealing with various design aids for VLSI. These papers are as follows:

R. Newton, D. O. Pederson, A. Sangiovanni-Vincentelli and C. Sequin, "Design aids for VLSI: The Berkeley perspective," *IEEE Trans. on Circuits and Systems, July 1981.*

G. Hachtel and A. Sangiovanni-Vincentelli, "A survey of third generation simulation techniques," *IEEE Proc.*, November 1981.

R. Brayton, G. Hachtel and A. Sangiovanni-Vincentelli, "A survey of optimization techniques for integrated circuit design," *IEEE Proc.*, November 1981.

7. Professor A. Sangiovanni-Vincentelli and V. Visvanathan, a graduate student, partly in collaboration with Professor of R. Saeks of Texas Technological University, have made a considerable amount of progress in the area of diagnosability

of nonlinear circuits and systems. Their work is reported in the following papers:

V. Visvanathan and A. Sangiovanni-Vincentelli, "Diagnosability of nonlinear circuits and systems, Part I: The DC case," Special joint issue of *IEEE Trans. on Computer and IEEE Trans. on Circuits and Systems* on Design for Testability, November 1981.

R. Saeks, A. Sangiovanni Vincentelli and V. Visvanathan, "Diagnosability of nonlinear circuits and systems-Part II: Dynamical systems," Special joint issue of *IEEE Trans. on Computers and IEEE Trans. om Circuits and Systems*, on Design for Testability, November 1981.

V. Visvanathan, "Applications of Differential Sensitivity to Large-Perturbation Problems: Diagnosability and Model Simplification", PhD Thesis, University of California, Berkeley, 1982.

8. Professor A. Sangiovanni-Vincentelli and E. Lelarasmee, a graduate student, partly in collaboration with Dr. A. Ruehli of IBM T.J. Watson Research Center, have developed a new family of relaxation based methods for large scale circuit simulation. It has been possible to characterize the convergence properties of these methods and to show that for a large class of circuits, i.e. MOS digital circuits, the method will always converge to the solution of the circuit equations. An experimental computer program called RELAX, has been written. Its performances are impressive: using the same models, RELAX has computed with the same accuracy transient responses of MOS digital circuits about 70 times faster than SPICE2. This research has been awarded a best paper award at the 1982 Design Automation Conference and the D.J. Sakrison Memorial Award given to E.Lelarasmee for outstanding research done by a graduate student in the Department of EECS, University of California, Berkeley. In addition the paper published by the IEEE Transactions on CAD of IC and Syst. has obtained the Guillemin-Cauer Award for the best paper published in the Transactions sponsored by the Circuits and Systems Society in 1981-1982. The papers where these results have been reported are:

E. Lelarasmee, A. Ruehli and A. Sangiovanni-Vincentelli, "The Waveform Relaxation method for time domain analysis of large scale integrated circuits", *IEEE Trans. on Comp. Aided Des. of Int. Circ. and Syst.*, vol CAD-1,No. 3, pp.131-145, July 1982.

E. Lelarasmee, A. Sangiovanni-Vincentelli and A. Ruehli, "A New Relaxation Technique for Simulating MOS Digital Integrated Circuits" *Proc. 1982 Int. Symp. on Circ. and Syst.*, pp. 1202-1205, Rome, May 1982.

E. Lelarasmee and A. Sangiovanni-Vincentelli, "RELAX: A New Circuit Simulator for Large-Scale MOS Integrated Circuits" *Proc. 19th Design Automation Conference*, pp. 682-690, Las Vegas, June 1982.

E. Lelarasmee, "The Waveform Relaxation Method for the time domain analysis of large scale integrated circuits: Theory and Applications", PhD Thesis, University of California, Berkeley, 1982.

Significant Accomplishments

1. We have made important progress in devising superlinearly convergent algorithms for the solution of semi-infinite optimal design problems.

2. We have developed a comprehensive theory of diagnosability for dynamical nonlinear circuits and systems.

3. We have made a considerable amount of progress in developing DELIGHT, a highly sophisticated interactive computing system for optimization-based computer-aided design of engineering systems and, in particular, of DELIGHT.SPICE for the design of complex integrated circuits.

4. We have developed a new family of relaxation-based methods for the simulation of large scale circuits that may open an entire new vista on circuit simulation.

Proposed Research Program

Introduction

The research which we propose to carry out is in three parts: (i) the development of a new formulation of the problem of optimal design of integrated circuits subjected to statistical fluctuations and algorithms for its solution; (ii) the development of efficient simulation algorithms and programs based on relaxation techniques; and (iii) the development of device and circuit models which allow to express system behavior in terms of a very small number of fundamental variables which can be controlled in the production process.

Our research results will be tested, evaluated and fine-tuned in our interactive computing facility which is currently being used to develop a multidisciplinary, optimization-based computer-aided design methodology. We have access to three DEC VAX11/780 computers and to a variety of sophisticated, interactive graphics terminals, an ideal medium for this type of experimental work.

Formulation and Optimization Algorithms.

A critical aspect of the design of integrated circuits subjected to statistical fluctuations is the choice of the objective function. The objective function should reflect the "cost" associated with the production of integrated circuits. The cost model should consist of the sum of all additive contributions to cost which depend either deterministically or stochastically on a set of continuous design parameters, be they electrical or fabrication process parameters, plus a constant cost covering all contributions to cost not dependent on those parameters. The sophistication of the model should exceed that of any model published heretofore. On the other hand, the goal is not to develop a detailed accounting of cost for all the cost-reduction purposes a manufacturer might have, but just to capture the essence of the manufacturers cost considerations as they pertain to the formulation of the appropriate optimization problem. This reformulation is expected to have a major theoretical impact on our algorithm development work.

In particular, we propose to incorporate in the cost model the contribution to yield loss due to spot defects. Using probabilistic models, we expect to be able to express expected defect yield in terms of the same parameters as for the parametric yield, since the defect yield can be related to the total device area. It is known that scaling up all device dimensions increases parametric yield but decreases defect yield. Yet no existing formulation addresses this conflict.

Another major innovation of the cost model we propose to develop in this research is the elimination of the assumption that all manufactured IC circuits are tested on the basis of rigid specifications and discarded if they fail to meet these specifications. This has not been the case in the manufacturing of

integrated circuits, yet the assumption is fundamental to the formulation of the standard yield maximization problem as approached in the literature. It is expected that the objective function to be developed will allow the assumption that manufactured IC's are to be sorted into a few performance ranges on the basis of the salient specification(s), and given values established for the particular performance range in which they fall.

As we have pointed out in State of the Art, taking manufacturing and identification errors into account creates very difficult statistical design problems. We propose to develop new algorithms for statistical design based on Monte Carlo techniques.

The speed of convergence of and the quality of design obtained by Monte Carlo based algorithms, are quite sensitive to the errors caused by the Monte Carlo evaluation of the yield, while the total computing time is dominated by the Monte Carlo analyses. Fortunately, for multinormal probability distributions, a formula is available which relates the variance of the Monte Carlo estimate of the yield $v(y(x))$ with the yield $y(x)$ and the number of trials N.

$$v(y(x))=(y(x)(1-y(x)))/N \qquad (*)$$

Since the variance decreases as the number of trials increases, the precision of the estimate can be increased at the expense of computing time. Fortunately, the uncertainties which affect many engineering systems can be modeled by multinormal distributions, and hence can be used to evaluate the error associated with the Monte Carlo estimate of the yield.

Current Monte-Carlo-based optimization algorithms, make no allowance for the errors produced by Monte Carlo analyses and hence it is quite likely that they will fail on a good number of problems. In principle, since (*) provides a quantitative means for controlling evaluation errors, it is possible to apply the theory on the use of adaptive approximations in optimization algorithms developed in [POL-71] to produce extensions of differentiable optimization algorithms for the solution of statistical design problems. We propose to explore this possibility in constructing robust optimization algorithms for statistical design.

Usually, in optimization algorithms the major computing cost is incurred in the function evaluations for step size determination. As pointed out in State of the Art, the cost of a function evaluation in Monte Carlo analysis is very high since it requires N simulations of the system being designed, where N is in general large when a reasonable accuracy is required. To reduce this cost, we propose to develop special purpose, efficient step size computation subprocedures. In addition, we propose to develop approximations to the yield, which will either involve no Monte Carlo analyses or will require fewer system simulations.

Circuit Simulation

This part of the project is devoted to the development of simulation techniques and programs which are very fast to make the yield evaluation and the optimization of large integrated circuits possible. In particular, we propose the development of aggregation methods for the solution of dc and ac circuit equations. As pointed out in the section on the State of the Art, aggregation methods have been proposed for the solution of linear systems of equations. The ac equations of an integrated circuit are indeed linear. However, the existing aggregation method cannot be applied directly because of their lack of reliability as discussed in the State of the Art. In particular, we will focus on the choice of the subspace onto which the aggregation methods project by considering the spectrum of the matrix A of the coefficients of the linear system of equations. It could be objected that calculating the eigenvalues of a matrix is

much more difficult and time-consuming than solving a set of linear equations by a direct method (e.g. Gauss elimination); however, we believe that a better choice for the subspace can be achieved even without computing the eigenvalues of A. For this purpose, we think of exploiting the behavior of the successive approximations generated by the relaxation process in order to gain relevant information about the spectral nature of the matrix. In fact, it is well known that relaxation methods are strongly affected by the spectral nature of the system to be solved: an obvious example is that they fail if the spectral radius of A, $\rho(A)$ is greater than 1. For the same reason, we should be able to gain some insight into the nature of the spectrum of A from the sequence $\{x_k\}$; this should lead to approximations closer to the actual solution even by one or two orders of magnitude.

The computational complexity involved should be of the same order as the one of the existing aggregation methods, so that a significant improvement in terms of computer time needed could be achieved.

In addition, we propose to extend aggregation methods to the nonlinear case so that the dc circuit equations can also be solved by relaxation techniques. This will make it possible to build a complete circuit simulator capable of transient, ac and dc analysis based on relaxation methods that have been proven so successful in the simulation of VLSI circuits.

Device Modeling

The major task in this area is to develop device models which lead to efficient computations in the context of optimization-based computer-aided design of integrated circuits involving yield optimization. Our initial work in this area led to the realization of a bipolar transistor model for integrated circuits in which only four basic process parameters are used to represent the *effects* of process tolerances. The simulation of a circuit with one hundred such devices can now be made with only four independent variables to be considered, instead of the eight hundred device parameters needed to specify the circuit.

We propose to extend this work to MOS circuits by conducting research on MOS modeling for statistical design. As in the case of bipolar transistors, a typical MOS transistor requires at least eight parameter values for accurate representation. Due to the close physical matching of monolithic devices, it should be possible to characterize all MOS transistors in a give circuit by appropriately derived process parameters. The optimum choice of modeling parameters is crucial to the success of such an undertaking, as is the need for extensive measurement of sample wafers and correlation of computer prediction with measured circuit performance. The project will begin with considerations of the basic physics involved in MOS transistor operation, coupled with modeling of fabrication processes such as oxidation, ion implantation and photolithography. Test structures will be devised and fabricated and subjected to statistical parameter evaluation as a function of controlled process variation.

References

[ABD-80] H. L. Abdel-Malek and J. W. Bandler, "Yield optimization for arbitrary statistical distributions - Part I: Theory," IEEE Trans. Circuits and Syst., vol. CAS-27, pp. 245-252, Apr. 1980.

[ABD-80] H. L. Abdel-Malek and J. W. Bandler, "Yield optimization for arbitrary statistical distributions - Part II: Implementation" IEEE Trans. Circuits and Syst., vol. CAS-27, pp. 253-262, Apr. 1980.

[ANT-80] K. J. Antreich and R. K. Koblitz, "A new approach to design centering based on a multiparameter yield-prediction formula," in Proc. 1980 IEEE Int. Symp. Circuits and Syst., (Houston,TX), pp. 886-889, Apr. 1980.

[ANT-81] K. J. Antreich and R. K. Koblitz, "An interactive procedure to design centering," in Proc. 1981 IEEE Int. Symp. Circuits and Syst., (Chicago,Ill), pp. 139-142, Apr., 1981.

[ANT-82] K. J. Antreich and R. K. Koblitz, "Design centering by yield prediction," IEEE Trans. Circuits and Syst., vol. CAS-28, pp. 88-96, Feb. 1982.

[BAN-77] J. W. Bandler and H. L. Abdul-Malek, "Optimal centering, tolerancing, and yield determination using multidimensional approximations," in Proc. 1977 Int. Symp. Circuits and Syst., (Phoenix, AZ), pp. 219-222, Apr. 1977.

[BAN-78] J. W. Bandler and H. L. Abdul-Malek, "Yield estimation for efficient design centering assuming arbitrary statistical distributions" Int. J. Circuit Theory Appl., vol. 6, pp. 289-303, 1978.

[BAN-78] J. W. Bandler and H. L. Abdul-Malek, "Optimal centering, toler- ancing, and yield determination via updated approximation and cuts," IEEE Trans Circuits Syst., vol. CAS-25, pp. 853-871, Oct. 1978.

[BEC-77] P. W. Becker and F. Jensen, Design of Systems and Circuits for Maximum Reliability or Maximum Production Yield, New York: McGraw-Hill, 1977.

[BRA-79] R. K. Brayton, S. W. Director, and G. D. Hachtel, and L. M. Vidigal, "A new algorithm for statistical circuit design based on quasi-newton methods and function-splitting," IEEE Trans. Circuits and Syst., vol. CAS-26, pp. 784-794, Apr. 1980.

[BRA-80] R. K. Brayton and R. Spence, "Sensitivity and Optimization", Elsevier, Amsterdam, 1980.

[BRA-81] R. K. Brayton, G. D. Hachtel and A. L. Sangiovanni-Vincentelli "A Survey of optimization techniques for integrated circuit design", Proceedings of the IEEE, Nov. 1981.

[CHA-75] B. R. Chawla, H. K. Gummel and P. Kozak, "MOTIS: an MOS Timing Simulator", IEEE Trans. on Circ. and Syst., Vol. CAS-22, pp. 301-310, Dec. 1975.

[COC-77] W. G. Cochran, Sampling Techniques, (3rd ed.), New York, Wiley, 1977.

[DIR-77] S. W. Director and G. W. Hachtel, "The simplicial approximation approach to design centering," IEEE Trans. Circuits Syst., vol. CAS-24, pp. 363-372, July 1977.

[HAC-81] G. D. Hachtel and A. L. Sangiovanni-Vincentelli, "A Survey of Third Generation Simulation Techniques", Proceedings of the IEEE, pp. 124-181, Oct. 1981.

[HAM-75] J. M. Hammersly and D. C. Handscomb, "Monte Carlo Methods", Norwich, England; Fletcher, 1975.

[HOC-83] D. E. Hocevar, M. R. Lightner, and T. N. Trick, "Monte Carlo based yield

maximization with a quadratic model," in Proc. 1983 IEEE Int. Symp. Circuits and Syst., (Newport Beach, Ca.), pp 550-553, April 1983.

[HOC-83] D. E. Hocevar, M. R. Lightner, and T. N. Trick, "A study of variance reduction techniques for estimating circuit yields," in Proc. 1983 IEEE Int. Symp. Circuits and Syst., (Newport Beach, Ca.), pp 558-561, April 1983.

[KJE-69] G. Kjellstrom, "Network optimization by random variation of component values," Ericsson Technics, vol. 25, no. 3 pp. 133-151, 1969.

[KJE-75] G. Kjellstrom, L. Taxen, and L. E. Blomgren, "Optimization methods for statistical network design," in Proc. IEEE Int. Symp. Circuits Syst., (Newton, MA), pp. 321-324, Apr. 1975.

[KJE-76] G. Kjellstrom and L. Taxen, "On the efficient use of stochastic optimization in network design," in Proc. 1976 Int. Symp. Circuits and Syst., (Munich, Germany) pp. 714-717, Apr. 1976.

[KJE-81] G. Kjellstrom and L. Taxen, "Stochastic optimization in system design," IEEE Trans. Circuits and Syst., vol. CAS-28, pp. 702-715, July 1981.

[KLE-82] J. Kleckner, R. Saleh and A. R. Newton, "Electrical Consistency in Schematic Simulation", Proc. IEEE Int. Conf. on Circ. and Comp., pp. 30-34, Oct. 1982.

[KLE-83] J. Kleckner, private communication, July 1983.

[LEL-82a] E. Lelarasmee and A. L. Sangiovanni-Vincentelli, "RELAX: A New Circuit Simulator for Large Scale MOS Integrated Circuits" Proc. of the 1982 Design Automation Conf., pp. 682-690, June 1982.

[LEL-82b] E. Lelarasmee, A. E. Ruehli and A. L. Sangiovanni-Vincentelli, "The Waveform Relaxation Method for the Time Domain Analysis of Large Scale Integrated Circuits", IEEE Trans. on CAD of ICs and Syst., pp. 131-145, July 1982.

[LEU-74] K-H. Leung and R. Spence, "Efficient statistical circuit analysis," Elec. Lett., vol. 10, no. 17, pp. 377-378, 1974.

[LEU-76] K. Leung and R. Spence, "Efficient frequency-domain statistical circuit analysis," in Proc. 1976 IEEE Int. Symp. Circuits and Syst., (Munich,Germany) pp. 197-200, Apr., 1976.

[MAD-78] K. Madsen and H. Schaer-Jacobsen, "Algorithms for worst-case tolerance optimization," Proc. 1978 Int. Symp. Circuits and Syst., (New York,NY), pp. 681-685, 1978.

[MAL-82] W. Maly and A. J. Strojwas, "Statistical Simulation of the IC Manufacturing Process", IEEE Trans. on CAD of ICs and Syst., pp. 120-131, July 1982.

[MCG-73] E. J. McGrath et al, "Techniques for efficient Monte Carlo simulation", Science Applications, Incorporation, March 1973, NTIS No. AD-762-721 through 723 (U.S. Dept. of Commerce, Springfield, VA.).

[NAG-75] L. W. Nagel, "SPICE2: a computer program to simulate semiconductor circuits", University of California, Berkeley, ERL Memo No. M520, May, 1975.

[NEW-79] A. R. Newton, "Techniques for the Simulation of Large-Scale Integrated Circuits", IEEE Trans. on Circ. and Syst., Vol. CAS-26, pp. 741-749, Sept. 1979.

[OGR-80] J. Ogrodzki and M. A. Styblinski, "Optimal tolerancing, centering, and yield optimization by one-dimensional orthogonal search technique," European Conf. Circuit Theory and Design, pp. 480-485, Warsaw, Poland, Sept., 1980.

[PIN-77] J. F. Pinel and K. Singhal, "Efficient Monte Carlo computation of circuit yield using importance sampling," in Proc. 1977 Int. Symp. Circuits and Syst., (Phoenix, AZ), pp. 575-578, Apr. 1977.

[RAN-81] P. J. Rankin and R. S. Soin , "Efficient Monte Carlo yield prediction using control variates," in Proc. 1981 IEEE Int. Symp. Circuits and Syst., (Chicago,Ill), pp 143-148, Apr., 1981.

[POL-71] E. Polak, "Computational Methods in Optimization: A Computational Approach", Academic Press, 1971.

[POL-79] E. Polak and A. Sangiovanni-Vincentelli, "Theoretical and computational aspects of the optimal design centering, tolerancing, and tuning problem," IEEE Trans. Circuits Syst., vol. CAS-26, pp. 795-813, Sept. 1979.

[SAN-81] A. L. Sangiovanni-Vincentelli, "Circuit Simulation", in P. Antognetti, D.O. Pederson and H. DeMan eds., Computer Design Aids for VLSI Circuits, pp. 19-113, Sijthoff and Noordhoff, 1981.

[SCH-66] Yu. A. Schreider, "The Monte Carlo method," Pergammon Press, 1966.

[SIN-80] K. Singhal and J. F. Pinel, "Statistical design centering and tolerancing using parametric sampling," Proc. 1980 IEEE Int. Symp. Circuits and Syst., (Houston,TX), pp. 882-885, Apr. 1980.

[SOI-78] R. S. Soin and R. Spence, "Statistical design centering for electrical circuits," Electron. Lett., vol. 14, no. 24, pp. 772-774, Nov. 1978.

[SOI-79] R. S. Soin and R. Spence, "Manufacturing yield optimization by statistical exploration," Int. Conf. Comp. Aided Design & Manufacturing of Elec. Components, Circuits, & Systems, IEE Publication No. 175, pp. 154-158, July 1979.

[SOI-80] R. S. Soin and R. Spence, "Statistical exploration approach to design centering," IEE Proc. vol. 127, Part G, No. 6, pp. 260-269, Dec. 1980.

[STR-80] W. Strasz and M. A. Styblinski, "A second derivative Monte Carlo optimization of the production yield," European Conference on Circuit Theory and Design, Warsaw, Poland, pp. 121-131, Sept. 1980.

[STY-79] M. A. Styblinski, L. Opalski, and J. Ogrodzki, "An orthogonal search of the region of acceptability in tolerance problems," in Proc. Int. Symp. SPACD-CAD (Bologna, Italy) 1979.

[STY-80] M. A. Styblinski, "Estimation of yield and its derivatives by Monte Carlo and numerical integration in orthogonal subspaces," European Conference on Circuit Theory and Design, Warsaw, Poland, Sept. 1980.

[STY-81] M. A. Styblinski, J. Ogrodzki, and L. Opalski, and W. Strasz, "New methods of yield estimation and optimization and their application to practical problems," in Proc. 1981 IEEE Int. Symp. Circuits and Syst., (Chicago,Ill), pp. 131-134, Apr., 1981.

[TAH-78] K. S. Tahim and R. Spence, "Statistical circuit analysis - A practical algorithm for linear circuits," in Proc. 1978 Int. Symp. Circuits and Syst., (New York,NY), pp. 180-184, . 1978.

[TAH-78] K. S. Tahim and R. Spence, "An integrated approach to manufacturing yield estimation and design centering," in Proc. ECCTD

[TAH-79] K. S. Tahim and R. Spence, "A radial exploration approach to manufacturing yield estimation and design centering," IEEE Trans. Circuits Syst., vol. CAS-26, pp. 768-774, Sept. 1979.

[TAH-80] K. S. Tahim and R. Spence, "A radial exploration algorithm for the statistical analysis of linear circuits," IEEE Trans. Circuits and Syst., vol. CAS-27, pp. 421-425, May 1980.

[WHI-83] J. White and A. L. Sangiovanni-Vincentelli, "RELAX II: A New Waveform Relaxation Approach for the Analysis of LSI MOS Circuits", Proc. 1983 Int. Symp. on Circ. and Syst., May 1983.

B. Consolidated List of JSEP Published Papers and Memorandums through 31 August 1983

Published

M. J. Chen C. A. Desoer	1983	"The problem of guaranteeing robust disturbance rejection in linear multivariable feedback systems," *Int. J. Control*, v. 37, n. 2, pp. 305-313.
N. P. Chen C. P. Hsu E. S. Kuh	8/83	"The Berkeley building-block (BBL) layout system for VLSI design," *Proceedings of the IFIP TC 10/WG 10.5 International Conference on Very Large Scale Integration*, pp. 37-44.
S. Hubbell D. J. Angelakos	8/83	"A technique for measuring the effective dielectric constant of a microstrip line," *IEEE Trans. on Microwave Theory and Techniques*, v. MTT-31, n. 8, pp. 687-688.
T. S. Parker L. O. Chua	8/83	"A computer-assisted study of forced relaxation oscillations," *IEEE Trans. on Circuits and Systems*, v. CAS-30, n. 8, pp. 518-533.
D. F. Williams S. E. Schwarz	7/83	"Design and performance of coplanar waveguide bandpass filters," *IEEE Trans. on Microwave Theory and Techniques*, v. MTT-13, n. 7, pp. 558-566.
H. K. Choi S. Wang	6/83	"GaAs/(GaAl)As deep Zn-diffused channeled-substrate laser," *J. of Appl. Phys.*, v. 54, n. 6, pp. 3600-3602.
B. Nye A. Sangiovanni-Vincentelli J. Spoto A. Tits	5/83	"DELIGHT SPICE: An optimization-based system for the design of integrated circuits," *IEEE Proceedings of the Custom Integrated Circuits Conference*, pp. 233-238.
M. Odyniec L. O. Chua	5/83	"Josephson-junction circuit analysis via integrated manifolds," *IEEE Trans. on Circuits and Systems*, v. CAS-30, n. 5, pp. 308-320.
A. Antreasyan S. Wang	4/83	"Semiconductor integrated etalon interference laser with a curved resonator," *Appl. Phys. Lett.*, v. 42, n. 7. pp. 562-564.

H. K. Choi S. Wang	4/83	"GaAs/GaAlAs active-passive-interference laser," *Electronics Letters*, v. 19, n. 8, pp. 302-303.
L. O. Chua R. L. P. Ying	3/83	"Canonical piecewise-linear analysis," *IEEE Trans. on Circuits and Systems*, v. CAS-30, n. 3, pp. 125-140.
E. Polak D. Q. Mayne Y. Wardi	3/83	"On the extension of constrained optimization algorithms from differentiable to nondiferentiable problems," *SIAM J. Control, and Optimization*, v. 21, n. 2, pp. 179-203.
P. F. Byrne	2/83	"High energy ion implantation effects in silicon," *J. Appl. Phys.*, v. 54, n. 2, pp. 1146-1147.
T. Wang S. E. Schwarz	2/83	"Design of dielectric ridge waveguides for millimeter-wave integrated circuits," *IEEE Trans. on Microwave Theory and Techniques*, v. MTT-31, n. 2, pp. 128-134. v. MTT-31, n. 2, pp. 128-134.
D. S. Kuo C. Hu M. H. Chi	1/83	"dV/dt breakdown in power MOSFET's," *IEEE Electron Device Letters*, v. EDL-4, n. 1, pp. 1-2.
D. J. Angelakos R. K. Najm	1982	"Bistatic scattering from objects with constrained current flow," *Electromagnetics*, v. 2, pp. 355-362.
P. F. Byrne N. W. Cheung D. K. Sadana	1982	"Megavolt arsenic implantation into silicon," *Thin Solid Films*, v. 95, pp. 363-367.
M. J. Chen C. A. Desoer	1982	"Necessary and sufficient condition for robust stability of linear distributed feedback systems," *Int. J. Control*, v. 35, n. 2, pp.255-267.
L. O. Chua R. L. P. Ying	1982	"Finding all solutions of piecewise-linear circuits," *Circuit Theory and Applications*, v. 10, pp. 201-229.
E. Polak	1982	"A recursive quadratic programming algorithm for semi-infinite optimization problems," *Applied Mathematics and Optimization*, v. 8, pp. 325-349.

N.-L. Wang S. E. Schwarz	1982	"Planar oscillators for monolithic integration," *International Journal Infrared and Millimeter Waves*, v. 3, n. 6, pp. 771-782.
S. Wang S. E. Schwarz	1982	"Novel semiconductor lasers for integrated optics," *SPIE*--Integrated Optics and Millimeter and Microwave Integrated Circuits, v. 317, pp. 93-98.
P. R. Gray R. G. Meyer	12/82	"MOS operational amplifier design--a tutorial overview," *IEEE Journal of Solid-State Circuits*, v. SC-17, n. 6, pp.969-982. of Solid-State Circuits, v. SC-17, n. 6.
S. K. Lui R. G. Meyer	8/82	"A high-frequency bipolar JFET I^2L process," *IEEE Trans. on Electron Devices*, v. ED-29, n. 8, pp. 1319-1323.
V. Borkar P. Varaiya	7/82	"Identification and adaptive control of Markov chains," *SIAM J. Control and Optimization*, v. 20, n. 4, pp. 470-489.
E. Lelarasmee A. E. Ruehli A. L. Sangiovanni-Vincentelli	7/82	"The waveform relaxation method for time-domain analysis of large scale integrated circuits," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, v. CAD-1, n. 3, pp. 131-145.
A. R. Bergen L. O. Chua A. I. Mees E. W. Szeto	6/82	"Error bounds for general describing function problems," *IEEE Trans. on Circuits and Systems*, v. CAS-29, n. 6, pp. 345-354.
E. Polak	5/82	"An implementable algorithm for the optimal design centering, tolerancing, and tuning problem," *Journal of Optimization Theory and Applications*, v. 37, n. 1, pp. 45-67.
A. E. Comer R. S. Muller	5/82	"A new ZnO-on-Si convolver structure," *IEEE Electron Device Letters*, v. EDL-3, n. 5, pp. 118-120.

H. K. Choi S. Wang	4/82	"Semiconductor internal-reflection-interference laser," *Appl. Phys. Letters*, v. 40(7), pp. 571-573.
S. Wang H. K Choi I. H. A. Fattah	4/82	"Studies of semiconductor lasers of the interferometric and ring types," *IEEE J. of Quantum Electronics*, v. QE-18, n. 4, pp. 610-617.
M. Marek-Sadowska E. S. Kuh	1981	"A new approach to routing of two-layer printed circuit board," *Circuit Theory and Applications*, v. 9, pp. 331-341.
M. J. Chen C. A. Desoer G. F. Franklin	12/81	"Algorithm design of single-input single-output systems with a two-input one-output controller," *The 20th IEEE Conference on Decison and Control*, pp. 133-136.
K.-C. Hsieh P. R. Gray D. Senderowicz D. G. Messerschmitt	12/81	"A low-noise chopper-stabilized differential switched-capacitor filtering technique," *IEEE Journal of Solid-State Circuits*, v. SC-16, n. 6, pp.708-715.
Y.-C. Lin A. R. Neureuther	11/81	"Alignment signals from resist-coated marks for direct wafer writing," *IEEE Trans. on Electron Devices*, v. ED-28, n. 11, pp. 1397-1405.
R. C. Ruby T. Van Duzer	11/81	"Silicon-coupled Josephson junctions and super-Shottky diodes with coplanar electrodes," *IEEE Trans. on Electron Devices*, v. ED-28, n. 11, pp. 1394-1397.
R. Saeks A. Sangiovanni-Vincentelli V. Visvanathan	11/81	"Diagnosability of nonlinear circuits and systems--Part II: dynamical systems," *IEEE Trans. on Computers*, v. C-30, n. 11, pp. 899-904.
V. Visvanathan A. Sangiovanni-Vincentelli	11/81	"Diagnosability of nonlinear circuits and systems--Part I: the dc case," *IEEE Trans. on Computers*, v. C-30, n. 11, pp. 889-898.
C. W. Chen T. K. Gustafson	8/81	"A phototransistor with concentric electrodes on the Si substrate,"

IEEE Electron Device Letters, v. EDL-2, n. 8, pp. 200-202.

C. W. Chen, T. K. Gustafson — 7/81 — "Characteristics of an avalanche phototransistor fabricated on a Si surface," *Appl. Phys. Letters*, v. 39(2), pp. 161-163.

C. Drowley, C. Hu — 6/81 — "Arsenic-implanted Si layers annealed using a CW Xe arc lamp," *Appl. Phys. Letters*, 38(11), pp. 876-878.

T. Matsumoto, L. O. Chua, H. Kawakami, S. Ichiraku — 5/81 — "Geometric properties of dynamic Nonlinear networks: transversality, local-solvability and eventual passivity," *IEEE Trans. on Circuits and Systems*, v. CAS-28, n. 5, pp. 406-428.

C. A. Desoer, M. J. Chen — 4/81 — "Design of multivariable feedback systems with stable plant," *IEEE Trans. on Automatic Control*, v. AC-26, n. 2, pp. 408-415.

S. Wang, C.-Y. Chen, A. S.-H. Liao, L. Figueroa — 4/81 — "Control of mode behavior in semiconductor lasers," *IEEE J. of Quantum Electronics*, v. QE-17, n. 4, pp. 453-468.

D. B. Rutledge, S. E. Schwarz — 3/81 — "Planar multimode detector arrays for infrared and millimeter-wave applications," *IEEE J. of Quantum Electronics*, v. QE-17, n. 3, pp. 407-414.

C. Y. Chen, S. Wang — 2/81 — "Effects of the current distribution on the characteristics of the semiconductor laser with a channeled-substrate planar structure," *J. of Appl. Phys.*, v. 52(2), pp. 614-620.

J. L. Wyatt, Jr., L. O. Chua, J. W. Gannett, I. C. Goknar, D. N. Green — 1/81 — "Energy concepts in the state-space theory of nonlinear n-ports: Part I passivity," *EEE Trans. on Circuits and Systems*, v. CAS-28, n. 1, pp. 48-61.

C. H. Sequin — 1980 — "Special feature: instruction in MOS LSI systems design," *IEEE Computers*, pp. 67-73.

C. D. Hartgring — 1980 — "A MESFET model for circuit

W. G. Oldham T.-Y. Chiu		analysis," *Solid-State Electronics*, v. 23, pp. 121-126.
P. Varaiya J. Walrand	1980	"A minimum principle for decentralized stochastic control problems," *Dynamic Optimization and Mathematical Economics*, ed. Pan-Tai Liu, pp. 253-266.
R. W. Coen R. S. Muller	1980	"Velocity of surface carriers in inversion layers on silicon," *Solid-State Electronics*, v. 23, pp. 35-40.
S. K. Lui R. G. Meyer	12/80	"High frequency bipolar - JFET -I^2L process," *International Electron Devices Meeting*, pp. 382-385.
C. W. Chen T. K. Gustafson	12/80	"A high-speed Si lateral photodetector fabricated over an etched interdigital mesa," *Appl. Phys. Letters*, 37(11), pp. 1014-1016.
C.-Y. Chen S. Wang	8/80	"Near-field and beam-waist position of the semiconductor laser with a channeled-substrate planar structure," *Appl. Phys. Letters*, 37(3), pp. 257-260.
A. N. Payne E. Polak	6/80	"An interactive rectangle elimination method for bi-objective decision making," *IEEE Trans. on Automatic Control*, v. AC-25, n. 3.
C. A. Desoer R.-W. Liu J. Murray R. Saeks	6/80	"Feedback system design: the fractional representation approach to analysis and synthesis," *IEEE Trans. on Automatic Control*, v. AC-25, n. 3.
L. O. Chua D. J. Curtin	5/80	"Synthesis of reciprocal piecewise-linear n-port resistors," *IEEE Trans. on Circuits and Systems*, v. CAS-27, n. 5.
D. B. Rutledge S. E. Schwarz T.-L. Hwang D. J. Angelakos K. K. Mei S. Yokota	5/80	"Antennas and waveguides for far-infrared integrated circuits," *IEEE J. of Quantum Electronics*, v. QE-16, n. 5.

C. A. Desoer Y.-Y. Wang	4/80	"On the generalized Nyquist stability criterion," *IEEE Trans. on Automatic Control*, v. AC-25, n. 2, pp. 187-196.
Y.-C. Lin I. Adesida A. R. Neureuther	4/80	"Monte Carlo simulation of registration signals for electron beam microfabrication," *Appl. Phys. Letters*, v. 36, n. 8.
C.-Y. Chen S. Wang	4/80	"Narrow double-current-confinement channeled-substrate planar laser fabricated by double etching technique," *Appl. Phys. Letters*, v. 36, n. 8.
C.-Y. Chen S. Wang	3/80	"Double-etching technique for the fabrication of submicron channels on a GaAs wafer and its application to laser fabrication," *J. Appl. Phys.*, v. 51, n. 3, pp. 1802-1808.
C. A. Desoer Y.-T. Wang	2/80	"Foundations of feedback theory for nonlinear dynamical systems," *IEEE Trans. on Circuits and Systems*, v. CAS-27, n. 2, pp. 104-123.
C. A. Desoer Y. T. Wang	1979	"The robust non-linear servomechanism problem," *Int. J. on Control*, v. 29, n. 5, pp. 803-828.
M. Mansour E. I. Jury L. F. Chaparro	1979	"Estimation of the margin of stability for linear continuous and discrete systems," *Int. J. Control*, v. 30, n. 1, pp. 49-69.
Y. C. Lin T. E. Everhart	12/79	"Study on voltage contrast in SEM," *J. Vac. Sci. Technol.*, v. 16, n. 6, pp. 1856-1860.
V. Borkar P. Varaiya	12/79	"Adaptive control of Markov chains, I: finite parameter set," *IEEE Trans. on Auto. Control*, v. AC-24, n. 6, pp. 953-957.
K. Youssefi E. Wong	10/79	"Query processing in a relatinal database management system," *Very Large Data Bases, Fifth Internatinal Conference on Very Large Data Bases*, Rio de Janeiro, Brazil, pp. 409-417.
E. I. Jury	10/79	"Remark on an equivalent

L. F. Chaparro		relation in least square approximation," *Proceedings of the IEEE*, v. 67, n. 10, pp. 1444-1445.
E. Polak A. Sangiovanni-Vincentelli	9/79	"Theoretical and computational aspects of the optimal design centering, tolerancing, and tuning prolem," *IEEE Trans. on Circuits and Systems*, v. CAS-26, n. 9, pp. 795-813.
C. Gonzaga E. Polak	7/79	"On constraint dropping schemes and optimality functions for a class of outer approximations algorithms," *SIAM J. Control and Optimization*, v. 17, n. 4, pp. 477-493.
S.-H. Kwan C. T. Chuang R. S. Muller R. M. White	7/79	"Dual-gate depletion-mode DMOS transistor for linear gain-control application," *IEEE Trans. on Electron Devices*, v. ED-26, n. 7, pp. 1053-1058.
P. A. S. Veloso	6/79	"Some remarks on multiple-entry finite automata," *J. of Comp. and System Sciences*, v. 18, n. 3, pp. 304-306.
J. M. P. Guedes S. W. Slayman T. K. Gustafson R. K. Jain	6/79	"Internal photoemission in Ag-Al_2O_3-Al junctions," *IEEE J. of Quantum Electronics*, v. QE-15, n. 6, pp. 475-481.
T.-L. Hwang S. E. Schwarz D. B. Rutledge	6/79	"Microbolometers for infrared detection," *Appl. Phys. Letters*, v. 34, n. 11, pp. 773-776.
Y. Yasuoka M. Heiblum T. K. Gustafson	6/79	"Coupling to an 'edge metal-oxide-metal' junction via an evaporated long antenna," *Appl. Phys. Letters*, 34(12), pp. 823-825.
E. Polak D. Q. Mayne	6/79	"On the finite solution of nonlinear inequalities," *IEEE Trans. on Automatic Control*, v. AC-24, n. 3, pp. 443-445.
D. W. Tsang	5/79	"Transport theory of high-

S. E. Schwarz		frequency rectification in Schottky barriers," *J. Appl. Phys.*, 50(5), pp. 3459-3471.

Memorandum

W. T. Nye	M83/33	"DELIGHT: An interactive system for optimization-based engineering design."
S. Boyd S. Sastry	M83/38	"Persistent behavior, sufficient richness and parameter convergence in adaptive control."
T. Nishi L. O. Chua	M83/21	"Topological criteria for non-linear resistive circuits containing sources to have a unique solution."
E. Polak	M83/16	"optimization-based design of SISO control systems with uncertain plant: problem formulation."
M. Odyniec L. O. Chua	M83/15	"Integral manifolds for nonlinear circuits."
M. Odyniec L. O. Chua	M83/12	Josephson junction circuit analysis via integral manifolds: Part II."
E. Polak	M83/11	"A modified Nyquist stability test for use in computer-aided design."
N. P. Chen C. P. Hsu E. S. Kuh	M83/10	"Berkeley building-block layout system for VLSI design."
D. Q. Mayne E. Polak	M82/87	"Non-differentiable optimization via adaptive smoothing."
T. S. Parker L. O. Chua	M82/81	"A computer-assisted study of forced relaxation oscillations."
C. A. Desoer	M82/79	"Simultaneous stabilization of nonlinear systems."
P. F. Byrne	M82/82	"Megavolt arsenic implantation

		into silicon."
E. Polak	M82/50	"Semi-infinite optimization in engineering design."
W. Nye A. Tits	M82/55	"DELIGHT for beginners."
G. DeMicheli A. Sangiovanni-Vincentelli	M82/57	"PLEASURE: A computer program for PLA simple/ multiple constrained/unconstrained reward column folding."
E. Polak D. Q. Mayne	M82/34	"Algorithm models for nondifferentiable optimization."
K. C. Hsieh	M82/39	"Noise limitations in switched-capacitor filters."
E. Lelarasmee	M82/40	"The waveform relaxation method for time domain analysis of large scale integrated circuits: theory and applications."
M. Odyniec L. O. Chua	M82/46	"Josephson junction circuit analysis via integral manifolds."
E. Polak Y. Y. Wardi	M82/22	"A study of minimizing sequences."
L. O. Chua E. W. Szeto	M82/27	"Higher-order nonlinear circuit elements: circuit theoretic properties."
L. O. Chua E. W. Szeto	M82/17	"Synthesis of higher-order nonlinear circuit elements."
L. O. Chua E. W. Szeto	M82/18	"State space theory of nonlinear two terminal higher-order elements."
E. Polak K. J. Astrom D. Q. Mayne	M81/99	"Interoptdyn-Siso: A tutorial."
E. Polak A. L. Tits	M81/91	"On globally stabilized quasi-newton methods for inequality constrained optimization problems."
M. Marek-Sadowska E. S. Kuh	M81/95	"A new approach to channel routing."
E. Lelarasmee	M81/75	"The waveform relaxation

A. E. Ruehli A. Sangiovanni-Vincentelli		method for time domain analysis of large scale integrated circuits."
E. Polak D. Q. Mayne Y. Wardi	M81/78	"On the extension of constrained optimization algorithms from differential to nondifferential problems."
M. Stonebraker J. Woodfill J. Ranstrom M. Murphy M. Meyer E. Allman	M81/62	"Performance enhancement to a relational data base system."
T. Lee W. Nye A. Tits	M81/69	"The design of digital filters using interactive optimization."
K. C. Hsieh P. R. Gray D. Senderowicz D. G. Messerschmidt	M81/52	"Noise reduction techniques for switched capacitor filters."
C. A. Desoer M. J. Chen	M81/58	"Necessary and sufficient conditions for robust stability of linear distributed feedback systems."
V. Visvanathan	M81/45	"Fault diagnosis of nonlinear circuits and systems: Part I-the DC case."
W. T. Nye E. Polak A. Sangiovanni-Vincentelli A. Tits	M81/19	"Delight: an optimization-based computer-aided design systems."
M. J. Chen C. A. Desoer G. Franklin	M81/12	"Algorithm design of single-input single-output systems with a two-input one-output controller."
E. Polak A. L. Tits	M80/50	"A recursive quadratic programming algorithm for semi-infinite optimization problems."
W. T. Nye	M80/23	"Dynamic arrays via a modified ratfor preprocessor."
M. A. Bhatti T. Essebo W. Nye	M80/14	"A software system for optimization based interactive computer-aided design."

K. S. Pister E. Polak A. Sangiovanni-Vincentelli A. Tits		
C. A. Desoer M. J. Chen	M80/13	"Design of multivariable feedback system with stable plant."
V. Borkar P. Varaiya	M79/69	"Identification and adaptive control of Markov Chains."
E. Polak A. L. Tits	M79/52	"A globally convergent implementable multiplier method with automatic limitation."
E. Polak D. Q. Mayne	M79/48	"Algorithms for computer aided design of control systems by the method of inequalities."
R. W. Coen R. S. Muller	M79/36	"A uniform channel IGFET."
E. Polak	M79/33	"An implementable algorithm for the optimal design centering, tolerancing and tuning problem."
D. J. Allstot	M79/30	"MOS switched capacitor ladder filters."

END

FILMED

1-84

DTIC