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DNA 6189T

AD-A 135 814

# ANALYSIS AND TESTING OF RADIATION-INDUCED TRANSIENT EFFECTS IN COMPLEX MICROCIRCUITS

James P. Raymond  
Mission Research Corporation, San Diego  
5434 Ruffin Road  
San Diego, California 92123

1 June 1982

Topical Report for Period 28 January 1980-1 June 1982

CONTRACT No. DNA 001-80-C-0140

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER DNA 6189T	2. GOVT ACCESSION NO. ADA135 814	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) ANALYSIS AND TESTING OF RADIATION-INDUCED TRANSIENT EFFECTS IN COMPLEX MICROCIRCUITS	5. TYPE OF REPORT & PERIOD COVERED Topical Report for Period 28 Jan 80 - 1 Jun 82	
	6. PERFORMING ORG. REPORT NUMBER MRC/SD-N-72	
7. AUTHOR James P. Raymond	8. CONTRACT OR GRANT NUMBER(S) DNA 001-80-C-0140	
9. PERFORMING ORGANIZATION NAME AND ADDRESS Mission Research Corporation, San Diego 5434 Ruffin Road San Diego, California 92123	10. PROGRAM ELEMENT PROJECT TASK AREA & WORK UNIT NUMBERS Subtasks X99QAXVB201-02 and Q31QAXVB201-01	
11. CONTROLLING OFFICE NAME AND ADDRESS Director Defense Nuclear Agency Washington, D.C. 20305	12. REPORT DATE 1 June 1982	
	13. NUMBER OF PAGES 130	
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. of this report UNCLASSIFIED	
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A since UNCLASSIFIED	
16. DISTRIBUTION STATEMENT of this Report Approved for public release, distribution unlimited.		
17. DISTRIBUTION STATEMENT of the abstract entered in Block 20, if different from Report		
18. SUPPLEMENTARY NOTES This work was sponsored by the Defense Nuclear Agency under RDT&E RMSS Codes B323080464 X99QAXVB20102 H2590D and X323080469 Q31QAXVB20101 H2590D.		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Transient radiation effects                      Secondary photocurrent Microcircuits                                      Short-term annealing Photoresponse                                      Radiation effects testing Single event upset                                  Radiation-inclusive transistor models Primary photocurrent		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) Analytical and experimental considerations in assessing transient effects of microcircuits exposed to a pulsed radiation environment are summarized tutorially with extensive references. The report represented the notes associated with lectures given at the 1981 and 1982 IEEE Radiation Effects Conference Short Course.		

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## 1. INTRODUCTION

Radiation effects on electronics are typically considered in terms of permanent damage and transient response. In general, however, damaging effects have a time-dependence (short-term annealing) and the transient response may result in permanent damage to a component (burn-out). The original definition of TREE (i.e., Transient Radiation Effects on Electronics) refers to the transient radiation of the nuclear weapon environment.

### 1.1 Scope (Figure 1)

In this review the transient effects of transient ionizing radiation on complex microcircuits will be presented from the perspectives of both analysis and testing. The principal emphasis will be on understanding the array response in terms of basic effect on the array elements. Appreciating the nature of cause and effect can then be instrumental in interpreting analytical and experimental assessments in arrays of evolving technology and function. The overall transient response of a microcircuit can appear mysterious and esoteric. In this review we will start from the critical effects in the basic microcircuit elements, illustrate these effects in basic circuits and then discuss the overall complex array.

Radiation environments considered will be those resulting in both bulk ionization throughout the semiconductor and local ionization from a single high energy particle. The concern for bulk ionizing radiation effects results from the requirement to harden military systems to a high intensity pulsed ionizing radiation exposure. System techniques have been developed to allow transient upset of semiconductor microcircuits with minimum degradation in system performance. This then leads to the dual concern of defining the radiation level which results in transient upset, and establishing recovery of electrical performance after exposure to a higher intensity ionizing radiation pulse. These two perspectives will be considered as the low-level and high-level photoresponse.

## **TRANSIENT IONIZING RADIATION EFFECTS**

- **Environments**

  - Bulk Ionization**

  - Single Particle Local Ionization**

- **Low-level Photoresponse/Upset**

- **High-level Survivability**

- **Radiation-induced Latch-up**

- **Short-term Annealing (Notes)**

**FIGURE 1. SCOPE.**

Transient effects similar in response to the high-intensity photo-response can also result from the ionization track of a single particle in a critical volume of the semiconductor device. This single event radiation effect is of major concern in the development of complex memory chips, where alpha particles released by radioactive decay of trace elements in the package can result in "soft error" rates which compromise the stored data and overall memory performance. Single event radiation effects can also be observed, however, in terrestrial satellites exposed to the natural space environment, and are a significant concern in new, very high density, VLSI arrays. Bulk ionization and local ionization effects have been merged in this review to highlight critical commonality and difference in the two effects.

A critical concern for both bulk and local ionization effects is the issue of radiation-induced latch-up. In almost all junction-isolated microcircuit a small, but significant possibility exists that a low-voltage, high current parasitic path could be initiated by the radiation exposure. This "latch-up" path can, in the best case, inhibit normal circuit operation until the power supply voltage is interrupted and restored, or, in the worst case can cause microcircuit burn-out.

The final issue in transient ionizing radiation effects is that of transient annealing of the permanent degradation of trapped oxide charge. The time dependence of the annealing of "permanent" damage can be within the electrical sensitivity of the system and therefore is a transient as well as permanent degradation effects. Study of transient annealing effects is presently concentrated on basic device studies and will be omitted from this review on complex microcircuit effects. A brief discussion and references have been included in the notes.

## 1.2 Role of Test and/or Analysis

The relative roles of test and analysis have developed with the understanding of basic radiation effects and the evolution of semiconductor component technology. Analysis and test must coexist in any reasonable evaluation. On one extreme even the "pure" analytical simulation relies on experimental data for model parameter values and on the other extreme the "empirical" experimental evaluation must be extrapolated to the "threat" environment by analysis. Historically, the initial assessment of critical effects in diode and transistors was experimental. That was followed by analytical insight that has led to a mature capability for the analytical simulation of discrete component circuits. As component complexity has increased the resources required for a complete analysis have become prohibitive and experimental characterization has become more practical. With the complexity of today's microcircuits, I believe that the resources for either a predominately experimental or analytical evaluations are far beyond those available within a hardened system development. Confident evaluation of complex microcircuit effect now must rely on both analysis and testing: analysis to identify the worst-case test conditions and interpret the experimental data and testing to quantitatively establish transient upset levels and survivability.

## 2. FUNDAMENTAL CONCEPTS

The transient response of a complex microcircuit is the result of free carrier generation in the bulk semiconductor. The excess carriers move in the semiconductor under the force of built-in electric fields and density gradients (diffusion) creating transient junction currents. The transient junction currents, in turn, interact to produce an overall device response which is reflected in the overall circuit and array response. The basic concepts then are:

- a) carrier generation in the bulk semiconductor
- b) junction transient currents
- c) direct junction interactions.

In those cases where the radiation flux is very high and carrier generation is essentially uniform the junction transient photocurrent is generally referred to as the diode primary photocurrent. Direct interaction between junctions can be related to bipolar transistor current gain and enhancement of the diode primary photocurrent is referred to as the transistor secondary photocurrent. Effects of localized ionization from single high energy particle are distinguished by referring to the junction response as the diode transient current.

A good understanding of these basic effects can be applied directly to understanding the nature of basic circuit response within the array which, in turn, can be instrumental in accurate interpretation of experimental results as well as guiding the definition of test conditions which will establish the worst-case array susceptibility.

## 2.1 Basic Ionizing Radiation Effects in Bulk Silicon

Radiation, in any form, produces a free hole-electron pair with the deposition of 3.6 eV by ionization in silicon<sup>1</sup>. For many years the principal concern of the bulk ionizing radiation effects has been the transient effects resulting from exposure to pulsed, high flux, high energy radiation environments. In this case, the ionization produced by a single particle or photon is small, but the aggregate effects may be large. These high flux environments are generally those associated with a nuclear weapon but may also include a brief reactor exposure or the transit through a planetary radiation belt. More recently, the sensitivity of microcircuits has increased to the point where a single high energy particle can create sufficient ionization to result in a critical microcircuit effect. Single particle transient effects are known as soft errors or single event upset.

### 2.1.1 Bulk Ionizing Radiation Effects

Traditionally, bulk ionizing effects are considered as the generation of hole-electron pairs uniformly throughout the bulk semiconductor at a rate proportional to the ionizing radiation intensity. A measure of the energy deposited by high energy photons is the mass absorption coefficient shown as a function of energy in Figure 2<sup>2</sup>. The mechanics of ionization from a photon is the energy loss from electrons produced from a primary photon-electron interaction. For a 1 MeV gamma ray, a typical Compton interaction produces a 600 keV electron and degrades the photon energy to 400 keV. The electron losses energy at an initial rate of approximately 45 MeV/cm<sup>1</sup>. The thickness of a typical semiconductor device, however, is on the order of 0.02 cm. The electron then passes through the device depositing less than 90 keV or generating 25,000 hole-electron pairs. From the absorption coefficient then energy deposited by the gamma ray spectrum is an arithmetic average of approximately 1500 eV or 520 electron-hole pairs. There is no interaction of this kind but rather it is the average including the low probability high energy event and the more probable passage of the gamma ray with no effect. The point is that significant transient effects from high energy photons are the result of high radiation flux generating carriers uniformly through the bulk semiconductor.

The mass absorption coefficient for gold has been included in Figure 2 to illustrate that energy deposited in the metals intimate with the semiconductor can influence the energy deposited in the semiconductor. Electrons all produced in the metal at a higher rate than in the silicon and some of these electrons deposit then energy in the semiconductor. Thus, the ionizing radiation dose in the device may be enhanced by the thin layer of metal. Dose enhancement effects are discussed in detail in References 3-5.

A major simplification in bulk ionizing radiation effects is consideration and specification directly in terms of energy absorbed by ionization, independent of how the energy was deposited. The absorbed radiation

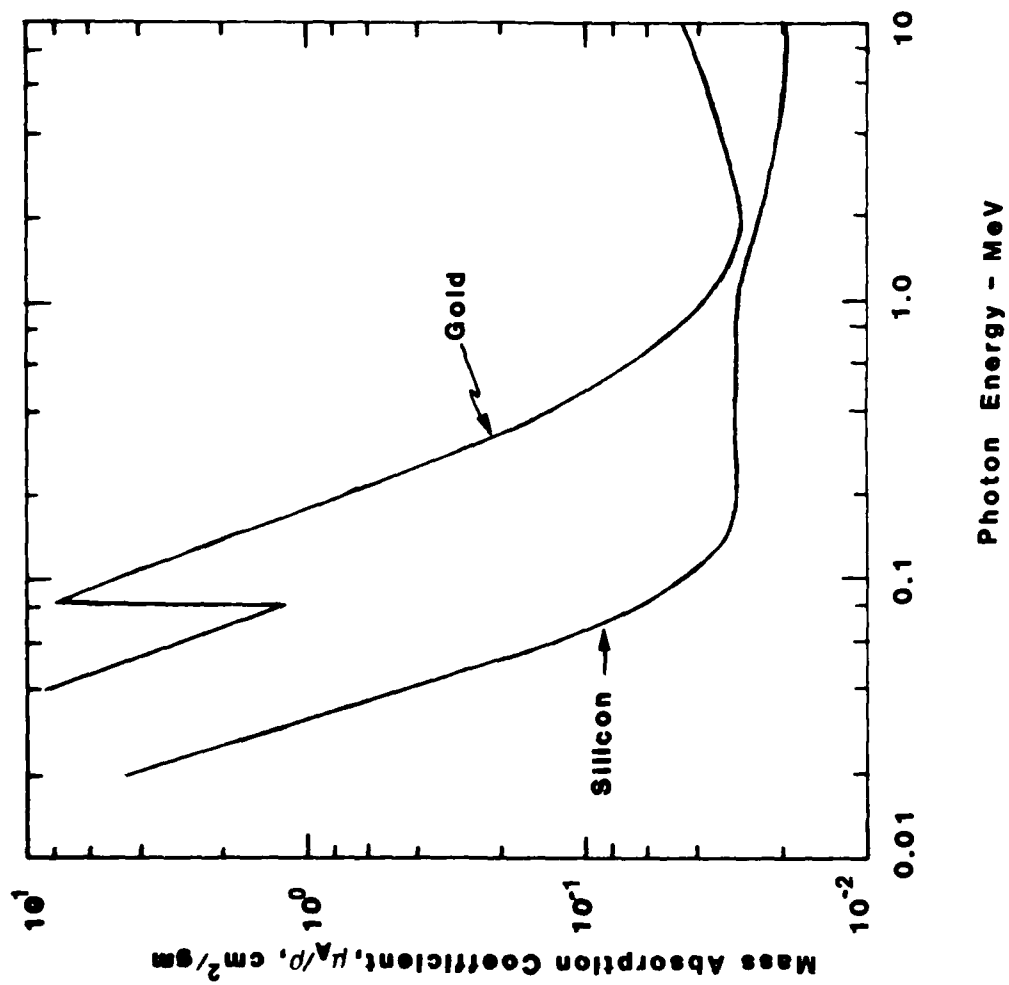


FIGURE 2. PHOTON ENERGY DEPOSITION IN MICROCIRCUIT MATERIALS.

intensity of an ionizing radiation environment can be measured with either a calibrated sample of semiconductor material,<sup>6</sup> a simple p-i-n diode, or CaF/LiF thermoluminescent (TLD) powder. The unit used for absorbed radiation intensity is the "rad" (radiation absorbed dose) which is defined as 100 ergs of absorbed energy per gram of material, or the "Gray" which is defined as 1 Joule of absorbed energy per kilogram of material (1 Gray (Si) = 100 rads(Si)). Since the generation of a single hole-electron pair in silicon requires approximately 3.6 eV, the radiation induced carrier generation rate is (by definition)

$$g(t) = g_0 \dot{\gamma}(t) \quad (1)$$

where,

$$g_0 = 4 \times 10^{13} \text{ hole-electron pairs/cm}^3\text{-rad (silicon)}$$

and

$$\dot{\gamma}(t) = \text{time-dependent absorbed ionizing radiation, rads(Si)/s}$$

A further simplification in the consideration of the transient photoresponse of a semiconductor device is that, for the high energy radiation of space, reactor and nuclear weapon environments, the material absorption lengths are generally much greater than the semiconductor device dimensions. The energy deposited in the device will be approximately uniform throughout and independent of orientation to the direction of exposure.

Carrier distribution in bulk semiconductors exposed to a pulsed ionizing radiation environment can be described by considering the carrier continuity equations in the presence of a radiation carrier generation rate,  $g(t)$ .

Considering an isolated, one-dimensional semiconductor region, the continuity equations of carrier flow become,



$$\frac{dn}{dt} = g(t) - \frac{(n - n_p)}{\tau_p} \quad (2)$$

Solution of even these simplified equations depends on the nature of the carrier lifetimes. In the simplest case the electron and hole lifetimes will be dominated by the minority carrier lifetime and will be constant over the range of carrier densities of interest. For n-type material we would then have,

$$\tau_n = \tau_p = \text{constant}$$

and the change in carrier density resulting from a step radiation environment as shown in Figure 3 is,

$$\Delta n = \Delta p = g_0 \dot{\gamma} [1 - \exp(-t/\tau_p)] \quad (3)$$

The changes in majority and minority carrier densities are equal. Relative effects will be much greater, therefore, on the minority carrier density than on the majority carrier density. The minority carrier density effects result in the junction photocurrent and secondary photocurrents in diodes and transistors. These effects will be discussed in detail in the next section. The increase in carrier density in the semiconductor increases the conductivity by

$$\Delta\sigma = q \Delta n (\mu_n + \mu_p) \quad (4)$$

The increase in conductivity is significant when the radiation-induced carrier density is comparable to the equilibrium majority carrier density. Conductivity modulation effects are usually dominated by the junction photocurrents, but are important in the observed results in junction field-effect transistors, diffused resistor elements of integrated

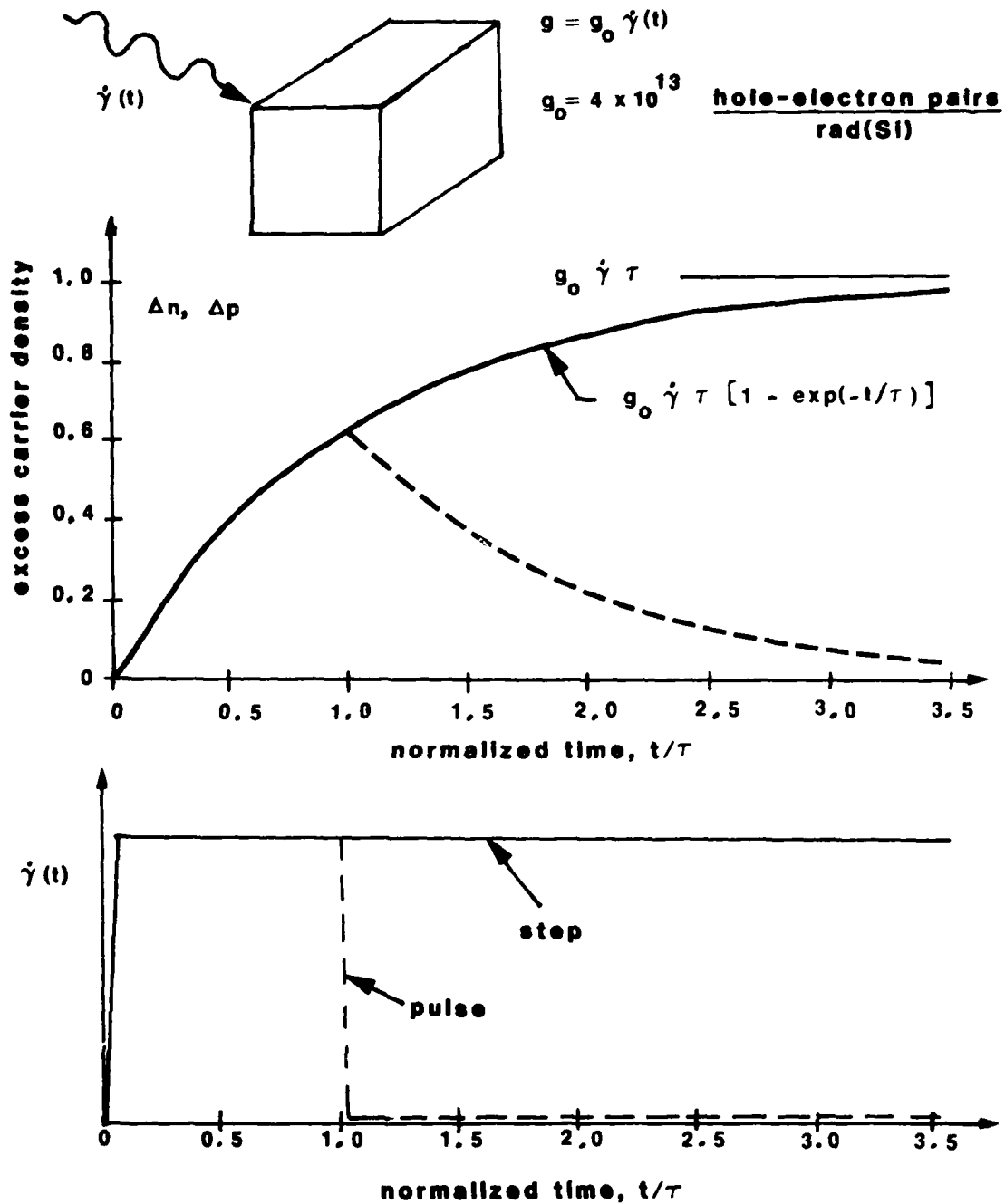


FIGURE 3. IONIZING RADIATION-INDUCED CARRIER GENERATION.

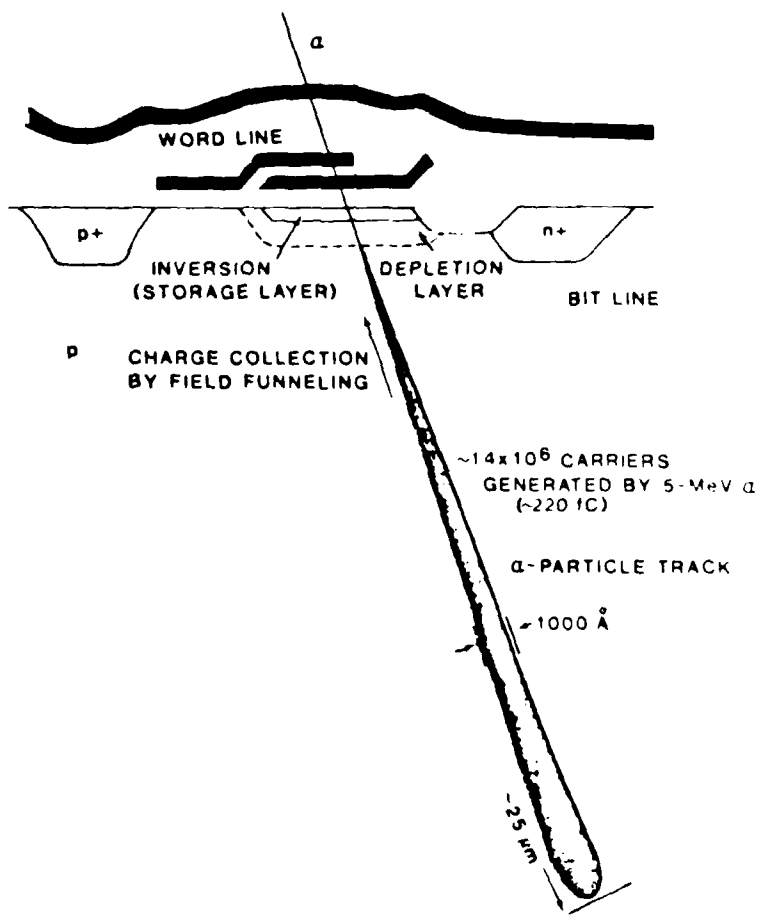
circuits, and junction diodes which are strongly forward biased. Conductivity modulation in bulk semiconductors has been used to study radiation-induced carrier generation and carrier recombination processes. The technique is especially useful in the study of neutron irradiated, damaged material<sup>6</sup>.

### 2.1.2 Localized Ionizing Radiation Effects

With the evolution of microcircuit technology, the electrical energy (for example, as charge in a dynamic n-MOS memory) committed to internal digital information has decreased dramatically. This trend has become an important concern because it was observed that information stored in dynamic MOS memories was being lost at an alarming frequent rate by "soft errors".<sup>7</sup> The soft errors were loss of stored data in the memory but with no apparent degradation of overall memory performance when the data were re-written. These soft errors are now understood to be the effect of the ionization track of a single high-energy alpha particle as illustrated in Figure 4. The alpha particles result from the radioactive decay of trans-uranic trace elements in the semiconductor ceramic package.

The popularization of concern over soft error effects due to trace materials in the array ceramic package reinforced concerns over possible effects due to cosmic rays and nuclear particles.<sup>8,9</sup> Extensive studies have analytically and experimentally established that single cosmic-ray or nuclear particles can cause transient upset of stored information in microcircuits of a wide variety of technologies.

The degree of effects in a microcircuit is determined by the ionization within a critical volume of semiconductor. The ionization may be the result of direct ionization of the incident particle or by ionization of secondary particles resulting from a nuclear reaction. Hole-electron pairs are produced along the track in a narrow column (on the



**FIGURE 4. SINGLE PARTICLE IONIZATION EFFECTS**

order of 1000 Å diameter).<sup>10</sup> The energy required to generate a single hole-electron pair is approximately 3.5 electron-volts just as in the case of bulk ionization. Generated carriers move under the influence of electric fields and diffusion gradients to appear as a transient current or modification in charge on a junction capacitance. The nature of the device effect will be discussed in Section 2.2.2.

The critical volume for a single microcircuit element is defined by a surface area which may vary from 5  $\mu\text{m}$  to 25  $\mu\text{m}$  on a side and a depth which may vary from 2  $\mu\text{m}$  to 10  $\mu\text{m}$ . For comparison, the range of a 4 MeV  $\alpha$ -particle in silicon is approximately 20  $\mu\text{m}$ . If the angle of incidence to the critical volume was shallow, all the energy of the particle could be deposited within the critical volume. The 4 MeV of deposited energy would result in the generation of approximately  $10^6$  electron hole pairs or a charge of 0.18 pC. If device performance is sensitive to charge storage on the order of this critical charge, single event upsets or soft errors can be expected.

Deposition of critical charge can result from: 1) the energy deposited by a single high energy particle stopped within the critical volume (such as  $\alpha$ -particle), 2) energy deposited in a fraction of the range of a highly ionizing particle (such as high energy cosmic rays), or 3) energy deposited by secondary particles resulting from a nuclear reaction within the critical volume (such as from the recoil atoms and/or  $\alpha$ -particle of high energy proton or neutron interactions). Nuclear interactions and energy deposition are presented in detail in References 11-13.

The critical distinctions between bulk and localized ionizing radiation effects in microcircuits are: 1) bulk ionization simultaneously affects all devices throughout the microcircuit while localized ionization typically affects only one device or logic cell, and 2) bulk ionization

effects can be related in terms of aggregate energy deposited in rads(Si) independent of the mechanisms but detailed energy deposition characteristics of high energy particles are important in defining localized ionization effects. Important similarities between bulk and localized ionizing radiation effects are experimental and analytical techniques which must be used to detect the worst-case environment for the initiation of a transient upset in a complex microcircuit. The distinctions and similarities between bulk and localized effects will be developed continuously through this discussion.

## 2.2 P-N Junction Transient Response

### 2.2.1 Diode Primary Photocurrent

Ionizing radiation-induced effects in the p-n junction are the key link between the bulk semiconductor effects just discussed, and the transient response of complex microcircuits. The nature of diode photocurrent was presented in early work by Brown<sup>14</sup> and Wirth and Rogers.<sup>15</sup> Following is a mathematical derivation presented as a formal development to supplement the general description of photocurrent magnitude and time dependence.

The diode response can be characterized in terms of the carrier distribution and flow in the n- and p-type neutral semiconductor regions, with the boundary condition relating carrier density to applied voltage at the junction. The junction boundary conditions, assuming the usual Boltzmann approximation, give the carrier density at the edge of the junction as,

$$n_0 = n_p \exp(q\phi_a/kT)$$

= electron density at the edge of the p-region

and  $p_0 = p_n \exp(q\phi_a/kT)$   
 = hole density at the edge of the n-region

where  $\phi_a$  is the applied junction voltage and  $n_p$  and  $p_n$  are the thermal equilibrium minority carrier densities for an ideal diode as illustrated in Figure 5. Remote from the junction, the carrier densities at the junction have no effect on the carrier density; therefore,

$$n_{x \rightarrow \infty} = n_p + \Delta n, \text{ in the p-region}$$

$$p_{x \rightarrow \infty} = p_n + \Delta p, \text{ in the n-region}$$

where  $\Delta n$  and  $\Delta p$  are the radiation-induced excess minority carrier densities as evaluated from equations (1) and (2).

Assuming uniformly doped n- and p-regions, space-charge neutrality, and low-level injection, the continuity equations for minority equations become,

$$\frac{dp}{dt} = D_p \frac{d^2 p}{dx^2} - [(p-p_n)/\tau_p] + g_0; \text{ in the n-region} \quad (3)$$

and

$$\frac{dn}{dt} = D_n \frac{d^2 n}{dx^2} - [(n-n_p)/\tau_n] + g_0; \text{ in the p-region} \quad (4)$$

The diode photocurrent is then determined from the depletion-layer generation and diffusion currents at the junction, or

$$i_d = i_{gx} + i_p \Big|_{x=0^+} + i_n \Big|_{x=0^-}$$

where  $i_{gx}$  is the depletion layer generation current,  $i_p$  is the hole diffusion current at the edge of the n-region, and  $i_n$  is the electron diffusion current at the edge of the p-region.

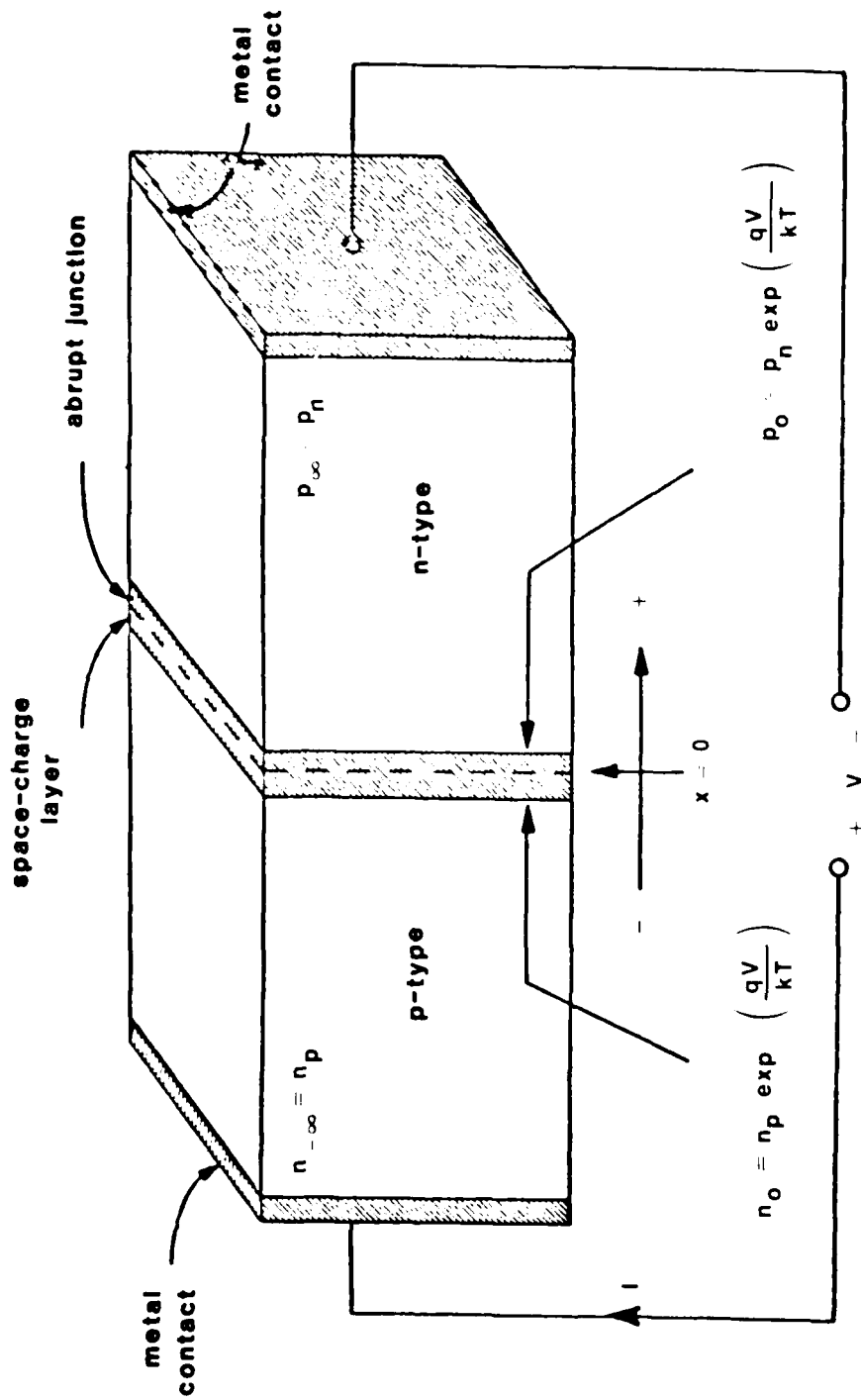


FIGURE 5. IDEAL DIODE STRUCTURE



Carriers generated in the depletion layer of the reverse-biased junction are rapidly swept out by the large electric field. Since the transient time of carriers across the depletion region is on the order of  $10^{-10}$  seconds, we can assume as equilibrium, or time-dependent current of,

$$i_{gx} = qAx_m \left( \frac{n_i}{\tau_0} + g_0 \dot{\gamma} \right) \quad (11)$$

where  $x_m$  is the depletion layer width,  $(n_i/\tau_0)$  is the thermal carrier generation rate, and  $(g_0 \dot{\gamma})$  is the radiation-induced carrier generation rate.

Diffusion current at the edges of the junction is expressed by,

$$i_p \Big|_{x=0^+} = -qA D_p \frac{dp}{dx} \Big|_{x=0^+} \quad (12)$$

and

$$i_n \Big|_{x=0^-} = qA D_n \frac{dn}{dx} \Big|_{x=0^-} \quad (13)$$

To evaluate the diffusion current we must solve the continuity equations (Eqs. 8 and 9) for the boundary conditions at the junction (Eqs. 5 and 6), and remote from the junction (Eq. 7).

First, using the modified boundary conditions remote from the junction (Eq. 3), the distribution of holes in the n-region is,

$$p(x) = [p(0) - g_0 \dot{\gamma} \tau_p - p_n] \exp(-x/L_p) + p_n + g_0 \dot{\gamma} \tau_p. \quad (14)$$

Diffusion current at the junction resulting from the enhanced minority carrier distribution is,

$$i_{p\gamma} = (qD_p A/L_p) [p(0) - p_n - g_0 \dot{\gamma} \tau_p] \quad (15)$$

The total diode radiation-inclusive current, including carrier generation in the depletion layer can be expressed as,

$$i_{dY} = I_s [\exp(q\phi_a/kT) - 1] - I_{pp} \quad (16)$$

where

$$I_{pp} = qAg_0\dot{\gamma} (L_p + L_n + x_m) \quad (17)$$

Overall equilibrium radiation-inclusive characteristics of the diode are summarized by the minority carrier distributions and the I-V characteristics shown in Figure 6. Intersection of the diode I-V characteristic with the coordinate axes gives the short-circuit photocurrent and an open-circuit photovoltage familiar in p-n junction solar cells.

The final case to be considered for the ideal diode is the development of time-dependent reverse-biased junction photocurrent in response to a step radiation environment. Returning to the continuity equation for the n-region we have,

$$\frac{\partial p(x,t)}{\partial t} = D_p \frac{\partial^2 p(x,t)}{\partial x^2} + g_0 \dot{\gamma}(t) - \frac{p(x,t) - P_n}{\tau_p} \quad (18)$$

The step ionizing radiation environment is defined by,

$$\dot{\gamma}(t) = \dot{\gamma}_0 u(t) \quad (19)$$

Using the Laplace transform on the time domain of Eqs. 18 and 19 the continuity equation becomes,

$$sP(x,s) = D_p \frac{d^2 p(x,s)}{dx^2} + g_0 \gamma \left( \frac{1}{s} \right) - \frac{p(x,s)}{\tau_p} \quad (20)$$

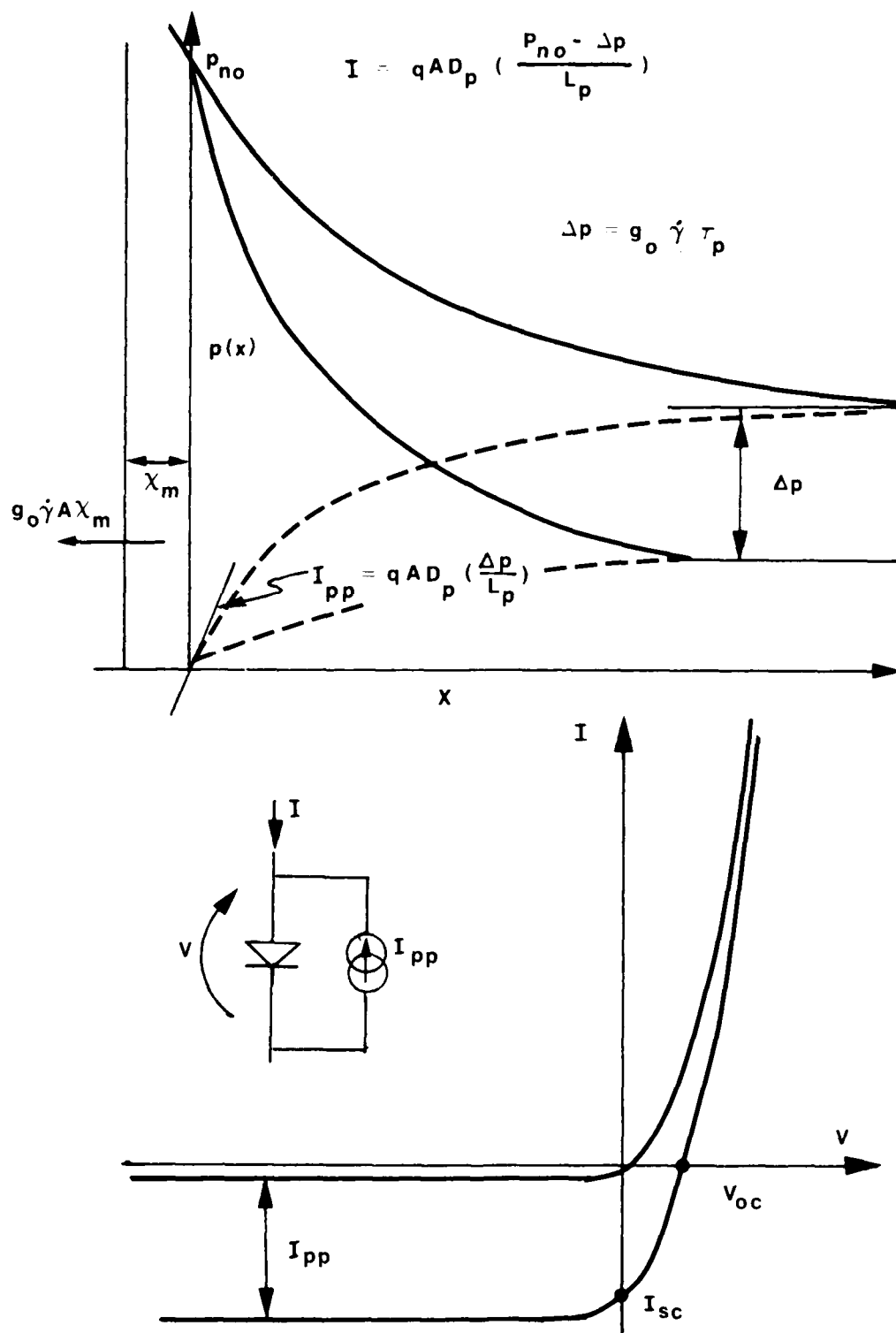


FIGURE 6. IDEAL DIODE CARRIER DISTRIBUTION AND I-V CURVE STEADY-STATE IONIZING RADIATION.

where we can assume that the thermal minority carrier is negligible compared to the radiation-induced level. Re-writing Eq. 20,

$$\frac{d^2 p(x, s)}{dx^2} = \alpha^2 p(x, s) - \beta \quad (21)$$

defining, 
$$\alpha = \left[ \frac{1}{D_p} \left( s + \frac{1}{\tau_p} \right) \right]^{1/2} \quad (22)$$

and 
$$\beta = g_0 \dot{\gamma} \left( \frac{1}{s} \right) = G(s) \quad (23)$$

for convenience, since the solution of the differential equation is of the form

$$P(x, s) = A + B \exp(-\alpha x) \quad (24)$$

where A and B must again be determined from the boundary conditions. At  $x = 0$  we must have the carrier density equal to zero at all times or,  $P(0, x) = 0$  which means,

$$A = -B \quad (25)$$

At  $x = +\infty$ , the time dependent increase in the carrier density is not influenced by the junction boundary condition. Taking the Laplace transformed form of Eq. 3 we have,

$$P(\infty, s) = g_0 \dot{\gamma} / s \left( s + \frac{1}{\tau_p} \right) \quad (26)$$

which must also equal the value of A. Substituting the values of A and B we have,

$$P(x, s) = \frac{q_0 \dot{i}}{s \left( s + \frac{1}{\tau_p} \right)} \left\{ 1 - \exp \left[ - \left[ \frac{1}{D_p} \left( s + \frac{1}{\tau_p} \right) \right]^{1/2} x \right] \right\} \quad (27)$$

A similar agreement gives the electron density in the p-region as,

$$N(x, s) = \frac{g_0 \dot{i}}{s \left( s + \frac{1}{\tau_n} \right)} \left\{ 1 - \exp \left[ - \left[ \frac{1}{D_n} \left( s + \frac{1}{\tau_n} \right) \right]^{1/2} x \right] \right\} \quad (28)$$

The diffusion diode photocurrent must now be determined from,

$$i_d(t) = qA_j \left[ D_p \frac{\partial p(x, t)}{\partial x} \Big|_{x=0^+} + D_n \frac{\partial n(x, t)}{\partial x} \Big|_{x=0^-} \right] \quad (29)$$

where,

$$\frac{dp(x, s)}{dx} \Big|_{x=0^+} = \frac{g_0 \dot{i}}{s \left( s + \frac{1}{\tau_p} \right)} \left[ \frac{1}{D_p} \left( s + \frac{1}{\tau_p} \right) \right]^{1/2} \quad (30)$$

$$= \frac{q_0 \dot{i}}{s(D_p)^{1/2} \left( s + \frac{1}{\tau_p} \right)^{1/2}}$$

and,

$$\frac{dn(x, s)}{dx} = \frac{g_0 \dot{i}}{x(D_n) \left( s + \frac{1}{\tau_n} \right)^{1/2}} \quad (31)$$

or

$$I_d(s) = qA_j \left[ \frac{(D_p \tau_p)^{1/2}}{(1 + s\tau_p)^{1/2}} + \frac{(D_n \tau_n)^{1/2}}{(1 + s\tau_n)^{1/2}} \right] \cdot \left( \frac{g_0 \dot{i}}{s} \right) \quad (32)$$

Taking the inverse transform of Eq. 32 the time-dependent diffusion photocurrent is expressed as,

$$i_d(t) = qA_j g_0 \dot{\gamma} \left[ L_p \operatorname{erf} \left( \frac{t}{\tau_p} \right)^{1/2} + L_n \operatorname{erf} \left( \frac{t}{\tau_n} \right)^{1/2} \right] \quad (33)$$

where  $(D_p \tau_p) = L_p$  and  $(D_n \tau_n) = L_n$ . The normalized error function response of a single component of the diffusion photocurrent is illustrated in Figure 7. The peak diffusion photocurrent as a function of radiation pulse width is shown in Figure 8. Since the error function response is a relatively unfamiliar function convenient evaluation is helpful for two important special cases (1) the equilibrium value for a radiation pulse long compared to the greater minority carrier lifetime and (2) the peak photocurrent resulting from a radiation pulse whose width is short compared to the minority carrier lifetime.

In summary then we have,

$$i_{pp} = qA_j g_0 \dot{\gamma} \left[ x_m + L_p + L_n \right] \quad \text{for } t_p \gg \tau \quad (34)$$

or

$$i_{pp} = qA_j g_0 \dot{\gamma} \left\{ x_m + (\pi/2) \left[ (D_p t_p)^{1/2} + (D_n t_p)^{1/2} \right] \right\} \quad (35)$$

for  $t_p \ll \tau$

with a general expression of

$$i_{pp}(t) = qA_j g_0 \dot{\gamma} u(t) \left[ x_m + L_p \operatorname{erf} \left( \frac{t}{\tau_p} \right)^{1/2} + L_n \operatorname{erf} \left( \frac{t}{\tau_n} \right)^{1/2} \right] \quad (36)$$

for the overall step photocurrent response of an ideal diode.

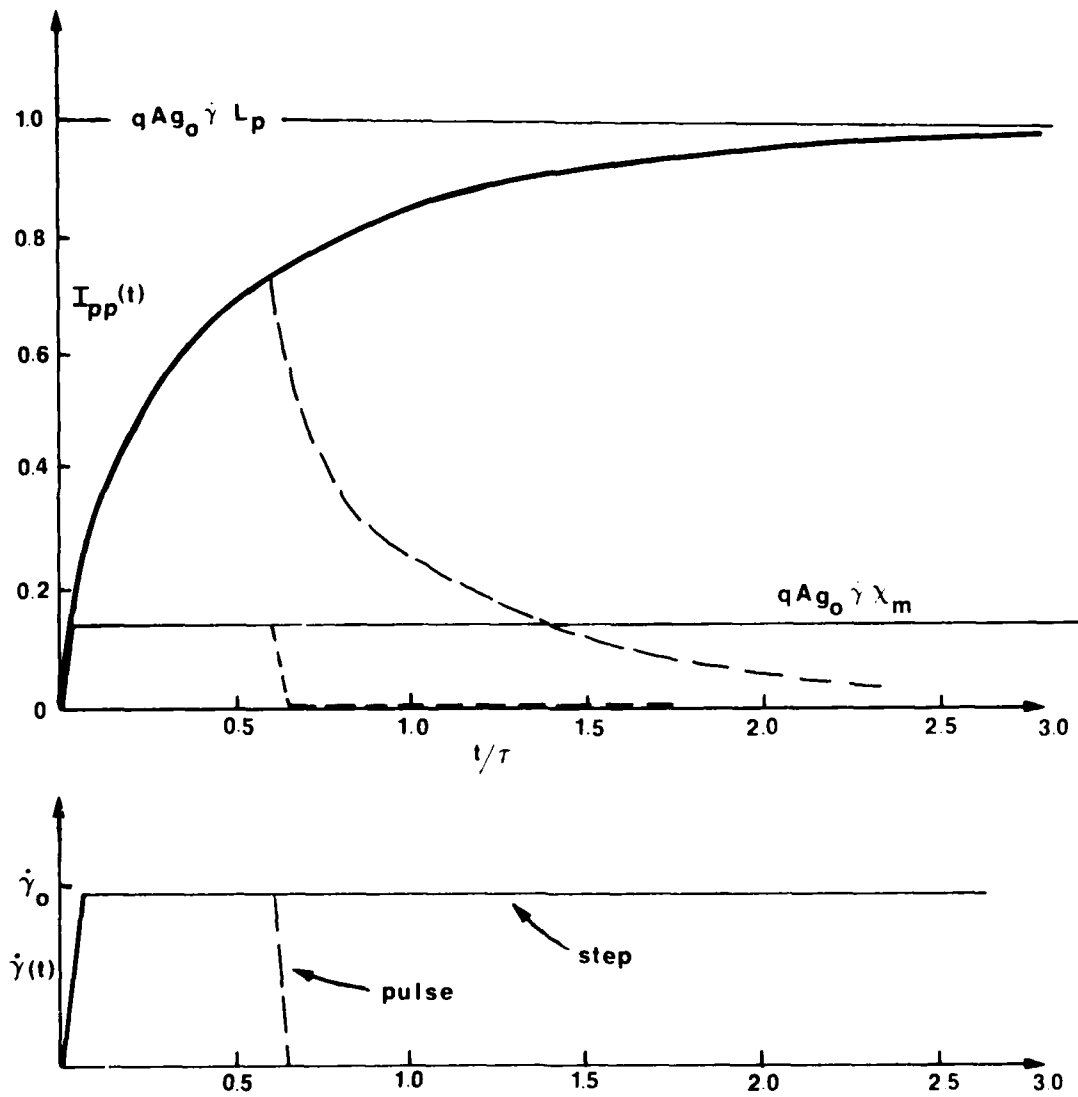


FIGURE 7. IDEAL DIODE TRANSIENT PHOTORESPONSE.

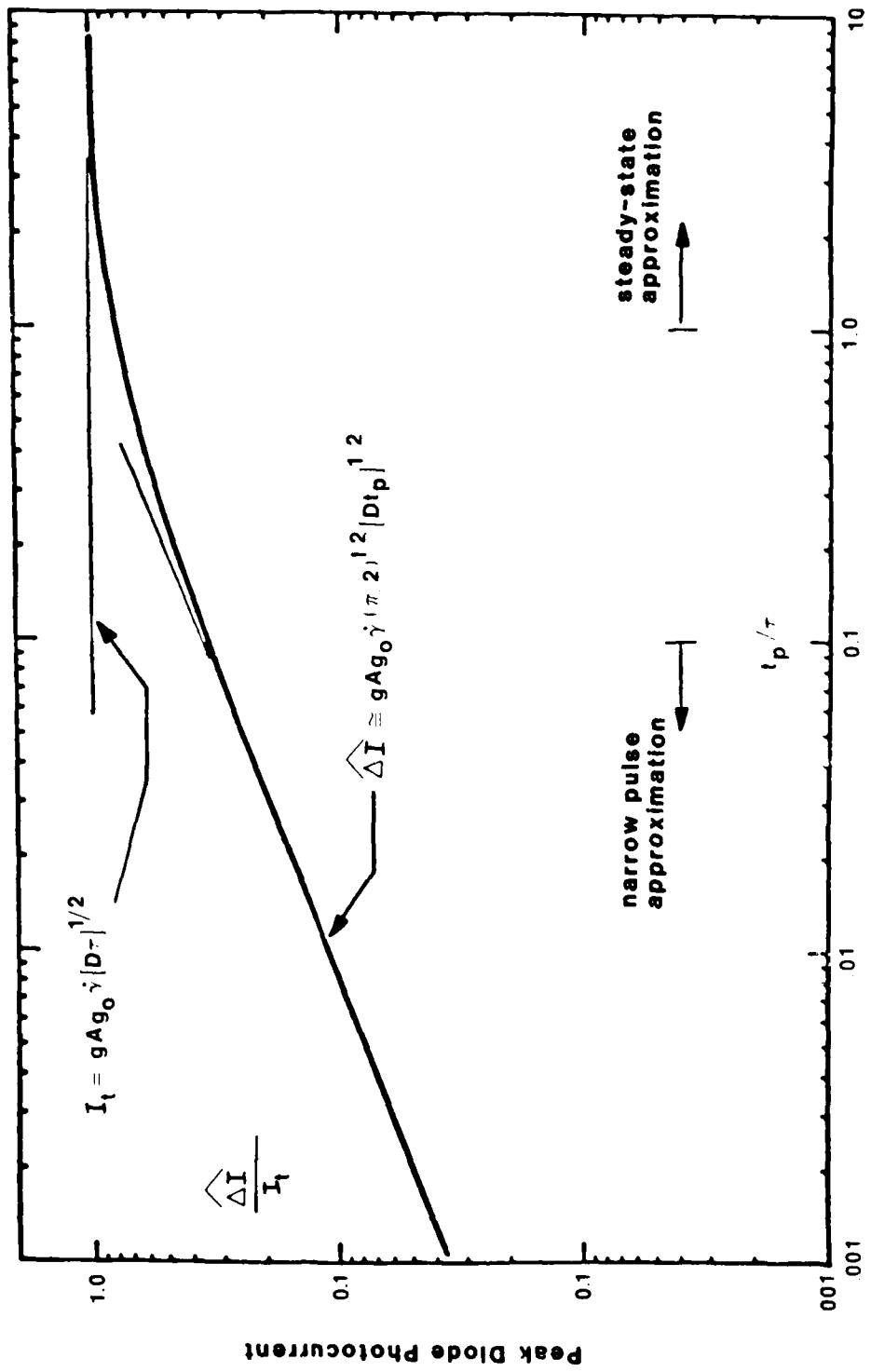


FIGURE 8. PEAK DIODE DIFFUSION PHOTOCURRENT AS A FUNCTION OF RADIATION PULSE WIDTH.



### 2.2.2 Transient Photocurrent-Localized Ionization

Carriers generated in the localized track of a high energy particle will be collected as a junction transient photocurrent. Those carriers generated in the junction depletion layer will be collected with transit delays less than 0.1 ns. Away from the junction depletion layer carriers will move along the ionization track toward the junction as well as by diffusion away from the track and toward the junction. Carrier collection along the ionization track can reach a significant length from the junction and has been termed "funneling". The specific transient current magnitude and waveform of an ionization track is a strong function of detailed physics and the orientation of the track with respect to the critical pn junction. One of the calculated estimates of the transient photocurrent is shown in Figure 9<sup>16</sup>. At this point it would appear that the transient current is dominated by a subnanosecond pulse with a small, slower diffusion component. If the pulse is shorter than a nanosecond then virtually all microcircuits will respond to the integral pulse or critical charge rather than the peak junction photocurrents. Possible exceptions to this might include very high speed ECL bipolar silicon or gallium-arsenide microcircuits. In general, however, the critical measure of the single particle ionization will be considered as the induced junction charge.

### 2.2.3 Radiation-Inclusive Diode Model

The time-dependent electrical and radiation-induced transient characteristics of a diode can be represented by the model shown in Figure 10. As with the bulk-ionization radiation-inclusive d-c diode model the key modification is the addition of the radiation-induced transient current generator. The model includes the voltage-dependent junction depletion capacitance and current-dependent diffusion capacitance which, with the d-c diode characteristic and parasitic resistances, represent the diode electrical transient response. Accurate representation of the diode response as an electrical transient is necessary, but not sufficient, for

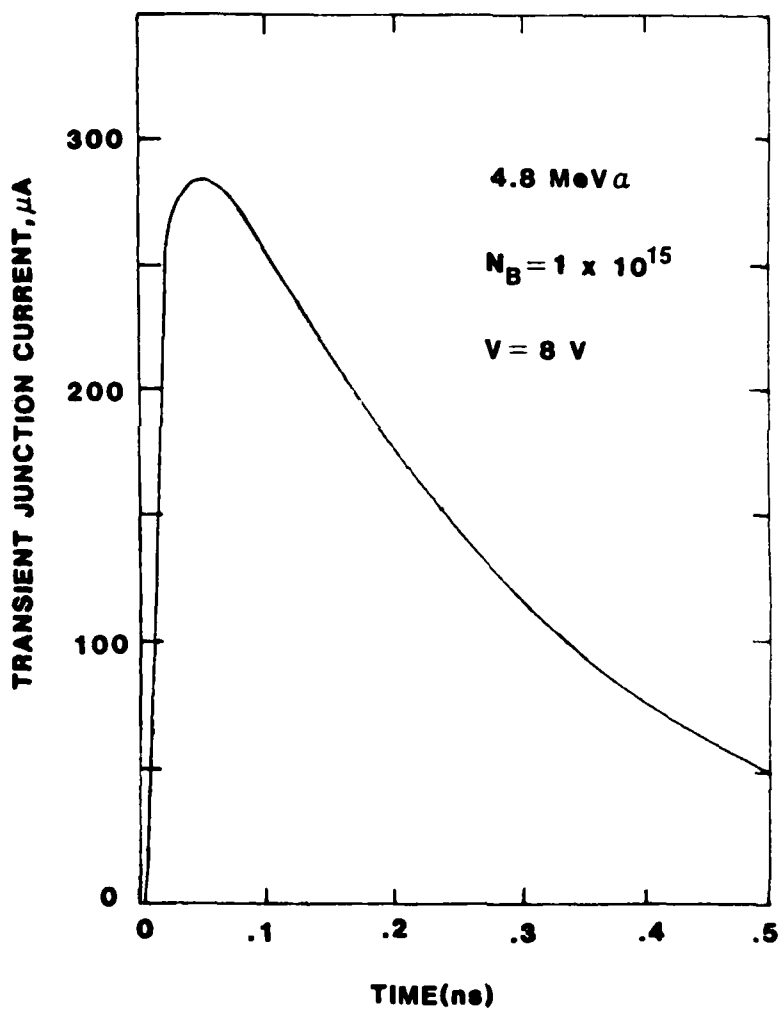


FIGURE 9. SINGLE EVENT ESTIMATED TRANSIENT JUNCTION CURRENT.

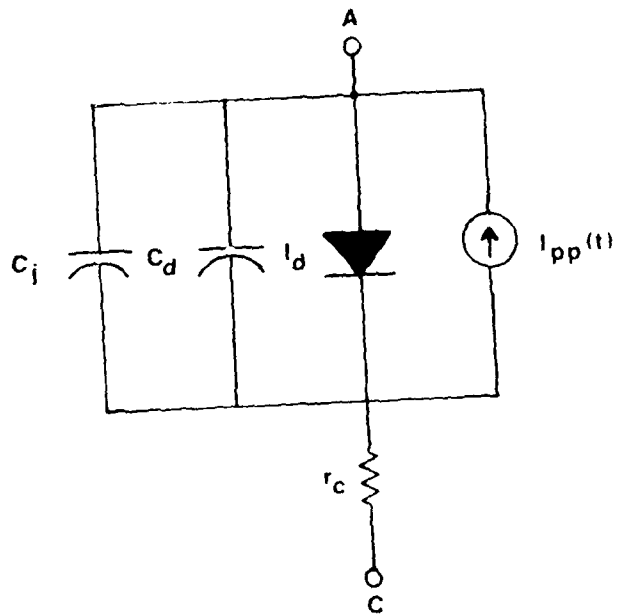


FIGURE 10. RADIATION-INCLUSIVE TIME-DEPENDENT DIODE MODEL.

accurate simulation of the diode radiation-induced response. The radiation-inclusive current generator is either the time-dependent primary photocurrent for a specific bulk ionizing radiation environment, or the transient junction current of a single ionizing particle.

The accuracy of the radiation-inclusive diode model is determined by the accuracy of the photocurrent generator and the accuracy of the model in simulating the electrical response. This is an important consideration in analysis and will be discussed more extensively in the transistor model description. One of the critical considerations in model accuracy is the determination of model parameter values. For the diode model of Figure 10 the data necessary for the model parameters are:

- 1) forward voltage at a low-level forward current
  - 2) forward voltage at a mid-level forward current
  - 3) forward voltage at a high-level forward current
  - 4) junction capacitance at a specified reverse-bias voltage
  - 5) diode saturated recovery time at specified forward and reverse switching currents
- and 6) measured time-dependent photocurrent  
or 7) junction breakdown voltage

Measurements 1 and 2 are necessary to define the constants,  $I_s$  and  $m$ , of the diode equation,

$$I = I_s \left[ \exp \left( \frac{qV}{mkT} \right) - 1 \right] \quad (38)$$

The difference in extrapolated voltage of the diode equation and the measured voltage at high forward current (3) defines the diode resistance.

$$I = I_s \left[ \exp \left( \frac{qV'}{mkT} \right) - 1 \right] \quad (39)$$

$$V = V' + IR_c \quad (40)$$

where  $V$  is the measured diode voltage.

The reverse-bias junction capacitance defines the depletion capacitance  $C_j$ . Variation with applied reverse-bias can be included by assuming an abrupt junction where,

$$C_j = \frac{C_{j0}}{(\psi_0 - V)^{1/2}} \quad (41)$$

where  $C_{j0}$  is the depletion capacitance at zero applied voltage,  $\psi_0$  is the built-in junction potential and  $V$  is the applied voltage. Alternatively, the capacitance can be measured as a function of voltage and fitting to the more general equation

$$C_j = \frac{C_{j0}}{(\psi_0 - V)^m} \quad (42)$$

where  $m$  is a function of the doping profile and varies from 0.33 for an graded junction of 0.5 for a graded junction.

The diffusion capacitance in the first-order diode model is an approximation to the distributed minority carrier storage in the forward biased ideal diode. The minority carrier lifetime can be determined (for the ideal diode) from the diode recovery time as shown Reference 17. With the minority carrier lifetime the diffusion capacitance is determined by,

$$C_d = \left( \frac{q}{kt} \right) \cdot \tau \cdot I \quad (43)$$

where  $I$  is the forward diode current.

The remaining parameter is now the diode photocurrent. If the diode is available to the external pins of the device the photocurrent can be measured directly in the pulsed ionizing radiation environment of a laboratory facility. The radiation level of exposure must be such that the photocurrent is large enough to measure accurately, and low enough so that diode saturation is avoided and the linear photoresponse is observed. The observed photoresponse will also be characteristic of the pulsed waveform of the laboratory environment. If the waveform of the threat environment is substantially different than that of the laboratory environment, then the measured response should be analytically separated into diffusion and depletion components and then extrapolated to the threat environment, using Eq. 36. If a linear accelerator is used for the laboratory environment measurement of the photoresponse as a function of radiation, pulse width and diode reverse bias can be very helpful in separating depletion and diffusion components of the photocurrent.

In a microcircuit, if design parameters are available, photocurrents can be calculated directly from the doping profile and junction areas. Junction areas on an existing microcircuit can be determined by optical measurement on a de-lidded device. The minority carrier lifetime in the critical substrate of a fabricated junction-isolated microcircuit can be estimated by a recovery time measurement of the substrate diode.

Critical parameters for the diode model in accurate simulation of single particle ionization effects are depletion capacitance, associated parasitic capacitances (including metallization), and the charge collected at the junction. Accurate definition of the capacitance is particularly critical since the radiation-induced time-response may be substantially faster than that anticipated in normal circuit operation. The

critical charge can be estimated by statistical analysis of particle energy deposition and/or estimates based on the observation of overall microcircuit response.

#### 2.2.4 Radiation-Induced Diode Saturation, Recovery Time

As mentioned previously, systems can be designed to detect the presence of a critical ionizing radiation environment and ignore errors in the electronics until system functions are regained. In this case the concern is for the survivability and recovery time of microcircuits.

It is misleading to assume that semiconductor devices "short" during a high level pulsed ionizing radiation exposure. It is believed that the bulk carrier generation remains linear with absorbed radiation intensity for both photon and electron exposures. It is also reasonable to assume that intense junction photocurrents remain linear until the radiation-induced excess minority carrier density approaches the majority carrier density. The overall currents in the devices will be very high and high injection level effects, voltage drops in parasitic resistances and conductivity modulation are critical and complex in the detailed device photoresponse. The basic effects, however, are radiation-induced diode and transistor saturated storage response, and the resulting transient circuit response at current levels which were probably never anticipated by the microcircuit designer.

Radiation-induced saturation of diodes and transistors is determined by circuit-imposed restrictions on current. In the diode circuit in Figure 11, the output voltage will drop with increasing radiation intensity until the load current is limited by the load resistor to approximately  $V/R_L$ . At that point further increase in radiation intensity and primary photocurrent will forward bias the diode. When the diode is forward biased minority carriers are injected from the junction. Following

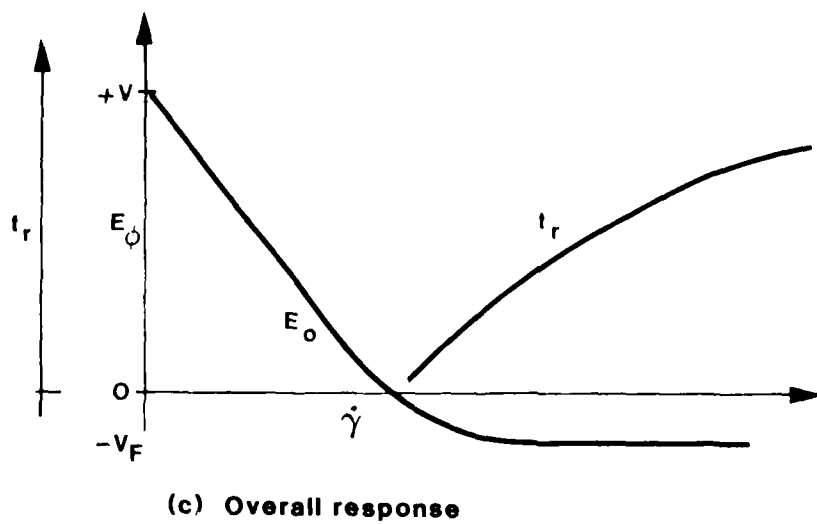
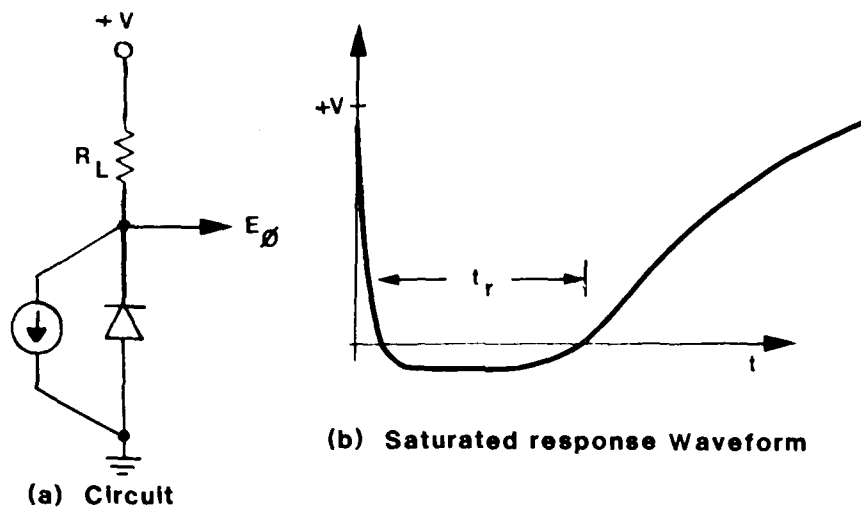


FIGURE 11. SATURATED DIODE PHOTORESPONSE



the end of the radiation pulse these injected carriers must be swept out before diode reverse bias can be reestablished (i.e., diode recovery time). Again, the simple diode recovery model is a good first-order model, but detailed analysis and prediction requires a complex device model. This saturated response and associated recovery is quite different than a transient "short-circuit".

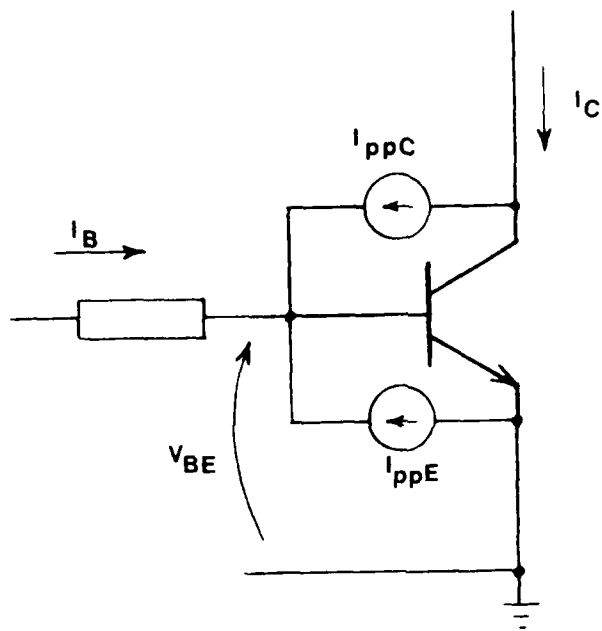
### 2.3 Transistor Secondary Photocurrent

The transient response of the bipolar transistor extends the transient junction currents resulting from radiation-induced carrier generation, to the interactions between junctions which involves transistor gain and enhanced transistor response. For bulk ionization in a bipolar transistor, the emitter and collector diode photocurrents have been termed primary photocurrent, and the enhanced response resulting from the transistor gain has been termed the secondary photocurrent.<sup>18</sup>

#### 2.3.1 Circuit Representation

To a good first-order approximation, the common-emitter photoreponse of a discrete transistor can be represented as an ideal transistor with diode (i.e., primary) photocurrent generators added in parallel with the collector-base and emitter-base junctions, as shown in Figure 12. The enhancement of the primary photocurrents can be illustrated simply by considering the common-emitter transient collector photocurrent as a function of circuit bias.

If the input resistance is zero (i.e., the base is shorted to the emitter) the transient collector current will simply be the collector primary photocurrent,  $I_{ppC}$ . In the other extreme, if the input resistance is very large (i.e., the base is effectively open). The primary photocurrents are effectively input base current which is multiplied by



**FIGURE 12. CIRCUIT MODEL OF TRANSISTOR ACTIVE REGION PHOTORESPONSE.**

the transistor common-emitter current gain,  $h_{FE}$ , to result in a transient collector current of  $h_{FE} (I_{ppC} + I_{ppE})$ . In general, the emitter primary photocurrent is small compared to the collector primary photocurrent which dominates the common-emitter transistor photoresponse. The variation of collector current with circuit conditions is illustrated for a simple circuit in Figure 13.

### 2.3.2 Minority Carrier Representation

The interaction between primary photocurrents and overall transistor photoresponse can be illustrated in more basic terms by considering the terminal currents of the transistor as determined by internal carrier distributions. Carrier densities in a uniform-base, one-dimensional transistor are shown in Figure 14. In the normal active region the emitter-base junction is forward biased and the collector-base junction is reverse-biased. Thus the carrier densities at the emitter junction are determined by the base-emitter voltage by,

$$n_{b0} = n_p \left[ \exp \left( \frac{qV_{BE}}{kT} \right) - 1 \right] \quad (14)$$

and

$$p_{e0} = p_{ne} \left[ \exp \left( \frac{qV_{BE}}{kT} \right) - 1 \right] \quad (15)$$

where  $n_{b0}$  is the electron minority carrier density at the emitter side of the base region and  $p_{e0}$  is the hole minority carrier density at the base side of the emitter region. The thermal equilibrium carrier densities are  $n_p$  and  $p_{ne}$  for the base and emitter regions respectively. The minority carrier density at the edges of the collector junction is zero because the junction is assumed to be strongly reverse-biased. I have also assumed an ohmic contact at the emitter which is within a minority carrier diffusion length of the junction and where the minority carrier density is zero at the contact.

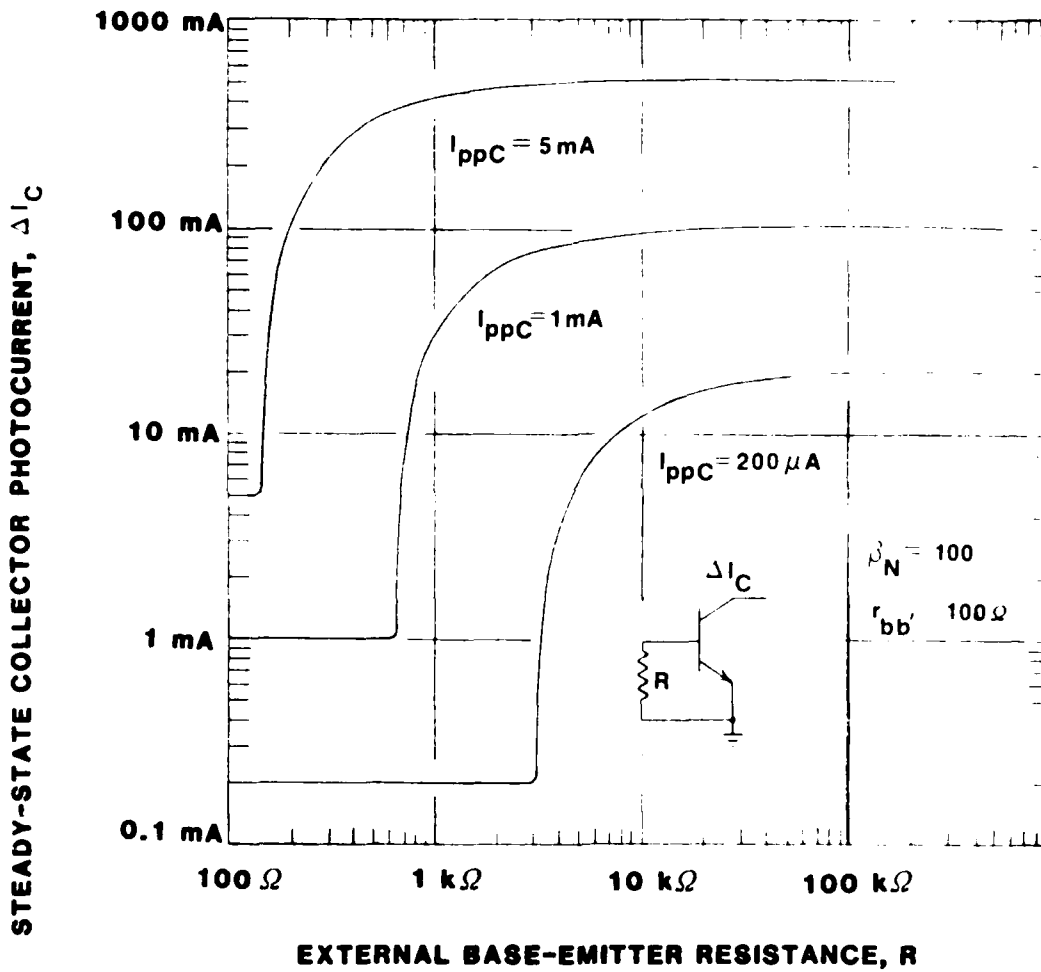


FIGURE 13. CIRCUIT VARIATION OF STEADY-STATE TRANSIENT COLLECTOR PHOTOCURRENT.

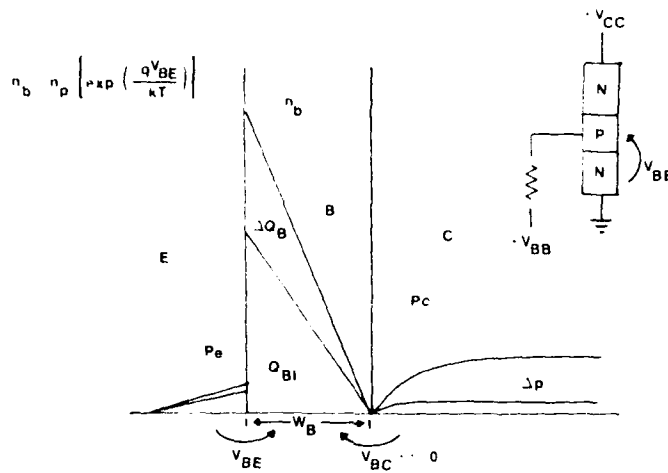


FIGURE 14. CARRIER DISTRIBUTION REPRESENTATION OF TRANSISTOR SECONDARY PHOTORESPONSE.

If we now expose the transistor to a steady ionizing radiation environment, the minority carrier density in the bulk collector region will be increased by

$$\Delta p_C = g_0 \tau_{pC} \quad \text{far from the collector junction} \quad (4)$$

as in the diode photoresponse. Holes generated within a few diffusion lengths of the junction will diffuse to the junction and into the base region. The hole diffusion current and current generated in the collector junction depletion region is the collector primary photocurrent. Holes entering the base region will increase the minority base charge if the emitter-base voltage is allowed to change. The balance between positive charge being swept into the base and transistor response will be determined by, 1) the boundary condition between carrier density and voltage at the junction, Eq. 44, 2) the increased base current due to an increase in base charge,  $\Delta Q_B$ , and 3) the circuit boundary conditions between the

emitter-base voltage and total external base current. If the base terminal of the transistor is effectively open, the base charge will increase until the additional recombination equals the radiation-induced carrier flow into the base, or,

$$\frac{\Delta Q_B}{\tau_{nb}} = I_{ppC} \quad (\text{open-base}) \quad (47)$$

The emitter junction voltage will increase to accommodate the excess base charge.

$$\Delta n_b = n_p \left[ \exp \left( \frac{q \Delta V_{BE}}{kT} \right) \right] \quad (48)$$

or

$$\Delta V_{BE} = \frac{kT}{q} \cdot \ln \left( \frac{\Delta n_b}{n_p} \right) \quad (49)$$

The increase in collector current resulting from the increase in base charge will be,

$$\Delta I_C = D_n \cdot \frac{\Delta n_b}{W_B} + I_{ppC} \quad (50)$$

$$\Delta Q_B = \frac{1}{2} \Delta n_b \cdot W_B \quad (51)$$

or

$$\Delta n_b = 2 \Delta Q_B / W_B \quad (52)$$

so,

$$\Delta I_C = \frac{2 D_n \Delta Q_B}{W_B} + I_{ppC} \quad (53)$$

but using

$$\frac{\Delta Q_B}{n_b} = I_{ppC} \quad (54)$$

$$\Delta I_C = \frac{2 D_b \tau_{nb} \cdot I_{ppC}}{W_B^2} + I_{ppC} \quad (55)$$

However, in our ideal transistor the common emitter current is given by,

$$\beta_N = \frac{2 D_n \tau_{nb}}{W_B^2} \quad (56)$$

so

$$\Delta I_C = (1 + \beta_N) I_{ppC} \quad (\text{open base}) \quad (57)$$

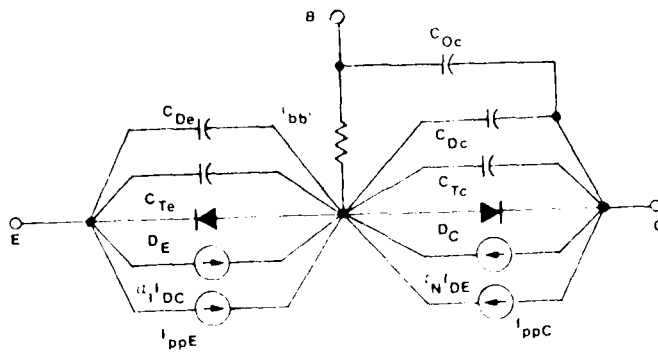
Thus, if the base of the common-emitter transistor is effectively an open-circuit, the increased base charge due to the collector primary photocurrent results in a secondary collector photocurrent which multiplies the primary photocurrent by the common-emitter current gain. Conversely, if the emitter-base junction was stiffly biased (such as with a low-resistance voltage source) all the excess carriers in the base would be removed, the base minority carrier charge would not change, and the observed transient collector photocurrent would only be the collector primary photocurrent.

### 2.3.3 Radiation-Inclusive Transistor Models

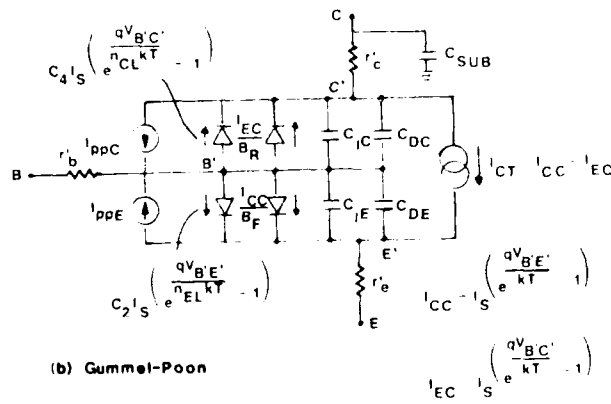
The overall considerations and studies directed to semiconductor device models and their extension to transient photoresponse are very

extensive and, in detail, well beyond the scope of this review. Historically, Caldwell, et al.<sup>18,19</sup> demonstrated that the measured primary photocurrent of a transistor could be included in a large-signal Beaufoy-Sparkes Charge-Control Model to accurately simulate the transistor large-signal photoresponse. Next it was shown by Kleiner<sup>20</sup> that similar results could be obtained by adding the primary photocurrent generator to the Ebers-Moll large-signal transistor model. At about the same time, I, in my own way, set out to demonstrate that both primary and secondary photocurrents could be represented implicitly in the transistor response by using the lumped-model representation of electrical performance in terms of device geometrical and bulk semiconductor parameters.<sup>21,22</sup> Also, at about the same time, it was demonstrated that the charge-control, Ebers-Moll and lumped-model were all electrically identical for identical assumptions in their derivation.<sup>23,24</sup> Some controversy remained, however, because different models were imbedded in large computer programs used to simulate radiation-induced circuit response. In addition to the transistor models developed to be used with circuit analysis computer codes, sophisticated one-dimensional semiconductor device computer codes were developed for detailed analysis of transient and permanent damage effects.<sup>25</sup> Model development for computer-aided analysis is extensively reviewed in Reference 26. I would like to summarize these modeling studies by observing that, unless the analysis has the luxury of starting from "first-principles", the two critical steps are: 1) defining an accurate electrical model, valid over the time and voltage/current levels which include the radiation-induced transient response and 2) defining the magnitude and waveform of the junction primary photocurrent generators. Ultimately, both these tasks require both experimental and analytical effort. For a single transistor, parameters for the electrical model can generally be determined by direct measurement. Typical forms of the Ebers-Moll and Gummel Poon models are shown in Figure 15. The Ebers-Moll is typically used with the SCEPTRE and SYSCAP circuit analysis codes.<sup>27-29</sup> The electrical form of the Gummel-Poon model is of the options built with the popular





(a) Ebers-Moll



(b) Gummel-Poon

FIGURE 15. RADIATION-INCLUSIVE TRANSISTOR MODELS.

SPICE circuit analysis code.<sup>30, 31</sup> Other popular radiation-inclusive circuit analysis computer programs are NET-II and CIRCUS-II.<sup>32, 33\*</sup> Electrical parameter values for the model elements can be obtained by measurement and primary photocurrents can be determined by direct measurement, or calculated with knowledge of device geometry and doping profile.<sup>34</sup>

In the direct application of the transistor model to a circuit design the primary photocurrents can be measured experimentally and included directly in the circuit model. Sources of error in measuring the transistor primary photocurrents include: 1) dosimetry, 2) internal package effects, 3) external package/instrumentation effects and 4) device non-linearities not considered in the objective of the test. A semiconductor device responds to holes and electrons generated in the bulk material as measured by rads or Grays(Si). Two general effects compete in determining the energy deposited in the bulk semiconductor from the external radiation environment. Materials of the device package can shield low-energy radiation and reduce the radiation environment to below that of the external environment. On the other hand, low-energy photons reaching the device package interact with the packaging material as well as with the bulk silicon such that the effective dose in the bulk silicon is increased (i.e., dose enhancement).<sup>3-5</sup> For device studies I recommend that the measurement of the radiation environment be in terms of a semiconductor device similar in package and location to the device under test. Frequently, PIN diodes are used for this application. The photocurrent of a fully depleted PIN diode (i.e., large reverse bias) is essentially determined by carriers generated and swept out of the depletion region. Thus, the measured photocurrent is a reasonably accurate representation of the

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\* DNA supported computer codes (e.g., SCEPTRE, NET-2 and CIRCUS-2) may be obtained by contacting DASIAC, Kaman-Tempo, P.O. Drawer QQ, Santa Barbara, CA, 93103, Attn: M.A. Espig.

time-dependent dose rate in the package of the diode. Potentially important considerations in extrapolating the measured photoresponse in a laboratory radiation environment to a system environment should be checked by measuring the device photoresponse in laboratory environments of different radiation spectrum. Exposure to a range of radiation pulse widths in a laboratory environment is also necessary to relate the measured primary photocurrent to that expected in the system environment.

Device response non-linearities must also be considered in the primary photocurrent measurements. The collector and emitter photocurrents of the transistor can be measured with the unused terminal (i.e., the emitter and collector, respectively) either left open circuited or shorted to the reference terminal. For the collector primary photocurrent, the measured photoresponse increases with identical waveform until critical non-linearities are encountered. With the emitter shorted to the base, the primary photocurrent is linear until the photocurrent through the base is sufficient to forward bias the emitter-base junction by the voltage drop across the transverse base resistance. If the emitter terminal is left open, the primary photocurrent is linear until the transverse base voltage drop exceeds the base-emitter breakdown voltage. Above these critical radiation intensities, the observed collector photocurrent includes a secondary response as well as the primary photocurrent response.<sup>35</sup> In addition to these considerations for the measurement of the emitter primary photocurrent, relative carrier collection by the emitter and collector junction must be included. The emitter primary photocurrent for a planar transistor will be composed principally by carriers generated in the inactive and active base regions of the transistor. Some fraction of these carriers have also been collected and measured in the collector primary photocurrent experiment. In general, this component or carrier collection will tend to overestimate the emitter primary photocurrent with respect to the way carriers are collected in the active transistor photoresponse. It is suggested that the emitter photocurrent can generally be

neglected in the common-emitter transistor photoresponse. In those circuit configurations where the emitter primary photocurrent may be important (e.g., emitter-follower) it is suggested that a transistor photoresponse can be measured in a circuit representative of application.

The linear response of transistor primary photocurrent should be checked by measuring the photocurrent at a lowest reasonable radiation intensity, checking the waveform to that expected from first-order carrier collection, and remeasuring at a higher radiation intensity to check on linearity of response with increasing radiation intensity.

#### 2.3.4 Transistor Transient Photoresponse

In general, the transient response of a transistor circuit requires a computer-aided numerical analysis. There are two cases, however, where we can bound the transistor response without numerical analysis: the linear, low-level response and saturated recovery from a high-level exposure.

If the transistor is operated as an element of a linear circuit and if the photocurrents are small compared to the circuit bias currents the circuit photoresponse can be estimated by simple linear model techniques. The upper bound of the linear common-emitter transistor photoresponse is when the source impedance is high compared to the transistor input impedance. It can be shown that this time-dependent upper bound is expressed by the product of the LaPlace transformed primary photocurrent and common-emitter current gain. Ignoring the emitter primary photocurrent we then have,

$$\Delta I_C(s) \leq (1 + \beta_N(s)) \cdot I_{ppC}(s) \quad (58)$$

or,

$$\Delta i_C(t) \leq \mathcal{L}^{-1} [(1 + \beta_N(s)) \cdot I_{pp}(s)] \quad (59)$$

where  $\beta_N(s) \approx \beta_N / [1 + (s/\omega_E)]$

and  $\omega_E$  = common-emitter gain cutoff frequency. This upper bound on transient collector photocurrent is illustrated in figure 16 for the primary photocurrent shown and a transistor of  $\beta_N = 100$  and  $f_E = 1$  MHz. If the primary photocurrent pulse is fast compared to the circuit and transistor time constants (as may be the case for the transient current resulting from localized ionization), the upper limit of the transistor collector current is the impulse response or,

$$\Delta I_C(s) \leq Q_{pp} \cdot \beta_N(s) \quad (60)$$

or

$$\Delta i_C(t) \leq Q_{pp} \cdot \beta_N \cdot \omega_E \left[ 1 - e^{-\omega_E t} \right] \quad (61)$$

where  $Q_{pp}$  is the charge of the primary photocurrent impulse function and  $\omega_E = 2\pi f_E$ .

When the transistor is exposed to a high-level ionizing radiation environment, the resulting photocurrents may exceed the current available through the circuit elements. The transistor, like the diode, does not become a "short-circuit" but saturates with a saturation recovery time after the end of the radiation pulse. Transistor saturated storage time resulting from electrical switching can be expressed approximately as,

$$t_s \approx \tau_s \ln \frac{-I_{B2} + I_{B1}}{-I_{B2} - V_{CC}/R_L \beta_N} \quad (62)$$

for the circuit as shown in figure 17a. Assuming that the circuit is in the "off" state and then saturated by the collector primary photocurrent, an upper bound of the radiation-induced recovery time can be expressed as,

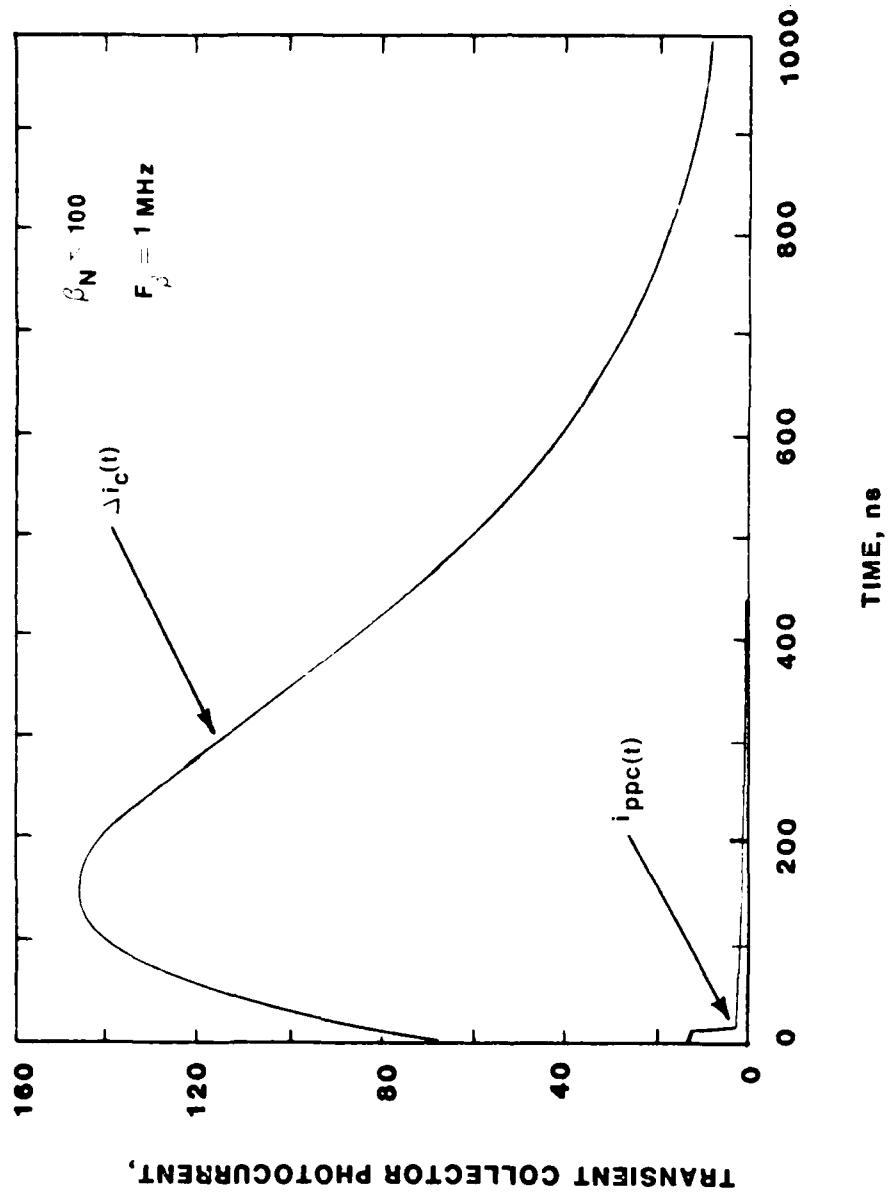
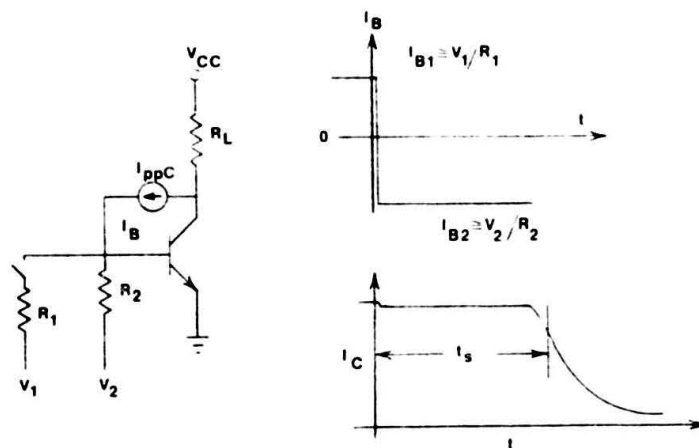
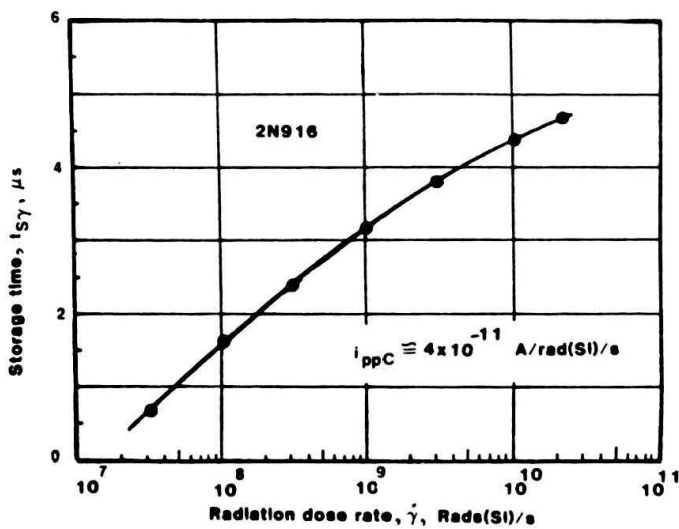


FIGURE 16. TRANSISTOR LINEAR SECONDARY PHOTORESPONSE.



(a) STORAGE RESPONSE CHARACTERISTICS.



(b) TRANSISTOR RADIATION INDUCED STORAGE TIME

FIGURE 17. TRANSISTOR HIGH LEVEL PHOTORESPONSE

$$t_{SY} \leq \tau_s \ln \frac{I_{ppC}}{-I_{B2} - V_{CC}/R_L \beta_N} \quad (63)$$

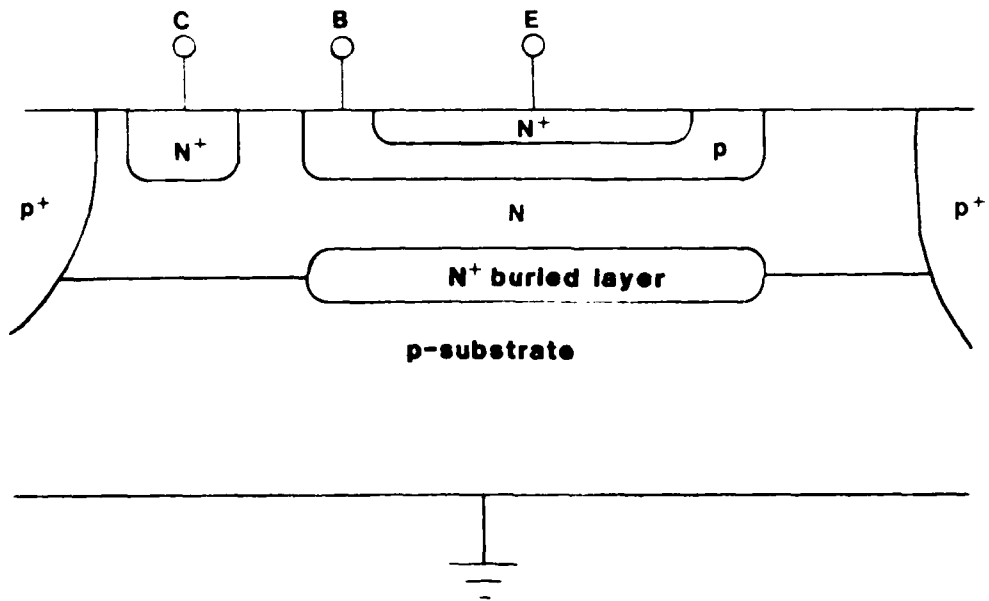
Equation 63 can be modified for specific circuit conditions to estimate the upper bound of transistor recovery time in the same way. The analysis is an upper bound because the collector primary photocurrent has been assumed to be held at its peak value. Carriers stored under conditions of the steady-state photocurrent will be greater than those resulting from the transient photocurrent. Radiation-induced storage times in a transistor as a function of increasing radiation level as shown in Figure 17b.

### 2.3.5 Microcircuit Transistor Element Photoresponse

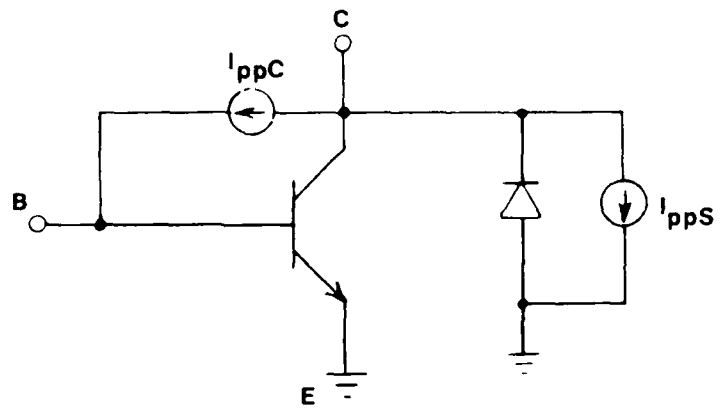
The final link between basic radiation-induced carrier generation and microcircuit photoresponse is the photoresponse of the individual microcircuit elements. In general, concepts of primary and secondary photocurrent apply directly to any microcircuit element. Specific cases of particular interest are the junction-isolated bipolar transistor and the MOS transistor.

The structure of the junction-isolated bipolar transistor element is shown in Figure 18a. The collector-substrate junction is electrically reverse-biased by biasing the substrate at the most negative circuit voltage to insure electrical isolation between circuit elements in the microcircuit. The radiation-inclusive model of the transistor element must include the substrate diode and photocurrent as well as the transistor as shown in Figure 18b. The substrate photocurrent will be determined principally by the carriers generated in the depletion layer and the p-type substrate. Carriers generated in the n-collector and n+ buried layer will be shared between the substrate and collector primary photocurrents depending on the detailed doping profile. The circuit response of the transistor element will be just as that of the discrete transistor, with





(a) Transistor Model



(b) Cross-section

FIGURE 18. JUNCTION-ISOLATED BIPOLAR TRANSISTOR ELEMENT.

the some reduction in the collector primary photocurrent due to the relatively small collector volume and the addition of a relatively large substrate junction photocurrent.

Radiation-inclusive models for MOS transistor elements can be just the inclusion of addition of diodes and primary photocurrent generators to the drain-substrate and source-substrate junctions of a large-signal model. Adding the photocurrent generators is relatively easy but defining the parameters for the large-signal model valid for fast transients can be very challenging. If the drain and substrate junctions are closely spaced (as is usually the case for modern transistors) secondary photocurrent response of the parasitic drain-substrate-source parasitic bipolar transistor should also be included in the model. Radiation-inclusive MOS transistor models are presented in detail in References 36-39.

### 3. TRANSIENT EFFECTS IN BASIC MICROCIRCUITS

Consideration of an MSI/LSI array photoresponse in terms of individual circuit elements could be an enormously complex problem. Digital microcircuits are, however, composed of logic and memory cells which are used repetitively through the array. The photoresponse of these cells can be related directly to the response of the circuit elements. Understanding the nature of the cell photoresponse can then be used to guide and interpret experimental measurement of the overall array photoresponse.

In this discussion several types of cells have been selected to illustrate variations in the nature of cell photoresponse. It is not intended for this to be an exhaustive review of all microcircuit logic cells but rather the illustration of particular natures in photoresponse representation of a wide variety of cells.

Analog microcircuits have been included (Section 3.4) because analysis can be very helpful in interpreting the low-level photoresponse of complex "linear" microcircuits.

### 3.1 TTL gate Photoresponse

The junction-isolated bipolar transistor-transistor-logic (TTL) cell illustrates a transient photoresponse which is determined principally by the peak photocurrent of the circuit elements. A radiation-inclusive gate model is shown in Figure 19. Electrical circuit elements have been shown schematically and current generators have been added to represent the primary photocurrents of the collector-base and collection substrate junctions.

For illustration we will assume a steady-state bulk ionizing the phase splitter transistor,  $Q_2$ , is turned off as well as the lower output transistor,  $Q_4$ . The upper output transistor,  $Q_3$  is on and acts as a resistance to sourcing output current. Now, for illustration, assume that the dominant photocurrent in determining the "off" state photoresponse is the substrate photocurrent of the lower output transistor as shown in Figure 20. The observed gate output voltage as a function of steady-state radiation intensity will then be as shown in Figure 20. (assuming that  $Q_3$  acts as a constant load resistance). As an individual logic element the definition of transient upset for the gate would depend on the point where the output voltage dropped below the allowed minimum "1" level. The basic nature of the output transient is to increase monotonically with radiation level with a relatively soft definition of transient upset. In an array, of course, the sharp threshold characteristics of the driven logic circuits would lead to a sharp definition of logic upset.

To discuss the nature of the gate in the "on" output state we will add the substrate photocurrent of the input transistor as a contributor to the gate photoresponse as shown in Figure 21. With the gate in

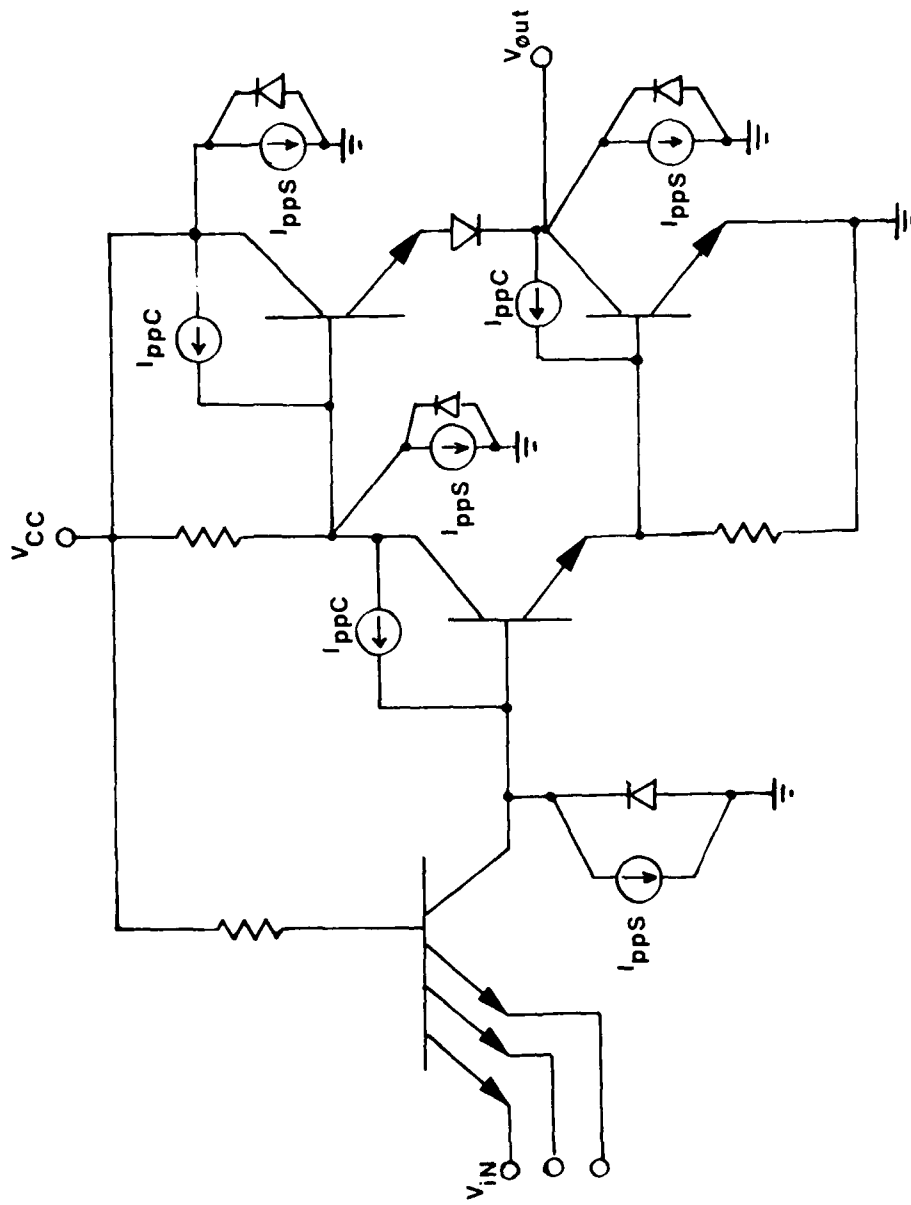


FIGURE 19. RADIATION-INCLUSIVE TTL GATE SCHEMATIC.

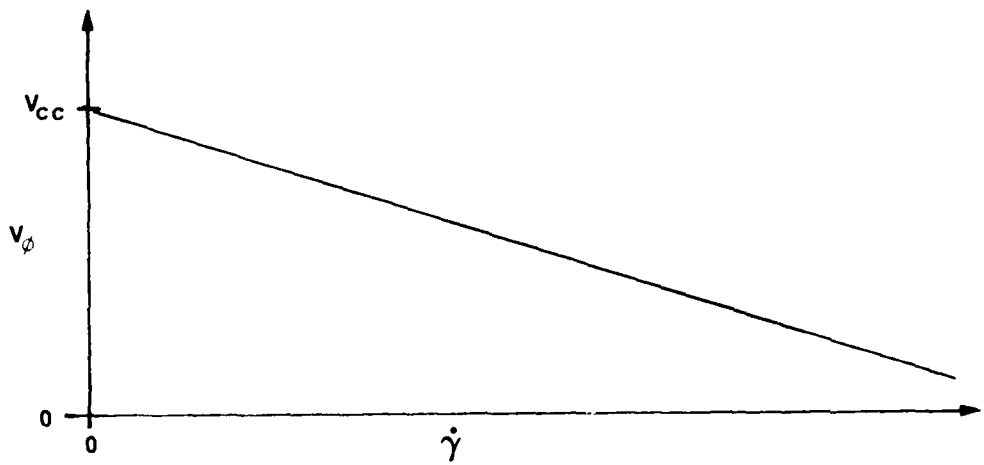
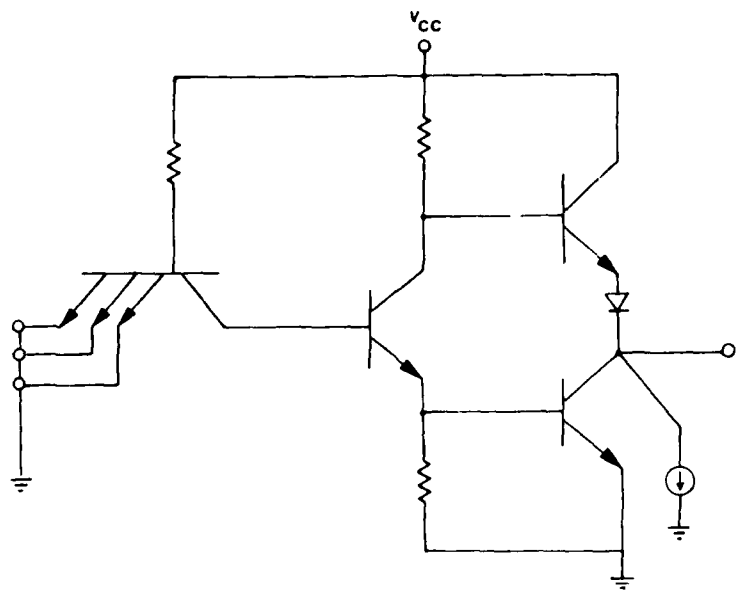
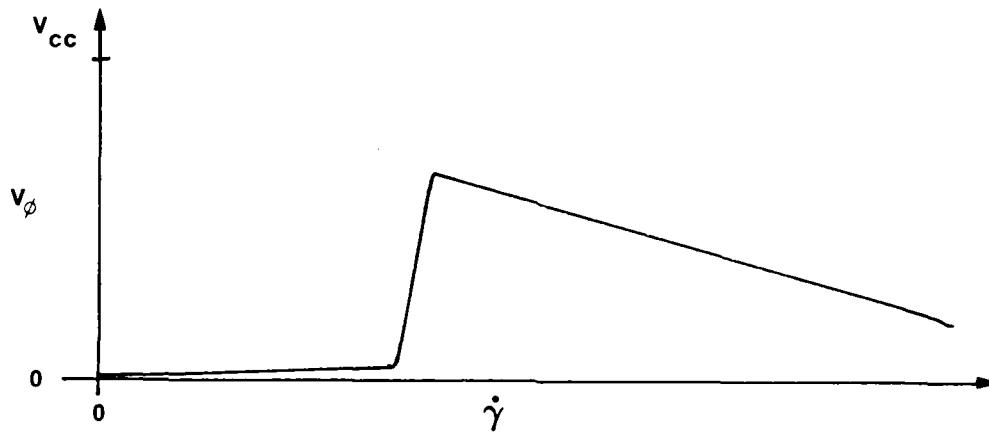
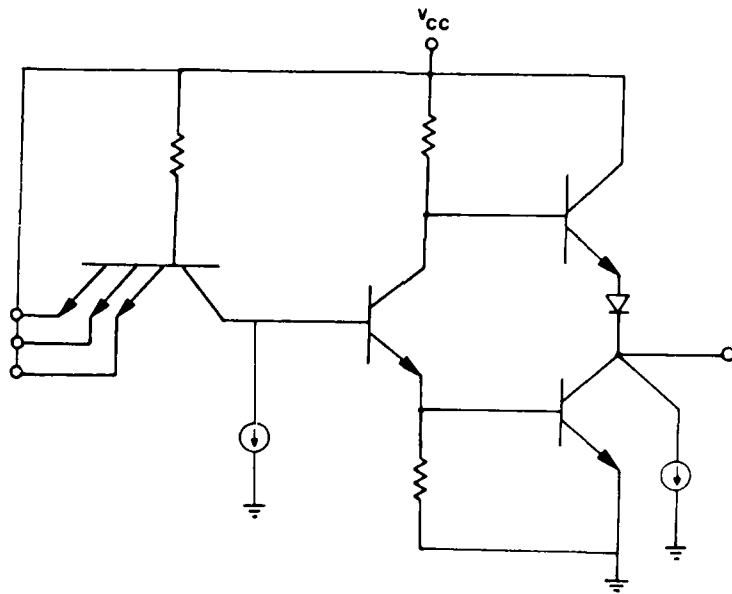


FIGURE 20. OFF STATE PHOTORESPONSE, OVERALL.



**FIGURE 21. ON STATE PHOTORESPONSE, OVERALL.  
TTL GATE STEADY-STATE PHOTORESPONSE.**

the "on" output state all the inputs are biased at the positive supply voltage. The input transistor provides bias current to the phase splitter holding it and the lower output transistor on. At a critical radiation intensity the substrate photocurrent of  $Q_1$  will be equal to the bias current and the output stage will turn off. The output voltage, however, will only increase to the point defined by the output transistor photocurrent generator even with  $Q_4$  turned off. The resultant output voltage as a function of steady-state ionizing radiation intensity is shown in Figure 21. The abrupt increase in output voltage at a critical radiation intensities illustrates a transient effect which can appear abruptly at a threshold radiation exposure even independent of the interactive threshold effects between signals of digital logic cells.

The overall gate response depends on the relative effects of the isolation junction photocurrents, which is determined by the relative area used for the transistor geometries. In a commercial part these geometries are determined by electrical performance and layout tradeoffs without regard to radiation-induced photocurrents. If the input transistor is very large the transient logic upset of the gate will be defined by the "0" state photoresponse. If the output transistors are relatively large the transient upset will be defined by the "1" state photoresponse, and it is possible that no significant "0" state photoresponse will be observed. In addition, the nature of the photocurrent and gate time responses will be included in the observed transient photoresponse. Possible waveforms are illustrated in Figure 22.

In summary, the "off" state of the junction-isolated TTL gate illustrates the gradual failure mode where the transient output voltage decreases monotonically with radiation intensity until a transient logic upset results. The junction-isolated gate in the "on" state also illustrates a strongly non-linear abrupt photoresponse which may, in fact, determine the worst-case logic upset level. In both cases, logic upset is

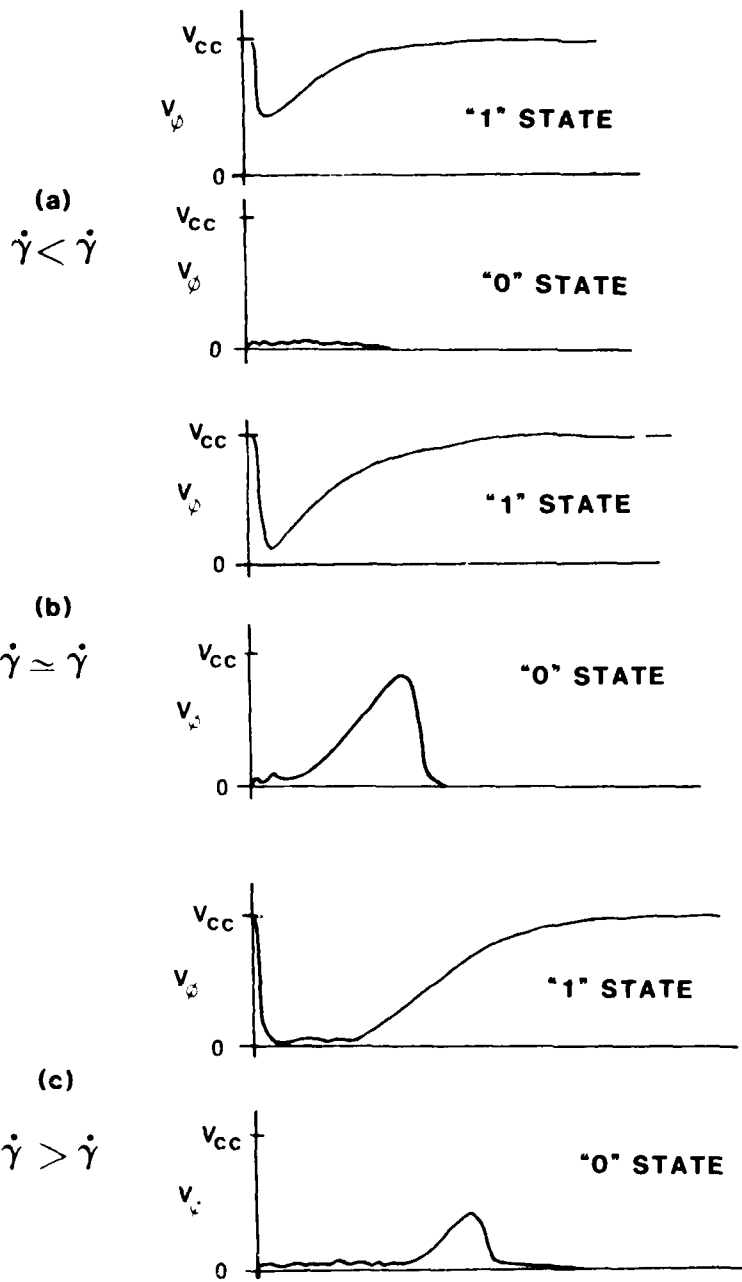


FIGURE 22. TTL GATE TRANSIENT PHOTORESPONSE.

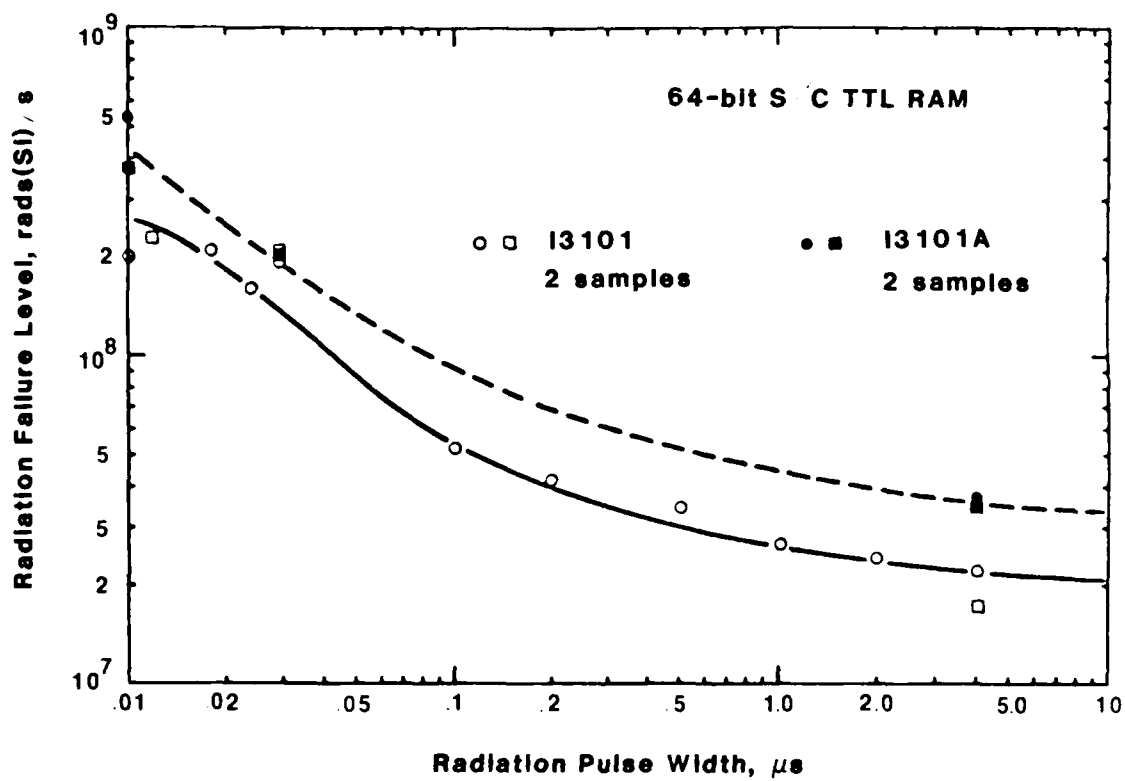


determined by the peak amplitude of the junction photocurrents. The variation in logic upset level with radiation pulse width then varies as the peak primary photocurrent. This is illustrated in the measured logic upset level of a simple (by today's standards) TTL RAM as shown in Figure 23.<sup>39</sup> With increasing radiation pulse width the peak photocurrents increase and the logic upset level decreases.

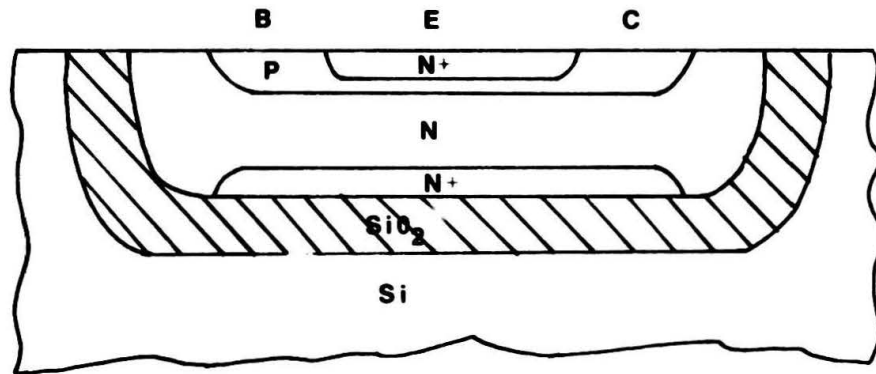
An alternate variation on the isolation technologies in bipolar arrays is replacement of the isolation junction by silicon dioxide in dielectric tubs. This eliminates the principal photocurrents leading to logic upset in the junction isolated array. In general the logic upset level of a dielectric-isolated array will be higher than that of a junction isolated array. The increase in upset level may, however, be less than the ratio of collector-substrate to collector-base photocurrents as might be expected. This is because of potential secondary photocurrents when the collector-base photocurrents interact with the relatively soft "off" bias networks. Further hardening of the dielectric-isolated array can be achieved by providing a shunt path for the collector base junction photocurrents. This can be realized by "photocompensation" when a diode of comparable area and doping profile is added in parallel with the emitter-base junction of the transistor as shown in Figure 24. The collector-base photocurrent entering the base mode of the transistor is compensated by the primary photocurrent of the diode. Thus, there is (in the perfect case) no net base current and the secondary photoresponse of the transistor is avoided.<sup>40</sup> Use of dielectric isolation and photocompensation can increase the worst-case logic upset level from between  $10^7$  and  $10^8$  rads (Si)/s to greater than  $10^9$  rad(Si)/s.

### 3.2 Dynamic n-MOS Memory Cell Transient Effects

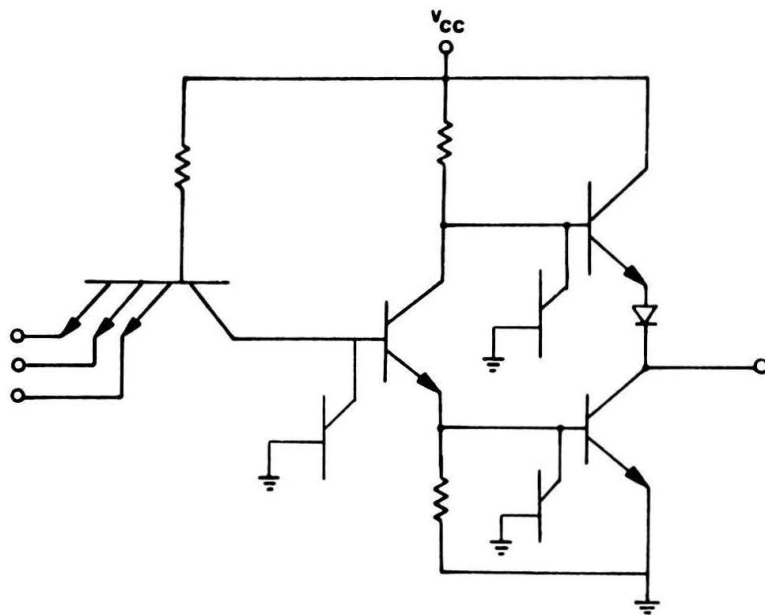
The key to dynamic LSI technology is the storage of logic information as the electrical charge state of an elemental capacitance. Major



**FIGURE 23. TTL RAM UPSET LEVEL DEPENDENCE ON RADIATION PULSE WIDTH.<sup>62</sup>**



**(a) DIC Transistor Element**



**(b) Photocompensated TTL Gate**

**FIGURE 24. RADIATION-HARDENED TTL GATE.**

applications of dynamic technology are in n-MOS LSI/VLSI random-access memory or the RAM subsystems of microprocessors. The technique has also been used in bipolar I<sup>2</sup>L RAMs and (while not called dynamic logic) is in charge-coupled device (CCD) arrays, CCD image sensors, CCD analog shift registers and in electrically alterable read-only-memories. In most cases the critical logic charge is stored on elemental junction capacitances. IN the EEROM's, however, the information is stored on isolated gates of MOS transistors. The principal advantage of dynamic LSI logic is the very small logic cell size. Increases in array complexity realized by the compact logic cells have been a major contributor to the competitive realization of VLSI. The present state of the art of dynamic n-MOS RAMs is somewhere beyond 64 kbits and near 256 kbits.

### 3.2.1 Data Loss - Bulk Ionization

The nature of n-mos memory cell photoresponse can be illustrated by the effects on an old dynamic shift register<sup>41</sup>. Three cells of the shift register are shown in Figure 25. Digital information is temporarily stored as the charge state of capacitors  $C_1$ ,  $C_4$ , and  $C_7$ . One cycle of information transfer through the shift register requires both a lead clock pulse ( $\phi_2$ ) and a lag clock pulse ( $\phi_1$ ). In the absence of the clock pulses both the transmission gates and load resistors are "off" MOS transistors. Thus, if the "off" resistance of the transistors were infinite, the gate input resistance of the inverter transistor also infinite, and there were zero leakage current to the substrate, the charge stored on the gate capacitances would remain indefinitely. Information is transferred to the internal inverter transistor during the turn-on of the lead clock pulse which decreases the effective resistance of the inverter load and enables the transmission gate. Given enough time, the charged state of the input is then transferred to the internal inverter transistor. Similarly, the lag clock pulse is then enabled, and the information stored on the internal transistor gate is transferred to the output of the cell. In practice, since the drain-source resistance of the "off" MOS transistor is not

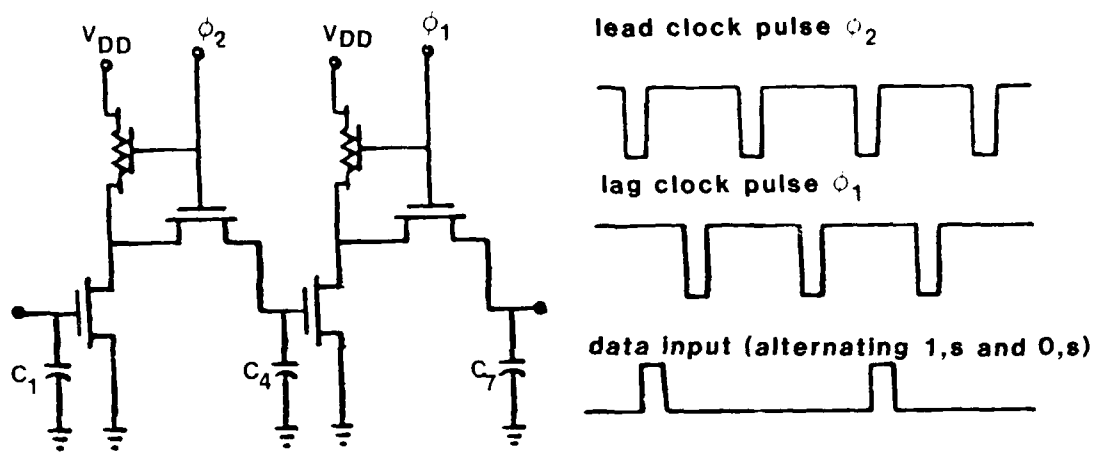


FIGURE 25. DYNAMIC MOS SHIFT REGISTER SCHEMATIC.

infinite, and since there is finite leakage current at the drain-substrate junction of the transmission gate, the information (charge) stored on the junction capacitance will leak off and must be refreshed at some minimum frequency. The minimum frequency of operation for the shift register must then increase as the thermal leakage current of the drain-substrate junction increases. In the absence of an ionizing radiation environment, this limitation is apparent in the specification of a minimum operating frequency that must be increased with increased operating temperature. The presence of a low level steady-state ionizing radiation environment will increase the junction leakage current with the radiation-induced carrier generation adding simply to the thermal carrier generation. In a wide-pulse, low-level ionizing environment we see an increase in the minimum frequency of operation.

Successful operation of the dynamic shift registers requires that the discharge time constant at the storage node be long compared to the longest time between clock pulses, which, in this case, is on the order of milliseconds. In a narrow-pulse ionizing radiation we would then expect that the critical level would be determined by the total radiation dose as long as the time between clock pulses was long compared to the pulse width of the junction photocurrent (or to the radiation pulse width and minority carrier lifetime in the substrate). The critical radiation dose rate for three of the shift registers is shown in Figure 26 as a function of the pulse width of the radiation environment<sup>47</sup>. As expected, the failure levels fall closely along lines of constant total radiation dose for all three device types.

The nature of the dynamic shift register radiation-induced transient effect is also consistent with the discharge of the storage capacitor. For a two-phase array with all cells in series such as the Intel 1406, the radiation induced failure is a narrow-pulse radiation environment appears as the transition of all internal cell to either the logic 1

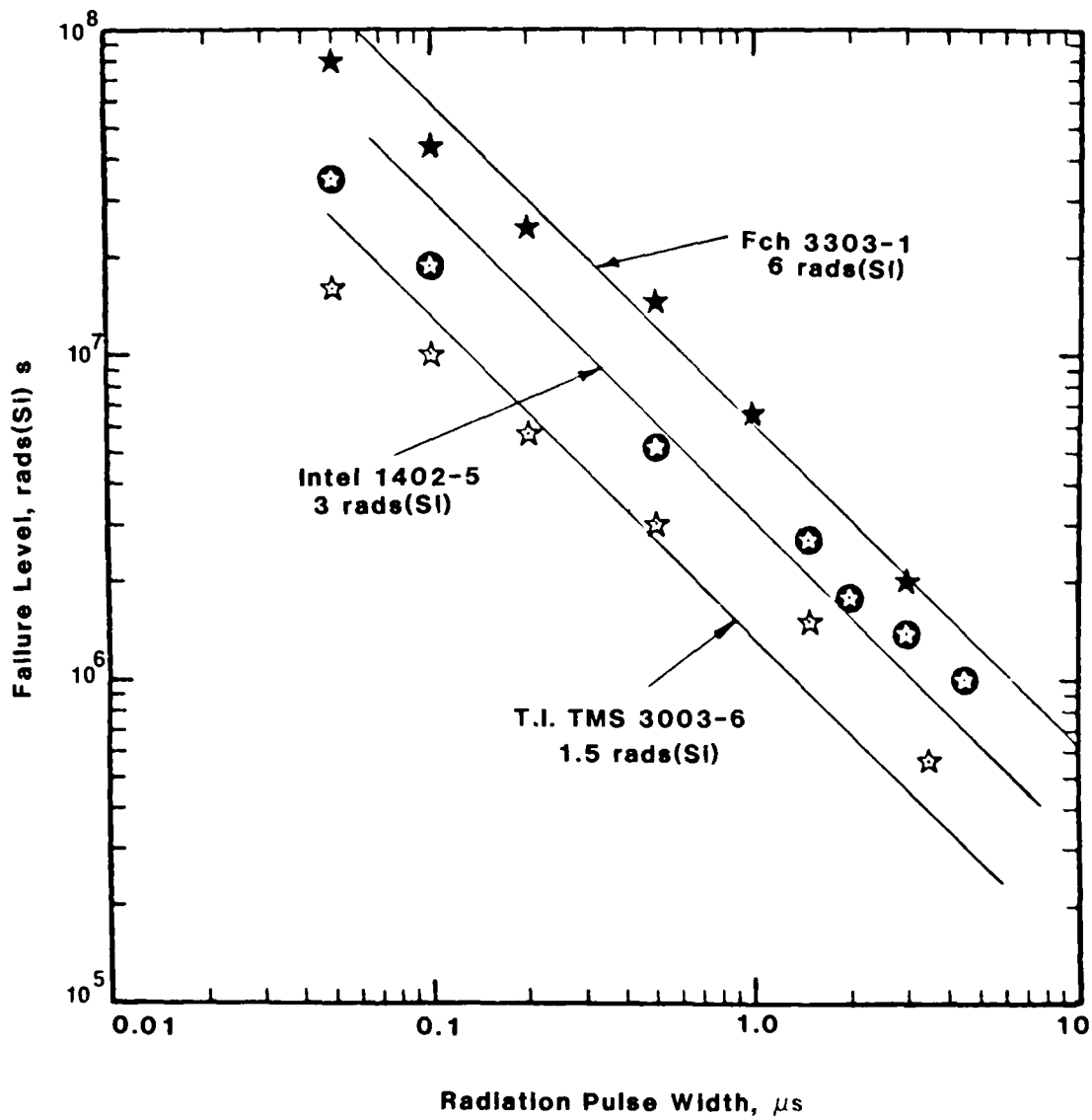


FIGURE 26. SHIFT REGISTER CRITICAL DOSE RESPONSE.

or 0 state. If the radiation pulse occurs after the occurrence of the lead clock pulse ( $\phi_2$ ) and before the lag clock pulse ( $\phi_1$ ) failure appears as the temporary transition of all internal cells to the logic 1 state, and if the radiation pulse appears after  $\phi_1$  and before  $\phi_2$ , failure appears as the temporary transition of all internal cells to the logic 0 state. This is just the response that would be expected if all internal storage capacitors were discharged at the relative timing indicated. On the other hand, the Intel 1402 is organized as two series chains of cells - one for the odd numbered bits and one for the even numbered bits. In this case, the failure appears as a square wave whose frequency is twice that of the clock pulses.

The susceptibility of the dynamic shift registers can be related to the discharge of the storage capacitors by the substrate diode photocurrent. In the case of the steady-state environment, the charge lost on the drain-substrate junction of the transmission gate will be,

$$\Delta Q = qAg_0 \dot{\gamma} L_p \Delta t_{\phi} \quad (64)$$

where  $\Delta t_{\phi}$  is worst-case (greatest) time between the termination of one clock pulse ( $\phi_1$  or  $\phi_2$ ) and the initiation of the other clock pulse ( $\phi_2$  or  $\phi_1$ ). This assumes that the effective resistance at the storage node is so large that the RC time constant is large compared to the period of the lowest clock frequency. This must be the case for normal operation with thermal leakage currents.

Estimation of the absolute values of junction photocurrents requires the knowledge of the junction area and the substrate minority carrier lifetime. The junction area is very difficult to evaluate from a device photomicrograph and, in general, may not be available from the manufacturer. The minority carrier lifetime can be inferred from the waveform of the array power supply photocurrent or substrate diode recovery time.



Given the substrate minority carrier lifetime, and a reasonable value for the substrate resistivity, the minority carrier diffusion length can be specified. The total charge from the junction photocurrent will then be,

$$\Delta Q = qg_0 A \gamma L_p \quad (65)$$

where  $\gamma$  is the total dose in the radiation pulse, assuming that  $\Delta t_{\phi}$  is long compared to the lifetime. As  $\Delta t_{\phi}$  decreases the total charge will decrease as the pulsed photocurrent is truncated. In terms of observable effect then, the radiation failure level should be a constant total dose as long as  $\Delta t_{\phi}$  is long compared to the lifetime, and should increase somewhat at increasing clock pulse frequencies.

The absolute magnitude of the critical total dose (or capacitor charge loss) is determined primarily by the minority-carrier diffusion length, junction parameters, and the MOS transistor threshold voltage. Referring back to Figure 25, the voltage on the storage capacitor will charge essentially to the supply voltage  $V_{DD}$ . Stored information will be compromised when the voltage is dropped below the threshold voltage of the inverter, such that the transistor does not appear "on" at the occurrence of the next clock pulse. This critical charge can then be expressed as,

$$\Delta Q_C = \int_{V_T}^{V_{DD}} (V_{DD} - V_T) C(V) dV \quad (66)$$

$$= \epsilon A \int_{V_T}^{V_{DD}} \frac{(V_{DD} - V_T)}{s_m(v)} dV \quad (67)$$

where  $x_m$  is depletion layer width of the reverse-biased junction. In terms of the ionizing radiation environment, the total critical dose must be,

$$\Delta Q_c = qAg_o \gamma_c L_p \quad (68)$$

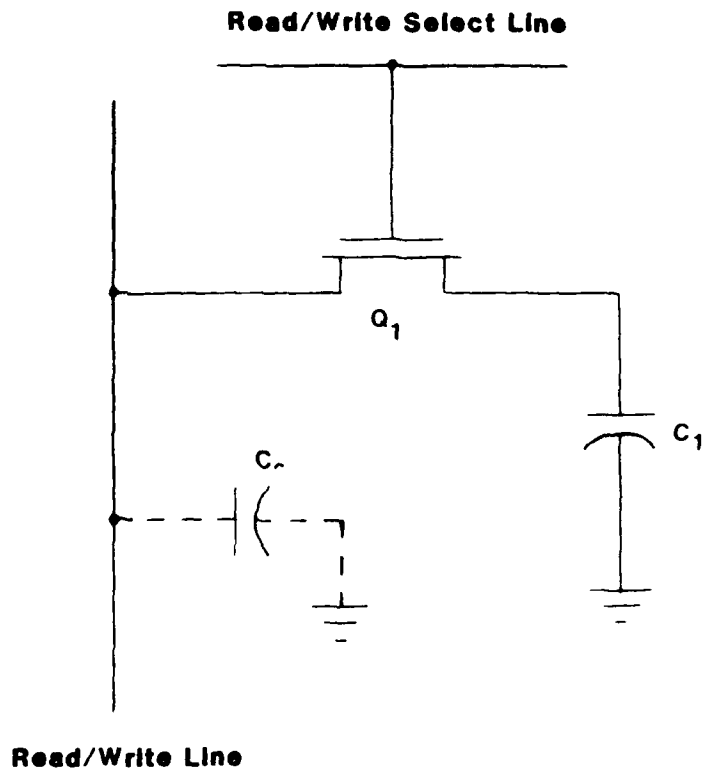
thus defining the total critical dose as,

$$\gamma_c = \frac{\epsilon \int_{V_T}^{V_{DD}} \left[ (V_{DD} - V_T) / x_m(V) \right] dV}{qg_o L_p} \quad (69)$$

The total critical dose is independent of junction area since both the photocurrent and capacitance are proportional to area. To evaluate the critical dose we must know the diffusion length, threshold voltage, and junction parameters (to evaluate the normalized depletion width as a function of reverse-bias voltage). The critical dose for these four types of old dynamic shift registers ranged from approximately 1-10 rads (Si). The point to be emphasized here is the nature of the photore-sponse. The failure mechanism is radiation-induced carriers generated in the critical collector volume of the junction capacitance. With this insight it is much easier to define the tests and analysis required to evaluate the radiation susceptibility of an array in a specific application.

### 3.2.2 Data Loss - Localized Ionization

The technology of data storage in dynamic MOS structure has evolved from the 3-transistor cell of the shift register just discussed to the 1-transistor cell shown in Figure 27. This evolution has resulted in dramatic increases in the size of dynamic MOS memories as well as a dramatic decrease in the charge used to store information in the memory



**FIGURE 27. ONE TRANSISTOR DYNAMIC RAM CELL.**

cell. It was the decrease of the critical charge to less than that generated by an  $\alpha$ -particle that brought the problem of soft errors to critical concern in commercial application. In some ways the sensitivity of a 16 k dynamic memory rivals that of state-of-the-art particle detectors.

The mechanism of soft errors in dynamic MOS memories is the discharge of the data stored on the memory cell capacitance. Since the refresh and circuit time constants are long compared to the pulswidth of the localized ionization transient pulse it is reasonable that a critical charge can be defined to the susceptibility of dynamic MOS memories.

In addition to dynamic MOS memories, charge-coupled device (CCD) arrays also depend on the manipulation of charge between circuit elements.

The susceptibility of microcircuits to localized ionization has typically been determined by measurements with analysis supporting the inferred results on critical charge and carrier collector volume. Particle accelerators are used to simulate the high energy particles of cosmic rays and neutron effects. Results of these studies are reported in a variety of different ways (which may or may not be consistent). If exposure to a given particle fluence and a number of errors are detected following exposure the results may be reported as an error cross-section - defined as the number of errors divided by the particle fluence. If a high energy particle radiation environment is defined (e.g., cosmic ray environment for a given satellite orbit) the results of laboratory exposure may be extrapolated to an expected bit error rate in the system using the critical charge as determined from laboratory experiments and device critical volume determined from microcircuit analysis. Experimental studies and analysis to system effects are discussed in detail in References 41-44. Relative susceptibility of microcircuit to localized ionization effects is summarized in Section 4.4.4.

### 3.3 Static Memory Cell Photoresponse

A static memory cell is a bistable circuit (e.g., flip-flop) used for the storage of a single bit of information. The data can be retained in the cell indefinitely as long as electrical bias is held on the array. The schematic of a simple n-MOS flip-flop is shown in Figure 28<sup>41</sup>. Pulsed ionizing radiation exposure will cause photocurrents and transient logic upset in the memory cells just as in the address decoder, read sense and output interface cells of the array. In addition, the junction photocurrents can dominate the signal biases in the cell to the point where the stored data is lost. The recovery logic state of the cell is then independent of its initial state. For a perfectly symmetrical flip-flop cell exposed to a super-critical ionizing radiation pulse, the cell recovery would be to its initial state on 50% of the exposures and to the logic complement on the other 50% of the exposures. This can be a potential concern in the characterization of a flip-flop or memory array. In some system applications the transient photoresponse of the memory may not be of concern provided that the stored data remain correct. In this case, accurate determination of the worst-case change-of-state radiation level is required. If the flip-flops were symmetrical then it would be sufficient to arbitrarily select a logic state and expose the cell a few times at each of an increasing radiation levels. The probability of observing the critical change-of-state would then be reasonable. Unfortunately flip-flops and memory cells are not symmetrical. Relatively small imbalances in device parameters, layout geometries, or doping profiles can result in a post-irradiation preferred logic state. If the cell is exposed while initially set in the preferred state, a transient response will be observed, but not a radiation-induced change-of-state. Conversely, when initially set in the complement of the preferred state, the flip-flop will switch consistently on every radiation exposure above the critical intensity. Possible photoresponse data on flip-flops with and without strongly defined preferred states is shown in Figure 29.

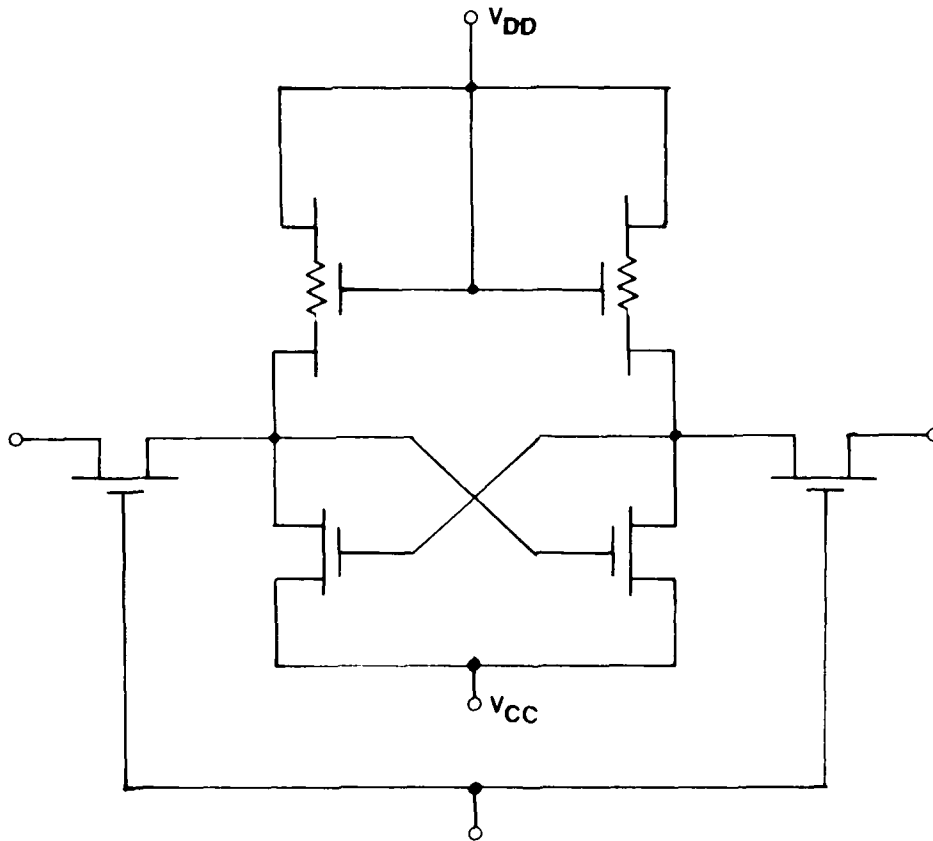


FIGURE 28. N-MOS FLIP-FLOP MEMORY CELL.

(a) No preferred state

Logic state

0	○	○	*	○	*	○	*	*
1	○	○	○	*	*	*	○	*

$\dot{\gamma}$

effect

○ no C-O-S

\* C-O-S

(b) Preferred state

Logic state

0	○	*	*	*	*	*	*
1	○	○	○	○	*	○	*

$\dot{\gamma}$

FIGURE 29. FLIP-FLOP C-O-S RESPONSE.

In general, the probabilistic nature of flip-flops and static memory cell change-of-state photoresponse is an important consideration in experimental characterization. The random preferred state is probably of more concern when testing individual flip-flops, since the statistics of hundreds of memory cells in an array is assuring. Preferred states can, however, be a result of assymetry in cell layout, which can vary for different cells throughout the array.<sup>45</sup> Preferred states can also result in MOS memories by the radiation induced threshold voltage shift, which is a function the gate bias (i.e., logic state). The pattern sensitivity (state dependence) is also of concern in characterizing permanent damage effects in MOS RAM arrays.<sup>46</sup> Potential damaging effects must be considered as exposure accumulates in the characterization of transient photoreponse. In this case, even though the magnitude of the critical change-of-state would probably not change substantially (until the array was close to failure from accumulated ionization) the worst-case data storage for observation of the effect could change with successive radiaiton exposures.

While the preceeding discussion has been oriented principally to bulk ionizing radiation effects, the nature of a preferred state is also important in the bit flips observed in static memories from localized ionizing radiation effects.<sup>46a</sup> There is, however, an important difference in the transient level required for a bit upset. In almost all cases the ionizing track of a high energy particle will cause a transient current in only one transistor of the memory cell. The transient current then appears as a current noise which, with sufficient charge, will change the logic state of the cell. The charge required will be greater when the cell is in its preferred state than when it is in the complementary state. For bulk ionization effects both transistors of the basic cross-coupled cell are disturbed and appear more as a common-mode noise than the unbalanced noise pulse of a localized ionization track. It would be expected that the critical charge necessary for a single even bit flip would



correspond to a noise current pulse substantially lower than the "common-mode" noise currents resulting from bulk ionization. Both effects, however, share the difficulties in observing data loss for the most sensitive state of the memory.

### 3.4 Analog Microcircuit Transient Photoresponse

With the evolution in microcircuit technology, the difficulties in both analysis and testing seem to become very formidable. Occasionally, however, we get lucky and discover a useful simplicity advantageous for both analysis and interpretation of test results. In this case I would like to discuss relatively simple models and analysis useful in simulating the low level photoresponse of analog microcircuits.<sup>47</sup>

A component model of a microcircuit is a tool which can be used by the system designer to optimize design parameters. For example, the designer shapes the electrical performance of an analog system by selecting loop gains; source, feedback and load impedances; as well as frequency compensation networks and circuit topology. A radiation-inclusive model of an analog microcircuit can be derived from the interconnection of all circuit elements with photocurrent generators. Electrical performance and photoresponse can then be calculated using a circuit analysis computer code. The principal difficulties with this approach are: 1) definition of the circuit elements (analog microcircuit designers are very clever and the published schematic does not always show the actual internal circuit topology, 2) determination of electrical and photocurrent parameter values and 3) the cost and running time of a relatively complex computer simulation. An alternative approach is to create a component model of the microcircuit which simulates the microcircuit behavior. Electrical parameter values can be determined from terminal measurements, and the resulting model is much simpler than the detailed model. In this sense the use of component models is very common for electrical performance simulation of

both analog and digital microcircuits. The question, in this case, is how to include the photoresponse in the component model.

The major analytical advantage that can be applied to a wide variety of analog microcircuits is linearity. If the electrical signals within the microcircuit are small compared to the electrical bias, the overall output response will be a linear function of the input signal. This also allows the application of superposition in modeling the microcircuit.

The principle of superposition states that the systems response to any number of simultaneously applied independent energy sources is exactly equal to the algebraic sum of the system's responses to each energy source applied separately. If we consider the system's response to be its terminal currents, and consider the independent energy sources to be the terminal voltages and ionizing radiation, then any linear system in an electrical and radiation environment can be represented by

$$I_i(s) = \left[ Y_{ij}(s) \right] E_j(s) + I_{pi}(s) \quad (70)$$

which, for an n-terminal device,

$I_i(s)$  is the (n-1) x 1 terminal current matrix

$Y_{ij}(s)$  is the (n-1) x (n-1) admittance matrix

$E_j(s)$  is the (n-1) x 1 terminal voltage matrix

and

$I_{pi}(s)$  is the (n-1) x 1 short-circuit terminal photocurrent matrix.

where all terms are Laplace transformed

It should be realized that the admittance and voltage matrices of equation (70) merely represent the system's electrical response, and to

that we have added the system's response to ionizing radiation, the short-circuit (i.e.,  $E_j(s) = 0$ ) terminal photocurrent matrix. It must also be emphasized that the elements of the photocurrent matrix are not necessarily identifiable junction photocurrents within the circuit. Insight into the relationship between response and internal circuit parameters is lost in a component model.

Since it is desirable to use a circuit analysis computer code such as SCEPTRE<sup>27</sup> or other codes, it is necessary to transform the analytical representation of equation 70 into an electrical network topology acceptable to such a code. From equation 70 we see that ionizing-radiation effects can be included by simply adding terminal photocurrent generators to the electrical model which, in this case, is characterized by the admittance parameters of the device.<sup>47</sup> A general network which can be used to realize the admittance parameters on a circuit analysis computer code is shown in Figure 30. A specific model used in the analysis of the  $\mu$ A709 operational amplifier is shown in Figure 31. In this case the frequency dependence of the gain is included in the dependent current sources, and the driving point impedances could be treated as resistive up to reasonable frequencies and pulse widths as shown by the frequency response and transient response shown in Figure 32.

With the electrical-model parameter values defined, it is necessary to determine values for the terminal photocurrent generators. In so doing, however, it is enlightening to at first consider the photoresponse of any high-gain, narrow-bandwidth linear microcircuit (such as an operational amplifier) to narrow-pulse transient ionizing radiation. If the upper-cutoff frequency of the device is small compared to the reciprocal of  $2\pi$  times the width of the radiation pulse (which is usually the case), the output photoresponse is essentially the "impulse" response of the device. It should be realized that the impulse response of any linear system is determined by the area under the impulse and not the actual

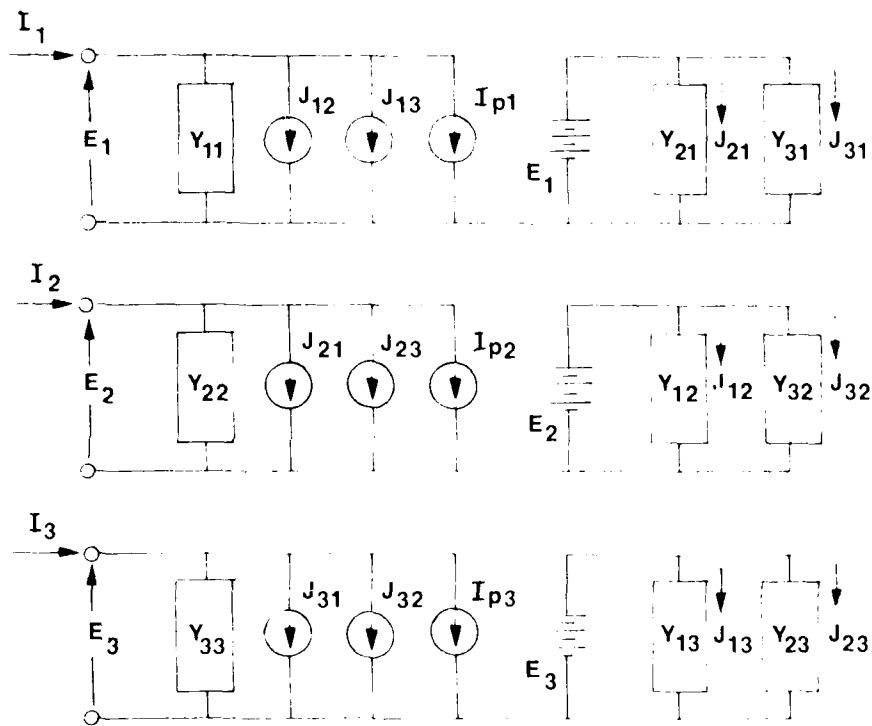


FIGURE 30. GENERALIZED RADIATION-INCLUSIVE ADMITTANCE MODEL.<sup>47</sup>

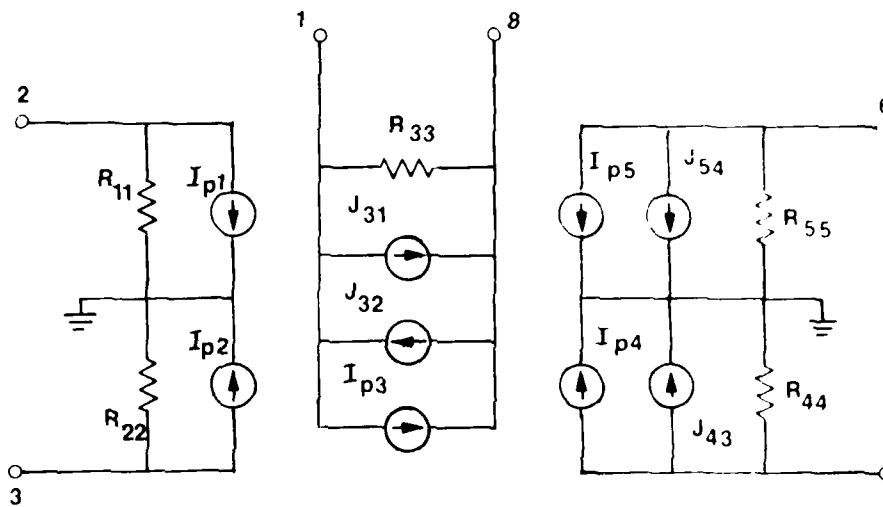
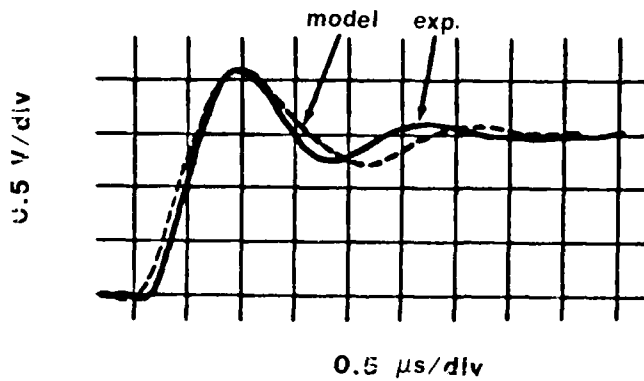
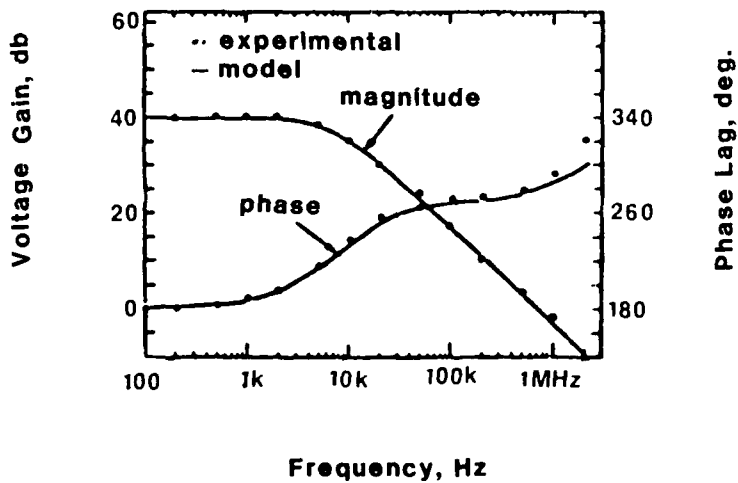


FIGURE 31.  $\mu A709$  SIMPLIFIED LINEAR RADIATION INCLUSIVE MODEL.<sup>47</sup>



(a) Step-Function Response



(b) Closed-Loop Frequency Response

FIGURE 32.  $\mu$ A709 TRANSIENT AND FREQUENCY RESPONSE.<sup>47</sup>

time-dependent amplitude. Therefore, for the  $\mu$ A709 we can assume that  $I_{pp}(t)$  follows the radiation pulse, and thus the terminal photocurrent generators can be of the form

$$I_{pi}(t) = k_i \dot{\gamma}(t) \quad (71)$$

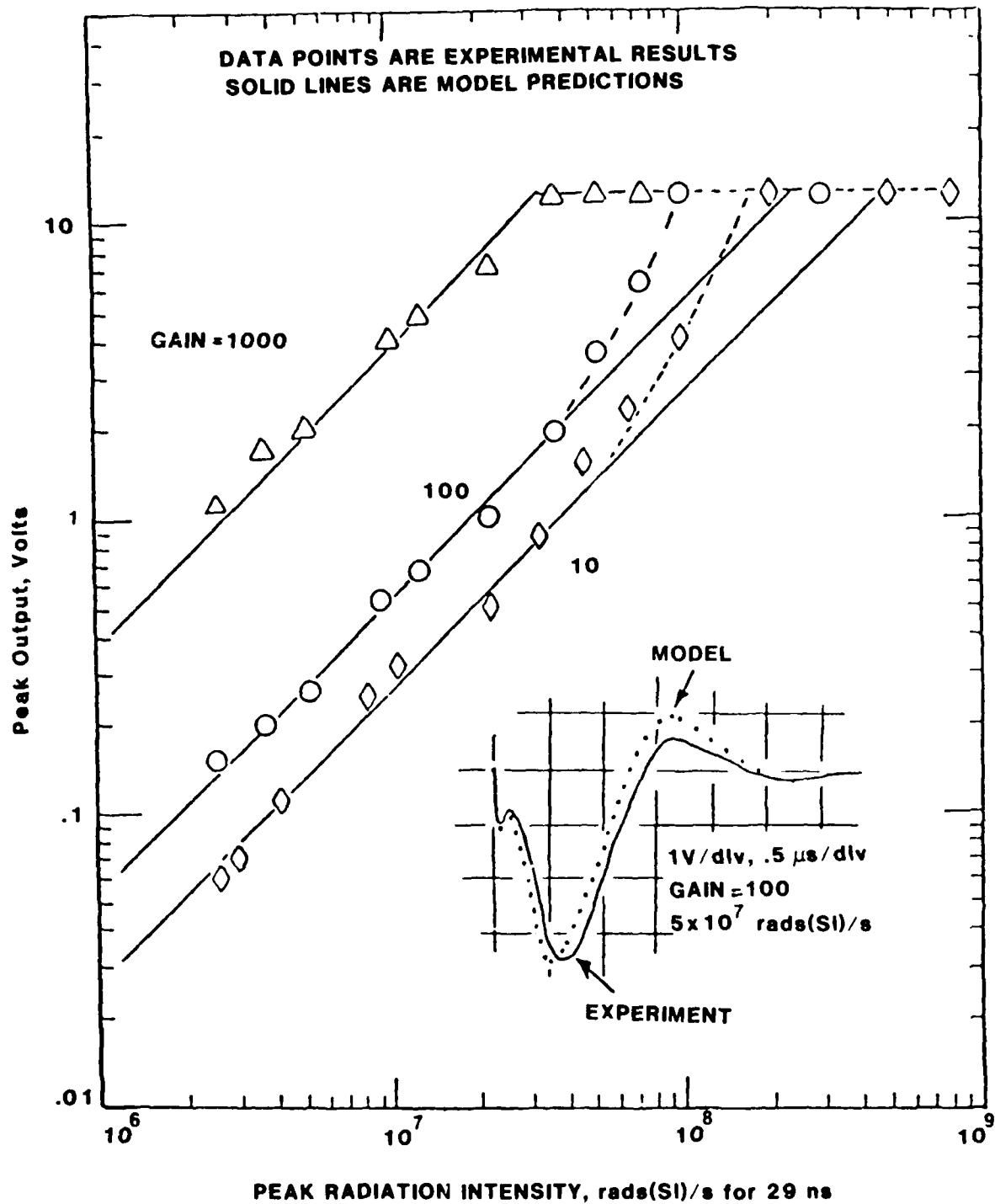
where  $\dot{\gamma}(t)$  is the ionizing dose-rate radiation intensity as a function of time, and the  $k_i$  are experimentally determined scaling factors.

Comparison of model photoresponse predictions and experimental data for closed loop gains of 10, 100, and 1000 are shown in Figure 33. The model accurately represents the small-signal electrical behavior and transient photoresponse of the  $\mu$ A709 operational amplifier for all reasonable parametric variations of source, load, feedback, and compensation networks.<sup>47</sup>

As the radiation intensity is increased, the transient photoresponse will increase until non-linear effects occur, and the linear model is no longer an accurate simulation. Extensions of the component model to include non-linear effects have been investigated, but no general solution form has been developed.<sup>48-50</sup>

### 3.5 Radiation-Induced Latch-up

The possibility of radiation-induced latch-up is a concern for almost all microcircuit technologies.<sup>51-53</sup> The exceptions are: CMOS/SOS, hardened dielectric-isolated bipolar and low voltage integrated-injection logic. The effect is the initiation of an anomalous high current path within the microcircuit that inhibits normal circuit operation. Latch-up will persist until either the power supply is interrupted or until the microcircuit burns out.



**FIGURE 33.  $\mu$ A709 PHOTORESPONSE <sup>47</sup>**



The mechanism involved, in the context of this discussion, is the potentially regenerative characteristic of a semiconductor pnpn path. In general, however, other device, circuit and system effects can result in an unrecoverable effect from ionizing radiation-induced transient. These effects might include regenerative paths in semiconductors due to transistor second breakdown, phase reversal in complex feedback (lock-up) or recovery to an unexpected digital state for which there is no system software provision.

### 3.5.1 Basic DC Characteristics

The regenerative pnpn path can be considered as the combination of a pnp and an npn transistor as shown in Figure 34. The d-c current-voltage characteristic of the pnpn path is shown in Figure 35. In the microcircuit the path will normally be biased at the high-voltage, low-current operating point. The current is generally very low and does not interfere with ordinary circuit operation. The increased current of the I-V characteristic is due to the voltage breakdown of the center p-n junction. The avalanche breakdown current is in the forward bias direction for the emitters of the pnp and npn transistors. With the transistors in the active bias region the collector-base junctions form a positive feedback loop, i.e., the pnp collector current equals the npn base current which is multiplied to become the npn collector current which equals the pnp base current. The positive feedback path becomes regenerative if this closed-loop current gain is greater than unity or if,

$$\beta_{\text{PNP}} \cdot \beta_{\text{NPN}} \geq 1$$

in terms of the transistor common-emitter current gain. Since the common-base current gain  $\alpha$  can be expressed as,

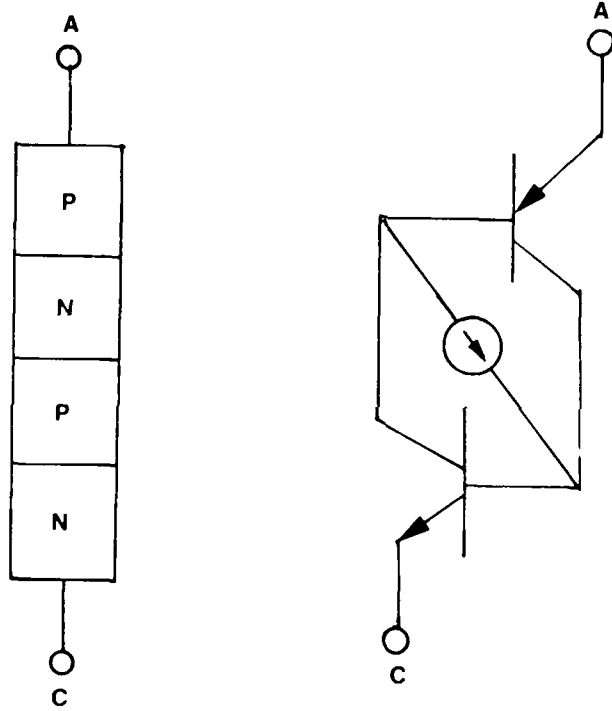


FIGURE 34. TWO TRANSISTOR SCR MODEL.

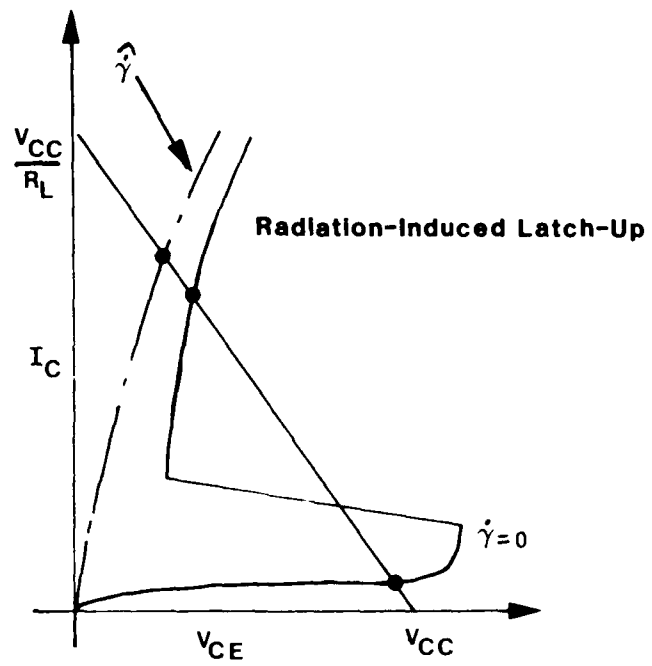


FIGURE 35. SCR I-V CHARACTERISTIC.

$$\alpha = \frac{\beta}{1 + \beta}$$

the regenerative criteria can also be expressed as,

$$\alpha_{\text{PNP}} + \alpha_{\text{NPN}} \geq 1$$

In the electrical SCR characteristic it is the increase in transistor bias current in the breakdown region that brings the transistor gains above the regenerative point and the I-V characteristic switches to a low-voltage, high-current region of operation. Latch-up can be produced in a microcircuit by increasing the voltage above the breakdown voltage.

The principal concern in this discussion is the initiation of high-current, low-voltage latch-up path by a pulsed ionizing radiation environment or single particle ionization track. Latch-up is initiated by the primary photocurrent of the central junction as shown in Figure 34. The primary photo current initiates forward conduction of the transistors and, if circuit bias conditions allow, initiate latch-up.

The critical parameter of the d-c latch-up characteristic as a parasitic path in the microcircuit is the minimum holding current, holding voltage shown in Figure 36. If the circuit can sustain operation at a higher current-voltage point then the question of latch-up reduces to the critical radiation environment required. On the other hand, if the holding current-voltage point cannot be sustained then latch-up will not occur in the microcircuit at any radiation level.

The idealized structure of the SCR pnpn path as shown in Figure 34a must be modified to simulate the critical parameters of the microcircuit parasitic path. In the microcircuit the transistors are generally unintentional and may have low gain and slow switching times. In terms of the schematic, shunt and series resistances must be included to accurately

represent the critical holding current and voltage as shown in Figure 36. Shunt resistance across the emitter-base junction of a transistor has a dramatic effect in reducing the effective transistor gain at low emitter currents. Thus, the values of the shunt resistors in Figure 36 will have a substantial effect on determining the latch-up holding current. The series resistors in the parasitic pnpn path act as negative feedback reducing the effective transistor gain which will increase the holding voltage. The variation in d-c characteristics of the pnpn path has been investigated by Estreich<sup>54</sup> and Oclasa<sup>55</sup>.

### 3.5.2 Microcircuit Latch-up

Crowley<sup>56</sup> has suggested an analytical technique which can be used to identify microcircuits that may potentially latch-up when exposed to an ionizing radiation environment. The technique includes a topographic examination of the chip to identify potential p-n-p-n paths, analysis of electrical bias conditions to determine if latch-up is possible (for example, if the circuit anode-cathode bias is negative latch-up will not occur), and measurement of the parasitic gains of potentially critical latch-up paths to determine a potential microcircuit problem. This technique has generally been applied to the analysis of junction-isolated bipolar TTL microcircuits.

Crowley's analytical technique has been applied by Pease<sup>57</sup> to the analysis of a variety of advanced bipolar LSI array technologies. Pease concluded that high-voltage analog-digital arrays were potentially susceptible to latch-up and that latch-up was possible but not likely in advanced operational digital arrays such as ECL, ISL and STL. Typically latch-up may be possible in a wide variety of arrays from the criteria of the produce of the transistor gains but is prevented by circuit bias conditions.

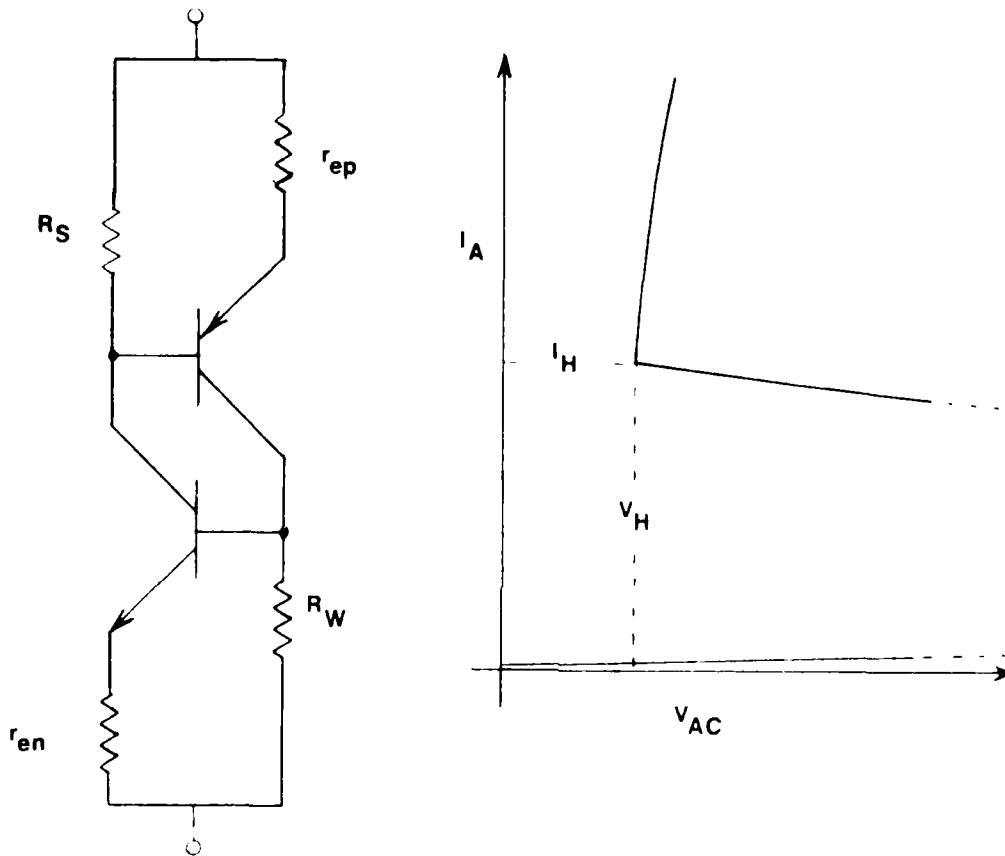
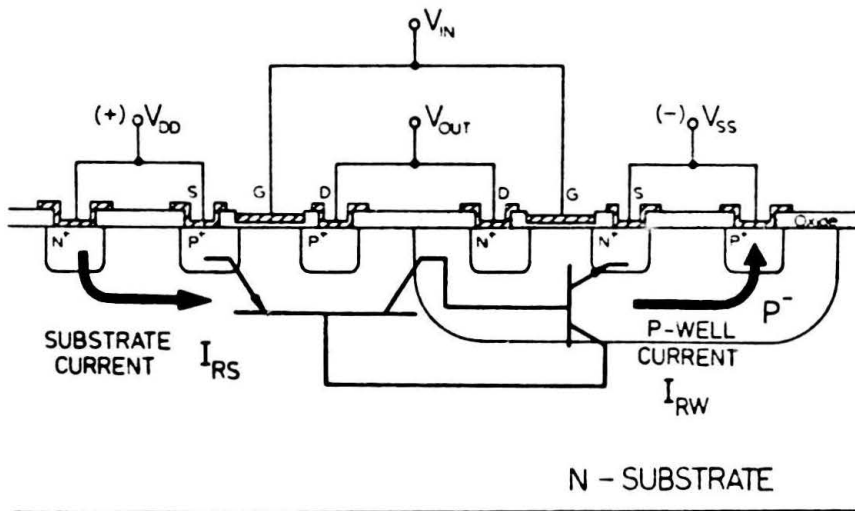


FIGURE 36. PNPN PATH WITH SHUNT AND SERIES RESISTANCES.

Radiation-induced latch-up is a significant concern for junction-isolated (bulk) CMOS microcircuits. CMOS radiation-induced and electrical-induced latch-up has been extensively studied and mitigating processing variations have been identified and demonstrated.<sup>58-60</sup> One of the critical CMOS latch-up paths is shown in Figure 37. Critical parameters, as for all latch-up paths are the transistor gains and resistance values. The possible effect of holding current on the shunt resistance values, as calculated by Estrich, is shown in Figure 38. The critical influence of holding current on shunt resistance has led to hardening by fabricating the circuit in a epitaxial film on a low resistivity substrate.<sup>60</sup> CMOS latch-up hardening has also been demonstrated by reducing the parasitic transistor gains with the use of gold-doping or neutron irradiation.<sup>58,59</sup>

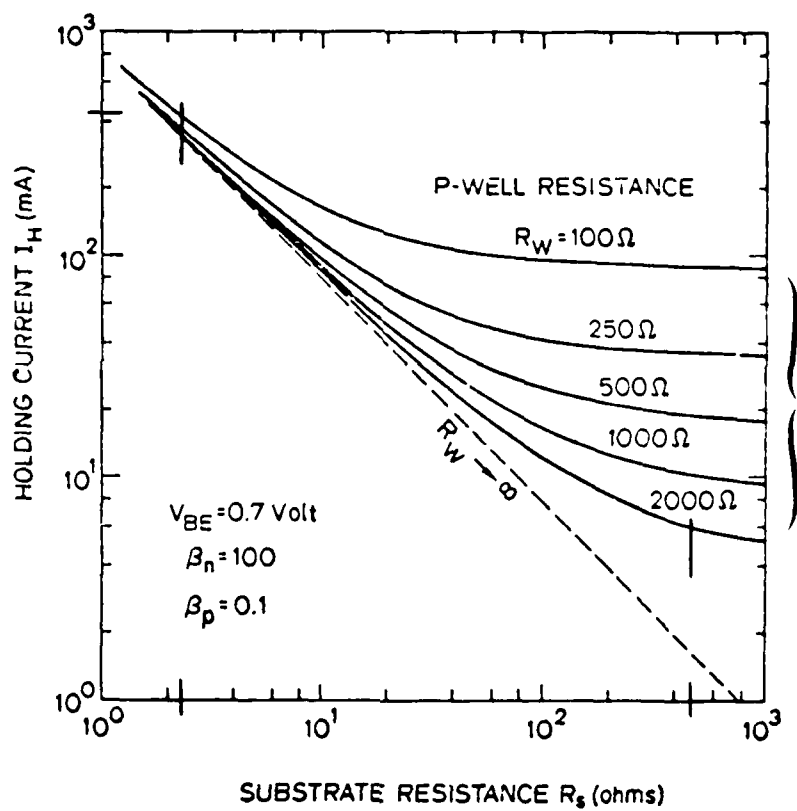
The issue of microcircuit latch-up can also be addressed on the system level. External current limiting can be used to decrease the current available to the microcircuit to below the holding current and prevent latch-up<sup>61</sup>. The current limiting network must be designed with consideration of overall system design parameters. Alternatively, the initiation of latch-up can be detected by excess power supply current and the system power voltage can be dropped and subsequently restored. The decrease in power supply voltage will break the latch and normal circuit operation will be restored. Critical design problems are detection of the excess power supply current and timing in the power supply requirements.

As microcircuits continue to increase in complexity there is concern that a potentially critical latch-up path could be activated internally without a measurable increase in the overall power supply photocurrent. The approach, in this case, is to operationally check the functional performance of the microcircuit following the radiation exposure. This makes the test more time-consuming, but with the observation of the power supply current, should detect any radiation-induced latchup.



**FIGURE 37. CMOS LATCH-UP PATH.**





**FIGURE 38. FUNCTIONAL DEPENDENCE OF LATCH-UP HOLDING CURRENT WITH EMITTER-BASE SHUNTING RESISTANCES.**

#### 4. TRANSIENT EFFECTS IN COMPLEX MICROCIRCUITS

An understanding of the nature of the basic logic cells is an essential guide to the analysis and testing of complex arrays. There are many very important questions which must yet be answered. The principal issue is that of cost-effectiveness. Analytical and experimental techniques used for devices and basic microcircuits can be directly applied to the study of LSI arrays.<sup>62</sup> The problem is that the time and effort required becomes prohibitive as the number of gates in the array increases to hundreds or thousands. In the following discussion I will try to comment on the current concerns and advantages of present techniques.

At this point it should be clear that the worst-case logic upset level of an LSI array is a function of the logic state during pulsed radiation exposure. In an LSI array there may be thousands of internal logic states, and it is clearly impractical to measure the upset level for each state. Even if the economics were realizable, the total accumulated ionization dose could cause circuit failure before the experimental series was completed. In this case, analysis can be of essential aid in defining a reasonable set of test conditions which include the worst-case. Before discussing analysis, however, the nature of LSI testing will be discussed. LSI testing can be categorized in one of two basic modes: static and dynamic. In static testing a specific logic state is established by dc logic inputs and initialization of internal memory cells. The output(s) response(s) are then monitored with increasing radiation intensity until logic upset or memory change-of-state is observed. If enough logic states are included in the characterization the worst-case upset will (may?) be observed in the output photoresponse. An alternative approach is dynamic testing. In this case the array is actively operated during the radiation exposure. There are two important options in dynamic testing: narrow-pulse exposure (typically < 100 ns) may more nearly represent the radiation environment of concern, but introduces the problem of relative timing between the radiation pulse and array electrical timing and

processing flow. The concern is that, for particular relationships in timing, the array logic upset susceptibility could be much greater than for arbitrary timing. In a wide pulse dynamic tests (typically  $> 1 \mu\text{s}$ ) it is possible to operate a relatively fast array through a few cycles during the radiation exposure. In this case the observation of the output response can reveal the inability of the array to perform a requested function as well as the presence of a logic error. This class of logic error "by omission" rather than by "commission" could also probably be observed in either the static logic tests or the narrow-pulse exposure. Wide pulse testing, however, should give greater latitude in logic state coverage (compared to static testing) or relative radiation pulse timing (compared to narrow-pulse, dynamic testing).

In general, I recommend a progression of static, dynamic wide-pulse and dynamic narrow-pulse testing for microcircuit characterization. To be consistent with the real requirements for cost and schedule, analysis should be used to identify the most probable worst-case test conditions in each case. In practice, however, quick examination of the data and adaptive redirection of the test conditions will be essential to a confident characterization.

From a system perspective I would also like to mention that a complete characterization of the array photoresponse should include measurement of the power supply photocurrent. In a junction-isolated microcircuit the principal effect is that of the substrate junction photocurrents and the sum of all these photocurrents for all elements is a substantial photocurrent through the power supply. As a rule of thumb, the power supply photocurrent in a junction-isolated microcircuit is like a diode with 50% of the chip area. Therefore for a 200 mil  $\times$  200 mil chip, a substrate lifetime of  $1 \mu\text{s}$  and a radiation pulse width of 100 ns, the power supply photocurrent will be on the order of 150 mA for an exposure to a  $10^7$  rads (Si)/s radiation pulse. Measured power supply photocurrents

for a variety of microcircuits are shown in Figure 39.<sup>19</sup> It would be expected that power supply photocurrents could be relatively important in arrays that use switched totem pole transistors for logic such as junction-isolated TTL or CMOS arrays. Fortunately CMOS is relatively tolerant to power supply voltage transients. The relative importance of power supply transients would not be expected to be quite as high for ECL or I<sup>2</sup>L logic arrays, because of the nature of the logic cells, or in dielectric-isolated bipolar or CMOS/SOS arrays because of the elimination of the large substrate photocurrents.

#### 4.1 Analysis in Support of Testing

As mentioned previously, the problem of experimentally determining the worst-case level for an LSI array is a formidable, essentially unsolved, problem. I believe that the photoresponse of an array must, ultimately, be defined in a hard radiation laboratory environment which can be directly related to the specified system environment. The problem to be solved, in my opinion, is to define a reasonable number of test conditions that will allow observation of the worst-case logic upset. That is, not only must it be in a state of maximum sensitivity, but the test must be such that the logic failure is observed as an erroneous output signal.

Two approaches have been advocated which work toward solving the LSI testing problem: the first is the use of analysis to identify the worst-case set of test conditions (i.e., test vectors), and the second is the use of a pulsed laser as a source of excitation to non-destructively emulate the pulsed radiation environment and allow experimental explorations to test conditions.

Analysis of an LSI array in terms of detailed models of the circuit elements is as economically absurd as the experimental measurement of

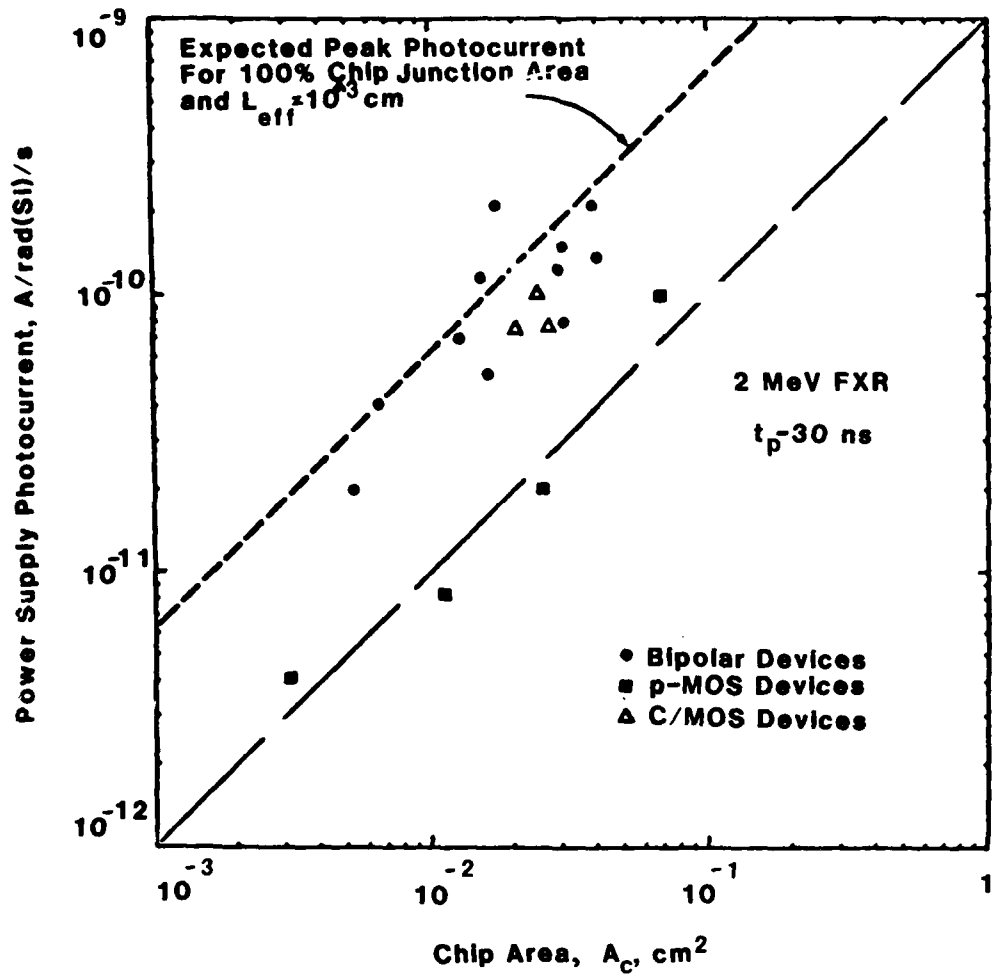


FIGURE 39. MICROCIRCUIT POWER SUPPLY PHOTORESPONSE

the photoresponse is all possible logic states. Fortunately such detailed modeling is unnecessary. In modeling a logic cell it is important to keep the insight of cell performance in terms of circuit topology and circuit element parameters. It is also important to retain the capability of defining cell performance as a function of input and output circuit interfaces. Once the logic array is defined, however, the cell topology, the element parameters and interfaces are fixed. In terms of modeling we then have four possible approaches depending on the design parameters of concern (summarized in Figure 40):

- 1) detailed cell modeling - including element parameters without interface boundary conditions for cell analysis and performance optimization.
- 2) simplified logic cell modeling - transfer function representation of internal cell behavior with general interface simulation for performance analysis of groups of cells.
- 3) transfer function simulation - overall simulation of the dc and transient cell performance for defined interfaces for detailed analysis of array performance.
- 4) logic simulation - simplified simulation of cell transient performance for overall analysis of array performances.

Analytic capability has been developed and demonstrated for all these levels of array simulation.<sup>63-72</sup> Given the opportunity to start with the array design, radiation-inclusive detailed circuit analysis can be performed by adding photocurrents to the electric model. As the array design evolves worst-case interface conditions can be used to define the worst-case upset level for each type of logic cell in the array. The worst-case logic upset of the array can then be identified by the response of the

**ANALYSIS**

**Detailed Cell Modeling**

**Simplified Logic Cell Modeling**

**Transfer Function Simulation**

**Logic Simulation**

**TEST**

**Direct Observation**

**Comparison To "Gold" Device**

**Pulsed Laser Emulation**

**FIGURE 40. LSI Modeling/Test Approaches**

most sensitive logic cells. The cell analysis will define the nature of the cell response (i.e., 0-1 or 1-0 transient). Logic simulation codes can then be used to identify the array input test conditions which will allow observation of the worst-case upset in radiation tests. The radiation-induced cell logic upset can be included in the logic simulation computer program by adding a logic input to the logic cell such that a logic input (the radiation pulse) causes a logic transition as defined by the detailed cell analysis.

The same approach can be used for the analysis of arrays already designed without concern for photoresponse effects. The problem is, of course, that it is very difficult to get detailed parameter data, circuit layouts and logic diagrams from the array manufacturer. Inferring these data from the examination of the chip and probe electrical measurements is possible but very laborious. Analysis can still be used to aid in the definition of critical test vectors if an accurate logic diagram can be defined in terms of actual logic in the array and not just a schematic of the overall performance functions of the array. This is necessary because the logic faults introduced analytically must reflect unique internal test conditions. Without detailed information or analysis of the test cells it is necessary to assume arbitrary failure modes for the radiation-induced logic upset of each type of cell. This will necessarily result in a substantial expansion of the required test conditions.

The minimum number of test vectors necessary to determine the worst-case logic upset in an array containing logic and memory elements has not been determined. Krebs<sup>69</sup> determined that the minimum number of test vectors for an array containing only logic circuits (i.e., combinational array) cannot be less than the number of internal logic gates. Estimates on the upper limits for a logic/memory array is the number of logic states in the array and all their possible combinations, including time-sequence effects for the memory cells. The upper limit, for even a modest size, is out of range for any reasonable consideration.



Another approach to attack the problem, particularly for arrays designed and fabricated, is to use a pulsed laser to excite a test sample. The use of a laser to simulate the response of semiconductor devices was suggested by Habing<sup>72</sup>, but variations in absorption in the semiconductor and shadowing of the metallization generally prevent a quantitative correlation between the optical-and hard-radiation device photoresponse. Ellis has pointed out, however, that nature of the optical photoresponse is qualitatively identical to the radiation photoresponse and correlation can be established for each particular array type<sup>73</sup>. The use of optical radiation to investigate the array photoresponse offers two substantial advantages: first, the accumulation of optical radiation is non-damaging and threshold voltage or gain degradation induced by accumulation by hard ionizing radiation is not a problem, and second, once the array is delidded, the test set-up is relatively convenient and inexpensive. I believe that the best possible test strategy, in the absence of a rigorously defined set of worst-case test vectors, is the opportunity for an investigator to conveniently expose a large number of possible test conditions with the capability to adapt the test strategy based on observed results.

#### 4.2 Summary of Complex Microcircuit Effects

The analysis and test of current microcircuit technologies is of continuing interest. It is very tempting to review published data and suggest failure ranges for microcircuit technology families. I will present a summary of these data on a variety of microcircuit technologies as a form for conclusion.<sup>39,74</sup> Typically, published data represents effects observed in a laboratory radiation environments with the microcircuit under nominal conditions of bias voltage(s), load and operating temperature. Laboratory test data must be carefully interpreted in terms of the system requirements. Caution must also be employed in relating effects observed on one member of technology family to the other members. If the failure mechanism involves detailed geometrical of the elements there may

be significant (e.g., order-of-magnitude) variations in upset level between members of the same family.

#### 4.2.1 Bulk Ionization Effects

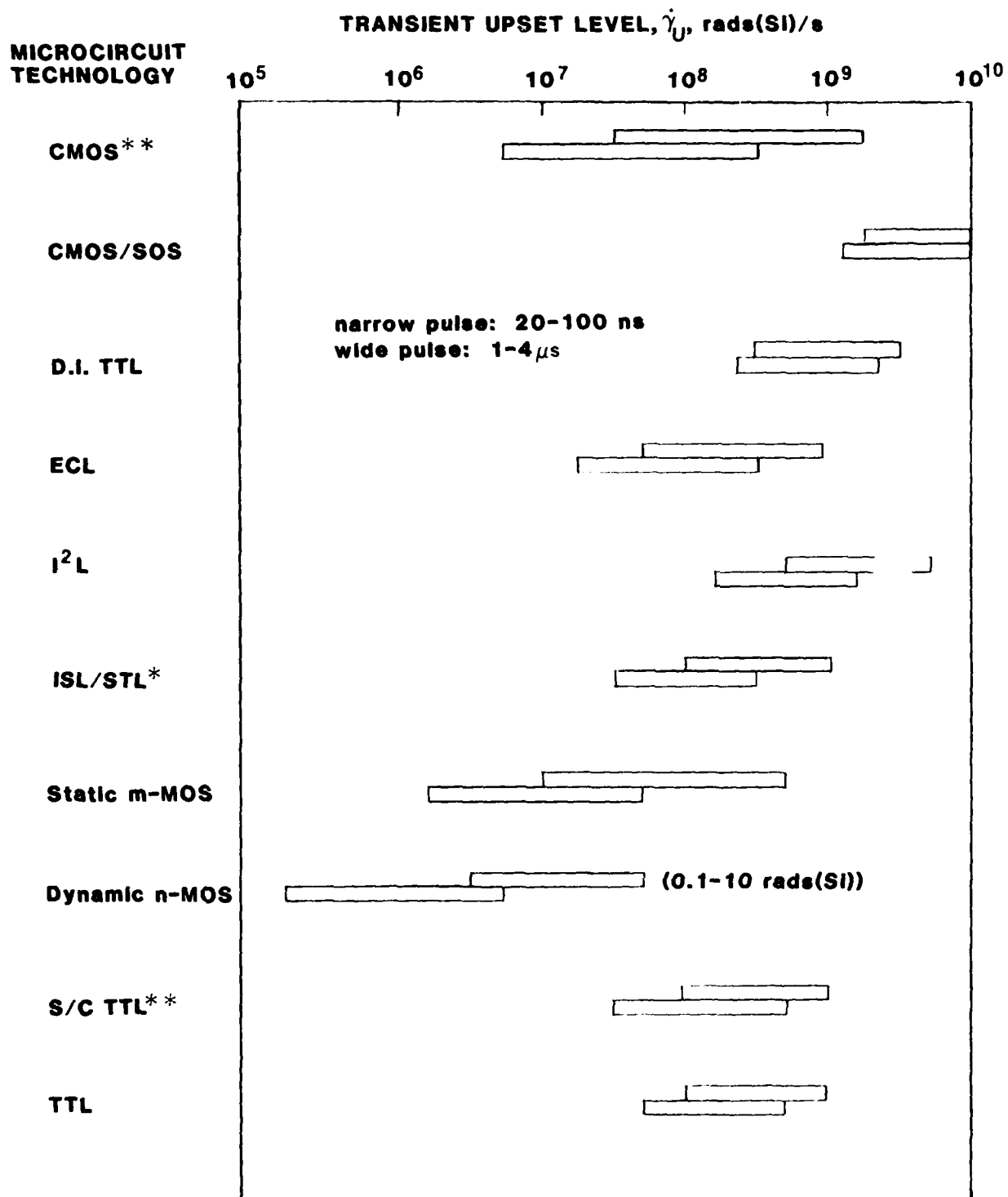
An overall summary of estimated transient upset levels is presented in Figure 41 for a number of complex digital microcircuit technologies exposed to narrow- and wide-pulse ionizing radiation environments (listed in alphabetical order). In general, these technologies using junction isolation and high lifetime substrates will show substantially lower upset levels for a wide pulse exposure for the narrow pulse exposure.

##### 4.2.1.1 CMOS

The transient upset level of CMOS arrays is a significant function of radiation pulse width and supply voltage. Minimum upset levels are at maximum pulse width and minimum supply voltage. Radiation-induced latch-up is of substantial concern. Worst-case operating conditions for latch-up are maximum supply voltage and maximum chip temperature. Power supply photocurrent can be substrated and must be accommodated in system design at the risk of decreasing the logic upset level.

##### 4.2.1.2 CMOS/SOS

The minimum volume of active semiconductor results in high upset levels and very little pulse width dependence. As with CMOS the upset level increases with increasing supply voltage but may be limited by radiation-induced conductivity of the dielectric substrate. Radiation-induced latch-up is not a concern because of the isolation between elements.



\*\* substantial latch-up concern  
 \* significant latch-up concern

**FIGURE 41. SUMMARY OF ESTIMATED TRANSIENT UPSET LEVELS**

#### 4.2.1.3 D.I. TTL

It has been assumed that all elements are individual dielectric tubs and photocompensation is used to increase the upset level. Transient upset levels are high, and not a strong function of pulse width but somewhat lower than CMOS/SOS because of increased volume of individual elements. Under the same assumptions, pnpn latch-up is of no concern. It must be pointed out, however, that "commercial" dielectric arrays may use multiple elements in a single dielectric tub which could lead to decreased upset levels and the possibility of radiation-induced latch-up.

#### 4.2.1.4 ECL

The relatively low upset levels are related to the relatively small voltage signal levels. The pulse width dependence is the result of a typical high lifetime substrate. Radiation-induced latch-up has not been observed in ECL arrays.

#### 4.2.1.5 I<sup>2</sup>L

It has been assumed that the entire array is "non-isolated" I<sup>2</sup>L which uses low supply voltage. The basic compensation of photocurrents within the cell results in the relatively high logic upset levels. The high-lifetime substrate leads to the dependence of upset level on pulse width. In the non-isolated I<sup>2</sup>L structure radiation-induced latch-up is of no concern. If, however, the I<sup>2</sup>L array is used with high-voltage interface or analog circuits radiation-induced latch-up is a substantial concern.

#### 4.2.1.6 ISL/STL

Integrated Schottky Logic (ISL) and Schottky Transistor Logic are advanced bipolar LSI technologies. The upset levels at narrow pulse

exposure are moderate because of small device geometries. The decrease in upset level with pulse width is the result of increasing substrate photocurrents. Radiation-induced latch-up does not seem to be a concern in the basic low voltage gates but may be a concern in the higher voltage junction-isolated interface circuits.

#### 4.2.1.7 n-MOS

The transient upset levels of static n-MOS are moderate and consistent with the substrate photocurrents and dependence of the high-lifetime substrate photocurrents with radiation pulse width. The transient upset level of dynamic n-MOS is essentially determined by the total dose in the ionizing radiation pulse. Thus, transient upset can be observed at very low dose rates for very long radiation pulses. The determination between static and dynamic n-MOS may not be obvious to the user. The development of on-chip refresh time makes the electrical operation appear as static but dynamic cells are used internally (e.g., the Fairchild F-9 microprocessor<sup>75</sup>).

The observation of transient upset level of n-MOS arrays may also be influenced to oxide trapped charge effects and the associated short-term annealing. Total dose failure levels for commercial n-MOS arrays can be as low as 500-2,000 rads(Si). The total dose in a  $10^8$ , 1  $\mu$ s pulse is 100 rads(Si). A single pulse exposure may then be close to the permanent damage failure level and certainly multiple exposures in an attempt to find the worst-case upset level will result in significant total dose-induced degradation. No radiation-induced latch-up has been observed in an n-MOS array.

#### 4.2.1.8 Schottky-TTL

The transient logic upset levels are typically moderate with a substantial decrease in upset level at wide radiation pulses. The pulse

width dependence is due to carrier collection from the high lifetime substrate. The upset levels are typically lower for low power SC TTL than for the high-speed SC TTL microcircuits. Radiation-induced latch-up is of significant concern, particularly in the output totem-pole interface network.

#### 4.2.1.9 TTL

The transient logic upset levels of gold-doped TTL microcircuits are essentially the same as those of SC TTL for narrow pulse exposures. Since the substrate lifetime in gold-doped TTL is much less than that of SC TTL the upset level does not decrease as dramatically with increasing pulse width. Latch-up is possible in TTL but because of the relatively wide spacing of elements and the low-lifetime substrate is not a significant concern.

#### 4.2.2 Localized Ionization Transient Effects

An overall summary of reported effects in complex digital microcircuits is shown in Figure 42 in terms of critical charge. Definition of the critical charge is necessary but not sufficient to the determination of a bit error rate. The effective surface area and carrier collection depth (i.e., critical volume) must also be known to estimate the transient currents from a given environment. In addition the circuit parameters of the cell may also be important in relative hardness between microcircuit technologies. In this discussion, critical charge is used just as a first-order comparative parameter between technologies.

##### 4.2.2.1 CMOS

Transient upset and latch-up have been observed on junction-isolated CMOS as a result of single particle localized ionization. The

MICROCIRCUIT TECHNOLOGY	SINGLE ERROR CROSS-SECTION, cm				ref.
	Critical Charge pC	120-140 MeV Kr 0	20-300 MeV p	14 MeV n	
CMOS	0.1-0.8	$8-9 \times 10^{-3}$			80
CMOS/SOS		$0.3-20 \times 10^{-5}$			79
n-MOS					76-78, 82
64 k d-RAM	~0.1		$3 \times 10^{-7}$	$\sim 1.5 \times 10^{-6}$	
16 k d-RAM	0.2-0.5		$0.1-1 \times 10^{-8}$	$0.4-90 \times 10^{-9}$	
4 k d-RAM	0.3		$\sim 1 \times 10^{-8}$	$0.4-6 \times 10^{-9}$	
4 k s-RAM	0.2-0.8		$0.2-80 \times 10^{-9}$	$\sim 3 \times 10^{-9}$	
$\mu P$	~0.1			$0.3-2.7 \times 10^{-11}$	
IL	0.1-0.7	$0.8-12 \times 10^{-5}$			81
SC/TTL		$0.2-26 \times 10^{-6}$			83

FIGURE 42. SUMMARY OF MICROCIRCUIT LOCALIZED IONIZATION SUSCEPTIBILITY

critical charge and single error cross section shown in Figure 42 represent effects on a very sensitive high density memory. Data on many other CMOS microcircuits indicates much lower susceptibility.

As with bulk ionization effects, the SEU susceptibility of CMOS decreases with increasing supply voltage. Unfortunately the higher supply voltage will probably increase latch-up susceptibility. Data on an epitaxial CMOS memory suggests substantial latch-up hardening compared to the non-epitaxial memory.

The relatively high SEU susceptibility of CMOS seems to be in contrast to the relatively low susceptibility to bulk ionizing radiation effects. It is possible that junction photocurrents compensate within the basic CMOS inverter under uniform ionization and the advantage of compensation is lost when transient current is induced in only a single element.

#### 4.2.2.2 CMOS/SOS

the SEU susceptibility of CMOS/SOS memories is substantially less than that of bulk CMOS memories. It would be expected that the critical charge of the CMOS/SOS memory cells would be the same or less than bulk CMOS cells. The relative decrease in susceptibility illustrates the effect of the substantial decrease in collection volume. The use of dielectric substrate also eliminates latch-up susceptibility.

#### 4.2.2.3 n-MOS

The SEU susceptibility of dynamic n-MOS RAMs has been a major concern in the semiconductor industry because of  $\alpha$ -particles from the package. As shown in Figure 42, the critical charge decreases with decreasing cell size (or increasing memory size). The combination of low



critical charge and carrier collection from relatively deep in the high resistivity substrate leads to high SEU susceptibility. It is interesting to note that the static RAM and microprocessor also have low critical charge characteristics but much low single bit error cross sections. I have assumed that the single bit error cross section times the particle fluence is the probability of a single bit upset. Clearly this would be valid for products significantly less than unity. It is possible that part of the low reported SEV for the microprocessor may be due to the difficulty in observing the worst-case upset.

#### 4.2.3.4 I<sup>2</sup>L

The observed SEU susceptibility is relatively low but higher than that expected from relative bulk ionizing-induced upset. As with CMOS/SOS, compensating effects present under bulk ionization but absent under localized ionization may contribute to the observed effect.

#### 4.2.3.4.5 SC/TTL

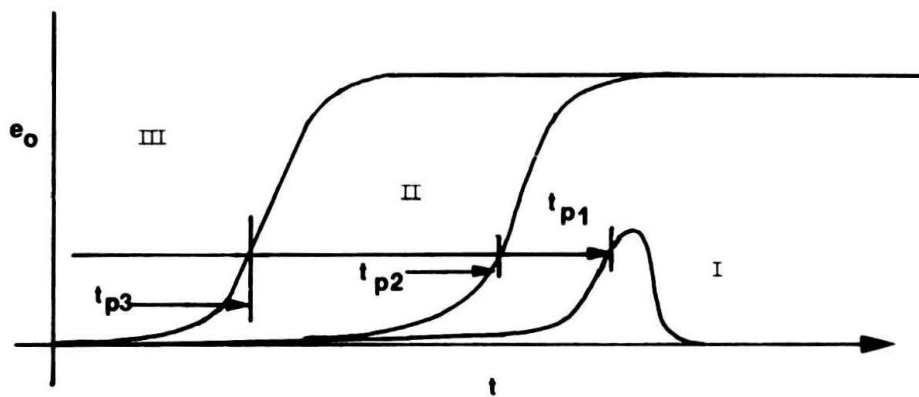
Schottky-clamped TTL as a relatively high power, large-scale technology is relatively insensitive to soft errors. Bipolar TTL memories seem to represent the worst-case susceptibility and data suggest that decreases in microcircuit geometry to increase yield (i.e., shrinking) increases the SEU susceptibility.

### 5. SHORT-TERM ANNEALING EFFECTS

Radiation effects that are generally considered to be important in long-term performance degradation in microcircuits have time-dependence that may be important in system application. Pulsed neutron exposure results in an important decrease in the minority carrier lifetime in the

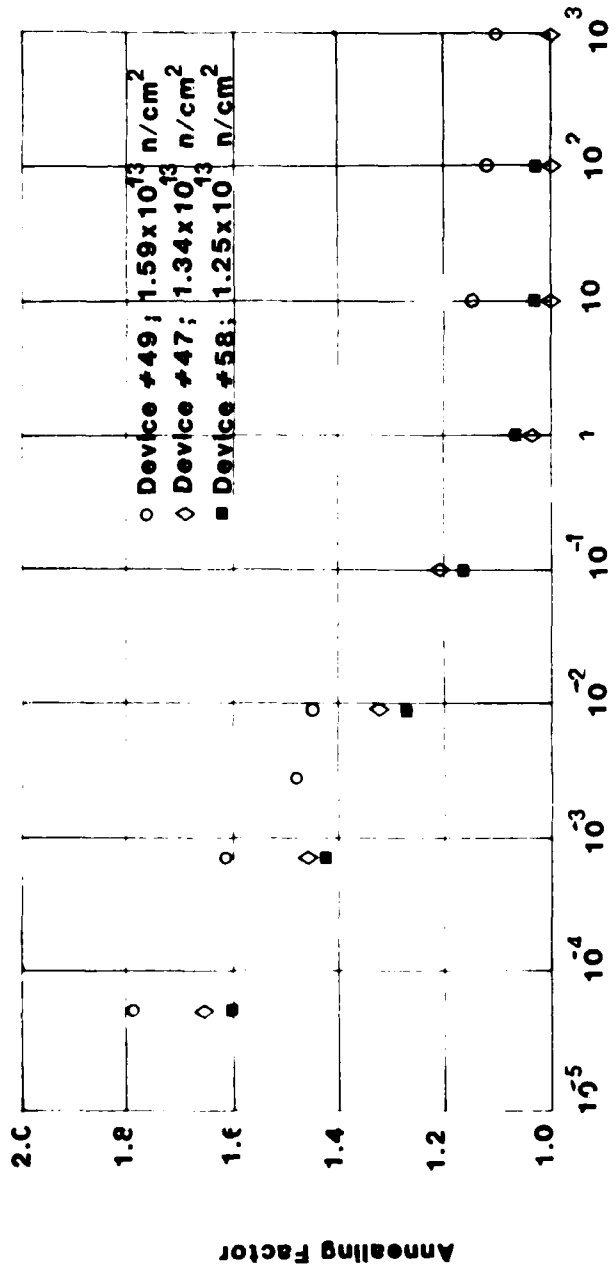
bulk semiconductor which permanently degrades the bipolar transistor current gain. At short times (i.e., microseconds-milliseconds) following exposure, the displacement damage and minority carrier lifetime degradation is substantially greater than the stable damage and device degradation. This effect, called short-term annealing, has been extensively studied in terms of effects in bulk semiconductor material, solar cells and transistors as a function of time following radiation exposure, neutron energy spectrum of the radiation pulse, and device current bias levels. In a very gross summary, the relative short-term annealing effect on the gain of a transistor is a factor on the order of two for a transistor operated at moderate bias currents and at times on the order of 1 millisecond following pulsed 1 MeV (equivalent) neutron exposure. The magnitude of the effect increases with decreasing time from radiation exposure, increasing neutron energy spectrum, and with decreasing bias currents in the transistor.

In this discussion, however, the concern is for the nature of these transient radiation effects in complex microcircuits. Gregory and Sander showed that the nature of transistor short-term annealing in a digital microcircuit appears as a transient increase in the microcircuit propagation delay shown in Figure 43.<sup>79</sup> Because short-term annealing effects are most severe at low transistor bias currents, additional charge must be delivered to a switching transistor to turn it on following pulsed neutron exposure. When the transistor has been turned on at least once, however, the excess charge required is reduced, and the transient increase in turn-on delay is decreased. The point, in this case, is that if short-term annealing effects in microcircuit arrays are potentially important in system application, the critical parameter is probably the electrical propagation delay through the logic gates immediately following radiation exposure. This is further illustrated in the short-term annealing effects measured on I<sup>2</sup>L ring counters as shown in Figure 44.<sup>80</sup> In this case the frequency of the ring counters is inversely proportional to



I: First switching response following exposure  
 II: Second  
 III: Third

**FIGURE 43. TTL Gate Short-Term Annealing.  
 (Artistic Illustration Based On  
 Data Of Sander And Gregory)<sup>69</sup>**



Time Following Peak Of Neutron Burst In Seconds

FIGURE 44.  $I^2$  L RING OSCILLATOR ANNEALING FACTOR (ref. 34)

gate propagation delay. In the I<sup>2</sup>L gates the charging currents are closely related to the elemental transistor gains and the gate propagation delay. The worst-case magnitude of short-term annealing effects on propagation delay in this characterization appear to be on the order of a factor of two.

Short-term annealing effects have also been observed on the ionization-induced threshold voltage shifts in MOS transistors.<sup>81,82</sup> The magnitude and time constants of the effect appear to be strongly dependent on fabrication processes and relative effects between trapped gate and interface charge. In p-MOS transistors the threshold voltage shift seems to depend on the trapped charge in the oxide and the time constants of charge transport and process-dependent trapping in the oxide. In n-MOS transistors, however, there also are important effects on threshold voltage shift which depend on the time-dependent formation (or annealing) or interface states. Short-term annealing effects have been observed on MOS microcircuits, generally in the recovery of array operation some time after pulsed ionization exposure.<sup>83,84</sup>

The nature and magnitude of annealing effects in complex microcircuits have not yet been related to observed effects in basic transistor elements. I would like to point out, even at this time, that the critical parameters in the complex microcircuits will only be indirectly related to the transistor threshold voltage shifts. Critical parameters of the complex arrays could include transient increase in signal propagation delays and a transient increase in power supply current. Effects could be particularly complex in CMOS arrays where the variation in threshold voltage shifts of the p-MOS and n-MOS transistors have different electrical effects. For example, the transient increase in the p-MOS threshold voltage will increase the gate propagation delay, the decrease in n-MOS threshold voltage due to oxide charge may cause a transient increase in power supply current, and the increase in n-MOS threshold voltage due to radiation-induced interface states will tend to increase gate propagation delays.

6. CLOSING REMARKS

The principal goal in this presentation has been to establish a good understanding between cause and effect in the transient effects in complex microcircuits. Results of extensive studies on transient effects in LSI/VLSI arrays on a wide variety of technologies have not been included in this review but are in the literature. I hope that this review will help you interpret the data in the literature as well as that to be presented in this Conference.

I wish to express my gratitude to the continuing support of the technical community by the Defense Nuclear Agency and the DoD lead Laboratories for Radiation Effects (Air Force Weapons Laboratory, Harry Diamond Laboratories and Naval Research Laboratory). Results presented here represent only a small fraction of the valuable work resulting from their support, insight and direction.

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