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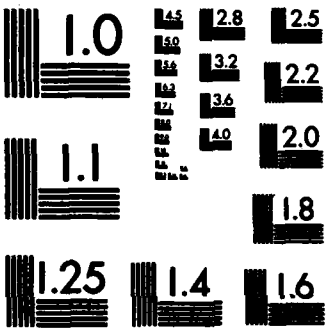

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TESTABILITY OF INTERCONNECTION STRUCTURES

FINAL REPORT

Gerard G. L. Meyer

Report JHU/EECS-83/18

ENGINEERING AND COMPUTER SCIENCE

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ABSTRACT

The goal of ~~the~~ this research effort supported by the Office of Naval Research under Contract N00014-80-C-0772 was to analyze the relationships between system structure and testability. This final report describes the approach that was followed to relate structure and testability and presents the results that were obtained.

INTRODUCTION

The complexity of current electronic systems usually requires these systems to be partitioned into a number of more manageable subsystems before the design process may proceed. As this approach is applied to the design of each subsystem, the resulting design becomes hierarchical in nature. Each design level consists of interconnecting subsystems from a lower design level and it is clear that under these constraints the design problem is basically an interconnection problem.

Systems must be designed not only to meet desired functional requirements but also to be reliable and easily maintainable . It is therefore imperative to provide efficient procedures which allow the user to (1) ascertain that the system is performing properly prior to use; (2) ascertain that the system is performing properly during use; and (3) detect, locate, and repair the cause of failures when they do occur. These procedures are particularly important if the system is to have fault tolerant capabilities since the system must react in the proper manner to the occurrence of faults. Unfortunately the existence of such procedures is by no means ensured, and even when they exist, the task of finding them may be prohibitively complicated.

Since the design problem is basically an interconnection problem and the need for inherent testability is essential, it follows that the interconnection structure must take into account testability constraints. This is true whether we consider the functional interconnection links of the system or an additional interconnection structure

whose only function is the testing of the system. In either case the designer must take into account not only the design requirements of the system, but at the same time he must provide for fault detection and fault location capability. Thus the analysis of the testability of interconnection structures is motivated by the desire to facilitate the design of easily testable and maintainable complex systems.

Most testing approaches require intimate knowledge of system operation and thus require the application of specialized stimuli and measurement of unique responses. Such methods leave few areas which may be generalized and applied to other systems and few areas in which the analysis of the system may be simplified. In attempt to generalize testing problems, some approaches have ignored the analysis of the system functions completely. These methods require systems to be available, which are believed to be fault free and their experimental response to noise or pseudo-random stimuli is recorded for comparison to other systems. Though simple to apply, the usefulness of this approach is difficult to evaluate since the stimuli and responses may have little in common with the system's normal functions.

It is generally true that subsystems are more easily (or at least less expensively) tested when isolated rather than embedded into a system. It is therefore the interconnection structure which complicates the problem by limiting access to and creating interdependencies between subsystems. The test approaches described, however, do not address the fact that if the subsystems are testable when isolated, it is the process of embedding them into a larger system which has complicated the

testing procedures. Clearly if the larger system provided the same access to the subsystems which is provided when the subsystems were isolated the testing process would be no more complicated that testing each individual subsystem. This never occurs and in fact it is agreed that the foremost difficultly related to testing complex systems is that the interconnection structure of the system often renders the individual subsystems virtually untestable. This is as true of complex integrated circuits as it is of complete radar systems.

In both the testing approaches described, the interconnected subsystems are treated as a new system and the task of testing them as essentially a new problem. Assume, however, that it is possible to determine testability properties of the interconnection structure independently from the subsystems themselves. Then using these properties and the knowledge that the subsystems are testable, it may be possible to develop tests for the entire system with only limited knowledge of the system's overall function. Thus in-depth analysis of the system has been avoided without approaching the task of test generation in a haphazard manner. Indeed, if this approach is taken to a logical conclusion, the testability of only the most basic circuit components must be analyzed in detail since more complex systems may analyzed in terms of their interconnections between testable subsystems.

Thus it is clear that not only is it beneficial to identify interconnection structures with good and bad testability properties, but it is also advantageous to develop analysis methods for the testability of general interconnection structures. These must necessarily include

methods for the analysis of (1) a structure's theoretical ability to detect faults; (2) a structure's theoretical ability to diagnose (isolate) faults; and (3) the existence of efficient algorithms for fault diagnosis.

It is particularly important to note that the diagnosis efficiency of a system is strongly related to its structure and could be an influential factor in determining the system's design. The diagnosis of the fault situation of a system can be viewed as a syndrome decoding problem, that is the location of a fault is obtained by decoding the syndrome resulting from the interaction between the fault and the system structure.

RESEARCH OBJECTIVES

In the area of testability and fault analysis of systems, an abundance of literature and several survey articles are available, however, nearly all of this information deals only with isolated testing of specialized subsystems. Relatively few authors (see Appendix II) have chosen to approach the problem of fault analysis at the system level and in terms of the interconnection structure. Furthermore, those existing studies have often relied on assumptions which are not met by real systems. These assumptions have included: (1) the necessity for independent test interfaces; (2) the requirement that all units of the system be capable of evaluating and testing any other unit; (3) the assumption that the interconnection links are fault-free; and (4) the requirement that the units are strictly logical (digital) in nature. We now discuss briefly these assumptions and their impact on system design.

The need for additional interfaces for testing contributes to the system's complexity by the addition of extraneous components whose only purpose are fault detection and location. Although appealing, this approach suffers several serious drawbacks: (1) the additional devices themselves are sources of possible failures; (2) faulty testing devices may result in incorrect diagnosis of subsystems; and (3) the interconnection links used during normal system operation may not be tested. Note that removing or isolating a subsystem for testing not only does not verify its communication links, but if a failure is due to faulty contact between the unit and the network, removing the unit may actually remove the cause of the failure.

The requirement that any subsystem is capable of testing any other subsystem is usually not met in real systems. For example, a radar system is comprised of subsystems whose nature and capabilities are widely varied. This dissimilarity in function limits the ability of certain modules to evaluate others. From a testability standpoint this is also a limitation on the interconnection structure. So although we leave the task of determining and generating the proper testing stimuli to the manufacturers of these subsystems, it is clear that we must address ourselves to the problem of testing various dissimilar modules when they are interconnected to form a system.

A diagnosis approach which does not consider interconnection link failure leads to the incorrect diagnosis of single or multiple subsystem failures in the event of an actual link failure. This results in the unnecessary removal and attempted repair of nonfaulty subsystems. Thus it is important to distinguish between link and subsystem failure. The ability to detect and isolate a faulty link is even more critical if the system has the capability of preserving its operation by rerouting or ignoring signals normally transmitted through that link.

Finally, the rapid advances in digital technology has led many researchers to simplify their analyses by considering only logical subsystem types. As a result, most of the fault diagnosis schemes developed up to this time are digital in nature and few are directly applicable to hybrid systems, i.e. systems which consist of both analog and digital components. The improvements now occurring in analog integrated circuit technology have renewed interest in analog fault

detection and location. Thus hybrid or specifically analog interconnection structures which have known good detection and fault diagnosis properties are needed.

Thus, the major task to which we have addressed ourselves is the following: assuming that the subsystems are testable, that is, we know how to check them when isolated, we must find ways to ensure that we may still evaluate the correctness of their operation when they are embedded into the system. Our criteria for fault detection emphasizes the overall functional operation of the system. This is done deliberately in an attempt to reduce the dependency of our testability models upon the individual parametric test requirements of isolated subsystems. Thus we have concerned ourselves with a system's overall functional requirements, but have avoided discussion of specific stimuli generation and response measurement problems.

RESEARCH RESULTS

The first and foremost objective of our research effort was to synthesize a class of testability models powerful enough to be applicable to a wide range of real systems and possessing enough structure to allow for a detailed analysis of their detectability and diagnosability properties. Our work has lead to the synthesis of a system level fault model, the HM fault model, that possesses the desired properties. In particular, the flexibility of the model allows the concept of morphism to be used, even in situations in which the morphic properties are not initially present. That work has resulted in a Ph. D. Dissertation [8] and several papers [2], [3], [5] and [6].

The second objective of our research effort was to develop decoding algorithms for the analysis of the syndromes produced by the interaction between allowable classes of faults and the models previously defined. These algorithms are necessary to insure the efficient location of the faulty subsystems and thus to facilitate their timely repair. Our work on the PMC model [PRE67] and the BGM model [BAR76] has lead us to recognize that a maximality property of the implied faulty sets in the case of the PMC model [7] [12], to propose a decoding algorithm for the BGM model [10] [11], and to analyze iterative techniques for decoding based on partial syndromes [4].

The third objective of our research effort was to relate the efficiency of the decoding algorithms to the complexity of the interconnection structures of the models. Our approach to that problem was to use

the HM model to introduce a partial ordering on the family of system-level fault models. The results are contained in [9] and show that a systematic classification of models is possible and that this classification can be used to synthesize decoding algorithms.

Finally, we have analyzed [1] a class of transmission models proposed by Sogomonyan [SOG64] and we have shown that such models may be viewed as particular case of the HM model [8].

In meeting our research objectives we have accomplished our goal to provide a simplified and efficient approach to the design of testable complex systems. By basing our testability measures on the system's interconnection structure, we have emphasized the testability of subsystems as they are actually used, i.e. embedded in a larger system.

APPENDIX I: PUBLISHED WORK

[1] Meyer, G. G. L., Transmission Model for Hybrid Fault Diagnosis, Workshop on Analog Fault Diagnosis, University of Notre Dame, South Bend, Indiana, May 26-27, 1981.

[2] Havlicsek, B. L. and Meyer, G. G. L., Morphic Properties of Deterministic and Nondeterministic Fault Models, Proc. Nineteenth Annual Allerton Conference on Communication, Control and Computing, Allerton House, Monticello, Illinois, September 30- October 2, 1981.

[3] Havlicsek, B. L. and Meyer, G. G. L., Totally Morphic HM Fault Model, Proc. 16th Annual Conference on Information Sciences and Systems, Princeton, New Jersey, March 17-19, 1982.

[4] Kennedy, M. A. and Meyer, G. G. L., A Filtering Approach to Transient Fault Diagnosis, Proc. Twentieth Annual Allerton Conference on Communication, Control, and Computing, Allerton House, Monticello, Illinois, October 6-8, 1982.

[5] Havlicsek, B. L. and Meyer, G. G. L., Diagnosability Properties of Weakly Morphic HM Fault Models, Proc. 1982 IEEE International Large Scale Systems Symposium, Virginia Beach, Virginia, October 11-13, 1982.

[6] Havlicsek, B. L. and Meyer, G. G. L., The Development and Application of System-Level Fault Models, Proc. 1983 Automatic Test Program Generation Workshop, San Francisco, California, March 15-16, 1983.

[7] Meyer, G. G. L., The PMC System Level Fault Model: Maximality Properties of the Implied Faulty Sets, Proc. Seventeenth Annual Conference on Information Sciences and Systems, Baltimore, Maryland, March 23-25, 1983.

[8] Havlicsek, B. L., A New System-Level Approach to Diagnosability, Dissertation submitted to The Johns Hopkins University in conformity with the requirements for the degree of Doctor of Philosophy, May 1983.

[9] Havlicsek, B. L. and Meyer, G. G. L., A Partial Ordering for System-Level Fault Models, Proc. Twenty-First Annual Allerton Conference on Communication, Control and Computing, Allerton House, Monticello, Illinois, October 5-7, 1983.

[10] Meyer, G. G. L., A Diagnosis Algorithm for the BGM System-Level Fault Model, Proc. Twenty-First Annual Allerton Conference on Communication, Control and Computing, Allerton House, Monticello, Illinois, October 5-7, 1983.

[11] Meyer, G. G. L., A Diagnosis Algorithm for the BGM System Level Fault Model, IEEE Trans. Computers, Accepted for publication.

[12] Meyer, G. G. L., The PMC System Level Fault Model: Maximality Properties of the Implied Faulty Sets, IEEE Trans. Computers, Submitted May 2, 1983.

APPENDIX II: REFERENCES

[ALL75]Allan, F.J., Kameda, T., and Toida, S., An Approach to the Diagnosability Analysis of a System, IEEE Trans. Computers, Vol. C-24, October 1975, pp. 1040-1042.

[BAR76]Barsi, F., Grandoni, F., and Maestrini, P., A Theory of Diagnosability of Digital Systems, IEEE Trans. Computers, Vol. C-25 , June 1976, pp. 585-593.

[CON74]Conti, R.A., A Method of Fault Isolation for Large Digital Systems, EASCON Conference Proceedings, 1974, pp. 81-85.

[COR76]Corluhan, A.M., and Hakimi, S.L., On an Algorithm for Identifying Faults in a T-Diagnosable System, Proceedings of the 1976 Conference on Information Science and Systems, The Johns Hopkins University, Baltimore, 1976, pp. 370-375.

[FUJ78]Fujiwara, H., and Kinoshita, K., Some Existence Theorems for Probabilistically Diagnosable Systems, IEEE Trans. Computers, Vol. C-27, No. 4, April 1978, pp.379-384.

[HAK74]Hakimi, S.L., and Amin, A.T., Characterization of Connection Assignment of Diagnosable Systems, IEEE Trans. Computers, Vol. C-23 , January 1974, pp. 86-88.

[HOL81]Holt, C.S. and Smith, J.E., Diagnosis of Systems with Asymmetric Invalidation, IEEE Trans. Computers, Vol. C-30, No. 9, September 1981, pp. 679-690.

[KAM75]Kameda, T., Toida, S., and Allan, F.J., A Diagnosing Algorithm for Networks, Information and Control, Vol. 29 (1975), pp. 141-148.

[KIM70]Kime, C.R., An Analysis Model for Digital System Diagnosis, IEEE Trans. Computers, Vol. C-19, No. 11, November 1970, pp. 1063-1073.

[KIM79]Kime, C.R., An Abstract Model for Digital System Fault Diagnosis, IEEE Trans. Computers, Vol. C-28, No. 10, October 1979, pp. 754-767.

[MAH76]Maheshwari, S.N., and Hakimi, S.L., On Models for Diagnosable Systems and Probabilistic Fault Diagnosis, IEEE Trans. Computers, Vol. C-25 , March 1976, pp.228-236.

[MAL78]Mallela, S., and Masson G.M., Diagnosable Systems for Intermittent Faults, IEEE Trans. Computers, Vol. C-27, No. 6, June 1978, pp. 560-566.

[MEY76]Meyer, G.G.L., and Masson G.M., An Efficient Fault Diagnosis Algorithm for Multiple Processor Architectures, Proceedings of the 1976 Conference on Information Sciences and Systems, The Johns Hopkins University, Baltimore, Maryland, pp.249-251.

[MEY77]Meyer, G.G.L., Fault Diagnosis of Modular Networks with a Small Number of Faults, Proceedings of the Fifteenth Annual Allerton Conference on Communication, Control, and Computing, Allerton House, Monticello, Illinois, September 1977, pp.727-731.

[MEY78]Meyer, G.G.L., and Masson, G.M., An Efficient Fault Diagnosis Algorithm for Symmetric Multiple Processor Architectures, IEEE Trans. Computers, Vol. C-27, No. 11, November 1978, pp. 1059-1063.

[PRE67]Preparata, F.P., Metze, G., and Chien, R.T., On the Connection Assignment Problem of Diagnosable Systems, IEEE Trans. Electronic Computers, Vol. EC-16 , December 1967, pp.848-854.

[RUS75a]Russell, J.D., and Kime, C.R., System Fault Diagnosis: Closure and Diagnosability with Repair, IEEE Trans. Computers, Vol. C-24 , November 1975, pp. 1078-1089.

[RUS75b]Russell, J.D., and Kime, C.R., System Fault Diagnosis: Masking, Exposure, and Diagnosability without Repair, IEEE Trans. Computers, Vol. C-24, No. 12, December 1975, pp. 1155-1161.

[SMI79]Smith, J.E., Universal System Diagnosis Algorithms, IEEE Trans. Computers, Vol. C-28, No. 5, May 1979, pp. 374-378.

[SOG64]Sogomonyan, E.S., Monitoring Operability and Finding Failures in Functionally Connected Systems, Automatic and Remote Control, Vol. 25, No. 6, June 1964, pp. 874-882.

[TOI82]Toida, S., A Graph Model for Fault Diagnosis, J. Digital Systems, Vol. VI, No. 4, Winter 1982, pp. 345-365.

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The goal of the research effort supported by the Office of Naval Research under Contract N00014-80-C-0772 was to analyze the relationships between system structure and testability. This final report describes the approach that was followed to relate structure and testability and presents the results that were obtained.

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