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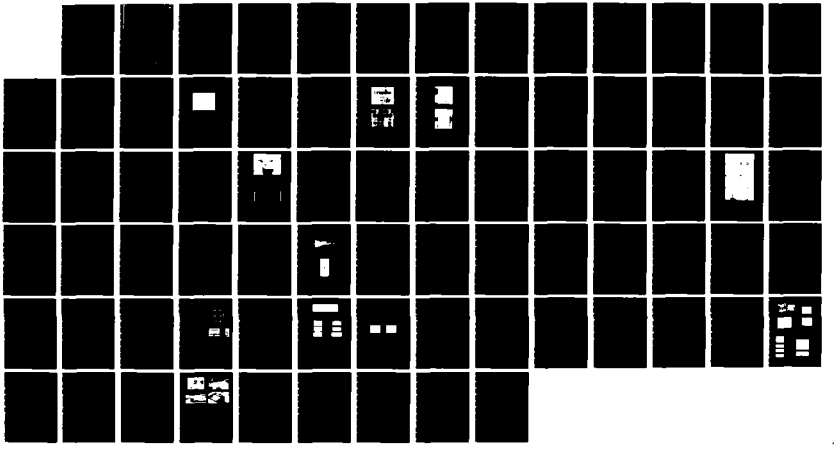

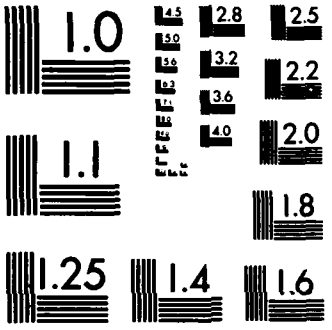

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GaAs FET LOGIC AT LOW TEMPERATURES

Texas Instruments Incorporated
Central Research Laboratories
13500 North Central Laboratories
Dallas, Texas 75265

27 July 1983

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Prepared for
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Ring oscillator circuits were fabricated on both VPE and ion-implanted active layers encompassing the 4×10^{16} to 1×10^{17} cm^{-3} doping range. The nominal pinch-off voltage was -2.5 V. Using an especially constructed experimental arrangement, the circuits were then characterized on-slice at 77 and 300 K, while test devices were characterized over the 77 to 430 K temperature range.

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Characterization of test devices included doping profile, Schottky barrier height, mobility, and FET measurements as well as DLTS measurements. The results show that the effect of temperature on $\int ndx$, ϕ_B, μ, and the saturation velocity are relatively small over a broad temperature range. These small effects act in concert to affect device currents by about -0.2% per °C. Based on our understanding of logic cell operation, the circuit speed would also be expected to have a temperature coefficient of -0.2% per °C. This expectation is close to the experimentally measured value.

For 10^{17} cm^{-3} doped layers, the speed ratio at 77 K compared to that at 300 K is 1.50 for both VPE and implanted layers. Since circuit current ratios are also about 1.5, the t_{pd} P_d product at 77 K is nearly the same as that obtained at 300 K. For 4×10^{16} cm^{-3} doped layers, the speed ratio improves to 1.68. However, since device currents are reduced with decreasing doping concentration, the circuit speeds at 300 K on 4×10^{16} cm^{-3} layers are only 70% of that obtained on 10^{17} cm^{-3} layers. This result indicates that the more highly doped layers are more suitable for cold temperature operation.

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SECTION I
INTRODUCTION

This report covers progress made on Contract No. N00014-79-C-0789, a three year research program, to investigate the speed advantage associated with the operation of GaAs integrated circuits at low temperatures (77 K). The work was carried out in conjunction with a TI internally-funded program to develop a viable, room-temperature, high-speed GaAs logic technology. In addition, an Air Force program, Contract No. F33615-80-C-1171, to develop and demonstrate a planar GaAs processing technology, has contributed significantly to the present program.

In Section II, material development is discussed. Process development and circuit development are discussed in Sections III and IV, respectively. The principal results of this investigation, the temperature characteristics of GaAs MESFET devices and circuits, are described in Section V.

SECTION II
MATERIAL DEVELOPMENT

A. Vapor Phase Epitaxy

A large number of GaAs epitaxial structures have been grown by vapor phase epitaxy on both Cr-doped and not intentionally doped LEC semi-insulating substrates during the course of this program. Epitaxial growth was done in a previously described reactor system.[1] The doping concentration of the active layer encompassed the low 10^{15} cm^{-3} to the low 10^{17} cm^{-3} range. The active layers were grown on buffer layers having a typical thickness of approximately 3 μm. The surface morphology of the epitaxial layers was very good. Van der Pauw mobility measurements on some slices were made at 300 K and 77 K (see Figure 1). In general, the measured mobilities are comparable to those reported in the literature. Mobility ratios [R_μ = μ(77 K)/ μ(300 K)] between 3 and 4.5 were obtained for mid-10^{15} cm^{-3} doped active layers. This ratio decreases as the doping of the active layer increases. Mobility measurements using a fat-FET structure were also correlated to van der Pauw mobilities at both 300 K and 77 K. The two methods of measuring mobility agreed to within ±15%.

The active layers were purposely grown thicker than required. Without anodic thinning, material uniformity was not adequate for circuit processing. Consequently, anodic thinning was employed to improve uniformity to an acceptable level. This procedure was also applied to ~ 10^{16} cm^{-3} VPE layers with success. Using preliminary CV material characterization data, the slice was then uniformly etched to a thickness slightly greater than that appropriate for a pinch-off of -2.5 V. The desired pinch-off was subsequently achieved by a gate recess etch step.

B. Deep Level Transient Spectroscopy (DLTS) Measurements

The work described in this subsection was performed primarily under AFWAL Contract No. F33615-80-C-1171 (Planar High Speed GaAs Technology). It is included in this report because it shows that the trap concentration of epitaxial and implanted active layers is similar.

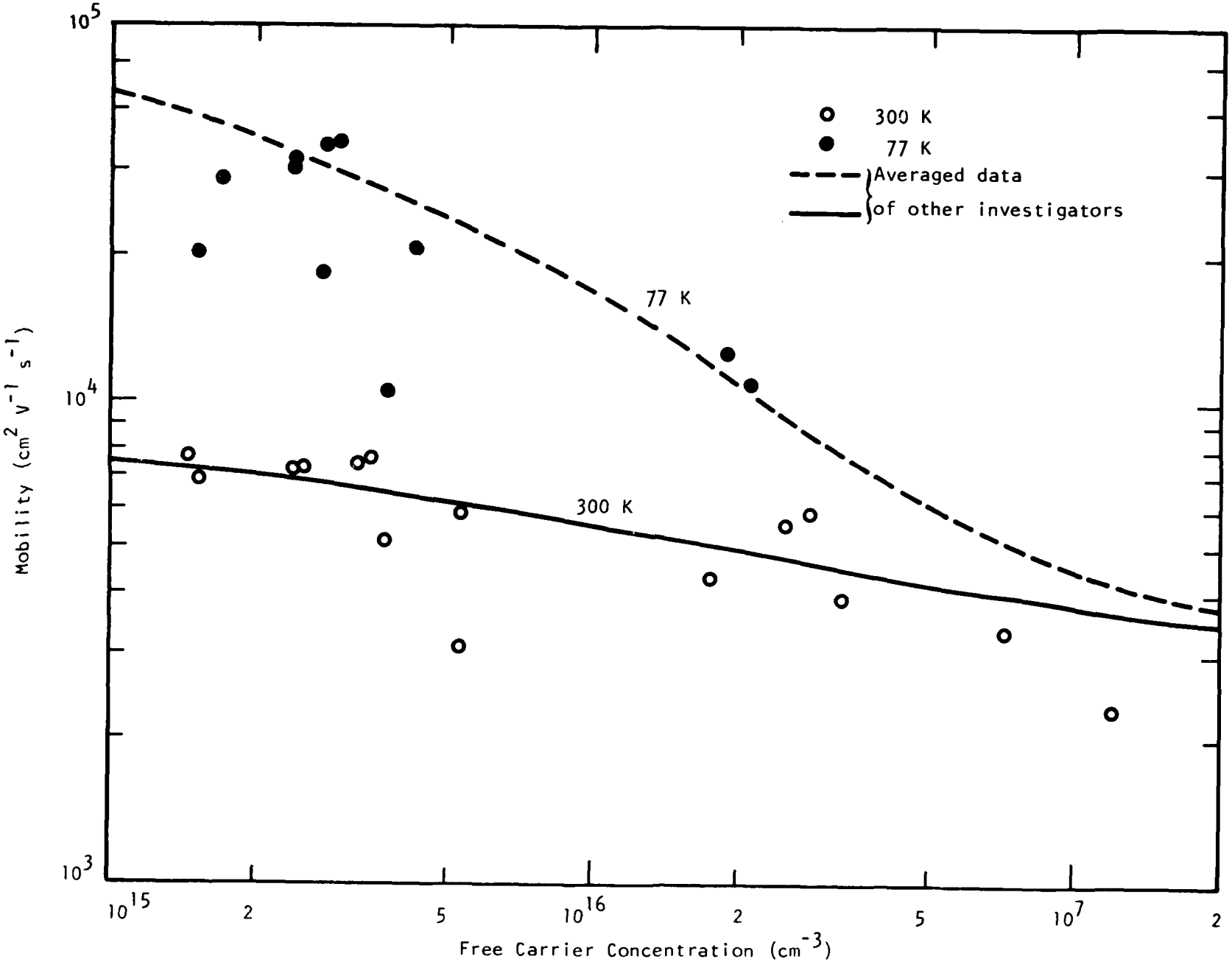


Figure 1 Van der Pauw Mobility Measurements of Vapor Phase Epitaxial Structures

Measurements by DLTS were used to compare the dominant deep traps in conductive layers prepared by direct implantation into GaAs substrates using standard Si implant/proximity anneal conditions. All epitaxial FET structures were also examined for comparison. Commercially available H-LEC (Metals Research) and TI-grown LP-LEC materials, as well as commercially available Cr-doped Bridgman material (Morgan Semiconductor), had been investigated as substrates for ion implantation (see also Appendix A). The results for TiPtAu Schottky contacts on implanted and epitaxial material are presented in Table 1. Several diodes on each material type were examined to ensure the reproducibility of these results.

In the commercial LEC material (shown in the table as Sample No. 1), a relatively high trap density (2×10^{15} cm^{-3}) is found at 0.79 eV below the conduction band (CB). This trap has not been definitively assigned, but is generally associated in the literature with oxygen or a native defect in GaAs. By comparison, the LP-LEC (Sample No. 2 in the table) shows a much lower trap density (3×10^{13} cm^{-3}) at 0.57 eV below the CB. This trap corresponds to Fe as an acceptor. Iron in the B_2O_3 encapsulant used in the bulk growth process (as determined by Spark Source Mass Spectroscopy) is suspected of being the source of the Fe impurity.

The results for two directly implanted Cr-doped Bridgman samples taken from the seed end (Sample No. 3) and tail end (Sample No. 4) of the same ingot are also shown in the table. For the seed end specimen, a single trap at E_C -0.84 eV is found, corresponding to the Cr acceptor with a concentration of 1.25×10^{14} cm^{-3}. It is notable that in the tail end, three traps are observed. Of these traps, the deepest (E_C -1.62 eV) dominates the spectrum, obscuring the energies of the other two traps. Furthermore, this very deep trap has an activation energy that is greater than the band gap at room temperature (1.43 eV). The large energy of this center may be due to the trap coupling to one of the indirect CB minima (X or L) above the direct gap minimum (Γ).

Table 1

DLTS Data for Ion Implanted and VPE Conductive Layers

Sample No.	Identification	Energy Level (eV)	Trap Concentration N_T (cm^{-3})	Capture Cross Section σ_n (cm^2)
1	H-LEC Undoped, Metals Research	E_c - 0.791	2.04×10^{15}	$1.05 \times 10^{-}$
2	LP-LEC Undoped, Texas Instruments	E_c - 0.586	3.05×10^{13}	$2.25 \times 10^{-}$
3	Bridgman Cr-doped, Morgan 5-53, Seed end	E_c - 0.842	1.25×10^{14}	3.1×10^{-21}
4	Bridgman Cr-doped, Morgan 5-53, Tail end	E_c - 0.45	*	*
		E_c - 0.79	*	*
		E_c - 1.622	2.54×10^{12}	1.31×10^{-21} (468 K) 0.98×10^{-21} (476 K) 0.79×10^{-21} (490 K) 0.61×10^{-21} (508 K)
5	VPE, Texas Instruments	E_c - 0.866	‡	‡
		E_c - 1.266	‡	‡

* Data not sufficiently pronounced to extract result

‡ To be determined

Finally, the DLTS results for an all-epitaxial FET structure (with ~ 10^{14} cm^{-3} undoped buffer layer between the sulfur doped 1 x 10^{17} cm^{-3} channel and the substrate), as grown by the $AsCl_3/Ga/H_2$ process, are presented in the table (Sample No. 5). This sample also exhibits a very deep center with an energy (E_C -1.266 eV) near that of the room temperature band gap. A second center at E_C -0.866 eV is also observed in this structure. This energy corresponds to the deep Cr center in GaAs. Presumably, Cr from the Cr-doped substrate is outdiffusing into the epitaxial layer during the growth process. The outdiffusion of Cr from substrates into the epitaxial layers at process temperatures is well documented in the literature.[2]

In summary, in all the material studied, the trap energies are deep enough not to appreciably change occupancy (i. e., their degree of ionization according to a Boltzmann distribution) for temperature changes decreasing from 300 K. On the other hand, for temperatures > 300 K, device properties are not expected to be significantly affected because trap concentration densities are small compared to the free electron concentration density.

SECTION III
PROCESS DEVELOPMENT

The present standard process consists of device isolation, nitride patterning for e-beam alignment marks, ohmic contact formation, first Schottky metal, gate delineation, first level metal, interlevel dielectric patterning, and second level metal. Each step involves an average of about 20 separate operations. Much of this development work was done under both an internally funded program and the Planar High Speed GaAs Technology Program sponsored by the Avionics Laboratory (AFWAL) under Contract No. F33615-80-C-1171.

A. Fabrication Sequence

The process usually starts with a sheet implanted or a VPE grown active layer. The layers are produced on 0.5 mm thick substrates to reduce breakage during processing. The substrate is then shaped by scribing along specific crystallographic orientations for subsequent alignment to the e-beam slice holder. Figure 2 summarizes the remainder of the process.

1. B^+ Isolation Implant (LE10)

About one year after the start of the program, we converted to the B^+ isolation implant technique. Although the previously used mesa isolation technique was highly reproducible, it had a minor drawback. The nonuniformity of the e-beam resist thickness at the mesa edge resulted in a tighter exposure window for 0.5 μm gate lengths. The B^+ isolation implant mask uses a negative resist over 200 nm nitride. This combination is patterned and a 30 nm etch of the GaAs surface is used for subsequent alignment. A B^+ implant dose of 10^{13} cm^{-2} at 120 keV is typically employed. The minimum distance between adjacent active regions is 3 μm.

2. Nitride Pads for e-Beam Alignment Masks (LE15)

This step involves delineation of relatively large geometries. A 200 nm nitride layer is patterned to separate the e-beam alignment marks from the GaAs, thereby helping to preserve their integrity. This step is not shown in Figure 2.

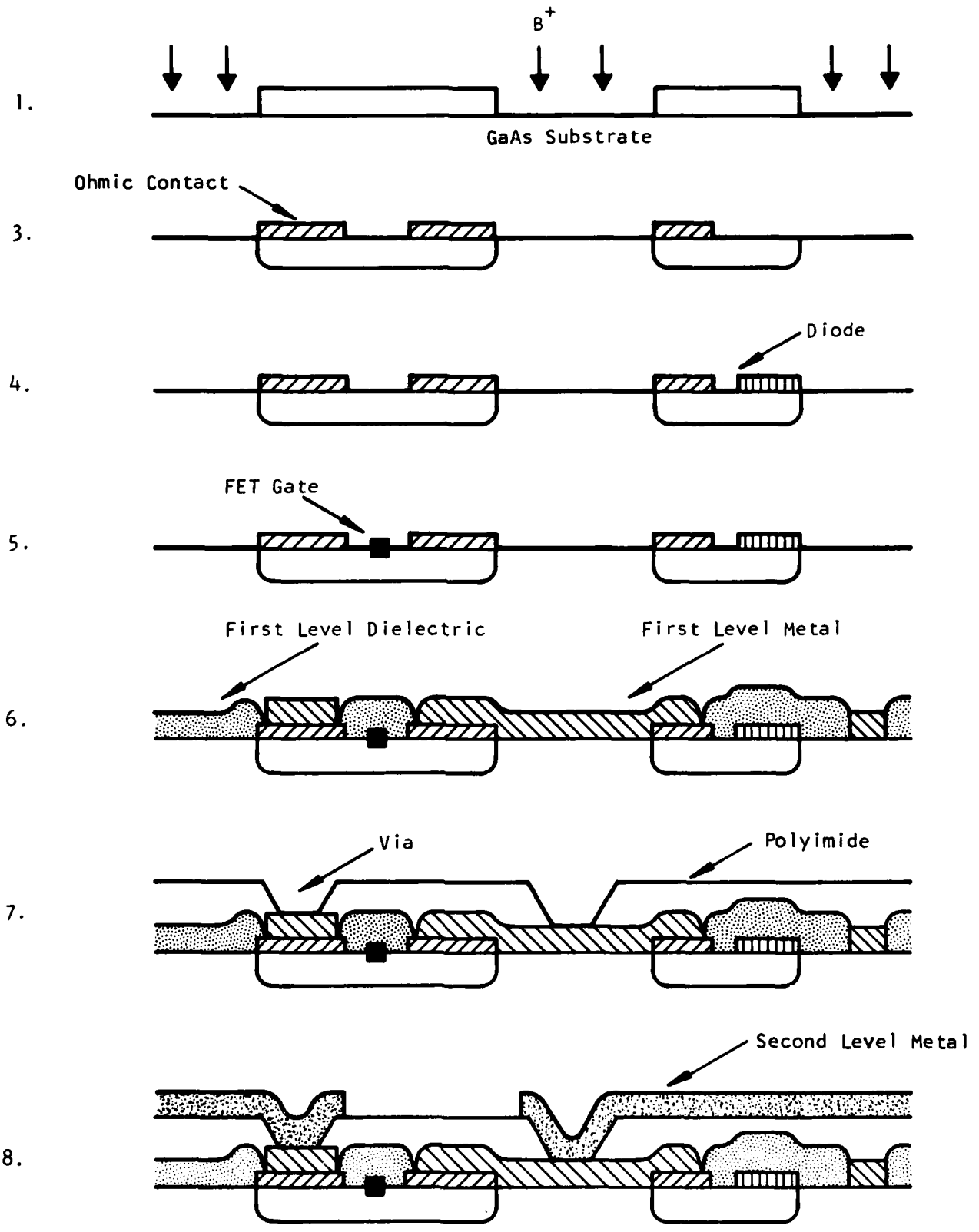


Figure 2 Fabrication Process Used at Texas Instruments

3. Ohmic Contacts (LE20)

The requirements for ohmic contacts are replication of small, closely spaced features; low contact resistance; contact uniformity; reproducibility; high quality alignment marks; edge acuity; and adequate surface morphology. Although initially we experienced considerable difficulty with this process step, the current standard process adequately satisfies all these requirements. Figure 3 shows an ohmic contact test pattern and the subsequent gate level alignment to it. Such results are typical of the process which employs a Ni/AuGe/Ni metallization and a subsequent ~ 430°C alloying temperature cycle. No contact failure has occurred since the process has been standardized. It is noteworthy that low contact resistance to mid -10^{15} cm^{-3} doped layers has also been obtained reproducibly.

The metallization consists of 10 nm Ni/~ 100 nm AuGe/~ 18 nm Ni and is patterned by lift-off. Alloying for 3 minutes in a He atmosphere at 430°C completes this step. Contact resistance, measured by the transmission line method, is less than 0.3 ohm per mm of contact width. The metallization resistance is ~ 2.7 Ω/square and has a maximum current carrying capability of ~ 10 mA per μm of contact length.

A considerable effort was made to improve the surface morphology of the ohmic contacts. Although such improvement is primarily cosmetic, it would reduce sheet resistance. A variety of noble and refractory metals overlying the standard metallization were tried. One combination exhibited an excellent surface morphology (comparable to that of an unalloyed sample). However, repeated trials for this combination failed to demonstrate a sufficiently high reproducibility.

4. First Schottky Metal (LE29)

The first Schottky metal is applied to the unetched GaAs surface. This step was originally incorporated into the standard process for material characterization. This step helps to determine more precisely the amount of gate recess etching required to obtain the desired pinch-off voltage (and thereby improves slice yield). It is also used at present, to fabricate the

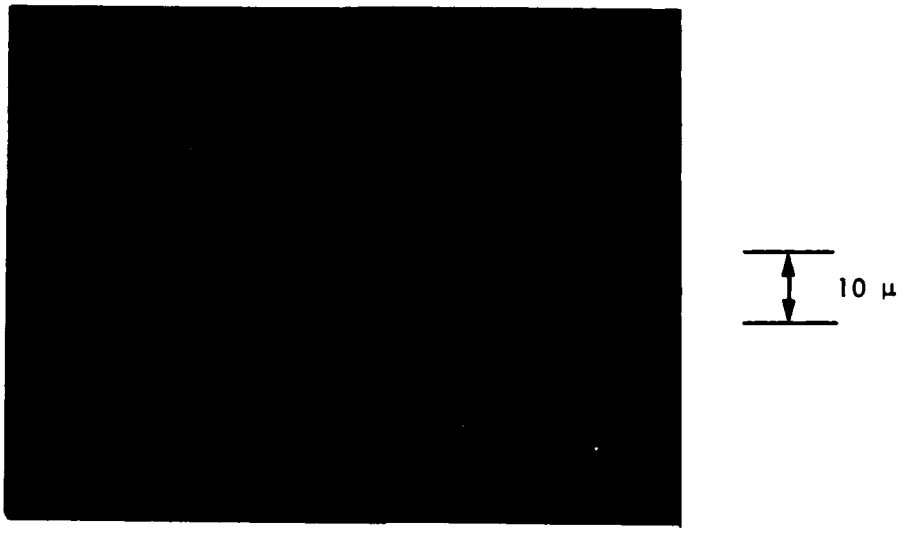


Figure 3 Ohmic/Gate Test Pattern. The duller appearing metal is the ohmic level; the brighter is the gate level. The pattern illustrates the replication of small, closely spaced ohmic features and the subsequent e-beam alignment to them.

Schottky diodes. The metallization, patterned by lift-off, consists of 13 nm Ti/13 nm Pt/125 nm Au. The sheet resistivity is typically about 0.4 Ω/square and the current carrying capability exceeds 15 mA/μm.

5. Gate Delineation (LE30)

The gate metal is applied next, after a recess of 50 to 100 nm. The gate is defined either optically or by e-beam. To minimize e-beam direct slice writing time, only gate stripes and the associated 2 x 2 μm interconnect pad are exposed. This also improves gate recess uniformity because only GaAs is visible to the etchant. The standard gate metal is 25 nm Ti/25 nm Pt/200 nm Au and is defined by lift-off. The sheet resistivity is < 0.2 Ω/square with a current carrying capability of 20 mA/μm.

6. First Level Metal (LE40)

A nitride assisted lift-off is used for the first level metal, the nitride also serves to passivate the GaAs surface of the active devices. This metallization is used to interconnect circuit nodes, provide bond pads, etc. A nitride thickness of ~ 200 nm is used. The metallization used is 25 nm Ti/400 nm Au. Metallization sheet resistivity is 0.1 Ω/square with a current carrying capability of 50 mA/μm.

7. Interlevel Dielectric (LE50)

A 0.7 μm thick polyimide is used in this step. Vias are etched for interconnects to the first level metal. The underlying nitride is used to help determine when the vias are cleaved. The yield of 0.1 mm^2 overlay capacitors (another test pattern) is > 95%, suggesting a pinhole density < 50 cm^{-2}.

8. Second-Level Metal (LE60)

The 25 nm Ti/430 nm Au metallization is patterned by lift-off. The second level metal is used to interconnect circuit nodes and for supply lines. Sheet resistivity is typically 0.09 Ω/square and the current carrying capability is 20 mA/μm of line width.

9. Electrical Characterization During Processing

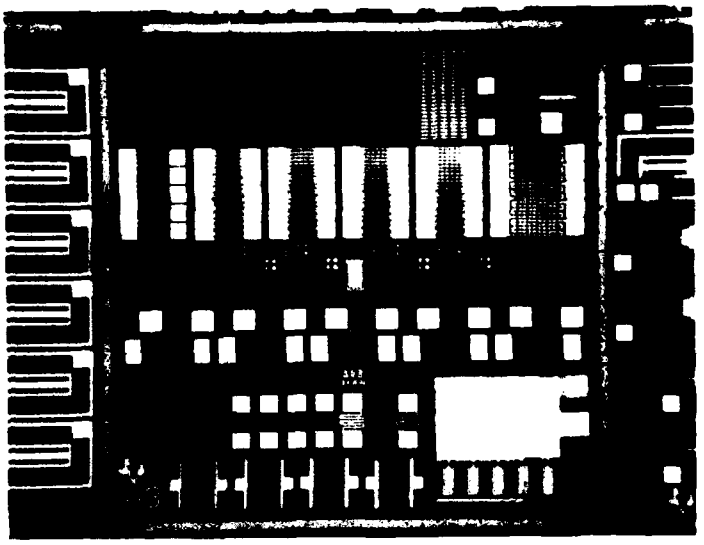
A data base related to processing was accumulated during the course of the program. A summary of the records established typical parameter values. The values are used as standards against which a slice in process is compared.

After the ohmic contacts are applied, data are taken to characterize the contact, the isolation, and the metallization resistance. In addition, data are taken to characterize the long-range, medium-range, and short-range material uniformity. After the first level Schottky metal, measurements include a pinch-off voltage map, a C-V profile map, and diode string characterization. After the first level metal, the FETs are characterized and interconnect patterns evaluated. After the second level metal, the yield of serially interconnected vias are evaluated. These data aid in continually monitoring the process and in screening out deficient material.

B. Design Rules

The minimum design rules presently in use have been established based on reproducibility and yield. They have been determined mainly with the use of test patterns. Figure 4(a) shows the test patterns; all are incorporated into one subfield. Figure 4(b) shows details of some of the structures. At the bottom, meander lines for each level are used to determine sheet resistivity and current carrying capability. Above the meander lines are test patterns of 1, 2, 3, and 4 μm lines and spaces. These are used to evaluate reticle quality. Above these, metal interconnect patterns between different levels are shown. They use 2 x 8 μm bars with a 2 x 2 μm overlap and have yields of ~ 85%. At the top, crossover patterns with yields of nearly 100%, are shown.

Figure 4(c) shows details of one of the via test patterns with nominal via sizes of 4 x 4 μm. Yields are typically ~ 90%. Figure 4(d) shows a large periphery metallization test pattern with 2.5 μm lines and spaces. Yields are typically ~ 90%.



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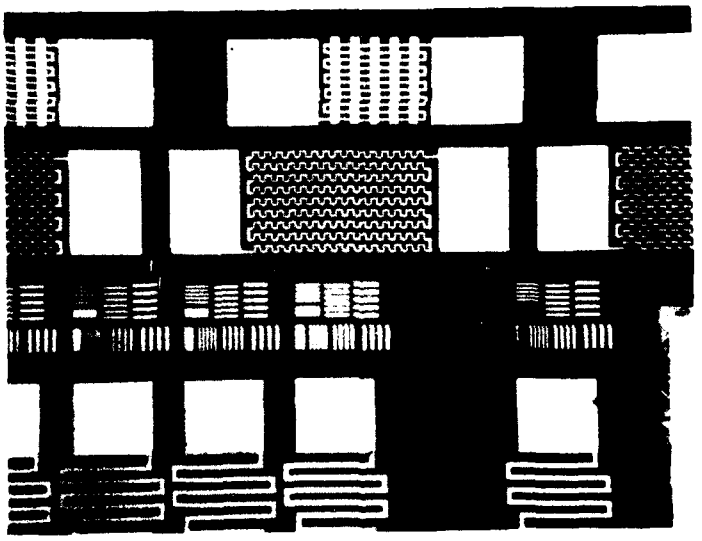
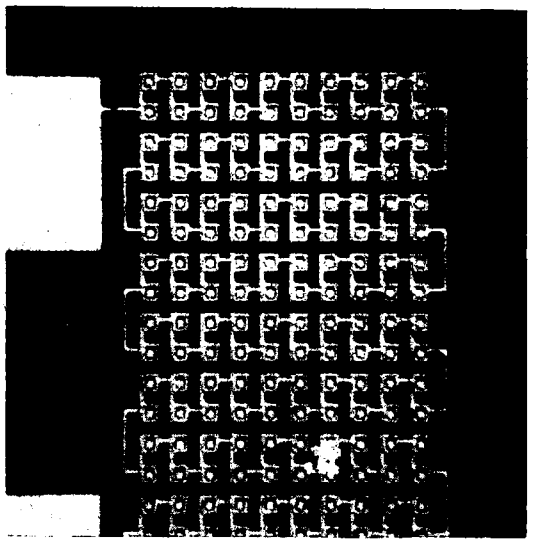


(b)

Figure 4 Test Patterns



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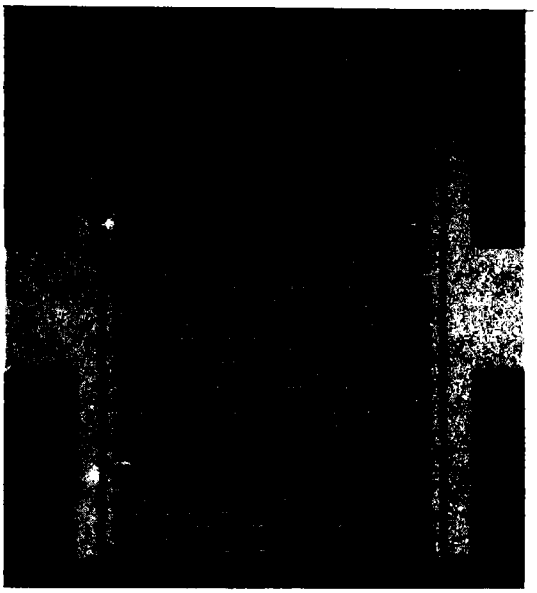
(c)



|←100 μm→|

(d)

Figure 4 (Continued)

Based on such results, the minimum design rules currently in use are:

- Minimum e-beam gate length: 0.75 μm
- Minimum optical gate length: 1.0 μm
- Minimum line width of all other metallizations is 2.0 μm with a minimum spacing to adjacent metal lines of 3 μm.
- Minimum interconnect overlap is 2 x 2 μm (any two levels).
- Minimum via size is 4 x 4 μm.
- Minimum separation between active regions is 3 μm.
- Maximum level-to-level registration error is ± 1 μm.

SECTION IV
CIRCUIT DEVELOPMENT

A. Logic Gates Studied

The first mask set used for this program was mask set C. Its use was for material development, process development, and to study the characteristics of two logic gates. The mask set was therefore generated with the support of funds from three programs: internal IR&D, AFWAC Contract No. F33615-80-C-1171, and the present program.

The two logic gates studied with mask set C used depletion mode FETs with pinch-off voltage, V_p, of -2.5 V. Two embodiments of the buffered FET logic (BFL) gate first introduced by Hewlett-Packard investigators[3] were included. These differed from each other only in the widths of some FET circuit elements. [Henceforth, when reference to the BFL gate is made, it will be understood that we are referring to the embodiment shown by Figure 2(a) of Appendix A.] The second logic gate was an embodiment of the Schottky diode FET logic (SDFL) gate first introduced by Rockwell International investigators[4]. The results of this study have been summarized and reported in the literature. A copy of the paper is contained in Appendix A.

Three other mask sets were used in the present program. The capacitively coupled logic (CCL) gate, proposed by Livingstone and Mellor[5], was studied with the use of mask set D. The feed-forward static (FFS) gate, conceived at Texas Instruments, was investigated with the use of mask set D2. These mask sets were generated primarily under TI internal funding. The final mask set, E1, was generated under AFWAL Contract No. F33615-80-C-1171 funding. This mask set was used to study the characteristics of the enhancement switch/depletion load (E/D) logic gate. A description of the mask sets can be found in Report Number AFWAL-TR-82-1134.

Table 2 summarizes the results of all logic gates studied. The results are for 1 μm gate length and for baseplate temperatures of 300 K. Since data for these gates were taken from different slices having different pinch-off voltages and doping, the data must be normalized to some standard conditions. The normalization was made based on our understanding of the effect of gate width, pinch-off voltage, and doping (see Subsection IV.B). The results shown in Table 2 are normalized for W_s = 20 μm, V_p = -2.5 V, and n = 1 x 10^{17} cm^{-3} for the depletion mode gates. The power dissipation values listed are for optimum supply voltages.

For a fan-out of 3, the results of Table 2 show that the propagation delays of all the gates are comparable. The major difference between the gates is in the power dissipation. The results also show that the E/D gate exhibits the lowest power dissipation by more than an order of magnitude. An additional advantage of the gate is its low component count. However, the cell has a low noise margin, requires tight tolerance on V_p (± 100 mV), and its use restricts the logic design to be NOR configured.

B. Effect of Doping

This subsection discusses the effect of active layer doping on the propagation delay and power dissipation of GaAs MESFET logic gates. At the beginning of the program, it was believed that the optimum doping for low temperature operation would be less than the ~ 10^{17} cm^{-3} doping typically employed for conventional MESFET circuits operating at room temperatures. Experimentally, this proved to be incorrect.

Table 3 shows electrical characterization data for two slices. The first, C8(32), was prepared by ion implantation and had an active layer doping of 1 x 10^{17} cm^{-3}. The second, CLD32, was prepared by VPE and had an active layer doping of 4 x 10^{16} cm^{-3}. The data show that the higher doped slice has a higher current capability even though the magnitude of its pinch-off voltage is lower than that of CLD32. Accordingly, the propagation delay of circuits on CLD32 would be expected to be larger than that obtained on the corresponding circuit on C8(32). This expectation is confirmed by the data.

Table 2

Summary of Logic Gate Characteristics

L = 1 μm, T = 300 K

Gate Type	$\langle t_{pd} \rangle$ for FO = 1 (ps)	FO Sensitivity (ps)	P_d (mW)	
BFL	85	17	39	
SDFL	100	35	22	
CCL	60	25	10	V_p = -2.5 V
FFS	60	22	16	
E/D	48	35	0.5	

Table 3

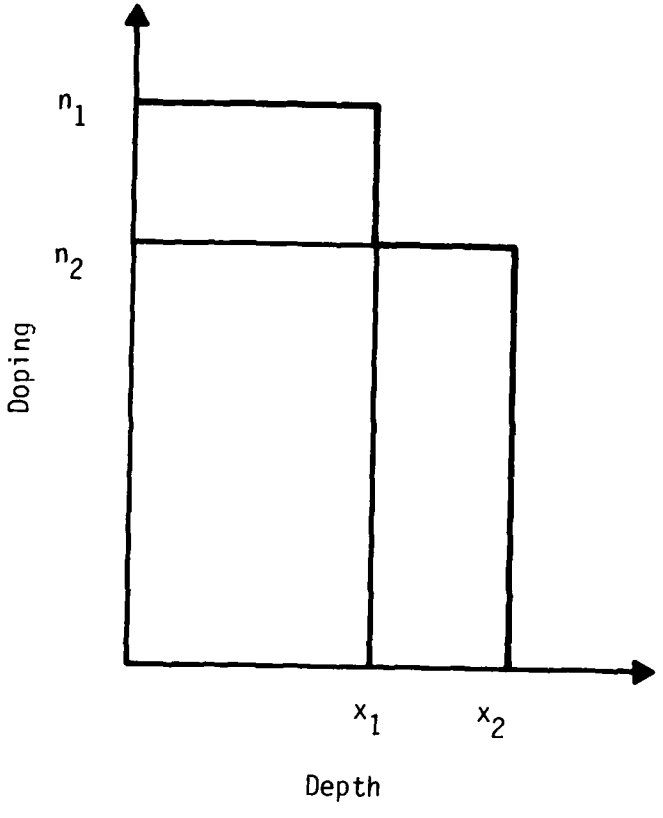
Characterization Data of Low-Doped and High-Doped Active Layers

Slice	$I_{DS\ max}$ (mA/mm)	I_{DSS} (mA/mm)	V_p (V)	R_{ON} (Ω)	$\langle t_{pd} \rangle$ (ps) L ≈ 1.6 μm FO = FI = 1
C8(32) $n = 1 \times 10^{17}$ cm^{-3}	293	211	-2.50	4.6	108
CLD32 $n = 4 \times 10^{16}$ cm^{-3}	223	170	-2.75	6.5	151

For a better understanding of the above results consider Figure 5. Here two idealized active layer doping profiles are shown. The Schottky gate is assumed to be recessed to a depth equal to the surface depletion layer. As shown on Figure 5, for $V_{p1} = V_{p2}$, then $n_1 x_1^2 = n_2 x_2^2$. The current between source and drain is assumed to be limited by velocity saturation and the channel cross section in the equations of Figure 5. The end result of such an analysis is that $I_{DS\ max}$ and I_{DSS} vary approximately with the square root of the active layer doping concentration.

Figure 6 shows the experimentally measured relationship between $I_{DS\ max}$ and n and verifies the relationship postulated above. Since the pinch-off voltages on these slices were not identically -2.5 V, the V_p, $I_{DS\ max}$ data for each slice was fitted to a straight line by linear regression and the $I_{DS\ max}$ value at V_p = -2.5 V was extracted.

The speed of all logic gates is governed by the rapidity with which the circuit signal nodes can be charged and discharged. For all the logic gates we have investigated, the signal node fall-time is inversely related to $I_{DS\ max}$,



$$\phi_B - V_p = \frac{QN}{2\varepsilon} X^2 \rightarrow N_1 X_1^2 = N_2 X_2^2 \quad (\text{For } V_{P1} = V_{P2})$$

$$I_{DS1} = Q v_o Z N_1 (X_1 - X_D)$$

where

$$X_1 = \sqrt{\frac{2\varepsilon}{QN_1} (\phi_B - V_{P1})}$$

and

$$X_D \cong \sqrt{\frac{2\varepsilon}{QN_1} (\phi_B - V_{GS} + \frac{V_D \ell}{\mu}}$$

for $V_{GS} > 0$

$$\frac{I_{DS1}}{I_{DS2}} \cong \sqrt{\frac{N_1}{N_2}}$$

Figure 5 Model to Study the Effect of Doping

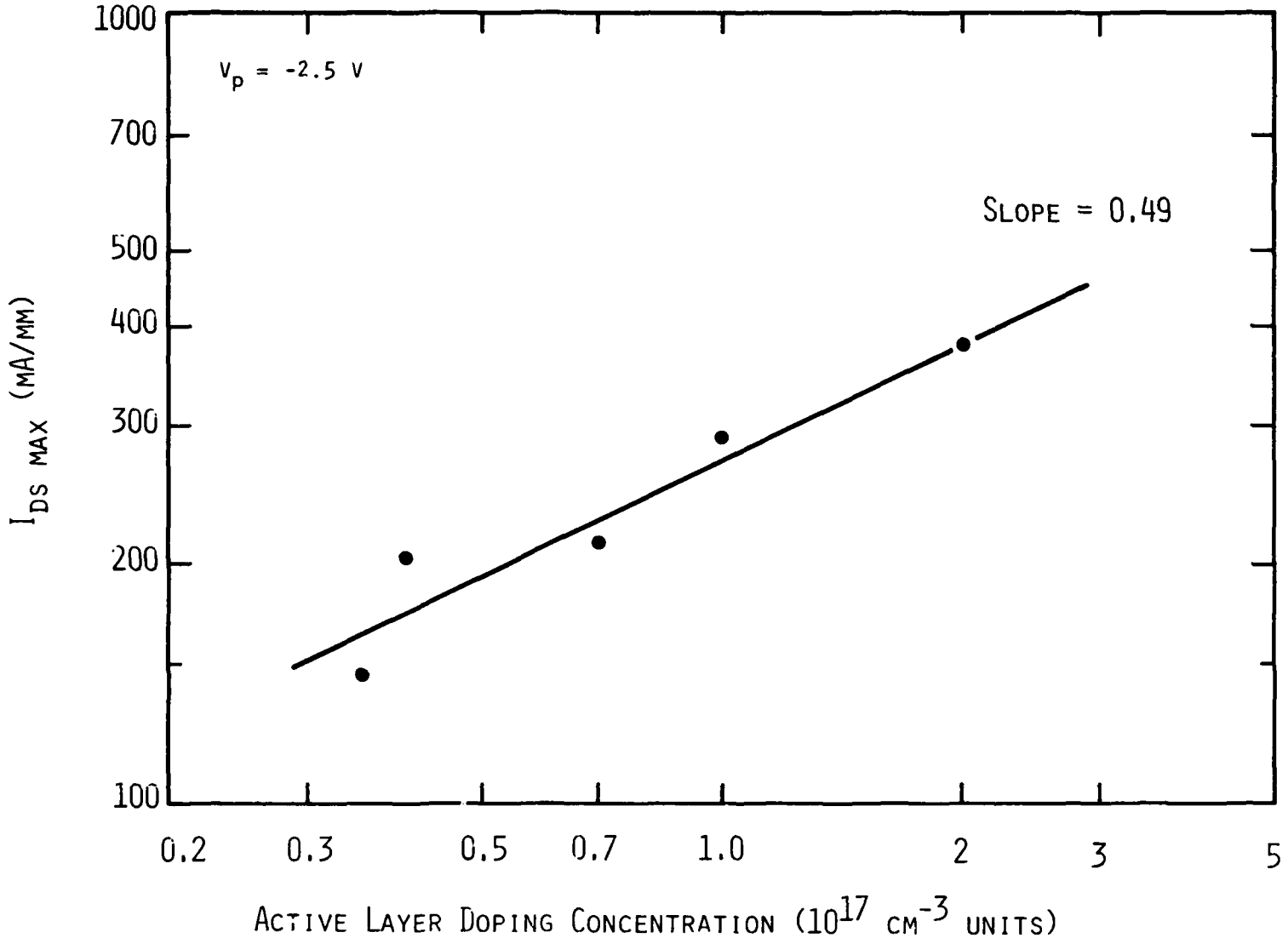


Figure 6 Experimentally Measured Relationship Between $I_{DS\ max}$ and Active Layer Doping Concentration

while the rise-time is inversely related to I_{DSS}. The propagation delay would therefore be expected to vary approximately as $1/\sqrt{n}$. (This is not strictly true since gate stripe capacitances are dependent on doping. In Reference 6, it is shown that gate stripe capacitances are small compared to total node capacitance. A root-mean-square method can be used to correct the propagation delay for this effect. However, the correction factor is quite small and can generally be ignored.) On the other hand, it should be obvious that the power dissipation will increase approximately as $\sqrt{n}$. Accordingly, the delay-power product is expected to be independent of doping.

The importance of the foregoing is that for maximum speed, the active layer doping should be increased to the maximum practicable value. This value is that which will result in obtaining σ/μ spreads of 10% reproducibly and was established experimentally. Slices with active layer dopings of 2.0, and 3.0×10^{17} cm^{-3} were implanted and evaluated. The mean value of $I_{DS\ max}$ for the slice doped at 3×10^{17} cm^{-3} was 351 mA/mm, significantly below the expected value of 470 mA/mm. This discrepancy is beleived to be the result of the highly nonideal profile caused by recessing close to the breakpoint of the profile. That is, at these doping levels, the rectangular approximation is no longer valid. On the other hand, the mean value of $I_{DS\ max}$ for the slice doped at 2.0×10^{17} cm^{-3} was in accordance with expectation. Based on this assessment, we have concluded that the highest practical doping level for $V_p = -2.5$ V circuits is about 2.0×10^{17} cm^{-3} when ion implantation technology is used.

Table 4 shows the results obtained for the slice (D15) doped at 2×10^{17} cm^{-3}. These results are compared to those obtained on slice C8(32) that had an active layer doping of 1×10^{17} cm^{-3}. Because $\langle V_p \rangle = -1.95$ V for this slice, whereas it was -2.5 V for C8(32), the R_τ ratios are somewhat higher than 0.71. It is worth noting that the delay-power products of the two slices are about the same.

Table 4

Propagation Delay and Power Dissipation

Slice: D15 $n = 2 \times 10^{17}$ cm^{-3} $\langle V_p \rangle = -1.95$ V $L = 2$ μm

Gate: BFL

Slice	FO	$\langle t_{pd} \rangle$ (ps)	(P_d) (mW)	R_τ
D15	2	124	56.3	0.81
		(7.5)	(10.8)	
D15	8	263	59.9	0.79
		(6.1)	(10.8)	

σ/μ ratios shown in parentheses.

R_τ is the $\langle t_{pd} \rangle$ of a particular circuit type divided by $\langle t_{pd} \rangle$ of the corresponding circuit on slice C8(32). Active layer doping of C8(32) was 1×10^{17} cm^{-3}.

SECTION V
TEMPERATURE CHARACTERISTICS

Figure 7 shows a photograph and an illustration of the arrangement used to make on-slice electrical measurements over the 77 to 430 K temperature range. At 77 K, no frosting occurs because LN_2 evaporation is sufficient to maintain a positive chamber pressure. For $77 < T < 300$, dry N_2 is directed to the LN_2 inlet port and frosting is minimal. The size of the probe ports permits about a ± 5 mm motion in both x and y; for additional slice motion, the slice is pnysically moved with a simple tool.

A. Device Behavior

This study includes the measurements of doping profiles, Schottky barrier height, fat-FET and van der Pauw mobility, and FET characteristics as a function of temperature. In addition, Deep Level Transient Spectroscopy (DLTS) measurements were also made (see Section II.B). The data reported are primarily for test devices on slice CLC21. The buffer and active layers of this slice were grown sequentially by vapor phase epitaxy. The 10^{17} cm^{-3} (m = 60 nm/decade) active layer was anodically thinned to ~ 400 nm. This was followed by a chemical surface etch of ~ 140 nm (to reduce the subsequent gate recess etch depth). A long range uniformity of 6.8% (σ/μ) on ungated source/drain structures was obtained which is satisfactory for circuit fabrication. (This also suggests that the VPE active layer preparation techniques can satisfy uniformity requirements for GaAs MSI circuit complexity.) The circuits were fabricated using the standard process (B^+ isolation).

1. Doping Profile Measurements

Figure 8 shows the doping profile of a C-V structure at several temperatures. The figure shows that the variation in doping profile is not very large over the 77 K to 373 K temperature range. As the temperature is increased from 77 K to 173 K (range I), the peak doping increased by ~ 6%, probably because neutral donors became active. Since 3 kT/2 = 10 meV at 77 K

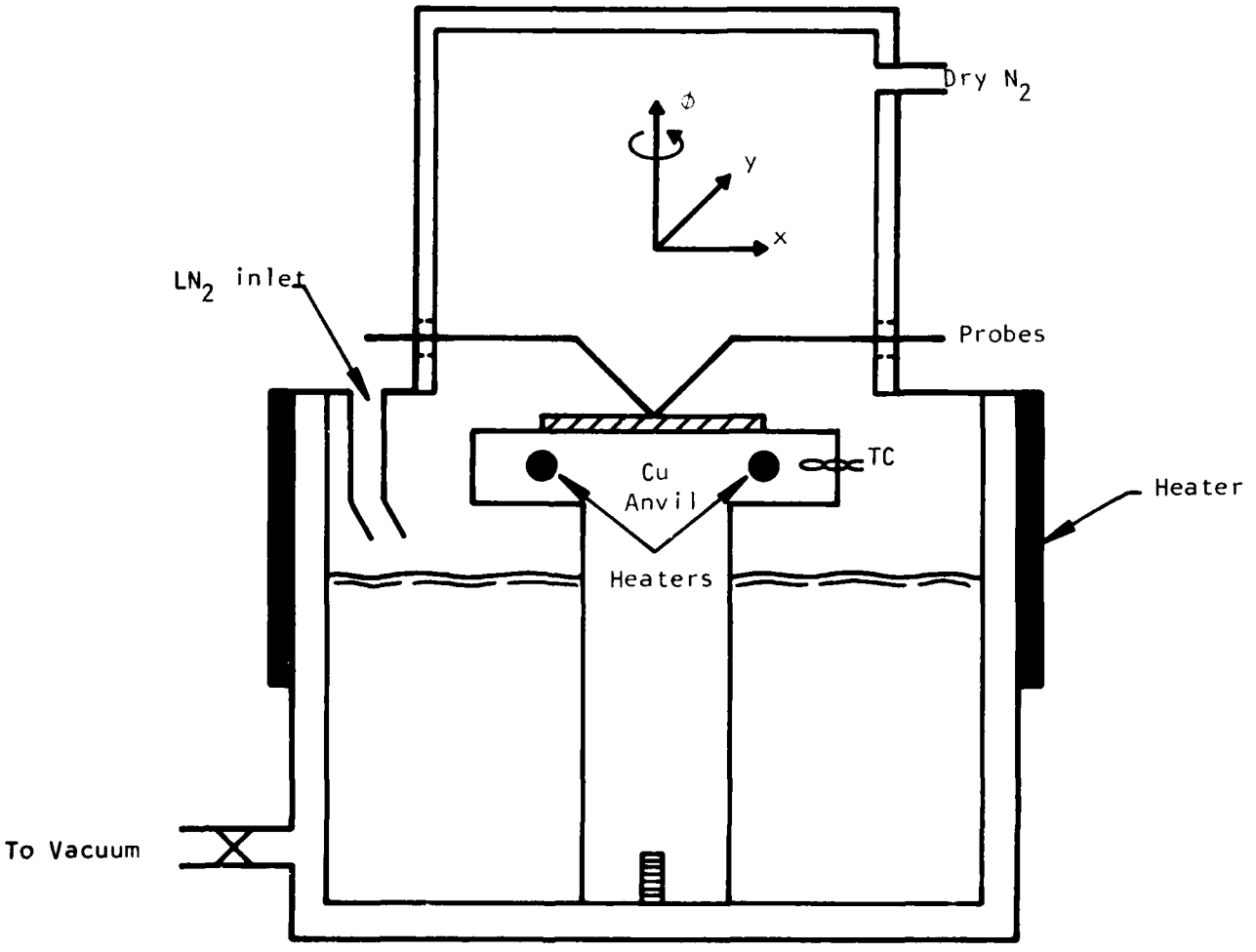


Figure 7 Experimental Arrangement for Low Temperature Measurements

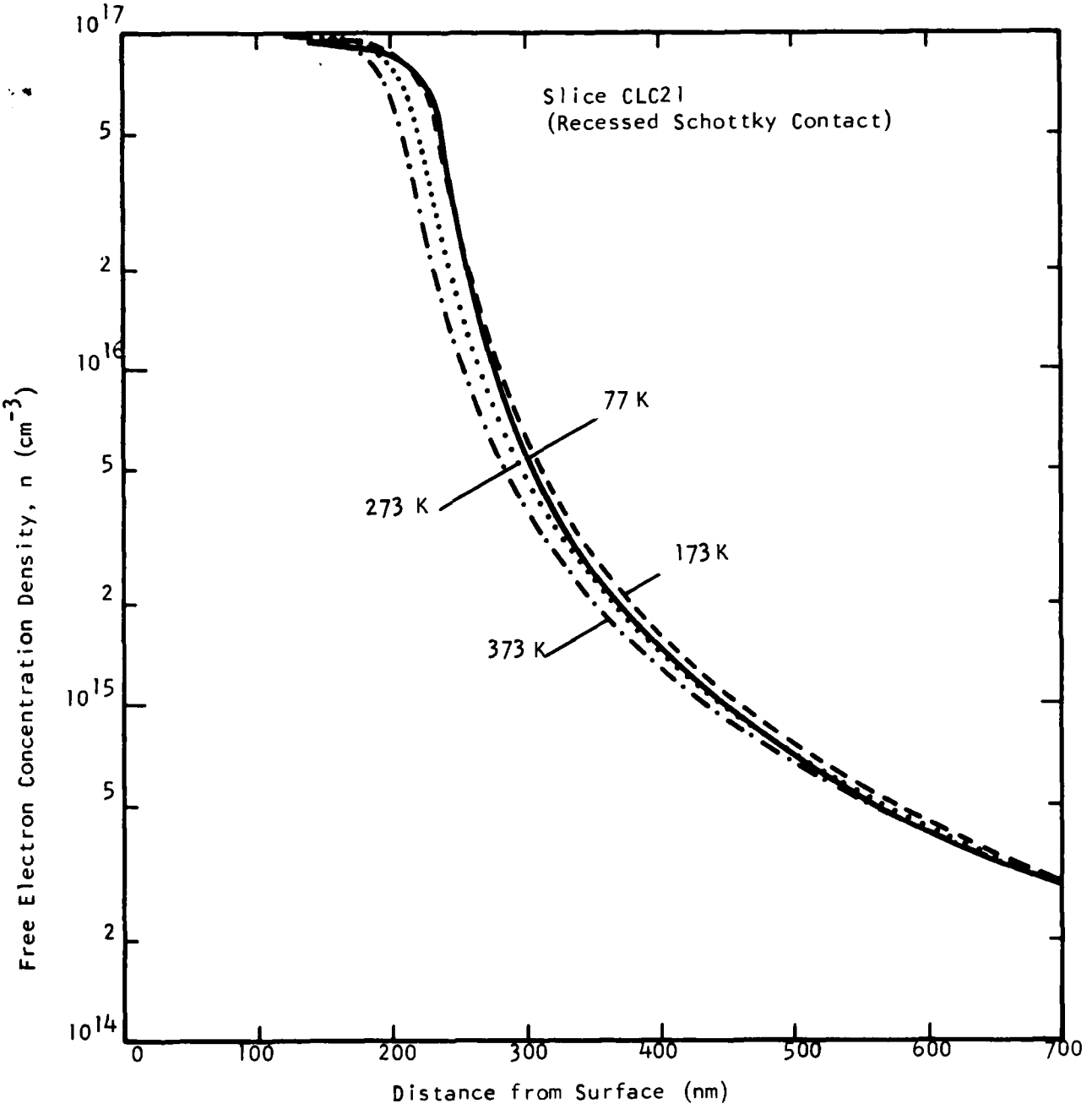


Figure 8 Doping Profile of Slice CLC21 At Several Temperatures

and since the ionization energy for the S impurity used in slice CLC21 is 6 meV, this is a reasonable assumption. However, the point at which $n(x_1) = 0.1\ n_{peak}$ is seen to be very nearly unchanged. As the temperature is increased from 173 K to 373 K (range II), n_{peak} remains constant while x_1 moves toward the surface at a rate of ~ 0.1 nm/°C. This behavior suggests that a change of -0.08%/°C in $(\phi_B - V_p)$ over range II should be expected. This, in turn, implies a change in $(\phi_B - V_p)$ of ± ~ 260 mV over range II, which is in reasonable agreement with the ± 175 mV variations typically measured.

To confirm the results of Figure 8, several other structures were profiled at 77 and 300 K. Identical results were obtained.

2. Schottky Barrier Height Measurements

The thermionic emission-diffusion theory of current transport across a Schottky barrier results in the equation

$$I_F = SAT^2 \exp\left(\frac{-q\phi_B}{kT}\right) \exp\left(\frac{qV_F}{nkT}\right) \quad ; \quad V_F > 3\ kT/q \quad , \qquad (1)$$

where the symbols have their usual meaning. The barrier height dependence on bias is usually incorporated through the ideality factor n. If Equation (1) is plotted on semi-log graph paper, a straight line should result. The extrapolated value of the forward current at $V_F = 0$ gives the saturation current, I_S, from which the barrier height may be determined.

Forward bias measurements were made on a diode structure at nine different temperatures over the 77 to 423 K range. V_F was recorded for I_F ranging from 1 μA to 10 mA in a 1, 2, 5 sequence. Figure 9 shows a plot of the data for $I_F \leq 1$ mA and demonstrates that Equation (1) behavior is maintained over the entire temperature range. Note also that the value of V_F necessary to sustain any fixed I_F decreases monotonically with temperature. After V_F was corrected for the series resistance drop, the data were analyzed by linear regression to obtain n, I_S, and ϕ_B. The results are presented in

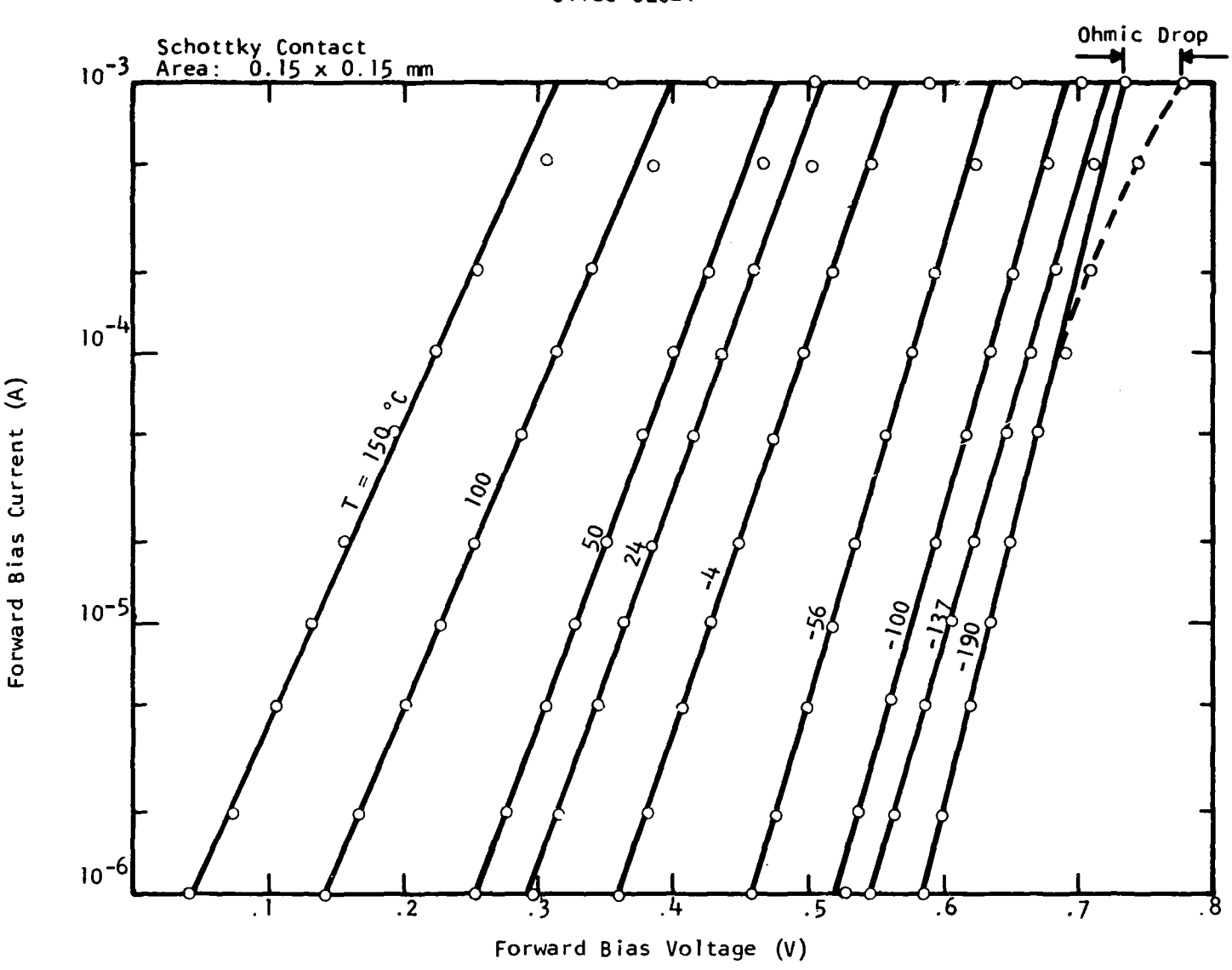


Figure 9 Schottky Diode Forward Characteristic at Several Temperatures

Figure 10. It is seen that the parameters of the Schottky contact are reasonably well behaved for T > -60°C. In this region $\phi_B \cong 0.71 \pm 0.04$ V, and n = 1.2 ± 0.1. For T < -60°C, ϕ_B decreases rapidly, while n increases rapidly. The reason for this behavior has not been determined, but is believed to be caused by changes in the interface state density that may result from changes in stress and/or from changes in the electrical activation of interface states as the Fermi level shifts with temperature.

3. Mobility Measurements

The dependence of average mobility on temperature was determined with the use of fat-FET structures. At each temperature the channel resistance was measured at five equally spaced I_{DS} values with $V_{GS} = 0$. (The maximum I_{DS} value was restricted to be about 10% of I_{DSS}.) The data were then analyzed by linear regression to obtain the channel resistance under zero bias conditions. Under the assumption that the channel height and free carrier concentration density are independent of temperature, the mobility was extracted. The solid curve of Figure 11 shows the results obtained with μ (T) normalized to μ (300 K).

The assumption of constant channel height and free carrier concentration density is known to be incorrect from the results of Figures 8 and 10. The implications of those data on the results shown are discussed below. Figure 11 suggests that over range II the mobility decreases at a rate of about -0.16% per °C. Since ϕ_B is approximately constant over this range, while $\int$ ndx decreases at about -0.08% per °C, the actual mobility variation is closer to about -0.08% per °C. Over range I, $\int$ ndx increases by ~ 0.06% per °C (neutral donors become active), while ϕ_B increases rapidly with temperature. The effect of increasing ϕ_B is to broaden the depletion width, which thereby reduces the channel height. Analysis of the data suggests that the channel height changes by about -0.2% per °C due to ϕ_B variation. These considerations indicate that the actual mobility variation in range I is about 50% greater than that shown.

The above discussion may be used to construct an estimate of the actual mobility profile. Such an estimate is shown by the dashed curve of Figure 11. Both curves in the figure suggest that the mobility at any

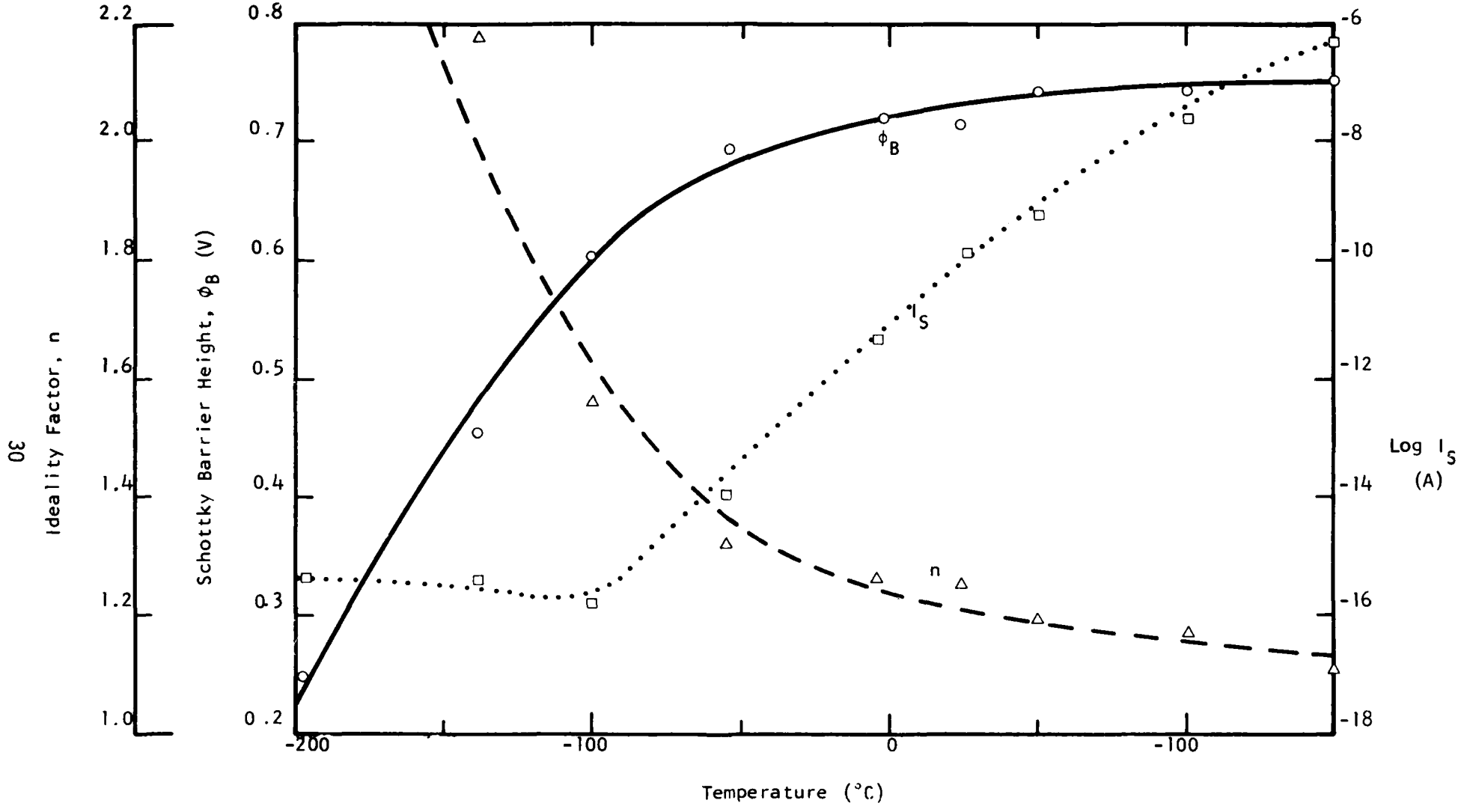


Figure 10 Dependence of Schottky Barrier Height on Temperature

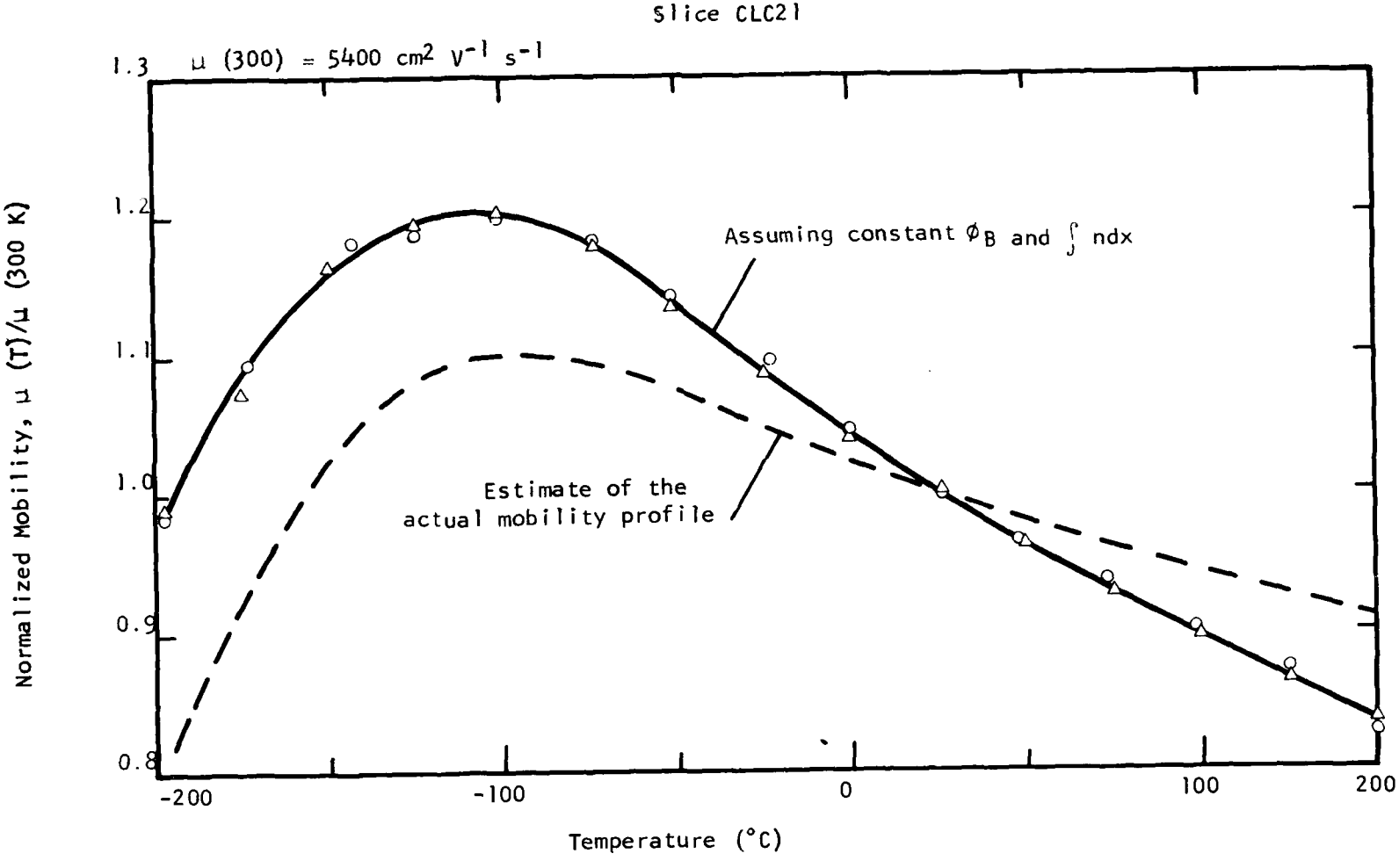


Figure 11 Effect of Temperature on Electron Mobility as Determined by Fat-FET Measurements

temperature between 77 K and 423 K is within ± 20% of μ (300 K). Further, a mobility peak at ~ 160 K is indicated. A word of caution: Figure 11 is applicable only to GaAs material underlying a Schottky gate of the type employed in our process. Stress-induced mobility effects may be different with other gate metallization schemes.

Finally, the mobility was measured by the van der Pauw technique. Two devices were evaluated; mobilities of 5600 and 4990 $cm^2\ V^{-1}\ s^{-1}$ at 77 and 300 K, respectively, were obtained for one, while 5510 and 4910 $cm^2\ V^{-1}\ s^{-1}$ were obtained for the other. The 300 K results are within 10% of the results obtained by the fat-FET method. The discrepancy between the results of the two techniques is larger at 77 K and is about 25%. This difference is thought to be caused by the stress-induced effects of the Schottky contact.

4. DLTS Measurements

The results of these measurements were discussed in Subsection II.B. The conclusions impacting device behavior are reiterated, below. In all the material studies, the trap energies are deep enough not to appreciably change occupancy (i.e., their degree of ionization according to a Boltzmann distribution) for temperature changes decreasing from 300 K. And, for temperatures > 300 K, device properties are not expected to be significantly affected because trap concentration densities are small compared to the free electron concentration density.

5. FET Characteristics

a. Depletion Mode Devices

Figure 12 shows the I-V characteristics of a 100 μm wide test FET at various baseplate temperatures. The dominant feature is that $I_{DS\ max}$ and I_{DSS} decrease monotonically with a temperature coefficient of about -0.2% per °C. Additionally, the pinch-off voltage is seen to have a small but obvious dependence on temperature over $77 < T < 300$ K.

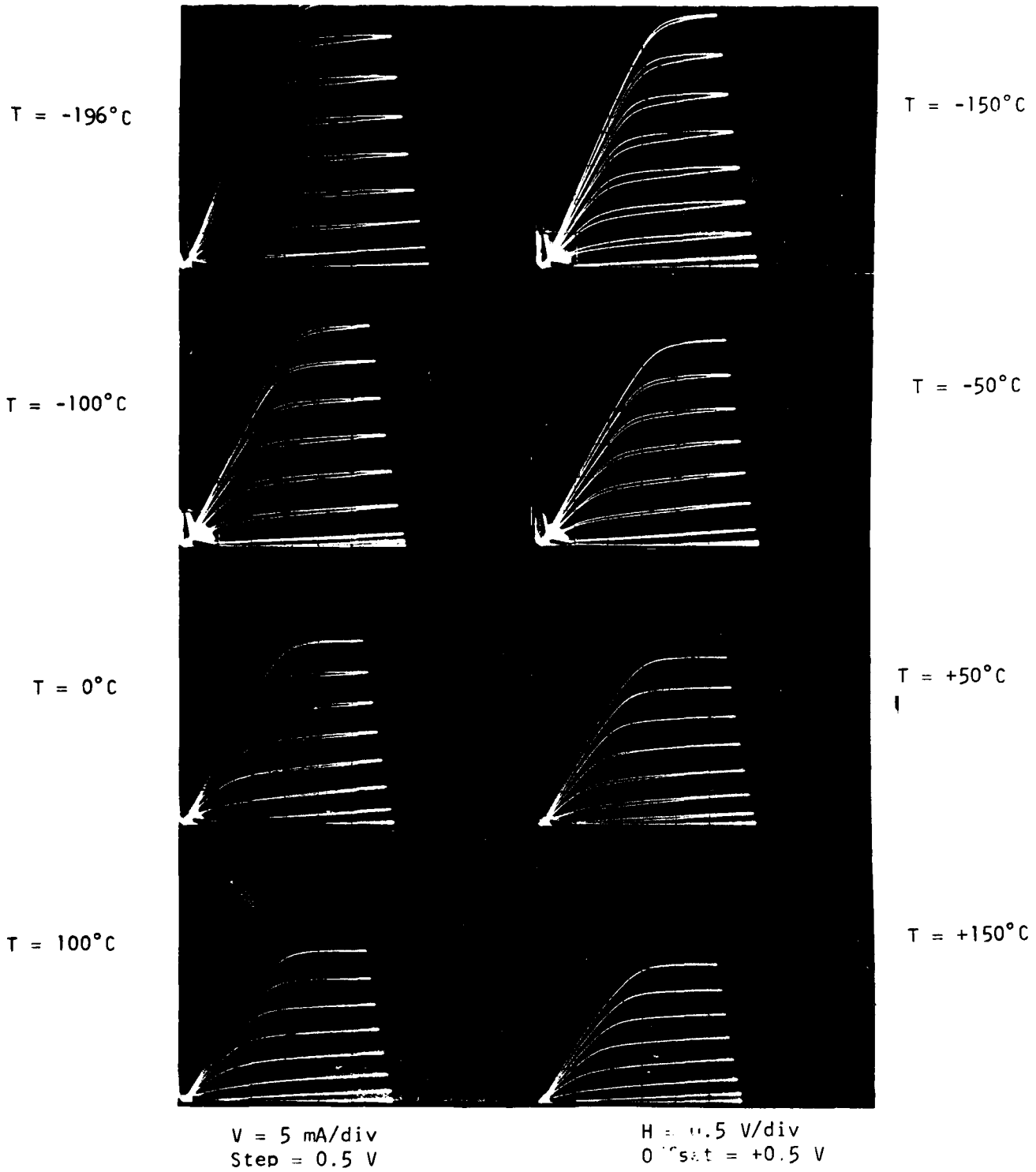


Figure 12 I-V Characteristics of a 100 μm Wide rET at Various Baseplate Temperatures (Slice: CLC21)

Figure 13 shows detailed measurements of how $I_{DS\ max}$, I_{DSS}, and V_p vary with temperature for a typical FET structure (source-drain spacing of 5 μm, L = 1 μm). Although there seems to be some structure within narrow temperature ranges, a straight-line fit to $I_{DS\ max}$ and I_{DSS} can be reasonably made. Both can be safely treated as having a temperature coefficient of about -0.2% per °C over the entire 77 to 423 K temperature range. The pinch-off voltage, on the other hand, is practically constant for the 220 to 423 K temperature range. Over the 77 to 220 K temperature range these -2.5 V pinch-off devices can be treated as having a temperature coefficient of ~ -5 mv per °C (which is probably due to ϕ_B variation). Hysteresis effects were typically < 2% on I_{DSS} and $I_{DS\ max}$ and < 5% on V_p. The above results were confirmed for several FETs across the slice by measurements at 300 and 77 K. The ratios of $I_{DS\ max}$, I_{DSS}, and $(\phi_B - V_p)$ at 77 K to that at 300 K were determined to have a mean value of 1.47, 1.57, and 1.19 respectively (with σ/μ spreads of 1.6, 1.9. and 5.6%).

Similar results were obtained on several ion implanted slices ($n \cong 10^{17}$ cm^{-3}) characterized at baseplate temperatures of 300 and 77 K. Table 5 shows typical data summarized in the form of parameter ratios, i.e., parameter at 77 K divided by the parameter at 300 K. Note that these data are very similar to the data obtained on the VPE slice and suggest that VPE and ion implanted active layers are approximately equivalent in terms of temperature effects.

The above data may be used to obtain an estimate of the effect of temperature on saturation velocity. Over range II, the mobility variation of -0.08% per °C affects the channel height by ~ -0.04% per °C. Since $\int$ ndx variation accounts for another -0.08% per °C, this suggests that the effective carrier saturation velocity varies by about -0.08% per °C.

b. Enhancement Mode Devices

Extensive low temperature evaluation of slice E1-2 was undertaken to investigate the effect on the logic levels. FET test data at 300 and 77 K are shown in Table 6. Here, $I_{DS\ max}$ is the source-drain saturation current for V_{GS} = 1.0 V, and V_p is defined as the gate voltage for which I_{DS} =

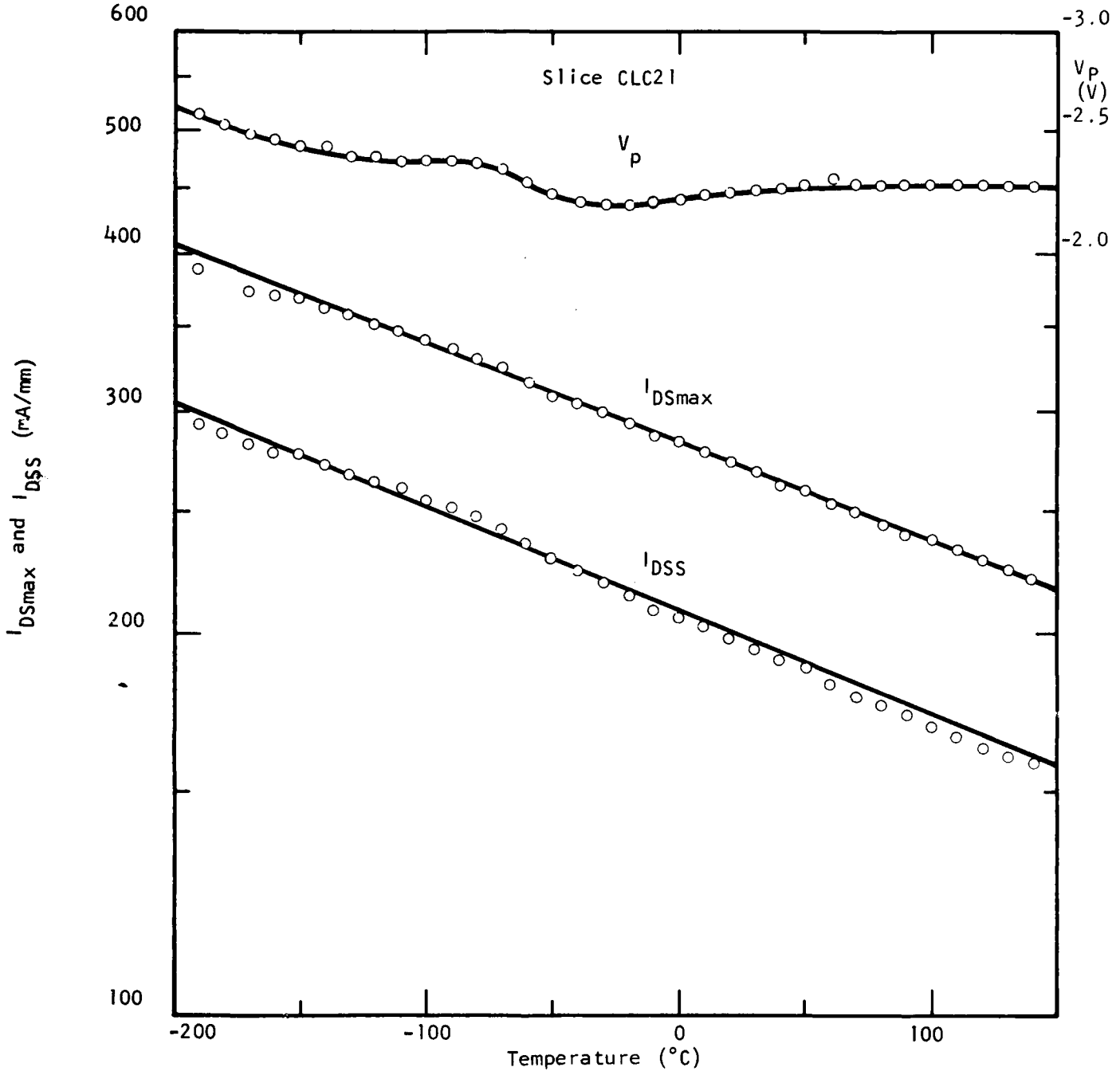


Figure 13 Effect of Temperature on $I_{DS\ max}$, I_{DSS}, and V_p for a Typical FET Structure

Table 5

Parameter Ratios of FETs at Baseplate Temperatures of 77 and 300 K. Slice C8(32).

Device No.	I_{DSS}	$I_{DS\ max}$	V_p	R_{on}
1	1.44	1.43	1.10	0.91
2	1.46	1.42	1.12	0.98
3	1.46	1.44	1.10	0.89
4	1.34	1.48	0.86	0.84
5	1.46	1.41	1.09	0.89
6	1.54	1.51	1.10	0.84
7	1.33	1.33	1.11	--
8	1.38	1.35	1.10	1.00
9	1.76	1.61	1.65	0.78
10	1.75	1.64	1.28	0.75
11	1.49	1.46	1.09	0.83
12	1.45	1.43	1.09	0.86
13	1.31	1.31	1.01	0.89
14	1.47	1.42	1.12	0.88
15	1.51	1.49	1.10	0.84
16	1.48	1.45	1.09	0.91
μ	1.48	1.45	1.14	0.87
$\sigma/\mu\%$	8.5	6.1	13.0	7.5

0.05 $I_{DS\ max}$. V_{on} is related to the lower logic level and is defined as the drain voltage at which $I_{DS} = 0.5\ I_{DS\ max}$ for $V_{GS} = 1.0$ V. It is seen that FET current drive capability is increased by ~ 15% and that the lower logic level is decreased by about 60 mV by the lower temperature.

Table 6

Mean Values of Enhancement Mode FET Characteristics at 300 and 77 K (Slice E1-2)

T (K)	$I_{DS\ max}$ (mA/mm)	V_p (V)	V_{on} (V)	g_m (mS/mm)
300	55.2	0.36	0.29	82
77	63.6	0.40	0.23	101

It is not known if the results shown in Table 6 are representative of all e-mode FETs since E1-2 was the only slice characterized at 77 K. (The 300 K results are typical of other slices.) However, it should be pointed out that the gate metallization and doping layer for this slice differ significantly from those used for depletion mode slices. If the results of Table 6 are representative, then the speed improvement of E/D circuits would be expected to be less than that of depletion mode circuits. Some of these results have been reported in the literature. A copy is contained in Appendix B.

6. Implications for Logic Gate Performance

For 10^{17} cm^{-3} active layers and -2.5 V pinch-off circuits, the effect of temperature on $\int ndx$, ϕ_B, mobility, and saturation velocity is relatively small over a broad temperature range. These small effects act in concert to affect device currents by about -0.2% per °C. Based on our understanding of logic circuit operation, we would expect the propagation delay to also have a temperature coefficient of about -0.2% per °C. This expectation is close to the experimentally measured value.

The other aspect of some importance to logic gate operation is the effect of temperature on the I_F V_F characteristic of Schottky diodes. Figure 9 shows that at fixed forward current bias, the diode drop decreases monotonically with temperature. For example, the diode string drop on slice CLC21 is about 4.0 V and 3.4 V at 77 and 300 K, respectively (at the respective pull-down currents). Both the upper and the lower logic levels depend on this voltage drop. Fortunately, the upper logic level can always be obtained by adjusting the V_{DD} bias supply. The lower logic level cannot always be attained by adjusting the V_{SS} supply. Accordingly, the diode string drop should be designed to be adequate at the maximum temperature at which the circuit is expected to be functional.

Although the majority of the results of this subsection were obtained from a single VPE slice, active layers prepared by ion implantation were shown to yield similar FET results. Accordingly, properly designed GaAs MESFET logic circuits can be expected to be functional over very broad temperature ranges. The military specification of -55°C to +75°C for electronic components should be readily realizable.

B. Ring Oscillator Results

The test system used for ring oscillator measurements consists of low frequency bias probes, a specially designed high frequency probe for sampling scope pick up, and a radiatively coupled probe for spectrum analyzer pick up. The test system is shown schematically in Figure 14. The bias supply probes are commercially available and have been modified by adding an rf choke with a shunt capacitor to ground located about 9 cm from the probe tip. The high frequency probe utilizes a standard probe base in which the probe tip has been replaced with a specially designed high frequency head. This unit, shown in Figure 15, consists of a 2 mm BeCu probe tip attached directly to a short section of a 50 ohm MIC transmission line, a 2 K-Ω chip resistor, and another 50 ohm line connected to the center conductor of a 50 ohm coaxial connector.

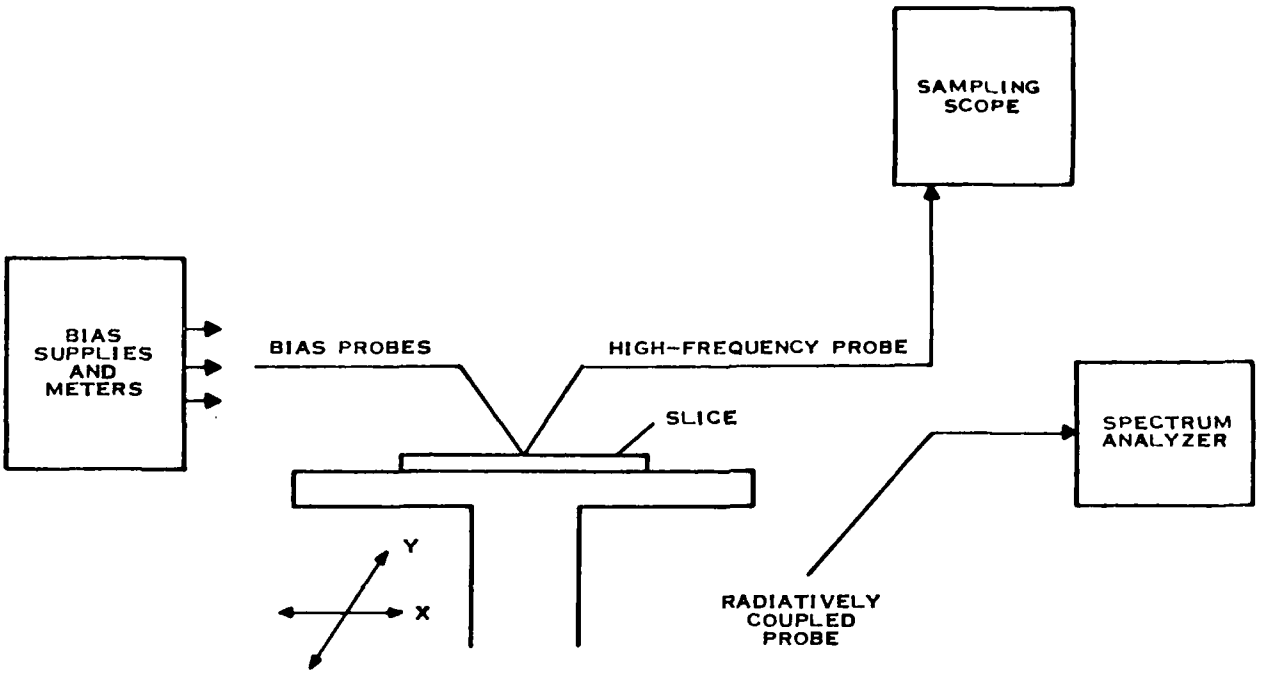


Figure 14 High-Frequency Test System

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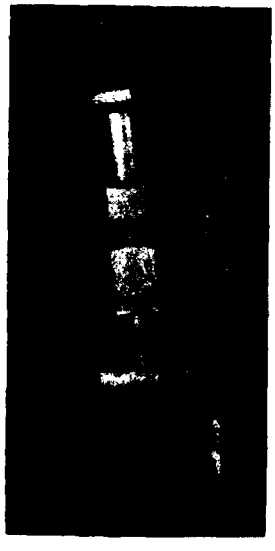

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Figure 15 High-Speed Probe Arrangement

Attenuation of the output waveform by the 2 K-Ω chip resistor and the succeeding 50 ohm system is necessary to avoid excessive loading of the output buffer. This probe was then characterized to determine vertical sensitivity; its frequency response was flat (within ± 2.5 dB) to 4 GHz.

1. Depletion Mode Gates

The BFL RO circuits on slice CLC21 were characterized at the two baseplate temperatures of 77 and 300 K. The master field selected was that from which the device characteristics shown by Figure 13 were obtained. Of the 16 BFL circuits, 11 were functional. Measurements were made at bias conditions: V_{DD} = 5.50 V, V_{SS} = -4.00 V at 300 K; and V_{DD} = 6.50, V_{SS} = -4.00 V at 77 K. Table 7 shows the data summarized in the form of parameter ratios, i.e., the parameter at 77 K divided by the parameter at 300 K. The first two columns are for I_{DD} and I_{SS} bias currents with the third column being the average of them. The fourth column is for the frequency of RO operation and indicates that on average the propagation delay at 77 K is 67% that obtained at 300 K. For example, the fastest circuit (L = 0.5 μm, FO = 1) shows propagation delays of 45.0 and 69.9 ps at 77 and 300 K baseplate temperatures respectively. The fifth column is the ratio of the previous two columns. It shows that the increase in circuit speed is directly proportional to the magnitude of the currents available for charging and discharging the circuit node capacitances. The sixth column is for power dissipation. Since the diode string voltage drop is greater at 77 K than at 300 K, it was necessary to increase V_{DD} for proper circuit operation. Accordingly, the increase in power dissipation is somewhat greater than the increase in circuit currents. The data of Table 7 indicate, on average, that the delay-power product at 77 K is about 11% greater than that at 300 K.

The above measurements were then repeated for each circuit by applying the optimum bias voltages at each of the two baseplate temperatures. In this case, propagation delays were typically reduced by ~ 5%. The results obtained upon data reduction were very similar to those shown by Table 7.

Table 7

Parameter Ratios of Five-Stage ROs at Baseplate Temperatures of 77 and 300 K

Slice: CLC21
Gate: BFL

L	FO	I_{DD}	I_{SS}	I	f	I/f	P_d
0.5	1	1.53	1.52	1.52	1.55	0.980	1.71
0.5	2	1.53	1.47	1.50	1.52	0.988	1.69
0.5	4	1.55	1.50	1.52	1.54	0.989	1.72
1	2	1.49	1.46	1.48	1.49	0.993	1.66
1	8	1.44	1.53	1.49	1.38	1.076	1.71
1.5	1	1.42	1.46	1.44	1.46	0.987	1.61
1.5	2	1.46	1.46	1.46	1.46	1.003	1.64
2	1	1.42	1.44	1.43	1.47	0.975	1.60
2	2	1.47	1.54	1.51	1.53	0.988	1.67
2	4	1.46	1.52	1.49	1.42	1.049	1.66
2	8	1.42	1.45	1.44	1.57	0.916	1.60
		———	———	———	———	———	———
	μ	1.47	1.49	1.48	1.49	0.995	1.66
	σ/μ(%)	3.2	2.4	2.2	3.9	4.1	2.7

To determine whether Table 7 results are dependent on the method of active layer preparation, the BFL RO circuits of an ion implanted slice were characterized at the two baseplate temperatures. Measurements were made at standard bias conditions: V_{DD} = 6.0, V_{SS} =-4.0 V at 300 K; and V_D = 6.5, V_{SS} = -4.0 V at 77 K. Table 8 shows the data summarized in the same format as Table 7. The mean value for the fifth column is 0.935 which differs from the 0.995 obtained for slice CLC21. This suggests that the parasitic node capacitances at 77 K are slightly lower (~ 6%) than those at 300 K for this slice. Although both substrates are Cr-doped, they came from different ingots. It may well be that the position of the "virtual" ground for slice CLC21 is substantially independent of temperature whereas that of slice C8(32) is somewhat temperature dependent. The last column is for power dissipation. The data indicate, on average, that the delay-power product at 77 K is nearly the same as that at 300 K.

The results shown by Table 7 and 8 are typical of those obtained on other depletion mode logic gates (SDFL, CCL, and FFS), and on slices encompassing the -1.0 to -2.5 V pinch-off voltage range. It can therefore be generally concluded that circuit speeds are improved by ~ 50% (with a ~ 50% increase in power dissipation) when GaAs depletion mode circuits are operated at 77 K.

The effect of doping on data of the type shown by Tables 7 and 8 is illustrated by Table 9. The active layer doping of CLC21 and C8(32) was 1 x 10^{17} cm^{-3}, whereas that of CLD32 was 4 x 10^{16} cm^{-3}. The data of Table 9 show a speed improvement of 68% at 77 K as compared to that at 300 K. This is greater than the 50% improvement shown by the other two slices. However, as shown by Table 3 (Section IV.B), the circuits on slice CLD32 were ~ 40% slower than the corresponding circuits on the other two slices at 300 K. Accordingly, the circuits on the more highly doped layers are still faster than the corresponding ones on the more lightly doped layer at 77 K.

Table 8

Parameter Ratios of Five-Stage ROs at Baseplate Temperatures of 77 and 300 K.

Slice: C8(32) Gate: BFL FO = 1

L (μm)	I_{DD}	I_{SS}	I	f	I/f	P_d
0.5	1.37	1.39	1.38	1.40	0.989	1.45
0.5	1.37	1.40	1.39	1.52	0.912	1.46
0.5	1.38	1.41	1.39	1.53	0.912	1.47
0.5	1.37	1.42	1.39	1.52	0.918	1.46
0.5	1.44	1.47	1.46	1.25	1.169	1.50
0.5	1.39	1.43	1.40	1.50	0.934	1.48
0.5	1.39	1.46	1.43	1.56	0.914	1.49
0.5	1.40	1.42	1.41	1.54	0.918	1.49
1.0	1.36	1.40	1.38	1.51	0.912	1.45
1.0	1.36	1.41	1.38	1.51	0.913	1.45
1.0	1.51	1.56	1.54	1.76	0.874	1.61
1.0	1.40	1.41	1.41	1.51	0.916	1.45
1.0	1.37	1.41	1.39	1.45	0.957	1.46
1.0	1.43	1.52	1.47	1.51	0.976	1.54
1.0	1.40	1.43	1.42	1.55	0.912	1.49
1.5	1.35	1.40	1.37	1.47	0.931	1.44
1.5	1.34	1.36	1.35	1.46	0.923	1.42
1.5	1.39	1.40	1.40	1.50	0.934	1.47
2.0	1.36	1.39	1.38	1.47	0.936	1.44
2.0	1.37	1.38	1.37	1.49	0.919	1.45
2.0	1.42	1.47	1.45	1.48	0.980	1.52
2.0	1.37	1.39	1.38	1.51	0.914	1.49
2.0	1.39	1.40	1.40	1.65	0.844	1.47
2.0	1.38	1.40	1.39	1.50	0.929	1.47
μ	1.39	1.42	1.40	1.51	0.935	1.48
σ/μ%	2.6	3.1	2.8	5.9	6.3	2.7

Table 9

Parameter Ratios of Five-Stage ROs at Baseplate Temperatures of 77 and 300 K

Slice: CLD32 Logic Bell: BFL FO = 1

L (μM)	I_{DD}	I_{SS}	I	F	I/F	P_D
1.0	1.61	1.60	1.60	1.57	1.02	1.59
1.0	1.58	1.58	1.58	1.72	0.92	1.58
1.0	1.63	1.71	1.67	1.53	1.09	1.79
1.5	1.52	1.47	1.49	1.75	0.85	1.50
1.5	1.62	1.48	1.54	2.11	0.73	1.57
1.5	1.64	1.56	1.60	1.98	0.81	1.61
1.5	1.62	1.57	1.60	1.61	0.99	1.60
1.5	1.61	1.58	1.60	1.43	1.11	1.60
1.5	1.63	1.59	1.61	1.70	0.95	1.61
1.5	1.64	1.57	1.59	1.78	0.89	1.59
1.5	1.65	1.64	1.64	1.52	1.08	1.64
1.5	1.68	1.71	1.69	1.52	1.11	1.83
2.0	1.80	1.59	1.70	1.86	0.91	1.73
2.0	1.62	1.55	1.59	1.90	0.84	1.60
2.0	1.61	1.56	1.58	1.61	0.99	1.59
2.0	1.64	1.63	1.63	1.56	1.05	1.69
2.0	1.60	1.56	1.58	1.77	0.89	1.58
2.0	1.57	1.56	1.57	1.44	1.09	1.57
2.0	1.66	1.58	1.62	1.59	1.02	1.63
μ	1.63	1.58	1.60	1.68	0.97	1.63
σ/μ(%)	3.4	3.8	3.1	10.9	11.6	4.9

The importance of the study on temperature effects is twofold. First, it is a readily available method for increasing circuit speeds by 50%. Since circuit node capacitances[6] are predominately due to topside interelectrode parasitics, these cannot be reduced significantly (> 20%) by modification of cell layout or by further reduction of metallization geometries without trade-off penalties. For example, reducing the source-drain spacing will improve FET transconductance but will also increase all the interelectrode capacitances of the device. The optimum device geometry for logic applications is not known. However, we believe the device design window is fairly broad; that is, large variations in device design will result in small variations in circuit speed. This is borne out by the fact that similar propagation delays have been obtained by various investigators using a variety of device geometries and circuit layouts. By cooling the baseplate to 77 K, the capacitive parasitics are substantially unchanged while the large signal transconductance of the FET devices is significantly increased thereby reducing the propagation delay. Second, the study of temperature effects has provided quantitative experimental confirmation of our understanding of logic cell operation.

2. E/D Gate

Seventeen 19-stage ROs on slice E1-2 were evaluated at 300 and 77 K. The speed of the circuits at 77 K was 1.27 times (σ = 0.04) that at 300 K, with an I_{DD} ratio of 1.15 (σ = 0.05). These factors, in conjunction with the data of Table 6 may be used to determine the propagation delays of particular RO types at 77 K. For example, for L = 1.13 μm, a propagation delay of 38 ps results with a fan-out sensitivity of about 28 ps.

By operating ripple dividers at 300 and 77 K baseplate temperatures, it was observed that the upper logic level was increased by about 150 mV. This observation, together with that previously mentioned on the lower logic level, indicates that noise margins for E/D circuits are improved under 77 K operation.

3. High Temperature Characterization

An experimental arrangement was constructed for on-slice electrical characterizations to be made at baseplate temperatures up to 350°C. Three 5-stage ring oscillators on slice D11 were characterized to determine the maximum temperature of operation. Figure 16 shows the results. The frequency of each RO exhibits a temperature coefficient of about -0.18% per °C. This result is in good agreement with the temperature coefficient for $I_{DS\ max}$ and I_{DSS} typically observed (see Figure 15). The ROs were operated under standard supply voltages of V_{DD} = 6.0 and V_{SS} = -4.0 V for baseplate temperatures up to 220°C. Above 220°C, it was necessary to reduce the supply voltages for the ROs to operate. Under these reduced biases, the ROs were functional for baseplate temperatures up to 300°C. The ROs exhibited their original properties when the baseplate temperature was returned to room ambient.

These findings were also confirmed during the course of a reliability study done under TI internal funding. The results of this study were summarized and will appear in the Technical Digest of the 1983 International Reliability Physics Symposium. A copy of the paper is contained in Appendix C.

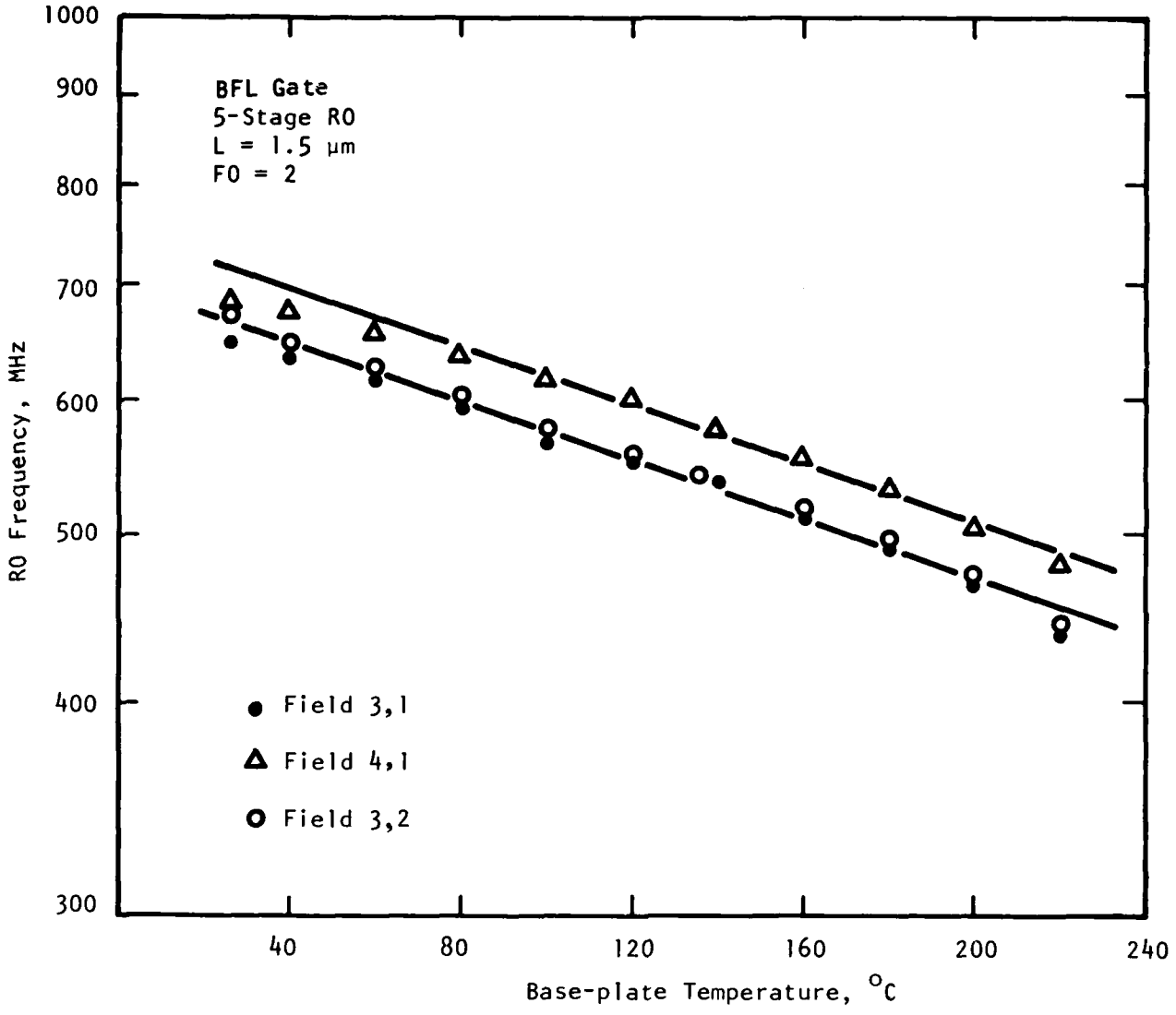

Figure 16 Dependence of Ring Oscillator Frequency on Baseplace Temperature (Slice D11)

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APPENDIX A

THE EFFECT OF LOGIC CELL CONFIGURATION, GATELENGTH, AND FAN-OUT ON THE PROPAGATION DELAYS OF GaAs MESFET LOGIC GATES

The Effect of Logic Cell Configuration, Gatelength, and Fan-Out on the Propagation Delays of GaAs MESFET Logic Gates

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Abstract—In this work, three different logic cell configurations, two with and one without a source-follower are employed. These logic cells are arranged in 5- and 11-stage ring oscillator (RO) circuits. The circuits are then fabricated with nominal gatelengths of 0.5, 1.0, 1.5, and 2.0 μm and fan-out loadings of 1, 2, 4, and 8 (consisting of source-gate capacitances). All these test circuits are incorporated into a 6-mm by 6-mm master field. Sufficiently large slices to result in a 4 × 4 array of the master field are used. Si^+ implantation into ⟨100⟩ Cr-doped Bridgman and not intentionally doped liquid encapsulated Czochralski (LEC) substrates have been used with success in terms of reproducibility, long range uniformity, and mobility.

Since circuit yields are high, each slice provides a sufficiently large data base for a meaningful statistical analysis to be carried out for each circuit type. These data (propagation delay versus circuit type) together with power dissipation results are presented. Preliminary modeling results of the experimental data are also presented.

I. Introduction

SINCE THE initial work of Van Tuyl and Liechti [1], GaAs digital integrated circuits have become the subject of intensive investigation at several laboratories. The motivation behind these investigations is the generally held opinion that GaAs circuits are faster than similar Si circuits. The speed advantage of GaAs vis-à-vis Si is still the subject of controversy. From the literature it appears that the speed advantage of logic circuits is considerably less than the approximately five-fold mobility advantage of GaAs over Si. Although a one-to-one circuit comparison is not available, the 4-GHz GaAs frequency divider [2] may be compared to the 1.5-GHz frequency synthesizer (÷M) using differential mode emitter-coupled logic (ECL) Si circuits [3]. If we assume that the results of these references are representative of the optimum performance available from the two technologies, then the speed advantage of GaAs is about 2.5 times that of silicon (at least, for circuits of MSI complexity). This advantage is not insignificant, because the performance of complex electronic systems would be more than doubled merely by appropriately incorporating a few GaAs circuits.

One particular arrangement of a GaAs MESFET logic cell, introduced by Van Tuyl and Liechti [1], [2], is shown in Fig. 1. The cell is a static one (low-pass filter type response) and consists of a logic branch and a driver/voltage shifter branch.

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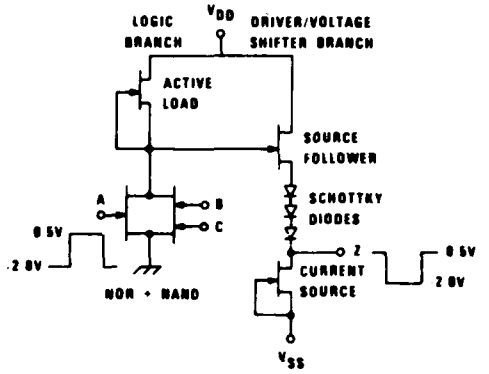

Fig. 1. Static GaAs MESFET logic gate [1], [2].

The latter appropriately adjusts the logic levels at the output node and provides the charge necessary to drive subsequent logic gates. The active load in the logic branch results in a nonlinear load line which provides gain and tends to "digitize" the input signal. The logic function of the gate is determined by the FET arrangement used in the logic branch. For example, if the dual gate FET associated with input gates *B* and *C* is removed, the inverter function results. If gate *C* is removed, the NOR function results; if gate *A* is removed, the NAND function results.

The main disadvantage of the logic gate shown by Fig. 1 is that 75–80 percent of the power dissipation occurs in the driver/voltage shifter branch. A modification to reduce the power dissipation was introduced by Welch and Eden [4] by removing the source-follower. The objective of our work was to determine the relative merits of these approaches and to determine the effect of gatelength and fan-out on circuit speeds. Such a data base, we believe, is necessary for making the tradeoff decisions that are encountered in the design of multigate integrated circuits. We begin this paper with a description of the logic cell configurations used in this work, a discussion of material considerations, a presentation of experimental results, a discussion of the results, and end with a summary of the important conclusions.

II. Logic Cell Configurations

The three logic cell configurations investigated in this work are shown in Fig. 2. The gatewidth of the switch FET, W_s, is 20 μm for all cases. Logic cells (*a*) and (*b*) are two particular embodiments of the cell shown by Fig. 1. They differ from each other only in the widths of some of the FET circuit ele-

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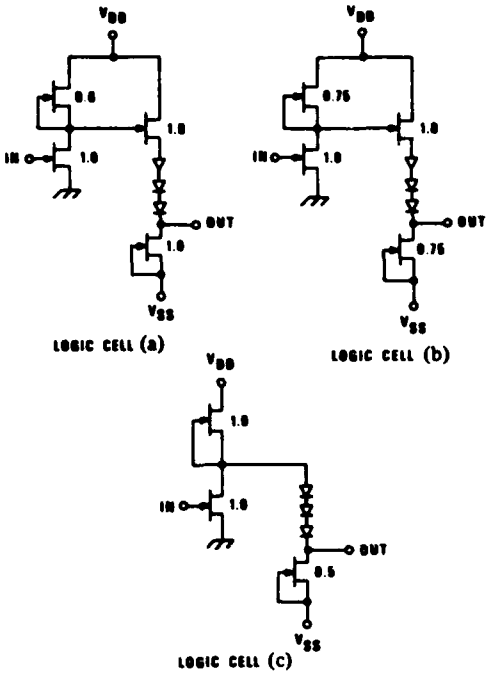

Fig. 2. Inverter logic cell configurations employed in present work. FET widths are shown normalized to $W_s = 20$ μm.

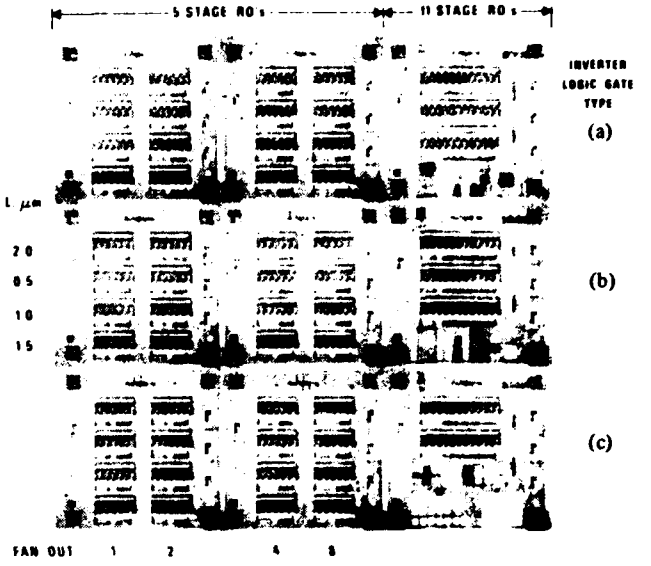

Fig. 3. Arrangement of RO circuits into a 6-mm by 6-mm master field.

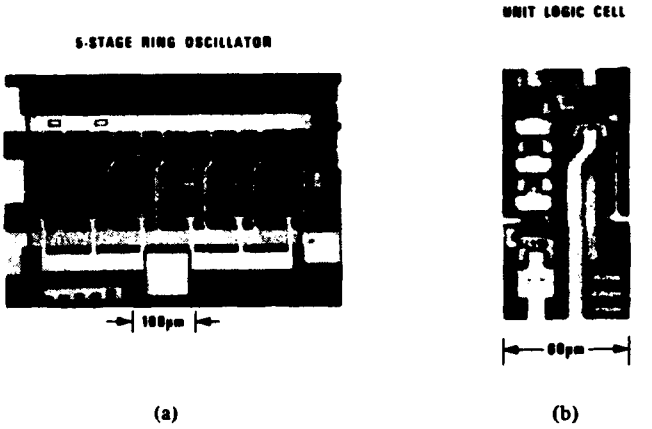

Fig. 4. Layout details of a 5-stage RO and a unit logic cell.

ments. In logic cell (*c*), the source-follower is removed to reduce the power dissipation of the logic cell. The three logic cell configurations of Fig. 2 were arranged in 5- and 11-stage ring oscillator (RO) circuits. These were then fabricated with nominal gatelengths of 0.5, 1.0, 1.5, and 2.0 μm and fan-out loadings of 1, 2, 4, and 8 (consisting of source-gate capacitances). All these test circuits, together with test devices (for material characterization) and test patterns (for process characterization) were incorporated into a 6-mm by 6-mm master field shown by Fig. 3. The 11-stage RO's in the third column were used to verify the propagation delays obtained from the 5-stage RO's. Fig. 4 shows some details of the layout employed. The area of the logic cell is 80 μm X 150 μm. The fan-out loads consisting of the source-gate capacitances can be seen in the lower portion of Fig. 4(b).

Slices with a minimum size of 28 X 28 mm were used in this work so as to fabricate a 4 X 4 array of the master field. This permits a meaningful statistical analysis to be carried out for each circuit type when yields are ~50 percent. The main features of the fabrication sequence include B^+ implantation for device isolation, AuGe based alloyed ohmic contacts, direct slice writing by e-beam of the gate level, and the use of polyimide for the dielectric standoff. A gate recess of 50–100 nm is employed to promote adhesion and to attain the desired value of the pinchoff voltage. All metallization patterns are obtained by using liftoff techniques.

III. Material Considerations

Table I shows results of saturation current measurements on a number of slices taken from two different ingots. The measurements were made on unrecessed 100-μm-wide gateless FET's. The slices were identically implanted with Si^+ at 3.9 and 1.1 X 10^{12} cm^{-2} at 180 and 50 keV, respectively. The slices were then proximity annealed at 850°C for 30 min [5]. The first group are ⟨100⟩ grown and oriented, undoped (not intentionally doped) substrates grown by the liquid encapsulated Czochralski (LEC) process. The LEC material was pulled at TI from a precompounded GaAs charge under a pressure of approximately 2 atm. The second group of ⟨100⟩ oriented substrates are from a commercially supplied Cr-doped ingot grown by the horizontal Bridgman technique. The Cr content of Bridgman grown crystals used in this laboratory has been determined by SIMS to be about 3 X 10^{16} cm^{-3} for the seed end slices [6] and increases down the crystal due to macroscopic segregation during bulk growth [5]. The Cr concentrations in the TI LEC were measured by SIMS to be at or below the 2 X 10^{15} cm^{-3} instrument background level [6]. The long range standard deviation-to-mean ($\sigma/\bar{I}$) ratio refers to uniformity over 24 X 24-mm regions. The medium range $\sigma/\bar{I}$ ratio refers to uniformity over 6 X 6-mm regions. The activation efficiency from *C-V* measurements is not available for the Cr-doped group as these slices were processed before an additional step was incorporated into the fabrication procedure (which includes test devices on the unetched GaAs surface). However,

TABLE I
UNIFORMITY AND REPRODUCIBILITY CHARACTERISTICS OF UNDOPED, LOW-PRESSURE, LEC AND CR-DOPED BRIDGMAN SUBSTRATES

	Lot No.	R_{sq} (Ω/sq)	Long Range T_{sat} (mA)	Long Range $\sigma/\bar{T}$ (%)	Medium Range $\sigma/\bar{T}$ (%)	Activation Efficiency (%)	Average Mobility ($cm^2\ V^{-1}\ s^{-1}$)
LEC	C15(71)	607	50.3	4.7	2.2	~64	4100
	C15(72)	568	49.3	8.4	5.3	~65	4300
	C23	547	52.7	3.6	3.5	72	4070
	C24	510	52.7	6.6	4.8	74	4100
	C25	617	50.3	4.8	2.8	72	4030
	C26	595	46.5	10.7	10.2	70	4160
Bridgman	C8(2)	753	42.2	6.0	3.0		4410
	C8(32)	547	51.0	6.5	-		
	C8(49)	527	51.4	5.8	-		
	C17(4)	670	45.4	7.1	5.3		
	C17(5)	606	50.0	7.9	8.5		

the comparable $\bar{I}_{sat}$ values suggest that the activation efficiencies of the two groups are about the same. The average mobility measured by the fat-FET method are shown in Table I for the LEC material. Although the mobilities of the unetched active layer could not be measured for the Cr-doped group, slices from other Cr-doped ingots exhibit mobilities comparable to those shown by the first group.

The data show that in terms of uniformity and reproducibility both substrate types are equivalent. The only difference observed between the substrate types is that the profile of Cr-doped substrates have a sharper transition (~600 Å/decade) than those of undoped substrates (~1000 Å/decade). This difference is not significant in circuit processing nor is it reflected in the statistical data of any important electrical parameter of the circuits or test devices. Since it will be shown that circuits fabricated on the two substrate types have equal propagation delays, we conclude that both substrates types are useful for logic applications.

The results shown in Table I are for substrates from "qualified" ingots. Material is qualified by first ion implanting/proximity annealing test substrates from along an ingot. The test substrates are then evaluated by *C-V* and ungated source/drain current measurements. Acceptable material has long range uniformity better than 10 percent and is characterized by approximately Gaussian profiles and high activation efficiencies (greater than 65 percent for Si^+ implantation at these dose levels as determined by integrating carrier concentration density profiles). From the small data base presently available, the yield of both the Cr-doped ingots and undoped LEC ingots is about the same. Future improvements in ingot reproducibility for both types can be reasonably expected. On the other hand, circular slices with a flat would be useful for further standardization of processing procedures. As LEC ingots can be grown in the ⟨100⟩ direction with good diameter control (whereas HB ingots are best grown in the ⟨111⟩ direction and when wafered along the ⟨100⟩ direction give rise to their irregular "D" shape), the circular substrate feature can be best satisfied by the LEC growth technique.

It is worth noting that we have investigated the use of commercially available undoped ⟨100⟩ oriented slices grown by the LEC method from a charge compounded *in situ* at high pressure. For the few slices processed, results were comparable to those shown in Table I. Profile abruptness for the commercially supplied undoped LEC substrates with *in situ* compounding is comparable to the TI LEC (~1000 Å/decade). Additionally, a few slices of ⟨111⟩ Cr-doped Bridgman (commercially supplied) and ⟨111⟩ LEC (grown at TI) were processed. Results were only slightly inferior (long range $\sigma/\bar{I}$ typically about 10 percent for qualified ingots) to those shown in Table I, suggesting that such substrates are also useful for circuit processing. The use of ⟨111⟩ oriented substrates was investigated to determine if slice breakage during processing is reduced. In that respect, it appears to offer only a slight advantage.

IV. EXPERIMENTAL RESULTS

The transfer characteristics of a unit logic cell is shown in Fig. 5(a). The gain, defined by the output to input voltage rate of change ratio, is typically about 8, 5.5, and 4 for logic cells (*a*), (*b*), and (*c*), respectively, for circuits with a pinchoff of −2.5 V. When cooled to 77 K, the output logic levels change slightly and are typically recovered by bias adjustment of about +12 percent on V_{DD}; Fig. 5(b) and (c). For logic cells on this slice, the power dissipation increased by ~90 percent at 77 K compared to that at 300 K (primarily due to the dependence of I_{DSS} and $I_{DS\,max}$ on temperature). The maximum frequency of operation of such a logic cell can be defined as that frequency at which the average gain during transition is unity. Fig. 6 shows the response of logic cell (*b*) to sinusoidal excitation at different frequencies. In Fig. 6(a)–(c), only the gates offset is varied and the output response changes as would be expected. Knowing the input signal amplitude, the gain is calculated and is also shown in Fig. 6. The gain is seen to decrease with frequency until at 4.0 GHz, the gain is near unity. Upon cooling the logic cell to 77 K, the gain increases to ~2.2 which suggests a maximum frequency of operation near 8 GHz. Unfortunately, the accuracy of data obtained from unit logic

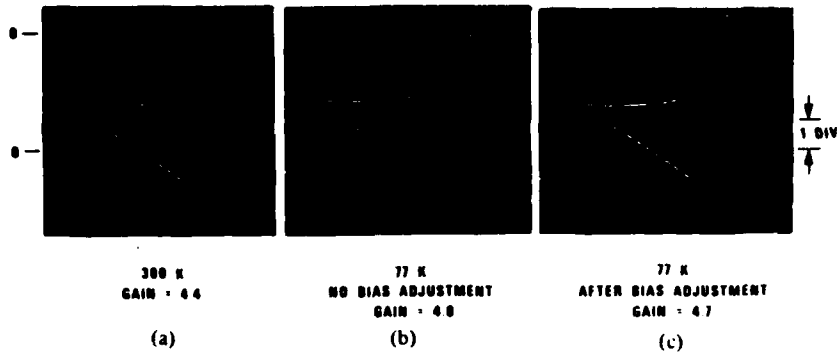

Fig. 5. Transfer characteristics of logic cell (*b*) at 300 and 77 K. Input- lower trace; output- upper trace. Vertical: 1.0 V/div; horizontal: 0.2 ms/div (all traces).

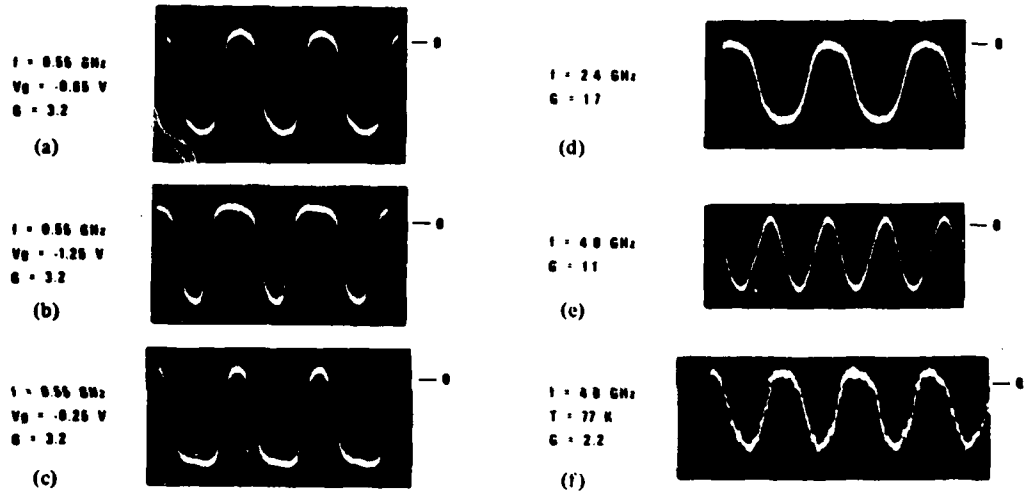

Fig. 6. Logic cell (*b*) response to sinusoidal excitation; $L = 1$ μm. $T = 300$ K except for (f). Vertical: 1 V/div (all traces); horizontal: (a)-(c) 500 ps/div and (d)-(f) 100 ps/div.

cells is not within the ±10 percent necessary for determining optimum logic cell design. For that purpose, RO circuits will be shown to be satisfactory.

Fig. 7 shows idealized waveforms for RO circuits. In Fig. 7(a), the propagation delay is due to signal path delay and the logic cells are assumed to have infinitesimal rise and fall times. For this case, the propagation delay per stage is given by

$$t_{pd} = \frac{1}{2nf}. \tag{1}$$

In Fig. 7(b), the signal path delay is assumed to be infinitesimal and the rise and fall times are assumed to be finite. The situation depicted is that the gain is unity throughout the transition and that the succeeding stage begins to respond when the prior stage is at midpoint (point P) in its transition. For this case, the propagation delay per stage is again found to be given by (1). More importantly, we can determine from this idealized construction the dwell time that the waveform is in the saturated logic levels. This is readily determined to be

$$\frac{t_{dw}}{T} = \frac{n-2}{n} \tag{2}$$

which suggests 60- and 82-percent dwell times for 5- and 11-stage RO's, respectively. Fig. 8 shows RO waveforms for 5-stage RO's with dwell times of ~40 percent (11-stage RO's typically exhibit dwell times of ~65 percent). The reasonable correlation between expectation and measurement lends confidence in the validity of the results that follow.

The waveforms shown by Fig. 8 were obtained under optimum bias conditions in order for a symmetrical waveform to result. Under other bias conditions, the waveform would be expected to be nonsymmetrical because the succeeding stage begins to respond at a point other than P. However, the fundamental frequency of the RO is expected to remain unchanged by such bias changes. These expectations are also confirmed by experimental observation.

The RO's were evaluated on-slice using a "conventional" probe station. Since each RO has one buffer stage, the bias supply currents are approximately constant. Here, micromanipulator probes with an RF choke (located about 6 cm from the circuit) were used to provide bias. To observe the RO waveform, a suitable high-speed probe was made. This probe consists of a high-frequency head affixed to a standard probe base. The head consists of a 2-mm BeCu probe tip at-

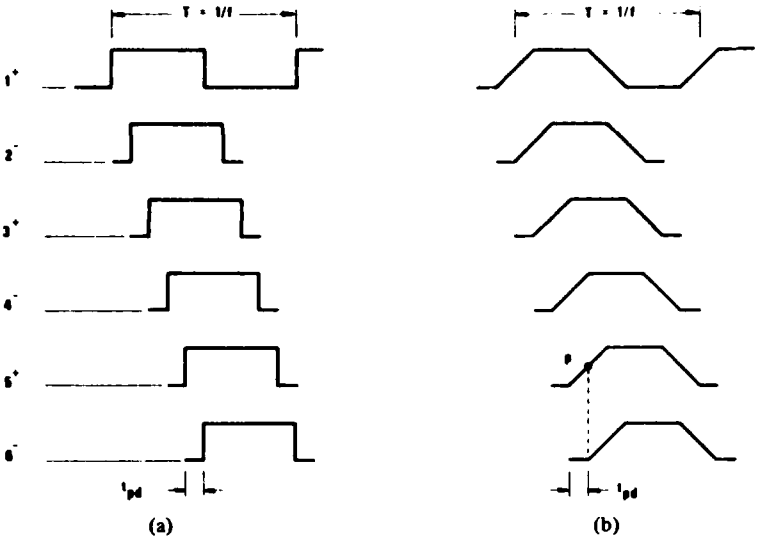

Fig. 7. Idealized RO waveforms.

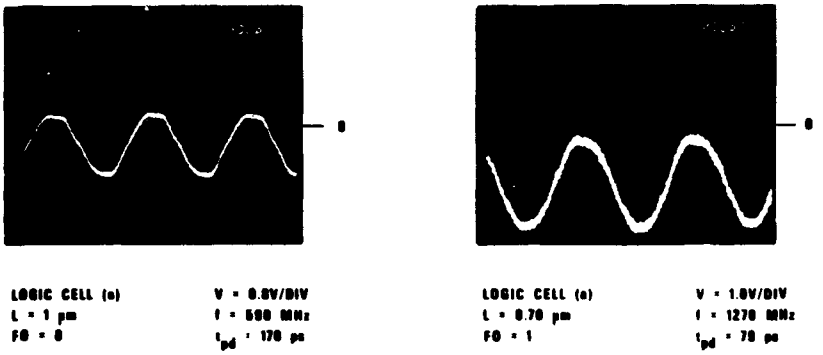

Fig. 8. 5-stage RO waveforms: lot C23.

tached directly to a short section of a 50-Ω MIC transmission line, a 2-kΩ chip resistor, and another 50-Ω line connected to the center conductor of a 50-Ω coaxial connector. Attenuation of the output waveform is necessary to avoid excessive loading of the output buffer stage. The probe in combination with a sampling scope system was then characterized over the 0.01- to 4-GHz frequency range to determine vertical sensitivity. RO circuits which did not exhibit the correct output levels were considered defective and excluded from the data base. For convenience, the frequency of good circuits was determined with the use of a spectrum analyzer. This datum together with those pertaining to power dissipation were recorded.

Measurements were made under ambient room light and temperature conditions. The supply bias voltages were standardized to +6.0 V and -4.0 V for V_{DD} and V_{SS}, respectively. These bias voltages are about 30 percent larger than the optimum required by most circuits. However, since some circuits require higher bias voltages and because many measurements are necessary, these values were selected so that the vast majority of functional circuits would operate between the correct logic levels. Accordingly, the power dissipation results presented later are ~30 percent larger than those obtained under optimum bias conditions. The higher bias voltages also causes the operating temperature of the circuits to be higher than that under optimum bias voltages. Accordingly, the propagation delays to be presented are ~5 percent larger than those that would be obtained under optimum bias conditions.

Table II shows part of the data summary for a typical slice. At top is shown the mean values of some of the more important electrical parameters together with the standard deviation to mean ratio. The sample size of 48 was taken over equally spaced intervals over the 24 X 24-mm region. Here, we have defined the pinchoff voltage V_p as that gate voltage at which I_{DS} is equal to 0.1 I_{DSS}. $I_{DS\,max}$ is the source-drain current at a forward gate bias of 0.7 V. The transconductance is measured between gate voltages of 0.7 and 0 V. These extrinsic measurements are primarily used to monitor the uniformity and reproducibility of the overall process. The mean value of the power dissipation of each logic gate configuration is shown next. The power dissipation of logic cell (*c*) is seen to be 55 percent that of logic cell (*a*). (Under optimum bias conditions, the power dissipation of logic cell (*c*) scales to 3.46 mW for $V_p = -1.0$ V; $P_d \propto |V_p|^2$. The agreement with a previously reported result of 2.26 mW [4], is satisfactory especially considering that the pull-down transistor width of [4] is smaller than that of logic cell (*c*).) In the yield column, all the various gate lengths are combined. This is because, for our process, yield is independent of gatelength for $L \geq 0.7$ μm. Additionally, yield was independent of fan-out for these circuits. At the bottom of Table II, the propagation delays of the shortest

TABLE II
DATA SUMMARY OF A TYPICAL SLICE [C8(32)]

$\langle V_p \rangle$ = 2.50 V	$\langle I_{DS\ max} \rangle$ = 293 mA/mm	$\langle I_{DSS} \rangle$ = 211 mA/mm	$\langle g_m \rangle$ = 117 mS/mm
$\sigma/\langle V_p \rangle$ = 7.3%	$\sigma/\langle I_{DS\ max} \rangle$ = 6.5%	$\sigma/\langle I_{DSS} \rangle$ = 8.9%	$\sigma/\langle g_m \rangle$ = 4.4%

Logic Cell Configuration	$\langle P_d \rangle$ (mW)	$\sigma/\langle P_d \rangle$ (%)	Total Yield (%)
a	51.0	8.2	52
b	44.9	10.1	49
c	28.1	11.2	48

$\langle t_{pd} \rangle$ IN ps OF 5-STAGE (11-STAGE) RING OSCILLATORS
Nominal Gate Length = 0.5 μm (Actual = 0.75 ± 0.05 μm)

	Fan-Out 1	2	4	8	Yield (%)
a	82.6 (81.1)	101.7	123.7	180.8	59 (56)
b	87.0 (88.7)	109.8	141.7	218.7	42 (50)
c	99.0 (102.0)	134.2	178.9	290.5	48 (50)

TABLE III
COMPARISON OF PROPAGATION DELAYS FOR LOGIC CELLS (*a*) AND (*c*) FROM A TYPICAL SLICE [C8(32)]

$\langle t_{pd} \rangle$ IN ps OF 5-STAGE RING OSCILLATORS

Nominal (Actual) Gate Length (μm)	Logic Cell Configuration	Fan-Out 1	2	4	8
0.5	a	82.6	102	124	181
(0.75 ± 0.05)	c	99.0	134	179	291
		(20)	(32)	(45)	(61)
1.0	a	92.0	109	148	221
(1.10 ± 0.10)	c	109	152	209	360
		(18)	(40)	(41)	(63)
1.5	a	108	133	180	295
(1.60 ± 0.10)	c	135	175	268	468
		(25)	(31)	(49)	(59)
2.0	a	119	153	220	332
(2.10 ± 0.10)	c	151	219	327	566
		(27)	(43)	(49)	(70)

NOTE: Number in parenthesis is the speed advantage of circuit (a) over circuit (c) in percent.

gatelength circuits are shown. Since yields of functional RO's are ~50 percent, the propagation delay associated with each RO type is on average the mean value of results obtained from eight functional circuits. The $\sigma/\langle t_{pd} \rangle$ ratio is typically about 7 percent. Note that the propagation delays obtained from the 5- and 11-stage RO's are in reasonable agreement.

Table III shows the results for all gatelength circuits for logic cells (*a*) and (*c*). By noting that the power dissipation of logic cell (*c*) is 55 percent that of logic cell (*a*), the speed-power product of the former is seen to be more favorable for all cases investigated. On the other hand the speed advantage of logic cell (*a*) over logic cell (*c*) is about 35 percent for FO = 2. This advantage increases with fan-out. The data also show that gate stripe capacitances are not dominant in determining circuit speed when FO $\leq$ 2. Rather, parasitic capacitances clearly predominate.

TABLE IV
SLICE-TO-SLICE COMPARISON OF THE AVERAGE PROPAGATION DELAY

Logic Cell: a L = 1.0 μm Fan-Out = 2

Lot	Measured L (μm)	$\langle t_{pd} \rangle$ (ps)	<100> Substrate Type	Implant Specie
C5(60)	1.10 ± 0.10	113	Cr Doped: M-5-45	Se
C8(32)	1.10 ± 0.10	109	Cr Doped: M-5-53	Si
C8(49)	1.40 ± 0.15	124	Cr Doped: M-5-53	Si
C23	1.05 ± 0.10	108	Undoped: T1-1	Si

Table IV shows slice-to-slice comparison for a particular circuit type. Similar agreement also was exhibited by the other circuit types. The data indicate that substrate type or implant specie does not significantly affect circuit speed. Additionally, it is noted that lot C5(60) was selectively implanted; no significant advantage or disadvantage results.

V. DISCUSSION

The propagation delay for logic gate (*a*), $L = 1$ μm, and FO = 2 can be compared to those obtained by other investigators who have also fabricated −2.5-V pinchoff circuits. Although not all circuit element widths are specified by these prior investigators, the 109-ps propagation delay shown in Table III compares well with the 111- and 95-ps propagation delays of [2] and [7], respectively, for 20-μm wide logic gates. This satisfactory agreement lends further confidence to the validity of the propagation delay matrix presented in this paper.

Assuming that the logic gates have a parasitic capacitance due to fringing fields approximately equal to the width of an 8-μm device [2], an assumption experimentally confirmed at our laboratory with the use of another mask set, then the propagation delays presented earlier can be reduced by 20 percent for $W_s = 50$ μm (experimentally verified) and by about 30 percent for $W_s = 100$ μm. The penalty for this potential speed improvement is, of course, a 2.5- and 5-fold increase in power dissipation. Alternately, the circuit speed would be expected to increase linearly with device transconductance. This can be achieved technologically by reducing source/gate spacing, deep recessing of the gate, or with the use of self-aligned gates. (The efficacy of the last approach was demonstrated by [7].) The use of such techniques, however, may adversely impact yield.

A simple and preliminary model of the propagation delay has been constructed. Results for such modeling activities are presented in Fig. 9 with experimental data points superimposed. The model is based on the assumption that the cell response time is related to the response time of the various circuit nodes by the root mean square method. Initial values of the circuit node response times are extracted from the experimental data for logic cell (*a*); these were then adjusted slightly to minimize the error matrix between calculated and measured values for logic cell (*a*). The model is then applied without modification to logic cells (*b*) and (*c*) where only device widths are changed. Satisfactory agreement between the experimental and calculated results are obtained. Also shown in Fig. 9 are the asymptotic values of the propagation delay as the gate length approaches zero.

The main advantage of such a simple model is that useful insight is rapidly gained without great effort and computer time expenditures. Its main deficiency is that little insight is gained into the sources of the parasitic capacitances. For that purpose, a more complex model, with node capacitances computed from cell layout, is used. Propagation delays, as computed by using SPICE 2, are in good agreement with measurements for all circuit types. A more complete description of this activity will be presented at a later date.

Four important results emerge from the modeling work. First, the reduction in the propagation delay as the gatelength is reduced below 1 μm is comparatively small. For example, reducing the gatelength (logic cell (*a*), FO = 1, from 1.0 to 0.5 μm results in an increase in circuit speed of 19 percent. Second, it is unlikely that the propagation delays will be significantly reduced (>25 percent) solely by modification of the cell layout. This is because a) fringing field effects are believed to already contribute significantly to the node capacitances, b) the contribution of top side interelectrode capacitances is a substantial fraction of the total node parasitic, and c) the circuit nodes are close to the minimum geometry consistent with present processing technology. Third, for logic cell (*a*), $L = 1$ μm, and FO = 2, the circuit speed is expected to improve by about 10 percent by employing a selective n^+ implant while simultaneously reducing the geometry of the voltage shifter diodes [4]. Finally, for FO ≤ 2, the response time of the logic branch circuit node for logic cell (*a*) is somewhat larger than that of the other circuit nodes. A 20-percent increase in the width of the devices in that branch would result in more evenly balanced node response times, and the propagation delay would be expected to be reduced by ~5 percent. For FO > 2, the response time of the output node begins to dominate so that increasing the width of the devices in that branch, as fan-out increases, would be indicated.

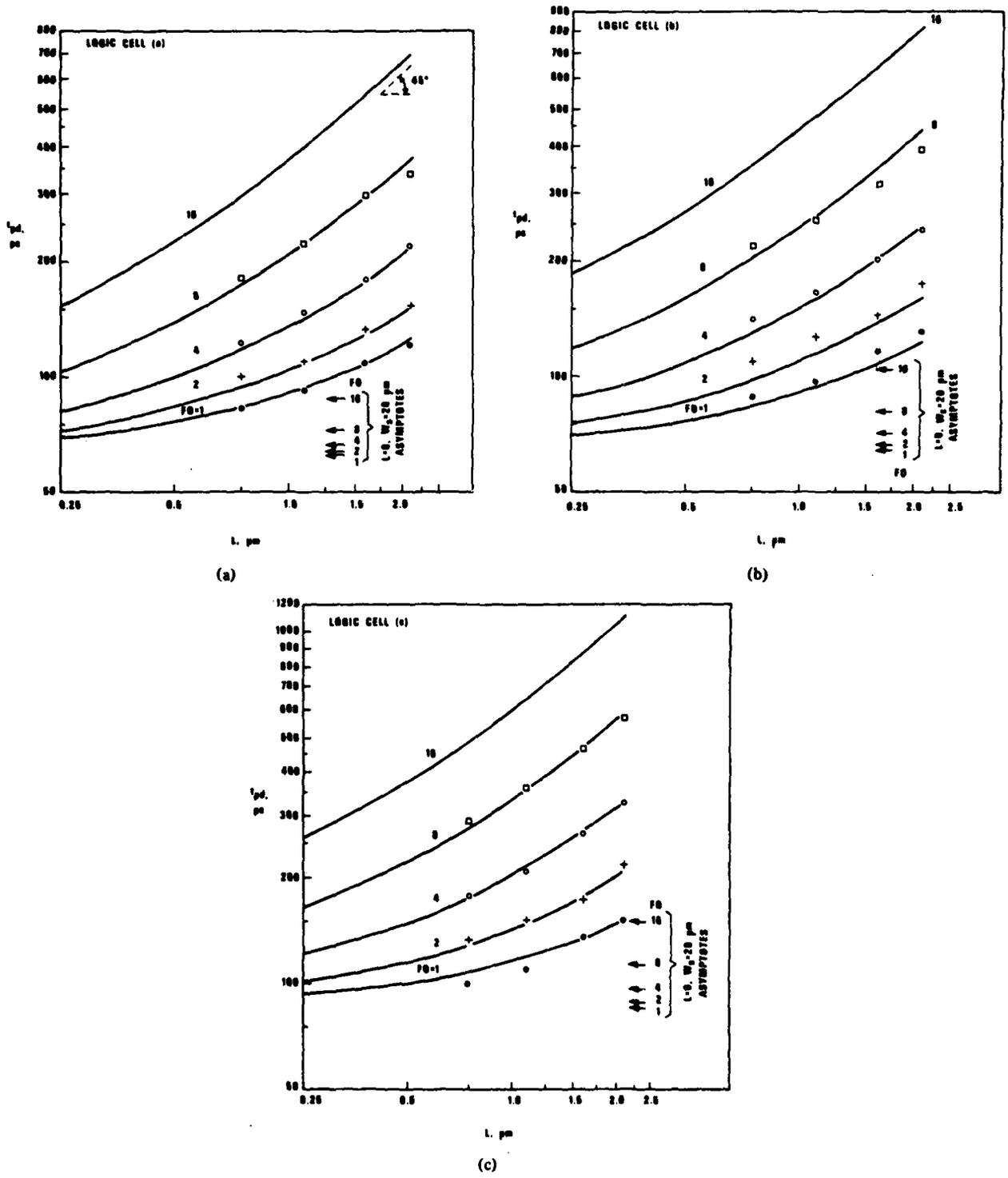

Fig. 9. Projection of propagation delays by modeling the experimental data for logic cells (*a*), (*b*), and (*c*). $V_p = -2.5$ V.

VI. Conclusions

For the −2.5-V pinchoff circuits investigated in this work, the more important conclusions can be summarized as follows:

a) With proper starting materials, the standard deviation-to-mean ratio of all important electrical parameters is typically <10 percent over 24 × 24-mm regions.

b) The power dissipation of logic cell (*c*) is 55 percent that of logic cell (*a*).

c) The speed-power product of logic cell (*c*) is more favorable than that of logic cell (*a*) for all cases investigated experimentally.

d) The speed advantage of logic cell (*a*) over that of logic cell (*c*) is about 35 percent for fan-out of two. This advantage increases with fan-out.

e) For a fan-out of two, the speed advantage of 0.5-μm gatelength circuits over 1.0-μm gatelength circuits is about 20 percent. Alternately stated, the contribution of the gate stripes to the node capacitances is small compared to contributions from other sources.

Acknowledgment

The authors thank W. W. Dunn and J. L. Brown for technical assistance in circuit fabrication, T. B. Brandon for technical assistance in materials preparation, W. A. White for assistance in electrical measurements, J. B. Sherer for supplying the TI LEC material and Dr. D. B. MacDonald for assistance in e-beam lithography. The use of a circuit layout program by Dr. K. S. Tan is also acknowledged.

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APPENDIX B

GaAs E/D LOGIC CIRCUITS

SESSION III: GaAs HIGH SPEED DIGITAL ICs

Chairman: *Larry J. Nevin*
Hewlett-Packard Co.
San Jose, CA

WAM 3.1: GaAs E/D Logic Circuits*

Mooshi R. Namordi, William A. White
Texas Instruments, Inc.
Dallas, TX

THE PARTICULAR EMBODIMENT used in this study of a GaAs enhancement/depletion (E/D) logic gate consisted of a 25μ wide enhancement mode FET switch and a 7μ wide depletion mode active load FET. The gate stripes of these two FETs were defined separately. A sintered Pt metalization[1] was used for the gate of the switch FET to permit adjustment of the pinch-off voltage. Silicon implantation was used to prepare the active layer. Slice size and fabrication process were similar to those previously reported[2].

The gate was then used to fabricate various circuits which were incorporated into a 6mm X 6mm master field. To study the effect of gate length and fan-out on the propagation delay, ring oscillator circuits were fabricated with nominal gate lengths of 1.0μ and 1.5μ and fan-out loadings of 1, 2, and 4. Other circuits included: 1, 2, 3, 4, and 5-stage prescalers, 5-stage shift registers, and exclusive-OR: Figure 1. Various test devices and test patterns were incorporated into the master field for device and material characterization.

Table 1 shows the propagation delays obtained at 300°K. Since yields of functional ring oscillators (ROs) were ~50%, the propagation delay associated with each RO type is, on average, the mean value of results obtained from eight functional circuits. The tight spread in t_{pd} suggests good device uniformity across the 24 X 24mm slice. Table 1 shows a fan-out sensitivity of about 35 and 45ps for L = 1.13 and 1.45μ respectively. The ROs operated at the correct logic levels, as evidenced by Figure 2, which shows logic levels at 1.0 and 0.4V. The propagation delays were insensitive to $V_{DD} \geq 1.2V$. The power dissipation per gate was typically ~0.55mW at V_{DD} = 1.2V. The test FETs of slice E1-2 exhibited a large signal transconductance of 82mS/mm and a small signal transconductance of ~130mS/mm. The impressive results of Table 1 reflect this parameter.

Extensive low temperature (77°K) evaluation of the slice was then undertaken. The transconductance of the test FETs was measured to be, on average, 23% greater at 77°K than that measured at 300°K. The speed of the ROs at 77°K was 1.27 times (σ = 0.04) that at 300°K. Accordingly, for L = 1.13 and 1.45μ, propagation delays of 38 and 48ps with fan-out sensitivity of about 28ps and 35ps were obtained at 77°K. By operating prescalers at 300° and 77°K base plate temperatures, it was observed that the upper logic level was increased by 150mV, while the lower logic level decreased by 60mV at 77°K compared to those obtained at 300°K. These observations indicate that noise margins are somewhat improved during operation at 77°K.

Figure 3 shows the proper functional operation of the exclusive-OR circuit. The upper and lower logic states are at 960mV and 400mV, respectively. Figure 3*b* indicates a gain of about 8 and enables us to estimate a lower bound of 0.2GHz for this circuit's speed capability.

Figure 4 shows the response of 5-stage prescaler to a 0.9GHz sine wave input. The circuit had a total power dissipation of 15.2mW. Proper operation at higher frequencies could not be obtained for these on-slice measurements because of RF signals on the bus lines. However, based on the RO data presented earlier, the speed capability of this circuit is expected to be about 1.8GHz when MIC mounted.

The shift register circuits were clocked with a high frequency sinusoid of about 1V peak-to-peak amplitude: Figure 5. Here, the oscilloscope is synchronized to the data and the $\overline{Q}$ output of the first stage, $\overline{Q(1)}$, is referenced to a vertical reticle. Because the clock is asynchronous to the data, a time uncertainty of $\pm T/2$ in the delay is expected. The delay is seen to be correct within this uncertainty. Clocking at still higher frequencies could not be done because of RF signals on the bus lines. However, the previously presented RO data would indicate that clocking to 3.1GHz should be possible.

Acknowledgments

The authors thank W.W. Dunn and J.L. Brown for technical assistance in circuit fabrication and W.M. Duncan for supplying the ion-implanted material.

Slice: E1-2	RO Length: 19-Stages		T = 300°K
Gate Length	*Fan-Out*	t_{pd} *(ps)*	σ / μ *(%)*
1.13μ	1	48.2	3.9
	2	83.5	1.6
	4	152	3.3
1.45μ	1	61.3	6.2
	2	107	2.3
	4	204	4.9

TABLE 1—Propagation delays of enhancement mode logic gates.

*Project supported by the Air Force Wright Avionics Laboratory under contract F33615-80-C-1171.

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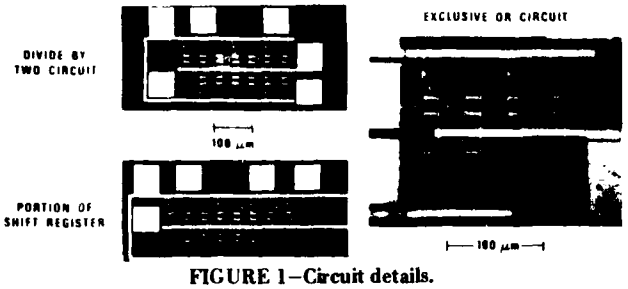
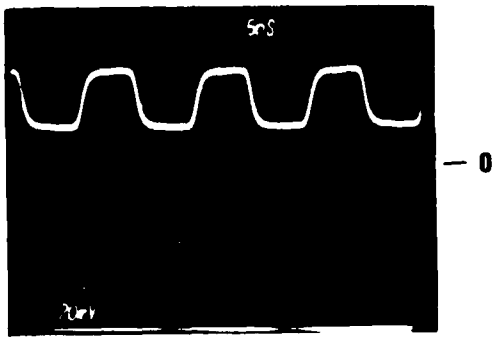
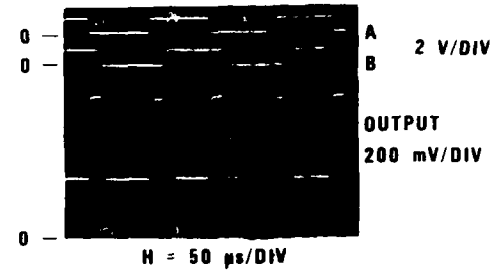


FIGURE 1–Circuit details.

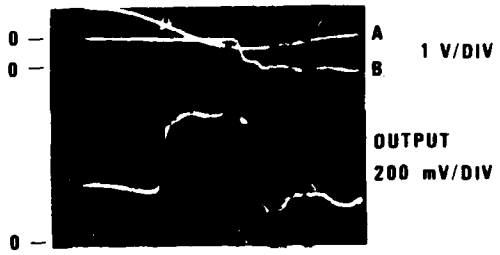


H = 5 ns/DIV V = 400 mV/DIV

FIGURE 2–Ring oscillator waveform: slice E1-2. RO-length = 73-stages, L = 1.45μ, FO = 2, V_{DD} = 1.2V, I_{DD} = 36mA, P_d = 0.58mW/gate, oscilloscope BW = 300MHz.



(a)



(b)

FIGURE 3–Functionality test of XOR circuit.

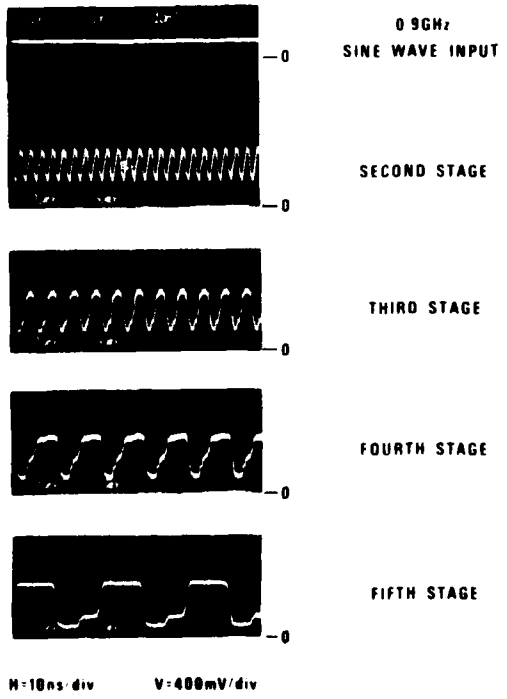


FIGURE 4–Response of a divide-by-32 circuit to a 0.9GHz sine wave input. Measurement was made on-slice.

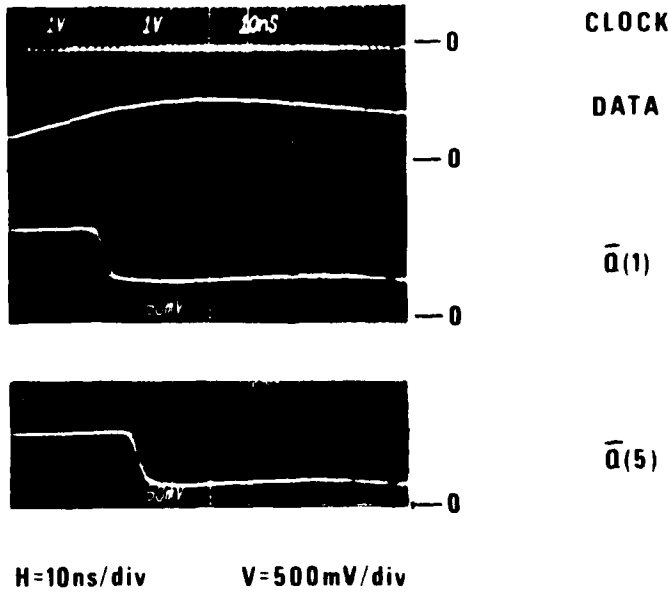


FIGURE 5–Response of a 5b shift register to a 500MHz sine wave clock. Measurement was made on-slice.

APPENDIX C

RELIABILITY OF GaAs MESFET LOGIC CIRCUITS

RELIABILITY OF GaAs MESFET LOGIC CIRCUITS

by

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ABSTRACT

Twelve depletion mode GaAs MESFET logic circuits were subjected to a step-stress life test. Each circuit consisted of an 11-stage ring oscillator with one buffer stage. Both BFL and SDFL circuits with $V_p \approx -2.0$ V and -1.0 V were represented. The circuits were operated for 500 hours at each of eight temperature stress steps ranging between 25° and 200°C with 25°C increments. No chip failures occurred upon completion of the life test. Reasonable interpretation of these results suggests that GaAs MESFET logic circuits should be very reliable.

Introduction

In the past several years, GaAs digital integrated circuits have been the subject of intensive investigation at several laboratories worldwide. Because considerable advancements have been made, it can be reasonably expected that GaAs digital integrated circuits will be in the market place in the near future. Accordingly, the reliability aspects of such circuits need to be addressed.

The objective of this study was to determine if any serious reliability deficiencies were present in GaAs MESFET logic circuits. If so, then the study of effective countermeasures to improve the reliability could begin. If no serious reliability deficiencies were present, then our objective was to establish a preliminary reliability baseline for GaAs MESFET logic circuits.

Experimental Procedure

Figure 1 depicts the test setup. Figure 1(a) shows a GaAs MESFET circuit mounted into an MIC arrangement. The circuit is an 11-stage ring oscillator with one buffer stage. The bias lines are shunted with 0.01 μf capacitors and the output line contains a 5 KΩ series resistor. The unit was prepared to withstand baseplate temperatures of about 200°C.

Twelve such units were mounted on a heat sink; Figure 1(b). Heaters attached to the heat sink can produce heat sink temperatures up to 350°C and are driven by a temperature controller. A coolant loop is also provided for rapid cooling of the heat sink. Semirigid coaxial lines are provided to monitor the output of each circuit.

Bias voltages, $V_{DD} = 6$ V and $V_{SS} = -4$ V, are applied through a power distribution system from a regulated power supply; Figure 1(c). Upon failure, the power distribution system protects the circuit from further damage making failure analysis possible. The bias voltages are about 30% greater than that required to provide additional electrical stress.

Finally, a sheet metal enclosure is used for circuit protection and for better heat sink temperature stability; Figure 1(d). Water cooling lines are attached for rapid temperature cycling at the end of each stress step.

The circuits were operated for 500 hours at each of eight temperature stress steps. Heat sink temperatures ranging between 25°C and 200°C with 25°C increments were used. (The heat sink was within ± 3°C of its set point during each stress step.) I_{DD} and I_{SS} data together with output frequency were measured daily. At the end of each stress step, the circuits were recharacterized (including output amplitude) at room temperature.

The circuits under test were obtained from slices processed using a previously described fabrication procedure and mask set[1]. Both BFL and SDFL circuits with $V_p \approx -2.0$ V (3-diode voltage shifter branch) and -1.0 V (2-diode voltage shifter branch) were included. All the circuits were 11-stage ROs with one buffer stage and FO = FI = 1. Nine circuits had a nominal gate length of 0.5 μm and three had a nominal gate length of 1.0 μm.

Experimental Results

Table 1 shows the results for a ring oscillator circuit during the life test. The parameter values shown were measured with the heat sink at room temperature at the completion of each stress step. For this circuit, it is seen that no significant changes in the parameter values have occurred because of the temperature stress steps. Similarly, the changes in the parameter values of the other circuits were also small (< 10%).

By completion of the 175°C temperature stress step, no failures had occurred. Shortly after the start of the 200°C stress step, three units failed. Upon removal and inspection of these units, it was found that all had failed due to Ag solder flow (creep) from one of the terminal posts (to which a flexible wire is attached as shown in Fig. 1(a)) to the circuit chip. Accordingly, these failures can not be judged as chip failures. The remaining units completed this step without any significant changes.

Because of the uncertainty that the units could withstand temperatures above 200°C, the remaining units were subjected to a temperature cycle test illustrated by Figure 2. The circuits were subjected to 132 such cycles without any significant change occurring.

An Interpretation Of The Results

To gain some appreciation of the reliability of complex GaAs MESFET logic circuits, it is useful to interpret the results of this study using some reasonable assumptions. These are:

1) A single logic gate fails at the completion of the 200°C stress step.

2) The failure distribution is log-normal with dispersion, σ.

3) The dominant failure mechanism under normal service is due to a physical process having a reaction rate of the form $R_o \exp(-E_A/kT)$.

4) The channel temperature is 30°C higher than the heat sink temperature.

5) The failure rate versus time plot is given by Figure 21 of Ref. 2.

The first two assumptions result in the plot shown by Figure 3 from which the median life for a heat sink temperature of 200°C is obtained. The parameter values of $\sigma < 2.0$ implies a mature fabrication process. This result, in conjunction with the next two assumptions, is used to generate the Arrhenius plot of Figure 4. The activation energy of 1.6 eV is based on those found for GaAs FETs[3,4] and for GaAs IMPATTs[5-7]. The activation energy of 1.2 eV (dashed line) is based on the worst case estimate of Ref. 3. It is seen that a median life of $> 10^{10}$ hours is projected for a heat sink temperature of < 50°C.

Consider now the probability of failure of a 10^3-gate circuit in a service life of 10^5 hours. Using the last assumption and $\sigma = 2.0$, the probability of failure of such a circuit is $< 2 \times 10^{-4}$ for a heat sink temperature of 50°C and $E_A = 1.2$ eV. It is worth mentioning that for smaller σ's, the probability of failure is smaller still.

Summary And Conclusions

This work can be summarized by the following three statements:

- No chip failures have occurred after eight 500-hour stress steps with heat sink temperatures up to 200°C.
- No chip failures have occurred after 132 temperature cycles between 40 and 200°C.
- Parameter changes of the circuits due to the temperature stress steps were typically small (< 10%).

The more important conclusions are:

- No serious reliability deficiencies exist for properly fabricated GaAs MESFET logic circuits.
- The data suggests that the reliability of GaAs LSI logic circuits can be expected to be very high.

Acknowledgment

The authors thank W.W. Dunn for technical assistance in circuit fabrication and B.P. Church for assistance with the life test.

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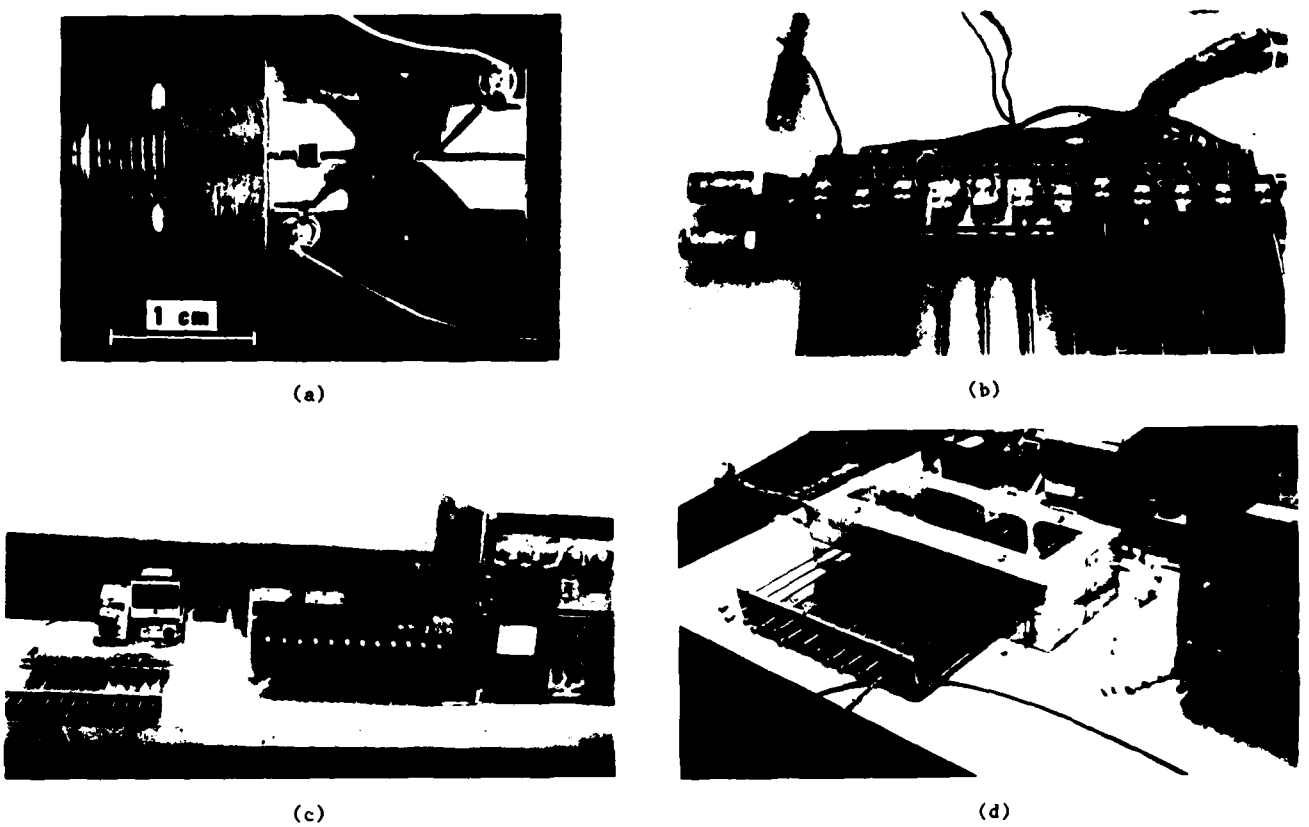

Figure 1. Life Test Setup

TABLE 1. CHARACTERISTICS OF A TYPICAL RING OSCILLATOR CIRCUIT DURING LIFE TEST

CELL TYPE: BFL (A)
GATE LENGTH: 0.5 μM
FO = FI = 1
RO LENGTH: 11-STAGES

SLICE: C49
<Vp>: -1.91 V
CIRCUIT NO: 7

AFTER COMPLETION OF STRESS STEP	I_{DD} (MA)	I_{SS} (MA)	F (MHz)	OUTPUT AMPLITUDE (dB)
START	47	32	415	-
25°C	46	32	415	-30
50°C	47	32	415	-29
75°C	47	33	430	-28
100°C	48	33	435	-28
125°C	49	33	440	-29
150°C	48	33	440	-30
175°C	48	33	410	-29
200°C	48	33	400	-30
CYCLING	48	33	410	-

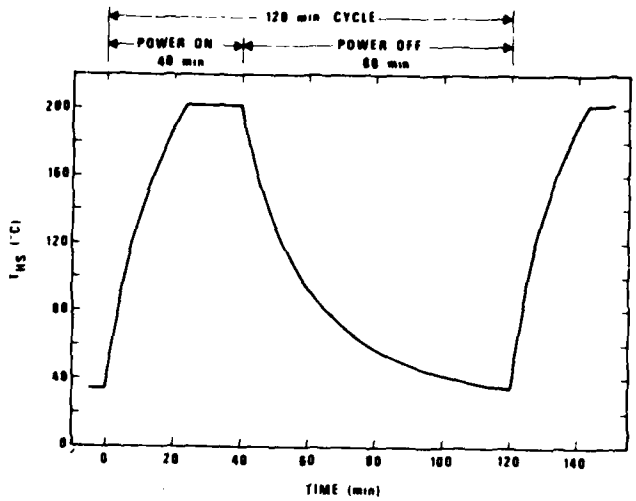

Figure 2. Heat Sink Temperature During Cycle Test

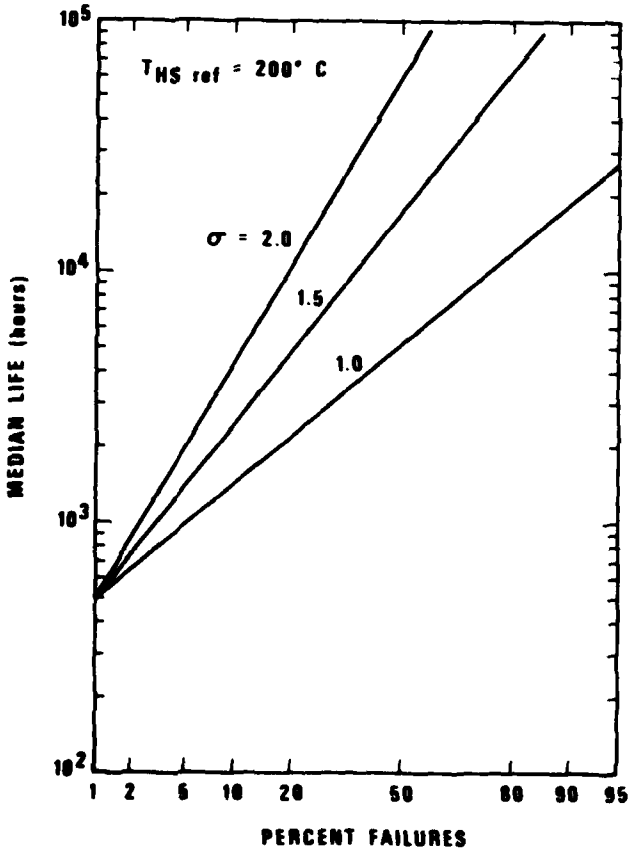

Figure 3. Median Life of a Single GaAs MESFET Logic Gate at a Heat Sink Temperature of 200°C. A single gate is assumed to have failed after 500 hours of operation.

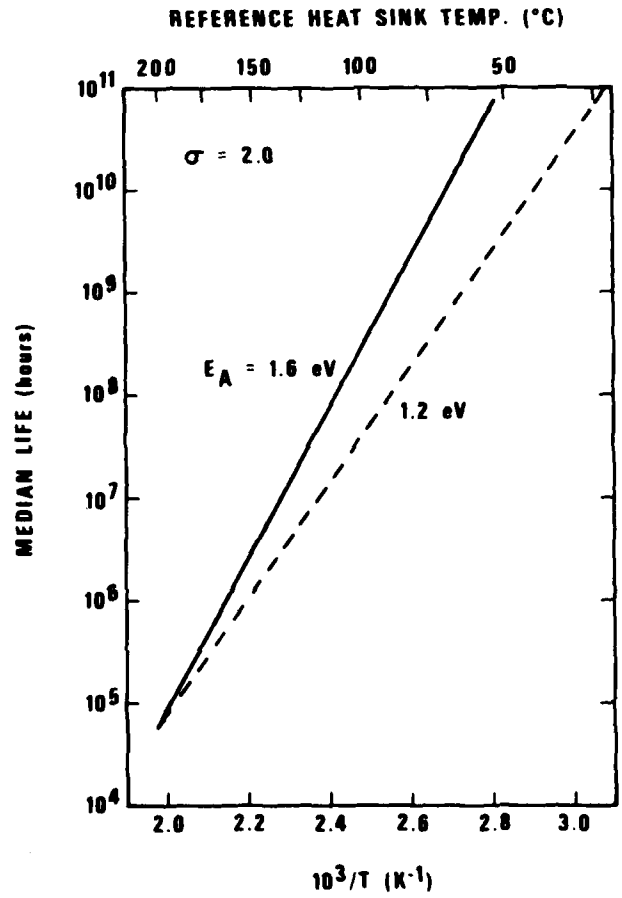

Figure 4. Arrhenius Plot for a Single GaAs MESFET Logic Gate

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