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AFWAL-TR-83-2046

PULSE WIDTH MODULATED DC LINK CONVERTER DEVELOPMENT
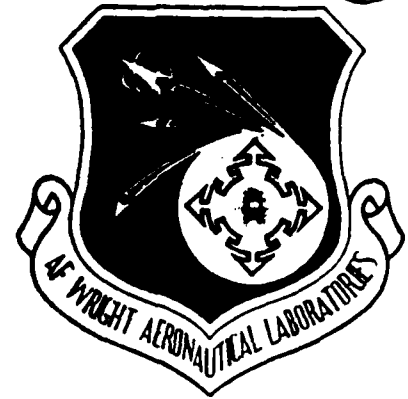
GENERAL ELECTRIC COMPANY
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FINAL REPORT FOR PERIOD SEPTEMBER 1981 — SEPTEMBER 1982

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Wm. U. Berger
Acting Technical Area Manager
Power Systems Branch

Major David Schorr
Chief
Power Systems Branch

FOR THE COMMANDER

James D. Reams
Chief, Aerospace Power Division
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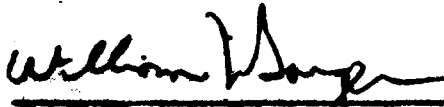| REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
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DC Link
VSCF (Variable Speed Constant Frequency)

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

Further development of power transistor and power Darlington current carrying and voltage blocking capabilities led to the application of new General Electric devices in a 40 KVA Pulse Width Modulated DC Link VSCF system.

The results indicate that the power Darlington devices selected exhibit large losses at the switching frequencies studied. Because of these losses, the devices (in their present status) are considered unacceptable for use in a DC VSCF system.

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FOREWORD

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LIST OF ILLUSTRATIONS

Section I
INTRODUCTION

1.0 OBJECTIVE

This program was an exploratory development effort to design, develop and test a 400 hz variable speed constant frequency (VSCF) type power system which employs a pulse width modulated (PWM) converter operating in conjunction with a variable voltage/frequency permanent magnet generator (PMG)*. The program objective was to demonstrate an advanced generating system concept which would yield performance, efficiency, volume, weight and cost advantages over state-of-the art VSCF systems. The converter/generator was to have been tested in a prototype system with the following general characteristics: 1) 40 KVA system rating, 115V, 3ϕ, 400 Hz, 2) Base speed as required, and 3) Minimum speed range 2:1.

2.0 SCOPE

This effort included the following tasks: 1) Design of a prototype permanent magnet generator, 2) Design of a "brassboard" converter, 3) Fabrication of the generator and the converter, 4) Generator and converter testing, 5) System testing and 6) Reporting. The program was to be accomplished in the distinct phases

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*The term pulse width modulated (PWM) will be used throughout this report as nomenclature for DC to AC conversion devices which create AC from DC via high speed solid state switching devices. A typical example of waveform construction via this technique is shown in Figure 2.

identified below. The time periods in parentheses were Air Force estimates of the times required to accomplish each phase.

Phase I   - Design (6 months)
Phase II   - Hardware Fabrication (11 months)
Phase III - Tests (7 months)

The following tasks were completed as a part of this effort:

a)   Design of a prototype permanent magnet generator
b)   Design of two different breadboard converters
    1)   Bridge Inverter (Original Design)
    2)   Interphase Transformer Inverter

c)   Limited breadboard converter testing
d)   Reporting.

3.0 BACKGROUND

There are three alternative technologies available today for the manufacturer who wishes to design an aircraft electrical power system. These are the cycloconverter, as is used in the F-18 and A4 VSCF systems, the constant speed drive-synchronous generator combination, and the DC link VSCF approach, used on the AV-8B and the F-5G.

Recent developments in the field of high power Darlington pair configured transistors have increased both current carrying capability and blocking voltage to the point that high power (40 KVA) pulse width modulated inverters are possible. These inverters, when used with a rectifying SCR bridge, should provide a DC link system competitive in size, weight, and electrical performance with cycloconverter and constant speed drive systems.

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Section II
CONCLUSIONS AND RECOMMENDATIONS

1.0 CONCLUSIONS

The work done by the General Electric Company during the project
has resulted in the conclusion that a 40 KVA pulse width modulated
DC Link VSCF using state-of-the-art Darlington transistors is not
viable at this time. The devices chosen for this application had
much lower base drive current requirements than discrete power
transistors of equivalent rating and were lower in cost than other
comparable Darlington pairs. Despite these advantages, high power
Darlington transistor technology is not sufficiently advanced for
a DC Link system to possess size, weight and efficiency advantages
over other comparable VSCF technologies.

2.0 RECOMMENDATIONS

This program did not produce a 40 KVA PWM VSCF which could meet
all the required specifications, because of device inadequacies.
A concerted effort should be made to further develop the tran-
sistor technology to the point where it becomes technically
viable in the PWM application.

Section III
ORIGINAL CIRCUIT DEVELOPMENT

1.0 DESIGN

The original concept for the PWM converter design was to use a 9
phase PMG and 3 three phase SCR bridges to generate 3 separate
DC links of approximately 200 volts DC each (Figure 1). These
DC voltages would then be converted to 3ϕ 115/208 volt AC using
three H bridge inverters with output filters used to eliminate
output harmonics. These bridges would use 500 volt, 200 amp
ZJ504 General Electric Darlington transistors to enable the out-
put voltage of the inverters to be pulse width modulated.

The algorithm chosen to accomplish this was to compare a variable
amplitude sinusoidal reference wave with a fixed amplitude high
frequency triangular carrier wave (Figure 2). The frequency of this
carrier wave determined the necessary filter size. The original
concept set this frequency at 4800 hz with a 400 hz sinusoidal
reference.

The output of the PWM logic was then fed to a proportional base
drive to drive two of the Darlington transistors (located in the
upper two legs of the inverter bridge) at a 4800 hz rate. The other
two Darlingtons (in the lower two legs of the bridge) were driven
at a 400 hz rate by a 400 hz square wave, generated by detecting
the zero crossings of the reference wave. So, two of the legs of
the inverter would conduct to produce positive or negative voltage
across the load and filter. The conducting legs were determined by
which half cycle of output voltage was being generated (Figure 3).

To test this concept a prototype breadboard was built using General
Electric D67DE7 700 volt, 100 Amp Darlington pair transistors. The
control logic was 2 circuit cards with standard 4000 series CMOS
logic.

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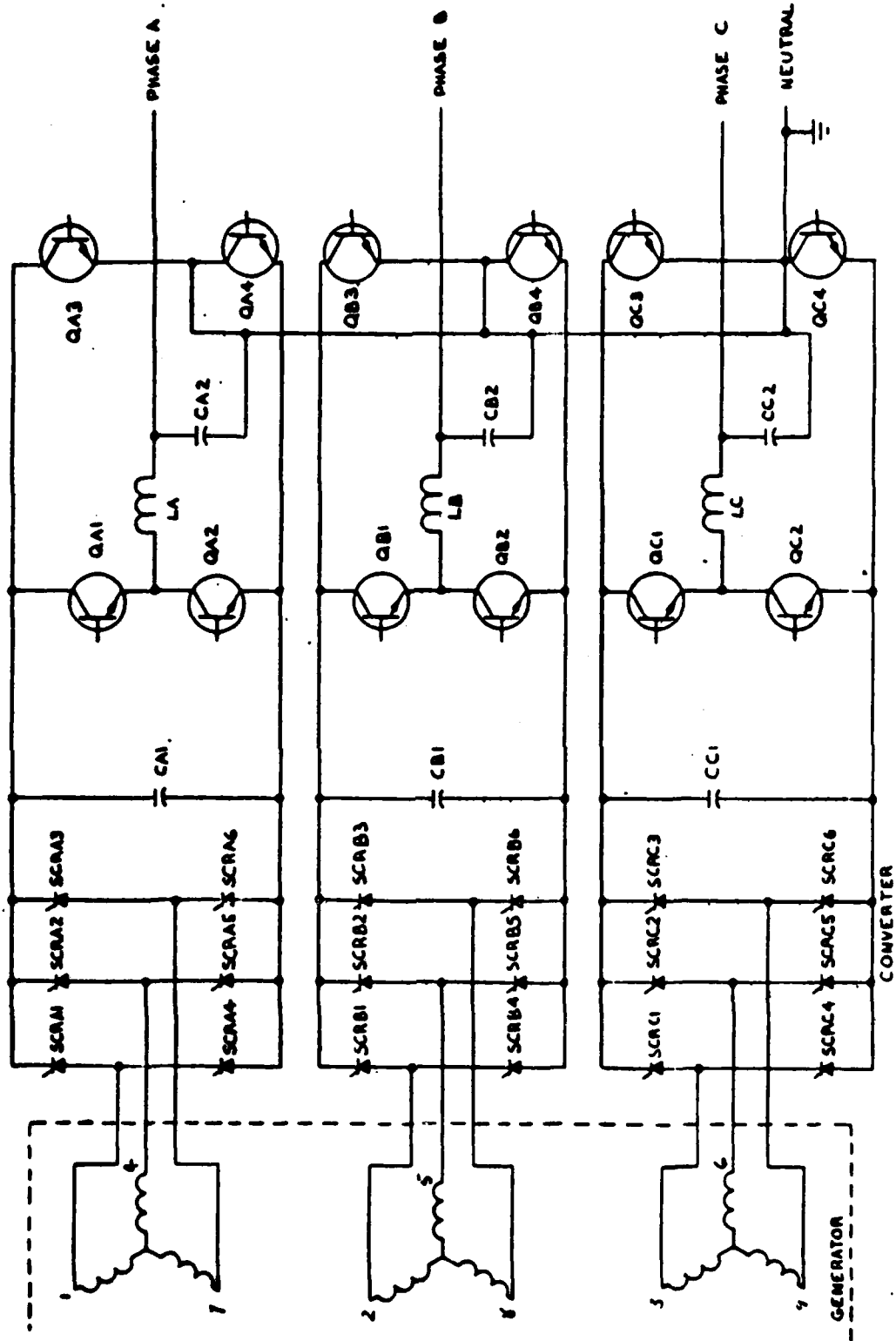
Figure 1. Original Power Circuit

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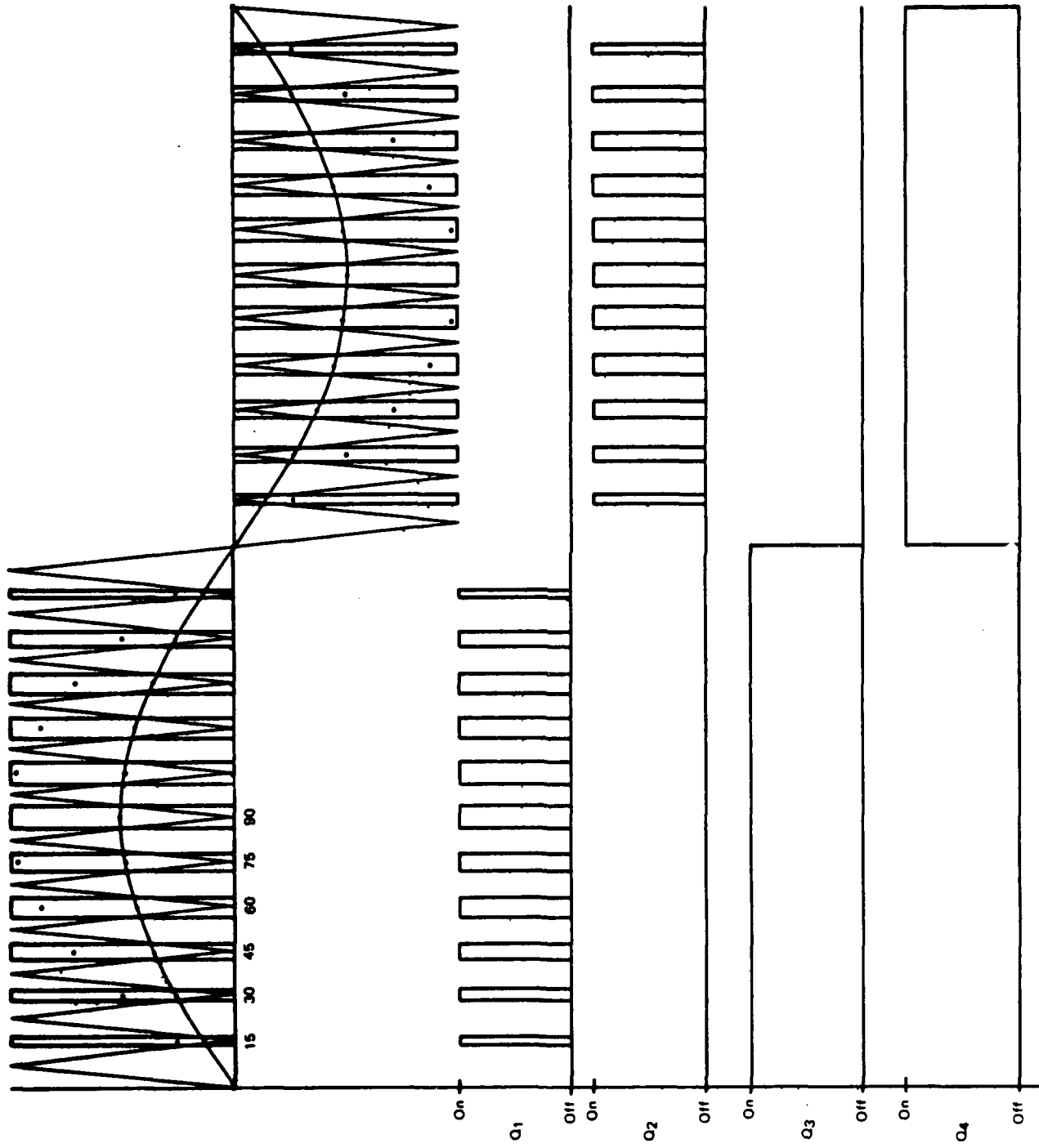
Figure 2. Triangular Wave-Reference Wave Comparison
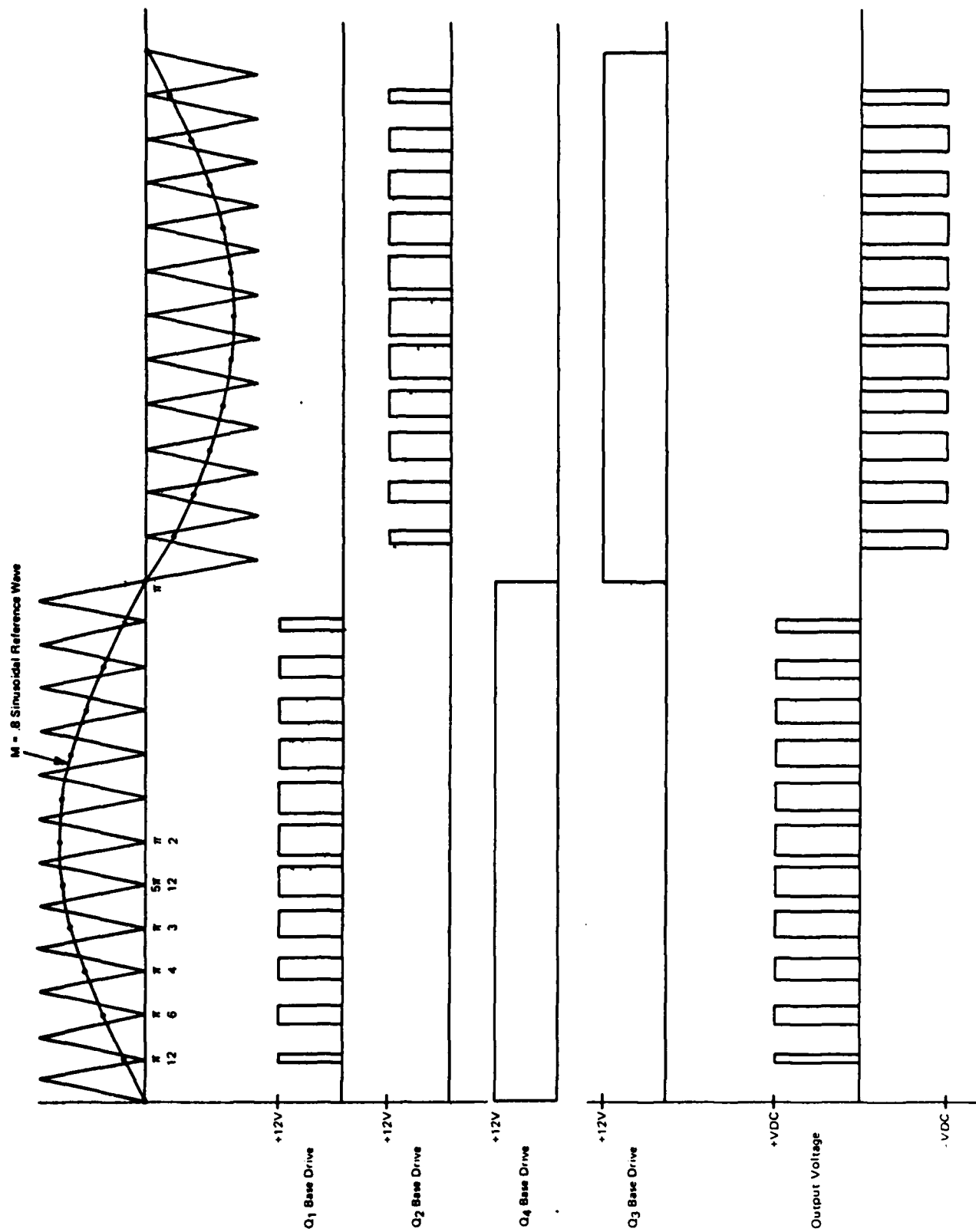
Figure 3. Base Drive Timing

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2.0 DESIGN CONSIDERATIONS

There were four areas in which changes from the original circuit were found to be necessary after extensive breadboard testing. These were as follows:

1) Output Filter Size
2) Proportional Base Drive Saturation
3) Location of Signal Ground
4) Undesirable Voltage Spikes at Zero Crossings.

This testing process exposed these areas as places where the design could be optimized and trade-offs made to improve the system performance.

The first consideration was that the output filter was required to be too large (212µh, 120µf, a corner frequency of 998 Hz) to reduce the output harmonics of the bridge voltage to acceptable levels. The energy in the output harmonics was concentrated around 4800 Hz, the frequency of the triangular carrier wave mentioned earlier. The effect is characteristic of PWM inverters which are modulated by triangular carriers and has been mentioned in several papers, Reference 1 being one such paper.

This problem of low frequency output harmonics and output filter size made it necessary to change the fundamental carrier wave frequency from 4800 to 9600 Hz. This change enabled the output filter inductor to change from 212µh to 121µh, yielding a break frequency of 1320.8 Hz. This change was possible because the new carrier wave frequency concentrated the bridge voltage harmonic energy around 9600 Hz, rather than 4800 Hz.

The second consideration was that the magnetics in the proportional base drive circuit (Figure 4) saturated in the middle of the output voltage waveform as the DC link voltage was increased, causing additional distortion in the output voltage. In addition, the base drive requirement of Darlington connected transistor pairs are not as severe as originally thought, so the proportional base drive was found not to be necessary. A new base drive circuit using MOSFET transistors (Figure 5) was used to replace the original proportional base drive circuit.

Using MOSFET devices reduced the parts count of the base drive by a factor of 4 to 1. In addition, it reduces the delay time between logic level signals and the output voltage of the inverter bridge. An additional consideration was that the current in each Darlington pair was no longer coupled to the base drive, so the magnetics in the new base drive did not saturate.

The third consideration was the location of signal ground. Originally, signal ground was located at the negative side of the DC supply, enabling the use of directly supplied base drives for the Darlington pairs switched at 400 Hz. However, it was more advantageous for feedback purposes to have signal ground at an emitter of one of the Darlington pairs whose base drive was pulse width modulated. This necessitated using an isolated drive for the Darlington pairs which were switched at 400 Hz (Figure 6).

The fourth consideration was undesirable voltage spikes at zero crossings of the reference wave. The reason for this was the switching between the two Darlington pairs at 400 Hz at the zero crossing points of the reference wave.
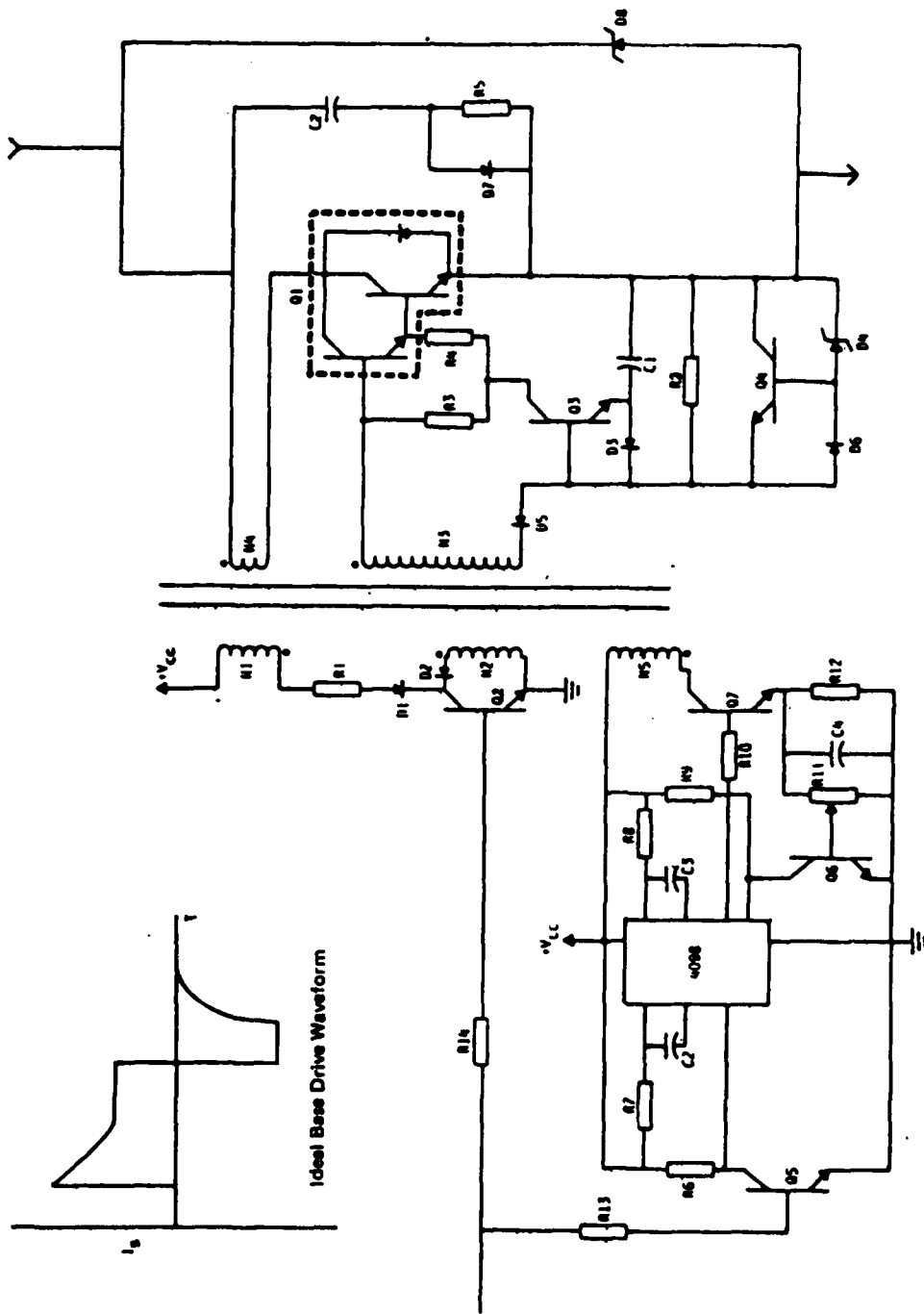
Figure 4. Proportional Base Drive Circuit
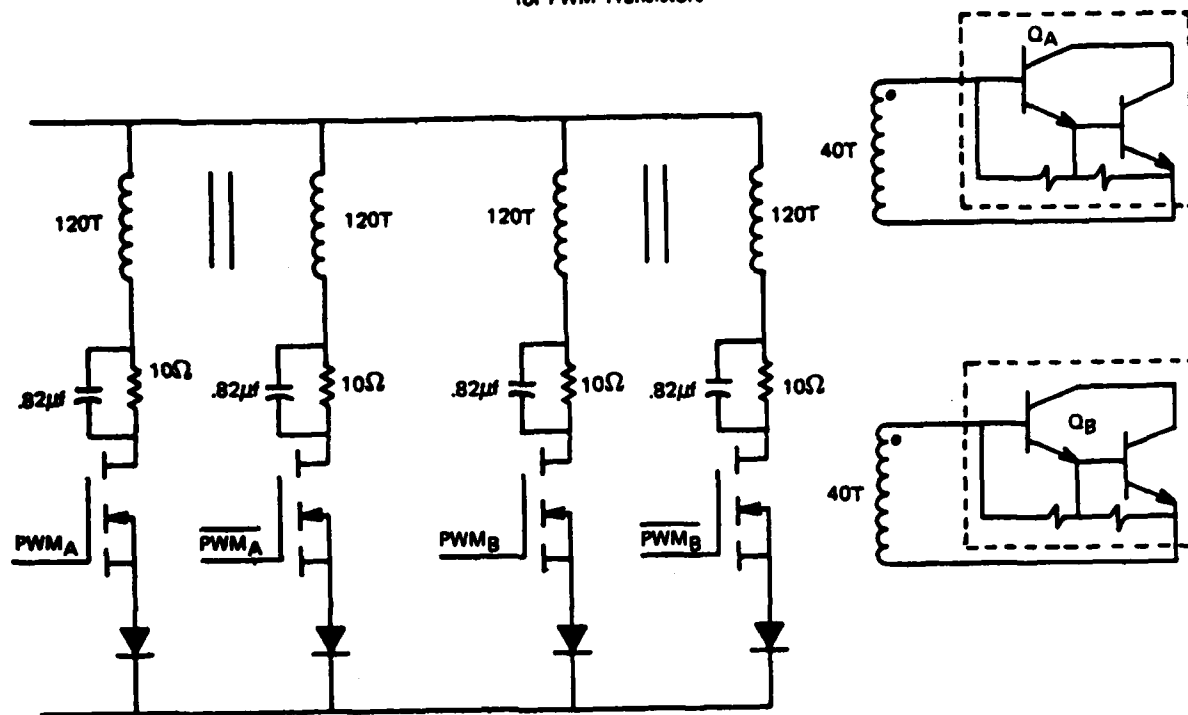
Simplified Representation
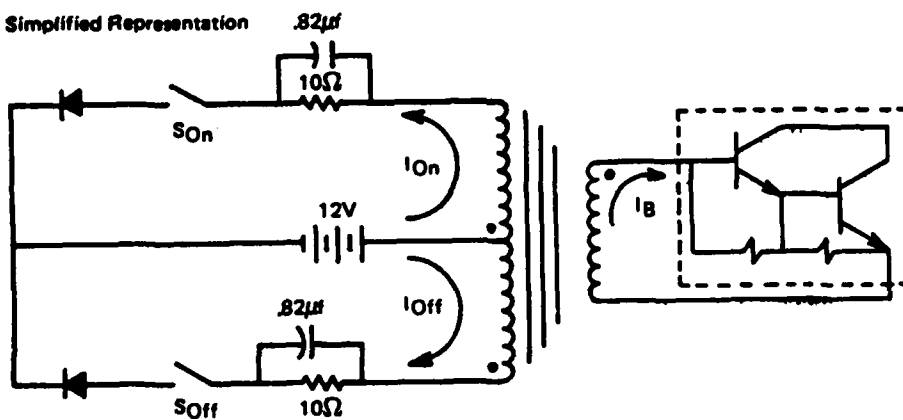
Produces waveform similar to ideal base drive waveform

Switching times below 1μs using MOSFET drives

Less complex (fewer parts) than proportional base drive

Proportional drive not necessary for Darlington transistor pairs (Darlingtons have low base current at rated current levels, unlike single BJT application).

Figure 5.   New Base Drive

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400 Hz Base Drive
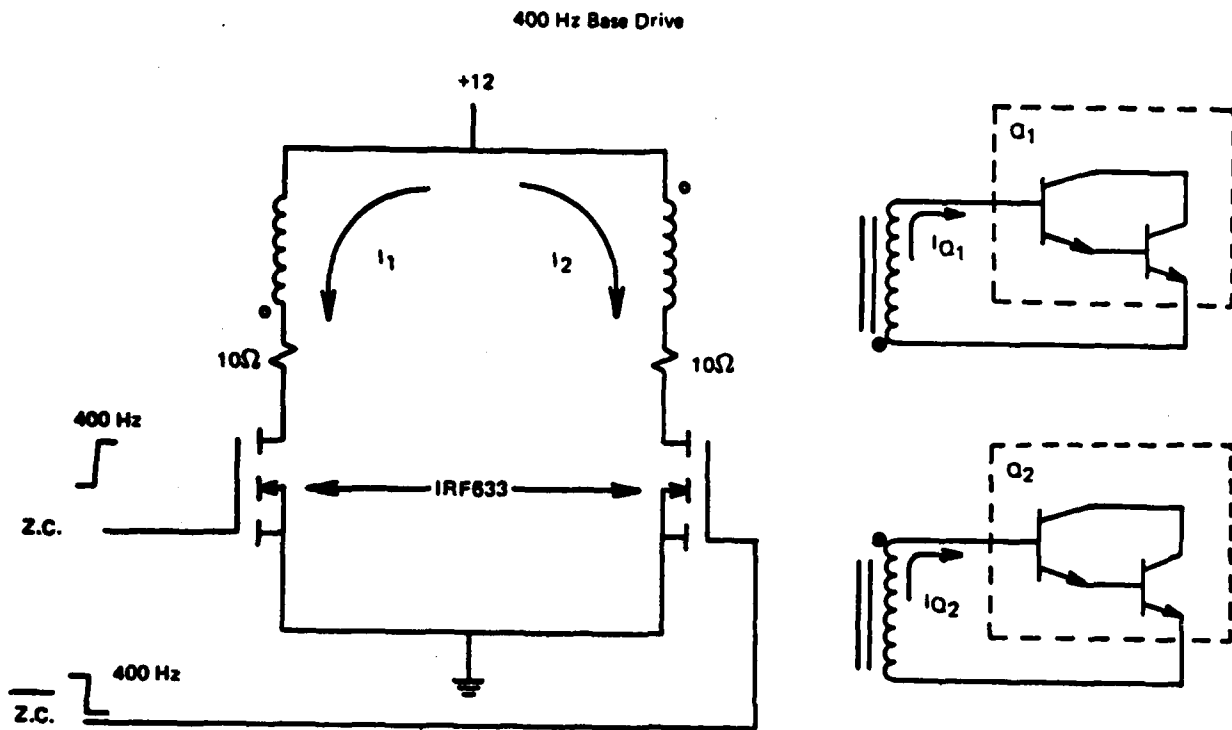
When the Zero Crossing (Z.C.) signal is +12 volts, I_1 flows, inducing a current I_{Q_1} to flow, turning on Darlington pair Q_1. When the inverted zero crossing signal ($\overline{Z.C.}$) is +12 volts, I_2 flows, inducing I_{Q_2} to flow, turning on Darlington pair Q_2. Using the IRF633 MOSFET devices enables the circuit to have switching time delays within the specification of the D67DE 100 Amp GE Darlington. Using bipolar devices adds 2-4 μs to the switching time delays.

Figure 6.   Isolated 400 Hz Base Drive

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If the current I in Figure 7 is nonzero when S_4 switches off and S_3 switches on, diodes D_3 and D_2 conduct until I is zero. This conduction made $V_{BR} \approx -V_{DC}$ at a time when that condition was not desired, e.g., at the zero crossing of the 400 Hz reference wave.
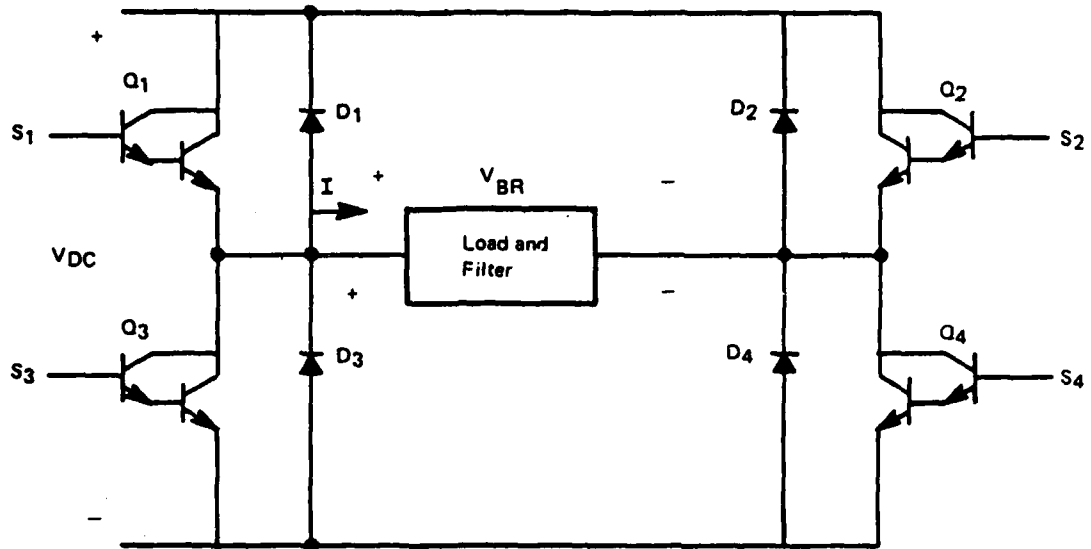
Figure 7. Voltage Spike Problem

This problem was resolved by reconfiguring the circuit so that both Darlington pairs switched at 400 Hz were on the ground side of the bridge, turning on Q_1, after the positive-negative zero crossing until S_3 requires Q_3 to turn on, and turning on Q_3 after the negative-positive voltage zero crossing until S_1 requires Q_1 to turn on (See Figure 8).

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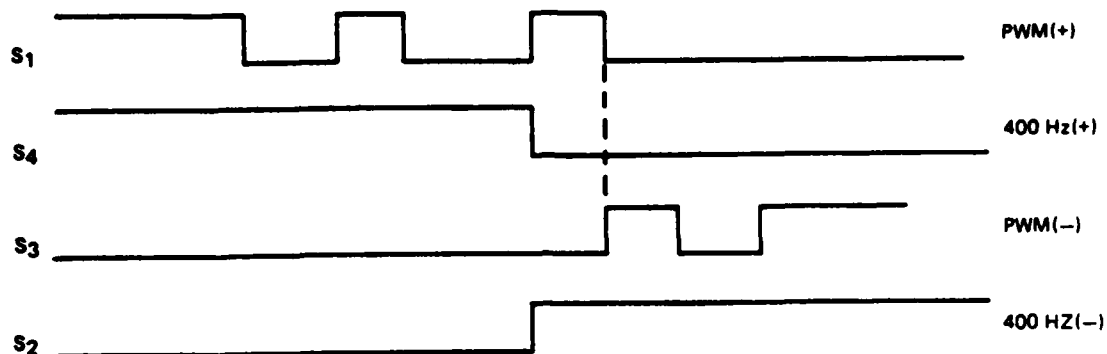
Figure 8. Positive-Negative Zero Crossing

Referencing Figure 7, assume I_{pos} flows through Q_1 and Q_4 initially. During the times when Q_1 is off, current flows through D_3 and Q_4. At the zero crossing of the reference wave, Q_4 turns off and Q_2 turns on. However, if I_{pos} still flows in the same direction, it must flow through D_2 and D_3. To prevent this from happening, Q_1 is turned on again after the zero crossing. This provides a path for I_{pos} to flow (through Q_1 and D_2) which prevents V_{DC} from appearing across the load until Q_3 turns on again. In this manner, this change eliminated the unwanted zero crossing voltage spike.

This consideration led to the idea of switching S_1 and S_3 in a complimentary fashion so that lagging current will always have a path to flow. To accomplish this, S_1 and S_3 were changed so that S_1 = PWM (+) + $\overline{PWM\ (-)}$ and S_3 = PWM (-) + $\overline{PWM\ (+)}$. A 5μs delay was introduced in the inverted PWM signals to prevent shorting of the DC voltage through Q_1 and Q_3.

Appendix A contains a detailed description of how these signals were generated with CMOS logic.

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At this point, the output filter inductor size was still not optimal, and the switching rate on the two PWM transistors (Q_1 and Q_3) could not be doubled again to 19,200 Hz without creating unacceptably high switching losses in the D67DE7 devices. So, a new switching algorithm was developed (originally for use in the IPT inverter discussed in Section IV) which was applied to the original circuit as well. This algorithm, shown in Figure 9, caused all four Darlington pairs to switch at 9600 Hz, while the output voltage switched at 19,200 Hz. This enabled the output inductor size to be reduced to 40 µh as opposed to 121 µh in the original circuit. A new control circuit and two more MOSFET base drives were built, but the algorithm was not tested in the original breadboard at full voltage before work was halted.
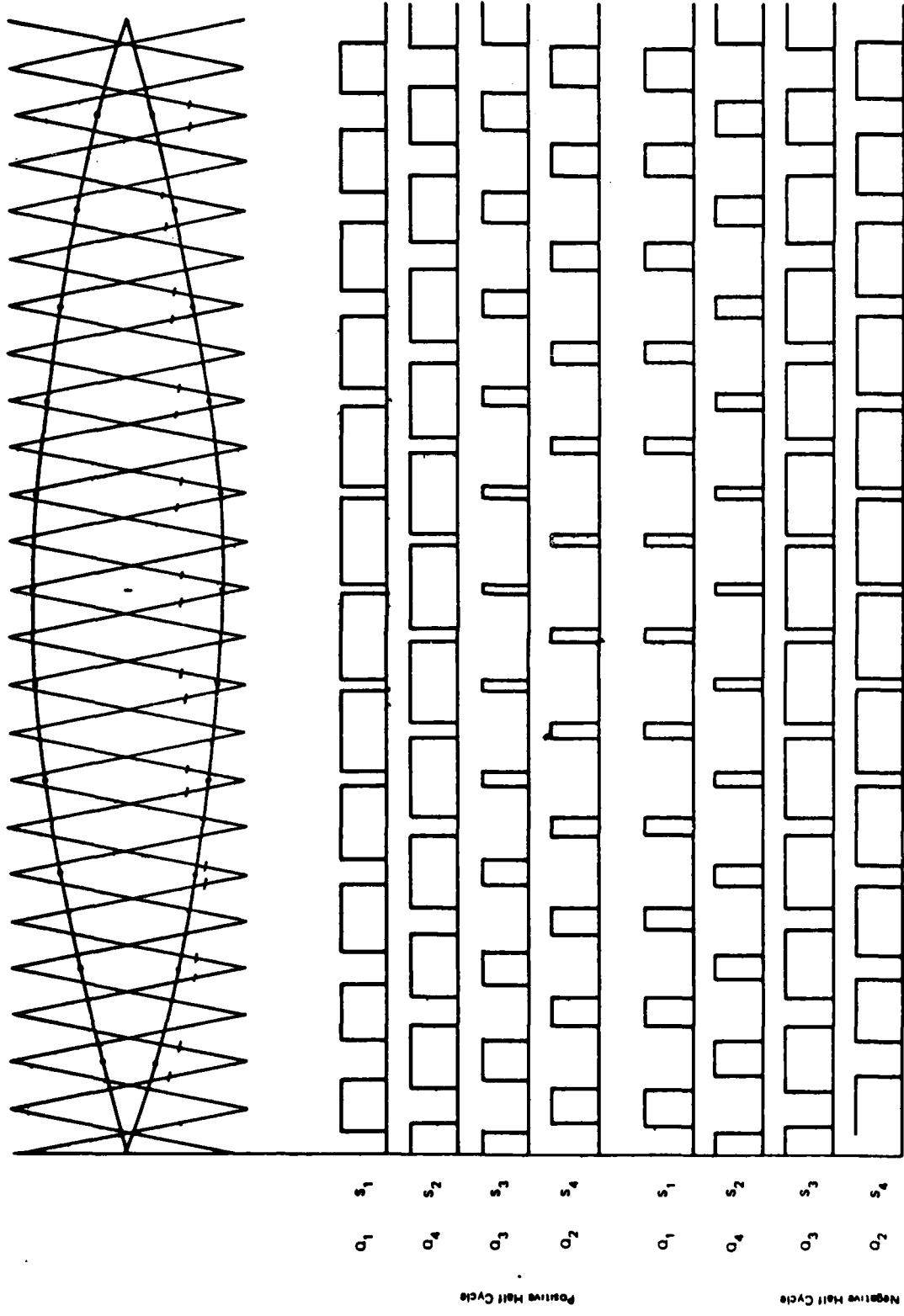
Figure 9. 9600/19200 Hz Switching Sequence

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Section IV
INTERPHASE TRANSFORMER INVERTER DESCRIPTION

1.0 DESIGN

The approach to DC link discussed in Section III was the version
which was presented in the proposal. That approach, using 3
three phase rectifier bridges and 3 inverter bridges was not
the most economical in terms of parts count. After much consid-
eration, General Electric developed an approach which appeared
attractive compared with both the bridge circuit General Electric
had been pursuing and alternative approaches which require
either a neutral forming transformer or a full output transformer.
This new circuit uses the interphase transformer concept to pro-
vide the advantages of current sharing and reduced ripple that
it has traditionally done for rectifier circuits.

Figure 10 shows the power circuit. The switches can be transis-
tors, gate turn off devices or thyristors if commutation means
are provided. The interphase transformer (IPT) is normally
designed with a small air gap in its magnetic path to accommo-
date some DC current resulting from imperfect switching patterns.
All or part of the separate filter inductance can be designed
into the IPT.

In Figure 10, a center tapped DC supply (±180V) is shown supply-
ing three IPT inverters. In comparing this arrangement with the
circuit shown in Figure 1, two differences are noted.

    1)   One third fewer parts than the three 3ϕ rectifier
           bridges (12 SCRs vs 18).

Figure 10. IPT-Inverter Power Circuit

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2) The double frequency ripple current which flows through the DC link capacitor on the output of each 3φ rectifier bridge in Figure 1 does not flow, except for unbalanced load conditions, in the DC link capacitors in Figure 10.
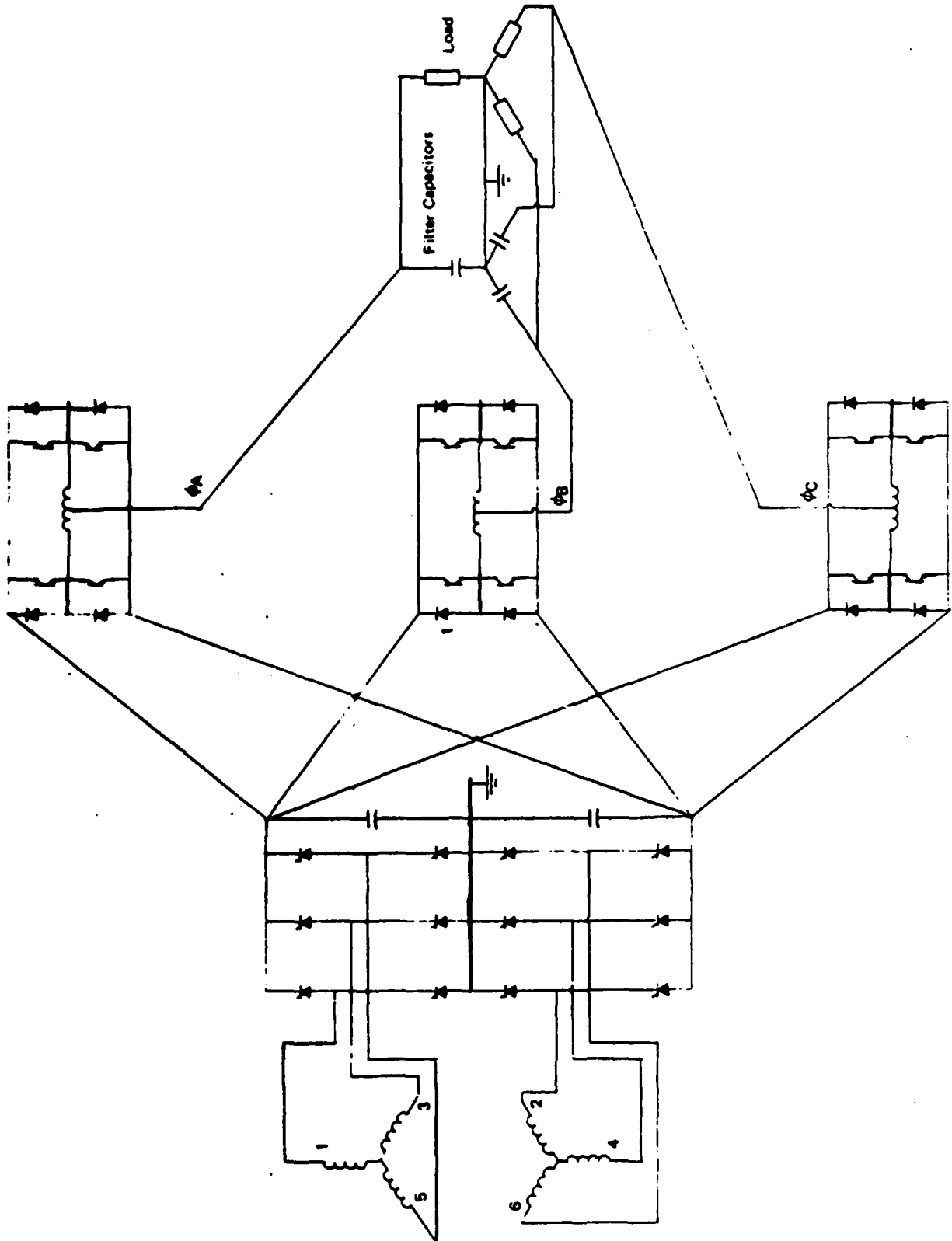
Figure 11 shows the switching sequence and voltages using standard triangle wave modulation. S_1 and S_3 cannot actually switch simultaneously but must have suitable delays to avoid the possibility of shoot-through currents which would occur if both transistors are allowed to conduct at once.

A complete switching sequence will be examined, first with current and voltage in phase and again with current and voltage out-of-phase.

Assume current and voltage are both positive (current flows into the load and the load voltage is positive with respect to ground). If switches S_1 and S_2 are both closed, current flows into the ends of the interphase transformer and out its center to the load. The output voltage is the + bus voltage neglecting switch and IPT losses. The interphase transformer forces equal sharing of current by S_1 and S_2 even though they have significantly different characteristics, since the ampere turns in the two windings must be equal except for excitation.

Next let S_2 be opened and S_4 closed. Equal currents must flow in both halves of the IPT so current must continue to flow into the right end of the transformer. Since S_2 is open, current must flow up from the negative bus. With ideal switches, the pumpback diodes would not be required and this current would flow up through S_4. The practical requirement of delaying the closure of S_4 until after S_2 is open as well as the unipolar
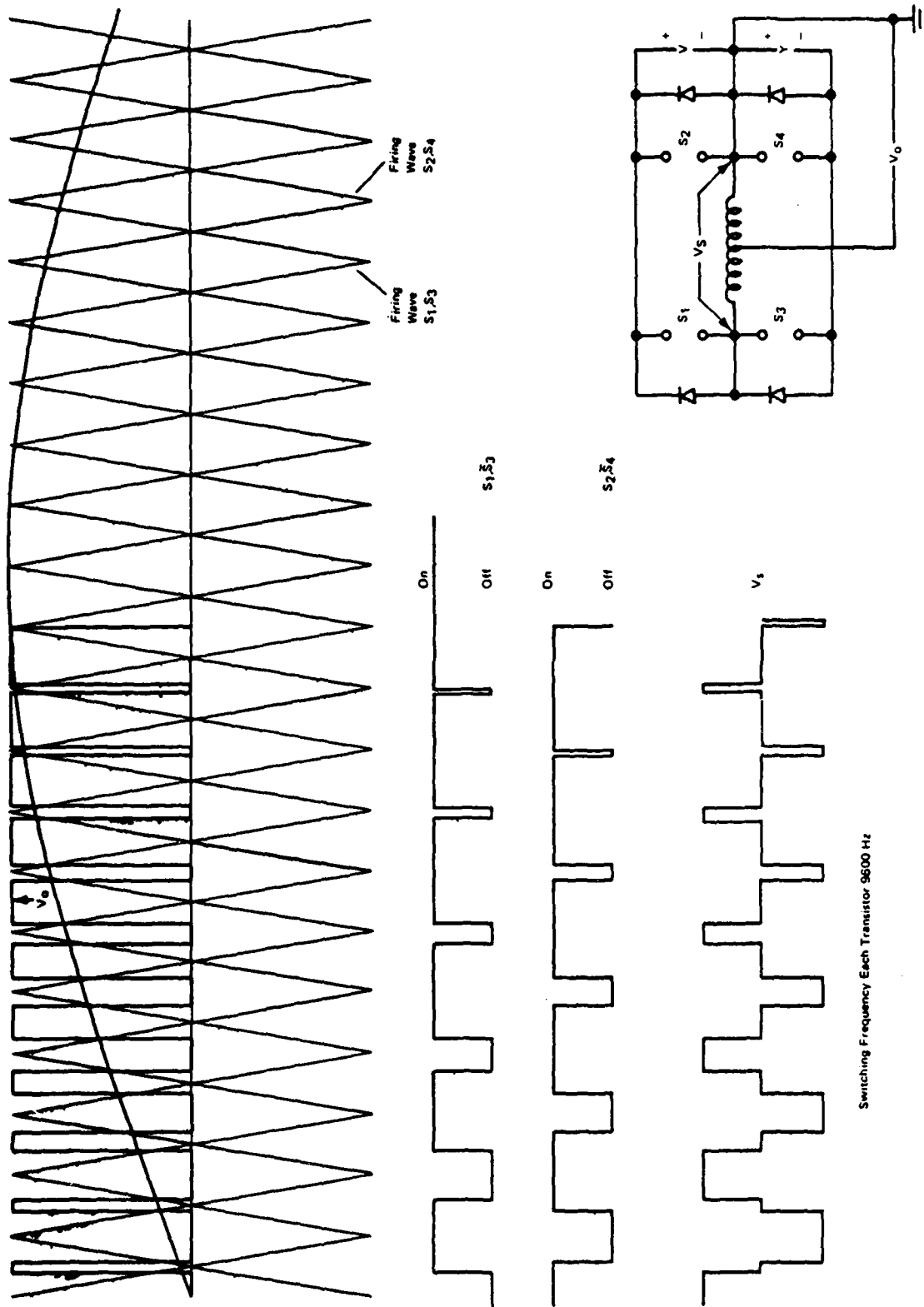
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Figure 11. IPT Inverter–Switching Sequence

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current flow of most semiconductor switches makes the diodes necessary thus the current path is up through diode 4. The IPT now spans the busses and its center tap is halfway between or at ground. When S_2 is turned on again, the output returns to the + bus voltage. The cycle is completed by turning S_1 off. Current flows through S_2 and diode 3 and the output voltage is zero. Figure 12 shows the current paths for the four segments of the cycle. Next let the voltage remain positive but the current be negative as it would be with lagging load in the early part of a positive voltage half cycle.

The switching cycle is the same as before but the current paths are different. Referring to Figure 13 during interval one when S_1 and S_2 are closed, circuit flows up through their companion diodes. Output voltage is at the + bus as before.

When S_2 opens and S_4 closes, current flows down through S_4 and continues through diode 1. The IPT again spans the voltage busses and the output voltage is zero.

Interval three is the same as one.

The cycle is completed with the opening of S_1 and closure of S_3. Current flow is through S_3 and diode 2. The IPT again forms a zero output voltage interval.

It has been shown that the IPT forces current sharing of even poorly matched switches. The second advantage of this circuit is in reducing the filtering required.
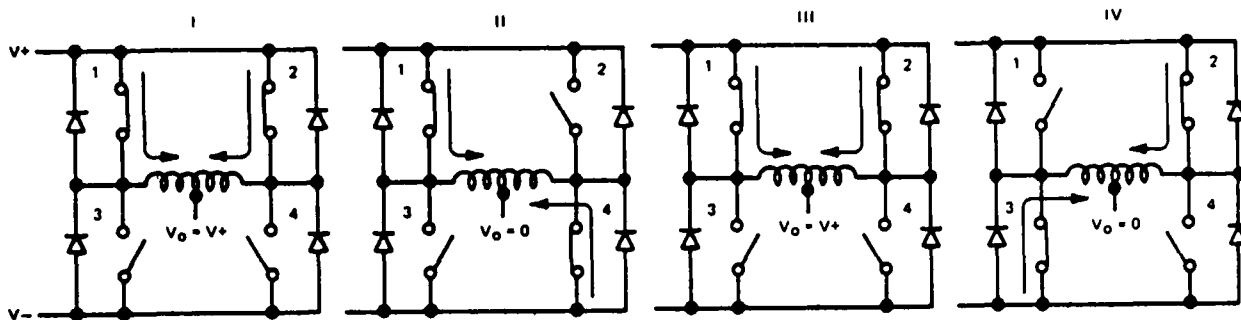
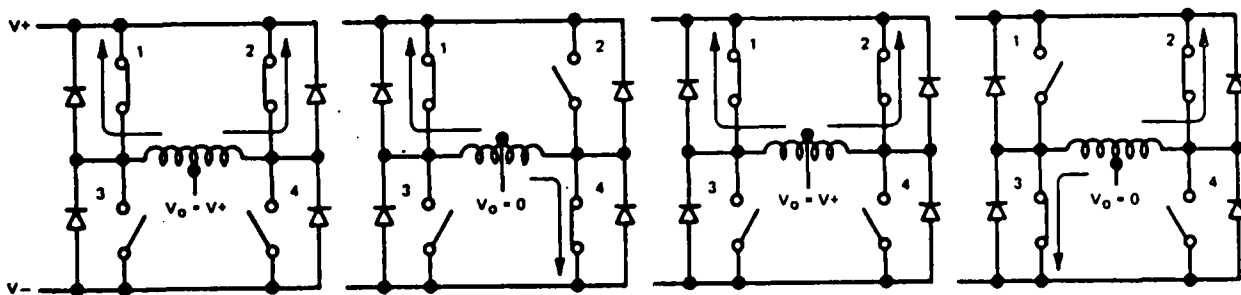Figure 12.   IPT Inverter - Current and Voltage Positive

Figure 13.   IPT Inverter - Current Negative Voltage Positive

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The ripple voltage and currents of this circuit will be compared with a conventional inverter with the same switching frequency and then with a conventional inverter composed of two sets of switches, switching out of phase and summed through individual filter inductors rather than an IPT.

A simple switch pair generates zero average voltage by switching from the + to - bus and back at a constant rate. The ripple volt seconds are the bus voltage times the half period at the switching frequency. As the periods when the switches are connected to busses become unbalanced, the average voltage rises, and the ripple decreases as shown in Figure 14. Also shown in Figure 14 are the ripple volt-seconds for the IPT circuit. There is no ripple at zero output voltage as well as at full output. The peak ripple occurs at half maximum output and is one fourth the ripple volt-seconds of the single switch pair at zero output voltage.

There is a significant advantage in using the interphase transformer rather than paralleling switch pairs with out-of-phase switching patterns through simple inductors as shown in Figure 15. The ripple voltage at the load is identical to the IPT circuit but the ripple currents can be much different. The ripple current flowing to the load and filter capacitors are identical if the simple inductors for the two inductor circuits have twice the inductance of that of the IPT circuits. The ripple current flowing between the switch pairs can be independently controlled in the IPT circuit without changing the output impedance of the circuit by varying the IPT end to end inductance. In the two inductor circuits, the ripple current flowing between switch pairs can be reduced only by proportionately increasing the output impedance. Typically the IPT end to end inductance is twenty or more times the filter inductance so the current

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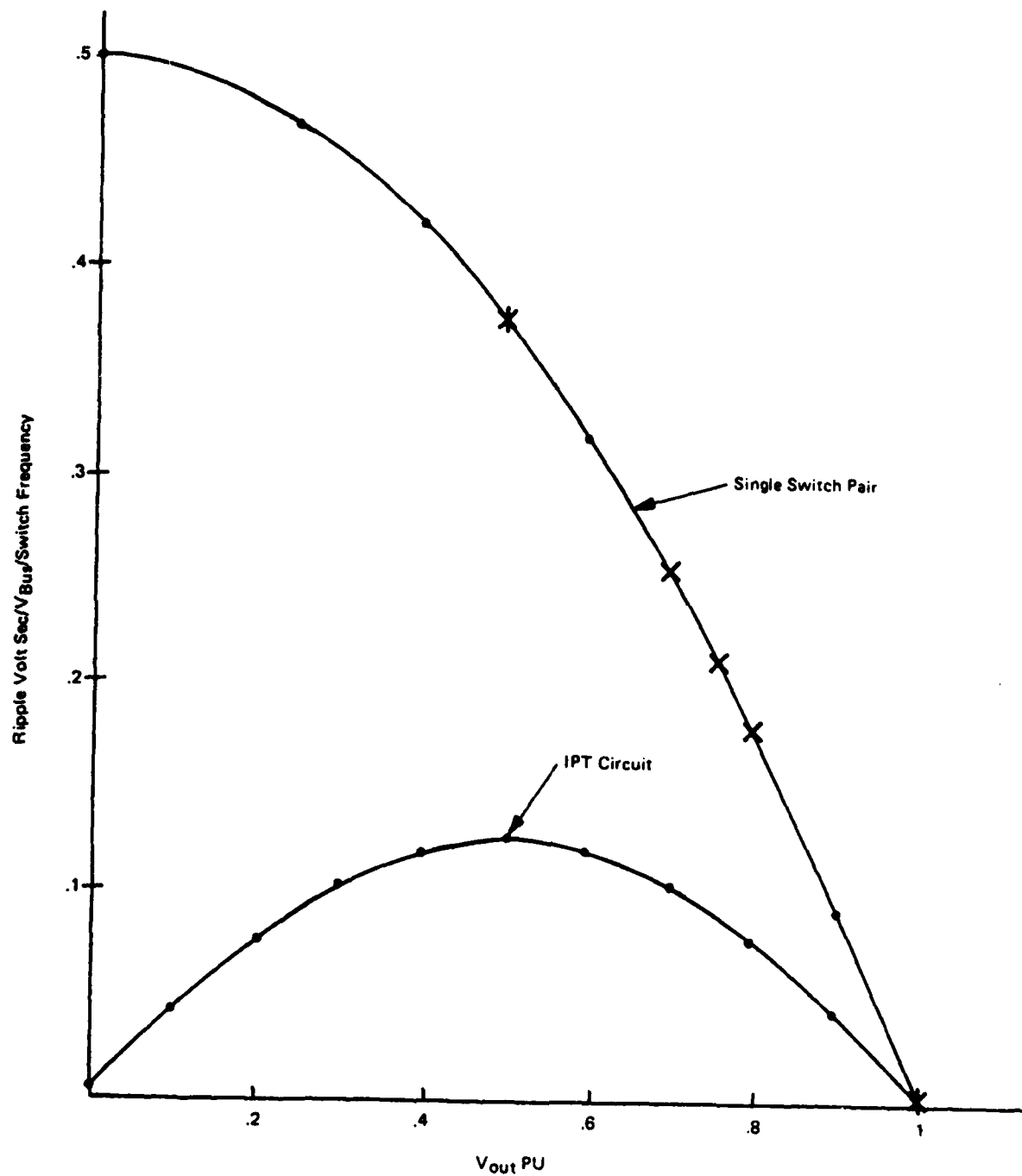
Figure 14.   Ripple Volt - Sec vs Volts
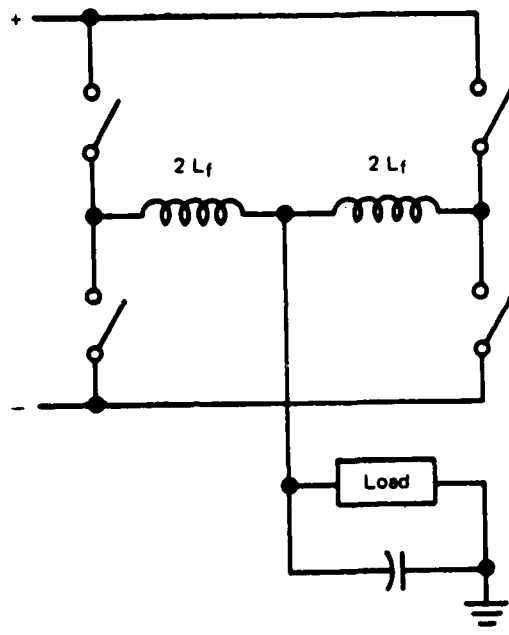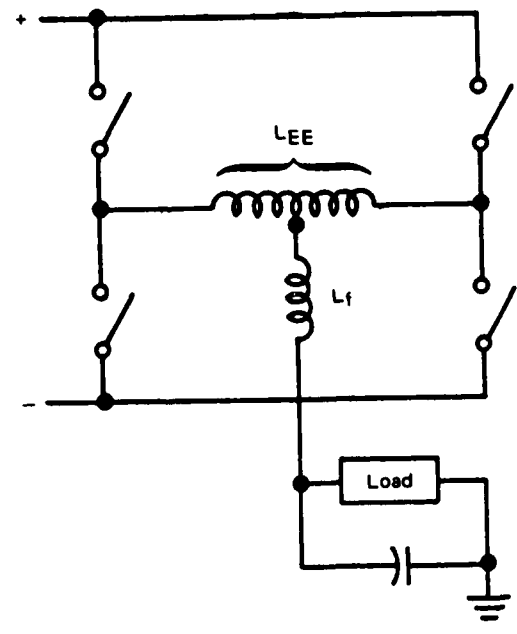
Figure 15.   Individual·Inductors vs IPT

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flowing between switch pairs is 1/5 or less than that of the two
inductor circuit.

Minimizing ripple current results in some saving in I^2R loss but
the major factor is reduction of the current which must be
switched, which is the sum of load and peak ripple current. Un-
less the peak ripple current can be held to a small fraction of
the load current, there is a large penalty in switching losses
and load handling ability.

Section V

GENERATOR DESIGN

1.0 DESIGN

The PWM converter circuit shown in Figure 1 required a nine phase
generator to supply three 3-phase SCR bridges. This generator
was the one which was designed originally. However, when it
became apparent that the interphase transformer converter was a
more attractive alternative than the 9 phase system, a change in
the generator design from 9 to 6 phase output was necessary (see
Section 4). This change only affected the stator windings, the
rotor was not changed. The generator was designed to comply
with the interface specifications. It was, after redesign, a
six phase synchronous machine having a frequency of 1250 hz at
base speed. The winding configuration was selected to be two
isolated three phase windings to supply power to a positive DC
link and a negative DC link in the converter. The generator
layout is shown in Figure 16.

The speed range selected was 15,000 rpm to 30,000 rpm which is
the specified speed range for the 60 KVA Advanced Development
Program. The laboratory test model of the generator was con-
figured to make maximum use of available tooling and test equip-
ment, while maintaining the ability to easily convert to a
production configuration. The rotor and stator are derived from
the 60 KVA program and housed inside the stator frame of the
F-18 generator. Although this frame is specifically designed
for an integral generator/converter system, the basic design can
be easily modified to permit separate mounting of the units in a
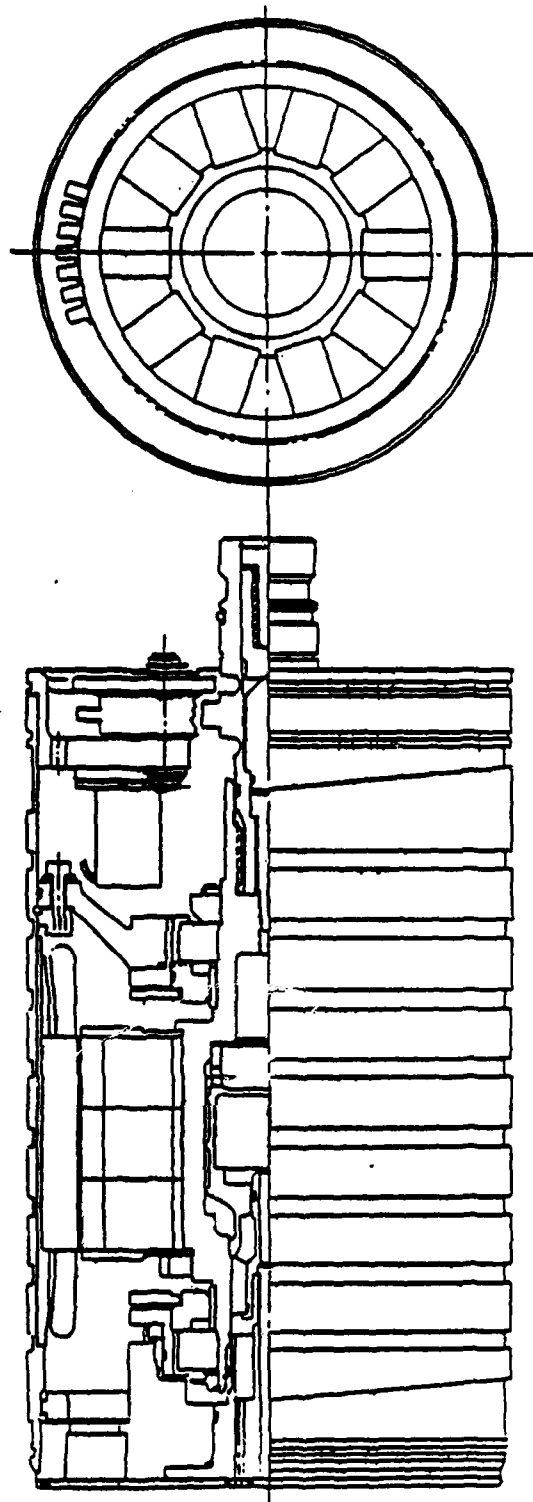production configuration, if desired.

Figure 16. Generator Layout

The adapter required to test the generator is shown in Figure 17. The weight of the generator/adapter package is less than 75 pounds and exerts an overhung moment less than 500 inch pounds.

The oil flow schematic for the generator is shown in Figure 18. Cooling oil for the generator at base speed is approximately 4 gpm. The electromagnetic design, based on the use of the F-18 stator frame shown in Figure 19. has the following features:

1. The stator is a conventional aircraft design with 6 mil permendur lamination to minimize weight and increase efficiency by reducing core losses. The punching has 90 slots and is wound with 16 strands of No. 23 HML magnet wire. The total stack length required was 2.88 inches.

2. The rotor has 10 poles. The magnets are Samarium Cobalt having an energy product of 21 MGOe. (This is the highest level available in production quantities and expected to be competitively priced when production quantities will be required.)

The rotor hub is made from Inconel and the poles are made from low carbon magnetic steel. The magnets are contained by a bimetallic shrink ring having alternate magnetic and non-magnetic segments. The two bearings used are the MM9107 having an ABEC7 precision. Two seals are used at either end to maintain a dry rotor cavity. These seals are the circumferential type having spring loaded carbon riding on a film of oil.
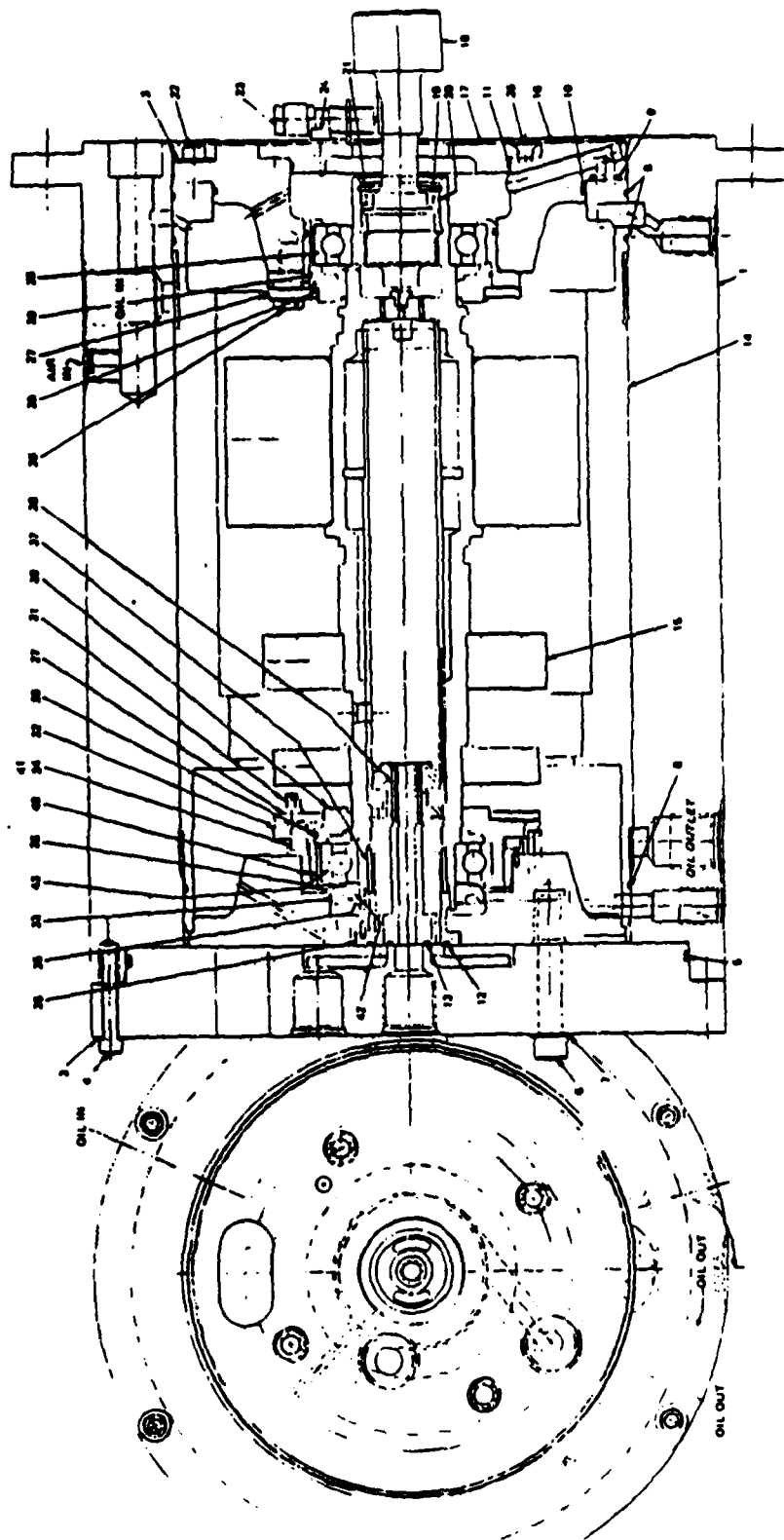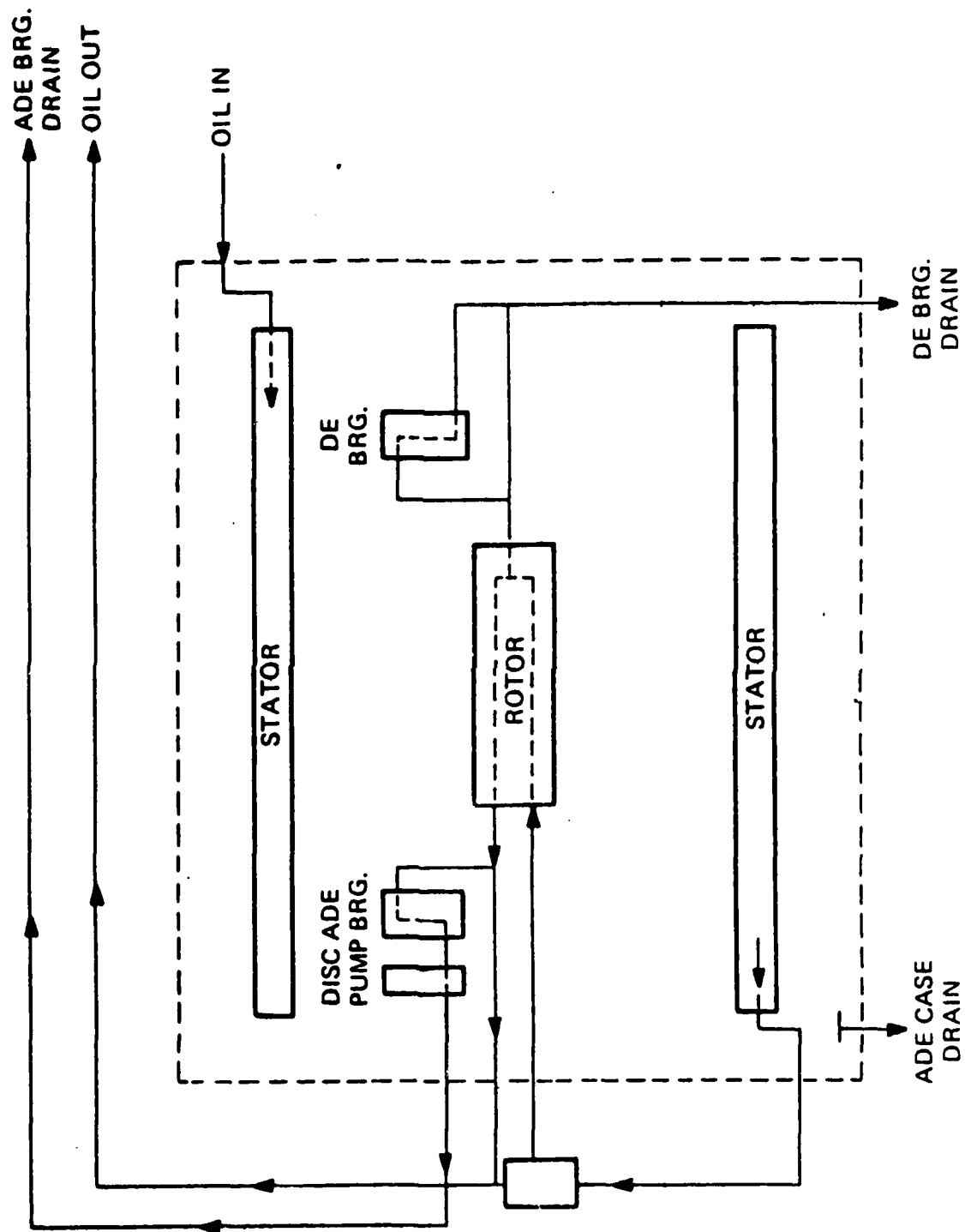
Figure 17. Generator Adapter
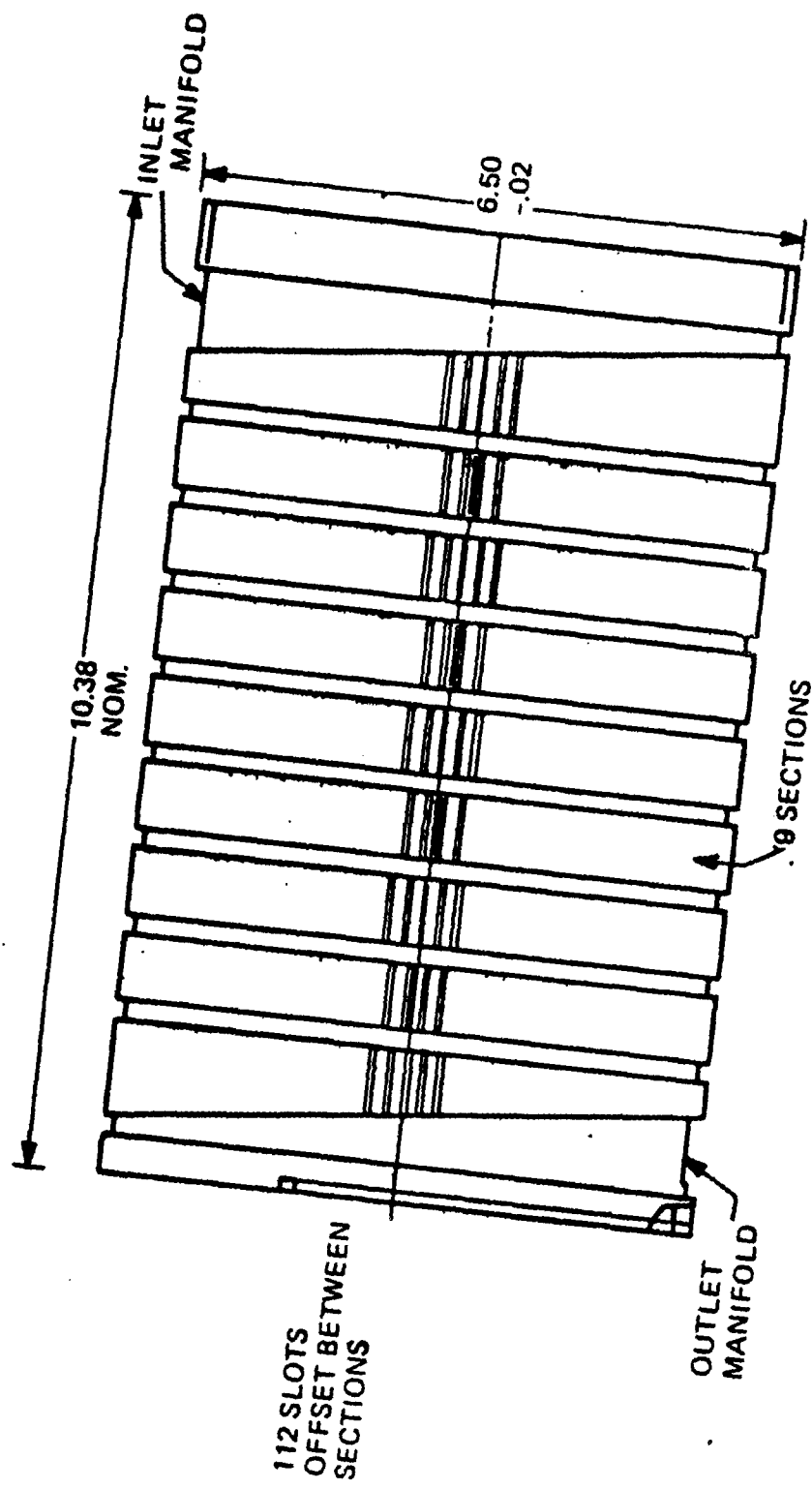
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Figure 18. Generator Oil Flow Schematic

Figure 19. F-18 Stator Frame

INLET MANIFOLD

6.50 -.02

10.38 NOM.

.9 SECTIONS

112 SLOTS OFFSET BETWEEN SECTIONS

OUTLET MANIFOLD

Appendix A
ORIGINAL DESCRIPTION OF CMOS LOGIC

The entire CMOS control circuit is shown in Figure A-1. This current used CMOS logic to produce PWM signals for Q_1 and Q_3 (see Figure 3, Section III) and 400 Hz signals for Q_2 and Q_4. The reference wave generator was a General Electric design which was originally used on the 60 KVA ADP and will not be discussed here.

A standard 1.2288 MHz crystal is used to generate a clock signal which is the input to a divide by three circuit and a 12 stage ripple carry binary counter/divider. The divide by three circuit (Figure A-2) produces 409.6 kHZ, which is an input to the reference wave generator, which generates 400 Hz sinusoidal reference waves for each phase.

The counter outputs are 9600 Hz and 4800 Hz square waves, which are falling edge synchronized. These signals are inputs to a D type flip flop which changes the 4800 Hz signal to be using edge synchronized.

The capacitor in series with the output of the D flip-flop removes DC content from the 4800 Hz square wave, and the op-amp integrator creates a +6 volt to -6 volt triangular wave from the square wave. The output of this op-amp circuit is fed to a unity gain inverting amplifier, which inverts the 4800 Hz triangular wave. These two triangular waves are inputs to voltage comparators shown in Figure A-3. The other output to the comparator is the reference 400 Hz sinusoid, altered as necessary by DC feedback. The action

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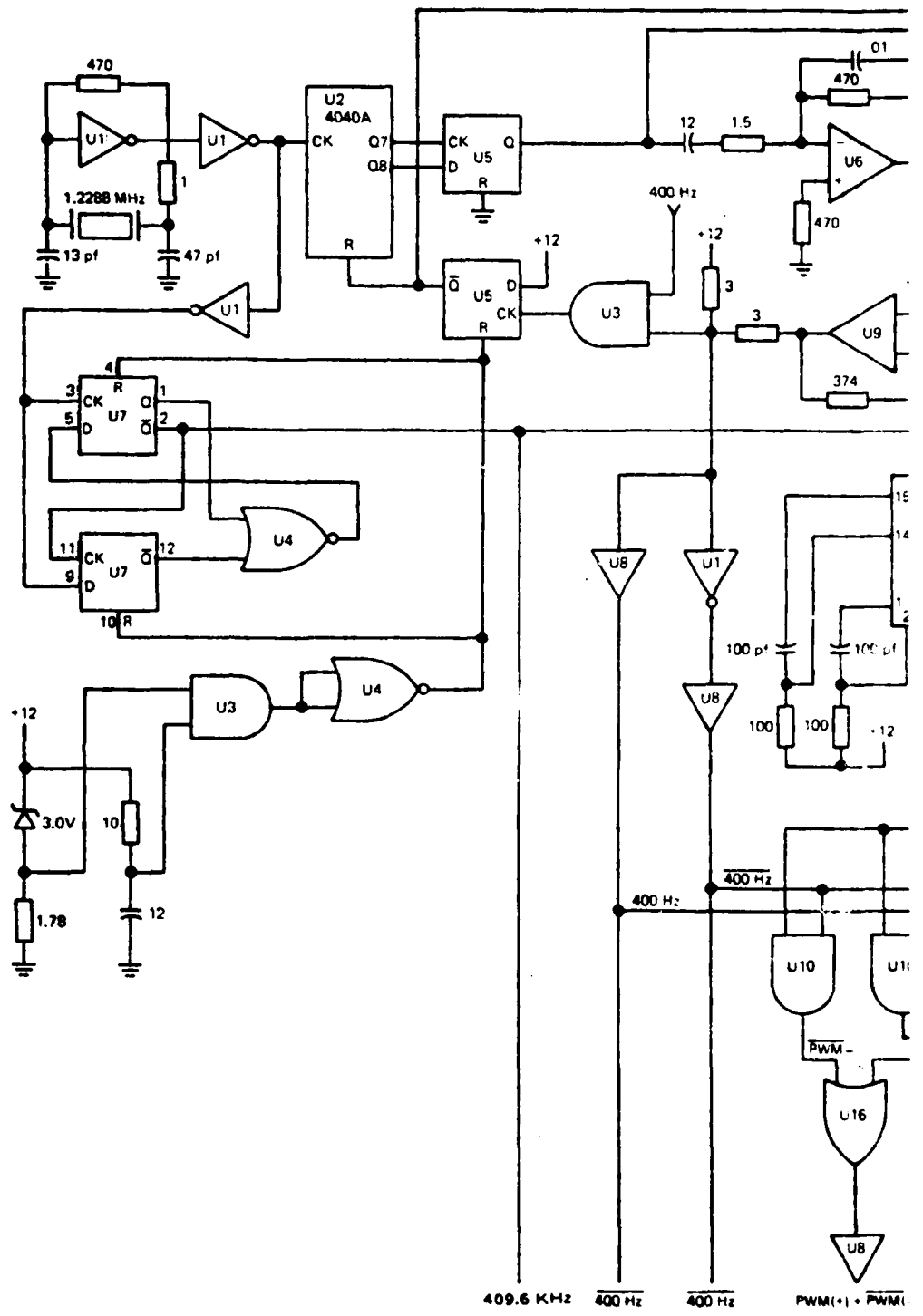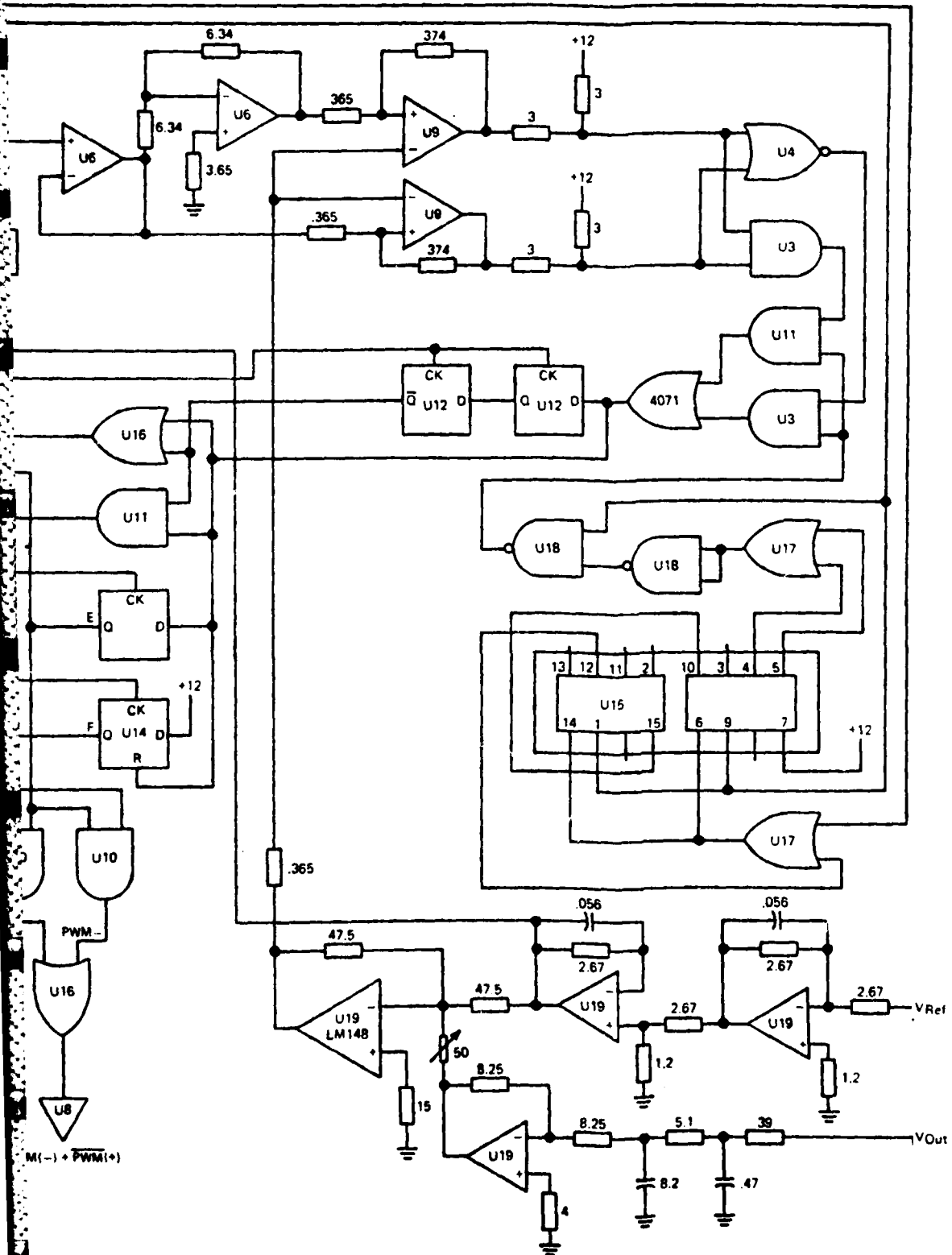
Figure A-1.
PWM CMOS Logic - Single Phase Ouptut

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This circuit produces logic level (12 volt) falling edges corresponding to
409.6 KHz. This output goes to the reference wave generator to be used to generate 400 Hz sinusoidal reference waves for each phase.
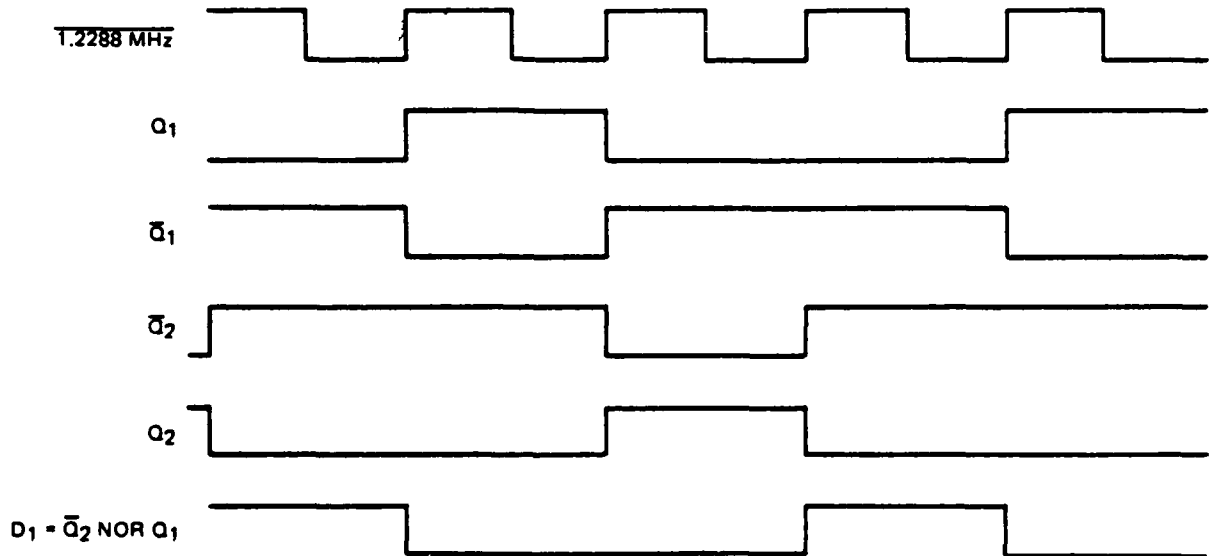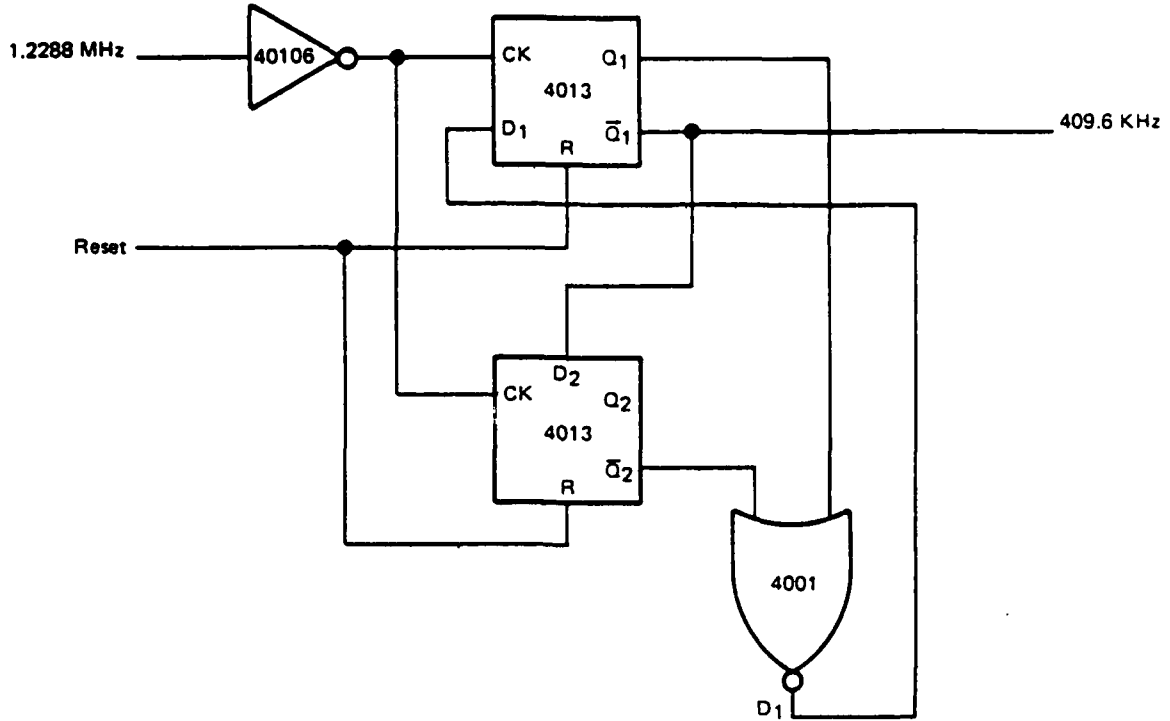
Figure A-2. Divide By Three Counter

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374KΩ

Carrier Wave

LM139 (A)

365Ω

Feedback Reference Wave

LM139 (B)

Carrier Wave **365Ω**

374KΩ

3KΩ 0 Volts

3KΩ

+12

3KΩ

3KΩ 0 Volts

4081 — Positive Half Cycle PWM

4001 — Negative Half Cycle PWM
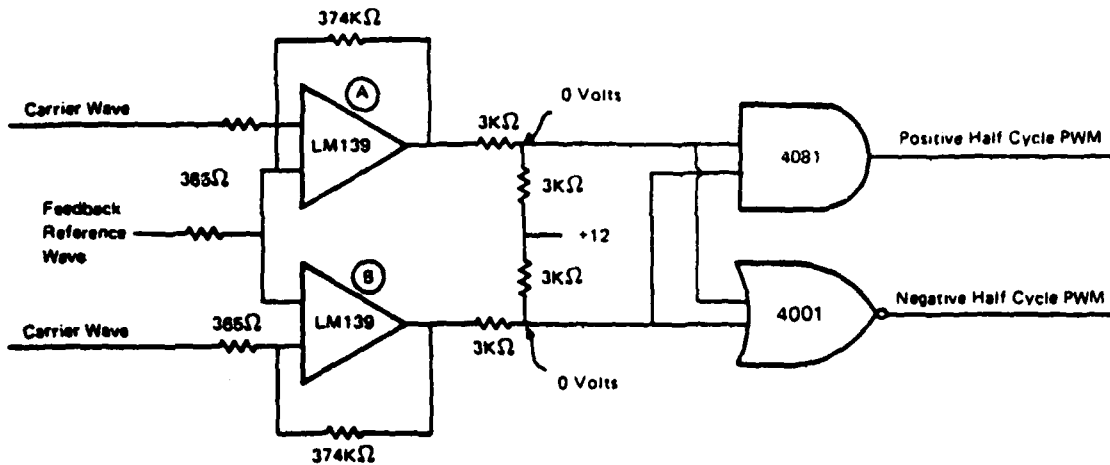
Sketch of Operation for Positive Half Cycle

0 Volts

Portion of Reference Wave

0 Volts

Output of Comparator (A)

Output of Comparator (B)

(A) and (B)

200mV   200mV

500mV   100µS

200mV   200mV

500mV   100µS

Figure A-3.   PWM Voltage Comparators

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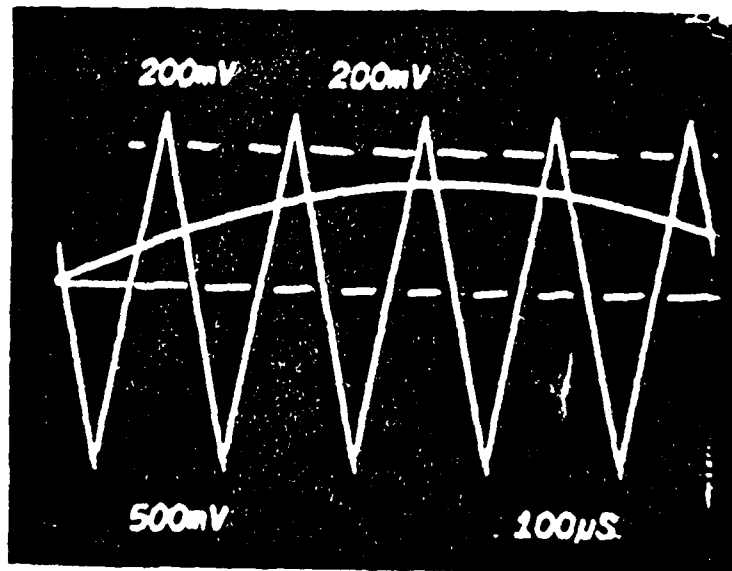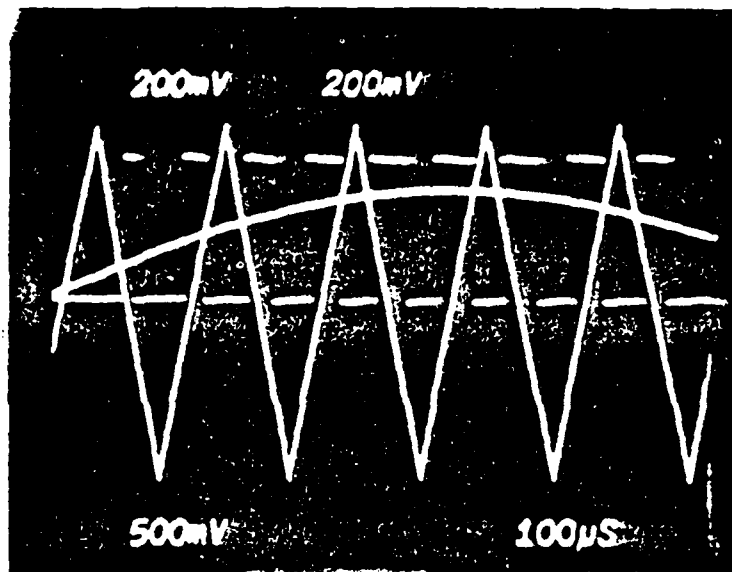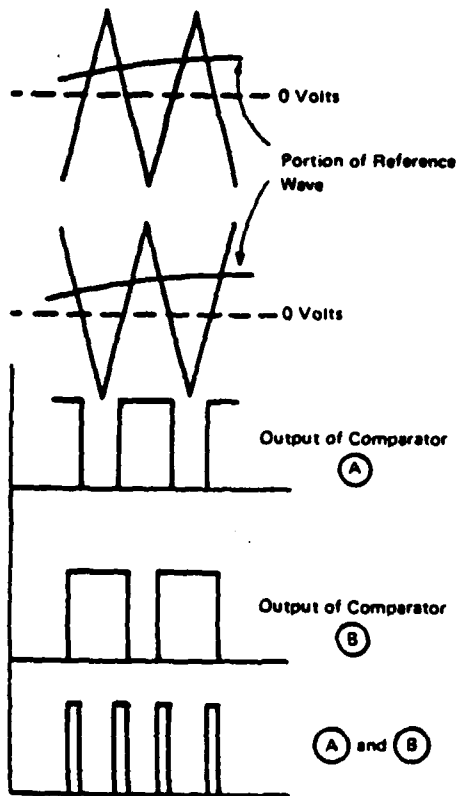of the LM139 is to produce a +12 volt signal when the triangular wave voltage is greater than the reference, and a -12 volt signal when the reference voltage is greater than the triangular wave voltage. The 3KΩ resistors connected to the outputs of the two LM139 voltage comparators act to make the LM139 outputs either 0 or +12 volts, rather than -12 or +12 volts. These comparator outputs are combined in an AND gate to produce the positive half cycle PWM, and in a NOR gate to produce negative half cycle PWM. This action is shown in Figure A-3. A LM139 was also used to produce the 400 Hz and 400 Hz square waves by detecting the zero crossings of the 400 Hz reference wave.

Spurious voltage spikes at the output of the LM139 voltage comparators which were generated when the 400 Hz reference wave passed through zero were eliminated by the circuit shown in Figure A-4. This circuit ensures that the logic level PWM signals remain at zero volts for a period of 7.5 electrical degrees (52.1 μs) centered around the 400 Hz reference wave zero crossing.

Figure A-5 shows the reference wave filter and DC content circuit. The reference wave filter is necessary to eliminate high frequency noise from the reference wave prior to it being used to create PWM and zero crossing signals. The DC content feedback circuit minimizes DC in the output waveform by altering the positive and negative half cycle PWM waveforms via the reference wave. Referring to Figure B-1, Appendix B, if the volt-second product of the positive half-cycle PWM is greater than the volt second of the negative half cycle PWM, there will be a DC voltage is the same polarity as V_{BR} across the load. The DC feedback acts to increase the volt second product of the negative

half cycle PWM by subtracting a small DC voltage from the refer-
ence wave, effectively making the negative half cycle PWM pulses
wider.

Figure A-6 shows the time delay/complement circuit which generated
the PWM(+) or $\overline{PWM}$(-) and PWM(-) or $\overline{PWM}$(+) signals to turn the
Darlingtons Q_1 and Q_3 on and off in a complimentary fashion. A
time delay between pulses was necessary to prevent inadvertent
shorting of the DC link voltage. This time delay had to be
approximately 5 µs to ensure that the Darlingtons had time to
turn off. The timing diagram for this circuit (Figure A-7) shows
how the waveforms are generated. The waveforms E and F in Fig-
ure 8 are complements of each other, with time delays inserted.
The AND and OR gates in Figure A-7 are used to generate the
required signals which are then sent to the base drive circuits.

This completes a discussion of the original CMOS logic circuit.
See Appendix B for a discussion of fourier analysis techniques
applied to a pulse width modulated waveform.
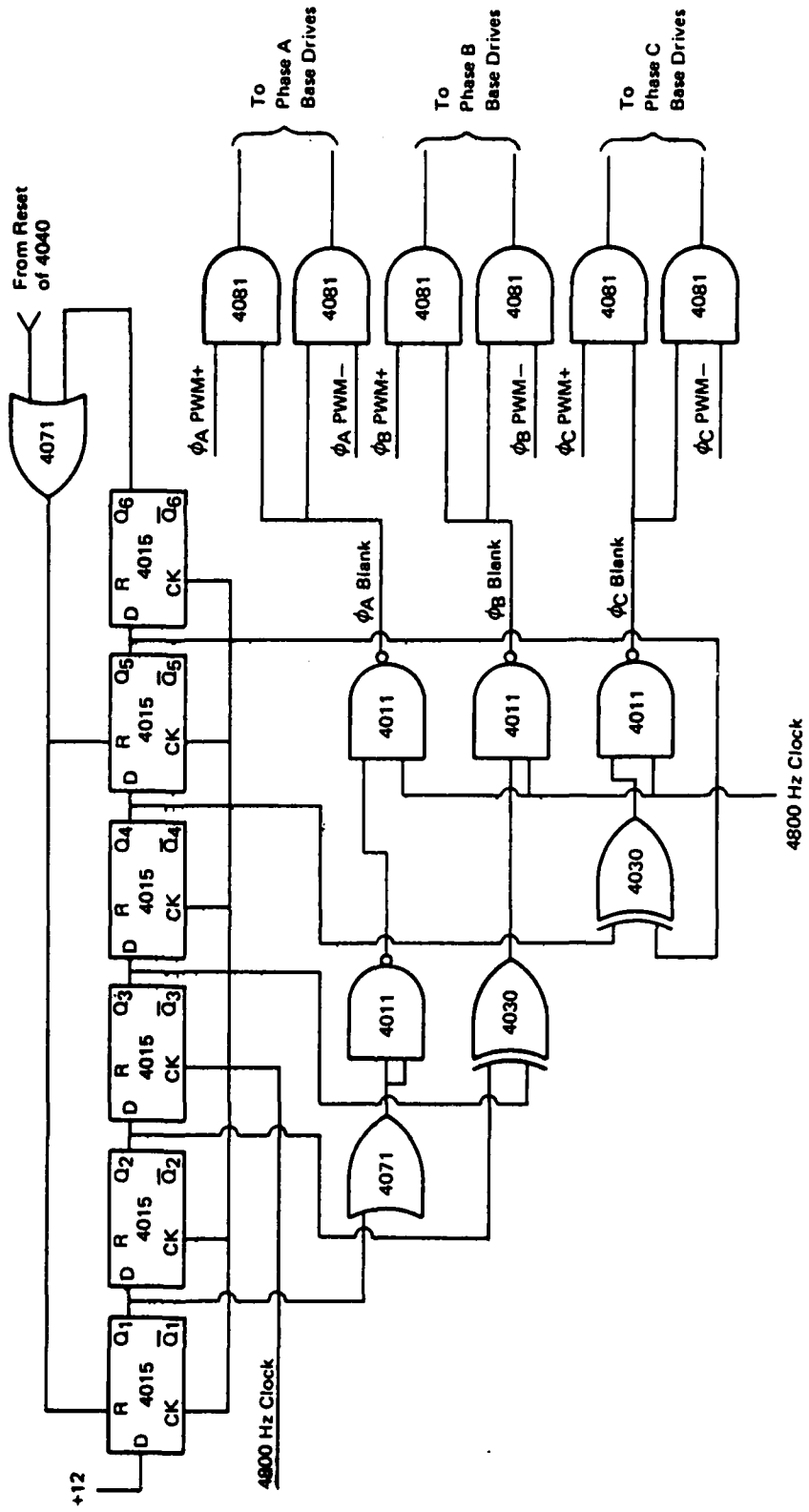
Figure A-4. Voltage Spike Blanking Circuit

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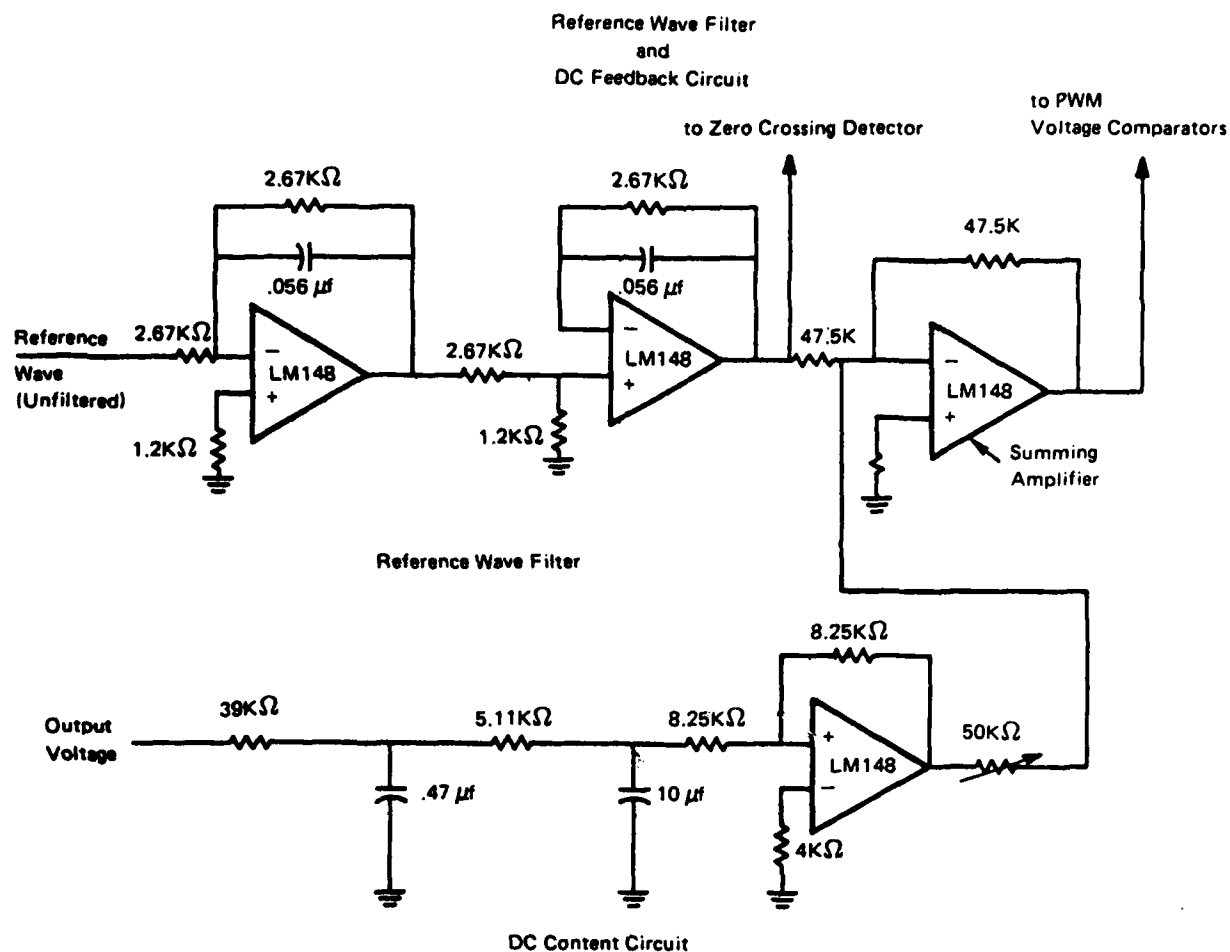
Figure A-5. Reference Wave Filter and DC Feedback

The Reference Wave Filter is a double polefilter with a break frequency of 1064.4 Hz. This filter produces a "clean" reference for the zero crossing detector and the summing amplifier. The DC content circuit has two break frequencies, one at 8.68 Hz, the other at 3.11 Hz. This circuit produces a DC level proportional to the DC level in the output voltage. This DC level is summed with the "clean" reference wave and the output of the summing amplifier is used to produce PWM waveforms which are altered to eliminate dc in the output voltage.

Figure A-6. Complement Circuit

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Figure A-7. Complement Circuit Timing Diagram

Appendix B
FOURIER ANALYSIS OF PWM WAVEFORM

Harmonic analysis of the pulse width modulated output voltage
waveform confirmed that the majority of the harmonic energy is
located near the carrier wave frequency. The harmonic spectrum
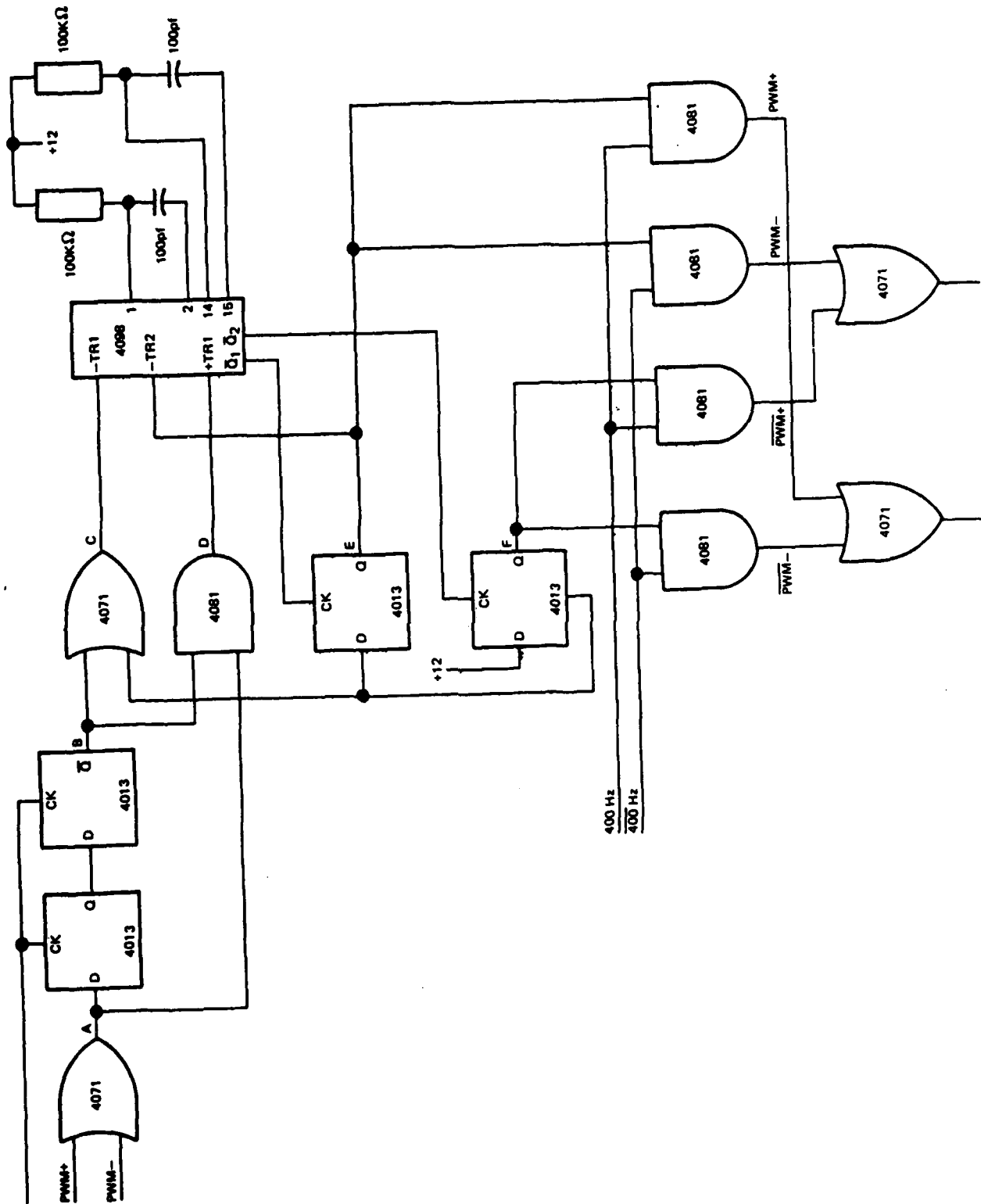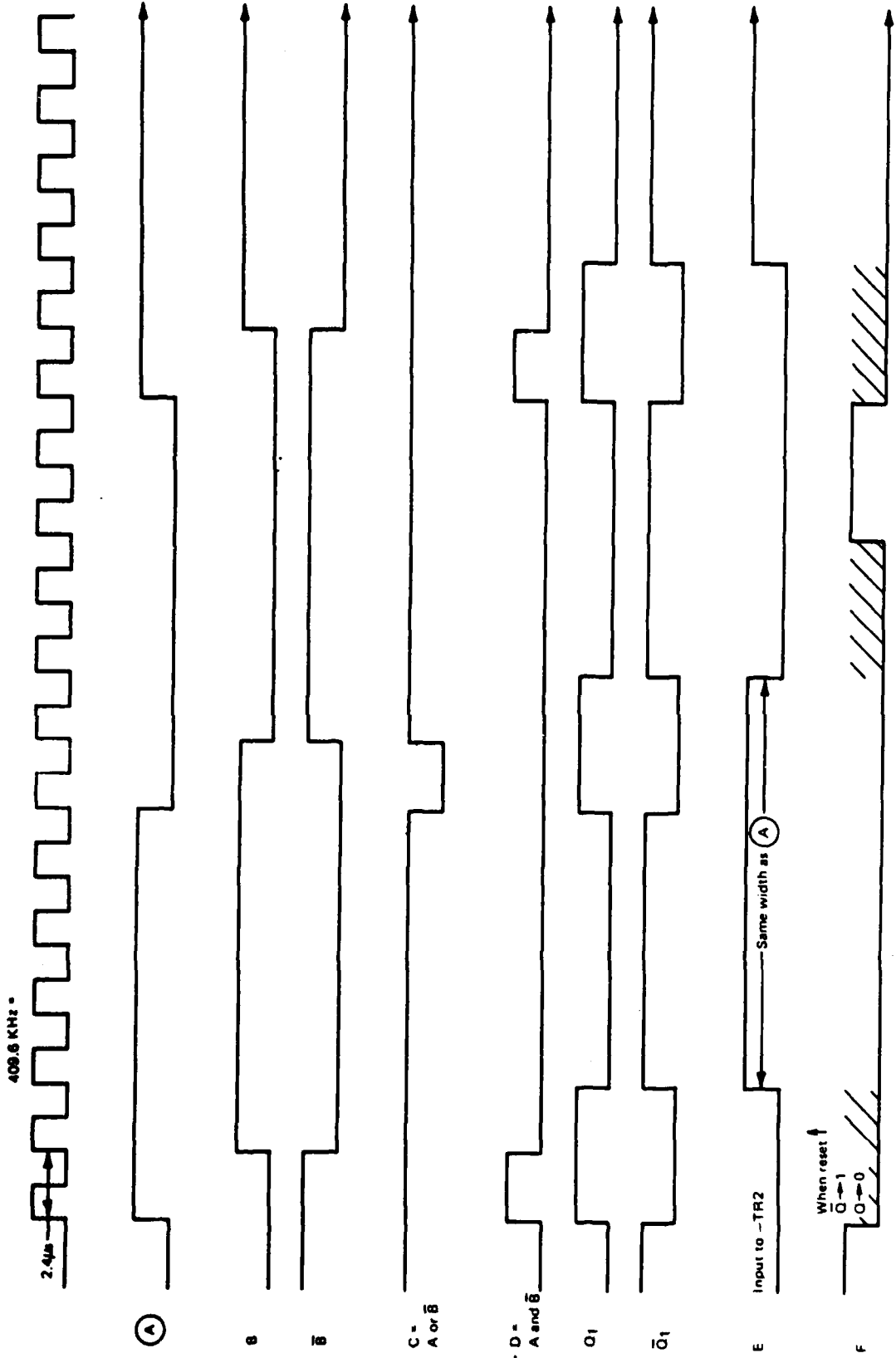also varies as a function of the modulation ratio, defined in
equation (1).

$$\text{Modulation Ratio} = M = \frac{\text{Peak Voltage of Sinusoidal Reference}}{\text{Peak Voltage of Triangular Wave}}$$

(1)

Possible values of M range from 0 to ∞, with practical opera-
tion being confined to $0 < M < 1.0$. To determine the harmonic
content of the PWM voltage waveform, the intersection points
(or firing of angles) of the carrier wave and reference wave must
be determined. This can be done by solving equation (2) for pos-
sible values of t (in μs) or ωt (in degrees of radians).

$$V_{ref} \sin \omega t = A\omega t + B$$

(2)

$$\omega t = 2\pi(400) \text{ rad/sec}$$

The coefficients A and B are the slope and y intercept of the
triangular wave carrier, referenced to a y-axis at the zero
crossing of the reference wave.

Referencing Figure B-1, the PWM waveform is quarter and halfwave symmetric, so there is no DC component (ideally) and no cosine components in the Fourier series (again, ideally). In terms of a general Fourier series $f(t)$, equation (3), $a_0 = 0$, and

$$f(t) = \tfrac{1}{2} a_0 + a_1 \cos \omega t + a_2 \cos 2\omega t + \ldots \qquad (3)$$
$$+ b_1 \sin \omega t + b_2 \sin 2\omega t + \ldots$$

$b_n = 0$, leaving only the coefficients of the sine terms to be nonzero. In addition, since the PWM wave has half-wave symmetry, there will be no even harmonics in the output spectrum. Considering that $f(t)$ in equation (4) is either V_{DC} or 0, if the firing angles are known, equation (4) becomes a trivial integral, whose solution is equation (5).

$$a_n = \frac{1}{\pi} \int_0^{2\pi} f(\omega t) \sin n\omega t \, d\omega t \qquad (4)$$

$$a_N = \frac{4 V_D}{N\pi} \left[\sum_{m=1}^{6} \cos \theta_{2m-1} - \sum_{m=1}^{6} \cos \theta_{2m} \right] \qquad (5)$$

The variable N is the harmonic number, and the variable m designates the firing angle (see Table I).

Table II shows the harmonics of a PWM waveform with 24 firing angles per half cycle (9600 Hz carrier wave frequency). The results of this table show that no appreciable harmonics exist until the 21st harmonic (8400 Hz) is reached. The 23rd, 25th and 27th harmonics are also high, but after filtering they are reduced to below 1% of the fundamental.

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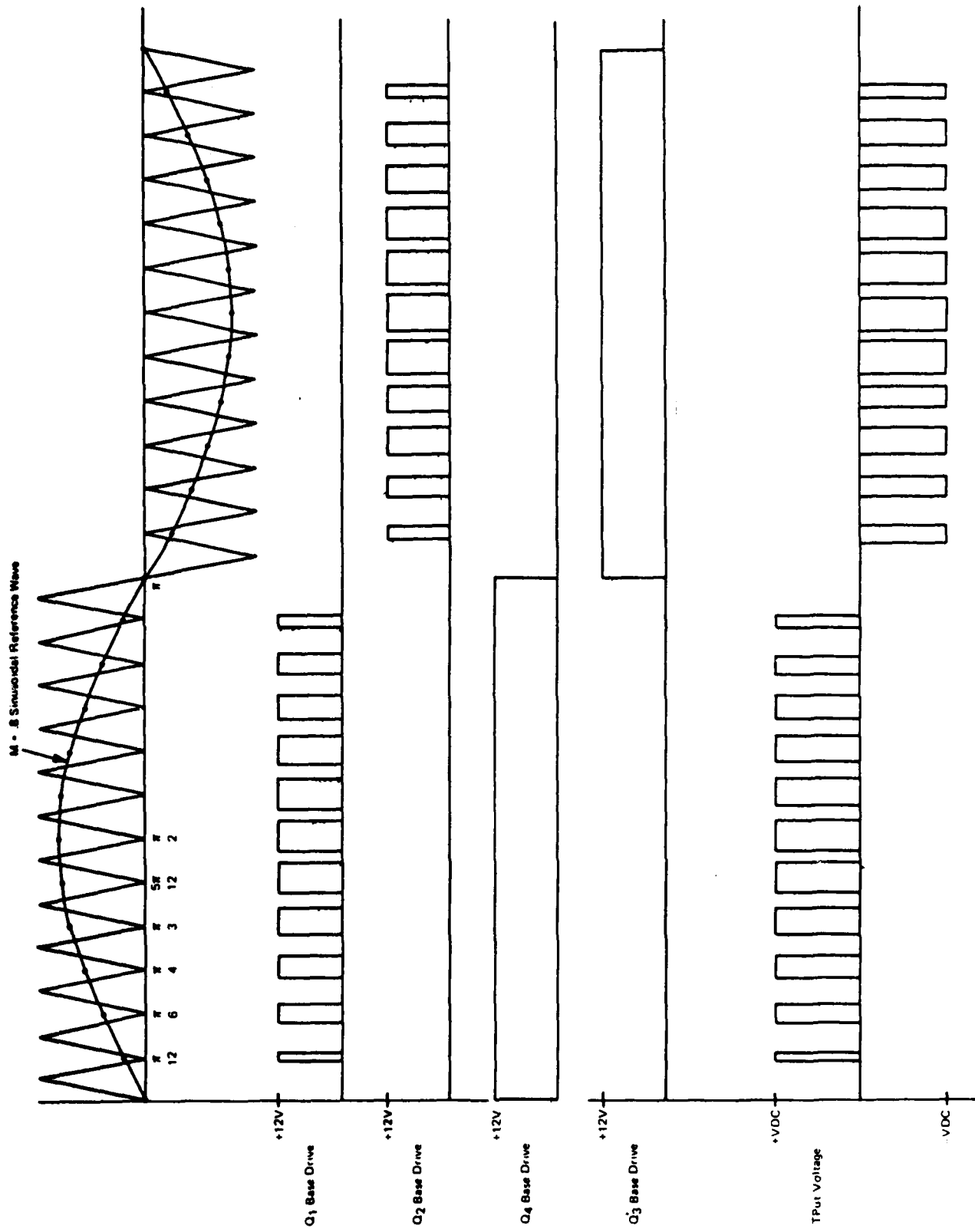
Figure B-1. PWM Waveform

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TABLE I
FIRING ANGLES FOR PWM WAVEFORM
M = .85

	t (μs)	ωt (deg)
θ_1	94.8	13.65
θ_2	117.7	16.95
θ_3	198.5	27.15
θ_4	233.3	33.60
θ_5	284.4	40.95
θ_6	346.9	49.95
θ_7	381.3	54.90
θ_8	457.3	65.85
θ_9	480.2	69.15
θ_{10}	565.6	81.45
θ_{11}	581.3	83.70
θ_{12}	625.0	90.0

TABLE II

HARMONIC CONTENT OF PWM WAVE
M = .85 V_{DC} = 200.0V

N	V_N	V_N/V_{DC}	V_N/V_1	20 log V_N/V_1
1	169.80	.849	1.0	0
3	-.62	0	0	$-\infty$
5	.55	0	0	$-\infty$
7	-.66	0	0	$-\infty$
9	-.10	0	0	$-\infty$
11	-.41	0	0	$-\infty$
13	-.47	0	0	$-\infty$
15	.61	0	0	$-\infty$
17	-.64	0	0	$-\infty$
19	-2.90	.014	.0165	-82.1
21	-32.81	.164	.1937	-32.82
23	-55.10	.2755	.3245	-22.51
25	59.41	.2970	.3498	-21.00
27	30.83	.1541	.1815	-34.13
29	2.34	.0117	.0138	-85.66
31	0.06	0	0	$-\infty$

Appendix C

DARLINGTON PARALLELING STUDY

The Solid State Applications Operation (SSAO) of General Electric performed a study of the problems involved in paralleling ZJ504 Darlington transistors, since two or three Darlingtons in parallel would be necessary to support fault conditions based on a 40 KVA system rating, using the original configuration. The peak fault current for a 3 per unit (p.u.) fault through each leg of the bridge would be approximately 600 Amperes, far exceeding the rating of a single device. The ZJ504 has the capability of supporting 200 Amps continually, and 400 Amps for 100 μs. When two devices are placed in parallel, the ability which they show to share current can be shown by the coefficient M, derived in Figure C-1. When M is unity, each device would conduct half the total current flowing in one leg of the inverter bridge.

Assuming an M of 1.1 and a 3 p.u. fault current means that the peak current flowing through the device carrying 52% of the current is 312 Amps. This current is below the 400 Amp/100 μs criteria outlined above, but there is a 700 μs period in each cycle where currents in each device are above 200 Amps. It is this period which was of concern as to whether the device would handle the current requirements.

The manner in which SSAO tested for parallel operation was to use the circuits shown in Figures C-2 and C-3 to switch the devices at approximately 10 KHZ to evaluate both steady state and dynamic matching. The results of these tests were that 1) Dynamic matching did not appear to be as severe a problem as

originally thought and 2) 22.76 Kw at 280 volts DC was success-
fully switched.

However, during this testing, four devices were destroyed, each
failing due to an overvoltage condition. The first device to
fail (Serial Number 194) was exposed to an overvoltage condition
which stressed SN 199 also. Then, SN 199 failed when a snubber
diode failed, overstressing SN 197. Serial Number 197 failed
during a test where it was exposed to >500 volts, overstressing
SN 255, which then failed during increased power testing.
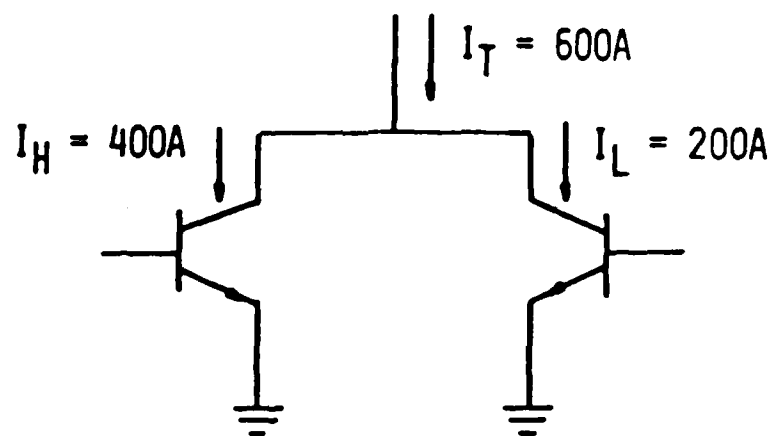
$$\text{FRACTIONAL MATCH} = \frac{I_H}{I_L} = M$$

THEN,

$$I_H = \frac{I_T}{\left(1 + \frac{1}{M}\right)}$$

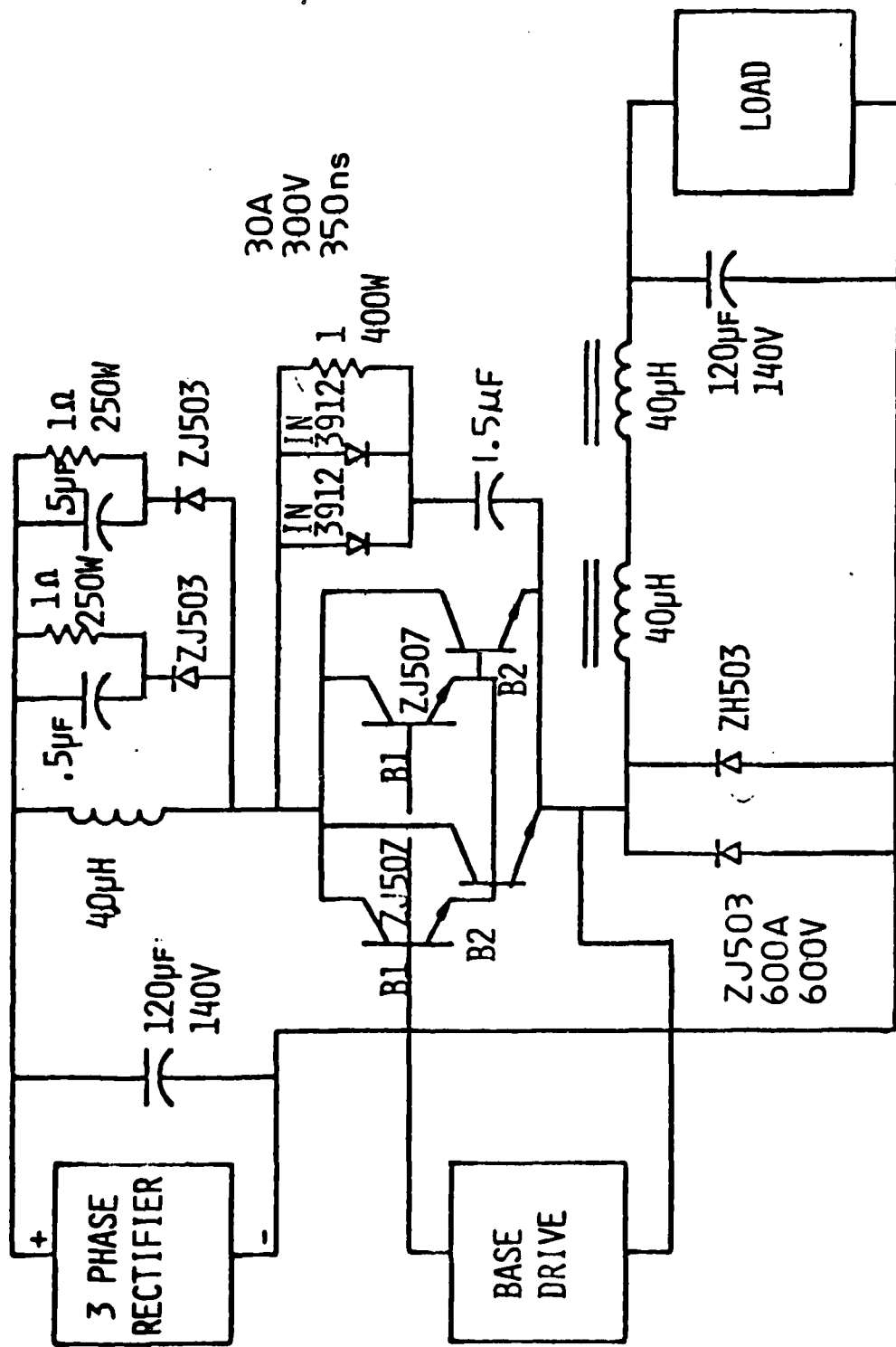Figure C-1.   Current Sharing and Matching Definition

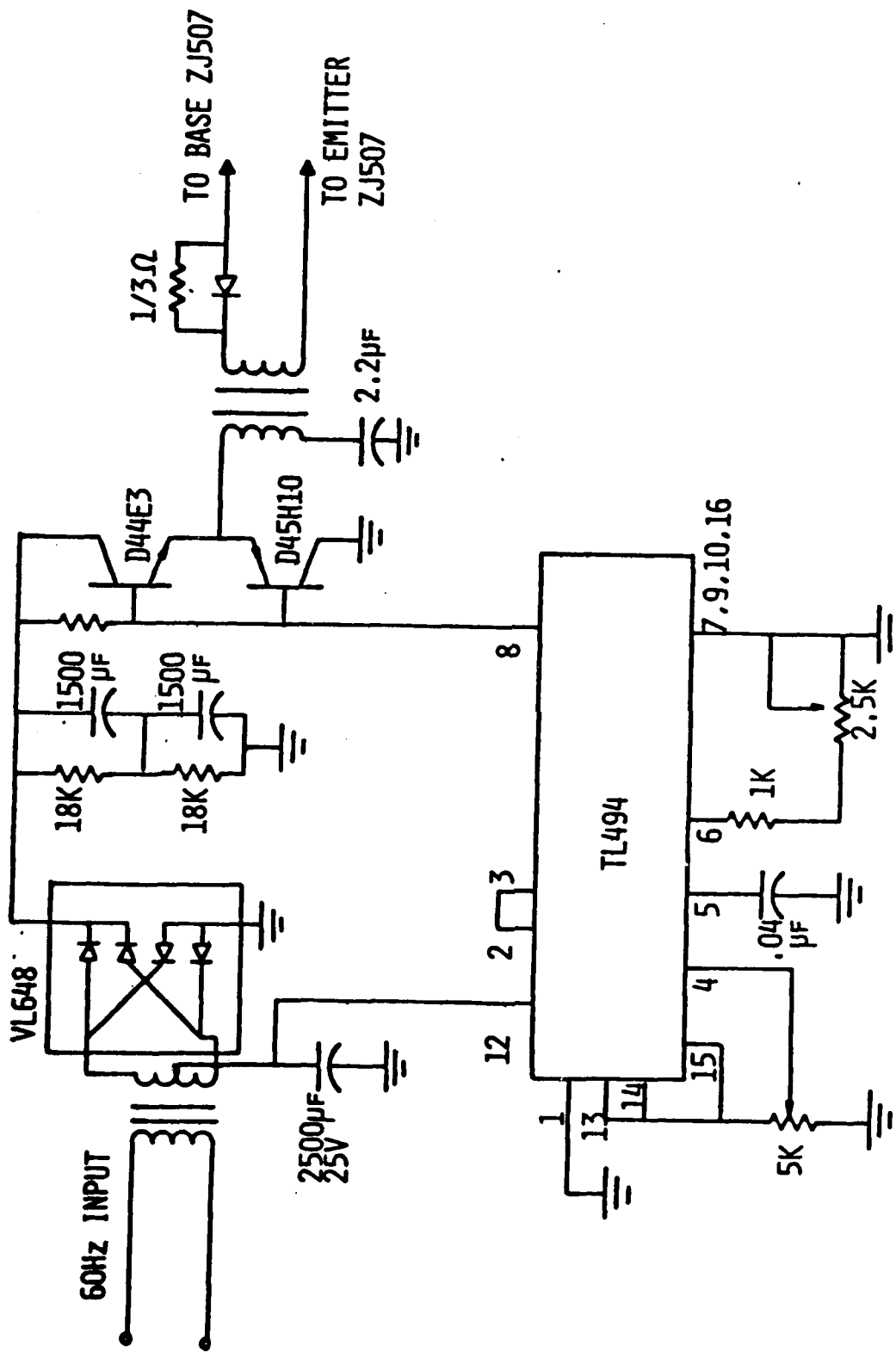Figure C-2. Switching/Paralleling Circuit

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Figure C-3. Base Drive Used by Solid State Applications Organization, General Electric Company

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Reference

1. "Supplying the Analysis of Harmonic Content in Complex Inverter Switching Waveforms," R.H. Lee, Proceedings of Powercon 8, 1981

END

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