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DEVELOPMENT OF SHORT GATE FET'S(U) HOWARD UNIV
WASHINGTON DC DEPT OF ELECTRICAL ENGINEERING
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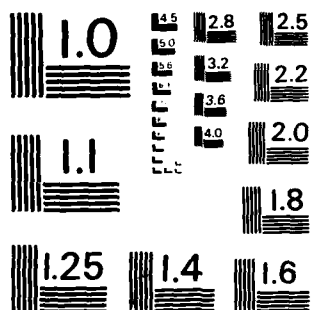
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) A summary of initial work performed under Air Force contract "Development of Short Gate Fet's" is presented. Approach taken toward fabrication of high speed fet's is discussed. Expected materials and fabrication problems are outlined.		

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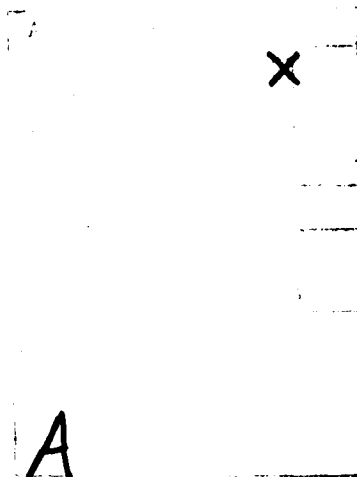
DEVELOPMENT OF SHORT GATE FET'S

Annual Report

Approved for public release;
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INTRODUCTION

This report is a summary of the activities that were performed under the contract "Development of Short Gate Fet's". Section one summaries the activities performed during the first six months and section two covers the second six months of the contract.



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MATHIAS, R.
Chief, Technical Information Division

SECTION ONE

In July 1980 work was initiated on sponsored research to look at short gate field effect transistors (fet's). In this section we will outline the approach we have taken to this research highlighting our accomplishments to date and present our plan for continuing work.

INTRODUCTION

The goal of this research is to extend the performance range of gallium arsenide (GaAs) field effect transistors to the submillimeter region ($f_c=40\text{GHz}$). To achieve these ends we propose to fabricate devices with electrical gate lengths less than .3 microns. Devices with electrical gate lengths this small are predicted to support electron velocities as high as $5 \times 10^7 \text{cm/sec}$.⁽¹⁾ This structure will be made by ion implantation into semi-insulating material (in our case a Cr doped buffer layer). This structure has several important advantages for our purposes.

First the electrical gate length of the device is equal to the metalurgical gate length of the device. Second, the source and drain (because of the heavy ion implantation) have negligible parasitic resistance. Third, since the structure is self-aligning a critical alignment step is eliminated. Fourth, the structure is accurately modeled since the contacts are planar and hence the fields are parallel and finally the heavily doped contact will provide the extra electrons needed for ballistic motion.⁽²⁾ As previously stated velocities of as high as $5 \times 10^7 \text{cm/sec}$ appears to be obtainable. Our goal is to see this high velocity reflected in increased dc and ac performance of our devices.

MATERIALS FABRICATION AND CHARACTERIZATION

Since the active region of these devices is becoming extremely small the requirements on the material are becoming more severe.

It is clear that the number of impurities and defects (such as dislocations) in the active region must be as low as possible. In addition there are problems which are unique to compound semiconductors. The most severe material problem is the lack of understanding of the substrate, for example impurities both shallow and deep can diffuse out of substrate into the active region. The substrate problem is complicated by the possibility of many types of crystalline defects which are uniquely present in compound semiconductors. For instance, in GaAs not only it is possible to have Ga vacancies and arsenic vacancies, but also Ga atoms on As atoms or vice versa.

To reduce the substrate problems we intend to grow a Cr doped buffer layer⁽³⁾ on our substrates by liquid phase epitaxy, (LPE). The advantages of the buffer layer are that it isolates the active layer from Cr diffusing from the substrate and is less susceptible to thermal conversion (after ion implantation). We are in the process of constructing a LPE reactor dedicated to the purpose of producing high quality LPE buffer lengths. To date the components for the system have arrived and construction has commenced. This system should be operational by the end of summer. In addition, a high quality graphite LPE "boat" has been designed and fabricated.

The ion implantation technique will be used to selectively dope our fet structures. The ion implantation will be done into the Cr doped buffer layers. A capless annealing system for annealing ion implantation damage has been constructed and is being characterized. Further we are working with the Naval Research Labs who are a large resource of experience in ion implantation and annealing of compound semiconductors.

As an alternative to ion implantation in the fabrication of the fet channel we intend to investigate the use of metal organic vapor deposition (MOCVD) to form the channel region. Some potential advantages of a vapor deposition channel are a uniform doping concentration (in the Z direction) and the elimination of possible defects introduced by ion implantation. The reason for choosing the MOCVD technique is that only low pressure MOCVD and MBE (molecular beam epitaxy) have the resolution to grow structures of these dimensions. Design and procurement of components for the MOCVD system has commenced.

We now have in our laboratory the capability to characterize materials by several methods, Hall mobility, CV measurements, photoluminescence, visual inspection (scanning electron microscope) and deep level transient spectroscopy.

DEVICE FABRICATION

The fabrication of fet's of these dimensions require solution of many important problems. During the course of the previous contract period we have identified the problems which we consider to be important and intend to concentrate on them during the next reporting period.

A. Lithographic Consideration

In order to reproduce dimensions of less than $.5\mu\text{m}$ there are only three possible lithographic systems capable of doing this; electron beam lithography, x-ray lithography and deep uv lithography. This system is presently being set up. In addition we have obtained permission to use the National Submicron Facility and we have begun fabrication of a mask set compatible with the deep uv system to be delivered. (The mask set is being fabricated by e-beam techniques.) At summer's end we intend to have developed our photo resist processing to be able to obtain submicron lithography.

B. Gate Construction

The gate construction of this device is a key issue. In this construction several things must be accomplished. It must act as an ion implantation annealing cycle (for self-aligned structures) and it must provide enough cross-sectional area for the parasitic gate resistance to be low. To achieve the last requirement we will pursue the T structure geometry. See figure 2. "High T" will achieve a low parasitic resistance and the "wings" of the T will act as an implantation mask. We intend to investigate the use of a silicide as a component in the fabrication of this gate to allow it to withstand the high temperature annealing cycle.⁽⁴⁾

C. Space Charge Limited Current

As the dimensions of the structure come closer and closer the combination of space charge limited current to the parasitic current of the device is increased. Since space charge limited current varies as $v^{\frac{3}{2}}$ ⁽⁵⁾ it can be expected to become dramatically important as the dimensions are decreased. We are investigating space charge limited current in parallel with investigating the lateral diffusion of ion implantation in GaAs. To do this we are fabricating test devices. The test devices consist of the source and drain implants produced on a substrate without a channel layer. We have fabricated 1 um and 2 um versions of these test structures and the data appears to be consistent with theoretical predictions lateral diffusions.

We are fabricating these devices by ion implantation at gate dimensions of .5um or less diffusion of the ion implanted species. This becomes an important limitation of how close the contacts might be spaced apart. As mentioned above we are using test structures to investigate this problem.

DEVICE PHYSICS

We are working with Lester Eastman of Cornell in order to understand the physics of electron transport in short dimensions. We believe that it is possible to achieve electron velocities of 5×10^7 cm/sec in these.⁽¹⁾ We intend to investigate what are the optimum geometrical parameters of these devices.

SUMMARY

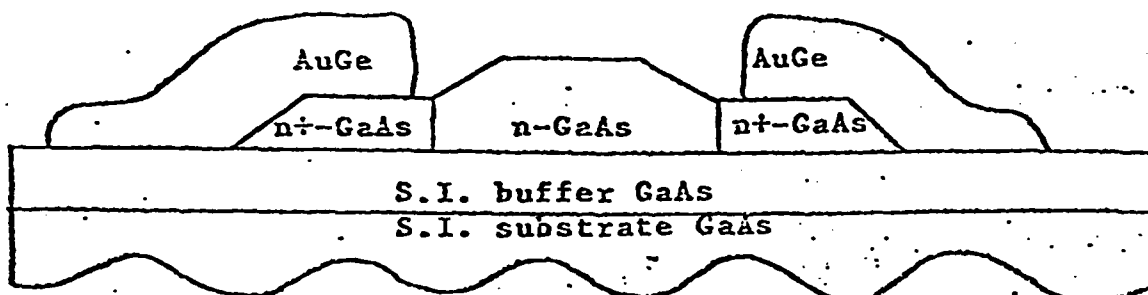
We have commenced research on extending the operation frequency of fet's. We believe that because of transient electron transport effects the electron velocities can approach 5×10^7 cm/sec. The role of space charge limited current in these dimensions appear to be an important one and experiments investigating these currents have commenced. In order for these devices to operate properly crystalline defects and impurities must be eliminated. This seems to indicate the epitaxial techniques of materials fabrication must be used. We will investigate direct implantation into LPE Cr doped buffer layers for both channel and drain-source regions as well as implantation into V.P.E. material for only the drain-source region.

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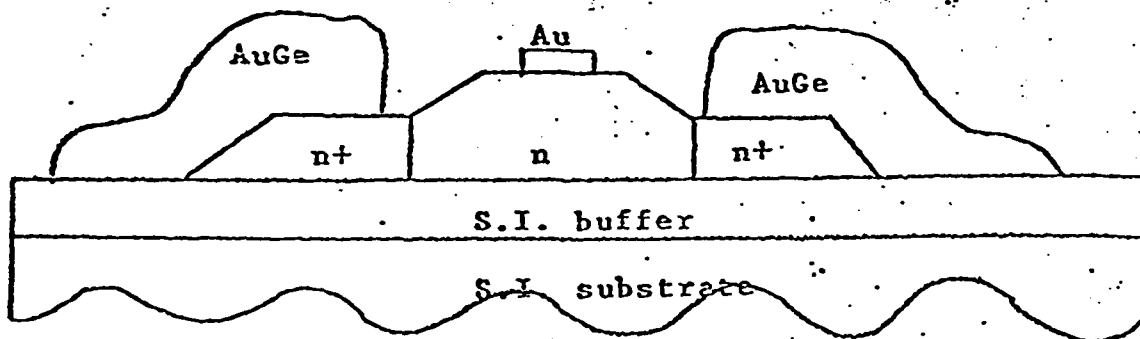
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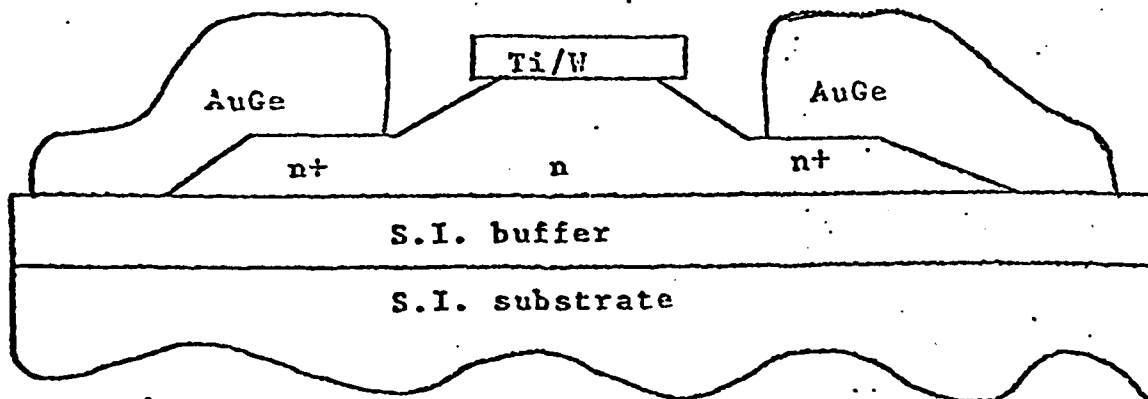
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(a) gateless MESFET



(b) realigned gate MESFET



(c) self-align gate MESFET

Figure 2

SECTION TWO

During this period we were able to obtain our deep uv photolithography system. Also during this period a test pattern was fabricated for us by the National Submicron Center. Initial results using this test pattern are shown in Figure 1. In addition we have fabricated a first generation mask set in "thick" quartz for our fet's. We were able using the facilities of the National Submicron Center to realize in chrome line widths of as small as .22 micron by wet chemical etching. This result was considered surprising since at first it was thought that the lateral undercut of the wet chemical etch would limit the line width to a larger value.

Materials growth is an area in which we have made strides during the past year. We have completed fabrication of a high purity LPE reactor (shown in figure 2). This reactor has several important features including a nitrogen purged glove box and UT-6 ultra carbon high purity boat. This reactor will be dedicated to the growth of high purity buffer layers for implantation; these buffers being either undoped or Cr doped. In order to compliment our liquid phase epitaxial system as well as to provide large areas of material we are in the process of completing construction of $AsCl_3$ reactor (shown in Figure 3). This reactor will be used to develop large area Cr doped buffer layers. This system should be operational within the next month.

Concurrent with the aforementioned work we are continuing construction of a MOCVD System. This system will allow us to investigate modulation doped structures. In the case of the MOCVD System all components have been ordered and major components have begun to arrive. Construction should be completed in time for the system to be utilized during the last year of this work.

During this year we have completed construction and calibrated our photoluminescence system. This system will be useful in characterizing our material after growth and after annealing.

We have been refining our device fabrication technology on standard dimension fet's (one and two micron). We have added O_2 plasma etching to our standard fabrication step as well as refined our cleaning step prior to metallization. Results of dc characterization of our fet's appear in Tables I and II. The best results of our mixer diode's appear in Table III.

Finally during this year we have spent a considerable effort in trying to understand lateral diffusion. However we have no conclusive results due to the complications introduced by substrate effects.

During the next year of the program our first priority is to complete development of the deep uv process. Others have successfully used this technique down to dimensions of .5 microns. We would like to see if by use of thin quartz (conformal techniques) that this experimental resolution limit can be extended. Concurrent with this we will develop the processing necessary to produce the "T" structure gate. This "T" structure is necessary to separate the highly doped contact from the gate region and prevent premature breakdown. By using various etching steps we should be able to get the base of this "T" to a dimension below .3 micron.

We now have two materials systems available to provide the base layers for ion implantation (LPE,VPE). During this current year we intend to fully characterize these layers before and after the annealing process.

In connection with the annealing process we will continue to investigate the effect of lateral diffusions. We will implant into substrates masked with lines of various widths and then check for electrical conductivity after anneals of various times and temperatures. In this way we will wish to ascertain the following, lateral struggle during implantation and lateral diffusion after annealing. We will also see if there is a surface diffusion component to process.

Finally we wish to fabricate fet's with gate dimension less than .5 micron and measure the dc and rf parameters and determine if there are any velocity enhancement effects. We intend to do this work with standard fet doped structures as well as modulation doped structures. We will, if time permits, investigate novel ohmic contact schemes for reducing parasitic resistances.

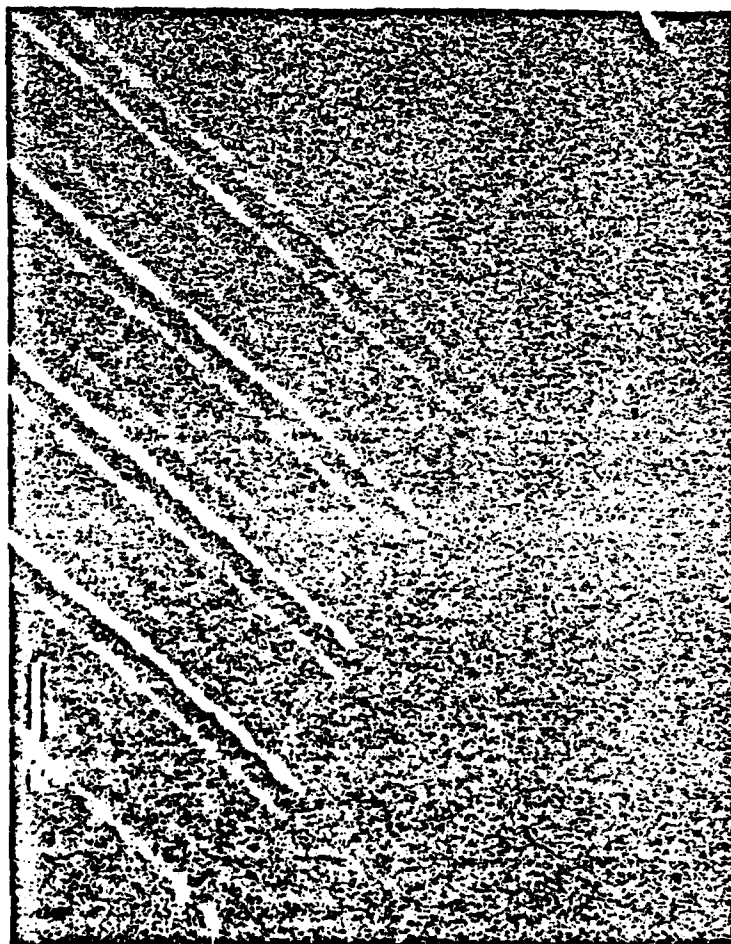


Figure 1
Photograph of lines produced in photo-resist by
Deep UV system. Large line is one micron.

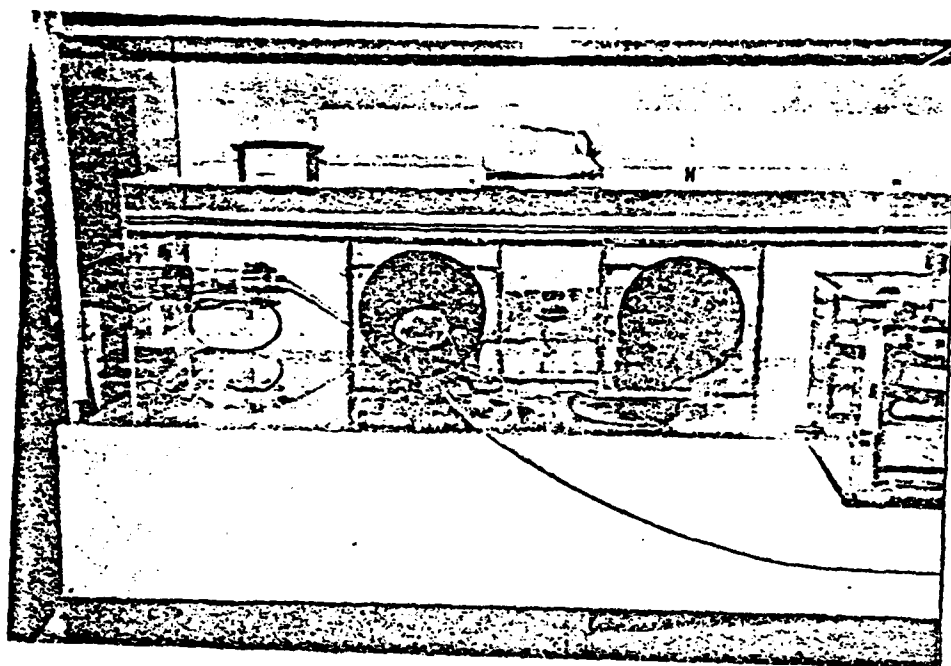


Figure 2
Photograph of High Purity L.P.E. System

TABLE 1

RESULTS OF DC TESTS ON GaAs MESFET

	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅
<u>Measured</u>					
Ideality Factor n	1.008	1.176	1.344	1.092	1.512
Built-in Voltage V _b (v)	0.857	0.891	0.842	0.792	0.857
Pinch-off Voltage V _p (v)	2.0	2.0	2.0	2.35	4.8
Terminal Pinch-off Voltage V _p (v)	2.857	2.891	2.842	3.142	5.657
<u>Parasitic Resistances *</u>					
Source R _s (Ω)	31.5	32.0	40.0	34.5	30.5
Drain R _D (Ω)	18.5	20.0	20.0	24.5	25.5
Transconductance g _m ($\frac{ms}{mm}$)	122.45	87	96.2	92.55	73.16
** Zero-Gate bias Current I _o (mA)		8.12	9.6	9.9	8.0
Max Channel Current Current I _m (mA)		17.0	17.5	18.8	30.0
<u>Calculated</u>					
Thickness a (μm)	0.2	0.2	0.2	0.21	0.28
Max Channel Factor		0.26	0.263	0.268	0.449
Fully open sat. Current I _s (mA)		65.38	66.54	70.15	66.8

* Measured using one-half of device

** Calculated assuming both halves device draw same current (X2 measured current)

TABLE II

THEORETICAL DC PARAMETERS

	I	II	III
V_b (V)	0.766	0.766	0.766
W_b (V)	2.89	3.19	5.67
V_p (V)	2.124	2.424	4.904
I_s (mA)	67.2	70.56	94.08
I_m (mA)	47.52	41	30.1
$*R_s$ (Ω)	10	8.88	8 18
I_o (mA)	9	10.1	27.86
g_m ($\frac{m}{mm}$)	89.3	86.03	78.56

* Resistance calculated for source side only
(drain approximately identical)

Assuming:

$$a_1 = 0.2\mu$$

$$a_2 = 0.21\mu$$

$$a_3 = 0.28\mu$$

$$N = 10^{17} \text{ cm}^{-3}$$

$$Z = 0.15 \text{ mm}$$

$$L = 2.4\mu \text{ (effective gate length)}$$

TABLE III

Schottky-Barrier Diode Performance Parameters

$$R_s = 9\Omega$$

$$C_o = .016 \text{ pF}$$

$$F_{co} = 1100 \text{ GHz}$$

$$\eta = 2.5$$

$$V_R = 5V \text{ at } 10\mu A$$

$$A = 4(\mu)^2$$