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F19628-80-C-0205

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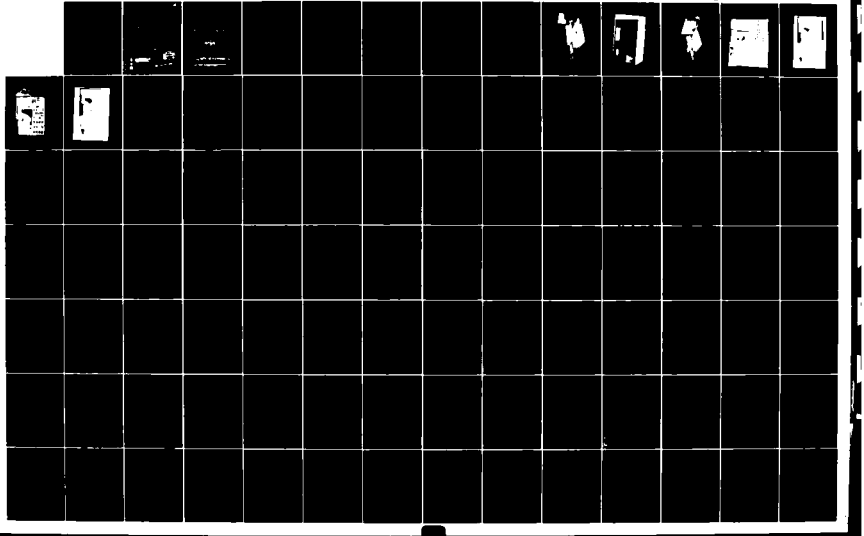

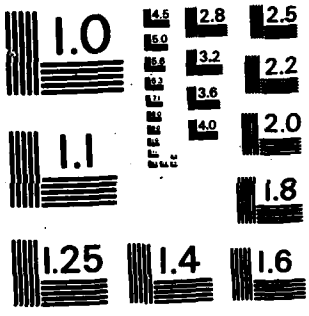

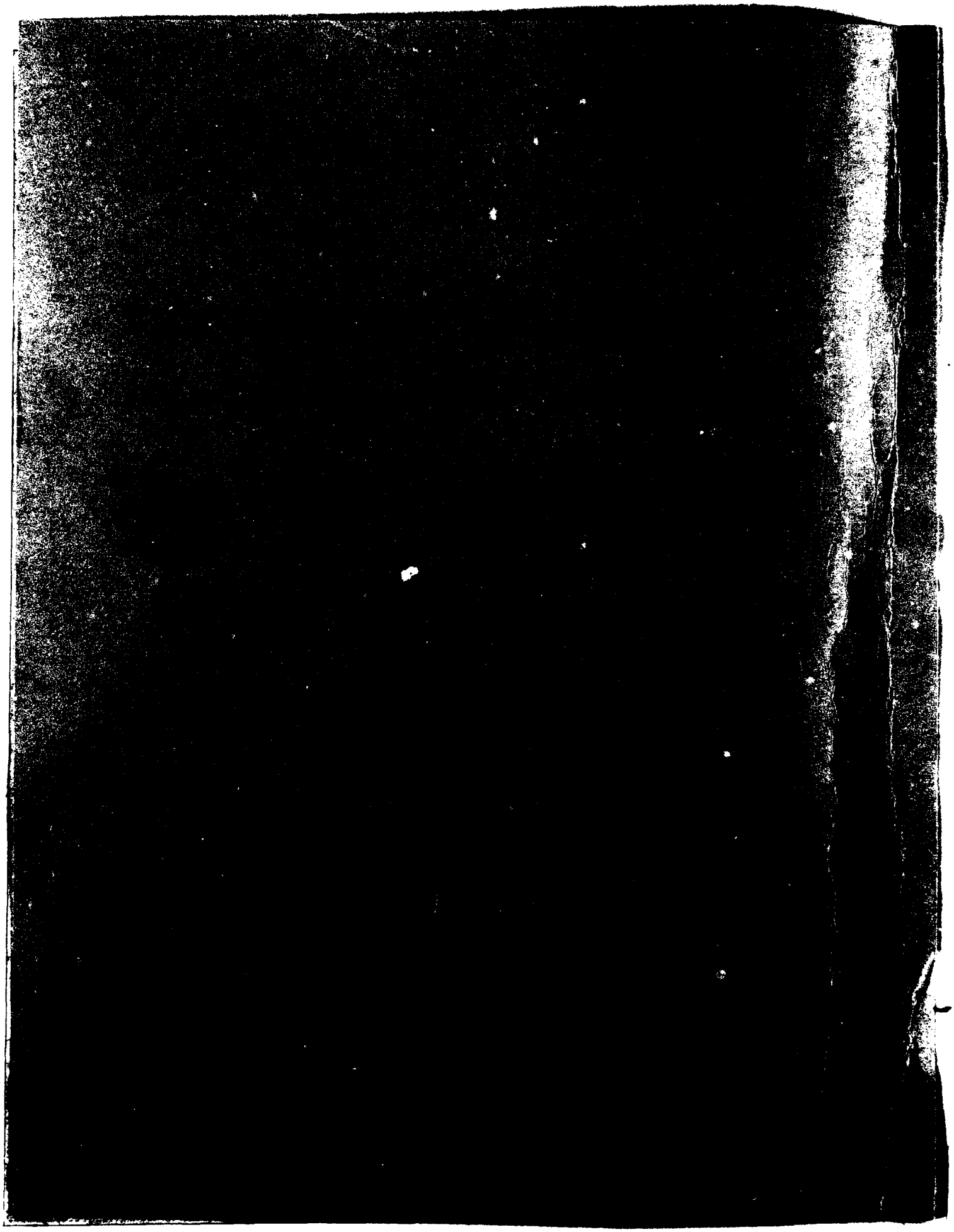

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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Spacecraft charging
Proton spectra
Electrostatic analyzer
Microprocessor instruments

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A multichannel proton electrostatic analyzer has been developed to monitor spacecraft charging by observing changes in the energy spectrum of the proton flux incident on the spacecraft. The analyzer uses electrostatic deflection plates to select incident ions within each energy band for detection by a channel electron multiplier. Command, control, input and output channel and mode selection, count accumulation, and processing are provided by a microprocessor under firmware control from replaceable programmable memories.

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CONTENTS

FIGURES

1. INTRODUCTION

The phenomenon of discharging among elements of spacecraft was first noticed in the late 1960s in causing upsets and permanent damage in electrically sensitive vehicle systems. Space objects undergo differential charging due to variations in physical properties among their surface regions. The rate and severity of the potential excursions depend on particle and photon environments present, and have beer described in Reference 1.

Integral charging, whereby the whole satellite is net negative with respect to the surrounding plasma, was measured first on ATS-5 (Ref 2) as a modification of the ion spectrum, noticeable as an acceleration to higher energies. Differential charging occurs when surface elements attain various voltage levels. These conditions are frequently relieved by "flashover" arcing, which results in system transients induced from the high surface currents. Differential charging may be reduced by attempts to ensure that the vehicle surface has uniform conductivity. Spacecraft systems may be made resistant to transient threats by robust design and by electrical protection at entry points.

The initial charging process may be reduced in severity by emission from the vehicle of an appropriate amount of electrons, ions or plasma. The search for an accurate method of assessing the potential condition is being pursued currently. A promising candidate is the continuous monitoring of the ion energy spectrum incident on the spacecraft. The voltage excursion is usually negative, due to the likelihood of higher fluxes of electrons compared to those of ions. Such a condition becomes exaggerated when the satellite is not illuminated by photoelectron-producing sunlight. Theoretically, knowledge of the ion spectrum, precise in intensity with respect tc energy and time, allows an accurate estimate of total excess charge present and hence the spacecraft voltage below the surroundings.

The present instrument attempts to provide a low-cost solution to these requirements. Its design affords a great deal of flexibility in choice of energy ranges, channel widths, dynamic range and number oi energy channels.

This versatility is derived from two features of the design:

1. Electronic functions are controlled by a microprocessor whose firmware is contained in four replaceable programmable memories.

2. Mechanical parameters of the analysis and detection system may be varied.

The components of the instrument are readily accessible. In the two flight models, all components are at the first level of reliability above commercial grade wherever such were available.

The microprocessor basis of the instrument logic provides, apart from adaptability in scientific application, compatibility with other such systems and with computer control in a more complex architecture. These final design versions are a significant technical advance beyond the concept envisaged in the RFP, IRT proposal and the R&D Design Evaluation Report (Ref 1) associated with this project.

The spectrometers are shown in both open and closed form in Figures 1.1 through 1.7.

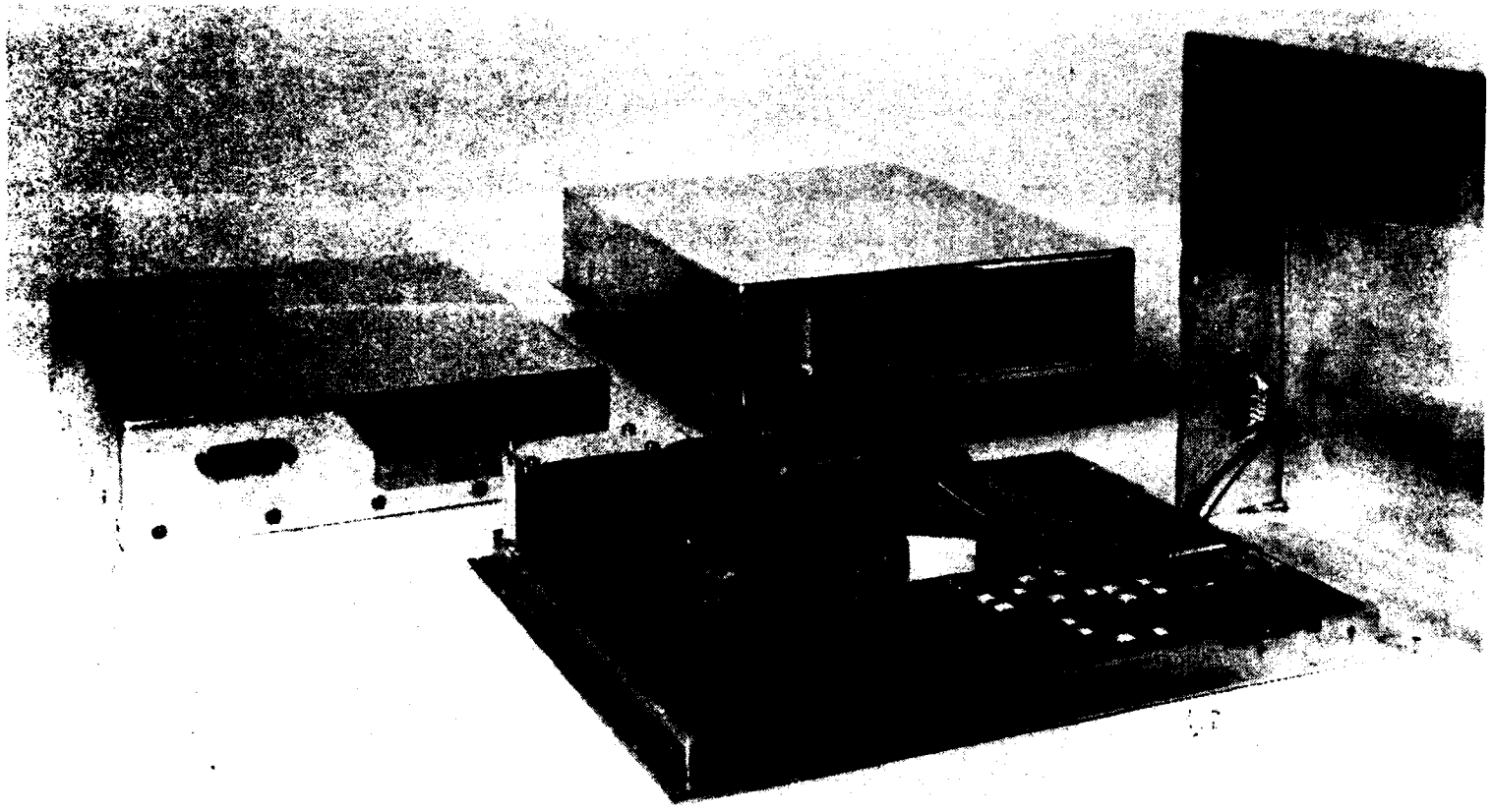

Figure 1.1. Prototype and flight model analyzers

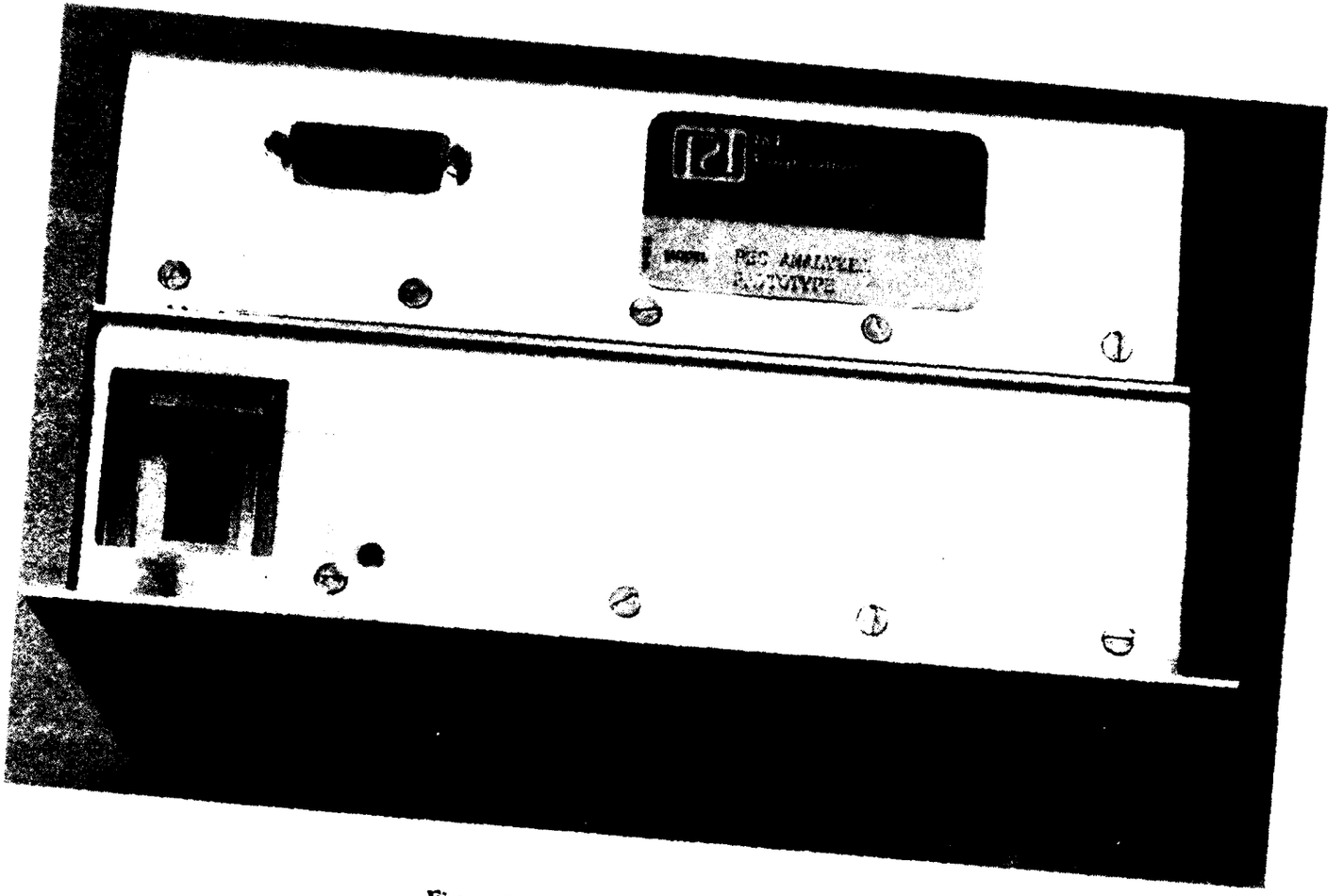

Figure 1.2. Front and rear views

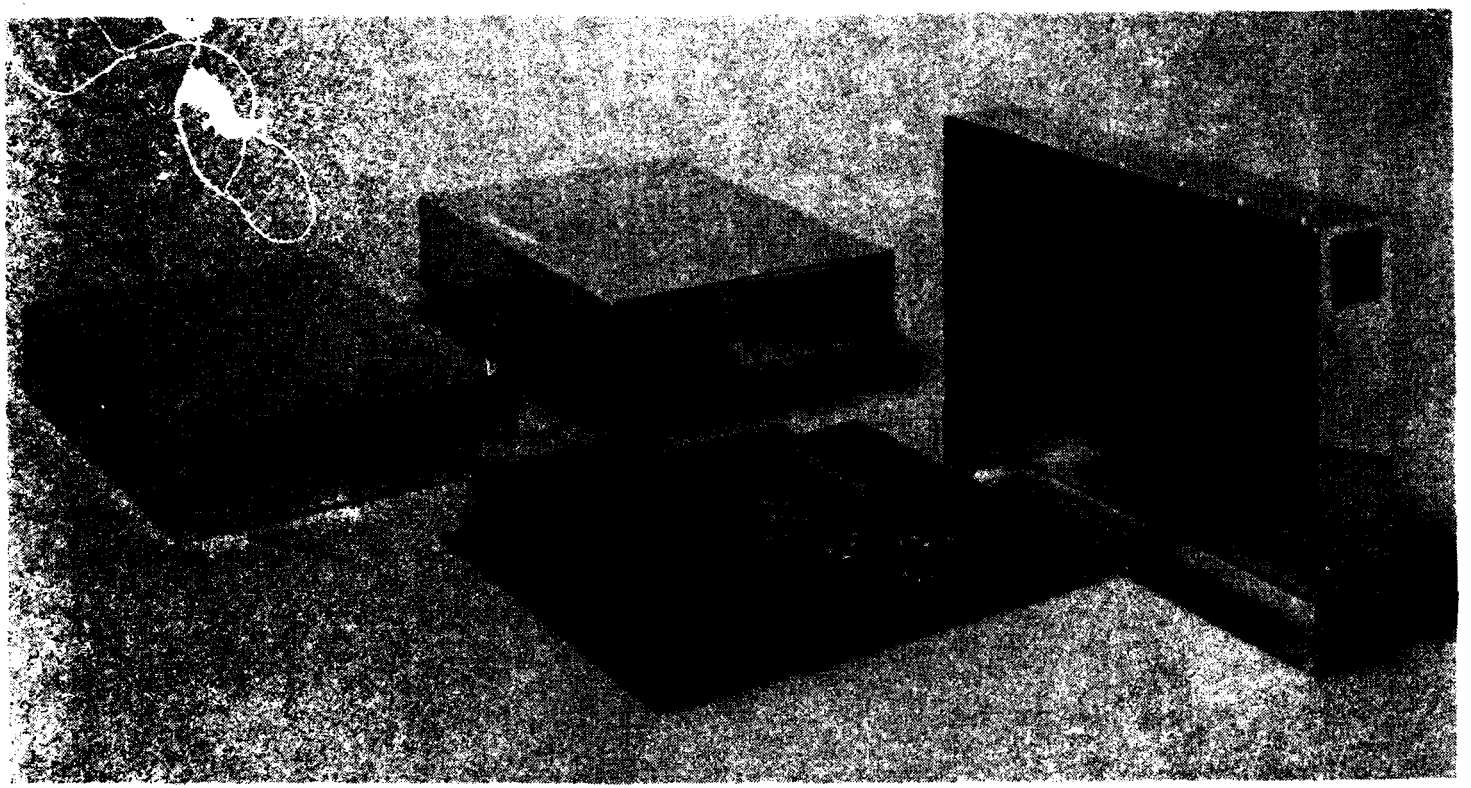

Figure 1.3. Three analyzer models

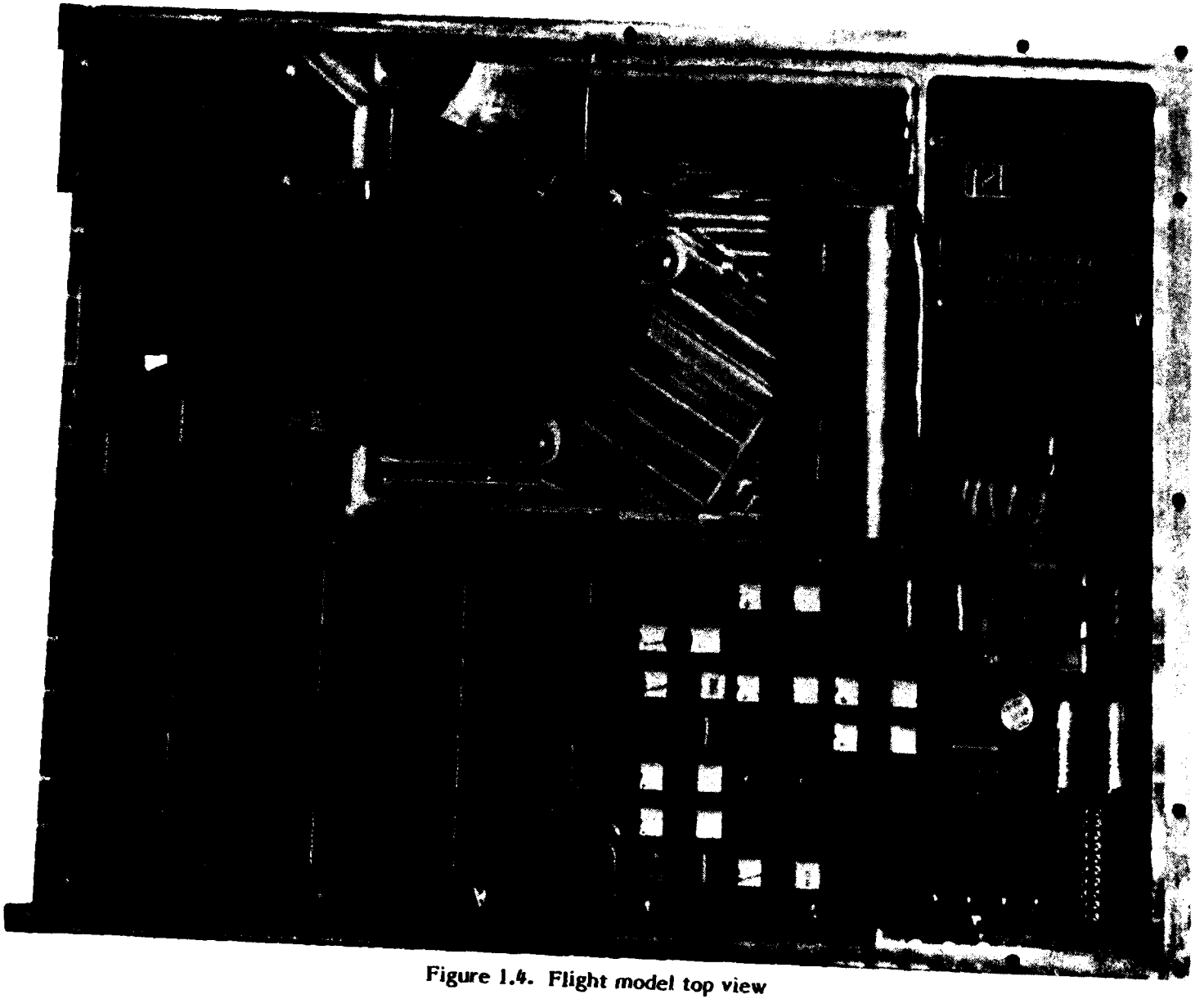

Figure 1.4. Flight model top view

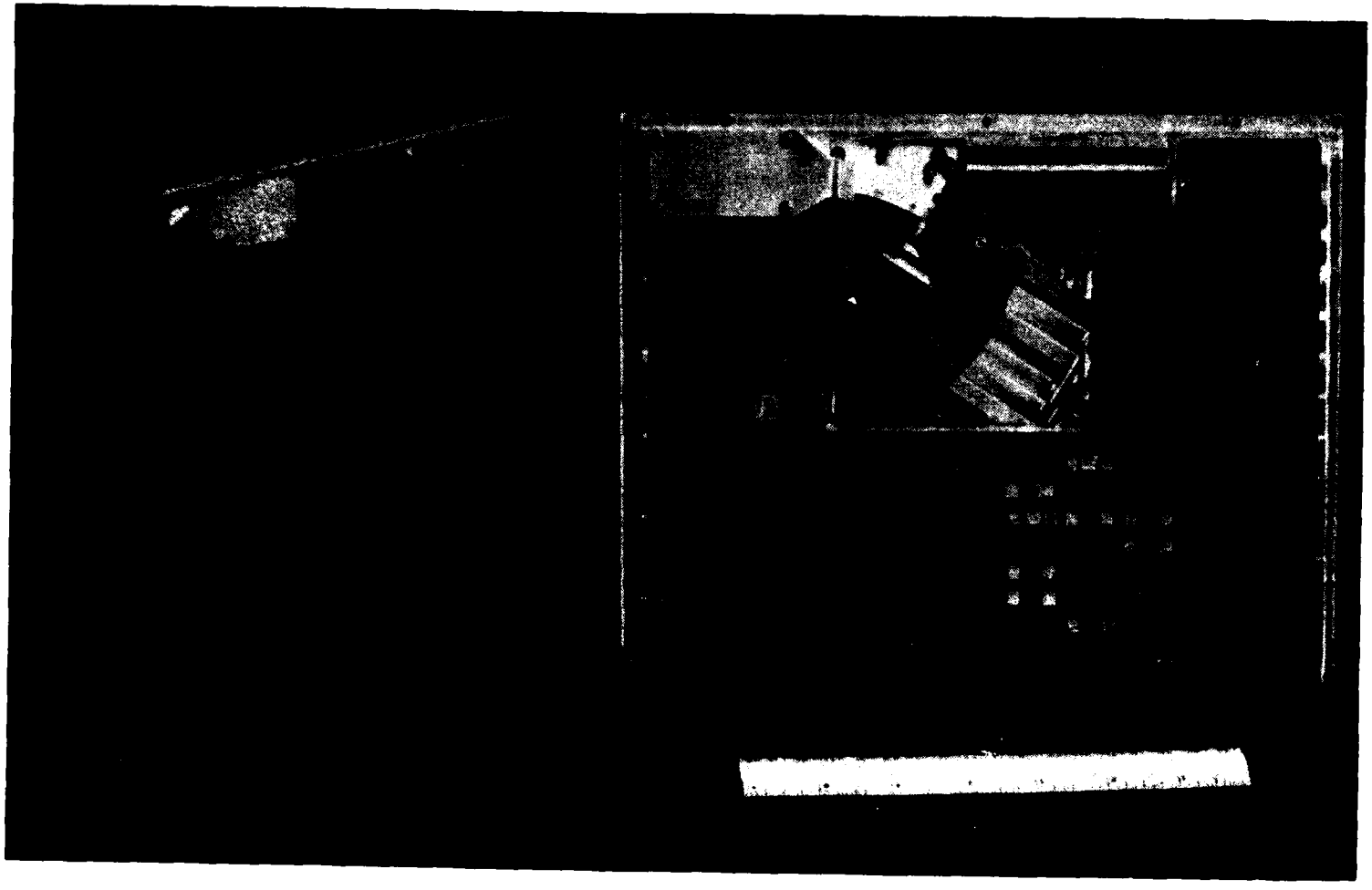

Figure 1.5. Flight model with cover

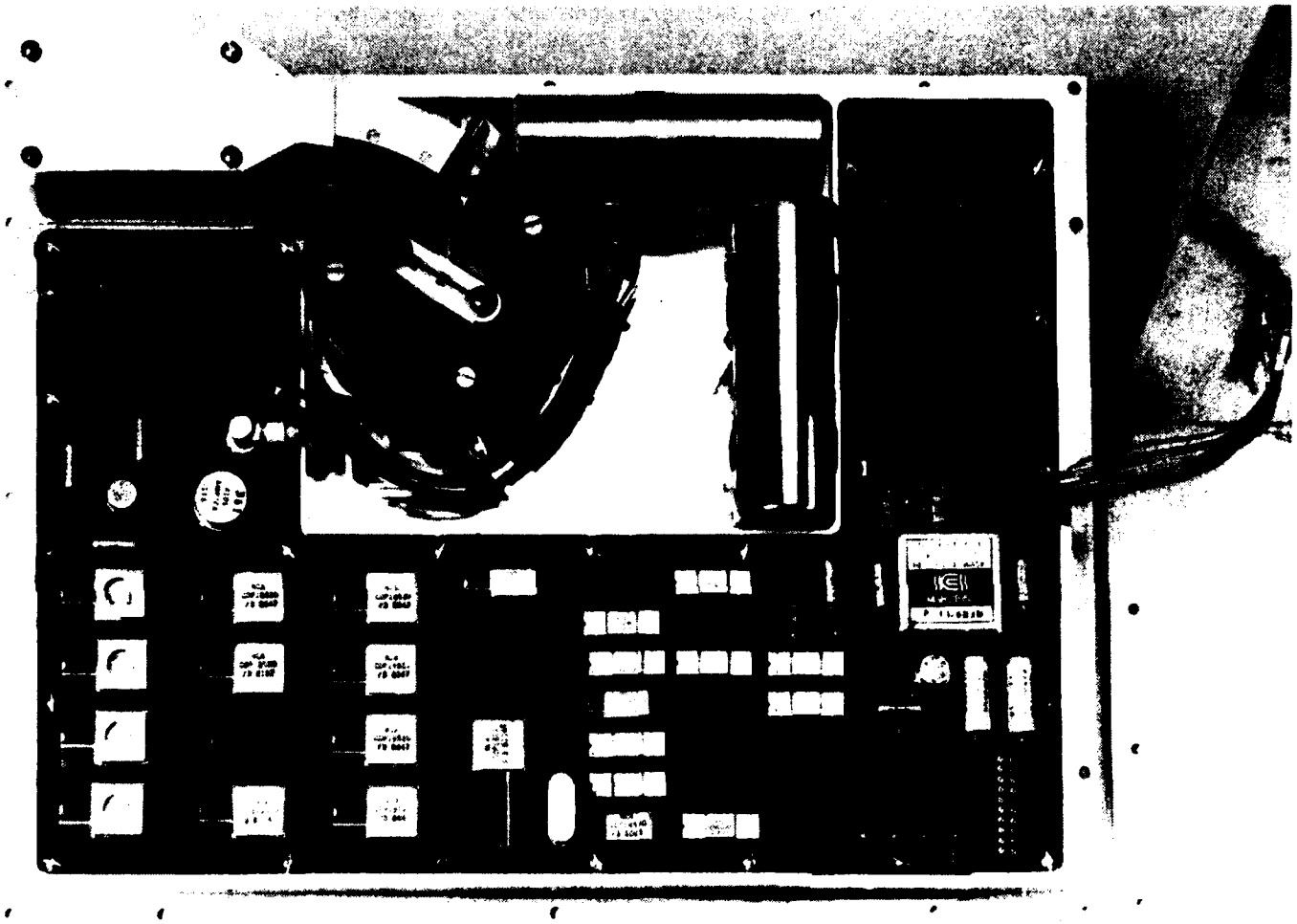

Figure 1.6. Flight model layout close up

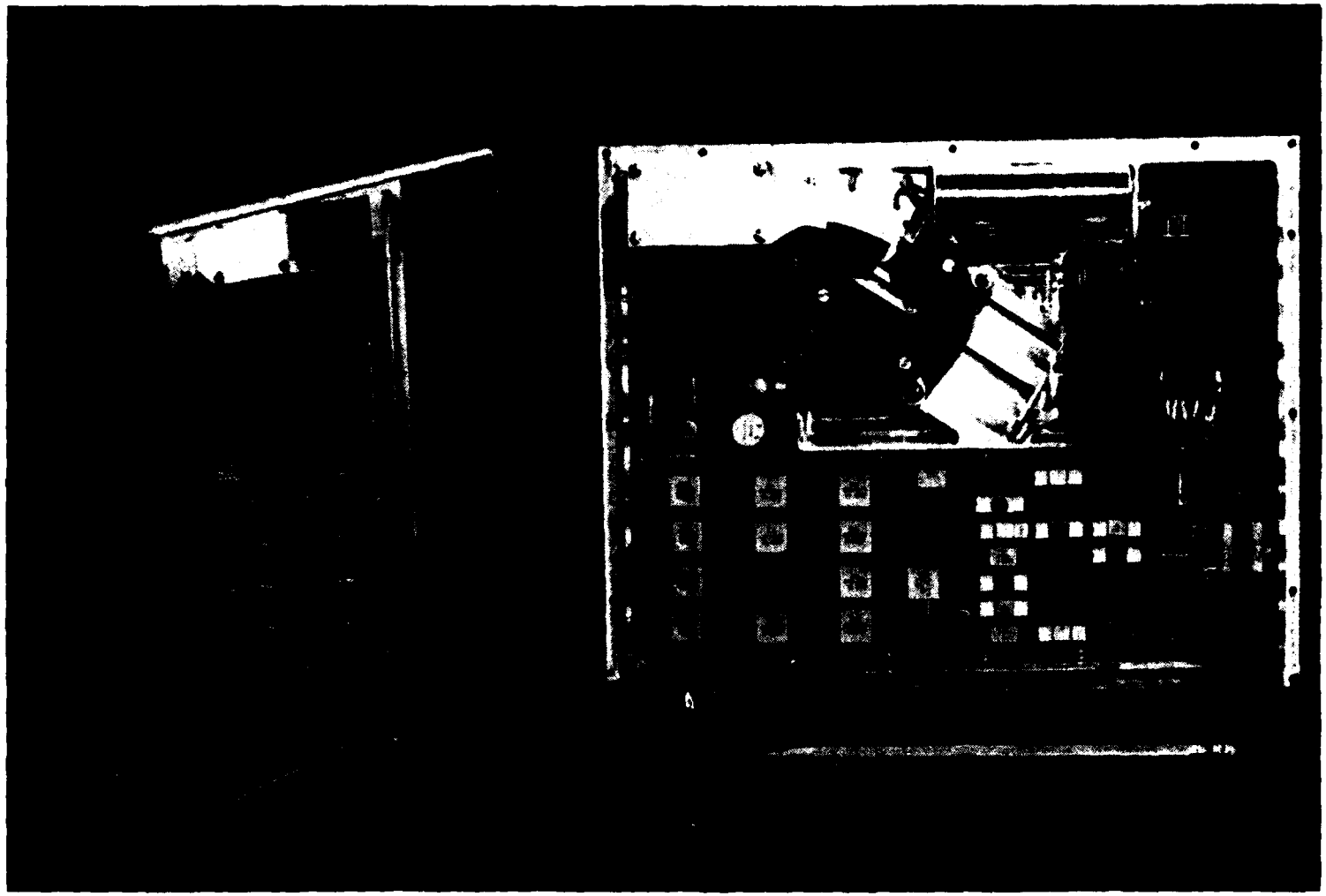

Figure 1.7. Flight model and cover

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2. MECHANICAL DESIGN

The assembly diagram for the flight models appears in Figure 2.1. Information on the design of the prototype unit has appeared elsewhere (Ref 3). There are differences between the prototype and flight model designs which are discussed in appropriate sections and summarized in the concluding discussion.

The machined metallic parts for the spectrometers were made from various aluminum alloys. The base plate (Figure 2.2) was milled from a 3/4 inch block of 6061 T4 alloy, heat treated and stress relieved. Provisions for all subsystems are seen in Figures 2.1 and 2.2. The remaining space is occupied by the Multiwire® circuit board. High voltage supplies (Venus Q30Z) for the detection and analyzer plates are secured in semi-cylindrical supports (Item 11, Figure 2.1; Note 2, Figure 2.2). The detector holder assembly of Figure 2.3 (Items 12 and 13 of Figure 2.1) is formed from Delrin and may be adjusted in analyzer exit length as a means of varying energy channel width.

The analyzer assembly of Figure 2.4 (Items 7, 8 and 9 of Figure 2.1) consists of two cylindrical section plates with the outer grounded to the base and the inner structure of Delrin containing the convex (negative) plate. The collimation system for the analyzer (Figures 2.5 through 2.8, Items 3, 4 and 5 of Figure 2.1) consists of interchangeable sets of three rectangular baffles each, which define the field of view from the center of the entrance plane of the cylindrical selector.

2.1 DETECTOR ASSEMBLY

The detector is a Model 4013C channel electron multiplier with attached collection cap and electrodes. It is mounted in a base machined from a block of black Delrin. Grooves in the base and lid are cut to suit the channeltron and it is held securely by the two pieces. Dimensions of the multipliers are not held to tight tolerances by the manufacturer, and hence tailoring of the mounting channels was determined a posteriori. The fits were deemed satisfactory enough to obviate the use of a potting material for the detectors. Access to the channeltrons is thus maintained.

The detector is a 270 degree continuous electron multiplier with an aperture formed as a 3 mm diameter cone. Details of their characteristics and performance may be found in Reference 2.

The two electrodes are attached by low-temperature solder to pins on the outside of the mounting base to relieve strain from the multiplier itself. The detector entrance is shielded by a hemispherical cap (Item 1, Figure 2.8) at ground potential, which provides mechanical protection and reduction in excitation and dielectric charging from scattered particles and secondaries under working conditions.

The detection length, between the exit plane of the curved plates and the multiplier entrance, may be varied in order to alter energy response characteristics. It may be secured in position by screws (Items 18 and 19 of Figure 2.1) to the base plate.

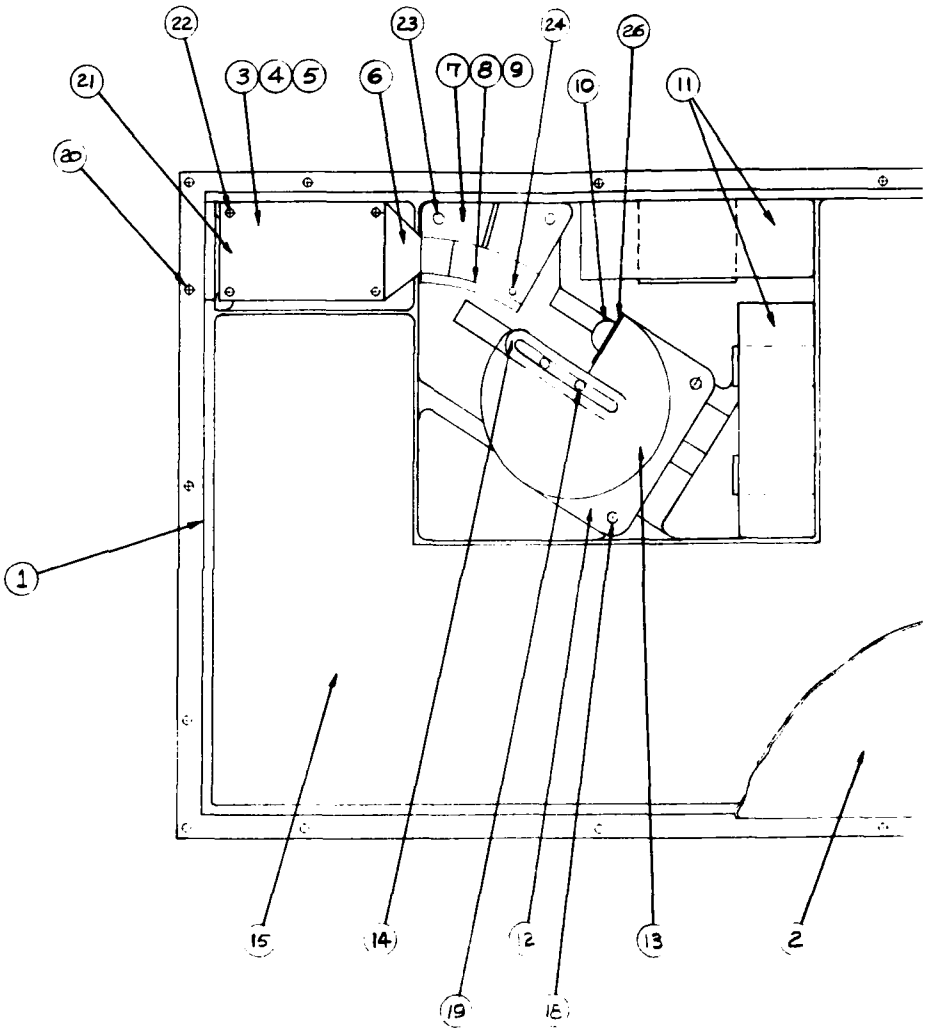
2.2 ANALYZER (ENERGY SELECTOR) ASSEMBLY

The electrostatic plate assembly of Figure 2.4 consists of three sections. The frame (Item 1) is milled from aluminum alloy and serves as the ground (positive) plate. A Delrin holder (Item 3) is bolted into the frame and contains the conducting innner (negative) plate. The active areas of each plate subtend 32 degrees, running the length of the selector and are 2 cm wide. Their separation throughout the arc is 0.35 cm. The radius of the central path is 7 cm. Each is serrated to a depth of 0.25 mm, at intervals of 0.8 mm in the manner shown, in order to reduce scattering of particles and photons into the detector.

2.3 COLLIMATOR

The entrance collimator is formed as a base and two side plates with slots for three field stops which define entrance angles to the analyzer plates. The horizontal inner dimension of the steps has the primary effect on integral energy response as it defines trajectories with respect to the vertical (analyzing) axis. The sets define total angles of 10, 12, 16 and 20 degrees. Their inner surfaces are beveled to semi-knife edges to reduce the effects of scattering and secondary production.

The lid of the assembly (Item 2 of Figure 2.8) forms a shield to prevent escape of particles into the space between the collimator and analyzer plates. Field stops may be changed after removal of the collimator cover.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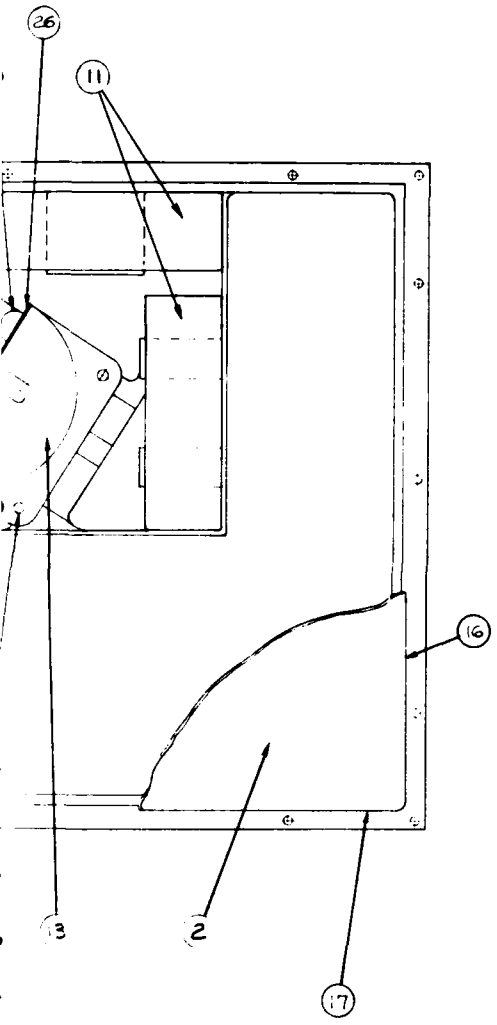

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	4	25		SCREW, 4-40 UNC x 3/8 SKT HD ST STL	
	6	24		SCREW 2-56 UNC x 1/4 FH ST STL	
	2	23		SCREW, 5-40 UNC x 1/4 RH ST STL	
	4	22		SCREW, 4-40 UNC x 1/8 RH ST STL	
	2	21		SCREW, 5-40 UNC x 5/16 FH ST STL	
	16	20		SCREW, 4-40 UNC x 1/4 RH ST STL	
	1	19		SCREW 5-40 UNC x 7/16 RH ST STL	
	2	18		SCREW, 5-40 UNC x 7/16 RH ST STL	
	23	17		SCREW, 4-40 UNC x 3/16 FH ST STL	
	1	16	CANNON DA-15S	PLUG, CABLE HARNESS	
	1	15		ELECTRONICS BOARD	
	1	14	007-3	STRESS PLATE	
	1	13	006	CHANNELTRON HOLDER CAP	
	1	12	006	CHANNELTRON HOLDER BODY	
	2	11	VENUS 930	DC TO DC CONVERTER	
	1	10	007-1	GROUND CAP	
	1	9	-004-2	ANALYSER HIGH VOLTAGE PLATE	
	1	8	-004-3	ANALYSER INSULATOR	
	1	7	-004-1	ANALYSER GROUND PLATE	
	1	6	007-2	COLLIMATOR COVER	
	3	5	005	COLLIMATOR FIELD STOP	
	2	4	-003	COLLIMATOR SIDE PLATE	
	1	3	-002	COLLIMATOR BASE	
	1	2	-009	COVER	
	1	1	-008	BASE PLATE	

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

MATERIAL

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PROTON SPECTROMETER ASSEMBLY & PARTS

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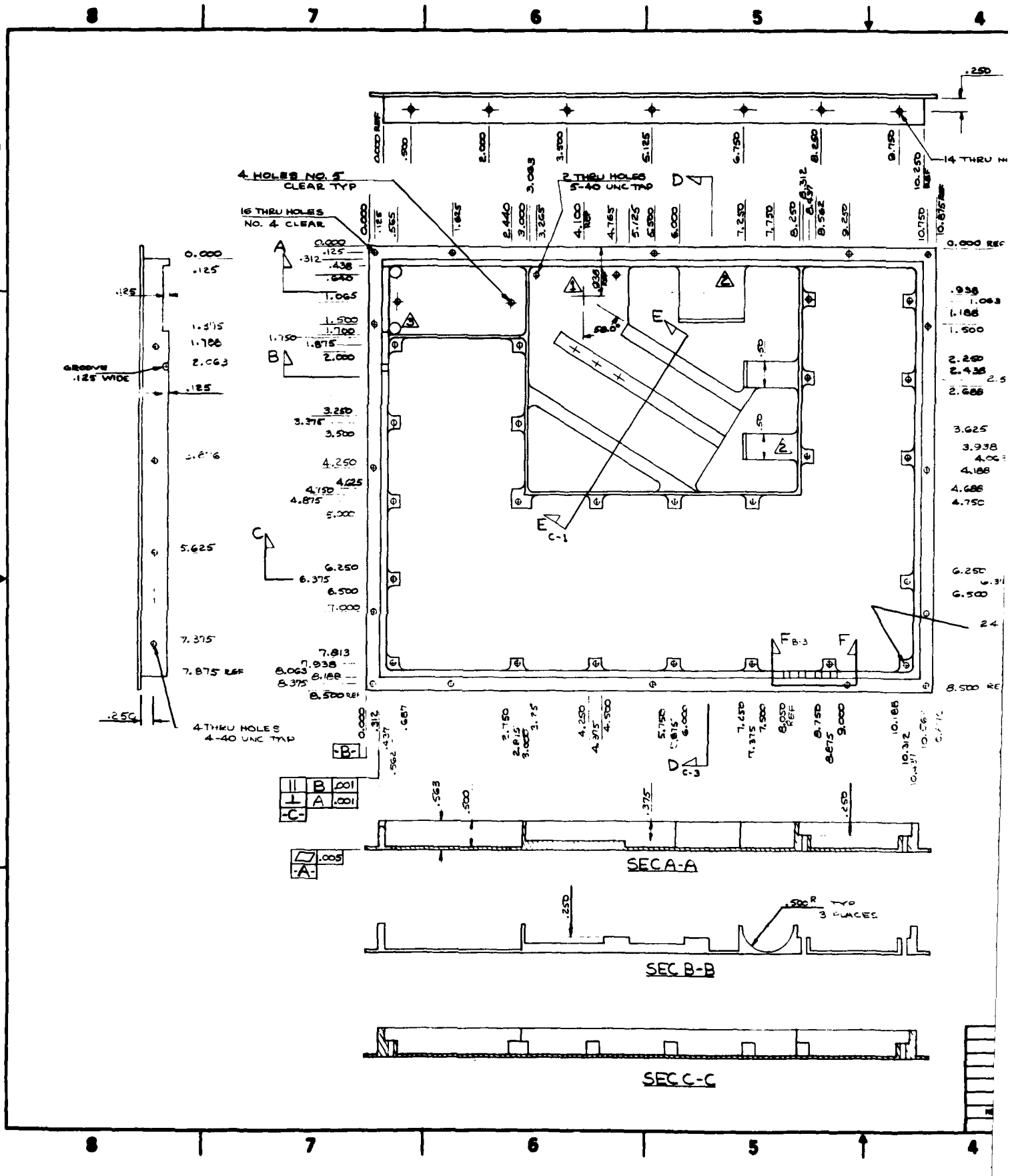
Figure 2.1. Spectrometer assembly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16 THRU HOLES NO. 4 CLEAR
2 THRU HOLES 5-40 UNC TAP
14 THRU H
GROOVE .125 WIDE
4 THRU HOLES 4-40 UNC TYP
.250R TYP 3 PLACES
SEC A-A
SEC B-B
SEC C-C

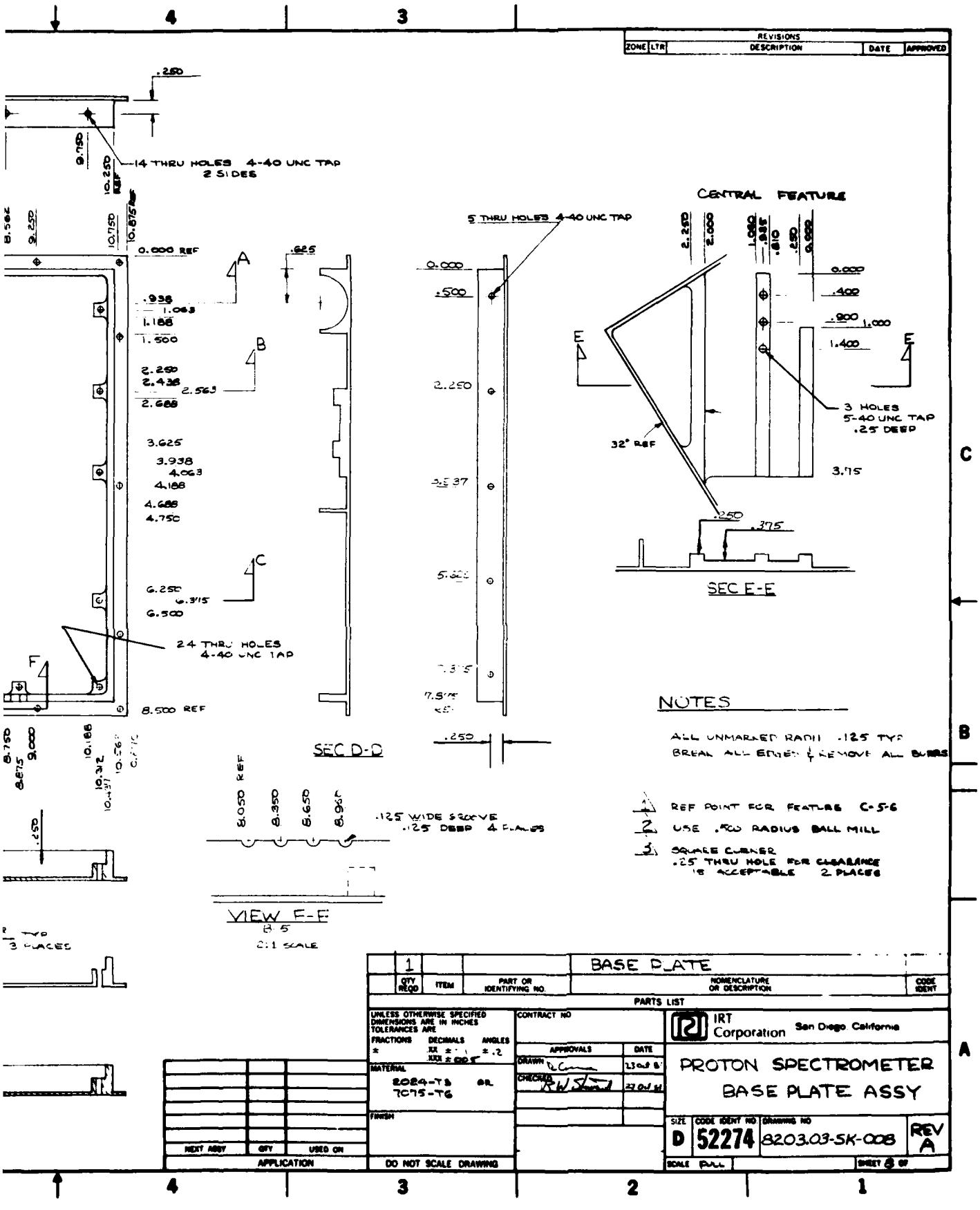

Figure 2.2. Base plate

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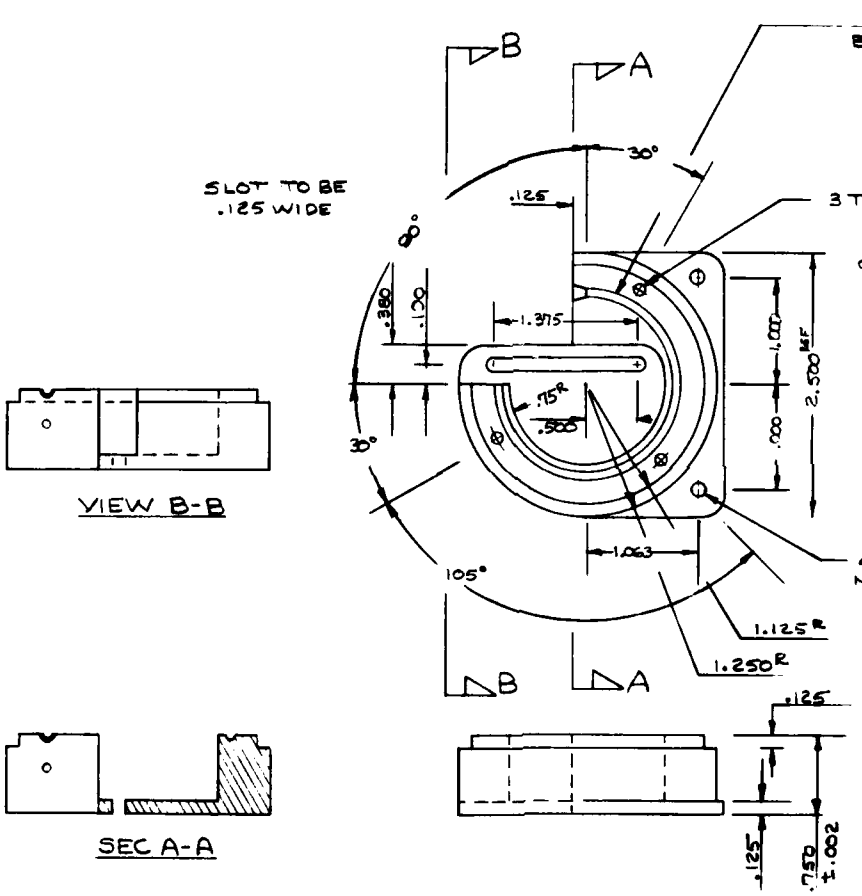

VIEW B-B

SEC A-A

3 HOLES
0-80 UNC TAP
.25 DEEP EQ SP
ON .650 SC

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	1	1		HC

NOTES

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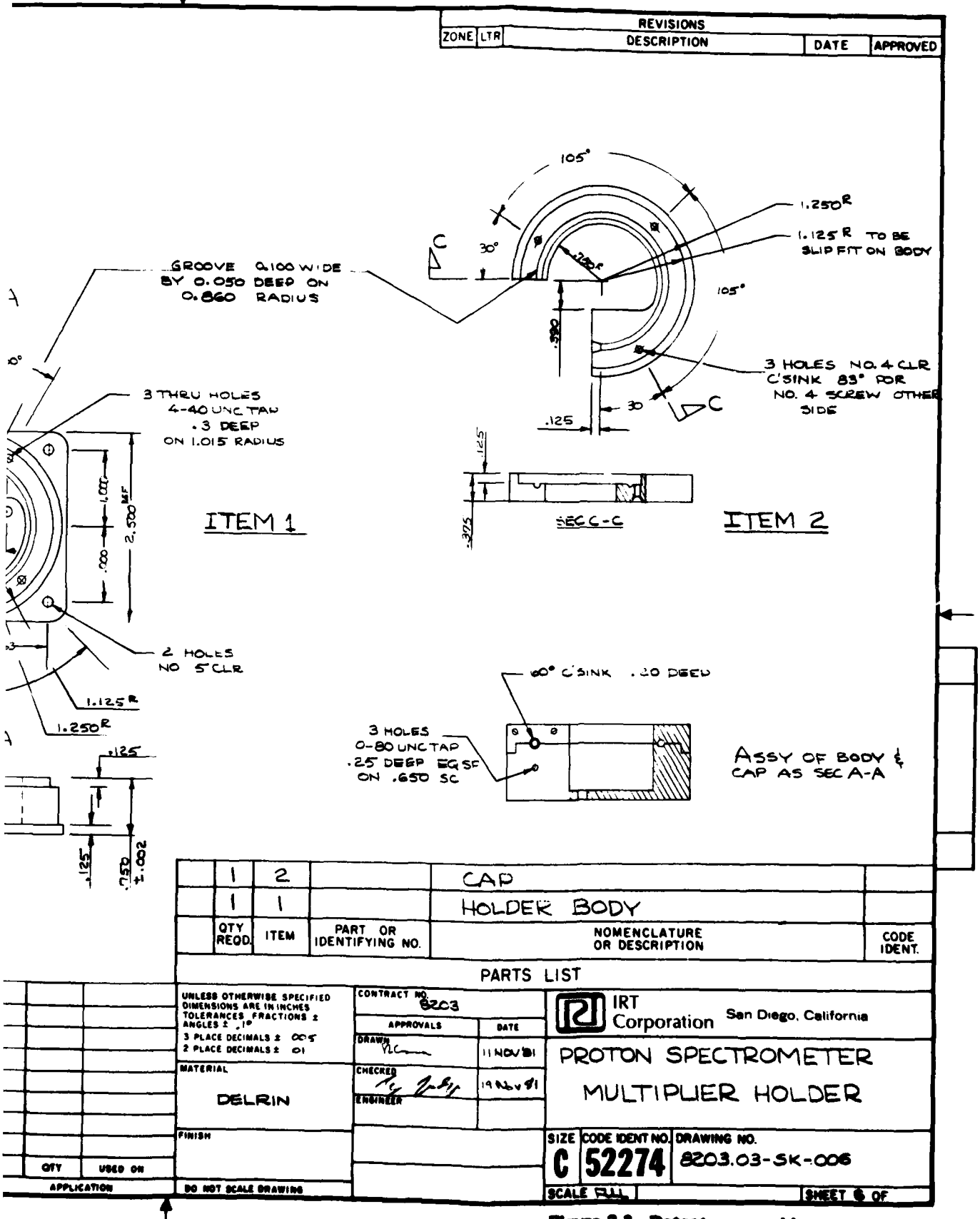
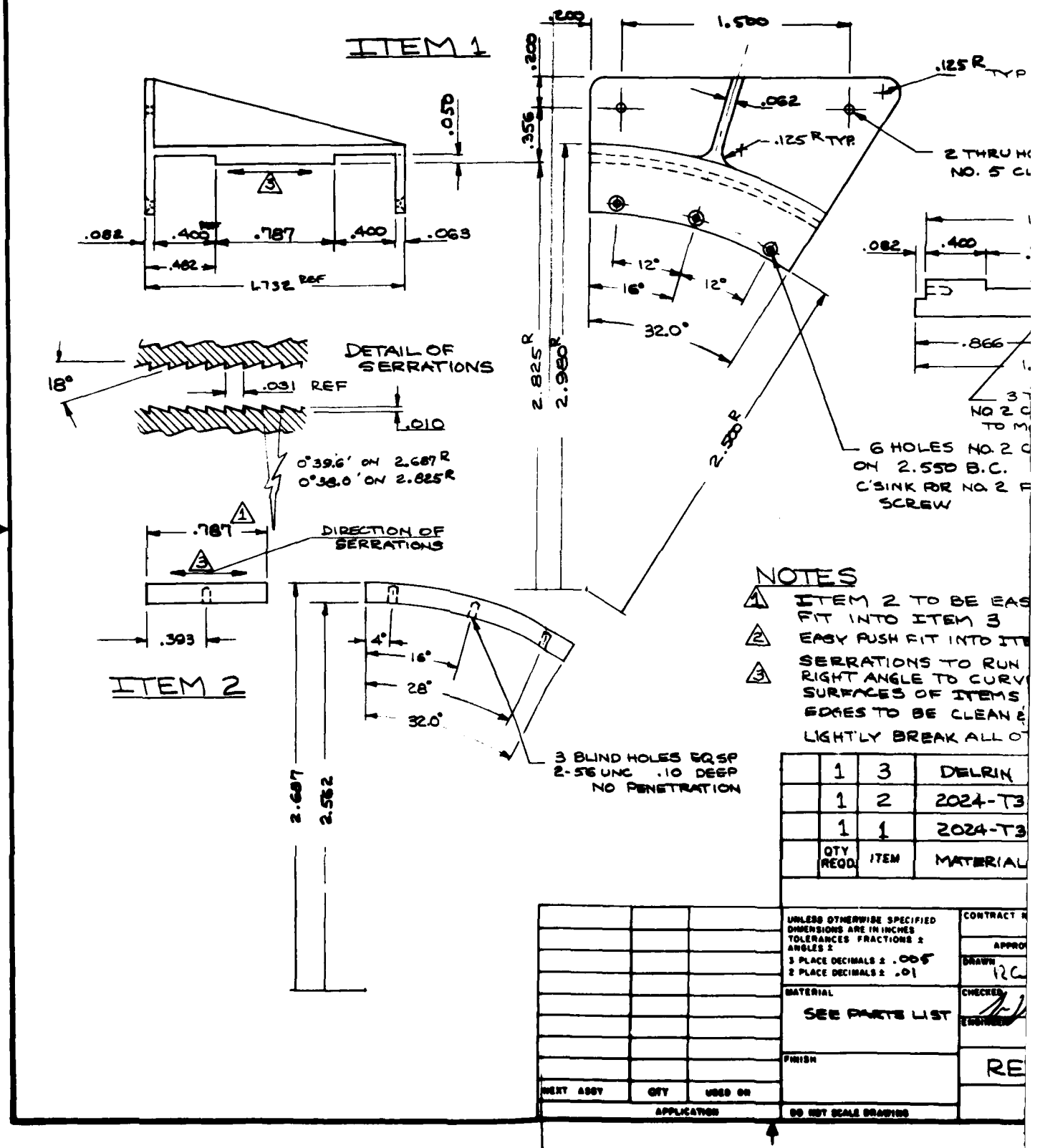


Figure 2.3. Detector assembly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.125 R TYP
.062
.125 R TYP
2 THRU H
NO. 5 CL
.356
.050
.082
.400
.787
.400
.063
.482
1.732 REF
12°
16°
12°
32.0°
.082
.400
.866
2.825 R
2.980 R
2.500 R
DETAIL OF SERRATIONS
18°
.031 REF
.010
0°39.6' ON 2.687 R
0°38.0' ON 2.825 R
6 HOLES NO. 2 C
ON 2.550 B.C.
C'SINK FOR NO. 2 F
SCREW
.787
DIRECTION OF SERRATIONS
.393
ITEM 2
4°
16°
28°
32.0°
3 BLIND HOLES EQ SP
2-56 UNC .10 DEEP
NO PENETRATION
2.687
2.562
NOTES
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FIT INTO ITEM 3
2 EASY PUSH FIT INTO ITE
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EDGES TO BE CLEAN &
LIGHTLY BREAK ALL O
1 3 DELRIN
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1 1 2024-T3
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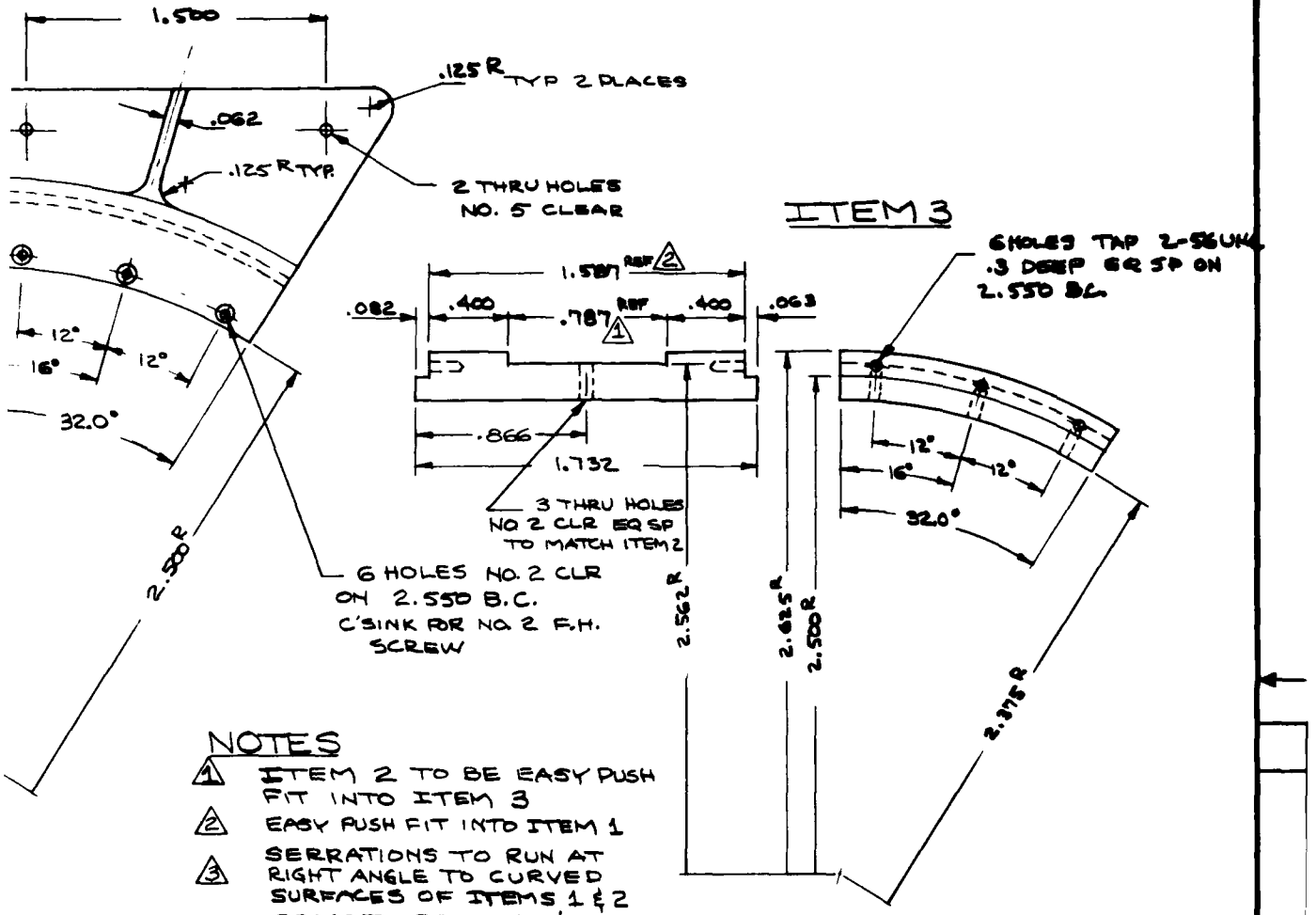

NOTES

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2. EASY PUSH FIT INTO ITEM 1
3. SERRATIONS TO RUN AT RIGHT ANGLE TO CURVED SURFACES OF ITEMS 1 & 2 EDGES TO BE CLEAN & SHARP

LIGHTLY BREAK ALL OTHER EDGES & REMOVE ALL BURRS

ND HOLES EQ SP
UNC .10 DEEP
NO PENETRATION

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PROTON SPECTROMETER ANALYSER

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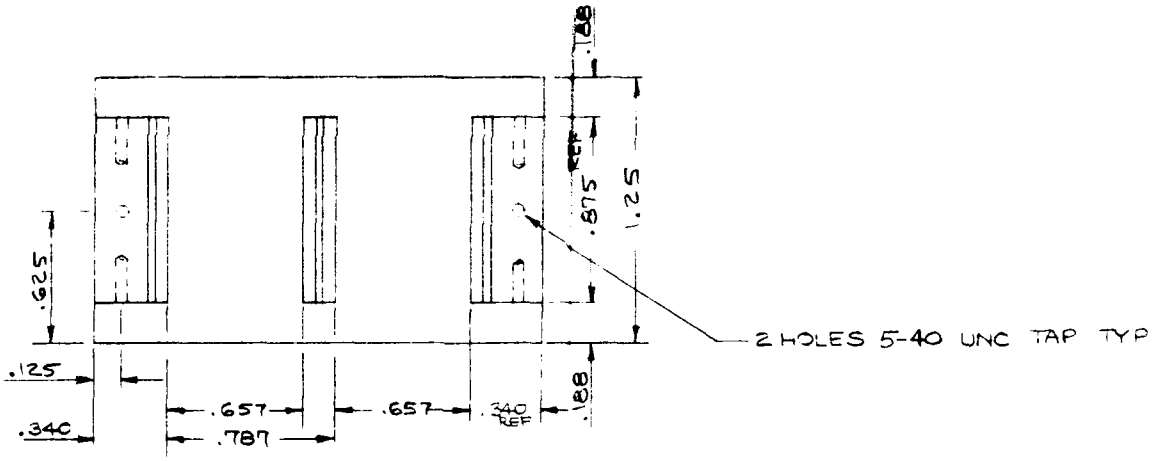

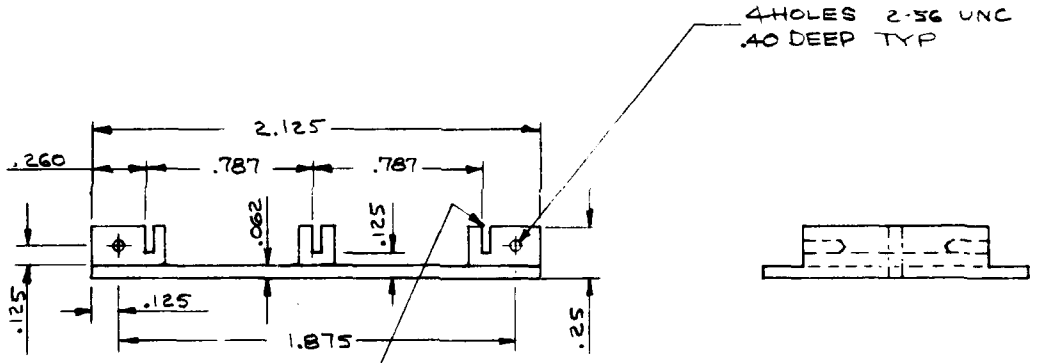

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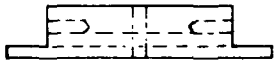

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PROTON SPECTROMETER-COLLIMATOR

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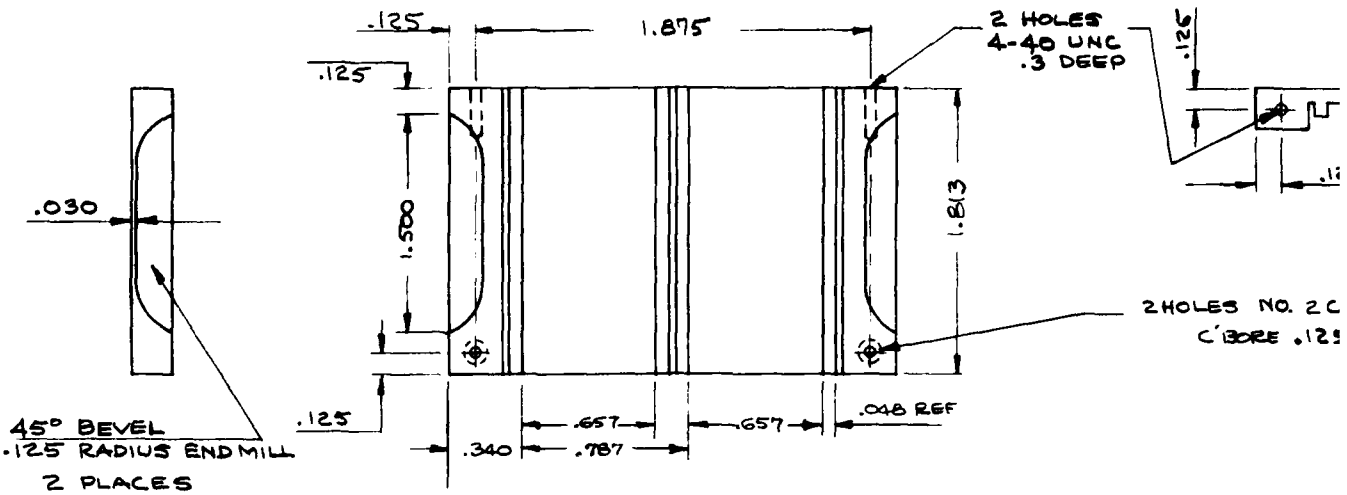
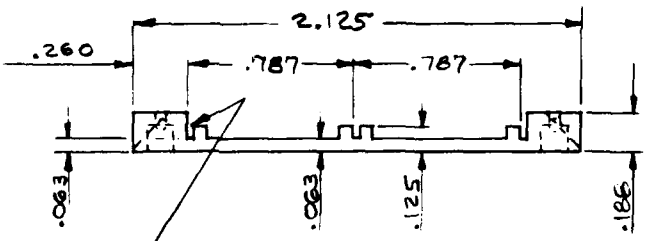
Figure 2.5. Collimator





SLOTS TO BE .032 WIDE BY .125 DEEP
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3 PLACE DECIMALS ±
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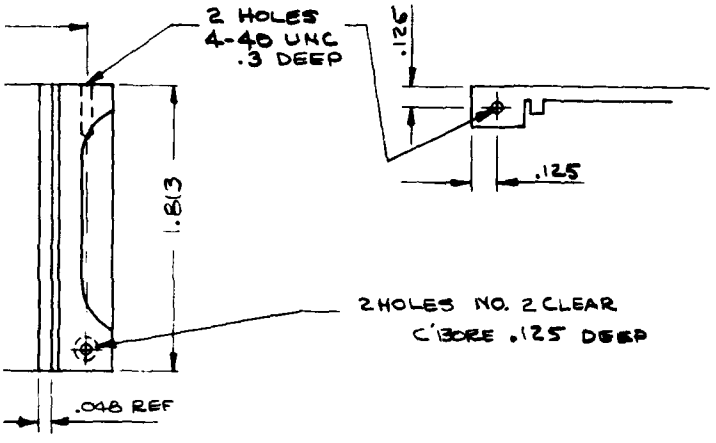
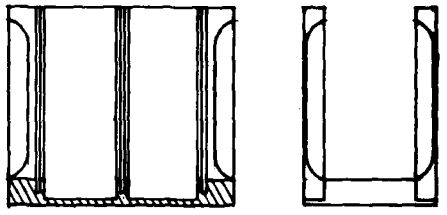
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		CHANGE CLOSE SIDE HOLES TO No. 2	5 Nov 81	





FULL SCALE ASSY
1 PC 8203.03-SK-002
2 PC 8203.03-SK-005

DE BY .125 DEEP
FIELD STOP (8203.03-SK-005)

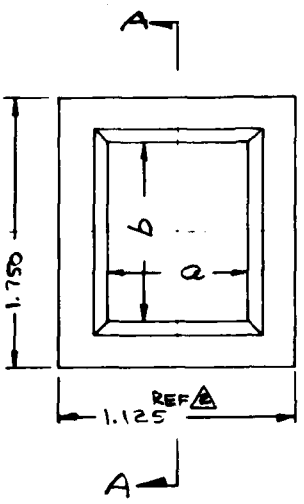
QTY REQD	ITEM	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT.
2			COLLIMATOR SIDEPLATE	

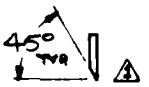
PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES FRACTIONS ± ANGLES ± 3 PLACE DECIMALS ± 2 PLACE DECIMALS ±	CONTRACT NO.	IRT Corporation San Diego, California	
MATERIAL 2024-T3	APPROVALS / DRAWN R Cuderman	DATE 15 Nov 81	PROTON SPECTROMETER-COLLIMATOR
FINISH	CHECKED / ENGINEER	11 June 81	
QTY / USED ON / APPLICATION	REV A 24 Dec 81	SIZE C / CODE IDENT NO. 52274 / DRAWING NO. 8203.03-SK-002	
DO NOT SCALE DRAWING		SCALE 2:1	SHEET 1 OF 2

Figure 2.6. Collimator

2





SECTION A-A

SET

	1	2	3
a1	.833	.664	.497
b1	1.004	.833	.664
a2	.555	.442	.331
b2	.669	.555	.443
a3	.278	.220	.166
b3	.335	.278	.221
θ(a)	20	16	12
φ(b)	24	20	16

NOTES

1. EDGES OF FIELD STOP TO BE BURR FREE BUT SHARP
2. ALL ITEMS TO BE EASY SLIP FIT INTO COLLIMATOR ASSY
3. ONE FIELD STOP PLATE TO EACH SET TO HAVE INNER DIMENSIONS AS PER TABLE
4. THREE FIELD STOP PLATES COMPRISE ONE SET

QTY REQD	ITEM	PART OR IDENTIFYING NO.
1	SET 1	ONLY

NEXT ASSY	QTY	USED ON
APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES FRACTIONS ±
ANGLES ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±

MATERIAL
2024-T3
.032 THICK

FINISH
32

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVAL

DRAWN RC

CHECKED

ENGINEER

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

SET

	1	2	3	4		
a1	.533	.664	.497	.413		
b1	1.004	.833	.664	.497		
a2	.555	.442	.331	.276		
b2	.669	.555	.443	.331		
a3	.278	.220	.166	.138		
b3	.335	.278	.221	.166		
θ(a)	20	16	12	10		
φ(b)	24	20	16	12		

SECA-A

SET TABLE

SE ONE SET

QTY REQD.	ITEM	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT.
	1	SET 1	ONLY FIELD STOP	

PARTS LIST

QTY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES FRACTIONS ± ANGLES ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±

MATERIAL 2024-T3 .032 THICK

FINISH 32

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN RC	14 MAY 91
CHECKED	11 June 91
ENGINEER	

IRT Corporation San Diego, California

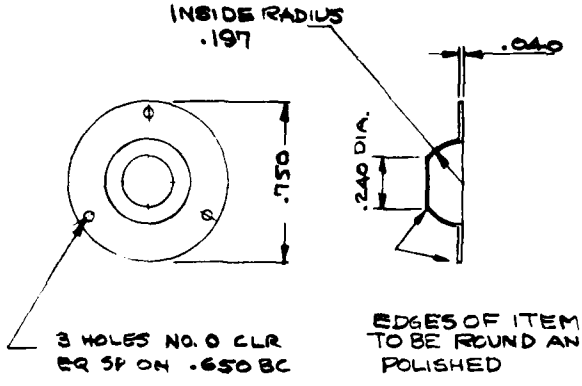
PROTON SPECTROMETER
COLLIMATOR

SIZE	CODE IDENT NO.	DRAWING NO.
C	52274	8203.03-SK-005

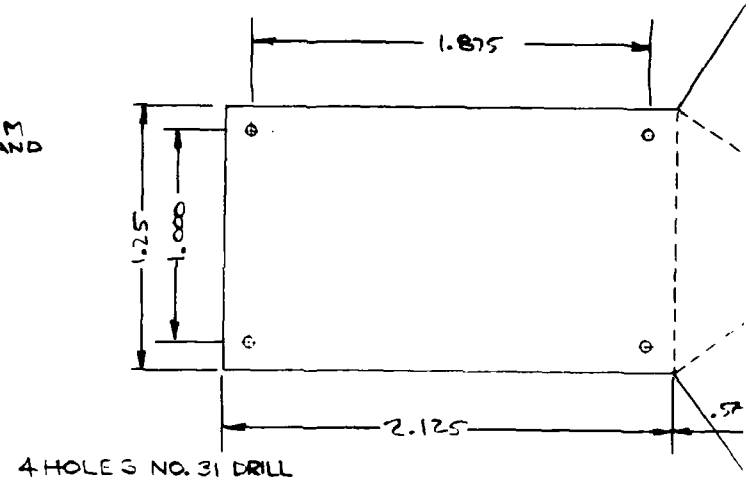
SCALE 2:1 SHEET 5 OF

Figure 2.7. Collimator stops

2

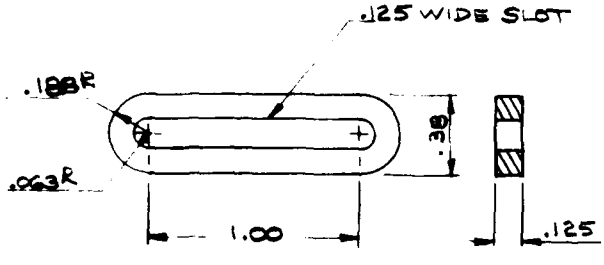


ITEM 1
REQD: 1
MATL: 2024-T3



ITEM 2
REQD 1
MATL: 5052-T32
.032 THICK

15°



ITEM 3
REQD: 1
MATL: 2024-T3

		5
		4
	1	3
	1	2
	1	1
	QTY REQD	ITEM	PART OR IDENTIFYING NO

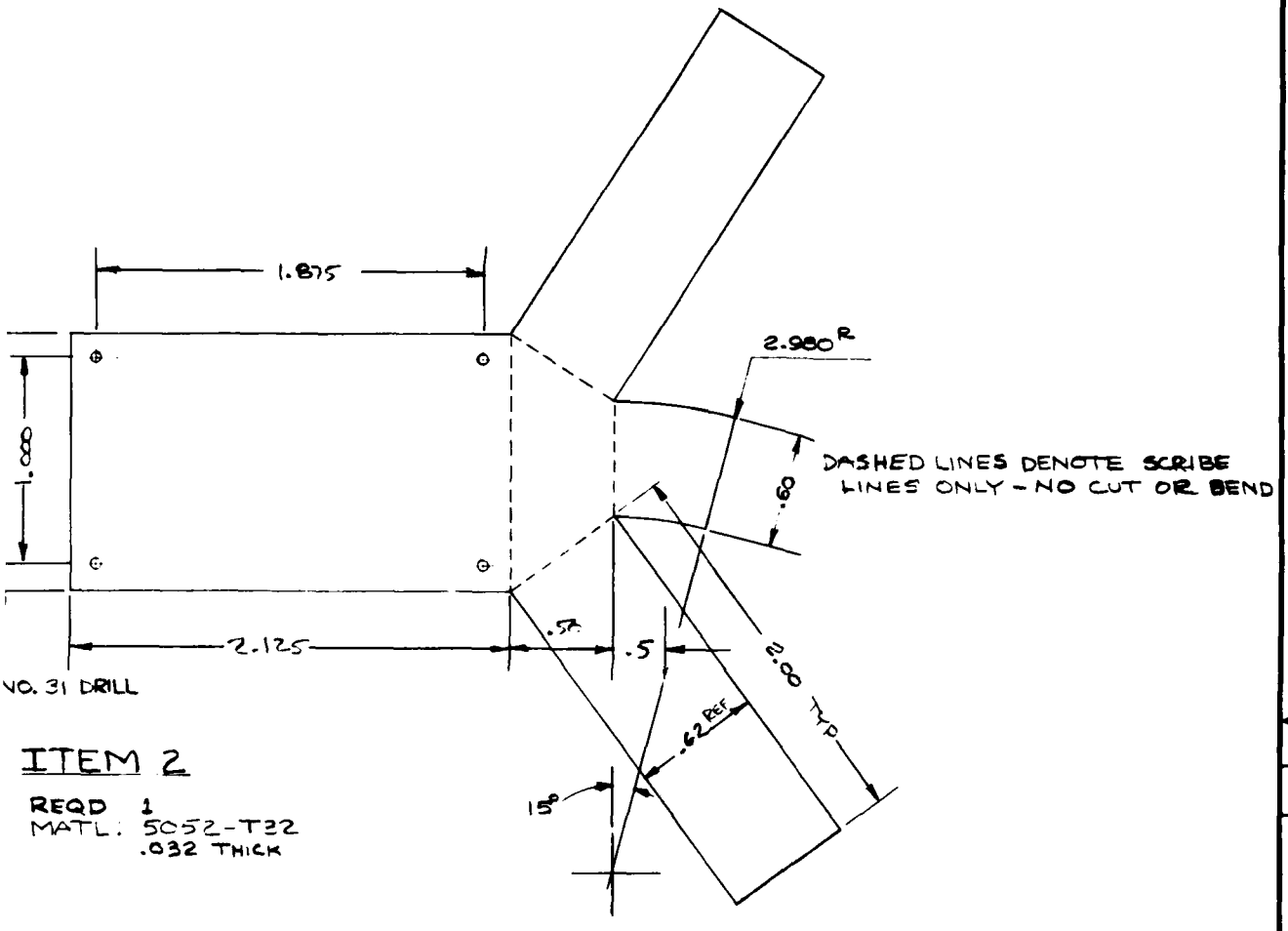
NEXT ASSY	QTY	USED ON
APPLICATION		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES FRACTIONS ±
ANGLES ±
3 PLACE DECIMALS ± .005
2 PLACE DECIMALS ± .01
MATERIAL
FINISH
DO NOT SCALE DRAWING

CONTRACT NO
APPROV
DRAWN
CHECKED
ENGINEER
REV

1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



ITEM 2

REQD 1
MATL: 5052-T32
.032 THICK

QTY REQD.	ITEM	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT.
	5			
	4			
1	3		STRESS PLATE	
1	2		COLLIMATOR COVER PLATE	
1	1		GROUND CAP	

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES FRACTIONS ±
ANGLES ±
3 PLACE DECIMALS ± .005
2 PLACE DECIMALS ± .01

MATERIAL

FINISH

DO NOT SCALE DRAWING

QTY | USED ON | APPLICATION

CONTRACT NO.

APPROVALS	DATE
DRAWN	18 May 61
CHECKED	11 June 61
ENGINEER	

REV A 24 Oct 61

IRT Corporation San Diego, California

PROTON SPECTROMETER
MISC PARTS

SIZE C | CODE IDENT NO. 52274 | DRAWING NO. 8203.03-SK-007

SCALE 2:1 | SHEET 1 OF

Figure 2.8. Shields and adjuster

2

2.4 SPECTROMETER COVER

The cover for the instrument is shown in Figure 2.9. It is an easy fit over the base plate and is secured by 4-40 flat head screws. The front surface contains apertures for the collimator entrance and for the sun sensor photodiode. These openings are protected in storage and transit by press-fit teflon covers. The rear surface contains the Cannon DA 15P male connector. The instrument model (P, F1, F2) is identified beside the connector.

After removal of securing screws, the cover may be removed carefully, favoring the front to avoid damage to internal connections between the plug and circuit board.

2.5 MOUNTING FOOTPRINT

The mounting and field-of-view provisions for the instrument are shown in Figure 2.10. Securement to a platform may be made by sixteen 4-40 screws.

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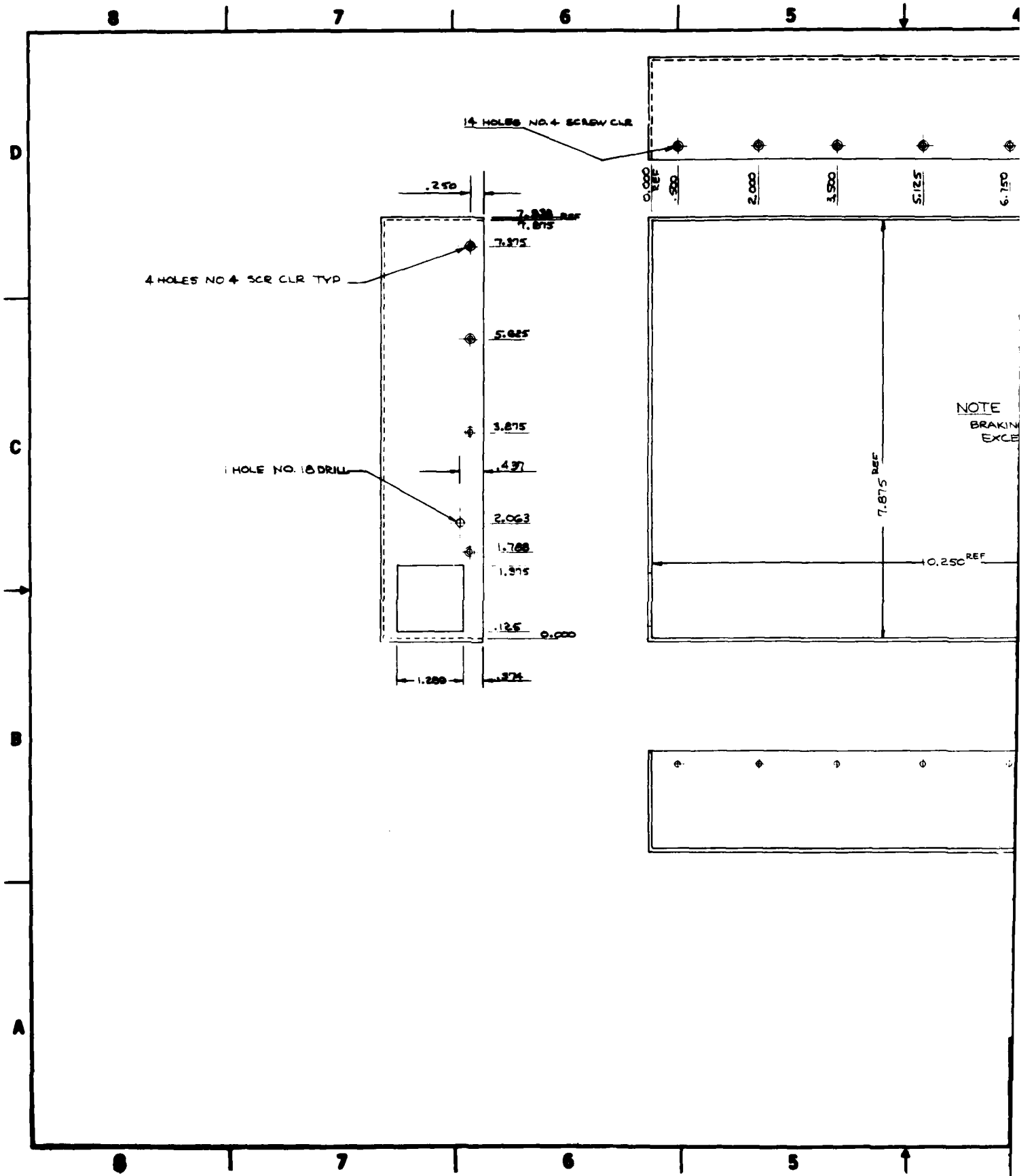

8
7
6
5
D
C
B
A
14 HOLES NO. 4 SCREW CLR
.250
7.875 REF
7.875
7.375
4 HOLES NO 4 SCR CLR TYP
5.625
3.875
.437
1 HOLE NO. 18 DRILL
2.063
1.750
1.375
.125
0.000
1.250
.374
0.000 REF
.500
2.000
3.500
5.125
6.150
7.875 REF
0.250 REF
NOTE
BRAKIN
EXCE

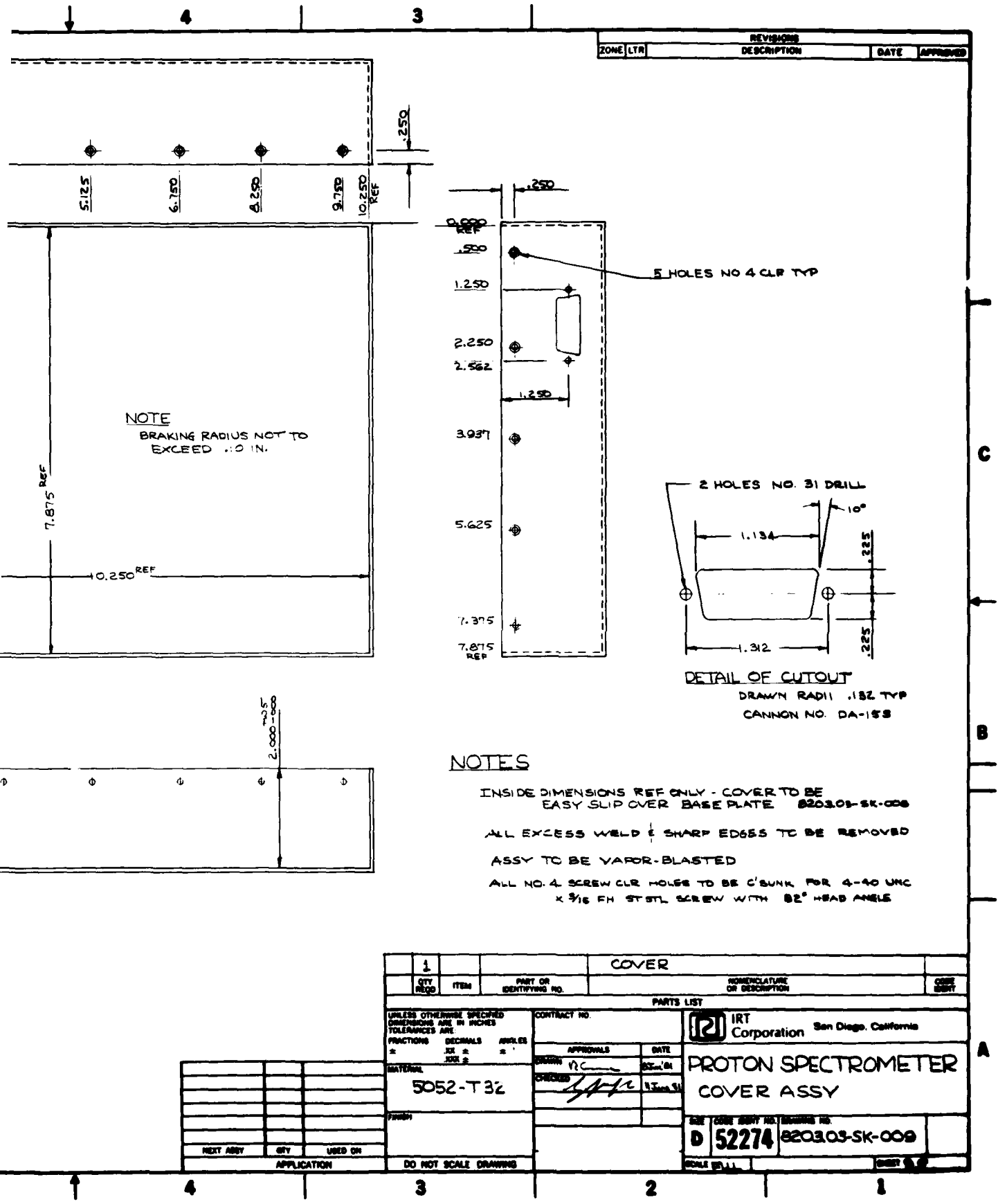
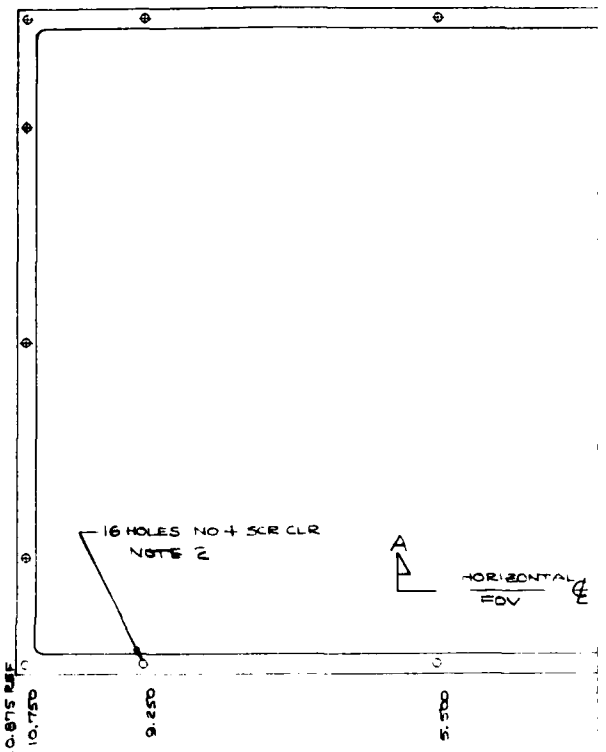
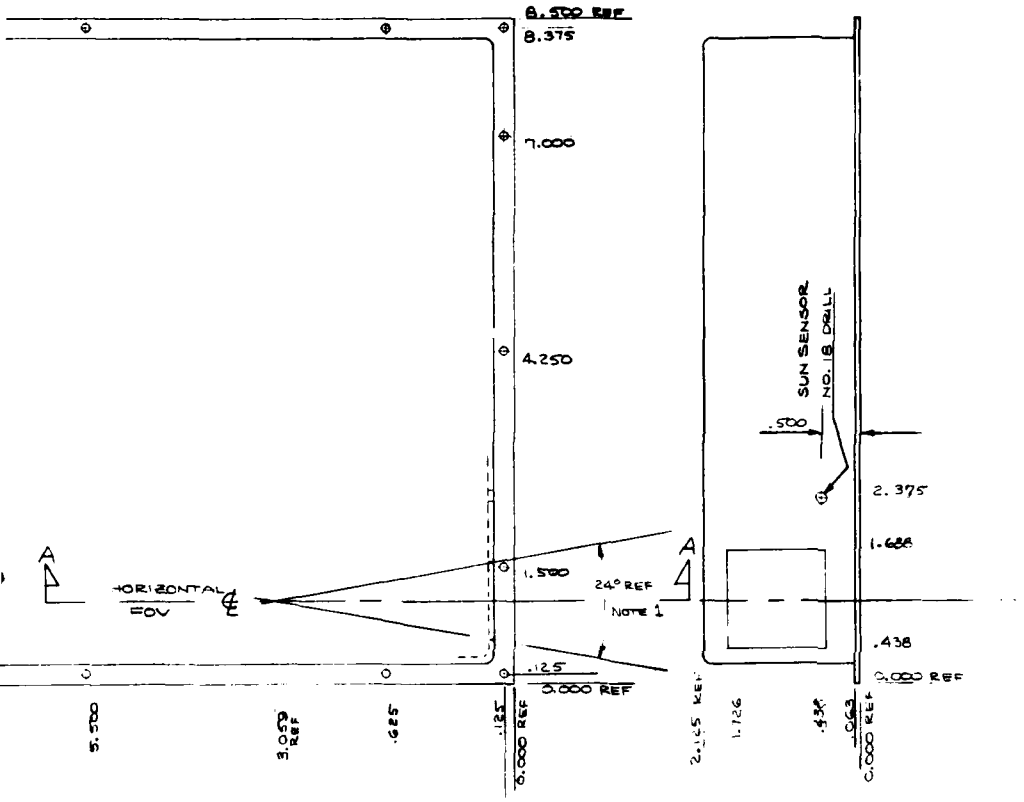
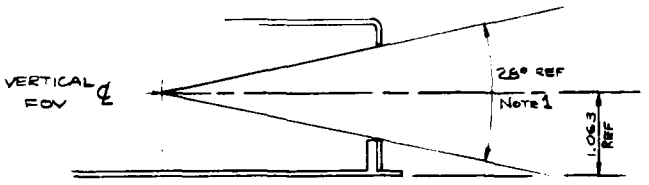


Figure 2.9. Spectrometer cover


16 HOLES NO 4 SCR CLR
NOTE 2
A
HORIZONTAL
FOV
℄
10.875 REF
10.750
9.250
5.500
VERTICAL
FOV
℄





SEC A-A

NOTES

1. ESTIMATED MAXIMUM APERTURE ANGLES
   FINAL VALUES TO BE DETERMINED IN CALIBRATION
2. CLEARANCE HOLES FOR 4-40 UNC MOUNTING SCR

QTY REQD	ITEM	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	CODE IDENT

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .01 .XXX ± .005 ANGLES ± .1°

MATERIAL

FINISH

NEXT ASSY | QTY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN RQ	28 JUL 81
CHECKED	30 JUL 81

IRT Corporation San Diego, California

PROTON SPECTROMETER
MOUNTING & FIELD OF VIEW DETAILS

SIZE D | CODE IDENT NO. 52274 | DRAWING NO. 8209.03-SK-010

SCALE Full | SHEET 0 OF

Figure 2.10. Instrument mounting

3. ELECTRICAL DESIGN

Schematics for the analog and digital electronic systems of the spectrometer are shown respectively in Figures 3.1 and 3.2. Figure 3.3 gives the location of units on the circuit board. The aim of the design was to achieve a high reliability for the system, together with low power consumption. CMOS devices were used wherever possible, and, when available, components had reliability ratings to MIL-STD-883C. Thus, in the flight models, all except the protection zeners, the photodiode and the EPROMs have this rating. In the prototype model all components are commercial grade. The maximum power required is 1.5 watts.

3.1 ANALOG CIRCUITRY

3.1.1 dc Supply Power Circuit

The instrument is designed to accept a primary supply voltage of 24 to 30 volts (specified as a nominal 28 volts). The $\pm$15 volts required by the electronics is generated by U33 (Integrated Circuits, Inc. MSR2815D dc-to-dc converter). The +5 volts required for the logic circuitry is generated by U34 (L305H voltage regulator) which runs off the +15 volt supply. The T11 provision of Figure 3.3 for zener protection was retained inadvertently after a design revision, and should not be used.

3.1.2 Amplifier/Discriminator and Counter Circuit

The amplifier/discriminator (U24-Amptek Model 101) can be exercised in two ways. The first is in its normal configuration of a proton event discriminator wherein the input signal comes from the channeltron. In the second configuration, the amplifier/discriminator receives its input signal from the microprocessor. This signal is supplied to TP1 and provides a method whereby the amplifier/discriminator can be functionally checked. The check consists of a predetermined number of pulses being applied to TP1. This number can then be compared to the number of pulses "seen" by the amplifier/discriminator as stored in the two 12-bit counters.

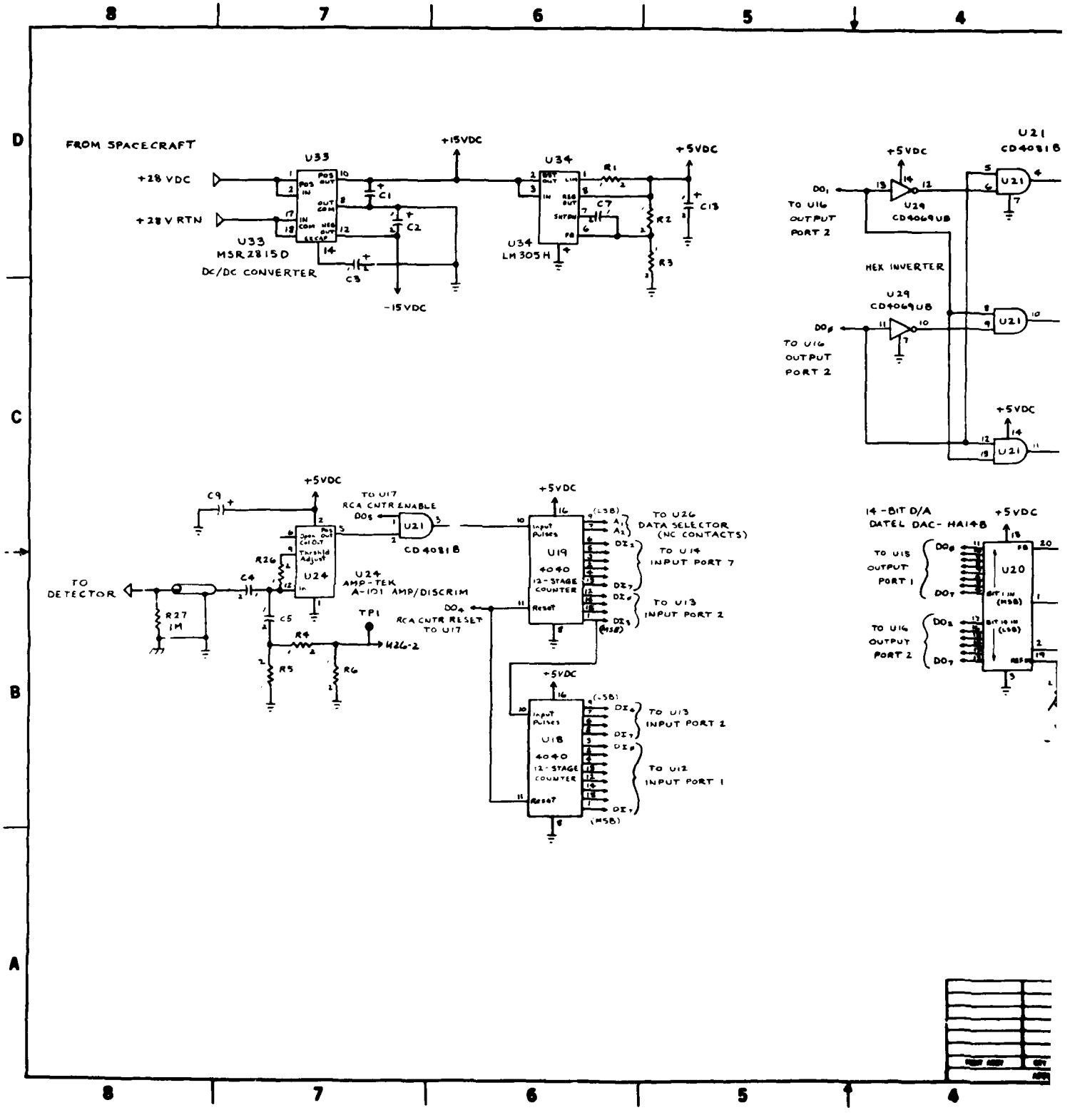
The counters (U18 and U19) are 12-bit counters cascaded together, allowing a maximum count of 2^{24}. To preclude unwanted counts from being registered, the output of the amplifier/discriminator is ANDed (U21) with a signal from the microprocessor which acts as an enable/disable control of the counters. The counters also have a reset under microprocessor control.

3.1.3 High-Voltage Circuit

The negative high voltages for the detector (channeltron) and the analyzer are generated by two Venus Q30Z power supplies (Z1 and Z2). These supplies have a 0.5 to 3 kV dc output which is proportional to a 2 to 12V dc input. The detector is connected directly across one of the power supplies (Z1) which has its positive output terminal at chassis ground. The analyzer is connected across both power supplies which are in a bucking configuration such that the analyzer is at a potential equal to the difference in the output voltages of the two supplies.

The system is designed to allow one of three detector voltages to be selected. These voltages are nominally -2200, -2400 and -2600 volts. The three dc input control voltages to Z1 to yield these three detector voltages are generated by connecting the +15 Vdc supply to the input of Z1 through one of three analog switches (U30, U31, U32). These switches are Harris HI1-5049 and are single-pole four-throw units that are switched by logic commands generated by the microprocessor and decoded by the logic gates of U29 and U21. Each switch has its four sets of contacts wired in parallel so that the "on" resistance of the switch will be reduced to less than 7.5Ω, according to the manufacturer's specifications. In series with each switch and the +15 Vdc supply is a Vishay Model 1285 1000Ω trimmer (R7, R8, R9). These trimmers are used to fine tune the input voltage to the detector power supply (Z1). The trimmers are 26 turn potentiometers selected for temperature coefficient and shock and vibration resistance.

The dc control voltage to the second power supply, Z2, is generated by a 14-bit digital code inputted to U20 (Datel DAC-HA14B D/A converter). The reference (nominally -12 Vdc) for the D/A converter comes from the -15 Vdc supply and is fine tuned with R21, a Vishay Model 1285 trimmer (described above). The output of the D/A converter is connected to U25 which is a Harris HA-2530 operational amplifier. This acts as a current-to-voltage converter, and the output voltage of the op amp drives power supply Z2. With 14 bits of resolution, the least significant bit is theoretically worth 0.18V on the output of Z2.


8
7
6
5
4
D
C
B
A
FROM SPACECRAFT
+28 VDC
+28 V RTN
U33
MSR2815D
DC/DC CONVERTER
+15VDC
-15VDC
C1
C2
C3
U34
LM305H
R1
R2
R3
C7
C13
+5VDC
U21
CD4081B
U29
CD4069UB
HEX INVERTER
DO1
TO U16
OUTPUT
PORT 2
DO8
TO U16
OUTPUT
PORT 2
C9
TO U17
RCA CNTR ENABLE
DO5
U24
AMP-TEK
A-101 AMP/DISCRIM
TO
DETECTOR
R27
1M
C4
C5
R26
R4
R5
R6
TP1
4426-2
DO4
RCA CNTR RESET
TO U17
U19
4040
12-STAGE
COUNTER
TO U26
DATA SELECTOR
(NC CONTACTS)
TO U14
INPUT PORT 7
TO U13
INPUT PORT 2
U18
4040
12-STAGE
COUNTER
TO U13
INPUT PORT 2
TO U12
INPUT PORT 1
14-BIT D/A
DATEL DAC-HA14B
U20
TO U15
OUTPUT
PORT 1
TO U16
OUTPUT
PORT 2

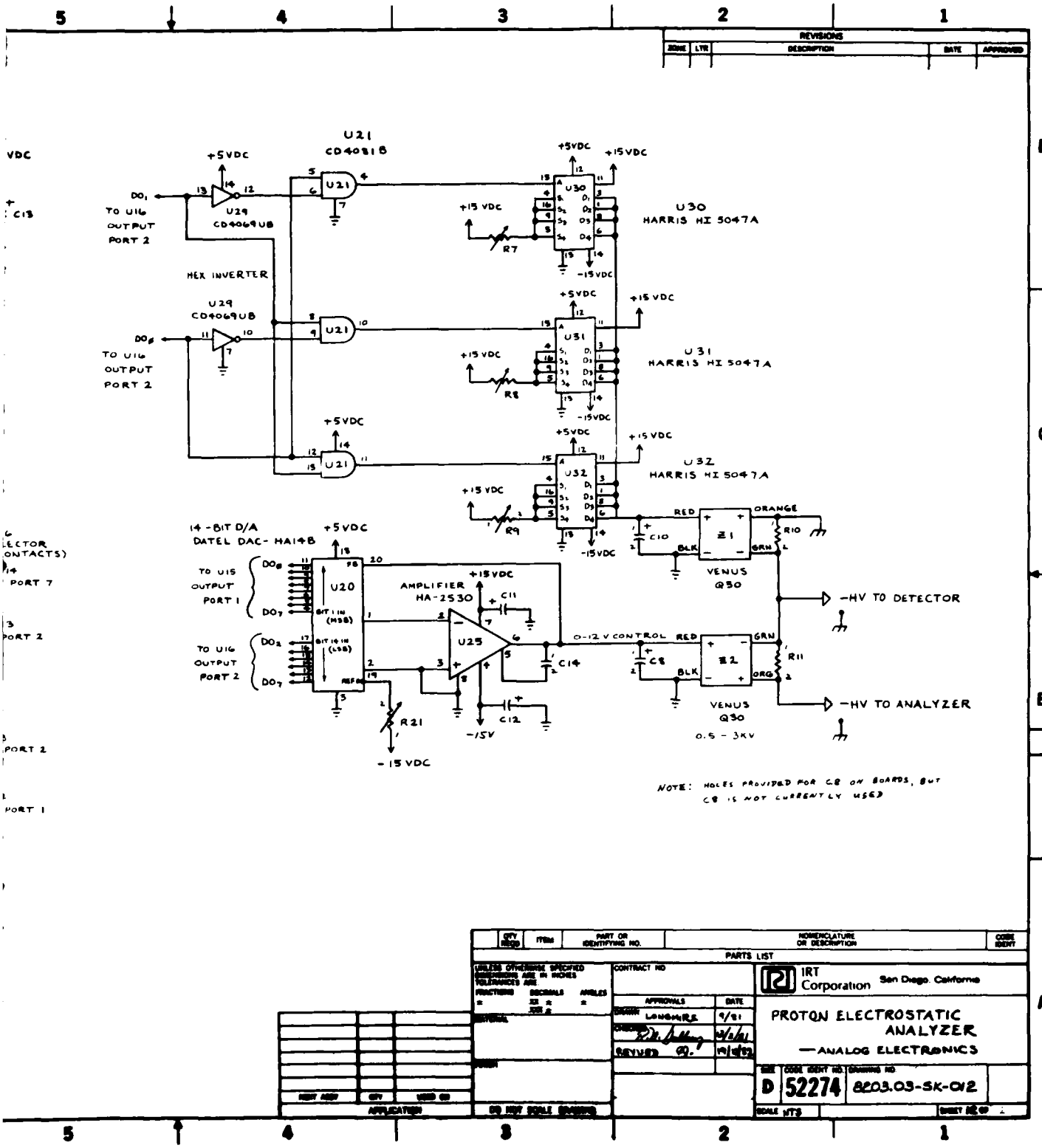
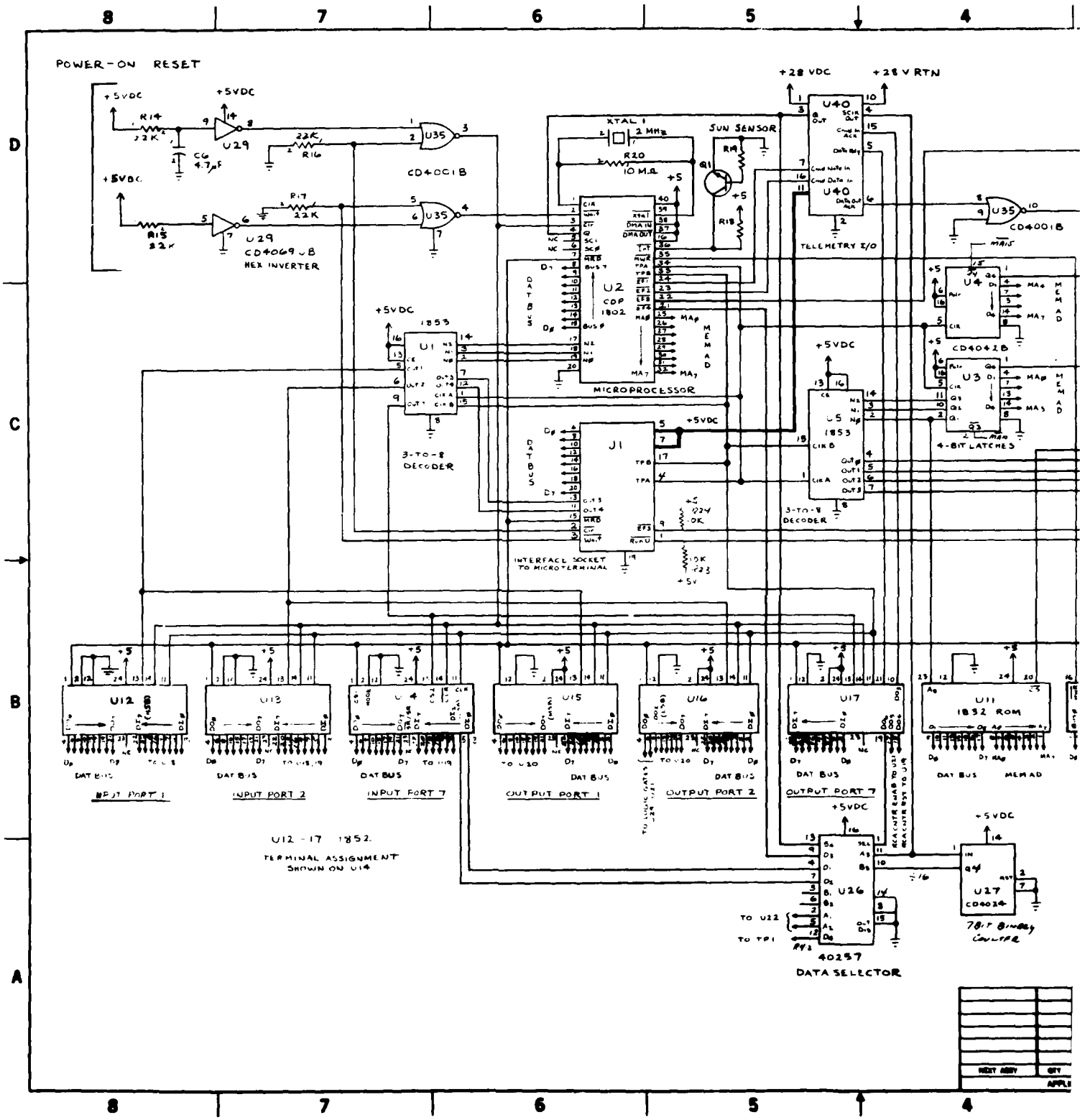


Figure 3.1. Analog schematic


POWER-ON RESET
+5VDC
R14
22K
C6
4.7μF
U29
R16
22K
U35
CD4001B
R17
22K
R15
22K
U29
CD4069UB
HEX INVERTER
XTAL 1
2 MHz
R20
10 M.Ω
Q1
SUN SENSOR
R19
R18
+28 VDC
+28 V RTN
U40
TELEMETRY I/O
U2
CDP 1802
MICROPROCESSOR
U1
1853
3-TO-8 DECODER
J1
INTERFACE SOCKET TO MICROTERMINAL
U5
1853
3-TO-8 DECODER
U4
U3
CD4042B
4-BIT LATCHES
U12
U13
U14
U15
U16
U17
U11
1832 ROM
INPUT PORT 1
INPUT PORT 2
INPUT PORT 7
OUTPUT PORT 1
OUTPUT PORT 2
OUTPUT PORT 7
DAT BUS
MEM AD
U12 - 17 1852
TERMINAL ASSIGNMENT SHOWN ON U14
U26
40257
DATA SELECTOR
U27
CD4024
7 BIT BINARY COUNTER

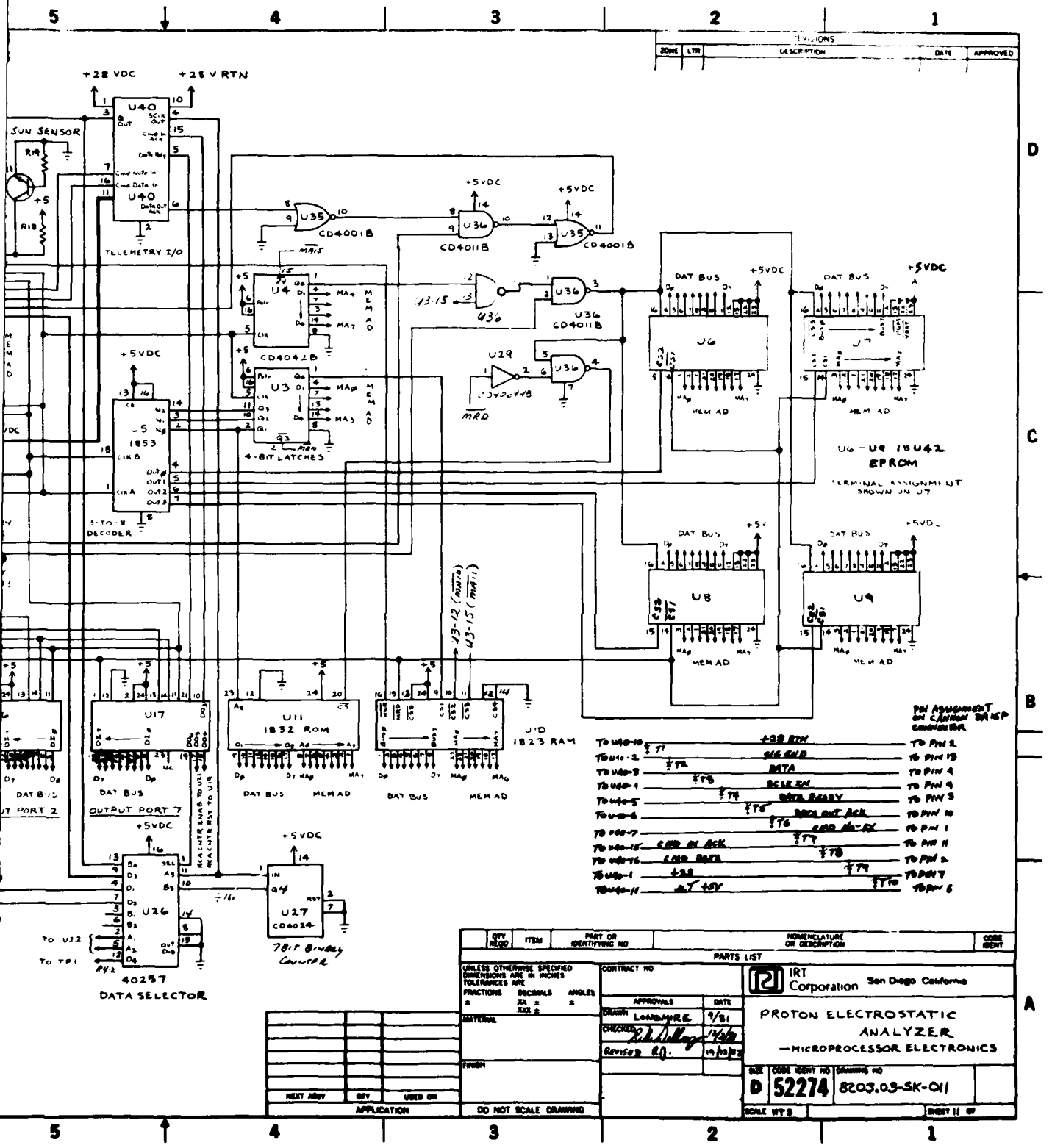


Figure 3.2. Digital schematic

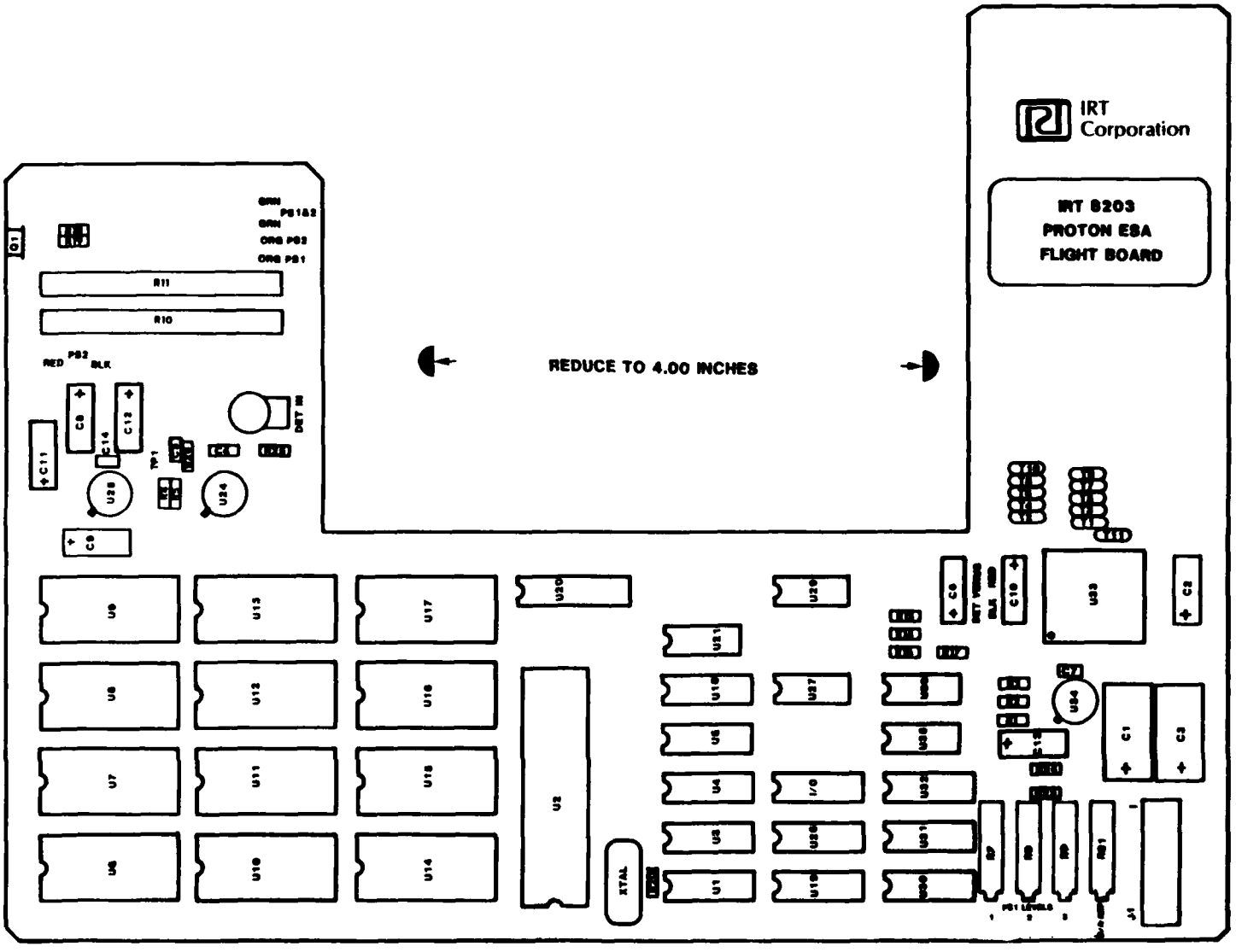


Figure 3.3. Flight board component layout 29/30

The bias for the channeltron (V_c) is supplied by the dc-to-dc converter Z1 (Venus Q30Z) controlled from U30, U31 and U32. The entrance of the multiplier may be held at voltages of -2200V, -2400V or -2600V. The collection end of the detector is held above case ground by a 1 MΩ resistor.

The 14-bit analog accuracy available from the D/A converter (U20) is used to control the output of the operational amplifier (U25), which in turn is the input to the high-voltage dc-to-dc converter Z2. The output of Z2 floats as a positive voltage or the negative output of Z1, the difference, with respect to case ground becoming the negative plate potential (V_a). The Z2 output, and hence the analyzer voltage, is determined from a look-up table in memory. The theoretical accuracy for the plate voltage is $\pm$0.1V.

As Z1 and Z2 are relatively high-power devices, there is a tradeoff determined between power requirements in this subsystem and response times (and, to a lesser extent, stability) of the analyzer voltage. Z1 is loaded with the detector and a 300 MΩ resistor in parallel, a total of about 200 MΩ. Z2 is loaded with 100 M . Under these conditions maximum power consumption by the two converters alone (disregarding the efficiency of U20) is about 300 mW. Increasing the loads to a maximum rating would raise the requirement to 1500 mW. Specifications for Z1 and Z2 are shown in Appendix A.

Differential voltages for Z1 and Z2 are set digitally in the look-up table. The analog voltages are then tuned in the following manner:

1. The detector bias (V_c) is set to -2200V (Step 01) using trimming resistor R7.
2. Analyzer voltage (V_a) for Step 0 (000) is set to -7.3V with R21.
3. Analyzer steps 1 to 7 are then measured and noted.
4. Steps (2) and (3) are repeated for a -2400V bias (10) and V_a (000) set to -7.3 with R8.
5. Steps (2) and (3) are repeated for V_c = 2600V with V_a (000) set to -7.3 with R9.

Results from these procedures for the three models are given in Section 4.

With V_a = 2200V the average gain of the detectors is over 10^7. The charge pulse appearing at the collector cap is taken out by shielded cable through capacitor C4 into the charge sensitive amplifier/discriminator U24. This is an Amptek A101 PAD which is sensitive to charge pulses down to 10^6 electrons. Its specifications are shown in

Appendix C. The discrimination level is set by the value of R26. Without a trimming capacitor to increase pulsewidth, its output is a +5V square pulse of width 220 ns. This pulsewidth provides a known counting rate dead time for the spectrometer.

An entry port (TP1) is provided for pulsed input (1 to 5V) to test counter functions.

3.2 DIGITAL ELECTRONICS

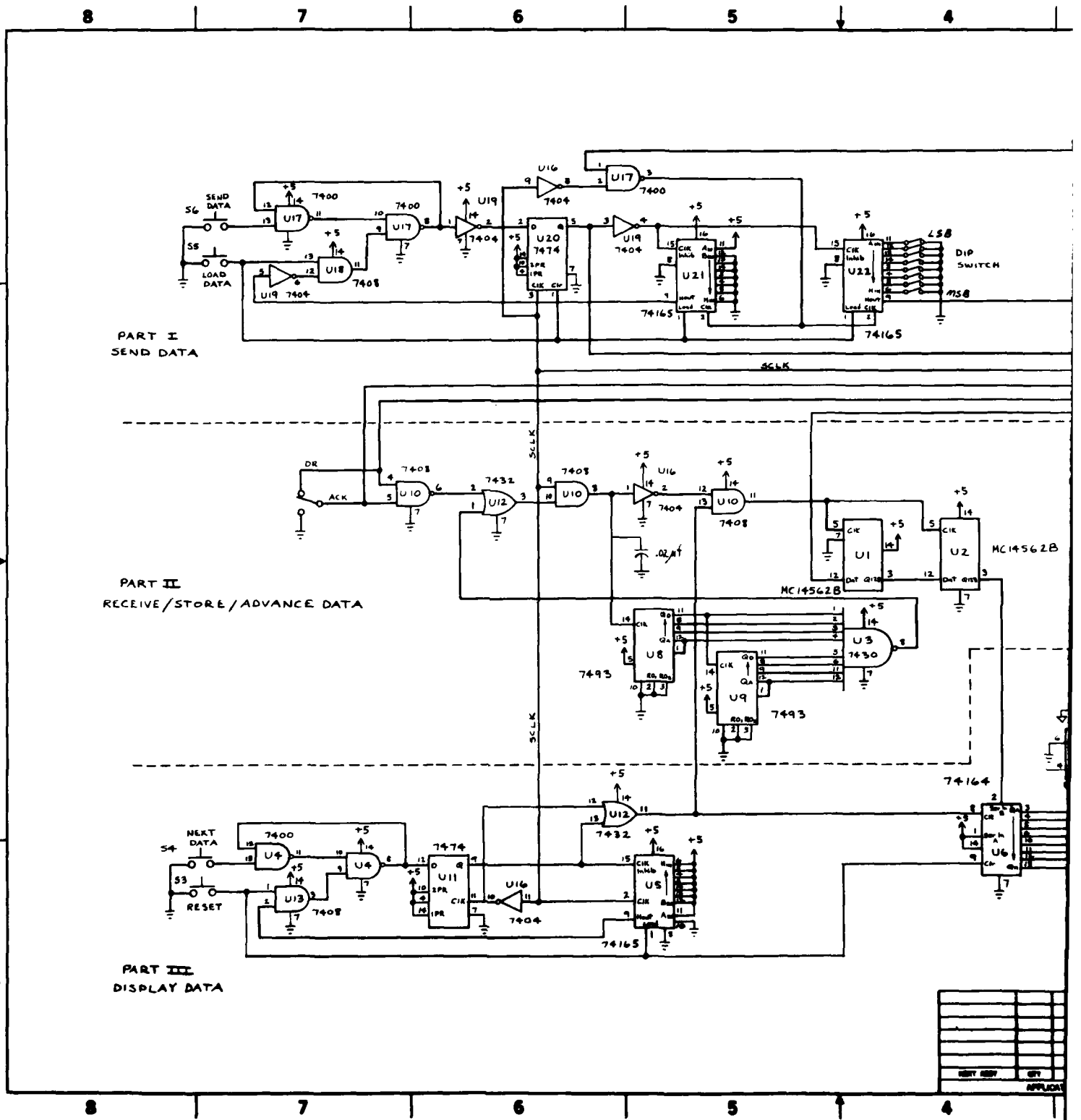
The schematic of the microprocessor circuitry is shown in Figure 3.2. The auxiliary circuit schematics for the I/O simulator and the EPROM programmer are shown in Figures 3.4 and 3.5.

The following sections describe the programming and logic used in the instrument.

3.2.1 Initialization

This set of software is used to initialize the instrument. When power is applied the CPU is driven to location 00 and the first function is to disable the interrupt until it is needed to recognize the Sun. The initial condition of the registers is as follows:

R0
R1 = 02B3 Interrupt Pointer Address
R2 = 8C6E Check Sum Storage Address
R3 = 0210 Output Subroutine Address
R4
R5
R6
R7 = 02
R8
R9
RA
RB = 0000 Timer
RC
RD = 00
RE
RF = 0200 used as the addresses for output volts.


8
7
6
5
4
D
C
B
A
SEND DATA
S6
LOAD DATA
S5
7400
7408
7404
U19
U20
7474
U21
74165
DIP SWITCH
PART I
SEND DATA
SCLK
DR
ACK
7432
.02μf
MC14562B
U1
U2
PART II
RECEIVE/STORE/ADVANCE DATA
7493
U8
U9
U3
7430
74164
U6
NEXT DATA
S4
S3
RESET
U11
U5
PART III
DISPLAY DATA

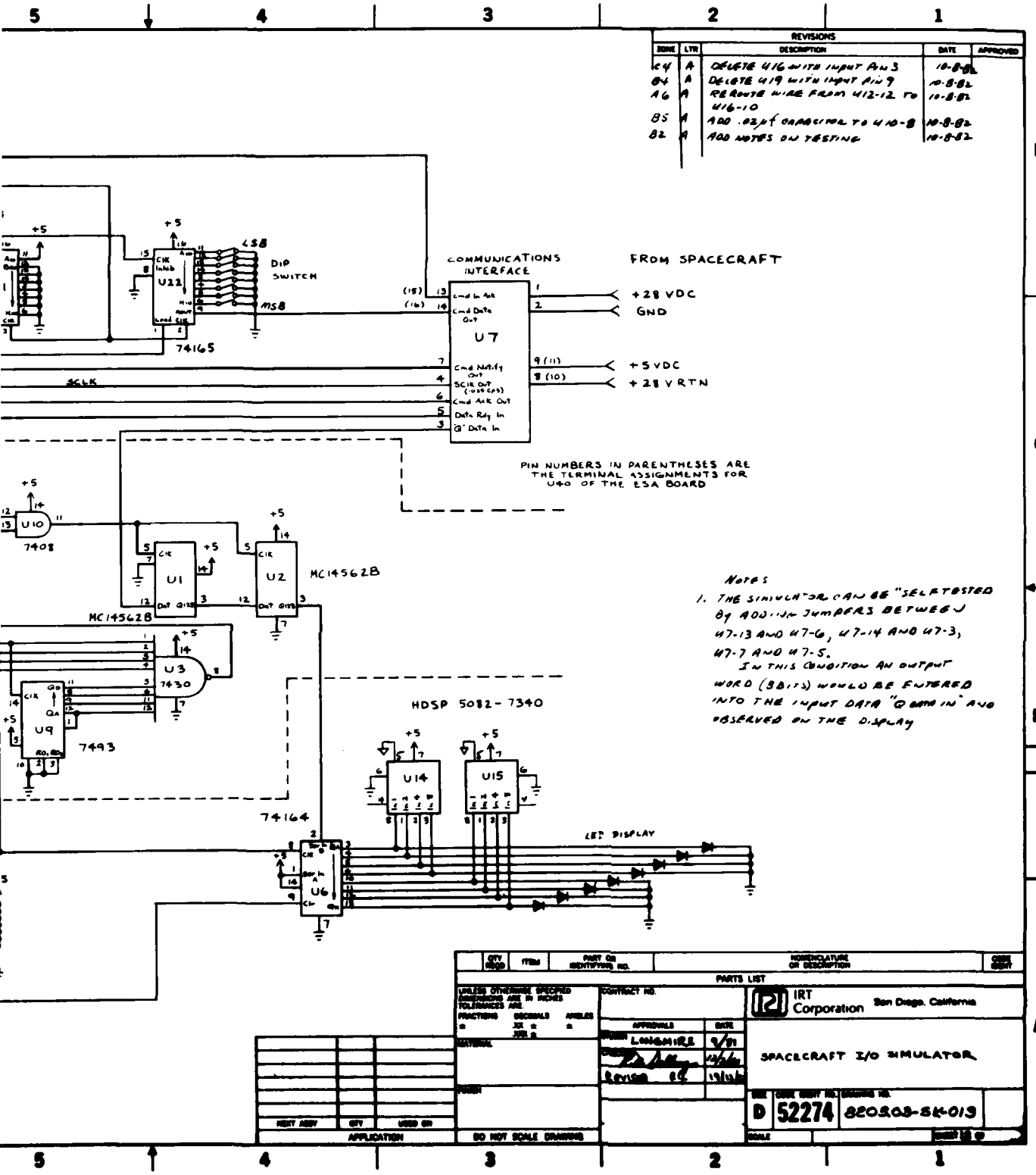
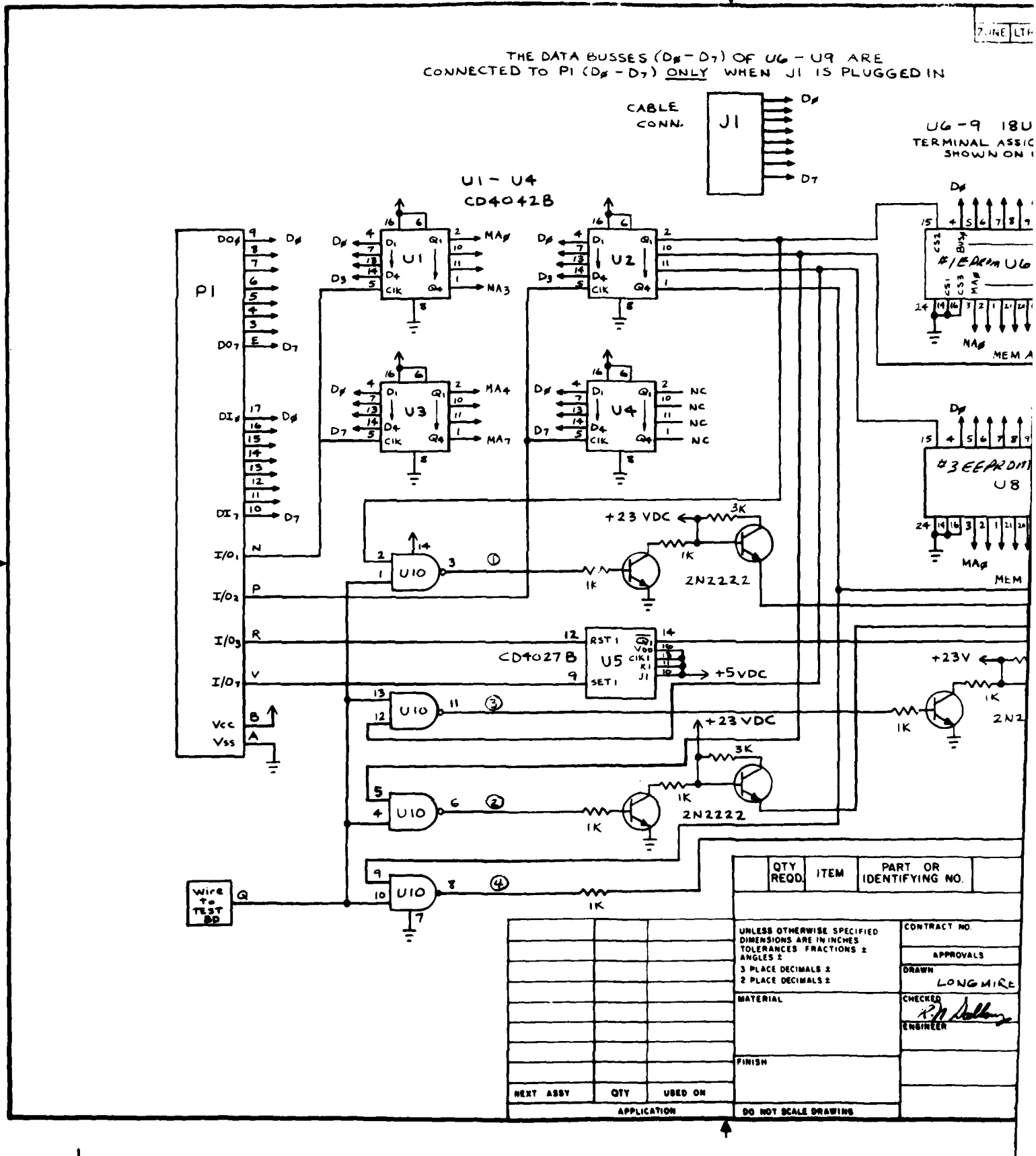


Figure 3.4. I/O simulator


THE DATA BUSSES (D0 - D7) OF U6 - U9 ARE CONNECTED TO P1 (D0 - D7) ONLY WHEN J1 IS PLUGGED IN
CABLE CONN.
J1
U1 - U4
CD4042B
P1
U1
U2
U3
U4
U5
U6 - 9 18U
TERMINAL ASSIG
SHOWN ON
MEM A
MEM
U8
+23 VDC
3K
1K
2N2222
U10
CD4027B
+5VDC
+23V
2N2
Wire to TEST BD
QTY REQD.
ITEM
PART OR IDENTIFYING NO.
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES FRACTIONS ±
ANGLES ±
3 PLACE DECIMALS ±
2 PLACE DECIMALS ±
MATERIAL
FINISH
CONTRACT NO.
APPROVALS
DRAWN
LONGMIRE
CHECKED
ENGINEER
NEXT ASSY
QTY
USED ON
APPLICATION
DO NOT SCALE DRAWING

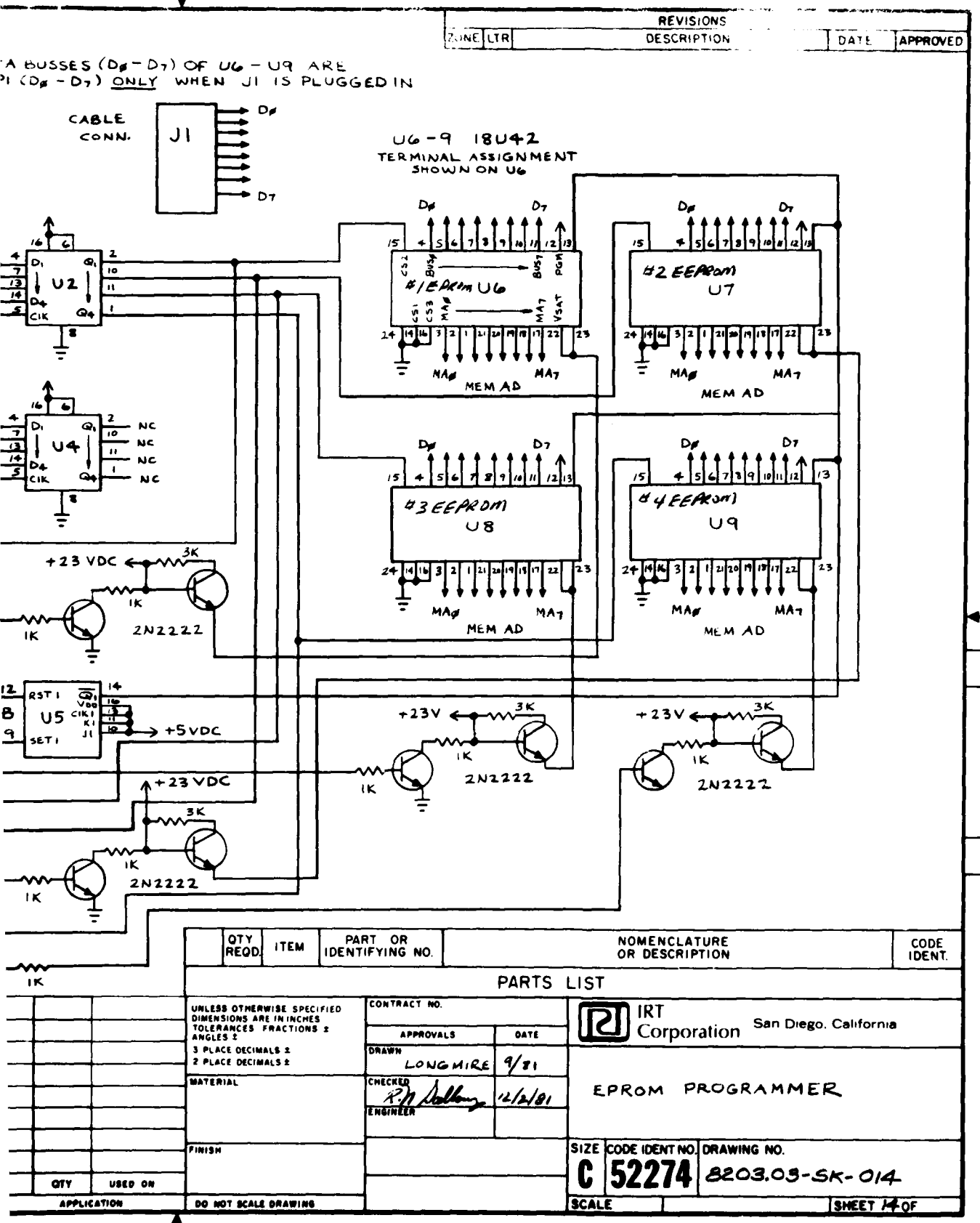


Figure 3.5. EPROM programmer

The Check Sum is accomplished starting at location 21 and completed at location 31. The Check Sum is accomplished by:

X REG Assigned to RB, RB = 0000 Putting RD.1 into D, Adding M(R(X)) + D → D Putting that sum into D.1, incrementing B and subtracting 03 to determine the end of the routine by testing D for not equal to zero, if it is not equal to zero branch to location 22 with the new address that is in RB and repeating the add operation until RB.1 = 03, at which time the contents of D.1 are stored relative to R2 which has the address 8C6E. The Check Sum in 8 bits is stored at 8C6E and D.1.

3.2.2 Test Counter

This routine tests the 24-bit data counter to determine that its operation is acceptable. This is accomplished by putting FE00 counts into the counter and checking the output for that number. The routine is implemented in the following way.

REG F is set to 0201, the address of the control bits that resets the data counter via the out 7 command. REG E is set to FE00, the value which will be countdown. Q is reset. Q will be the counter driver and is switched to the counter input with the instruction that is stored at location 241. The sequence starting at 23D sets the X REG to F, resets the counter, relieves the reset and diverts the Q output to the amplifier input that drives the counter. Q is set, E is decremented, Q is reset, E is tested for zero; if E is not zero the program loops back to set Q again and the loop continues. When E is equal to zero, the count is stopped and data from the counter is input to D and tested for the correct data, i.e., 00FEXX. The LSB of D.1 is set with a 1 if the test is successful and a zero if the test was unsuccessful. Register D.1 contains diagnostic data. The LSB from the Check Sum is discarded. The diagnostics are complete and D.1 is not used or read except to output data. The program branches to location 0035.

3.2.3 Input Subroutine

The address for the input subroutine is completed by adding 0090 to R7. R7 now contains 0290, the address of the input subroutine. The branch is accomplished by changing the program counter to REG 7 with the instruction SEP R7 (D7).

At location 290 the program branches to 280 to set up and save register values. The bit counter R6.0 is loaded with 08 (the number of bits in the input word), the low order bits of RF.0 are saved in RE.0. This address is saved in order to preserve

continuity from wherever the program came and to use the REG F for the input subroutine. REG F is then loaded with the address 0209 (08). 08 is the acknowledge command when out 7 is executed. The X REG is then set to REG F and the program branches to location 0292 which awaits an input command. After receipt of an input command the system clock going high, the acknowledge command is output with out 7. (RF(020A)). When the system clock goes low, the contents of R5.1 are loaded into D and a shift left command is given (0 LSB of D). EF2, the command input, is tested for zero. A zero causes the contents of D to be stored in 5.1, the bit counter decremented and tested for zero. If the bit counter is zero, the program branches to EXIT, restores RF to the original value and the program counter is reselected to be REG 0. If a one was detected on EF2, an 01 is added to D, and the data stored in 5.1, bit REG, is tested. The bit register will be zero when eight data bits have been read and stored in R5.1. REG 5.1 contains the command word that was last received. After the initial reading of the command word, the program would normally jump to location 39 (EXECIN). When the system clock = 1, register 5.1 is transferred to REG 5.0 and REG 6.1. REG 5.1 is then loaded with 00.

3.2.4 Execute Same Command

If the command is to be repeated, the entry is at location 041.

The X REG, REG 2 for the interrupt is set to 8C6E. R2 will be the X register. The command in 6.1 is read into the D REG. The input command is tested for "IGNORE THE SUN SENSOR" (01), the seventh bit. The interrupt is disabled if the sun sensor is to be ignored and enabled if it is required.

The input word is entered into D and tested for the sweep or dwell mode. The dwell mode is true if bits 5 and 6 are true, the exclusive or will cause the register to be zero if it ' true and the program will jump to location 160 and execute the dwell mode. If it is not zero, the program jumps to location 00F0 which is the start of the sweep mode.

3.2.5 Dwell Mode

The initial step is to ask if an input command is ready. If a notify command is present, the program would jump to read the command and then return to location 169. Register 7 should always contain the address of the input routine except when that routine is being executed.

The current command is read into D and anded with F8 to delete the least significant three bits. The remains is shifted two places to the right to form part of the address for the voltage data. This value is part of the address for the X register which will be the A register, and is stored in RA.0. The high-level address is 03 and is stored in RA.1. The voltage data address is now complete (03XX) = 0000 0011 0XXXXX0, the start is always at even number. The X REG is set to A and the sun sensor storage location is checked to see if the sun has been seen in order to not override and turn on the power supplies. If the sun has been seen, the routine continues without the prescribed power supply voltage. If it has not been seen, the power supplies are set with the output commands and the routine continues.

The countdown time is set to 10 seconds, RB the countdown register is loaded with 0500 and the X REG address is set to 201. The contents contains the command to reset the counter. The X REG is assigned to RF. Following the reset command the reset is relieved and the divided down system clock called "SLOW CLOCK" is activated. A 50 ms delay is generated and executed. The program then looks to see if an input command is ready; if not, the program awaits the system clock going high, after which the data counter is enabled for ten seconds by decrementing the B register to zero and then disabling the data counter. The input command is interrogated; if not active, the data-ready command is generated (at 01B5) and the system awaits the acknowledge command. After acknowledge is received, the bit counter R6.0 is loaded with 08 and the first eight bits of data from the data counter is input to the D register and the output subroutine located at the address (0210) in R3 is called.

3.2.6 Output Subroutine

The output subroutine outputs data via the Q line based on the data in D and the number of stored bits in the bit counter (R6.0). The data is shifted to the left, which causes the MSB to be shifted into DF and Q is set to the same state as DF when the system clock goes to 1. This process continues until the bit counter is decremented to zero and the routine drives back to where it came from and executes the next instruction. In this case the return is to location 01BF. The bit counter is loaded with 08, the second eight bits of data are loaded from the data counter to the D register and the output subroutine is used to output the data via the Q line. The third set of eight bits is then loaded and output. Following transmission of the third set, the program goes back to 01CA and the bit counter is loaded with 04 to output three energy bits and the sun sensor status bits.

Following the above four bits, the command word (eight bits) is taken from R6.1 and put in the D register for transmission. The last eight bits to be transmitted is the diagnostic data that is stored in D.1. After that transmission the data ready line is taken to zero and Q is reset. Summarizing,

SWEEP Mode Register Designation
RA = Voltage Output Code
RB = SWEEP Time
RF = 0201
RE = BOBO ~500 ms
SEX RF
REG C = 8C00
R6.0 = SWEEP CNTR (Number of Steps) = 08
RB is put in R8
RE = E REG set to 1010 ~50 ms.

The output word consists of the following: (1) Twenty-four bits of counter data, (2) four bits, the last of which is sun status, (3) the command word, (4) the diagnostic data; the first seven bits is the Check Sum, the last bit is the counter test status where a one is acceptable, a zero indicates a fault.

3.2.7 New Command/Old Command

The future command register is loaded into D from R5.1 and tested for a zero. If it is zero, the program branches to "SAME COMMAND" at location 0041. If R5.1 is nonzero, the program branches to EXECIN at location 0039 where the "NEW" command is loaded into R5.0 and R6.1 and 5.1 is set to 00 and the program then proceeds to location 0041 and the command is executed.

3.2.8 Sweep Mode

The sweep mode (Location 61) is executed if the dwell mode is not selected. If bits 1 and 2 are one, the dwell mode is selected. The code in bits 1 and 2 dictates the sweep time.

The code immediately branches to location FO where the channeltron code is shifted to the low order of REG A and the high order set to 03. The address that is located in REG A is 03X0, 00000011 00XX0000. The program then branches back to

location 068 where the sun sensor is tested for a positive indication prior to setting the initial values for the power supplies. If the sun has not been seen, the voltages are set by setting the X REG to RA and outputting the values from the address in RA.

The countdown timer R8 is set to 0000 and the sweep time is broken out of the command word with the instruction AND IMMED 06. If zero, the time is 0.25 s, if the 1 bit is set the time is 10 seconds and the other choice is one second. Based on the sweep time, the countdown timer is set to 0020 for 0.25 second, 0080 for 1.0 second and 0500 for 10 seconds.

3.2.9 Check Input Command Request

The notify line is tested to see if a new command is being sent. The input command is read by the input subroutine.

Following the input command inquiry the F REG is set to 0201 by setting the lower order bits to 01. A delay of 500 ms is set and executed by counting down the E register from BOBO to zero.

The data counter is reset by an output to port 7 of 10, the reset command, the reset command is relieved and the slow clock ~1 kHz started. The data storage is initialized at 8C00 and the address is located in register C. The sweep register or the number of analyzer steps is set to 08 and put in register 6.0. The sweep time is saved ir register 8. The delay time of 50 ms is set into the E register and the delay is exercised. The delay is required to allow the power supplies to settle. When the clock goes high the data counter is enabled and REG 8 is decremented to zero the countdown for sweep time. When the countdown is complete, the data counter is disabled. Data is stored in locations that are addressed by REG C. The first eight bits from the input port is stored in 8C00, second in 8C01, third in 8C02. The D.0 register is stored in 8C03. The second set of data is stored in 8C04 through 8C07, the third in 8C08 through 8C0B, etc. The sweep code is stored in the three most significant bits of REG D.0.

The sweep count is decremented and tested for zero. If not zero, the cycle is repeated with new voltages. When the sweep is complete the data is output at location 0100.

3.2.10 Sun Sensor Response

The sun sensor is connected to the interrupt input of the CPU. During "INITIALIZE" the R1 register is set to 02B3 the address of the interrupt processing.

When the input command is executed, the sun sensor register (D.0) is set to zero. The input command in 5.0 is looked at to see if the "IGNORE THE SUN SENSOR" command was received, bit 7, #01. If the "IGNORE" command was received, then the X REG is set to zero and the interrupt is disabled. If "DO NOT IGNORE" was received, the program jumps to location 0056 (X to 0) and the interrupt enabled by using the return (70) instruction. At the start of the sweep and dwell modes the sun sensor register D.0 is looked at prior to setting the voltages to be sure that an activated interrupt is not overridden. When new voltages are to be set the sun sensor register (D.0) is looked at prior to setting new voltages so that the interrupt is not overridden.

3.2.11 Interrupt Routine

After the interrupt is enabled (return) and the sun sensor sees the sun, the program jumps to location 0283. Register 2 was initialized at 8C6E. The contents of R2 are decremented to 8C6D and the save instruction is given, storing X and P register numbers in 8C6D. R2 is decremented to 8C6C and the CPU "D" register (accumulator) is stored in 8C6C and the X REG is decremented with the STXD instruction R2 = 8C6B. RF.0 is stored in 8C6B and R2 is decremented to 8C6A. RF.1 is stored in 8C6A and R2 is decremented to 8C69. The sun sensor status is set true, D.0 contains (10). The F register is set to 0200; 0200 contains 00. The F REG is set to the X REG and the out 1, out 2 instructions are given, along with keeping RF set to 0200. This operation causes the power supplies to be set to zero.

In order to exit the interrupt routine without enabling the interrupt, the instructions set P and set X are manufactured based on the contents of 8C6D. The original value for X and P was stored in this location with the save instruction. The "X" bits, the four MSB's are deleted with the and immediate #OF and DO is or'd with the value to obtain the set P instruction "DN." The DN is stored in 8C6D relative to the X REG which is R2. R2 is decremented to 8C6C. The X REG is set to F, whose contents contain 8C6D. The contents of 8C6D (X,P) is loaded into the accumulator and shifted four bits to the right which puts the value of X in the four LS bits. The set X instruction is formed by ORING EO with the X value and EX is obtained. This value is stored relative to X (R2 set to X) at location 8C6C and R2 is decremented to 8C6B. The exit instructions will be EX and DN, which sets X and P to the original values.

The F register and the D accumulator is restored by incrementing the X REG and R2 three places to 8C6E.

3.3 CHECKOUT OF ANALYZER

1. Check Power and GND
2. Install components
3. Apply Power through Simulator Cable, assuring that the connector is keyed properly.
4. Measure current from 28 Vdc supply. Current should be less than 40 mA.
5. Measure ±15, +5V outputs at appropriate locations on board. Fifteen volts should be ±2V, 5V should be ±0.5V.
6. Check components for overheating, i.e., U25, U24. Burned fingers require removal of power and proceed with locating problems.
7. If overheating is not a problem, proceed with the following checkout.
8. U24 should have no digital output. U25 should be approximately 0V; dc oscillations should not appear, except for CPU clock noise.
9. When power is applied, the CPU should start by addressing location 0000 which disables the interrupt, initializes the registers, sets the power supplies to zero, does check sum, counter test (location 230), then at location 38 jumps to the input subroutine (location 290) and awaits an input command from the simulator. Cursory checks are made by looking with a scope to see if memory chip #1 (U6) is first addressed then jumps to memory chip #3 (U8) to do counter test, back to #1 and back to #3 for input routine. After a command has been received the command should be executed.
10. Dwell mode.

3.4 SOFTWARE LISTING

		INITIALIZE	
00	DISABLE	71	
01		00	X=0, P=0
02	LDI	F8	
03		#02	
04	PHI R3.1	B3	
05	PHI R1.1	B1	
06	PHI RF.1	BF	
07	PHI R7.1	B7	
08	LDI	F8	
09		"00	
0A	PLO RF.0	AF	
0B	PHI RB.1	BB	RB = 0000
0C	PLO RB.0	AB	RF = 0200
0D	PHI RD.1	BD	
0E	LDI	F8	
0F		#B3	
10	PLO R1.0	A1	R1 = 02B3
11	LDI	F8	
12		#8C	
13	PHI R2.1	B2	R2 = 8C6E
14	LDI	F8	
15		#6E	
16	PLO R2.0	A2	
17	LDI	F8	
18		#10	R3 = 0210 OUTPUT SUBROUTINE
19	PLO R3.0	A3	
1A	SEX RF	EF	
1B	OUT1	61	
1C	DEC RF	2F	SET Hi Volts to Zero
1D	OUT2	62	
1E	DEC RF	2F	
1F	OUT7	67	RF (201)
20	NOP	C4	
21	SEX B	EB	
22	GHI D.1	9D	
23	ADD	F4	ADD Contents of D with Contents
24	PHI RD.1	BD	of Memory as Addressed by X
25	INC RB	1B	
26	GHI RB	9B	
27	SUB IMMED	FD	CHECKSUM
28		#03	
29	BNZ	3A	
2A	ADDRESS	22	
2B	GLO RB	8B	
2C	SDI SUBIMM.	FD	
2D		#FF	
2E	BNZ D =/ 0	3A	
2F	ADDRESS	22	

30		GHI D.1	9D	Store CHECKSUM in RAM 8C6E Check
31		STR VIA R2	52	Sum for Test Purposes
32		LBR	C0	
33		ADDRESS	02	
34		ADDRESS	30	Branch to Counter Test At Loc 230
35		LDI	F8	
36			#80	
37		PLO	A7	R7 = 0280 INPUT Subroutine
38		SEP D7	D7	Program Jump to the INPUT Subroutine
39	EXECIN	B4	37	ESCAPE when SYS CLK = 1 = EF4,
3A		ADDRESS	39	A NEW COMMAND was RECD.
3B		GHI 5.1	95	5.1 Contains NEW COMMAND
3C		PLO 5.0	A5	5.1 into 5.0 and
3D		PHI 6.1	B6	SAVED in 6.1
3E		LDI	F8	
3F			#00	
40		PHI 5.1	B5	R5.1 = 00
41	SAME CMD	LDI	F8	ENTRY HERE is a rerun of the
42			#8C	Old Command
43		PHI	B2	
44		LDI	F8	XREG Value for the INTERRUPT.
45			#6E	R2 Becomes the XREG.
46		PLO R2.0	A2	R2 = 8C6E
47		GHI 6.1	96	Command is taken from 6.1 and put
48		PLO R5.0	A5	in 5.0
49		LDI	F8	
4A			#00	SUNSENSOR REG is set to Zero
4B		PLO RD.0	AD	RD.0 = 00
4C		GLO R5.0	85	See if Input Command Asks to
4D		ANDI	FA	Ignore SUNSENSOR by Looking at Bit 7.
4E			#01	
4F		BZ D=0	32	(Patch)
50		ADDRESS	E2	Do Not Ignore SUNSENSOR
51		SEX R0	E0	-- Ignore SUNSENSOR
52		DISABLE	71	DISABLE INTERRUPT If Asked to
53			#00	Ignore SUNSENSOR.
54		BRANCH	30	
55		ADDRESS	59	
56		SEX R0	E0	
57		RETURN	70	Enable INTERRUPT
58			#00	This Number is Arbitrary (Value)
59		GLO	85	Look at CMD to Determine if the
5A		ANDI	FA	Dwell or Sweep Mode Should be Used.
5B			#06	
5C		XRI	FB	Exclusive or Immed.
5D			#06	
5E		LBZ	C2	Long Branch to DWELL MODE
5F		ADDRESS	01	DWELL MODE ADDRESS
60		ADDRESS	60	
61	SWEEP	BRANCH	30	Channeltron Bias SWEEP Time
62		ADDRESS	F0	7 6 5 4 3 2 1 0 -- SUNSENSOR Ignore
63			C4	Analyzer Volts

```
64
65
66
67
68                  GLO RD.0
69                  BNZ
6A                  ADDRESS
6B                  SEX RA
6C                  OUT 1
6D                  OUT 2
6E                  LDI
6F
70                  PHI RB.1
71                  PLO RB.0
72                  GLO R5.0
73                  ANDI
74
75                  BR,D=0
76                  ADDRESS
77                  ANDI
78
79                  BR,D=0
7A                  ADDRESS
7B                  LDI
7C
7D                  PLO RB
7E                  BR
7F                  ADDRESS
80                  LDI
81
82                  PHI RB
83                  BR
84                  ADDRESS
85                  LDI
86
87                  PLO RB
88 RSTCNTR          B1
89                  ADDRESS
8A                  SEP R7
8B                  LDI
8C
8D                  PLO RF
8E                  LDI
8F
90                  PHI RE
91                  PLO RE
92                  DEC RE
93                  GHI RE
94                  BNZ
95                  ADDRESS
96                  SEX to F
97                  OUT 7
```

```
C4
C4
C4
C4
8D
3A
6E
EA
61
62
F8
#00
BB
AB
85
FA
#06
32
85
FA
#02
32
80
F8
#80
AB
30
88
F8
#05
BB
30
88
F8
#20
AB
34
8B
D7
F8
#01
AF
F8
#B0
BE
AE
2E
9E
3A
92
EF
67
```

If SUNSENSOR True Do Not Set Output Voltages

RA = 03 X 0
RA = 03 X 1
RA = 03 X 2

RB = 0000 Countdown Timer Count is Added Below.
Determine the SWEEP Time

*.25 Sec *

10 Sec

1.0 Sec

RB = 0080 into TIMER

RSTCNTR

RB = 0500

RB = 0020

Branch if Notify (EF1) = 0
READ an Input CMD if Notify = 1

Set RF to 0201

Delay 500 msec
RE = BOBO

Reset Counter
Output 0001 0000 to Port 7

	98	NOP	C4	RF = 201 (10)
	99	OUT 7	67	RF = 202 (40) Slow Clock, Relieve Reset
	9A	LDI	F8	Initialize Data Storage Pntr. to 8C00
	9B		#8C	
	9C	PHI	BC	Register C = 8C00
	9D	LDI	F8	
	9E		#00	
	9F	PLO	AC	
	A0	LDI	F8	
	A1		#08	Initialize SWEEP CNTR R6.0 = 08
	A2	PLO R6.0	A6	or the Number of Analyzer Steps
TIMER	A3	GHI	9B	Countdown Timer RB
	A4	PHI	B8	RB.1 R8.1
	A5	GLO	8B	The SWEEP Time is Saved
	A6	PLO	A8	in the B REG and Counted Down in
	A7	LDI	F8	the 8 REG.
	A8		#10	
	A9	PHI	BE	RE = 1010 = 50 mSec
	AA	PLO	AE	
	AB	DEC	2E	
	AC	GHI	9E	50 mSec Delay
	AD	BNZ	3A	
	AE	ADDRESS	AB	
	AF	NOP	C4	
	B0	B4	37	ESCAPE when Slow Clock = 1
	B1	ADDRESS	B0	
	B2	OUT 7	67	203 = RF (60) Start Counter
	B3	BN4	3F	ESCAPE when SLOW CLK = 0
	B4	ADDRESS	B3	
	B5	B4	37	ESCAPE when SLOW CLK = 1
	B6	ADDRESS	B5	SWEEP TIME
	B7	DEC R8	28	Decrement Countdown Timer
	B8	GLO R8	88	LOAD Countdown And Test
	B9	BNZ	3A	for Zero
	BA	ADDRESS	B3	
	BB	GHI	98	
	BC	BNZ	3A	
	BD	ADDRESS	B3	
	BE	OUT 7	67	204 = RF = (00) STOP CNTR, FASTCLK
	BF	SEX to C	EC	X REG for Input Data is REG C.
	C0	INP 1	69	8C00 Input Data to RAM
	C1	INC	1C	
	C2	INP 2	6A	8C01 Input Data to RAM
	C3	INC	1C	
	C4	INP 7	6F	8C02 Input Data to RAM
	C5	INC	1C	
	C6	GLO	8D	
	C7	STR	5C	8C03
	C8	INC	1C	8C04 D.O Into 8C03
	C9	ADDI	FC	
	CA		#20	Increment SWEEP Code (Bit 5)
	CB	PLO RD.0	AD	XXX0 0000

CC	DEC	26	DEC SWEEP # COUNT
CD	GLO	86	Test for Complete and
CE	LBZ	C2	If True Branch to Output Data
CF	ADDRESS	01	
D0	ADDRESS	00	
D1	SEX RA	EA	
D2	GLO	8D	Not Zero Means the Sun was Seen
D3	ANDI	FA	and the New Voltages Should Not
D4		01	Be Set. D7 and D8 are Bypassed.
D5	BNZ	3A	
D6	ADDRESS	D9	
D7	OUT 1	61	
D8	OUT 2	62	Voltages are Output from
D9	SEX RF	EF	the Address in A REG.
DA	OUT 7	67	
DB	NOP	C4	RF 0205 (10) Reset Counter
DC	OUT 7	67	
DD	LDI	F8	RF 0206 (00) Relieve Reset
DE		#03	Reset RF for Output Control
DF	PLO	AF	
E0	BR	30	
E1	ADDRESS	A3	Branch to Take New Data with
E2	LDI	F8	*TIMER* A New Voltage.
E3		#02	
E4	PHI RI	B1	
E5	LDI	F8	(PATCH)
E6		#B3	Restores R1 (2B3)
E7	PLO R1	A1	Prior to Enabling
E8	BR	30	the Interrupt.
E9		56	
EF	NOP	C4	
F0	GLO	85	
F1	ANDI	FA	
F2		#C0	
F3	SHR	F6	
F4	SHR	F6	Shift to Get XX00 Bits to L.S.
F5	PLO	AA	Position 00XX and PLO RA
F6	LDI	F8	
F7		#03	
F8	PHI	BA	
F9	BR	30	RA = 03 (00XX 0000)
FA	ADDRESS	68	

OUTPUT DATA FROM SWEEP MODE

0100	LDI	F8	
0101		#07	
0102	PLO RF	AF	RF = 07
0103	LDI	F8	
0104		#8C	
0105	PHI R.C.1	BC	Initial RAM Address
0106	LDI	F8	RC = 8C00
0107		#00	
0108	PLO R.C.0	AC	
0109		C4	
010A		C4	
010B		C4	
010C		C4	
010D		C4	
010E	SEX RF	EF	
010F	LDI	F8	
110		#08	RE.0 = 08 = 8 Data Blocks
111	PLO RE	AE	
112	BN4	3F	ESCAPE When SCLK (EF4) = 0
113	ADDRESS	12	
114	B4	37	ESCAPE When SCLK (EF4) = 1
115	ADDRESS	14	
116	OUT 7	67	0207 = (80) Data Ready
117	BN3	3E	ESCAPE When ACK (EF3) = 0
118	ADDRESS	17	
119	LDI	F8	Load Data Via C REG.
11A		#08	and Advance C REG
11B	PLO R6	A6	Load Bit CNTR with 08
11C	LDA	4C	
11D	SEP R3	D3	Go to Output Subroutine
11E	LDI	F8	
11F		#08	Load Bit CNTR with 08
120	PLO R6	A6	
121	LDA	4C	Load Data via C and Advance
122	SEP R3	D3	Go to Output Subroutine
123	LDI	F8	
124		#08	
125	PLO R6	A6	Load Bit Cntr with 08
126	LDA	4C	Load Data via C and Advance
127	SEP R3	D3	Go to Output Subroutine
128	LDI	F8	Load Bit CNTR with 04, Outputs
129		#04	SWEEP Code and SUNSENSOR Bit.
12A	PLO	A6	
12B	LDA	4C	Load Via C and Advance
12C	SEP R3	D3	Go to Output Subroutine.
12D	DEC RE	2E	
12E	GLO E	8E	
12F	BNZ	3A	Test for 8 Sets of Data
130	ADDRESS	19	

131	LDI	F8	
132		#08	Load Bit CNTR with 08
133	PLO R6	A6	
134	GHI R6.1	96	Command Word Output
135	SEP R3	D3	Go to Output Subroutine
136	LDI	F8	
137		#08	Load Bit Counter with 08
138	PLO	A6	
139	GHI RD.1	9D	Diagnostic Word Output
13A	SEP R3	D3	Go to Output Subroutine
13B	B4	37	ESCAPE When SCLK (EF4) = 1
13C	ADDRESS	3B	
13D	OUT 7	67	0208 (00) DATA READY = 0
13E	NOP	C4	
13F		C4	
140		C4	
141		C4	
142		C4	
143	NOP	C4	
144	B1	34	Branch if CMD Notify (EF1) = 0
145	ADDRESS	47	
146	SEP R7	D7	Input CMD WRD Subroutine
147	GHI	95	
148	LBNZ	CA	Branch to Execute
149	ADDRESS	00	New or Old Command
14A	ADDRESS	39	
14B	LBR	C0	
14C	ADDRESS	00	
14D	ADDRESS	41	

OUTPUT From SWEEP

Bits	
8	1N1
8	1N2
8	1N7
4	RD.O MSBITS
.	
.	
.	

8 Times
8 R6.1 Command Word
8 RD.1 Diagnostic Word
7 Bits Check Sum
1 Bit Counter Test

DWELL MODE

160	NOP	C4	
161		C4	
162		C4	
163		C4	
164		C4	
165	NOP	C4	
166	B1	34	Branch if CMD Notify (EF1) = 0
167	ADDRESS	69	
168	SEP R7	D7	Branch to Input Subroutine
169	GLO R5	85	5.0 D
16A	ANDI	FA	DELETE TIMER/SUNSENSOR
16B		#F8	Bits
16C	SHR	F6	Shift Right two Places
16D	SHR	F6	00XX XXX0
16E	PLO	AA	REG A the Address
16F	LDI	F8	For DWELL Voltages
170		#03	RA = 03 00XX XXX0
171	PHI	BA	(EVEN NUMBERS!)
172	SEX RA	EA	
173	GLO	8D	Test SUN SENSOR
174	ANDI	FA	
175		01	
176	BNZ	3A	Do Not Output Voltage
177	ADDRESS	7A	If the SUNSENSOR is Set
178	OUT 1	61	
179	OUT 2	62	
17A	LDI	F8	
17B		#05	
17C	PHI	BB	RB = 0500 For Time
17D	LDI	F8	Count = 1 sec
17E		#00	
17F	PLO	AB	
180	LDI	F8	
181		#02	
182	PHI	BF	Index REG ADD
183	LDI	F8	RF = 0201 (10)
184		#01	
185	PLO	AF	
186	SEX RF	EF	
187	OUT 7	67	201 = (10) RESET CNTR.
188	NOP	C4	
189	OUT 7	67	202 = (40) RELIEVE RESET +
18A	LDI	F8	START SLOW CLOCK
18B		#10	1010 RE + Countdown 50 Msec
18C	PHI	BE	
18D	PLO	AE	
18E	DEC	2E	
18F	GHI	9E	Countdown 50 Msec
190	BNZ	3A	
191	ADDRESS	8E	

192	NOP	C4	
193	NOP	C4	
194	NOP	C4	
195	B4	37	
196	ADDRESS	95	ESCAPE When SCLK (EF4) = 1
197	OUT 7	67	203 = (60) Start Data Counter
198	BN4	3F	ESCAPE When SCLK (EF4) = 0
199	ADDRESS	98	
19A	B4	37	ESCAPE When SCLK (EF4) = 1
19B	ADDRESS	9A	
19C	DEC	2B	
19D	GLO	8B	
19E	BNZ	3A	One Second Countdown
19F	ADDRESS	98	For Data Acquisition
1A0	GHI	9B	
1A1	BNZ	3A	
1A2	ADDRESS	98	
1A3	OUT 7	67	204 = (00) Stop SCLK and Data
1A4	NOP	C4	Counter when Countdown is Comp.
1A5	NOP	C4	
1A6	NOP	C4	
1A7	SEX RF	EF	
1A8	NOP	C4	
1A9		C4	
1AA		C4	
1AB		C4	
1AC	NOP	C4	
1AD	INC	IF	205
1AE	INC	1F	206
1AF	NOP	C4	
1B0		C4	
1B1		C4	
1B2		C4	
1B3		C4	
1B4	NOP	C4	
1B5	OUT 7	67	207 = (80) DATA READY
1B6	BN3	3E	ESCAPE When ACK (EF3) = 0
1B7	ADDRESS	B6	
1B8	NOP	C4	
1B9	LDI	F8	
1BA		#08	Initialize Bit Counter
1BB	PLO R6.0	A6	
1BC	INP1	69	Input 1st 8 Bits of Data to D
1BD	NOP	C4	
1BE	SEP R3	D3	Call Output Subroutine
1BF	LDI	F8	
1C0		#08	Reset Bit Counter
1C1	PLO	A6	
1C2	INP 2	6A	Input 2nd 8 Bits of Data to D
1C3	NOP	C4	
1C4	SEP R3	D3	Call Output Subroutine
1C5	LDI	F8	

1C6		#08	Reset Bit Counter
1C7	PLO	A6	Output 3rd 8 Bits of The Data Word
1C8	INP 7	6F	
1C9	SEP R3	D3	Call Output Subroutine
1CA	LDI	F8	
1CB		#04	Output 4 Bits of Analyzer
1CC	PLO	A6	Volts and SUN SENSOR Status
1CD	GLO RD.0	8D	
1CE	SEP R3	D3	Callout Output Subroutine
1CF	LDI	F8	
1D0		#08	
1D1	PLO	A6	
1D2	GHI	96	Output CMD Word From R6.1
1D3	SEP R3	D3	Call Output Subroutine
1D4	LDI	F8	
1D5		#08	Load Bit Counter
1D6	PLO	A6	
1D7	GHI	9D	Output Diagnostic 8 Bits from D.1
1D8	SEP R3	D3	Call Output Subroutine
1D9	SEX RF	EF	
1DA	OUT 7	67	208 (00) Reset DATA READY
1DB	REQ	7A	Reset Q
1DC	B1	34	
1DD	ADDRESS	DF	Branch if CMD Notify (EF1)=0
1DE	SEP R7	D7	Input CMD Word
1DF	GHI	95	Load Next CMD (R5.1) into D
1EO	LBNZ	CA	If a New Command was Received
1E1	ADDRESS (MSB)	00	Branch to EXECIN.
1E2	ADDRESS (LSB)	39	New CMD ADDRESS
1E3	LBR	C0	Otherwise Branch to SAME CMD
1E4	ADDRESS (MSB)	00	
1E5	ADDRESS (LSB)	41	Same CMD ADDRESS

	Bits	Source
	8	1N1
	8	2
	8	1N7
	4	D.O SUNSENSOR & ANA VOLTS
	8	6.1 Command Word
	8	D.1 Diagnostic Bits
		XXXXXXX X
200	(00)	CHECKSUM Counter Test Results
201	(10)	RESET CNTR
202	(40)	Slow Clock
203	(60)	Start CNTR
204	(00)	SWEEP
205	(10)	Reset CNTR
206	(00)	
207	(80)	DATA READY
208	(00)	
209	(08)	
20A	(00)	

OUTPUT SUBROUTINE

EXIT	020F	SEP	D0	
ENTER	210	PLO	A4	Begin Output Subroutine
	211 CONTINUE	GLO	84	
	212	SHL	FE	Shift Left MSB to DF
	213	PLO	A4	Save in R4.0
	214	B4	37	Escape when SCLK (EF4) = 1
	215	ADDRESS	14	
	216	BDF	33	Branch to Set Q if Data Bit = 1
	217	ADDRESS	1B	
	218	REQ	7A	Reset Q
	219	BR	30	Branch to DEC REG
	21A	ADDRESS	1C	
	21B	SEQ	7B	Set Q
	21C	DEC	26	DEC Bit CNTR R6
	21D	BN4	3F	Escape When SCLK (EF4) = 0
	21E	ADDRESS	1D	
	21F	GLO	86	Load Bit CNTR R6
	220	BZ	32	Branch to Exit if R6 = 0
	221	ADDRESS	0F	Exit
	222	BR	30	Otherwise
	223	ADDRESS	11	Continue

TEST COUNTER

230	LDI	F8	
231		#02	
232	PHI	BF	
233	LDI	F8	REG F Contains 0201 The
234		#01	Address of Control
235	PLO	AF	Thru OUT 7.
236	LDI	F8	
237		#FE	
238	PHI	BE	E REG is Countdown
239	LDI	F8	Register Contains
23A		#00	FE00
23B	PLO	AE	
23C	RESET Q	7A	
23D	SEX RF	EF	
23E	OUT 7	67	LOC 201 (10) Reset CNTR
23F	NOP	C4	
240	OUT 7	67	LOC 202 (40) Relieve Reset ±ST Slow
241	OUT 7	67	LOC 203 (60) Clock Also Diverts Q
242	SET Q	7B	To the Amp Input
243	DEC RE	2E	Start CNTR
244	GHI RE	9E	
245	RESET Q	7A	
246	NOP	C4	
247	BNZ	3A	D ≠ 0 Branch

248	ADDRESS	42	
249	GLO	8E	
24A	BNZ	3A	
24B	ADDRESS	42	
24C	OUT 7	67	204 (00) Stop Count
24D	NOP	C4	
24E	NOP	C4	
24F	NOP	C4	
250	NOP	C4	
251	NOP	C4	
252	INP 1	69	8 Bits from Counter (00)
253	BNZ	3A	
254	ADDRESS	#62	
255	INP 2	6A	8 Bits from Counter (FE)
256	SDI	FD	Subtract Immed
257		#FE	
258	BNZ	3A	
259	ADDRESS	62	Input 2 ≠ FF
25A	GHI	9D	
25B	SHR	F6	Shift Right 0 MSB
25C	SHL	FE	Shift Left 0 LSB
25D	ADDI	FC	
25E		#01	Puts One in LSB of D.1
25F	PHI	BD	If Test is Successful
260	BR	30	
261	ADDRESS	66	
262	GHI	9D	
263	SHR	F6	Shift Rt 0 MSB Shifts LSB Out
264	SHL	FE	Shift Lft. 0 LSB Restores MSB & PUTS
265	PHI	BD	A Zero in LSB in Reg D.1.
266	LBR	C0	The Status Bit for the
267	ADDRESS	00	Counter A1 in LSB
268	ADDRESS	35	Indicates the Counter
269	NOP	C4	Test was Successful.
			(Odd Number)
26F		C4	(PATCH)
270	GHI 5.1	95	If a New Word Has Been
271	BZ D=0	32	Received Do a Retur to P=D
272		75	
273	BR	30	
274		8F	
275	B1	34	This is a Software Filter.
276		8F	If the CMD Notify
277	B1	34	Drops to Zero the Program
278		8F	Branches Back to Its Origin.
279	B1	34	If CMD Notify Stays High and 5.1 is Zero
27A		8F	the Program Goes to 280
27B	BR	30	the Start of the Input
27C		80	Subroutine.

INPUT SUBROUTINE

INITIAL	280	LDI	F8	(PATCH)
ENTRY	281		#08	Set Up Bit Counter
	282	PLO R6	A6	
	283	GLO	8F	
	284	PLO	AE	Save Current Value of RF.0
	285	LDI	F8	
	286		#02	
	287	PHI	BF	RF = (0209) (08)
	288	LDI	F8	
	289		#09	
	28A	SEX RF	EF	
	28B	BR	30	
	28C	ADDRESS	92	
EXIT	28D	GLO	8E	
	28E	PLO	AF	Restore F to Orig. Value
	28F	SEP	D0	
ENTER	290	BR	30	
	291	ADDRESS	70	
	292	NOP	C4	
	293	B1	34	Escape When CMD Notify=1
	294	ADDRESS	93	
	295	B4	37	Escape When SYS Clock=1
	296	ADDRESS	95	
	297	OUT 7	67	Output (08) Acknowledge
	298	BN4	3F	Escape when SCLK (EF4) = 0
	299	ADDRESS	98	
	29A	GHI	95	Load Next Byte (R5.1) to D
	29B	SHL	FE	Shift Left
	29C	B2	35	Branch if Data Bit (EF2) = 0
	29D	ADDRESS	AO	ADDRESS
	29E	ADI	FC	ADD 01 to D
	29F		#01	
	2A0	PHI	B5	Save Shifted CMD WRD
	2A1	B4	37	Escape When SCLK (EF4) = 1
	2A2	ADDRESS	A1	
	2A3	DEC R6	26	Decrement Bit CNTR
	2A4	GLO	86	Test for End of Command
	2A5	BNZ	3A	
	2A6	ADDRESS	98	
	2A7	OUT 7	67	Reset Acknowledge (00)
	2A8	BR	30	
	2A9	ADDRESS	8D	ADDRESS
	2AA	NOP	C4	
	2AF	NOP	C4	

INTERRUPT ENTRANCE

EXIT	2B0	LBR	C0	That Generates EX and DN
	2B1	ADD	8C	
	2B2	ADD	69	
ENTRY	2B3	SAVE	78	T 8C6E P=R1, X = R2
	2B4	DEC	22	R2 8C6D
	2B5	STXD	73	Save D in 8C6D, R2 (8C6C)
	2B6	GLO RF	8F	
	2B7	STXD	73	Save F.0 in 8C6C, R2=(8C6B)
	2B8	GHI RF	9F	
	2B9	STXD	73	Save F.1 in 8C6B R2=(8C6A)
	2BA	GLO RD	8D	
	2BB	OR IMMED	F9	
	2BC		#10	Set Sun Status
	2BD	PLO RD	AD	
	2BE	LDI	F8	
	2BF		#02	
	2C0	PHI RF	BF	RF = 0200 (00)
	2C1	LDI	F8	
	2C2		#00	
	2C3	PLO RF	AF	
	2C4	SEX RF	EF	
	2C5	OUT 1	61	
	2C6	DEC RF	2F	Output Zero Volts to Power Supplies
	2C7	OUT 2	62	
	2C8	LDI	F8	
	2C9		#8C	
	2CA	PHI RF	BF	RF Contains 8C6E (T)
	2CB	LDI	F8	
	2CC		#6E	
	2CD	PLO RF	AF	
	2CE	LDX	F0	T D
	2CF	SEX R2	E2	
	2D0	ANI	FA	
	2D1		#OF	
	2D2	ORI	F9	Create DN Instruction
	2D3		#DO	
	2D4	STXD	73	Store DN in 8C6A, R2=8C69
	2D5	SEX RF	EF	
	2D6	LDX	FO	T D
	2D7	SHR	F6	
	2D8	SHR	F6	
	2D9	SHR	F6	Shift MSB to LSBITE
	2DA	SHR	F6	Results 0X
	2DB	ORI	F9	
	2DC		#E0	The Instruction SEX EX is Formed.
	2DD	SEX R2	E2	
	2DE	STR	52	EX 8C69; R2 = 8C69
	2DF	INC	12	R2 - 8C6A
	2E0	INC	12	R2 - 8C6B

2E1	LDXA	72	8C6B (F.1) D, R2 8C6C
2E2	PHI RF	BF	Restores F.1
2E3	LDXA	72	8C6C (F.0) D; R2 8C6D
2E4	PLO RF	AF	Restores F.0
2E5	LDXA	72	8C6D(D) D; R2 8C6E
2E6	BR	30	
2E7	ADDRESS	B0	

LOOK-UP TABLE ROUTINE

0300	(MSB)	00	Channeltron: 0 Volts Analyzer: 0
0301	(LSB)	00	
0302	-	00	0
0303	-	00	
0304	-	00	0
0305	-	00	
0306	-	00	0
0307	-	00	
0308	-	00	0
0309	-	00	
030A	-	00	0
030B	-	00	
030C	-	00	0
030D	-	00	
030E	-	00	0
030F	-	00	
0310	-	BB	Channeltron: 2200 Volts Analyzer: 7.3
0311	-	1D	
0312	-	BA	15.6
0313	-	69	
0314	-	B8	33
0315	-	E5	
0316	-	B5	71
0317	-	AD	
0318	-	AE	151
0319	-	D9	
031A	-	A0	322
031B	-	45	
031C	-	81	685
031D	-	49	
031E	-	3F	1460
031F	-	25	
0320	-	CC	Channeltron: 2400v Analyzer: 7.3
0321	-	2E	
0322	-	CB	15.6
0323	-	7A	
0324	-	C9	33
0325	-	F6	
0326	-	C6	71
0327	-	BE	
0328	-	BF	151
0329	-	EE	
032A	-	B1	322
032B	-	56	
032C	-	92	685
032D	-	5A	
032E	-	50	1460
032F	-	3A	
0330	-	DD	Channeltron: 2600v Analyzer: 7.3

0331	-	43	
0332	-	DC	
0333	-	8B	15.6
0334	-	DB	
0335	-	0B	33
0336	-	D7	
0337	-	D3	71
0338	-	D0	
0339	-	FF	151
033A	-	C2	
033B	-	67	332
033C	-	A3	
033D	-	6B	685
033E	-	61	
033F	-	4B	1460

4. SPECTROMETER DESIGN

Electrostatic analyzers for ionospheric and space measurements operate with differential energy channels whose nominal centers increase in a geometrical sequence. Due to the physical design, the energy bandwidths, ΔE_i, are close to a constant fraction of the central energy E_i. Such a series has the advantages that a wide energy may be scanned and that analysis of data is mathematically convenient.

Under these circumstances the raw counting rate dN/dt in any channel represents the differential energy flux density, ϵ_i, as a function of energy. Then ϵ_i/E_i is the differential particle flux, Φ_i, and Φ_i/E_i is a form of the velocity distribution function f.

Design of a spectrometer involves compromises among such performance parameters as energy range, energy definition (channel width), dynamic range, temporal and spatial determination and mode versatility. The technical parameters for the present instrument are as follows:

1. The ion energy range lies between 40 eV and 20 keV.
2. The range is accomplished in eight steps.
3. The channels overlap in energy by two percent at FWHM.
4. A complete sweep is accomplished in 0.25, 1 or 10 seconds, selected externally, or may dwell at a single channel indefinitely.
5. The geometrical factor G $\approx 10^{-3}$ cm^2 sr.
6. An incident current density of 100 nA cm^{-2} is observable.

With these constraints the aim of the design is summarized as:

1. The multiplication factor for the geometric sequence is 2.13, i.e.,

$$E_i = 2.13\, E_{i-1}$$

2. The energy resolution δ in each channel is 74 percent at FWHM, thus

$$\delta = \frac{\Delta E_i}{E_i} = 0.74 \quad .$$

Table 4.1 shows the nominal central energies and bandwidths.

Table 4.1. Design Goals for the Energy Channels (keV)

Central Energy	FWHM Positions		Bandwidth
0.073	0.046	0.100	0.054
0.156	0.098	0.214	0.116
0.333	0.210	0.456	0.246
0.71	0.45	0.97	0.52
1.51	0.95	2.07	1.12
3.22	2.03	4.41	2.38
6.85	4.32	9.39	5.08
14.6	9.2	20.0	10.8

The command and telemetry requirements were:

1. External commands may make a selection of complete cycle scan times of 0.25, 1 and 10 seconds, and a dwell mode in any channel.
2. The detector bias may be switched off and on by command. This will also be accomplished automatically by a sensor that prevents illumination of the aperture by sunlight.
3. Telemetry (output) information supplies:
   a. cycle mode
   b. channel number
   c. accumulated counts by channel (sweep mode) or time period (dwell mode)
   d. sun sensor state
   e. detector bias state.
4. Telemetry is TTL compatible.
5. Analog voltages lie in the range 0 to 5.1V.

Command and telemetry are composed mainly of CMOS devices for low power and weight. High voltage power supplies for the analyzer plates and detector, and the amplifier/discriminator systems have been obtained commercially.

Electrostatic analysis is a common method of energy selection used in space experiments. The analysis parameters, energy range, channel width and geometric factor are related functions of the physical dimensions of the assembly. Depending on the experimental requirements, analyzer plates may be of spheroidal, toroidal or cylindrical cross section. The first two types are able to focus an isotropic, polyenergetic beam about two axes. Hence their inherent focusing abilities are greater than that of a cylinder, and suit narrow energy band and large geometric factor applications. In the present design a wide energy resolution is required, together with a relatively small geometric factor to accommodate high incident current and cylindrical section analyzer plates.

The geometric dimensions of a cylindrical analyzer upon which the measurement parameters depend are shown in Figure 4-1. The dependence of G and δ on the dimensions b, d and r, and angles α, ϕ and θ have been discussed by several authors (e.g., Refs 4-7). Consideration of the properties of such an instrument is largely empirical, due to the number of variables present, the energy dependence of the responses and the necessity of treating incident flux as distributed in energy and direction.

The present design has sought to simplify the procedure and to introduce some flexibility into the response characteristics. The entrance aperture, defined by angles and ϕ, is symmetric about the center of the entrance to the analyzer plates. The radius r defines the path of the main beam, corresponding to a particle at a central energy E_i incident normally at the center of the entrance aperture. The detector entrance lies on the normal to the center of, and distant b from, the exit plane of the plates.

The main beam is defined by

$$\frac{E_i}{q} = \left(\frac{r}{2d}\right)V_i$$

where

q = particle charge (electronic units)

d = internal plate separation

V_i = plate potential at step i (i = 0 to 7).

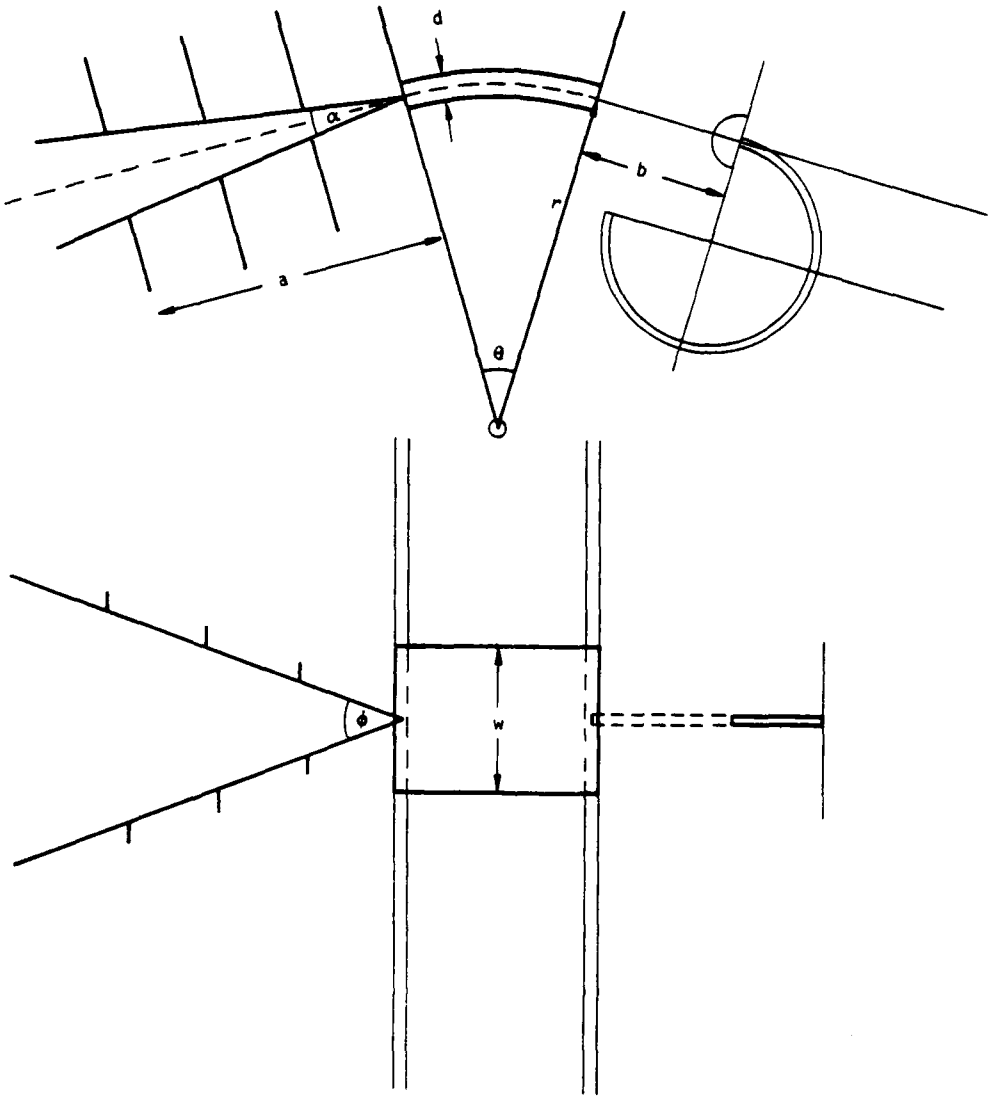


Figure 4.1. Spectrometer parameters

The channel width, δ, at FWHM is approximately constant throughout the energy range. The geometric factor G and δ are strong functions of b, r/d and θ, and are weakly dependent on α and ϕ. Adherence to the centering of entrance and detection areas eliminates some unnecessary variables.

The pursuit of small G (in anticipation of occasional very high fluxes) and large δ engenders a design conflict. This has been resolved by employment of a small detection area and a short analysis path, which results in the low-energy resolution necessary. The dimensions of the spectrometer indicated in Figure 4-1, and others defining the response, are given in Table 4.2.

Table 4.2. Dimensions of Analysis and Detection Assemblies

Notation	Function	Dimension	Comments
a	Entrance aperture length	6 cm	
α	Entrance azimuthal angular aperture	16^{o} max.	Variable by baffle selection. Axis parallel to that of cylindrical plates.
ϕ	Entrance zenithal angular aperture	20^{o} max.	Variable by baffle selection. Axis perpendicular to that of
r	Main path radius	7 cm	
θ	Main path, plate, angular dimension	32^{o}	
d	Plate internal separation	0.35 cm	
S_o	Main path length	3.91 cm	
S_1,S_2	Plate lengths	3.81,4.01 cm	
w	Plate width	2 cm	
b	Exit plane-detector separation	4 cm max.	Variable
	Detector cross-section diameter, active area	0.3 cm, 0.071 cm^2	3 mm diameter Channeltron
G	Geometric factor	1.6×10^{-3} cm^2 sr max.	Nominal
	Channeltron cross-section external diameter	0.206 cm	
	Channeltron mean diameter	4.37 cm	
	Multiplication factor	10	$E_i/V_i = r/2d$
	Background shield aperture	0.4 cm	
	Plate serration depth and angles	0.25 mm, 18^{o}	

Confirmation of acccuracy of design parameters may be obtained experimentally. In order to allow tuning of these values it was decided to make the dimensions α, ϕ and b variable. α and ϕ are defined by machined baffles as interchangeable sets. The

position of the mouth of the channeltron can be adjusted between 1 and 4 cm from the exit plane of the analyzer.

The analyzer is operated with the outer plate at ground potential and the inner plate at negative voltage. This arrangement has the advantages of a reduction in complexity of step generation and reduces the fringing fields at the analyzer exit. The multiplication factor of 10 requires a voltage at step 7 of 1.46 kV. The grounded outer plate enables the side panels of the analyzer to be formed as grounded conductors and to avoid possible charging within the analyzer.

4.1 ENERGY CALIBRATION

Calibration of the instrument was made by spatial and angular integration of its response to monoenergetic He^+ beams across the total bandwidth at the central energies of channels 1 through 7.

Ions were generated by leaking helium into a small chamber containing a hot cathode, the energy of the beam being determined by the expulsion voltage from the chamber. Species other than He^+ were removed by magnetic deflection. The resulting flux has a cross-sectional area of about 1 x 5 cm such that the long dimension is in the horizontal plane perpendicular to the analyzing axis of the spectrometer. The current density of the beam was measured with a Faraday cup connected to a Keithley 642 electrometer. Final ion emission of energies below 100 eV became very inefficient and precluded the calibration of channel 0.

The detection rate response of the instrument was measured across the energy sub-band at increments of one degree about the analyzing (vertical) axis. The total response characteristic of a channel may be obtained by summation of each energy step.

The usual measure of spectrometer properties, and one computed in this work, is that of its detection response in an isotropic isoenergetic particle flux. This may be done with a monoenergetic parallel beam by varying the angle of incidence in small increments about a vertical axis through the midpoint of the entry plane of the plates (angle α in Figure 4.1) at a fixed analyzing potential. Only variation about the vertical axis is necessary as the dispersion in energy of the incident flux takes place in this sense. At each increment the counting rate response is determined as a function of energy in a constant intensity beam. Thus, at any energy step E_i the response F is given by

$$F(E_i,E) = \int_{-\alpha/2}^{+\alpha/2} \int_{o}^{\infty} \epsilon_i(E)\, dE\, d\alpha$$

There are second-order effects in the response measurement due to counting rate dependence on discrimination level and detector efficiency as a function of energy and counting rate, detector bias, age, impact position in the cone and ion species. Thus, these parameters must be specified for the determination and there will be small variations in response properties as these are changed.

The spectrometer models were mounted horizontally with the aperture in the approximately 1 cm by 5 cm uniform beam. A Faraday cup was mounted beside the aperture and connected to an electrometer to measure current density of the flux. It was determined that beam current was dependent on filament power ($I_f V_f$) and ion chamber differential pressure above ambient (Δ p) approximately as

$$j \approx R(I_f V_f - P_o)^2\ \Delta p\ pa/cm^2$$

where R is a constant and P_o is a threshold power for a given filament. Required currents could be approximated by the source parameters. Aperture and geometric factor values of the spectrometer were estimated from Faraday cup current measurements.

A series of four degree incremental angular responses are shown as an example for Step 2 in Figures 4-2 and 4-3. The series are alternated to provide some clarity. It is apparent that the angular response is dominated by fluxes incident at negative angles (clockwise in α from the central trajectory). This effect, a deviation from the idealized selection condition, is due to the shortness of the analyzing plates compared to the optimal focusing angle (cf. Refs 4-7), and is difficult to predict from design algorithms. The skewed response for this channel is also seen in Figure 4-4, an integration across the energy domain. Total isotropic responses for channel 2 are shown in Figure 4-5. Also shown are the contiguous skirts of channels 1 and 3. Figure 4-6 shows the isotropic responses of channels 1 through 7. Ion production became increasingly inefficient below 200 eV and it was not possible to calibrate channel 0 satisfactorily. It can be seen that the skewing effect becomes less noticeable in the higher energy

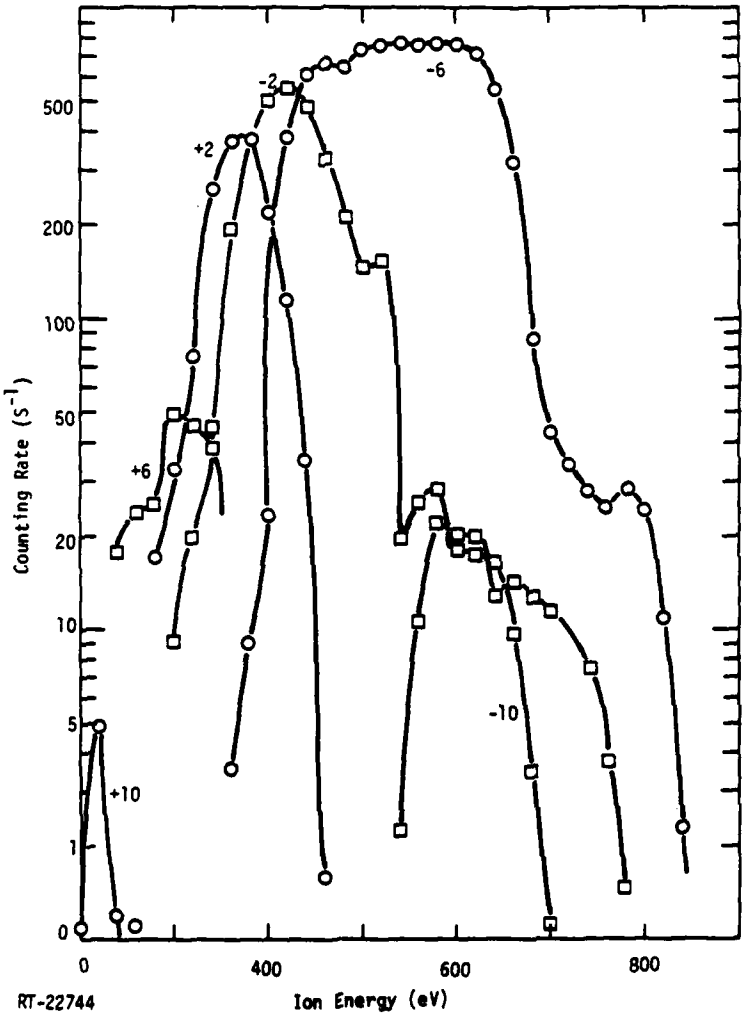


Figure 4.2 Channel 2 responses at discrete angles at constant current

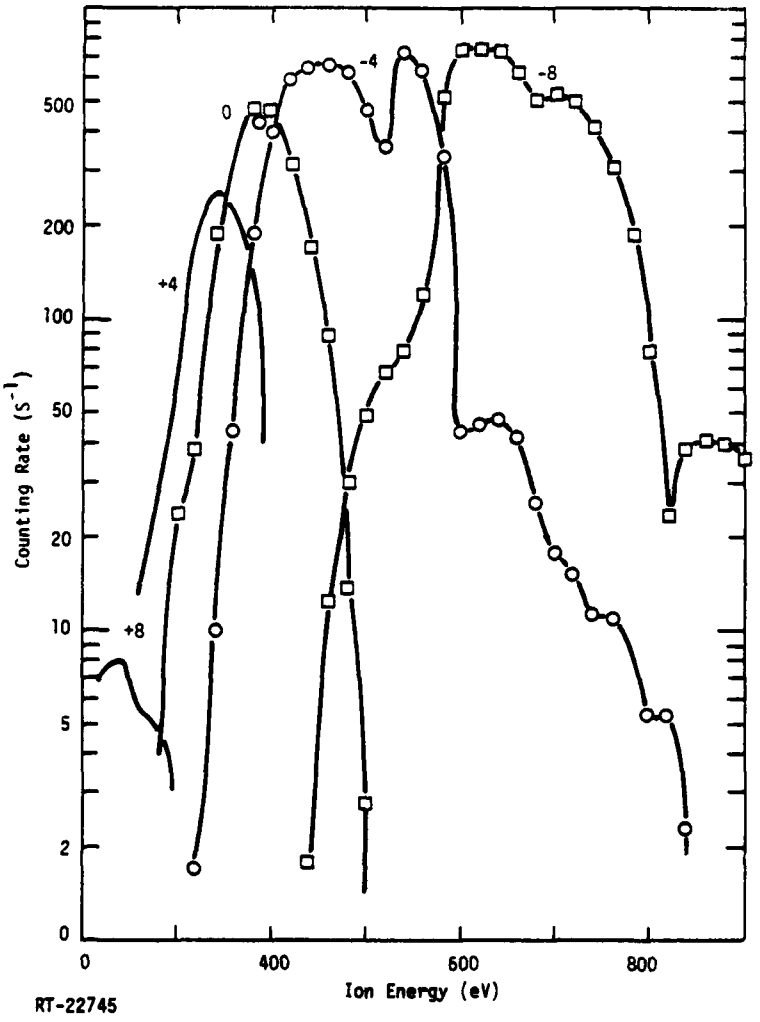


Figure 4.3. Channel 2 responses at discrete angles at constant current

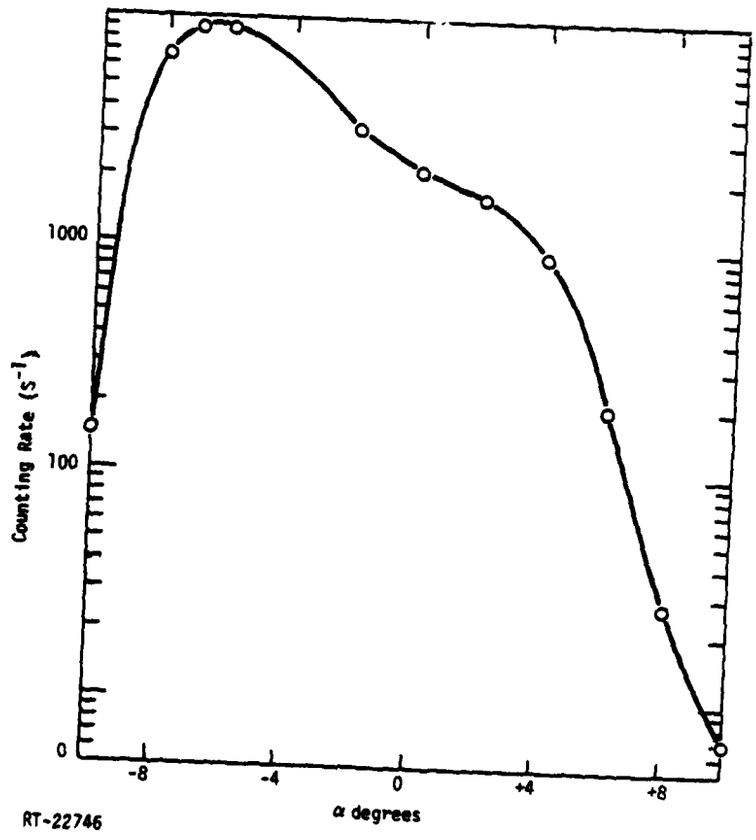


Figure 4.4. Integrated response of Channel 2 over energy

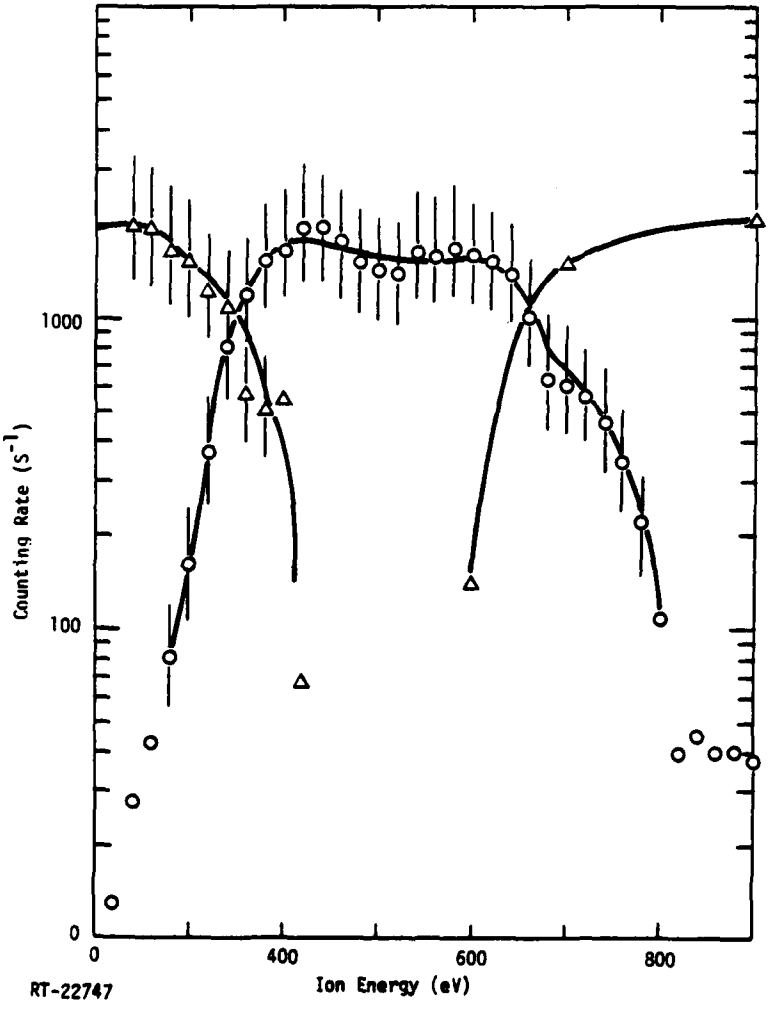


Figure 4.5. Response of Channel 2 integrated over angle

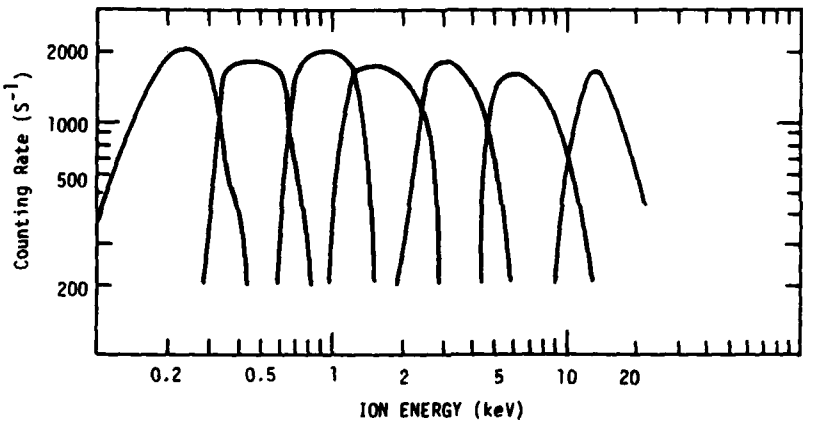


Figure 4.6. Responses of Channels 1 through 7 to isotropic isoenergetic fluxes at constant current

channels. This indicates that the field topography in the region of the plates and detector entrance also influences the microstructure of a passband.

Comparison with the calibration curves of Reference 8, which are measurements made on the prototype model with a 1 mm 4011C detector, shows that substitution of the 3 mm channeltron has tended to flatten the peak of the responses in the lower energy bins by adding some high-energy sensitivity. This has increased the bandwidths slightly so that they are close to the design goals, but has skewed some channel centers to higher values. The broadening of parallel beam response at certain angles (Figures 4-2 and 4-3) may well have a beneficial effect in the broader context of intended use. Although design parameters have been executed, as is usual, for isotropic fluxes, these seldom occur naturally. It is probable that, under conditions where a spacecraft is at a negative potential, the ambient ions are consequently accelerated into a flux which, at the spectrometer entrance, is relatively narrow, both in energy and angle content. This suggests conditions such that there are finite probabilities of such beams going undetected. The broad "parallel" sensitivities of Figures 4-2 and 4-3 serve to decrease the chance of a miss.

The nominal central values of the energy channels were set to levels specified in Reference 1 by the method of Section 3.1.2 and given in Table 4.3. The voltage levels between the inner plate and ground wave measured using a Tektronix 6103A probe feeding a Keithley 610B electrometer whose output was read on a Hewlett-Packard 3455A digital multimeter. Calibration was made with a Cohu 326 voltage standard. Maximum total errors in these measurements are estimated at $\pm$0.3V.

Table 4.3. Analyzer Voltages of the Prototype, Flight 1 and Flight 2 Spectrometer Models

Step No.	Nominal Voltage	Prototype Detector Voltage			Flight 1 Detector Voltage			Flight 2 Detector Voltage		
		2200	2400	2600	2200	2400	2600	2200	2400	2600
0	7.3	7.35	7.15	7.25	7.25	7.15	7.20	7.25	7.25	7.15
1	15.6	15.3	16.66	13.45	14.95	15.4	15.2	15.4	15.9	15.98
2	33.3	33.0	34.7	32.3	32.8	32.6	32.7	33.0	32.8	33.0
3	71	66.8	71.4	72.6	70.6	72.2	68	71.4	71.3	72.2
4	151	149.4	153.4	153.4	151.1	152.5	149.8	152.2	151.9	153.1
5	322	327.2	319.8	319.2	324.7	325.7	332.1	325.7	326.4	327.3
6	685	689.7	682.8	680.0	693.1	692	686.6	694.1	695.4	696.2
7	1460	1461.4	1454.7	1445.4	1485.1	1476.6	1466.8	1484.9	1484.9	1485.8

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5. DISCUSSION

This spectrometer has been designed to serve the needs of an automatic spacecraft charging-detection and discharging system. Its original concept consisted of a hard-wired instrument whose performance parameters adhered to the proposed specifications. Two reasons impelled a change to a microprocessor-based programmable system. First, the relative complexity of functions required of a simple and inexpensive instrument required an electronic design complicated and unwieldy beyond the sense of the project. Second, such a change injected the design with a high degree of flexibility in application and performance, and suggested straightforward interface capability with other programmable subsystems.

The idea of a particle spectrometer sensitive to an energy range with a ratio of 435 in eight steps is unusual. It is based on feasibility studies modeled on data from the SC9 instrument (Ref 9) flown on the P78-2 stationary satellite. These indicated that continuous comparison of counting rates in narrow energy bins showed promise as a real-time monitor of spacecraft potential conditions. It was felt that similar success could be achieved with relatively few wide channels.

The considerations involved in design of a broadband spectrometer, short analyzer plates and wide acceptance angles led to such unwelcome secondary effects as channel microstructure, response variability over the energy range, danger of rapid channeltron aging under high current conditions and the chance of nondetection of anisotropic fluxes. These features have been taken into account in the present instrument and attempts made to optimize performance with respect to all such considerations. As the concept of automatic quantification of spacecraft charging and relief is in its development stage, it was felt that the greater the flexibility provided in the detection system, the more useful it would prove to the investigators.

For example, it may be required that the number of discrete channels be increased, the energy range lowered and the bandwidths reduced. This may be achieved easily by replacement of the detector, narrowing of the acceptance angle with a

smaller set of collimators, increasing the plate-detector separation and reprogramming of the memory system.

The dynamic range of the instrument is extremely large. Twenty-four bits of counting rate data are available for any data interval, i.e., energy step period or 10 seconds in the dwell mode. This is a recording of over 16 million separate events. At very high rates the apparent counting rate A must be corrected for the dead time (T = 220 ns) effect of the amplifier. The real counting rate, N, is given by

$$N = \frac{A}{1-AT} \text{ sec}^{-1}$$

Table 5.1 indicates the corrections necessary at various counting rates. Adjustment of the dead time to higher values allows reduction of the number of data bits, at the risk of lower precision occurring at high rates.

Table 5.1. Real (N) and Apparent (A) Counting Rates for a Dead Time (T) of 220 ns

A	N
2 MHz	3.571 MHz
1	1.282
500 kHz	562.8 kHz
100	102.25
50	50.56
10	10.02

The modes of data collection are scans of the eight steps in nominal periods of 0.25, 1 and 10 seconds, and indefinite dwells at any energy level with data output at 10 second intervals. Thus the accuracy in the worst case (A≒1.68 MHz, N = 2.66 MHz) is thought to be adequate for the application. The efficiency of the channeltron varies with proton energy E and N (Ref 1)

The nominal aperture of the instrument may be estimated from the dimensions of the outer collimator plate (a x b, Figure 2-8), the distance to the detector surface r and the active area of the channeltrons as

$$G \doteq \frac{s\,a\,b}{r^2} = 1.6 \times 10^{-3} \text{ cm}^2 \text{ st} \quad .$$

This will allow counting of a 100 nA/cm^2 beam at a particular energy in the fastest scan mode. It is advised that such high fluxes not be used frequently in testing so that detector aging be avoided.

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1. R. Judge, "Proton Electrostatic Analyzer - R&D Design Evaluation Report," IRT 8203-002 (May 1981).

2. S. E. DeForest, "Spacecraft Charging at Snychronous Orbit," J. Geophys. Res., 77 651 (1972).

3. R. Judge, "Proton Electrostatic Analyzer - Second Quarterly R&D Status Report," IRT 8203-003 (June 1981).

4. A. Septier (Ed.), "Focusing of Charged Particles," Two Volumes, Academic Press, New York (1967).

5. Y. Delage and J-D Carette, "Spectrometres Electrostatique, Partie I," Can. J. Phys. 49, 2118 et seq. (1971).

6. P. Decreau, R. Prange and J. J. Berthelien, "Optimization of Toroidal Electrostatic Analyzers for Measurements of Low Energy Particles in Space, Rev. Sci. Instrum. 46, 995 (1975).

7. J. F. Crijo, R. Prange, C. Cornic and P. Salvetat, "Rocket-Borne Double Focusing Analyzer for Particle Spectroscopy in the Lower Magnetosphere," Rev. Sci. Instru. 47, 6 (1976).

8. R. Judge, "Proton Electrostatic Analyzer - Third Quarterly R&D Status Report," IRT 8203-004 (September 1981).

9. S. L. Spiegel, "Design of a Computer Algorithm to Measure Satellite Surface Charging," communication from AFGL (10 December 1980).

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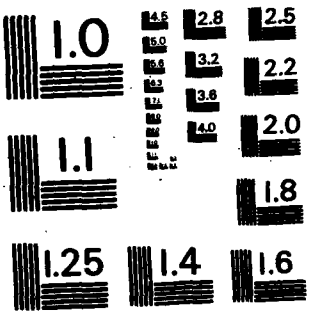
AD A133 588 PROTON ELECTROSTATIC ANALYZER(U) IRT CORP SAN DIEGO CA 2/2
R JUDGE FEB 83 IRT-8203-005 AFGL-TR-83-0081
F19628-80-C-0205

UNCLASSIFIED F/G 14/2 NL



APPENDIX A

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A meeting between representatives of AFGL and IRT agreed to the following contract understandings:

A. CONTRACT SPECIFICATION INTERPRETATIONS

(Unambiguous interpretations omitted, numbering by original specification number.)

1, 5, 6, 7, 10 and 15 agreed to.

2. The instrument will survive a current density of 100 nA/cm^2 at the aperture.

3. AFGL to advise on the technical necessity of FWHM channel overlap of between 0 and 2 percent. Relief from the specification was sought due to the energy response nature of such an instrument and the difficulty of obtaining a narrow overlap range.

4. Indicated sweep times may be approximated to periods convenient to instrument.

8. Flight exposure is two years, shelf life is three years. Use of the detector under variable (minimum) bias indicates a two-year lifetime and does not require the employment of multiple detectors. Compliance will be demonstrated by analysis. Orbital environments are assumed benign.

9. AFGL will conduct environmental tests at the specified levels. The prototype instrument is designed for functional tests only and is not intended for acceptance test survival.

11. The analyzer plates of each model are serrated to reduce photon scattering. Collimator and plate surfaces of the flight models would be gold blackened as schedule and expense allowed.

12. Diagnostic output selection was made by IRT with best engineering judgment. The preliminary diagnostics met the intent of the specification.

13. Protection against potentially damaging transients entering or leaving the instrument was achieved by addition of zener diodes to the interface lines.

14. Maximum power consumption of two watts is acceptable for rocket applications.

16. Replacement of a detector in an ESA may require recalibration of the instrument.

B. OTHER UNDERSTANDINGS

1. Flight Environment

   a. The flight models are intended for a rocket mission to an altitude 300 km under quiet conditions.

   b. Thus radiation-hard components and detector shielding are not required in the flight models.

   c. IRT to be advised on any change in this environment and will respond with cost, weight, power and schedule impact estimates.

   d. IRT will provide for fast outgassing behavior of the instrument consonant with maintenance of adequate protection for components. They will also advise on minimum power-on altitude.

   e. AFGL will provide information on vehicle, instrument location, launch site, local time window, solar and lunar aspects, required ionospheric conditions and any other data pertinent to successful operation.

   f. Instrument apertures will be protected by plates or caps to be removed shortly prior to launch and so identified.

2. Shelf Environment

   a. When stored for longer periods than three days, the instruments will reside in dry, clean argon or nitrogen atmospheres at slight positive pressures. The atmosphere will be refreshed each month. The container need only be a plastic box or thick bag.

3. Mechanical Interface

   a. Securement to a vehicle platform may be by baseplate bolts, brackets or straps.

   b. Current dimensions are acceptable for vehicle integration.

4. Telemetry Interface

   It is not the intent that the current instrument interface directly with S/C telemetry.

a. The command word will be transmitted to the ESA with MSB (0) first and designate:

0, 1	channeltron bias
2, 3, 4	analyzer voltage for dwell mode
5, 6	sweep time or dwell
7	true, overrides sun sensor.

b. Data transmission from the ESA has MSBs first in the following format:

Dwell Mode

0-35	as defined in Second Quarterly Report (Q2)
36-43	diagnostic data

Sweep Mode

0-223	bits 0-27 as defined in Q2 and transmitted eight times (once) for each analyzer step)
224-231	command word
232-239	diagnostic data.

c. The telemetry system will be based on an S/C clock, faster than the current 1024 s^{-1}. Upon coding completion, the fastest convenient clock time, determined by the number of P instructions executed for output of each data bit, will be determined and documented.

Hardware and software impacts for a faster rate will be evaluated.

d. In order to speed up data transfer during the dwell mode, no input command will be accepted during transmission of dwell data. In the sweep mode, the next input command will be accepted only after completion of the sweep.

5. Miscellaneous Items

a. From the results of instrument calibration, an attempt will be made to calculate a factor for each channel which will enable an absolute counting rate to be obtained.

b. After all data is gathered on the components, IRT will perform a reliability calculation for the complete system.

c. A power-off, power-on reset practice is acceptable and would be used for recovery in a satellite flight after any soft error problems were detected.

d. Soft error occurrence is very unlikely in a rocket flight.

e. Selection of an RCA 1802 P-based electronic system is acceptable.

f. Ground test equipment development is the responsibility of AFGL. IRT will provide informal information based on their own test setups.

g. Final checks of detector operation may be made by use of a suitable radioactive source placed at constant position with respect to the instrument.

h. The final report shall include test results, appropriate drawings, design assumptions, S/W descriptions and requirements for instrument use and treatment.

i. On receipt of requirements for algorithm manipulation capability incorporation into the IRT instrument, IRT will provide feasibility and cost and schedule impact estimations.

6. Action Items

a. IRT provided a preliminary interface control document. This included maximum dimensions, mounting footprint, functional interface, pin assignments, weight and power estimates and required aperture angles.

b. AFGL will provide required pyro shock data.

c. AFGL will investigate relief on Item A3.

APPENDIX B

IRT PROTON ESA INTERFACE PIN ASSIGNMENTS

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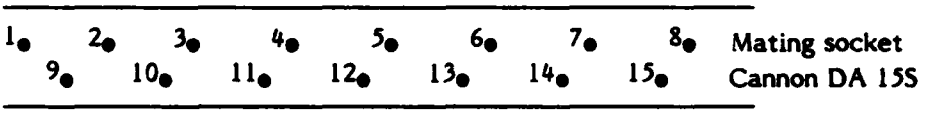
IRT PROTON ESA
INTERFCE PIN ASSIGNMENTS



Cannon DA 15P connector pins as
viewed from exterior of ESA

Functional Interface

Type	Designation	Formal Name	Cannon DA ISP Pin Assignment	V40 Pin Assignment
Power	+28 Vdc	+28	7	1
Power	+28 Vdc RTN	+28 RTN	8	10
Power	ESA signal ground	SIG GND	13	2
Input	Spacecraft clock	SCLK IN	9	4
Input	Command Notify	CMD NOTIFY	1	7
Input	Command Data	CMD DATA	2	16
Input	Data Out Acknowledge	DATA OUT ACK	10	6
Output	Data Ready	DATA READY	3	5
Output	Command In Acknowledge	CMD IN ACK	11	15
Output	ESA Data Output	DATA	4	3
Term	+5 Vdc		6	11

Pins 5, 12, 14 and 15 not used.

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APPENDIX C

CHARGE SENSITIVE AMPLIFIER

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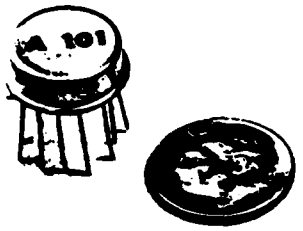
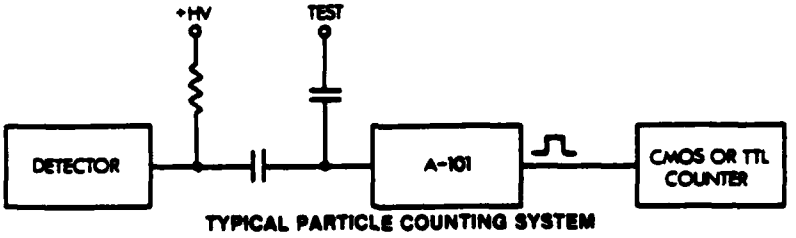
A-101 PAD
HYBRID CHARGE SENSITIVE PREAMPLIFIER · DISCRIMINATOR



Designed for direct applications in the field of aerospace instrumentation, mass spectrometers, laboratory and research experiments, medical electronics, and electro-optical systems.

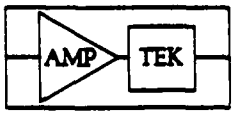
Model A-101 is a hybrid charge sensitive preamplifier, discriminator, and pulse shaper developed especially for instrumentation employing photomultiplier tubes, channel electron multipliers and other charge producing detectors in the pulse counting mode. While this unit was specifically designed for satellite instrumentation, the following unique characteristics make it equally useful for space, laboratory and commercial applications:

- **Small size (TO-8 package) allows mounting close to collector of multiplier.**
- **Power required is typically 15 milliwatts.**
- **Single power supply voltage.**
- **Outputs interface directly with C-MOS and TTL logic.**
- **Input threshold is externally adjustable.**
- **Output pulse width is variable with external trim capacitor.**
- **168 hours of burn-in time.**
- **One year warranty.**



TYPICAL PARTICLE COUNTING SYSTEM

The hybrid assembly of the A-101 is performed in a Class 100 filtered air clean room facility using thin film technology and unpackaged chip components. The substrates are ceramic with gold deposited conductors. The cases are filled with dry, inert gas, hermetically sealed and leak tested. The units then undergo burn-in for 168 hours under full load at 125°C in order to minimize infant mortality.



AMPTEK INC

6 DE ANGELO DRIVE, BEDFORD, MASS. 01730 / (617) 275-2242

SPECIFICATIONS

(V_s = 5V, T = 25°C)

INPUT CHARACTERISTICS

THRESHOLD: Model A-101 has a nominal threshold referred to the input of 1.6×10^{-13} coulomb. This is equivalent to 10^6 electrons. The threshold can be increased by the addition of a resistor between Pins 9 and 12. See Figure 1.

STABILITY: <1.5% of threshold. 0° to 50°C. See Figure 3.

NOISE: RMS noise level <0.4% of threshold.

PROTECTION: Back-to-back diodes to ground.

OUTPUT CHARACTERISTICS

1) Pin 5 provides a positive 5 volt output pulse capable of interfacing directly with CMOS.

Pulse characteristics are:

RISETIME: 6 ns

FALLTIME: 20 ns

WIDTH: 220 ns nominal. May be increased to greater than 2 µs by the addition of a capacitor between Pins 3 and 4. See Fig. 2.

AMPLITUDE: 5 volts

2) Pin 6 is an open collector output and with an external pullup resistor provides a negative going pulse (the complement of Pin 5). This output can drive TTL and can be wire-or'ed with other units. Pullup resistor may be connected to V_s or to other positive supply up to +15V.

GENERAL

COUNT RATE: 4×10^6 CPS

PULSE PAIR RESOLUTION: 250 ns

OPERATING VOLTAGE: +4 to +10 VDC

OPERATING CURRENT: 3ma Quiescent
4ma @ 10^6 CPS

TEMPERATURE: −55° to +70°C operational

BURN-IN: 168 hours at full load and 125°C.

RADIATION RESISTANCE DATA: on request

PACKAGE: 12-Pin, TO-8 case.

OPTIONS: Qualification to MIL-STD-883/B

OPERATING NOTES:

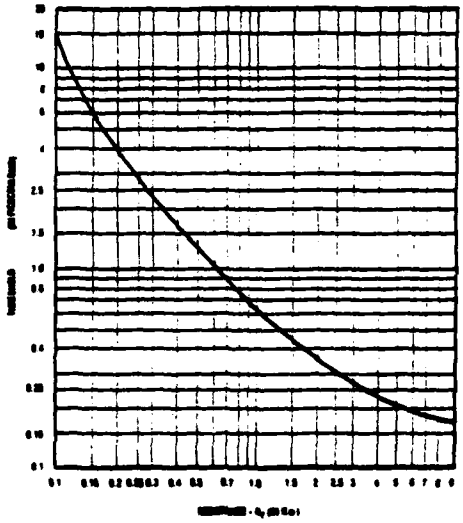
POWER REQUIREMENTS:

All device specifications apply to operation at +5V. The unit can be operated up to +10V with increased power dissipation and threshold. Supply is internally bypassed. Care should be taken in circuit layout and in some applications power supply decoupling may be helpful.

The case is internally connected to Pin 1, ground.

INPUT

The detector is normally capacitively coupled to Pin 12 with a capacitor of adequate voltage rating. Alternately, the detector anode can be direct coupled to the input if the cathode is at negative potential. The A-101 is sensitive to a negative charge pulse of at least 0.16 picocoulomb. This threshold may be increased by the connection of a resistor between Pins 9 and 12. Approximate values are given in Figure 1.

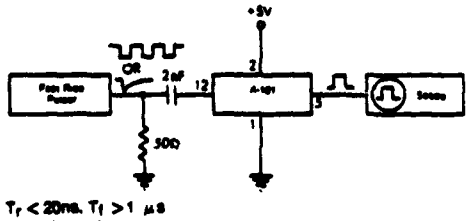


Input threshold as a function of external resistance
Figure 1

The A-101 can be tested with a pulser by using a small capacitor to inject a test charge into the input. The unit will trigger on the negative-going edge of the pulse which should have a transition time of less than 20 ns. Either a tail pulse with a much longer fall time (>1 µsec) or a square wave may be used. (If a square wave is used, triggering on the positive-going edge will occur for large pulses).

Charge transfer in the test circuit is according to Q = CV where Q = Total amount of charge, C = Capacitor, and V = Voltage. Use only a small capacitor in this circuit (1-10pf). DO NOT connect a low impedance pulser through 500 pf when testing as this will produce a large pulse through the input transistor and may cause irreversible damage.

TEST CIRCUIT



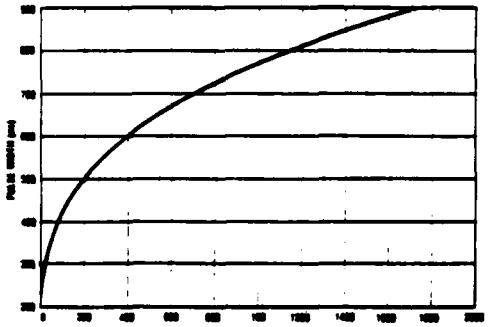
T_r < 20ns, T_f >1 µs
Negative going
Amplitude: 0.25 V = 0.5 picocoulomb

OUTPUTS

The output at Pin 5 is a positive, 220ns wide pulse.

Pin 6 is an open collector output and should be left unconnected if not used. A negative going output can be obtained by connecting a pullup resistor (Typically 1k Ω) between V_S and Pin 6. The pullup resistor may be tied to any positive voltage up to 15V (as required for example, in interfacing with particular logic families). In multi-detector systems, where more than one preamp drive the same counter, the open collector outputs of several A-101s can be connected together to the counter input with a single pullup resistor. DO NOT CONNECT THIS PIN DIRECTLY TO V_S (PIN 2) AS THIS MAY DAMAGE OUTPUT STAGE AND VOID WARRANTY.

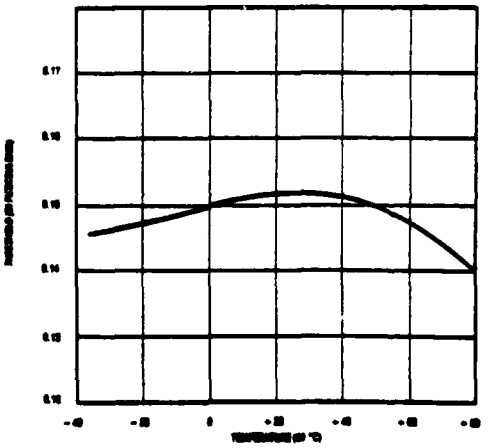
The output pulse width can be increased by the connection of a capacitor between Pins 3 and 4. See Figure 2 for typical values.



Pulse width as a function of external capacitance

Figure 2

If the standard pulse width is adequate Pins 3 and 4 must be left unconnected.



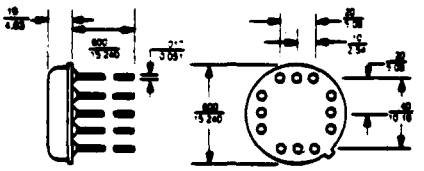
Threshold vs Temperature (Typical)

Figure 3

GENERAL

Due to its hermetic seal and small size, the A-101 is well suited to use within a vacuum chamber. In such applications the mounting should provide adequate heat dissipation and care should be taken to avoid electrical discharge near the input which can damage unit and void warranty.

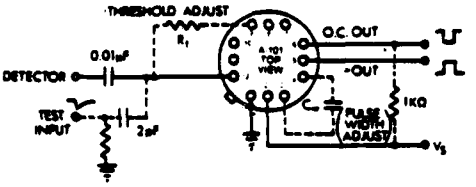
Use care in soldering leads - avoid overheating



TO-8 TYPICAL DIMENSIONS: inches / mm

PIN ASSIGNMENTS

1. GROUND
2. V_S (+ 4 to + 10 VDC)
3. Pulse Width Adjust
4. Pulse Width Adjust
5. Positive Output
6. Open Collector Output
7. No Connection
8. No Connection
9. Threshold Adjust
10. No Connection
11. No Connection
12. Input



Connection Diagram

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APPENDIX D

HIGH VOLTAGE POWER SUPPLIES

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Venus

MODEL Q15 & Q30 BATTERY OPERATED PHOTO-MULTIPLIER POWER SUPPLIES

Variable DC to DC Converter Output
Proportional to Input
Q-15 Output to 1500VDC
Q-30 Output to 3000VDC

Q30

FEATURES:

- High efficiency. Requires only 10 ma input current at no load
- High Input/Output Isolation
- All Silicon Components
- Input/Output Floating
- Short Circuit Protected
- Small, Lightweight
- Shielded, Encapsulated
- Separate Case Ground
- Off The Shelf Delivery

DESCRIPTION:

The "Q" series are versatile miniature DC to DC converters designed to operate from battery or other low power sources. This highly efficient all silicon unit is ideal for powering portable field and remote equipment requiring high voltage proportional to DC input over a wide range of load conditions.

Both input and output leads of the "Q" are floated enabling any desired combination of source and output polarities. The case is isolated from both input and output and a separate case-ground lead is provided.

A series diode protects the circuit against reversed input polarities and both input and output are protected against short circuits.

The "Q" circuit is all silicon and the unit is fully encapsulated and shielded in a nickel-plated steel can. The silicon-rubber insulated leads are 10 inches long and are color-coded for easy installation and wiring. Designed to withstand extremes of shock, vibration, acceleration, and thermal shock in accordance with the requirements of MIL-STD-810, each "Q" is fully tested before shipment and is guaranteed against defects in material or workmanship. Calculated MTBF is 75,000 hours at 71°C. for airborne applications using the method of MIL HDBK 217A.

APPLICATIONS:

• Photomultipliers • Flying Spot Scanners • Image Dissectors • Ionization Chambers
• Beam Converters • Medical Electronics • Cathode Ray Tubes • Sensitization Tubes • Geiger Tubes

Q-15 & Q-30

ELECTRICAL CHARACTERISTICS:

	Q-15	Q-30
Input Voltage	2 to 12VDC	2 to 12VDC
Input Current	Refer to graph	Refer to graph below
Output Voltage	250 to 1500 Prop. to Input	500 to 3000VDC ±5%Prop. to Input±5%
Output Current	400ua	200ua
Ripple @ F.L.	0.40%	0.25%
Insulation Strength	3500V Input to Output/Output to Case	3500V Input to Output/ Output to Case

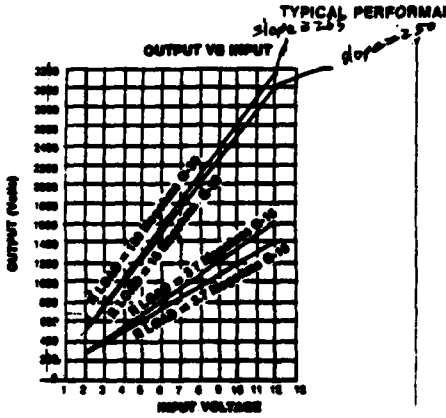
PHYSICAL CHARACTERISTICS:

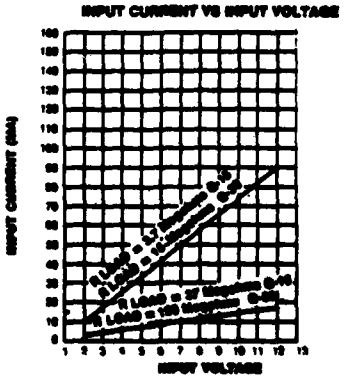
Dimensions	1" Diameter × 2½" Long
Volume	2 cu. in.
Weight	3.5 oz.
Packaging	Solid encapsulation, steel can
Finish	Bright nickel-plate
Terminations	5 silicone rubber leads 10" long

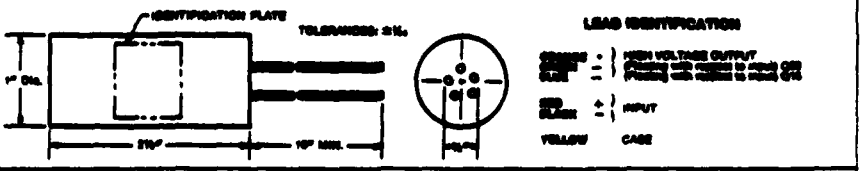
ENVIRONMENTAL CHARACTERISTICS:

Temperature Range	−55°C to +71°C
Temperature Coefficient	< +0.025%/°C
Shock	40 g's per Mil-Std-810 Method 516, Procedure IV
High Altitude	Specify Q15Z +Q30Z for 100,000 feet.
Vibration	20 g's per Mil-Std-810, Method 514, Curve E, Figure 514-3
Thermal Shock	−55°C to +71°C per Mil-Std-810, Method 504, Class 2

TYPICAL PERFORMANCE @ 25°C







Venus Scientific Inc. 255 SMITH STREET, FARMINGDALE, NEW YORK 11735

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APPENDIX E

ANALYZER/SPACECRAFT INTERFACE LINE DEFINITION

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The seven ESA interface lines are TTL compatible. They are described as follows:

1. S/C Clock

   1024 Hz, approximately 50% duty cycle. The exact frequency is not important. It is used by the S/C and the instrument to transfer digital signals; that is, commands to ESA and data to S/C.

2. Command Ready (Notify) - S/C to ESA

   This signal goes true on a positive-going edge of the S/C Clock and signals the ESA that a command word is ready from the S/C. Signal goes false on the eighth positive-going clock edge following the start of the true signal or the Command Ready Acknowledge line.

3. Command Ready Acknowledge - ESA to S/C

   The signal goes true on the positive-going edge of the S/C Clock, after the ESA has completed a readout from the last mode cycle. This signals the S/C to start shifting the command word to the ESA at the S/C Clock rate.

4. Command Word

   This is a serial digital data line dedicated to the one-way communication of command data from the S/C to the ESA. The Command Word is loaded into the S/C serial output register before the Command Ready line is set true and thus the MSB of the Command Word is available on this line when it is set true. The ESA reads the MSB on the first negative-going edge of the Clock after the Command Ready Acknowledge line goes true. The second MSB is shifted on to this line on the first positive-going edge of the S/C Clock after the Command Ready Acknowledge line is set true. This action continues until the LSB is read and shifted, at which time the Ready and Acknowledge lines are set false.

5. Data Ready - ESA to S/C

   This is the line for notifying the S/C that the 256-bit data word is ready to be sent from the ESA. It is equivalent ot the Command Ready line in the other direction. It is set true on the positive-going edge of the Clock.

6. Data Ready Acknowledge - S/C to ESA

This line notifies the ESA that the S/C is ready to accept the serial data from the ESA. It may be set true at any time.

7. Data Output - ESA to S/C

This is a serial data line for transmitting ESA output data to the S/C. The first bit of the Data word is not available on this line until the first positive-going edge of the Clock after the Data Ready line and the Data Ready Acknowledge are set true, and is read on the next negative-going edge of the Clock. This action continues until all 256 bits are read and shifted, at which time the Data Ready line goes false.

APPENDIX F

COMMAND AND DATA BIT DEFINITION

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This appendix describes the bit assignments used to input commands to the analyzer and to output data to the spacecraft. Table F-1 gives the input command bit assignments. Table F-2 lists output data bits in the sweep mode. Table F-3 gives the output data bit assignments for the dwell mode.

Table F-1. Input Command Data Bit Assignments

Channeltron Voltage			Analyzer Voltage				Sweep Time and Channel Dwell Modes				Sun Sensor
MSB			Command Word								LSB
7	6		5	4	3		2	1			0
0	0	0 V	0	0	0	7.3 V	0	0	0.25 sec		0 Enabled
0	1	2200 V	0	0	1	15.6 V	0	1	1 sec		1 Disabled
1	0	2400 V	0	1	0	33.3 V	1	0	10 sec		
1	1	2600 V	0	1	1	71 V	1	1	Dwell Mode		
			1	0	0	151 V					
			1	0	1	322 V					
			1	1	0	685 V					
			1	1	1	1460 V					

Table F-2. Output Data Bit Assignments - Sweep Mode

Bit Location	Bit	Designation
1	23-	MSB
2	22	
3	21	
.	.	24 data bits - count from lowest energy channel
.	.	
23	1	
24	0-	LSB
25	5-	MSB
26	4	3 voltage code bits for 1st energy channel 000
27	3-	LSB
28	0	Sun sensor bit
29	23-	MSB
30	22	
31	21	24 data bits - count from 2nd energy channel
.	.	
.	.	
52	0-	LSB
53	5-	MSB
54	4	3 voltage code bits for 2nd energy channel 001
55	3-	LSB
56	0	Sun sensor bit
.	.	
	Six additional data units for energy channels 3 through 8	
.	.	
225	7-	MSB
226	6	
227	5	
228	4	Playback of input command word
229	3	
230	2	
231	1	
232	0-	LSB
233	7-	MSB
234	6	
235	5	
236	4	Diagnostic data - bits 7 through 1 are checksum
237	3	Bit 0 is counter test indicator, 1=success,
238	2	0=failure
239	1	
240	0-	
.	.	
	Bits 241 through 256 are not assigned	

Table F-3. Output Data Bit Assignments - Dwell Mode

Bit Location	Bit	Designation
1	23-	MSB
2	22	
3	21	
.	.	24 data bits - counts in commanded energy channel
.	.	
.	.	
24	0-	LSB
25	5-	MSB
26	4	Commanded energy channel - analyzer voltage code
27	3-	LSB
28	0	Sun sensor bit
29	7-	MSB
30	6	
31	5	
32	4	Playback of input command word
33	3	
34	2	
35	1	
36	0-	LSB
37	7-	MSB
38	6	
39	5	
40	4	Diagnostic data - bits 7 through 1 are
41	3	checksum. Bit 0 is counter test indicator,
42	2	1=success, 0=failure
43	1	
44	0-	


DATE
ILME