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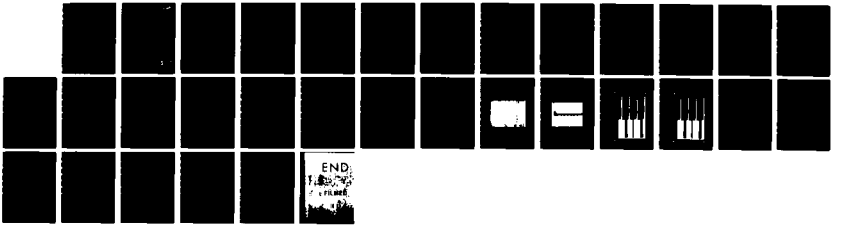

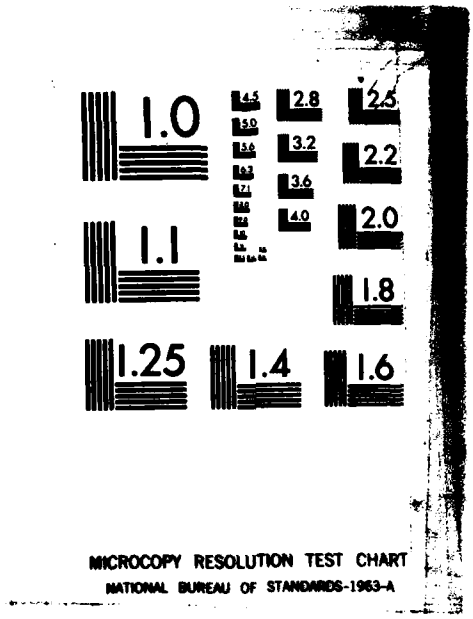
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TECHNICAL REPORT NO. 14

A MODULAR TWIN BUS MICROPROCESSOR SYSTEM FOR LABORATORY AUTOMATION

by

Bruce H. Newcome and Christie G. Enke

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This modular microprocessor system can be used to create a wide range of custom-tailored computer systems out of a standard set of active modules. New modules can be easily incorporated into the system as the requirements of the instrumentation change and as improved integrated circuits become available. A unique feature of this system is the existence of two sets of bus traces on the mother board. The second bus can be used as an extension of the system bus, an interprocessor bus in a distributed processing system, a hardware driven peripheral bus, or the system bus of a second microprocessor. The

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20. Abstract (continued)

second bus is shown to add substantially to the versatility and power of the system. The second bus also provides the means by which a single processor system can be upgraded into a distributed processor network without obsoleting the special interfaces designed for the single processor.

A Modular Twin Bus Microprocessor System For Laboratory Automation

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ABSTRACT

This modular microprocessor system can be used to create a wide range of custom-tailored computer systems out of a standard set of active modules. New modules can be easily incorporated into the system as the requirements of the instrumentation change and as improved integrated circuits become available. A unique feature of this system is the existence of two sets of bus traces on the mother board. The second bus can be used as an extension of the system bus, an interprocessor bus in a distributed processing system, a hardware driven peripheral bus, or the system bus of a second microprocessor. The second bus is shown to add substantially to the versatility and power of the system. The second bus also provides the means by which a single processor system can be upgraded into a distributed processor network without obsoleting the special interfaces designed for the single processor.

INTRODUCTION

The microcomputer system described in this article was developed in our laboratory specifically for the purpose of automating a variety of research instruments and to support research in the development of new methodologies in computer-based instrumentation. In recent years a number of research groups have designed microprocessor systems that are better suited to the research environment than either the popular personal computer designs or the industrial modular microcomputer systems.(1-8) This system is a second generation design which incorporates a number of concepts derived from experience with both the ADD8080 system (4,5,6) and from a previous system in our laboratory (7,8). The system is modular, but a wide variation in module size is provided. Individual function modules which differ widely in their circuit complexity can be combined in compact systems that match the specific requirements of each instrument exactly. This modularity also allows the microcomputer system to be easily modified by the addition,deletion, or replacement of individual functions as the needs of the experiment change.

A significant feature of this system is that the basic card structure can support two busses. One bus functions as the usual microprocessor bus. Modules can be connected to either bus or to both busses. Examples of applications of the second bus are an interprocessor bus in a distributed processing network, a hardware driven bus used for high speed data aquisition, and the local bus of

another microprocessor system acting as an intelligent peripheral.

The various sized single function modules (CPU,Memory,I/O port,etc.) are interconnected by soldering them to another printed circuit board which has two sets of bus traces (figure 1). The set of all these modules make up a "library" of functions from which specific microprocessor systems can be constructed by selecting just the modules needed. This minimizes the design time needed to construct any new system. The accomodation of various sized modules on the dual-bus board allows each module to be only as large as its function requires. The result is a very compact system. With currently available commercial board level systems (e.g. MULTIBUS (9) or STD (10) boards) the size of the board invites combining functions that require only a fraction of a board or, in other cases more than one board is required to accommodate a single function. In developmental systems, the ability to upgrade or replace functions on an individual basis, as this system allows, is very important. The principal physical support elements in the system are the dual-bus board which supports the active modules and the backplane which provides bus interconnections among a set of dual-bus boards. Soldered connections between the modules and the dual-bus board eliminate the contact cost and contact reliability problems normally encountered in small module systems. High reliability plug and socket connections between the dual-bus board and the backplane provide a system that is modular on the board level, compact, and easy to maintain. As will be shown, the dual bus capability is an essential aspect of the system's

versatility.

HARDWARE DESCRIPTION

A. DUAL-BUS BOARD

The dual-bus board consists of two sets of bus and power traces on one side of the board and a ground plane on the other. As shown in figure 2, solder pads are provided at one inch (2.54 cm) intervals along the bus traces to provide connection to the pins of the active modules. This allows the modules to be made in different widths from one inch (2.54 cm) to nine inches (22.86 cm) according to the amount of space needed, and also allows various parts of the bus to be picked up at different places on a module's circuit board. This last feature is important since it reduces the amount of board space used for bussing signals around the module and thus allows a more compact layout. It provides the laboratory equivalent of a multilayered board.

The bottom bus traces are always used as the system bus. This bus and a number of board-specific signals are connected to the mother board by a right angle header along the rear edge of the board. The top bus traces can be used in two ways; either as an extension of the system bus by adding a set of vertical jumpers to interconnect the two sets of bus traces or as a separate auxilliary bus which can be connected through the backplane by completing the interconnection to the backplane contacts. If the top bus is used as an extension of the

system bus, the board-specific connector space (the header contacts at the top half of the rear edge) can be used to carry input/output signals through the backplane to the instrument under control. By making all connections between the instrument and the circuit boards through the backplane connector, the boards can be unplugged or extended without having to disconnect or rearrange cables.

B. BACKPLANE

The backplane (fig. 3) has four sets of holes where connector sockets can be mounted to receive the dual-bus board's header. The power and system bus signals are connected along the lower half by a set bus of traces; the board-specific signals such as connections to external devices are brought out to pads where various types of cable connectors can be soldered to them (now committing that slot to that specific board). Pads are also provided to jumper the system bus to another backplane when a system requires more than four dual-bus boards. The backplane is designed specifically to attach to the rear of the edge guides of a Bud(11) SR-20108 card cage. The backplane circuit board is 3/32" thick to provide extra stability for insertion and removal of the dual-bus boards.

C. ACTIVE MODULES

The standard active modules are listed in Table I along with

their principal integrated circuits and width in inches. All of the modules are half height (3.7in, 9.4cm) and connect to a single set of bus traces except the bus multiplexer and graphics controller which are full height (7.8in, 19.8cm) and connect to both busses on the dual-bus board. As can be seen from the table, a number of interface functions are included along with all of the functions needed to create a basic system. This allows new instrument interfaces to be created by the simple addition of standard modules. The module list is constantly being expanded as new functions are being implemented. A conscious effort is made to design each new module to meet general purpose applications as well as satisfy the initial "motivating" application. Good documentation also facilitates new applications of existing designs.

D. DEVELOPMENTAL AND EXPERIMENTAL GOALS VS PRODUCTION DESIGN

It is widely recognized that circuit board area and number of connectors (the most expensive part of electronic systems) are reduced as the board size increases. Thus the goal of economy is in conflict with function-level modularity which provides flexibility, adaptablity, and ease of upgrade and repair. The latter attributes are essential in systems designed for research and development in computer-based instruments, while economy of production is essential for a commercial design. The system described here moves easily from development to production by replacing dual-bus boards with proven combinations of function modules with identically sized, single boards

which duplicate those combinations of functions exactly. The modularity or replaceability would then occurs on the level of the 8"x 10" circuit board size, a size which is a good compromise between economy of production, reliability and ease of maintainance.

DUAL BUS CAPABILITY AND APPLICATION

A unique feature of this system is the existence of the top bus on the dual-bus board. The simplest use of the top bus is as an extension of the system bus where it increases the compactness of the system by doubling the space for system function modules. However, the special capability provided by this second bus is taken advantage of when it is used as an auxilliary bus. Several examples of such auxilliary bus applications are described below.

The original purpose of the top bus was its use as an interprocessor bus in a network of microprocessors. Full height interface modules have been designed which control the communication between the system (lower) and interprocessor (upper) busses. With one set of these modules for each processor, up to 8 microprocessors can be interconnected into a distributed processing network for instrumentation applications for which more than a single microprocessor is required. The details of the network configuration and the interprocessor hardware are described in a related paper (12).

Another important use of the top bus is it's use as a "peripheral bus". This is a bus where the address and control signals are generated by hardware other than the microprocessor. For this type of application a full height bus multiplexer module was developed which can multiplex the two sets of traces on a single dual bus board. This capability of multiplexing between the system bus and the peripheral bus has facilitated the development of some very powerful interfaces. The use of the bus multiplexer in switching modules between the two busses is illustrated in figure 4. This module consists of two pairs of tri-state buffers each one of which buffers the data, address, and control signals on the bus. One pair of buffers (A,D) connects the top set of traces to the peripheral bus and the bottom set of traces to the system bus. The other pair of buffers (B,C) connects the top set of traces to the system bus and the bottom set of traces to the peripheral bus. Thus if memory modules are connected to both the top and bottom set of traces, selecting one pair of buffers or the other allows banks of memory to be swapped between the two busses. This allows data to be written into memory at hardware speeds over the peripheral bus then exchanged with memory which was previously on the system bus. Collected data can then be read by the system bus for processing while new data is being collected in memory on the peripheral bus with virtually no time wasted in the transfer of the collected blocks of data. In this manner data can be taken at direct memory access (DMA) speeds without stopping the microprocessor.

In a spectrophotometric instrument developed in our lab(13), the

linear diode array detector employed needs rates of storage that normally would require a DMA controller. However if a conventional DMA controller were used, the processor would be held during data transfer and there would be insufficient time between transfering blocks of data to load the instrument parameters for the next block of data. A solution to the problem which takes advantage of the dual bus is the microprocessor system shown in figure 5. The top bus on several dual-bus boards is used as a peripheral bus which is connected from board to board through a ribbon cable connected across the top of the backplane. One of the dual bus boards in the system contains a bus multiplexer and two banks of memory and another contains an ADC, a set of counters to generate the addresses, and the logic needed to generate the control signals for the peripheral bus. Thus while a block of data is being converted and stored in memory by the hardware, the microprocessor can be loading the interface with the parameters for the next block of data.

Another example of the use of a peripheral bus application of the top bus could be as the memory bus of a raster video controller. This implementation would allow data to be moved between the video controller and memory without interferring with the microprocessor's operation. It would also allow the use of standard memory modules which would simplify the design and construction of the video controller module. The capabilities of the graphics system could then be tailored to the individual application by varying the size of graphics memory according to the desired resolution and/or color

capability of the system.

A third possible use of the top bus is as a second microprocessor's system bus. By using the bus multiplexer, blocks of data could be moved quickly between two microprocessors. For example, one of the two microprocessors could act as an intelligent data base manager for the main processor. Upon receipt of a request for data from the main system, the data base manager computer would search the data base for it, store the requested information in the switchable memory for transfer to the main system, and notify the main computer of the task completion.

ACTIVE MODULES OF PARTICULAR INTEREST

A number of the active modules have unusual design features or particularly versatile properties and thus warrant more detailed description. The RAM/ROM memory module shown in the lower right-hand corner of figure 1 can take a mixture of PROM or static RAM memory chips that have the standard 24-pin layout. Software can be developed in RAM, burned into PROM and then reinstalled in the same board. This module has a total capacity of 8 Kbytes if 1 Kbyte and/or 2 Kbyte memory chips are used but the capacity increases to 16 Kbytes if 2 Kbyte and/or 4 Kbyte memory chips are used. The type of memory chip that each socket can contain and the total capacity of the module is programed by wire-wrap jumpers on the board.

The differential transceiver module is very useful when parts of the interface to the instrument have to be remote from the microprocessor. It also allows a subset of the system bus to be differentially driven to the remote interface, thus reducing noise problems encountered when standard TTL signals are driven a significant distance. The availability of this module also encourages the placing of DACs and ADCs remote from the microprocessor which results in shorter analog signal paths and thereby improved performance.

The address decoding for all the modules other than memory is done on a separate chip select module to avoid the duplication of this function on each module. The chip select module is 9.4cm (3.7in) high and 5.1cm (2in) wide and is shown in the upper left-hand corner of figure 1. The schematic diagram for this module is presented in figure 6. The circuit consists of two 74LS136 quad exclusive-or gates which decode the most significant seven address lines. They produce an active HI signal when the 512 byte block of addresses specified by jumpers J1 through J7 is addressed. This signal is used is used to enable a 74LS138 decoder which decodes address lines A8,A7,and A6 to form eight active LO chip select signals of 64 bytes each. The highest chip select output is also used to enable a second 74LS138 decoder which decodes A5-A3 to subdivide it into eight eight-byte chip select signals. The second decoder is also qualified with Read and Write command signals so that the chip select signal are LO only during a valid read or write. This makes these select lines useful

for latching data and strobing flip-flops in user interfaces.

A schematic diagram of the parallel input-output module is given in figure 7. This module was chosen to illustrate the ease and simplicity with which a module can be designed using LSI circuits. The module consists of an 8255A-5 parallel I/O port and a 74LS04 inverter mounted on a 2" wide board. Three sockets for jumpering the 24 I/O lines off board (usually to the top rear board connector) and a place to connect a chip select signal are provided. Also available for convenience are several uncommitted inverters and various bus signals.

SOFTWARE

Along with the modular approach to the hardware, an approach to the microprocessor software which is modular, easily minimized, and well suited for control and experimentation is needed. The polyFORTH programing system from FORTH,Inc was selected for implementation in this system(14). Many of its special features make it nearly ideal for this kind of application. Much of its desireability and success in this system are because it, like the computer system, was especially designed for instrument control and programmable experimentation. Its principal feature is that as the program for each function is developed, the name of the program becomes a command in the language. Thus the language develops naturally to a higher and

higher level as more code is written. The high-level language produced is specific to the functions needed by the application at hand and no more complex than necessary for that application. The speed of program execution is faster than most compiled high level languages and only a little slower than programs written in assembly language. The system overhead required is very small - as little as 1 Kbyte in a minimum system. Versions of code appropriate for ROM can be easily produced. Despite its simple implementation for basic operations, it evolves easily into a sophisticated, powerful operating system including even multi-tasking capabilities.

CONCLUSIONS

This system has been used extensively in our department in at least twelve instruments for over two years with excellent results. It has been used to automate a wide variety of instruments such as an absorbance-corrected flourometer, a diode array spectophotometer, a triple quadrupole mass spectrometer, and a coulostatic electrochemical analysis system. These systems have been very reliable with no development of contact problems which plagued previous micro systems in the laboratory environment. Though these systems are very different in their functions and modes of operation, the common elements in hardware and software greatly facilitated their development. As can be seen from table 1, the large variety of completed module designs allows most new systems to be constructed in

2 to 3 weeks. The use of FORTH language also helps speed the development of new systems because it provides an easy way to write modules of testable code for each function which then naturally evolve into a high level command language.

ACKNOWLEDGEMENTS

We would like to acknowledge the many helpful suggestions of H. Gregg, C. Myerholtz, and P. Aiello. This work was supported in part by the Office of Naval Research.

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9) Multibus is a tradmark of Intel Co., Santa Clara, CA..

10) STD Bus is a trademark of Prolog Co., Monterey, CA..

11) Bud Industries, Inc. Willoughby, OH..

12) Newcome and Enke (in preparation)

13) Aiello,P.J. Enke,C.G., ACS Symposium Series "Image Devices in Spectroscopy", in press.

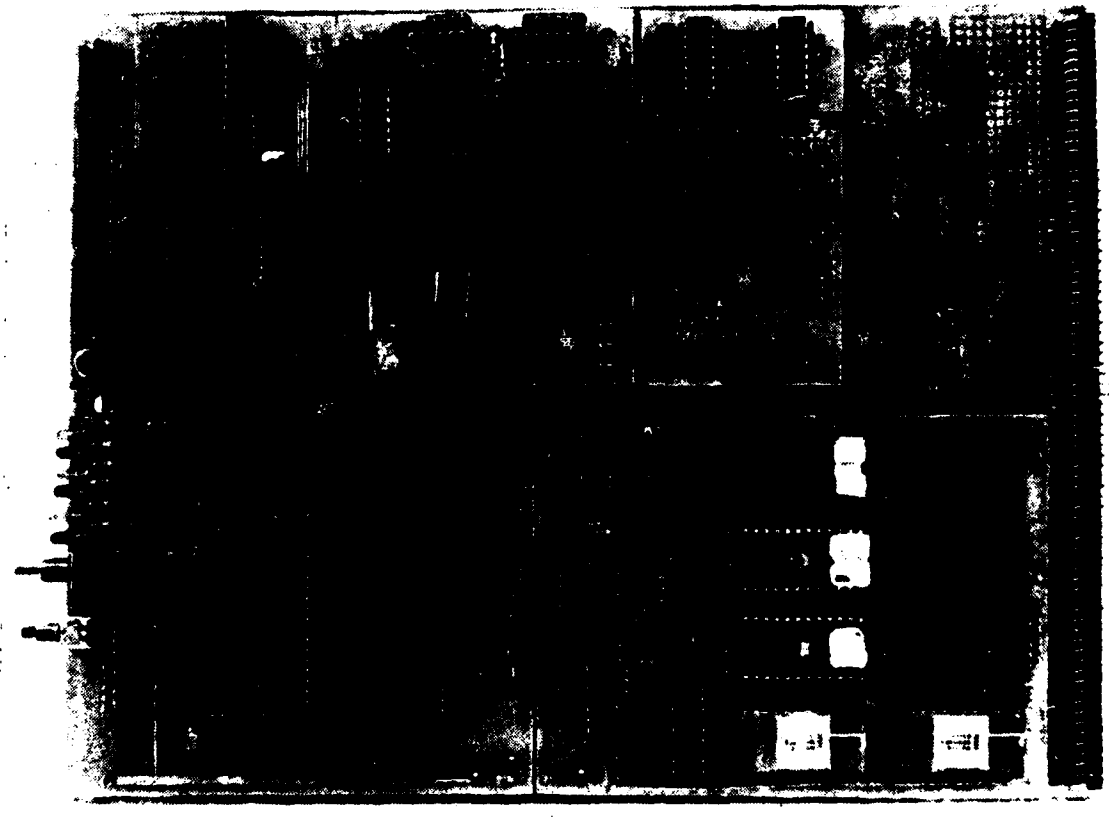
14) PolyForth is a trademark of Forth,Inc. Hermosa Beach, CA..

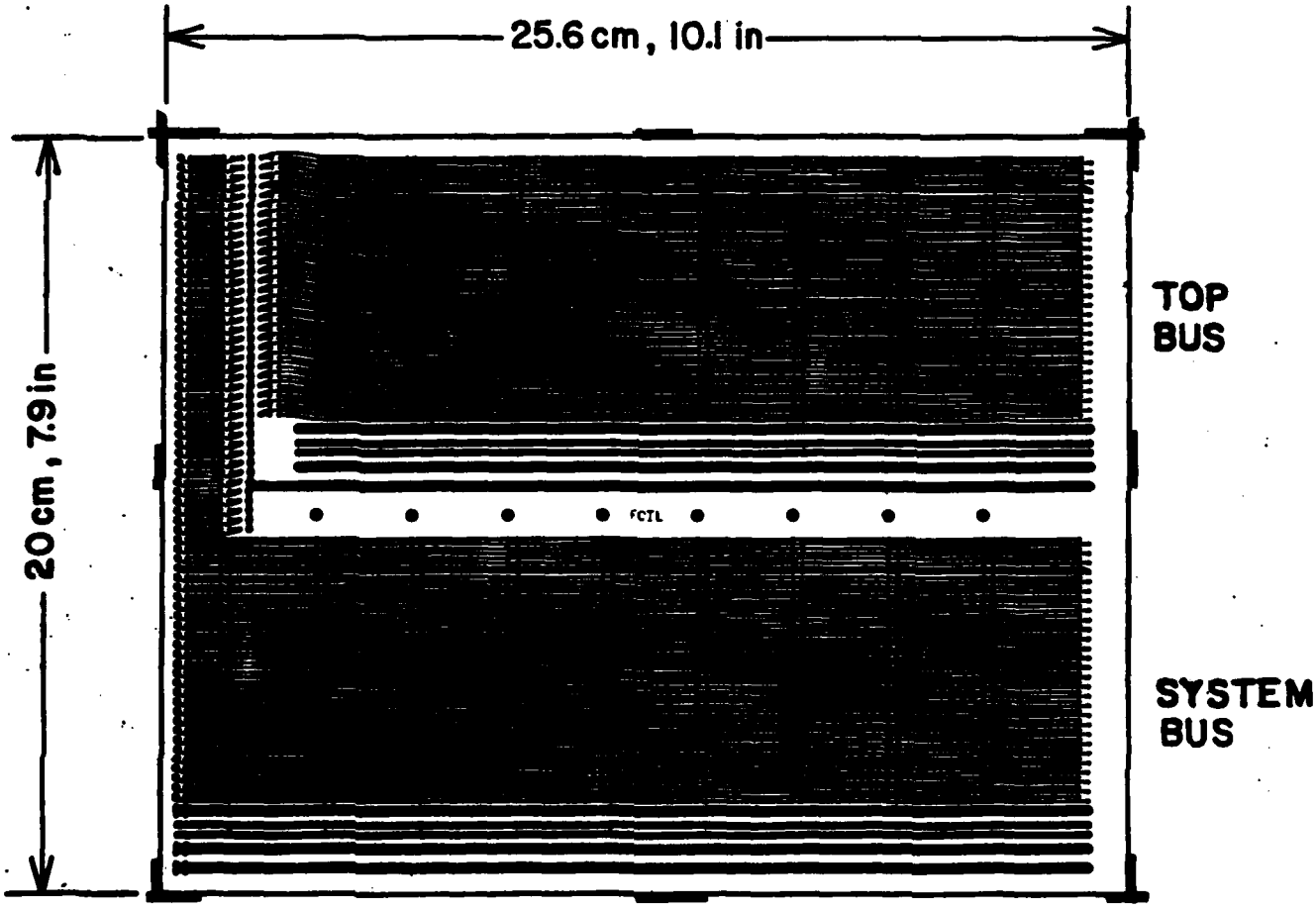
List of Figure Captions

Table I. Standard Active Modules

This Table list all the currently available active modules that have been designed for this system along with their widths in inches and the principal integrated circuit that was used to implement the function.

MODULE	WIDTH (in.)	I.C.
CPU I	5	8085A
CPU II	5	8088
RAM/ROM	5	4118,2716,2016,2732
INTERRUPT CONTROLLER	2	8259A-5
DUAL USART	3	8251A
PARALLEL I/O	2	8255A-5
8K RAM	5	2114
CHIP SELECT	2	*
COUNTER/TIMER I	2	8253-5
COUNTER/TIMER II	2	9513
DUAL DAC (8-BIT)	1	AD558
DUAL DAC (12 BIT)	3	DAC1230
BUS MULTIPLEXER	3	*
ADC (12 BIT)	2	AD574
DIFFERENTIAL TRANCEIVER	3	75119
WAIT STATE	1	*
ACTIVE TERMINATOR	1	NONE
AC TERMINATOR	1	NONE

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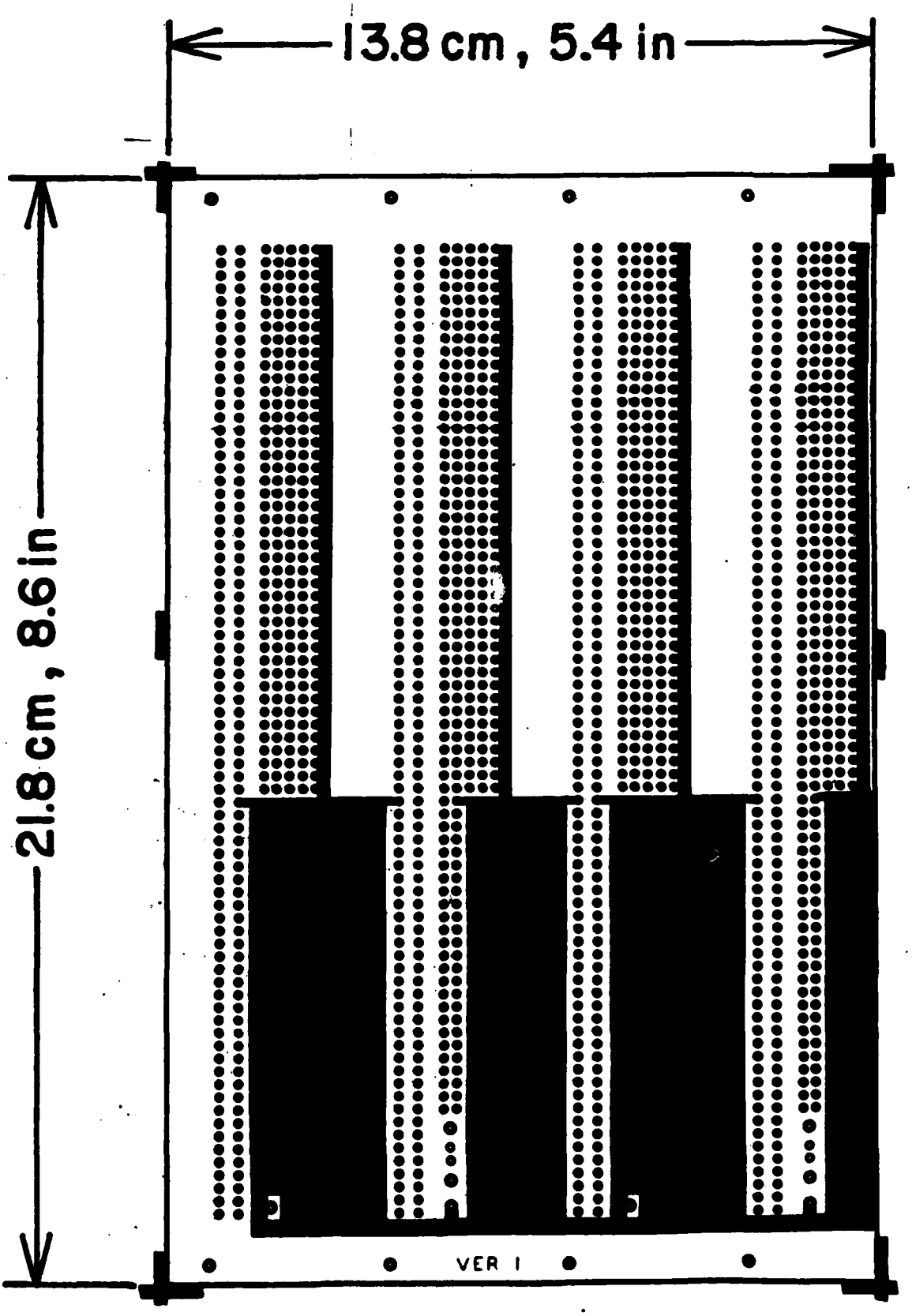
BUS
FCTL
SYSTEM
BUS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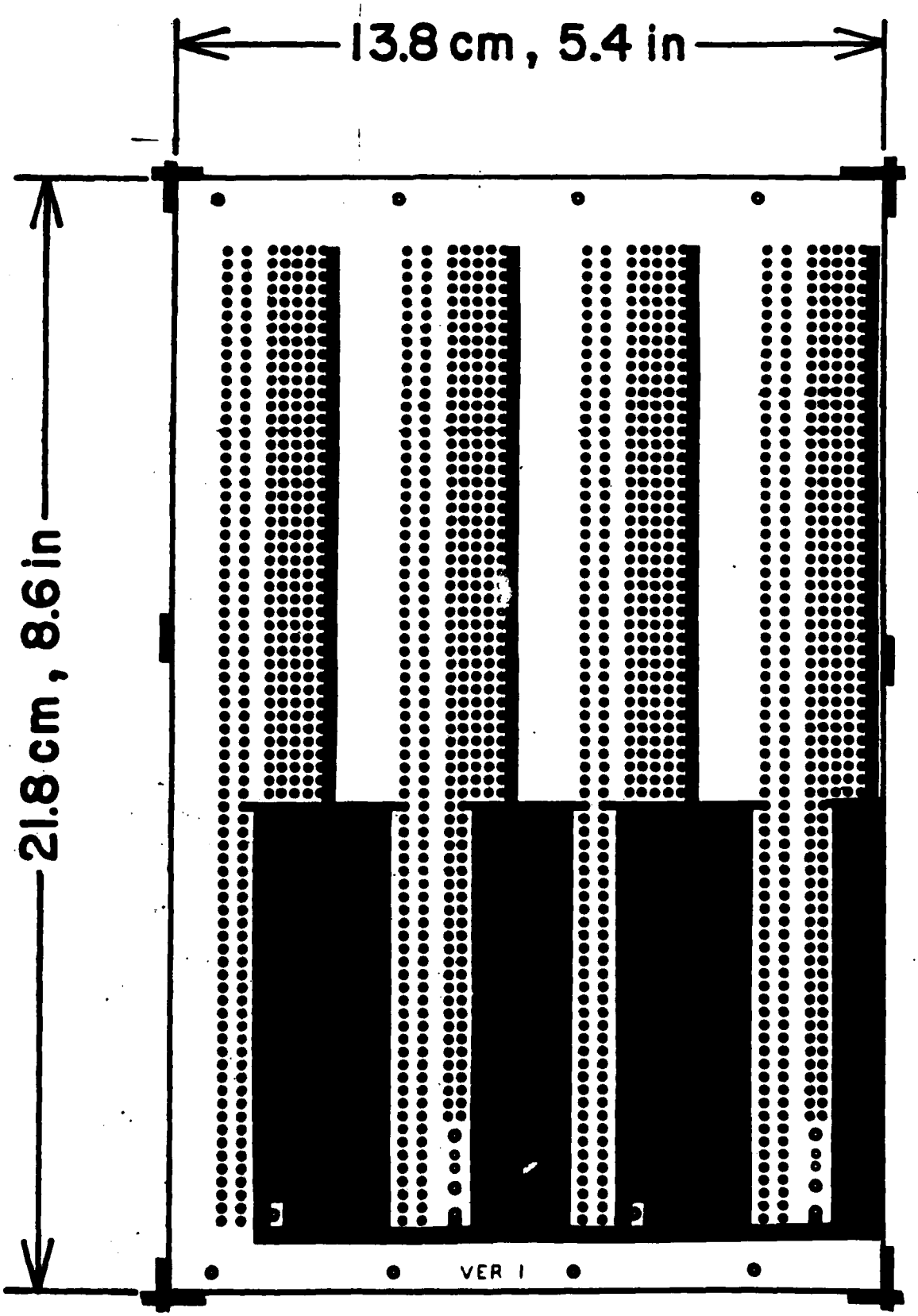
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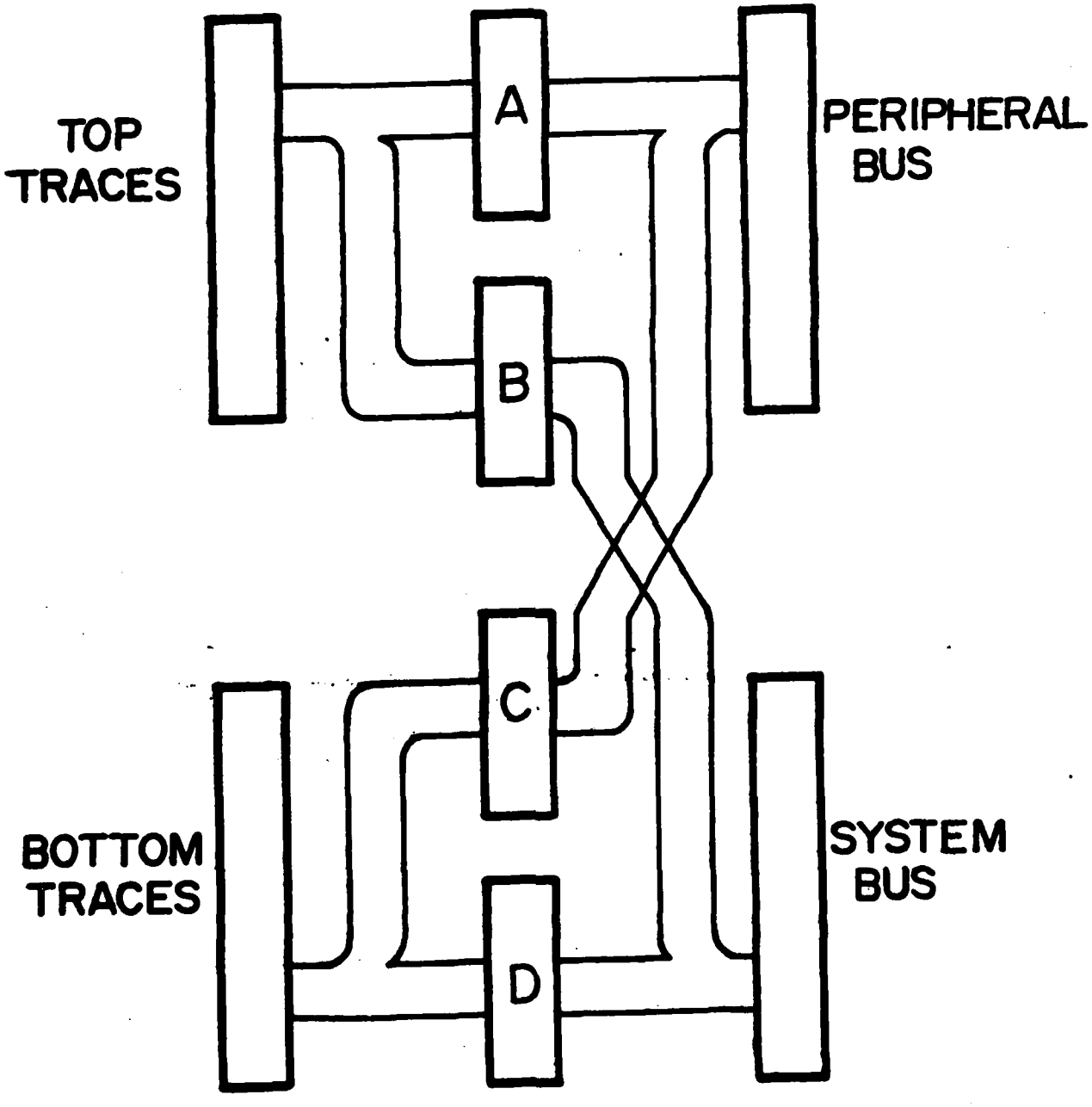
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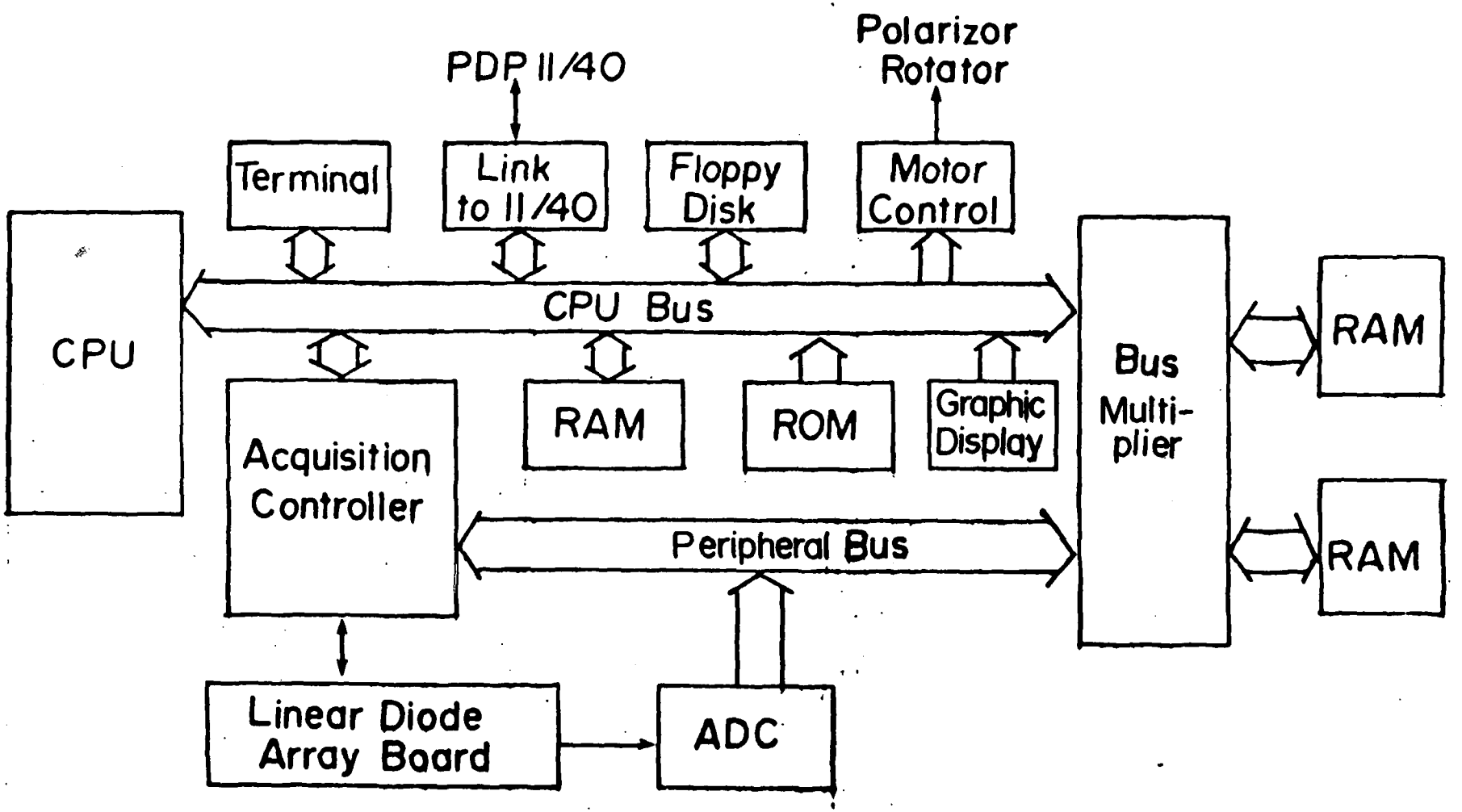
BUS
BOTTOM
TRACES
SYSTEM
BUS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Polarizor Rotator
Terminal
Link to 11/40
Floppy Disk
Motor Control
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Bus Multi-plier
RAM
RAM
ROM
Graphic Display
Acquisition Controller
Peripheral Bus
RAM
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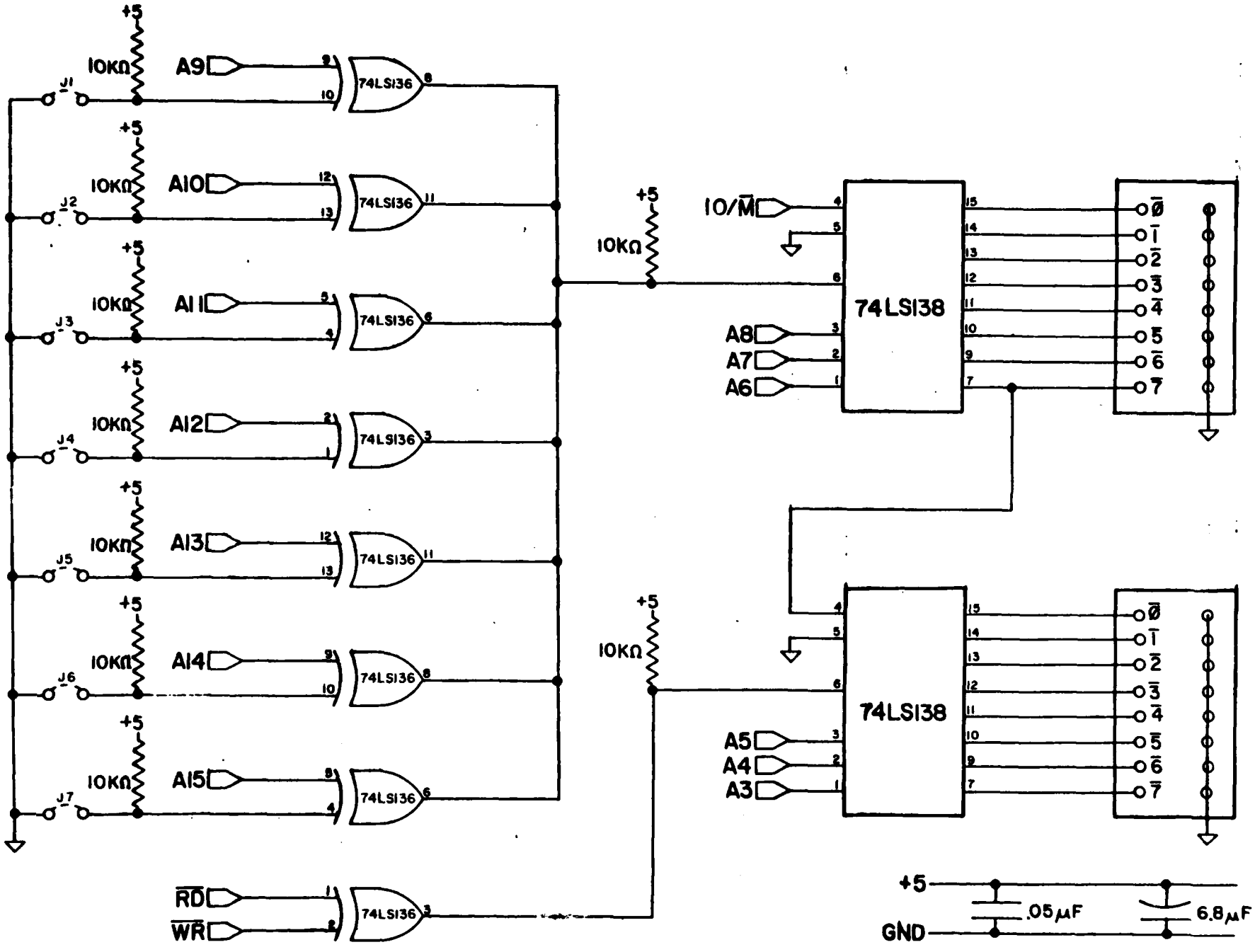
ADC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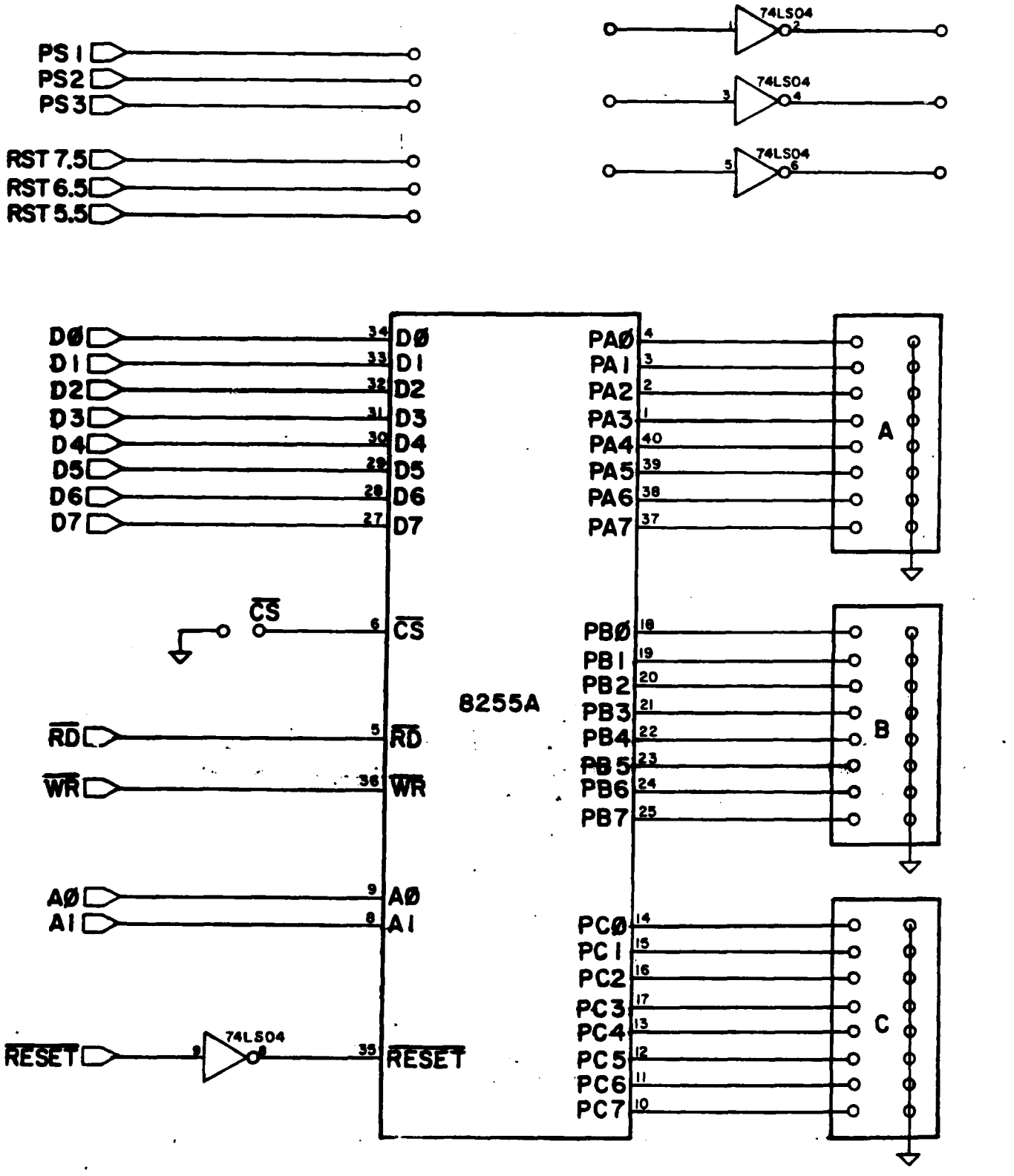
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