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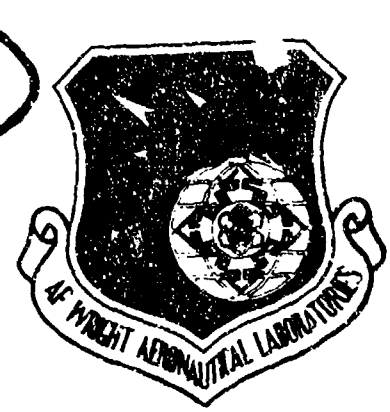

A STUDY OF DIGITALLY CONTROLLED FLIGHT CONTROL ACTUATION

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This report describes a study of flight control actuation systems with an objective to determine the degree of digitalization possible between the digital flight control processor and the control surface. A typical analog actuation system is defined as a reference for comparison with five alternates, each mechanized with increasing amounts of digital equipment.

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The report provides a basis for determining the direction of digital actuation systems. It verifies that distributed actuation systems are now feasible and promise enhanced performance, reliability, and cost reductions.

FOREWORD

This report, "A Study of Digitally Controlled Flight Control Actuation," was prepared by HR Textron Inc. for the Controls Systems Development Branch of the Flight Dynamics Laboratory, Air Force Wright Aeronautical Laboratories. Work was performed under contract F33615-80-C-3623, program element 62201F, project 2403, work unit 24030275. Mr. Duane Rubertus was contract monitor for the Air Force Wright Aeronautical Laboratories.

This report covers work initiated August 1980 and completed July 1983.

The technical report project was directed by Howard H. Belmont with consulation from David Carleton, James Coakley, Lowell Lykken, and Manfred Runkel. Individual contributions were made by Alan Dippel, Dennis Gilroy, Doug Keever, and Eric Abrahamsen, and members of the Systems Engineering Computer Group of HR Texton.

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SUMMARY

Digital technology has effectively been applied to the computational aspects of flight control systems but must interface with traditionally analog power elements (e.g., hydraulic servo actuators).

To evaluate this interface, the flight control actuation subsystem was defined in terms of three equipment elements (control processor, servo processor and servo actuator complex) and their communication interfaces.

It was then possible to synthesize these elements as digital or analog or as a combination. It was also possible to evaluate the assignment of functions to these elements and to evaluate location options for the servo processors.

A set of design issues were then identified with respect to these elements and these included the above-mentioned functional task assignments and physical locations; but in addition, included requirements on a serial bus, electronics capable of a high temperature environment, feasibility of digital mechanization, and fault detection/redundancy management considerations.

These element alternatives were evaluated by synthesizing five actuation system configurations and comparing them in performance and physical factors to a baseline configuration of known characteristics. An HR nonlinear computer model was used to evaluate performance. Calculations were made of weight, cost, and reliability. Estimates were made where hardware was not developed.

Results showed no essential change in performance for configurations in which digital mechanizations were limited to electronics and the electrohydraulic servovalve. Digital implementation at high power levels (actuator) could not meet performance objectives, and physical/cost/reliability objectives were exceeded.

The most significant result was projected by configurations which placed the servo processor in proximity to, or integrated with, the actuator itself. This resulted in the substitution of a digital serial bus for large bundles of wires between the control processors and the actuators. Electronics to withstand this environment was found to be "developed" on a government sponsored program, but not yet in production.

Recommendations for new development programs include (1) the application of now-available high-temperature digital electronic circuits to the design of a servo processor to be integrated with the actuator, (2) design, fabrication, and test of a flight worthy "smart actuator", (3) development of a control-loop optimized, serial data bus, (4) study of flight control architecture based on distributed systems and "smart actuator" hardware.

SECTION I
INTRODUCTION

A. BACKGROUND

A revolution in electronic computational and communication devices coupled with evolutions in actuation devices has created opportunities to improve the performance, availability, and maintainability of flight control systems at lower development procurement and operational costs. At the same time, designs of new, manned aircraft with special maneuvering requirements have placed ever increasing demands on flight controls and their interaction with engine controls, armament controls, navigation systems, and the cockpit interface.

The most significant events in the electronic revolution are those related to digital technology. The first stage has already taken place through the introduction of the digital computer to perform computations for vehicle control-law transfer functions.

During the course of the technology survey involved with this study, it was noted that the majority of the flight control technology-based programs were being funded in the areas of digital processing and software developments and in sensor design and development. Both of these activities were focused on near-term payoff for production flight control applications.

A review of technology programs in the actuation area showed that effort was oriented toward the direct drive valve, 8000 psi non-flammable fluids and toward the all-electric airplane. However, only a limited amount of R&D has been accomplished on digital actuation; therefore, this work and the results that were obtained are considered to be quite timely.

The near-term gap identified was an optimization of the interface between a digital computational element and an ultimate analog control surface.

B. STATEMENT OF THE PROBLEM

Digital technology has been applied to flight control systems quite effectively and efficiently, particularly in the computational elements. Further, it has a higher reliability than many of its analog counterparts.

The problem in flight control actuation systems is that the control surfaces are analog, requiring considerable power. The question is "Where should the digital-to-analog conversion take place?"

C. TECHNICAL APPROACH

The technical approach adopted for this study was to establish an in-depth paper analysis involving a definition of the major elements of an actuation system. Various configurations were developed involving these elements from a baseline to modified forms wherein the digital-to-analog point was moved along the control path from command generator to power transducer. As this process developed, several "issues" arose requiring analysis in order to understand their implications on overall design goals and requirements.

D. STUDY OBJECTIVES

This study addresses questions concerning the interface of redundant flight control computers with redundant actuators. In particular it asks: "Where is the optimum digital-to-analog conversion point between the control processor and outward to the actuation device itself?" The details involve:

- What elements of the actuation system (servo processor and actuator complex) should be mechanized in digital technology?
- Where can and should the servo processor electronics be located?

- Considering the options in elements and locations, what interface data communications are required between the elements of the flight control actuation system?
- What is the optimum configuration for today's technology?
- What is the optimum configuration for future technology?
- What development programs are recommended to be pursued?

E. GROUND RULES

- The flight control system selected as a baseline was a triplex, analog, fly-by-wire system driving a hydraulically powered active-on-line actuation system as a primary surface. Specifications are contained in Appendix A.
- The baseline system is commanded by analog computers. All other configurations are commanded by digital processors. Baseline characteristics are detailed in Appendix B.
- The flight control computer configuration is a triplex self-checking pair based on "A Multi-Microprocessor Flight Control System," Honeywell Systems and Research Center, May 1981, AFWAL-TR-81-3044.
- For study purposes it was assumed that the flight control system is for a vehicle with 12 fly-by-wire controlled surfaces.
- For the purposes of this study, "digital" includes techniques such as pulse-width modulation or other discontinuous signal forms.
- The control processor's cost, weight, reliability, and software are not incuded in the study. It is assumed the processors are providing information at a specified output data rate.
- Configuration performance comparisons are made by a servo-actuator dynamic analysis computer program, described in Appendix C.

SECTION II
TECHNICAL APPROACH - ELEMENTS, ISSUES AND CONFIGURATIONS

The technical approach taken was to break down the flight control actuation system into equipment elements. This was done in order to assess what functions should be assigned to these elements, how they were to be dispersed within the airfra , and their equipment content - analog or digital.

A. DEFINITION - ACTUATION SYSTEM ELEMENTS

The actuation system is displayed in figure 1 to include the three equipment elements and the communication links between them. The elements and links are defined as follows: The definition of the functions performed are tentative and later analysis will evaluate these choices.

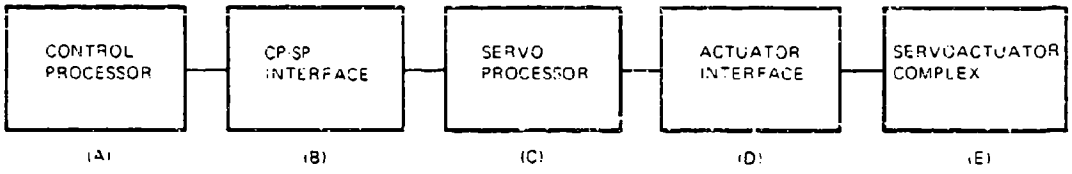

Figure 1. Actuation Systems Elements

- Control Processor - This element is that portion of the flight control computer complex devoted to generating the control surface command signals.
- CP-SP Interface - This is the communication link between the control processor (A) and the servo processor (C).
- Servo Processor - This element performs the functions, electrically of servoamplification, failure detection, servo loop closure, redundancy management, and electrical/ hydraulic power control.
- Actuator Interface - This is the communication link between the servo processor (C) and the servoactuator complex (E).

- Servoactuator Complex - This element contains the various actuator components including the electrohydraulic valve, hydraulic amplifiers, power cylinder (ram), position and pressure transducers, hydromechanical failure detection, and hydraulic power control devices.

B. CONFIGURATIONS AND ISSUES

Before proceeding with the process of evaluating the effects of mechanizing the elements and links of the actuation system using digital technology, it was necessary to establish a baseline configuration of known performance. This baseline configuration is defined in detail in Appendix B.

From this baseline departure point it was then possible to analyze the effects of digital equipment substitution for the analog equivalents. However, the simplicity of digital inputs and outputs and their interconnection technologies gave rise to options about where the element could be located - in proximity to the control processor, at the actuator, or in an aircraft compartment between.

In addition to the issue of location, other issues arose, and the process of design of alternative system configurations became an iteration process between issues and element design.

1. Issues

As as previously discussed, design options required detailed evaluation. This process began with a top-down approach considering the overall system issues first. Their determination then led to the next level of issues and so on. Figure 2 depicts this progression.

The issues, briefly described below, are analyzed in detail in Section III.

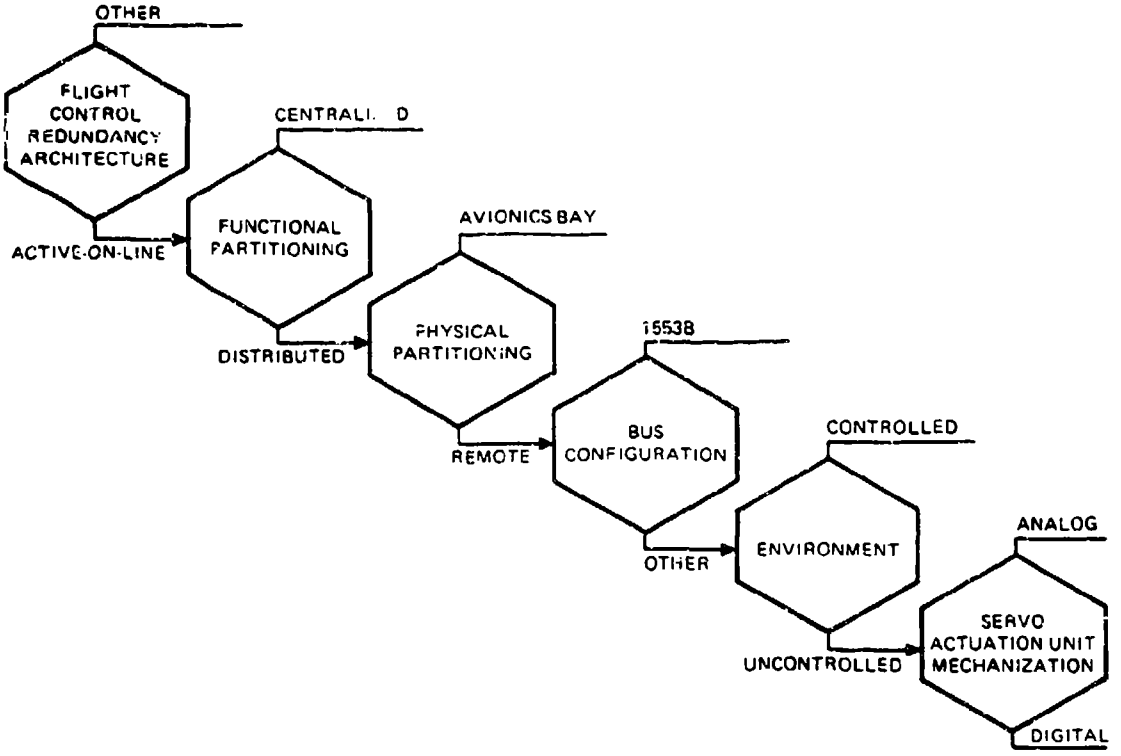

Figure 2. Technical Design Issues Affecting Actuation System Configurations

- Flight Control Actuation Redundancy Architecture:

  Basic architecture to achieve redundancy and reliability objectives

- Functional Partitioning:

  Designation of functions to be performed in each actuation system element.

- Physical Distribution:

  Physical location of each actuation system element.

- Bus Configuration:

  Format, protocol, and application of digital data buses.

- Environment

  Electronics compatible with an uncontrolled temperature environment.

- Servo Actuation Unit Mechanization:

  Digital mechanization of electrohydraulic valves, feedback elements, and actuator power cylinders.

2. Configurations - Five configurations were ultimately selected by this iterative design process. These are not only applicable to flight control systems, but provide a vehicle for evaluating and demonstrating the technical issues involved. The configurations are depicted in figure 3. It should be noted that they progressively show more use of digital technology by virtue of element mechanization or by element physical location, introducing digital communication buses in lieu of hardwire interconnections.

A detailed description of each configuration is provided in Section IV. The following is a brief description of each and a discussion as to why the configuration was chosen:

Baseline - All configurations are referenced to the baseline. It is an active-on-line, triplex system employing, per surface, a triple tandem power stage (ram), three servo valves, and three servo processors. The control processors are a triplex pair which are self-checked through their servo processors, which also monitor the actuator complex. For a 12-surface system, all 12 servo amplifiers per channel are housed in one enclosure with their host control processor.

This configuration was specified because it does not require computer synchronization or cross-channel monitoring except to signal reconfiguration logic, thus simplifying the electronics while providing two-fail-operate redundancy. This system is all analog.

Configuration I - Same as baseline except the control processors are digital. A digital-to-analog converter and notch filter are

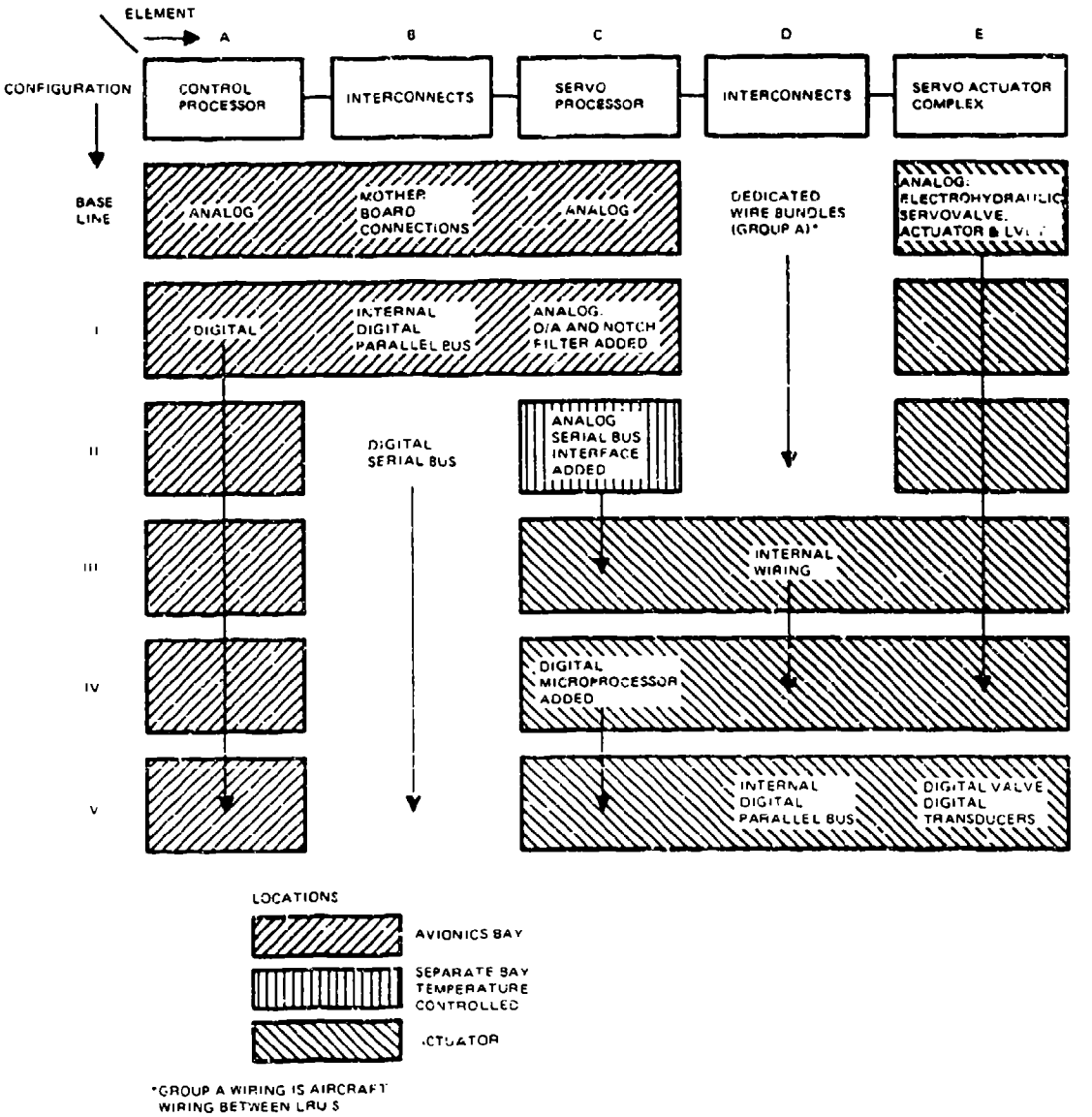

Figure 3. Configuration Vs Element Features

installed at the input to the servo processors to smooth out the control processor's sample rate signal. Loop closure and redundancy management are performed by analog circuits in the servo processor.

This configuration was selected to analyze the effects of a digital sample rate command signal on hydraulic systems and components.

Digital-to-analog conversion is in the servo processor in the avionics bay.

Configuration II - Same as I except that each of the three channels of 12 servo processors are packaged together in a separate, temperature-controlled bay from that of the control processors. Interconnections between a control processor and its servo processors are by means of a digital serial bus.

This configuration was selected to evaluate the use of the MIL-STD-1553B bus and its traffic as a function of performing redundancy management and other functions in the servo processor or in the control processor. Digital-to-analog conversion is in the servo processor in an intermediate location between avionic bay and actuator.

Configuration III - Same as I and II except the servo processors are located at the actuators. This results in 12 groups of three servo processors and places the servo processors in a "high temperature" environment.

This configuration was chosen to evaluate the MIL-STD-1553B serial bus under a different servo processor grouping configuration. It also provides an analysis of the effects of the uncontrolled temperature environment of the actuator on the performance and reliability of the servo processor. Digital-to-analog conversion is in the servo processor at the actuator location.

Configuration IV - This configuration continues to place the servo processors at the actuators. However, dual microprocessors are employed in each servo processor to interface with three serial buses connecting each servo processor with the three sets of control processors. Servovalve modeling and redundancy management are performed digitally in the microprocessor.

This configuration was chosen to evaluate the effect on system reliability of employing a voting plane at the servo processor-actuator.

It also demonstrates the use of a microprocessor in the servo processor - the so-called "smart actuator" concept. Approximately half of the servo processor functions are performed digitally.

Configuration V - This configuration is all digital except for the ram itself. It also employs a microprocessor pair in the servo processor units which performs all functions in a digital format. Feedback position and pressure transducers are digital encoders.

This configuration was chosen to demonstrate the all-digital servo processor and its relationship to digital elements in a servo actuator complex. Digital-to-analog conversion is accomplished in the servovalve.

C. EVALUATION

These selected configurations were evaluated using an HR Textron-developed nonlinear dynamic simulation mathematical model to analyze the performance of the various flight control system configurations. The model was used to evaluate performance in the following areas: system stability, transient step response (includes slew rate, over- shoot, settling time), frequency response, resolution, and failure transients. A detailed description of the equations and relationships comprising the nonlinear model is presented in Appendix C.

Estimates were made of factors affected by physical configuration such as weight, volume, reliability, and cost.

Since certain of the configurations involved the use of technologies not presently developed or in full production, some qualitative assessments were made by HR Textron experts in those fields and compared to the baseline.

Final results, conclusions, and recommendations for future development were then made with projections for anticipated maturation of new technologies.

SECTION III
DESIGN ISSUES

This section addresses, in detail, the design issues that came up for analysis as the configurations described in figure 3 took shape. Given the flexibility, increased capability, and higher reliability of digital technology, the task became one of determining how the use of digital techniques in these configurations could enhance the overall system.

These design issues are derived from detailed configuration designs contained in Section IV:

- Redundancy architecture to achieve reliability objectives.
- Distribution of functions to be performed by each element in the actuation system.
- Physical distribution of the actuation system elements.
- Format, protocol, and application of digital data buses.
- Electronics compatible with an uncontrolled environment.
- Digital mechanization of servo actuator elements.
- Digital control processor sample data rate effects on the hydraulic system.

A. REDUNDANCY ARCHITECTURE

The ground rules established the use of an active-on-line hydraulic actuator configuration for all system configuration studies.

The active-on-line system provides fail-operate, fail-operate, fail-safe redundancy without cross-channel comparisons or voting schemes and with only three channels. The threshold, hysteresis and failure transients compare very favorably with the force-sharing concept. This evaluation was verified in a study, "The Evaluation of a Force-Sharing and an Active-on-Line Fly-by-Wire Actuation System," Dynamic Controls, Inc. Technical Report AFFDL-TR-79-3117 Vol. II, July 1980.

A schematic of an active-on-line actuation scheme is shown in figure 4. In this scheme there are three channels, each having an electrohydraulic servovalve (EHSV) controlling flow to one ram of a triple-ram actuator. One channel is active and controls the static position of the load. The remaining two channels are on-line. The

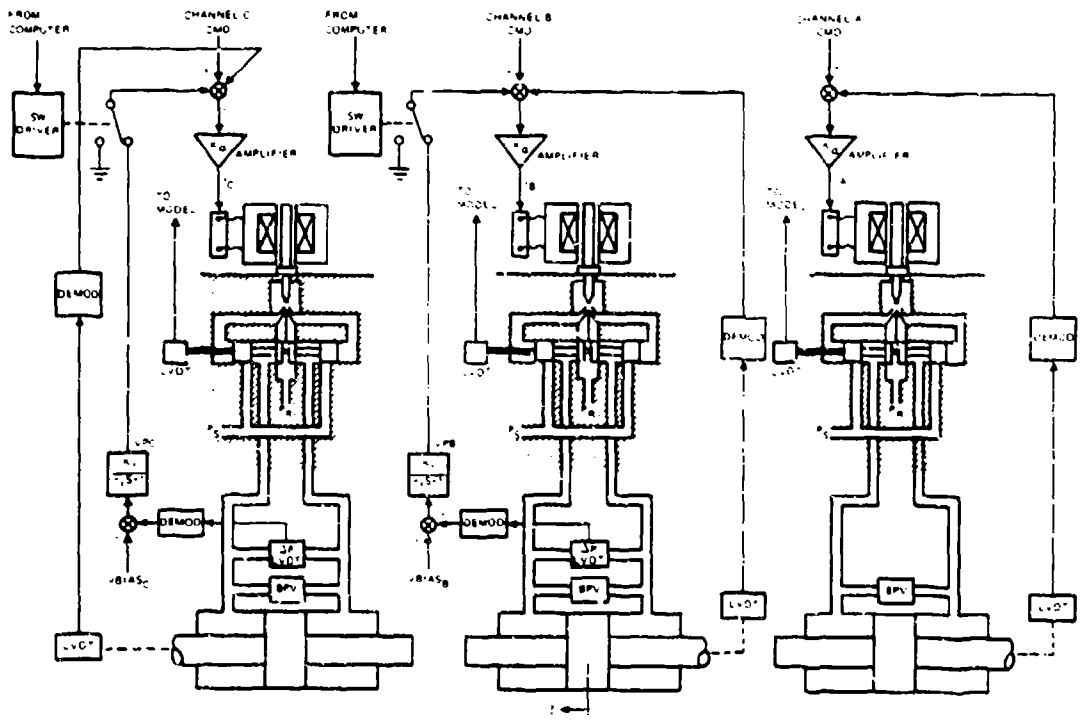

Figure 4. Active On-Line System

on-line channels are characterized by introducing pressure feedback signals which are passed through a simple lag circuit and then subtracted from the error signal between the position command from the flight control processor and the ram position feedback. This results in a greatly reduced static pressure gain in the on-line channels, so that they carry very little of the static load, eliminating the force-fight problem. However, because of the simple lag, they share the load dynamically, and this reduces transients (in the event of a hardover channel failure) to a level comparable to that of a forcesharing configuration.

Should there be a failure in any channel, a bypass valve in that channel is opened, removing that channel from influence on the system. If the failed channel is the active channel, the pressure feedback on one of the standby channels is eliminated, making that channel active. In the event of a second channel failure, the above sequence is repeated. Again, if the failed channel is the active channel, the pressure feedback on the remaining standby channel is eliminated, making it active.

Because it is very inefficient powerwise, the output of the active-on-line ram described in this report would normally be used as input to the valving for a power ram to drive the control surfaces. However, for this analysis it was decided not to introduce the complexity of an additional power stage since it would be common to all the configurations and would, therefore, only dilute any comparisons between them. Thus, it is assumed that the active-on-line ram is of a size to drive the control surfaces directly.

Servo Processor Configurations - In the paragraphs above, the basic hydraulic active-on-line scheme was described, and it is carried through to all configurations. The servo processor relationships to the control processor and servo valve make up the difference in the study configurations.

Failure detection is totally in-line and is accomplished within each channel servo processor by dual monitors, each of which compares the position of the spool of the EHSV with the output of an electronic EHSV model. The same feedback signals (including pressure feedback in the on-line channels) are input to the EHSV and to the EHSV models of a given channel. The two monitors are used for redundancy: a detected failure with either monitor will fail the channel. Each monitor is driven by one of a control processor pair, so that the control processor pair is also monitored. There is a single self-monitored LVDT in each channel for ram position feedback and for pressure feedback in the on-line channels.

As will be seen in Configuration II, where a dual parallel data bus is employed, the feature of dual monitors in the servo processors also monitors the internal parallel bus system.

In Configuration III three serial buses communicate with three servo processors at each actuator location. This provides for high redundancy since the failure of a bus can only disable one channel of an actuator.

Configuration IV provides for the highest redundancy since it incorporates a voting plane where the input of all serial buses is fed to all servo processors. This concept goes beyond the ground rules for an active-on-line system, but is incorporated to demonstrate that reliability may be enhanced when servo processor reliability is decreased due to the unfavorable temperature environment of that configuration.

B. FUNCTIONAL DISTRIBUTION

The architectures of the actuation system configurations from baseline to Configuration V are marked by a trend to distributed systems. Technology developments which have made or will make this possible are the microprocessor, digital circuits, the serial data bus and, high temperature electronics.

The advantages of a distributed system architecture are attractive. By taking tasks out of the central computer and assigning them to their logically associated peripherals, the central computer's workload can be reduced. The central computer can now perform a system management role, with detail functions being performed by the distributed subsystems.

Advanced System Considerations - Current flight control systems have evolved into "centralized" system architectures. This is to say, that a single, central, flight control computer (even though redundancized) performs all of the computational tasks associated with the necessary sensors and actuators to control the aircraft.

Future aircraft of statically unstable airframe designs, and the operational need to perform more specialized maneuvers, will impose tighter structural limits and more complex control problems. Integration of flight controls with other systems, such as engine controls, will increase the management scope of the flight control computer's task.

The introduction of modern, high speed, digital computers has brought about greater computational power. However, if the "centralized" system approach is continued, the additional communication and computation requirements to achieve integration will drive the size, speed, and complexity of this centralized computer ever upward.

The Honeywell study and report on a "Multi-Microprocessor Flight Control System" reaches the conclusions that the most logical solution is to partition the system into its sensor processing, control

laws processing, and servo processing functions and to partition between these units along functional lines. With the advent of the microprocessor and its inherent advantages (small size and low cost), the distribution of tasks from a central flight control computer is not only quite achieveable but can also enhance overall system computational capacity.

Computational Load - Partitioning of systems was discussed above from the viewpoint of an overload of the control processor. Part of that overload has to do with the capacity of a computer to perform all the tasks required in the time available. Considering that problem in the present system examples shows that every unique servo processor function performed in the control processor must be performed 12 times. Real-time functions, such as loop closures, are very capacity limiting.

Simplification of Interfaces - A general guide to functional distribution is to simplify the data exchange between units. For example, if all functions of loop closure, failure detection, and redundancy management are performed in the 12 servo processors of each channel instead of in the control processor, the data exchange between control processor and servo processors could consist of:

- Position command
- Actuator/servo processor status to control processor

Any combination of loop closure, failure detection, or redundancy management functions, which are included in the program control of the flight control processor, will increase the data exchange. The magnitude of this effect differs between configurations and is discussed under Section III, "Serial Data Bus."

C. PHYSICAL DISTRIBUTION

Physical partitioning decisions are based on the effects and benefits of placing the servo processors in the avionics bay, at other strategic locations, or at each actuator itself (figure 5).

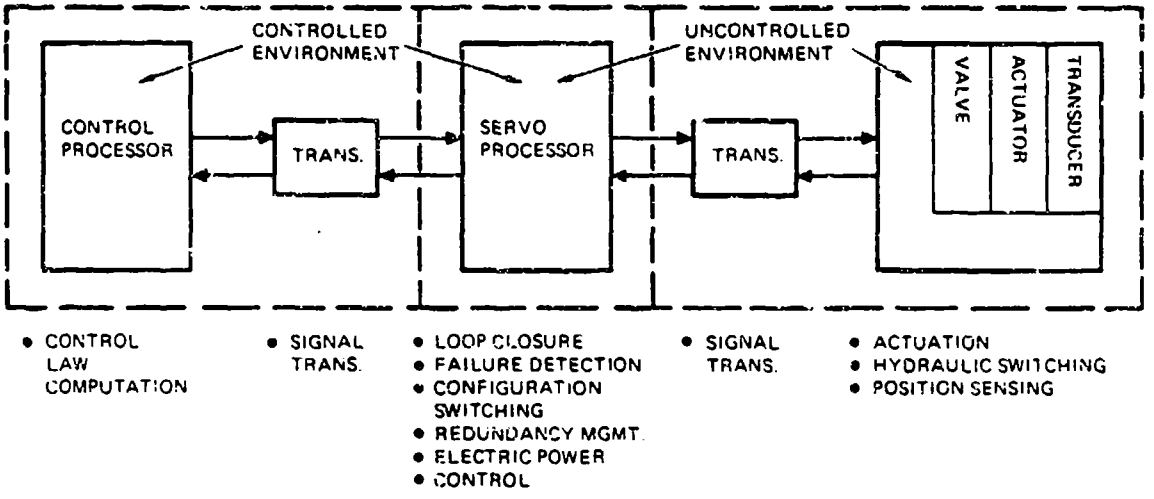

Figure 5. Physical Location Options

The serial data bus, introduced in Configuration II, can transfer data at a rapid rate with verification at the receiving end. This has led to the design and implementation of physically distributed systems, which, when complemented with "high-temperature electronics", will allow the servo processor to be incorporated with the actuator itself.

The following descriptions of Configurations I through III shows the equipment relationships between control processor, servo processor, and actuator, including the data bus variations involved.

Configuration I - This configuration is represented by figure 6. Details can be found in Section IV, figures 29, 30, and 31. It is significant to note that for each control processor channel there are as many analog servo processors as there are control surface actuators. Thus, for 12 control surfaces, there are 12 channel A servo processors. These 12 channel A servo processors are physically grouped together in the same enclosure with the channel A pair of control processors. The

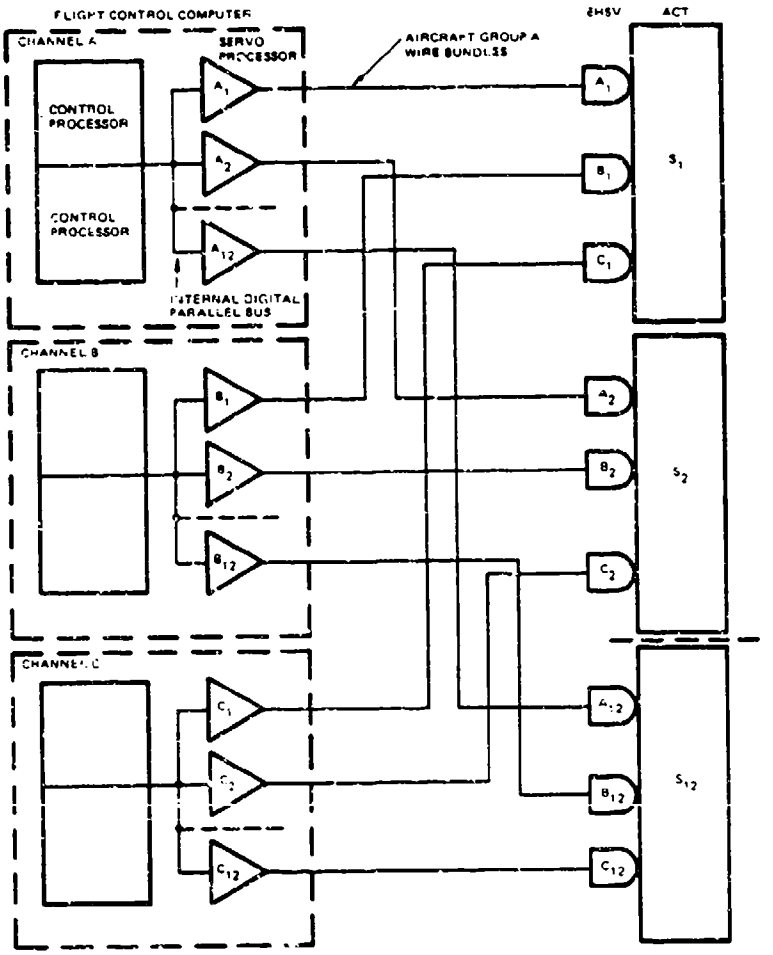

Figure 6. Configuration I Physical Locations

resulting three enclosures (channels A, B, and C) are physically dispersed within the avionics bay.

Since the servo processors are packaged with control processors in the same electronic enclosure and share the same power supply, the interwiring between them can be handled by two digital, parallel buses, both common to all 12 servo processors in the enclosure and implemented by means of mother board connections.

This interconnection density, however, approximates 10 per servo processor or 120/channel for an aircraft with 12 control surfaces. There are also a significant number of interconnect wires (49) between

each actuator complex and the computer complex. For an aircraft having 12 flight control surfaces, this represents 588 interconnections of aircraft group A wiring.

Configuration II - This configuration is representative of a physically distributed system. In Configuration II (figure 7) the servo processors are grouped by channel designator A, B, or C. This results in three enclosures each containing twelve servo processors located in one or more separate temperature-controlled bays.

Each servo processor enclosure has its own power supply which is common to all servo processors within the enclosure.

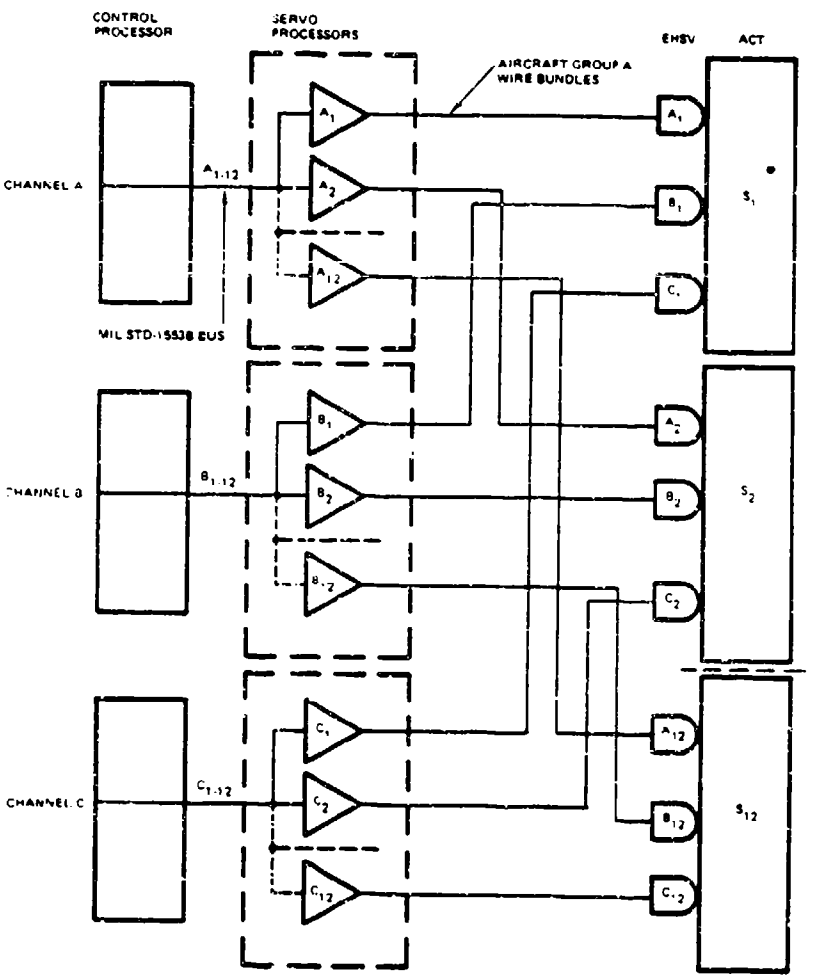

Figure 7. Configuration II Physical Locations

The control processor/servo processor link is now a serial bus between control processor-servo enclosures. Parallel bus data distribution is used within servo processor enclosures, similar to Configuration I. Connections from servo processors to actuator (group A - 588 wires) are the same as in the baseline and Configuration I, although shorter due to the servo processor locations.

Configuration III - Figure 8 shows a physical layout for Configuration III. The servo processors are now located at the actuator itself. It should also be noted that contrary to Configurations I and II, where the servo processors were collected in three groups of 12, they are now collected in 12 groups of three.

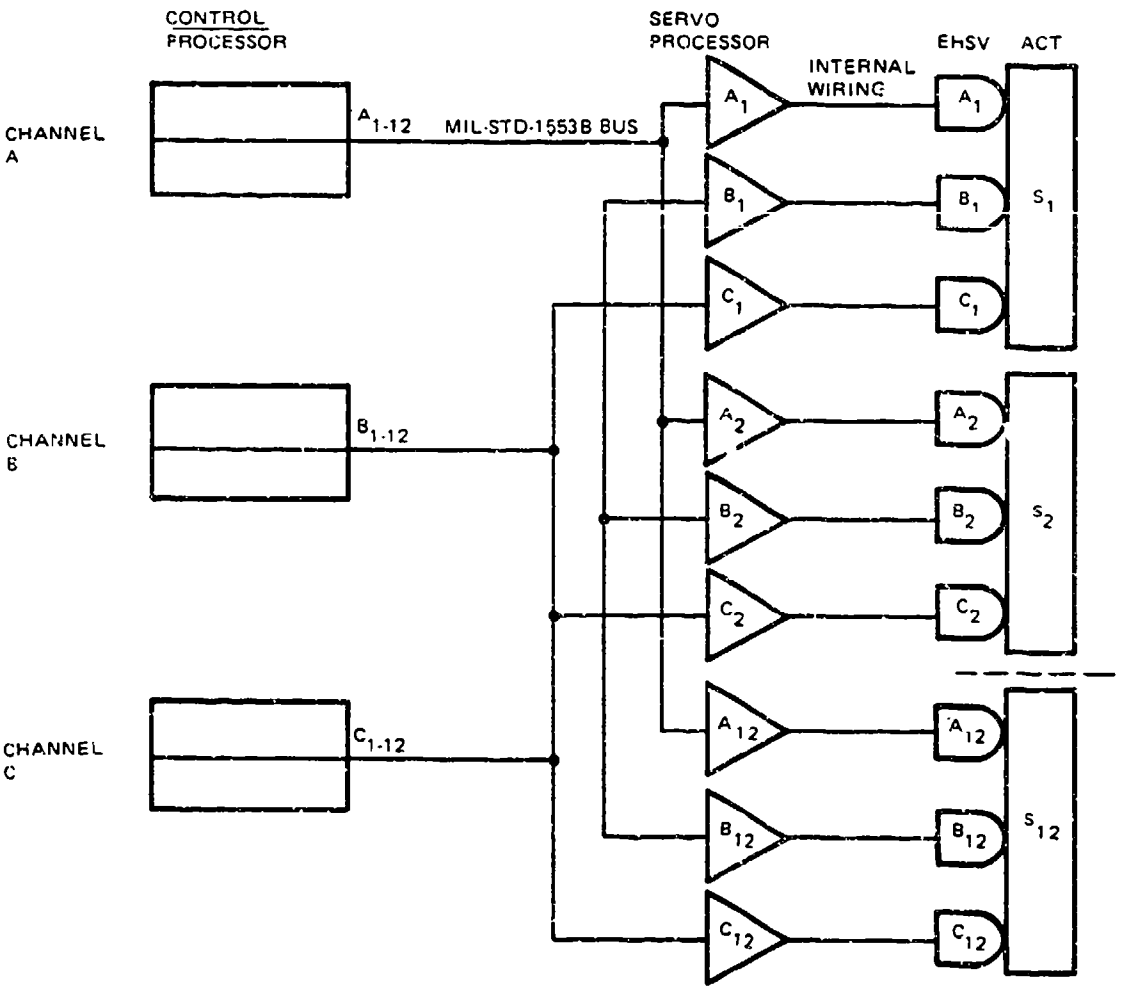

Figure 8. Configuration III Physical Locations

Each servo processor has its own dedicated power supply and monitors. The actuator/servo processor multiwire interface is now very short. The control processor/servo processor serial bus is now distributed to all actuator locations. All data exchanged between each servo processor and its control processor is via a serial digital bus. Each servo processor has its own reconfiguration logic, and its fail status is exchanged by means of dedicated wires between the servo processors serving a particular actuator.

D. SERIAL DATA BUS - FORMAT, PROTOCOL, AND APPLICATION

The following analyses will evaluate the applicability of the MIL-STD-1553B bus to a control processor-servo processor interface. MIL-STD-1553B is the standard for serial data transmission.

Under MIL-STD-1553B specifications, there must be a bus controller. There are two choices:

- Each control processor could be a bus controller. This would have an undesirable effect on the control processor's ability to accomplish its main function.
- An autonomous bus controller could be utilized that treats both the control processor pair and each servo processor as a remote terminal.

Trade-offs will be the effect on redundancy management and on the time required to process the bus traffic. For the purposes of this study, the second option is assumed. However, the bus controller is physically integrated with the control processor.

Dedicated Bus Interface - If all control processor commands were transmitted on the same bus, any bus failure would totally disable the actuator - an unacceptable single-point failure. Each servo processor channel of an actuator must interface with a different control processor on a physically different serial bus. With three physically different serial buses, the failure of any one bus disables only one channel of the actuators.

Remote Location Environments - The servo processor of Configuration III will be remotely mounted in locations where space is limited. This will require special high temperature components and the use of hybrid microelectronic packaging techniques. Presently available MIL-STD-1553B transmitter-receivers, when implemented with hybrid technology and screened to MIL-STD-883B, are prohibitive in size and have costs approaching $1000 per bus interface unit.

In considering the type of bus for flight control actuation standardization, a trade-off should be made between hardware requirements and bus protocol. That, along with the integration of the terminal with the servo processor, should provide a smaller overall, lower-cost product.

MIL-STD-1553B Protocol - Figure 9 represents the protocol for this data bus.

Data transfer between terminals is directed by a bus controller. Transfer is initiated by two commands which select sending and receiving terminals. The receive and transmit commands include the addresses of the terminal to receive the transmission and that of the terminal which will transmit. The status words (from each) are used to verify the action being performed.

MIL-STD-1553B Format Overhead - Calculated below is the overhead for each transmission based on figure 9. The equivalent of 5.4 words must be sent with each transmission on the bus to define which elements will transmit and receive and to verify the transmission of the data.

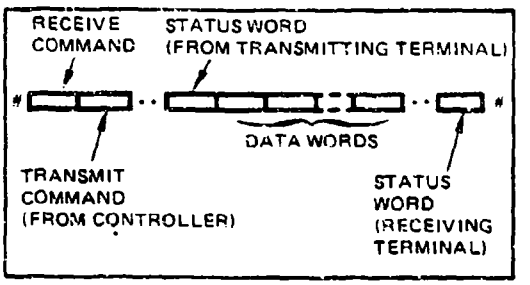

Figure 9. Remote Terminal-to-Remote Terminal Transfer

Format Overhead for One Data Transmission	Words	Time μsec
Bus Controller (BC) issues receive command	1.0	20
Bus Controller issues transmit command	1.0	20
Maximum delay	0.6	12
Transmitting terminal issues status to BC	1.0	20
Maximum delay after data transmission (**)	0.6	12
Receive terminal sends status to BC	1.0	20
Delay before next transmission cycle (#)	0.2	4
Total nondata time in each transmission	5.4	108

When a significant number of data words are sent with each transmission, the 5.4 data word "overhead" is not critical. However, when the number of data words are less than five words per transmission, more time is spent for overhead than is required to transmit the data.

Maximum Data Exchange - The maximum number of words that can be exchanged in a typical flight actuation application is shown below:

Assumptions: 12 actuator channels
100 Hz update rate each channel
(10,000 sec. period)
2 transmissions per channel update:
1 from control processor
1 from servo processors

Assuming a design limit of 70% bus utilization, the time for each channel update is: 10,000 x 70%/12 = 583.3 sec.
Overhead for 2 transmissions: (108 x 2) = -216 sec.
Time available for data words: 367.3 sec.
Time for 1 data word: 20 sec.
Total words exchanged in 1 update: 18.36 words

This shows that if two transmissions were required per channel update a maximum of 18 data words (total) could be exchanged. If three transmissions were required per channel update, the total allowable data words that could be exchanged in all three transmissions would be reduced to twelve.

MIL-STD-1553B Capability - We have specified the sample data rate of the control processor to be 100 Hz (10,000 μsecond period). The 1553B format has a maximum allowance of 32 data words per transmission. The number of transmissions possible is then based on the overhead plus the data words. We have previously developed the overhead for one data transmission (in either direction), and from MIL-STD-1553B we know the length of one word.

	Words	Time (μsec)
Period (100 Hz)		10,000
Overhead	5.4	108
Data Words	1	20

The percent usage of the bus (which should not exceed 70%) can be calculated as follows:

% Bus Utilization

$$= \left(\frac{\text{overhead time + data word time}}{\text{time allotted}}\right) \times 100$$

$$= \frac{(\text{transmissions} \times 108\ \mu\text{sec}) + (\text{data words} \times 20\ \mu\text{sec})}{10{,}000\ \mu\text{sec}} \times 100 \quad (1)$$

We can now evaluate configurations II, III and IV to determine the factors which dictate the number of data words required and the number of transmissions required per sample data period.

Configuration II Serial Data Bus - In this configuration (figure 10) the 12 servo processors for a given channel are housed together in a separate compartment remote from that of the control processor. When the control processor and servo processor are in separate enclosures, bus timing, connector size, and least number of interface wires all favor using a serial bus as the data link.

The serial data from the control processor pair is translated to a parallel format within the enclosure for distribution to each servo processor. The addition of th parallel bus and control logic makes it possible to utilize only one serial-parallel translation circuit for all servo processors. Weight, cost, and system complexity favor this approach.

Configuration II - Bus Utilization - Transmissions per sample data period required for Configuration II, assuming that redundancy management and loop closure are performed in the servo processor, are as follows:

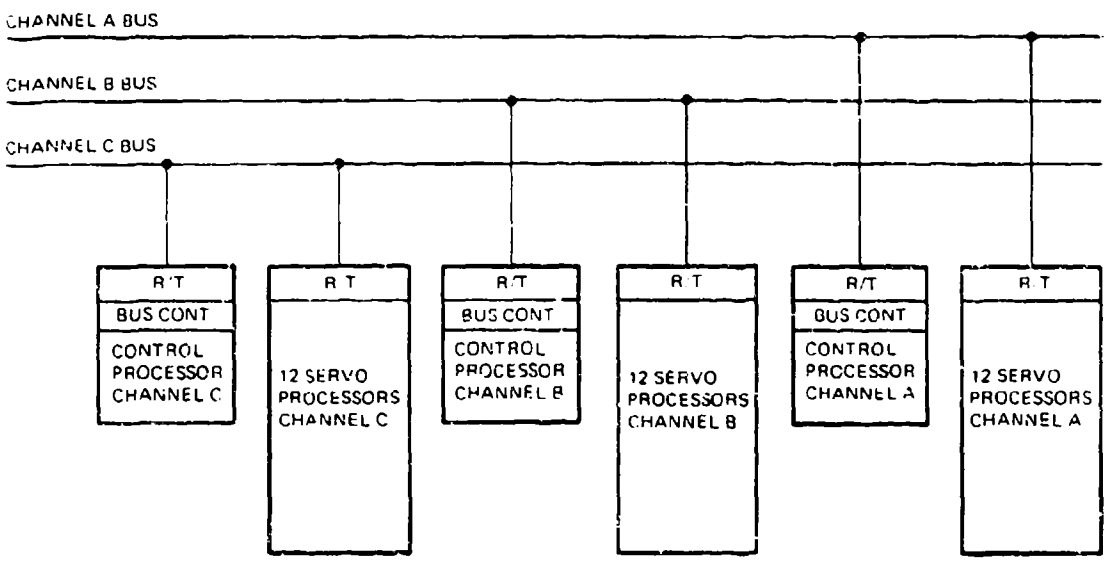

Figure 10. Configuration II Serial Data Bus

Transmissions	Data Words
1 (CP → SP) of:	1 - CP fail-status
	12 - position commands
1 (SP → CP) of:	2 - SP fail status
2	15

Using equation (1) shows:

$$\%\text{Bus Utilization} = \frac{(2\text{x}108)+(15\text{x}20)}{10{,}000} \text{ x } 100 = 5\%$$

Since only one update cycle is required, the bus has almost 14 times the capacity required (70% being the upper limit).

A calculation was made to evaluate the data bus load if a function, such as redundancy management, were performed in the control processor instead of in the servo processor. This would require sending all required data to the control processor.

Since a given transmission is limited to 32 words, the redundancy management data words are split up into four separate transmissions.

Transmissions	Data Words
1 (CP → SP) of:	1 - CP fail-status
	12 - position commands
4 (SP → CP) of:	32 - (4x8) redundancy mgmt. inputs
5	13 + (32x4) = 141

Using equation (1) shows:

$$\%\text{Bus Utilization} = \frac{(5\text{x}108) + (141\text{x}20)}{10{,}000} \text{ x } 100 = 34\%$$

This calculation shows that the data bus would accommodate this data traffic. However, this illustration bears out the benefits of proper functional distribution as discussed under "Functional Partitioning" since the data bus utilization increased from 5% to 34%.

Configuration III Serial Data Bus - In Configuration III the servo processors are grouped at the actuator, with each of the three units representing a different control processor channel (figure 11).

For reference, figure 36 in Section IV, is the block diagram of the serial bus interface which is resident in each servo processor. The serial bus is bidirectional. The "fail status" of both sides of the servo processor are transmitted back to the control processor. This interface differs from Configuration II in that each servo processor must have a dedicated bus interface. The functions of the bus interface have now been slightly reduced. The "word decode and control" function now has only the input for one control processor to control, rather than all servo processors of the same channel.

With Configuration III the economy of common bus transceivers and power supplies has been lost. However, the possibility of some single point failures that can disable one third of all the actuator channels, has also been eliminated.

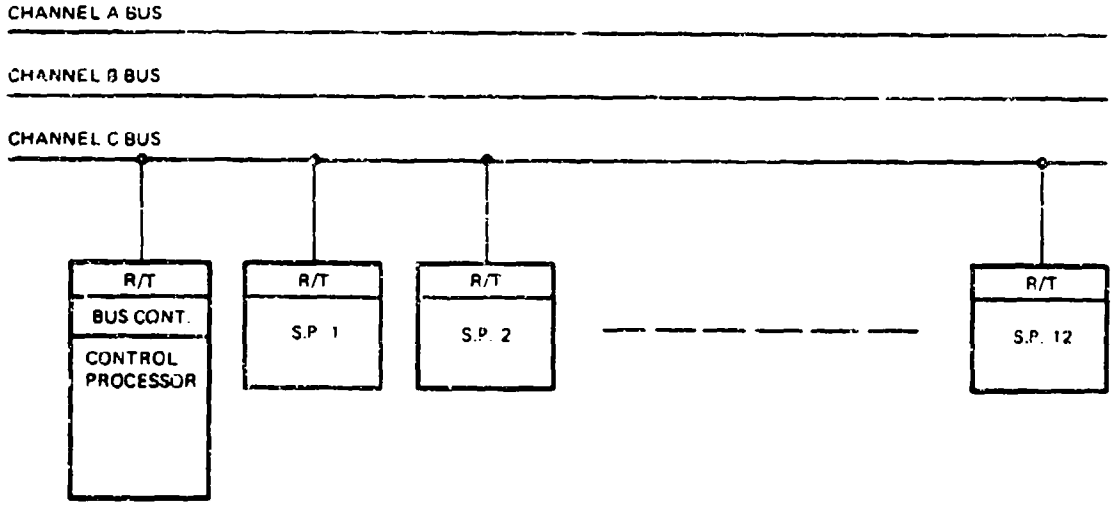

Figure 11. Configuration III Serial Data Bus

Configuration III Bus Utilization - Transmissions per sample data period, assuming that redundancy management and loop closure are performed in the servo processors, are as follows:

Transmissions	Data Words
12 (CP → SP) of:	1 - CP fail status
	1 - position command
12 (SP → CP) of:	1 - SP fail status
24	3 x 12 = 36

However, there are now 12 servo processors to be dealt with separately, calling for 24 transmissions per sample data period.

Using equation (1) shows:

$$\%\text{Bus Utilization} = \frac{(24\text{x}108) + (36\text{x}20)}{10{,}000} \text{ x } 100 = 33\%$$

If it were now intended to perform redundancy management in the control processor:

Transmissions	Data Words
12 (CP SP) of:	1 - CP fail status
	1 - position command
12 (SP CP) of:	1 - SP fail status
	8 - redundancy mgmt inputs
24	11 x 12 = 132

Using equation (1) shows:

$$\%\text{Bus Utilization} = \frac{(24\text{x}108) + (132\text{x}20)}{10{,}000} \text{ x } 100 = 52\%$$

The bus can handle this traffic. This example illustrates the strong effect of the overhead protocol of the MIL-STD-1553B bus capacity

when a high number of transmissions are required, since adding the redundancy management data words had less effect than in Configuration II.

Configuration IV Serial Data Bus - This configuration was introduced to show how a voting plane in servo processors, located at the actuator, could improve reliability, if necessary. It involves implementation with dual microprocessors in the servo units.

In Configuration IV, commands from each control processor are routed by data bus to all servo processors (figure 12). Thus, each control processor talks to 36 servo processors. It would not be feasible to carry that traffic without using the "broadcast mode" of the MIL-STD-1553B bus protocol. In this mode, the CP controller issues a receive command to a specific address, "31", followed by the necessary data words. Terminals (servo processors) are equipped to recognize the broadcast command and, therefore, receive that particular data. No status commands are issued.

Configuration IV Bus Utilization - Transmissions per sample data period for one bus are as follows:

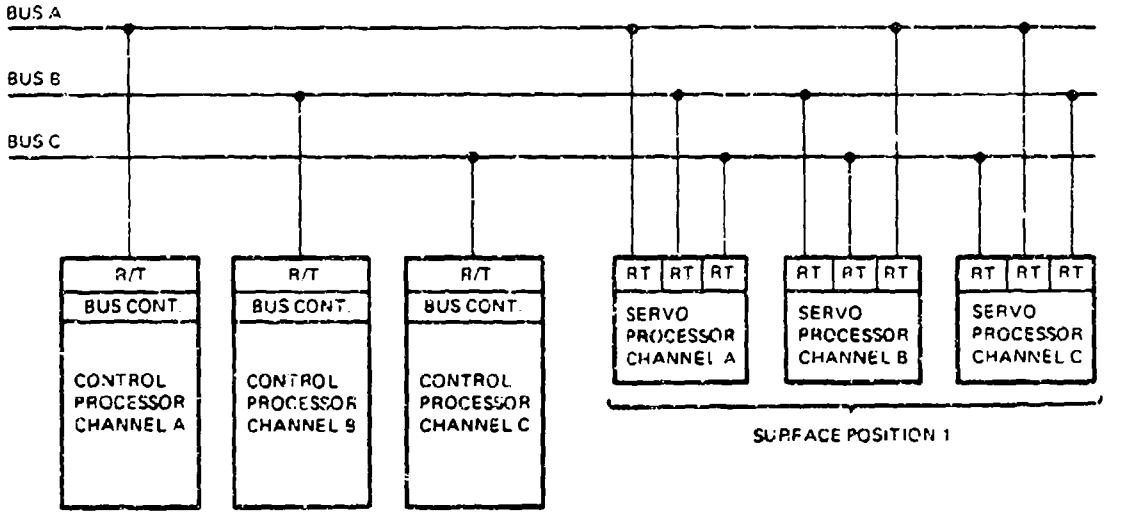

Figure 12. Configuration IV Serial Data Bus

Transmission	Data Words
12 (CP broadcast to each surface's SP's)	1 - reset 1 - position command 1 - CP fail status
12 (SP "A" broadcast to CP-A and to all SP's)	1 - SP"A" fail status
12 (SP"C" broadcast to all SP's)	1 - SP"B" fail status
12 (SP"C" broadcast to CP-C and to all SP's)	1 - SP"C" fail status
48	(6 x 12) = 72

Using equation (1):

$$\%\text{Bus Utilization} = \frac{(48 \times 108) + (72 \times 20)}{10{,}000} \times 100 = 66\%$$

This shows that the bus has the capacity. However, it should be noted that this is only possible because the "broadcast" mode of MIL-STD-1553B is employed. What is sacrificed is the verification that transmissions have been received.

There was no need to consider redundancy management at the control processor in view of the use of microprocessors in the servo processors.

E. HIGH TEMPERATURE ELECTRONICS

The Environment - Configuration III has physically distributed the servo processor to be integrated with the actuator. This poses a problem of obtaining electronic components which can withstand that temperature environment.

Conceivably, a controlled environment for the servo processor could be created at the actuator. This would require a heat-exchange system at each actuator location. From an overall aircraft design viewpoint, this would be undesirable, adding weight and complexity as well as accessibility problems for maintenance. The more attractive alternative is to develop electronics capable of surviving the uncontrolled environment. The packaging technology for a servo processor which can withstand the vibration, shock, altitude, and contaminants (sand/dust/-oil) of such an uncontrolled environment is available today. The major environmental problem is temperature.

One source of heat is the valve-actuator hydraulic fluid, which is heated as work is performed on it. The valve-actuator body itself may experience temperatures from -65°F (-54°C) to + 275°F (+135°C) in a type II hydraulic system. Another source of heat comes from aerodynamic heating of stagnant compartment air as a function of aircraft speed. These temperatures have been quoted (for fighter aircraft) as between 10°C to 71°C for cruise conditions, 132°C maximum for a 10 minute dash, and 168°C maximum for a 2 minute dash (figure 13). A similar source, depending upon the installation, could be heat radiated from nearby engines.

Heat generated by the electronics itself is a third source, and this can be affected by the circuit design approach employed.

Even under these conditions of temperature, it can be shown that with the development of three technologies, reliability can be comparable with present equipments which are housed in conditioned environments.

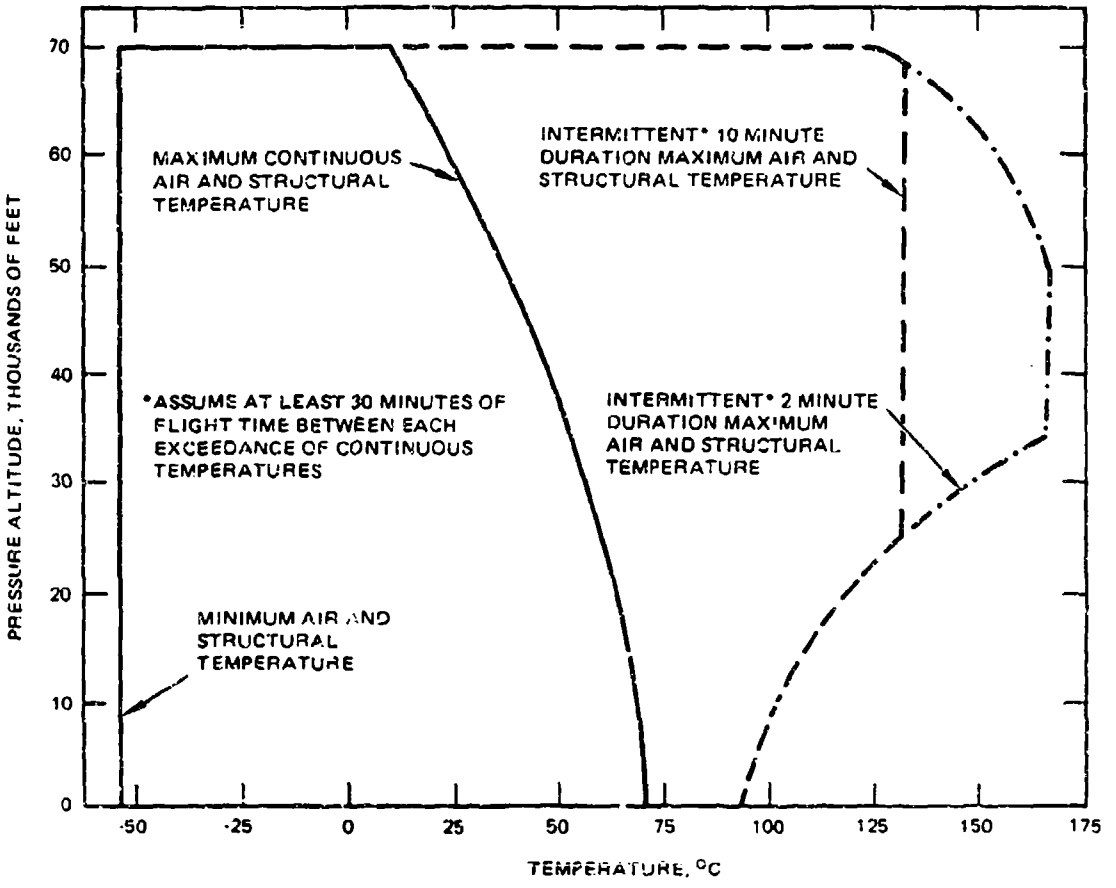

Figure 13. Temperature-Altitude Requirements for Supersonic Aircraft

These technologies are:

a. High-temperature electronic component technology.

b. Thermal packaging technology.

c. Switching circuit design technology.

Semiconductor Development Status - Research and development in high temperature components and in high temperature packaging techniques has progressed significantly since work was started in the 1960's by NASA for application to spacecraft. This work tapered off as better cooling systems were developed. It was revived in the 1973-74 time period for well-logging instrumentation during the energy crisis. This application was able to live with short-term reliability of 400 hours, thus no long-term reliability testing was required.

Research into semiconductor components involving high temperatures is on-going at several companies and government organizations. These activities can be grouped into the following categories:

a. Those being developed for relatively short-term reliability as for geothermal and oil drilling applications.

b. High-temperature testing to accelerate failures which would occur at normal temperatures, as is done by Bell Telephone Laboratories and others.

c. Those which are being conducted under government sponsorship, such as the NAVAIR/NRL/GE program for application to engine controls.

The discussion following will concentrate on the work being done under the NAVAIR/NRL contract to General Electric since that program is concentrating on the level of reliability pertinent to flight control. A discussion of efforts in other companies is included to show extensiveness of the work in the industry.

NAVAIR/NRL/General Electric Program - The General Electric Company's Electronic Laboratory in Syracuse, New York, is under contract to the Naval Research Laboratory, Code 6810, (Contract N00173-79-C-0010) for the development of high-temperature electronics to be used for engine control applications. The program is under the sponsorship of the Naval Air Systems Command. The purpose of the program is to develop a family of electronic components which can operate at 300^{o}C for 10,000 hours. This translates to more than 320,000 hours at 200^{o}C, a probable top specification for flight control.

These components are intended for engine controls mounted on an engine in an uncontrolled, high-temperature environment. This presents the same technical problem as mounting electronics at or on a flight-control actuator. The functional requirements of the circuitry are also similar to the flight-control application.

The desire to place the control electronics on the engine is based on the following:

a. Remotely located controls generally require long wire runs which result in unacceptable high vulnerability and low reliability of the control system.

b. Engine controls mounted on each engine assure that a single failure affecting only one of the engine controls will not propagate to other engines.

In the first phase of the program, G.E. Syracuse concluded that Integrated Injection Logic (I^2L) was the best technology available for this application. I^2L is a bipolar, large-scale integration circuit technology shown to be capable of operation at 300°C. The results of G.E.'s testing has shown that the major reliability problem is the metallization migration into the semiconductor material at elevated temperatures. A double metallization layer is needed for digital applications at 300°C operation, and the system chosen is platinum silicide/titanium-tungsten/gold. Platinum silicide forms stable ohmic contacts to silicon, and gold interfaces easily with the outside world. A thick layer of titanium-tungsten is needed to separate those materials.

Latter phases of the program call for the design, development, and testing of a family of products, including a microprocessor, read-only-memory (ROM), random-access-memory (RAM) and possibly, a digital-to-analog converter. G.E. is predicting availability of these components, operating at 300°C, in the 1985-86 time frame and almost immediate availability at 200°C.

Other High Temperature Electronics - Other developments in high-temperature electronics are underway in government and commercial circles - mostly for the geothermal and well-logging industry. Sandia Laboratories, Harris Semiconductor, Burr-Brown, and Teledyne Microelectronics all report activities for this application. NASA-Lewis has announced success in growing cubic silicon carbine (SIC) single crystal wafers - which portends to be the breakthrough for obtaining this

technology. SIC has been a prime candidate for many years for use in high-temperature electronic applications.

Electronic Packaging for High Temperature - Some research in packaging technology was done in the 1978-79 period by HR Textron Inc. using existing components. Hybrid techniques were employed wherein semiconductor chips were attached to the package substrate with eutectics, reducing the thermal path impedance between the microcircuit package and the semiconductor junction from approximately $90^{o}C$/watt to 10^{o}/watt. This work has also been done by the G.E. Company at their Evendale Engine Division in applications related to the FADEC engine control program.

Circuit Design Approach - The use of switching techniques in a circuit design reduces the internal power dissipation of the semiconductor devices employed. Acting as saturated switches, these devices operate predominately in one of two modes: saturation and cutoff. The devices operate for only small periods of time (switching transition) in the active region. It is operation in the active region which generates the most significant junction self-heating. A design approach to maximize the use of switching techniques will generate less junction self-heating than its linear circuit counterpart.

The significance of reducing internal power dissipation and self-generated junction heating is to increase the ambient temperature which can be tolerated.

Driving a conventional electrohydraulic servovalve with switching circuits (i.e., pulse-width modulation) is not a new concept. Expanding this design approach to include feedback transducer signal processing and command/feedback summation (loop closure), offers a circuit design approach for servoactuation control with potentially higher thermal environment tolerance than conventional linear concepts. Some work has been done by HR Textron Inc. in this area, with good results.

General Electric's Aircraft Engine Group has reported using a linear, variable phase transducer (LVPT) in their system design as a feedback sensor. This device can measure linear displacement by exciting two primary coils, measuring the phase difference at the output of the secondary by "OR-ing" the output with the phase clock, and counting the resultant pulses. The resulting system is digital circuitry-intensive which will be compatible with I^2L components.

F. DIGITAL SERVO ACTUATION ELEMENTS

The digital servo actuation elements to be discussed include the servovalve, the actuator, and the position/pressure feedback devices.

1. Digital Servovalves - The digital servovalve candidates selected for discussion are:

- parallel-binary servovalve
- pulse-width-modulation-driven, conventional EHSV
- stepper-motor-driven servovalve

Parallel Binary Servovalve - The parallel binary servovalve-driven actuator is discussed in Configuration V in Section IV. The servovalve in this configuration is a parallel wire, binary servovalve (figure 14) which was designed, built, and tested under United States Air Force contract AF33(657)-8644. This valve had an 8 bit (8 coils) torque motor. While there is no technical reason for this servovalve not to match the performance of a linear servovalve, its complication in manufacturing and the multiplicity of wires to drive it do not recommend it.

Pulse-Width Modulation Standard Linear Servovalve - A preferable approach is to use pulse-width modulation (PWM) techniques with a conventional analog electrohydraulic servovalve (EHSV).

This concept allows a "digital" type of transmission to the EHSV. The driver could be a voltage driver or a current driver. The shortcoming of a voltage driver is that as the EHSV coil impedance changes with temperature, the resultant coil current will change. This appears as an effective forward path gain change in the loop closure path of the servoactuator. Corrections to this can be made by current sensing or temperature sensing.

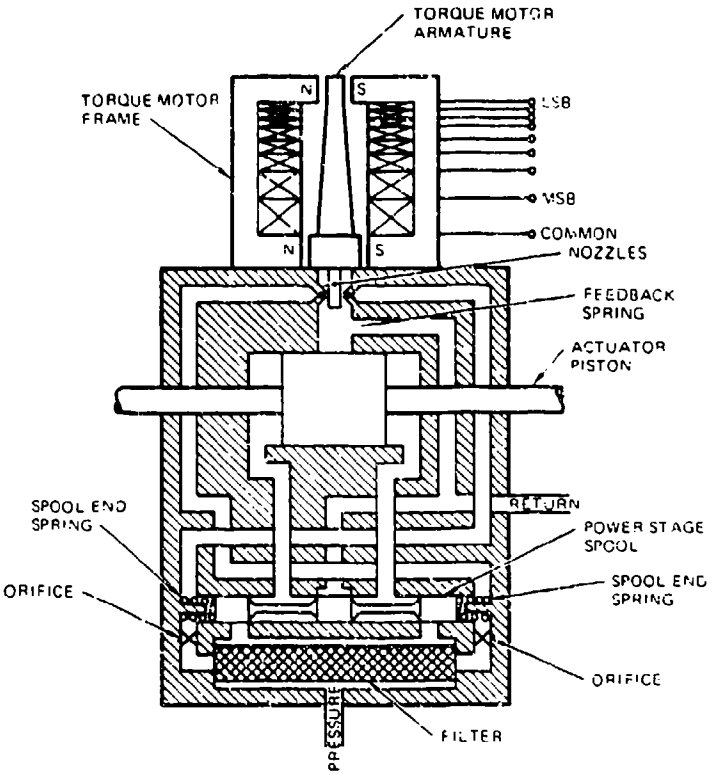

Figure 14. Parallel Binary Servo Actuator, Multicoil Torque Motor Schematic

Pulse-width modulation fundamental frequencies can be set high enough with respect to EHSV armature natural frequencies to eliminate armature or suspension fatigue. The problem inherent with this approach is limiting the length of the wiring loop between the servo processor and the valve, since the varying current can be a source of electromagnetic interference (EMI). However, this approach is ideal for a configuration which locates the servo processor at the actuator.

A variation in Configuration III would be to use PWM switching techniques to drive the servovalve, and, in addition, to use digital switching techniques to excite and demodulate the transducers (LVDT's). This technique is compatible with the high-temperature electronics described in Section III and is the configuration recommended for further development.

Stepper-Motor-Driven Servovalve - A stepper motor could be used to drive a servo valve spool. Stepper motors accept a continuous control pulse train and increment a predetermined amount of rotation for each control pulse and, therefore, could be applied to an actuation device. It easily converts digital information to exact incremental rotation, and there is no need for any feedback device such as a tachometer (rate) or an encoder (position). If the system is driven open loop, the problems of feedback loop phase shift and resultant instability common to servo drivers are eliminated.

Proper application of a stepper motor requires a consideration of:

- Distance to be traversed.
- Maximum time allowed for the travel.
- Desired static (detent) accuracy.,
- Desired dynamic accuracy to return to static accuracy (settling time).
- Required step resolution (combination of step size and gearing to the load).
- Total system friction, system inertia, and the speed/torque characteristics of the stepper motor.

A stepper motor accelerates and decelerates with each control pulse even when it is rotating at a maximum speed which causes a velocity change on its output shaft rotation at all operating speeds. Thus a stepper motor would be unsuitable for constant velocity application.

Stepper motors are extremely sensitive to power supply voltages and internal motor heating caused by continuous operation at high speeds. These conditions can be improved by series and suppression resistances that limit steady-state current to motor windings and control the damping effects of the suppression diodes connected across the motor windings.

Calculation and/or measurement of inertial or friction loads connected to the motor is necessary since in an open loop stepper motor system, the motor does not "know" if excessive inertial or friction has caused the motor to gain or lose one or more steps. If any steps are randomly lost or gained, the positional accuracy is lost. However, a minor loop may be closed around the stepper motor with an encoder for system performance enhancement. The most significant improvement from such an arrangement would be in the positional accuracy. The motor would now "know" that it has reached a commanded position.

A stepper motor must be coupled to the load by some means which does not contribute backlash in excess of that necessary to meet system specifications. Timing belts and precision lead screws fit this description.

Open motor enclosure may eject flame in the event of an insulation or component failure. Totally enclosed motors will prevent such flame hazards but make the cooling of the motor extremely difficult.

2. Digital Actuator - For purposes of this study, a digital actuator is defined as one in which the electrical signal input to the valving is a digital actuator position command rather than an actuator rate command. Measuring the actuator position is, therefore, unnecessary. It may be desirable to monitor the ram position for failure detection and/or for initializing its position.

Within the above definition two basic concepts are evident. In concept 1, the valving element is the digital-to-analog converter. The valving element has a mechanical summing point for the digital command and the actuator position, with the difference, or error signal, determining valve opening (actuator rate). For this concept, the actuator and mechanical feedback are analog, but with the valving element as a summing point the combination satisfies the above digital actuator definition.

In concept 2, the actuator is constructed from a number of series-connected pistons with binary related strokes. For this concept, each piston has its own valving.

Concept 1 - Two approaches that satisfy concept 1 will be described briefly. The first approach involves using a servovalve with binary digital or with pulse-width-modulated (PWM) input to the torque motor coils and with mechanical feedback (torque) to the torque motor armature (see figure 15). The binary digital servovalve could, for example, have multiple coils on a single armature with a binary relationship between the number of turns in the various coils. The PWM approach has considerable advantage and would be a logical choice between the two. Note that the problem of actuator null shift inherent in using the torque motor as a summing point for mechanical feedback has not been avoided by this approach.

This concept has the servovalve as its D/A conversion element and the mechanical loop closure is analog. Since this type incorporates mechanical feedback, a whole new group of considerations different from

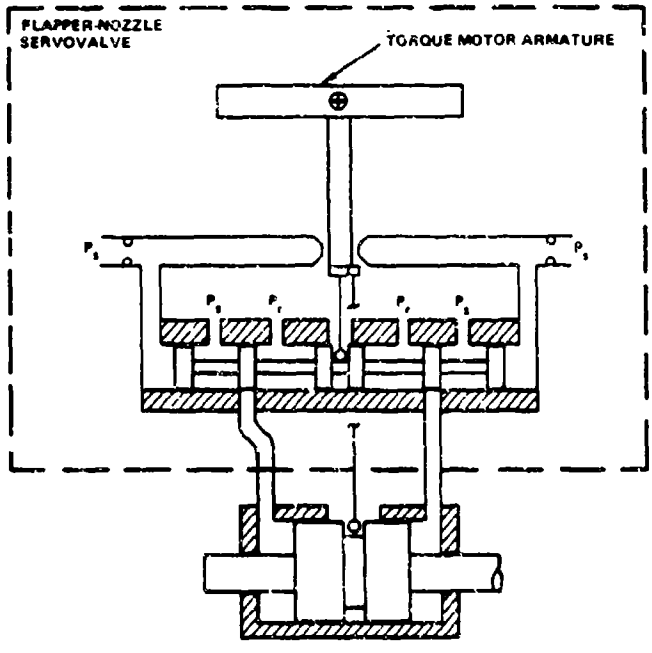

Figure 15. Binary Digital Servovalve

those in the baseline configuration are introduced. It would, therefore, be very difficult to make valid comparisons. This is not to say that mechanical feedback does not have merit in some applications.

The second approach to concept 1 is one in which a stepper motor produces a stepped input that is summed with a rotation proportional to actuator displacement by means of a mechanical differential. The output of the differential displaces a valve spool that controls flow to the actuator (see figure 16). In this figure the spline and screw work together to form a differential. This approach has the disadvantage of requiring initialization with some type of position sensor since the output does not have an address. In fact, it may require periodic or continual position updating because of the possibility of lost steps.

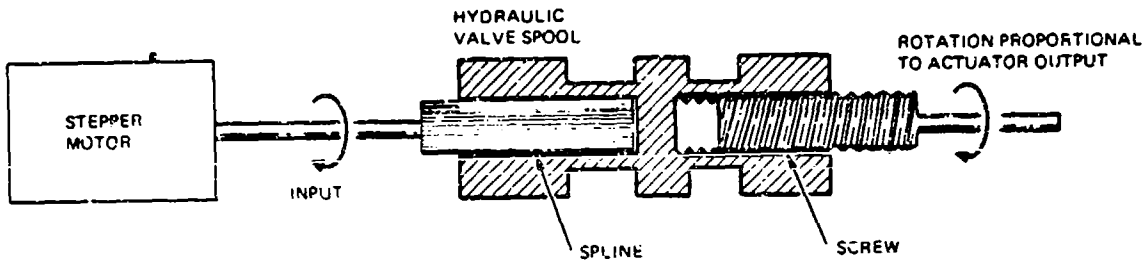

Figure 16. Stepper Motor Input

Concept 2 - Concept 2 consists of a series of actuator pistons connected end to end and having a binary relation between strokes of the different pistons (see figure 17). The stroke of the shortest piston is equal to the resolution required, and the total output is twice the

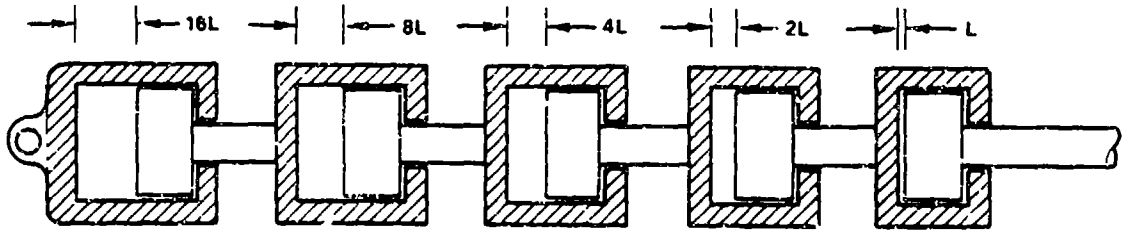

Figure 17. Digital Actuator

stroke of the longest piston minus the stroke of the shortest piston. Thus, five pistons stacked in series give resolution of 3.2% of total stroke. Separate on-off valving is required for each piston. If back and forth hunting is to be avoided upon the introduction of commands that require extending the long-stroke piston and retracting several of the shorter stroke pistons, the valve flows must be carefully controlled to assure equal traverse time of all pistons under all pressures, at all operating loads, and in both directions. This is not an easy task and could dictate substantial overdesign in load-carrying capability to negate the effect of load. The electrical command is parallel binary, and since digital signals will almost surely be sent to the location of the actuator as serial information (because of the number of wires required for paralleled transmission), actuator mounted electronics to do the conversion would be a near necessity. Note also that there are a large number of sliding seals. This basic type is inherently very heavy and complex mechanically, which alone would remove it from contention for most, if not all, aerospace applications. A positive feature is the elimination of many sources of null drift. This approach exemplifies the difficulties incurred from mechanical digital-to analog conversion at high power levels.

3. Digital Transducer - A study of existing "digital" transducers to provide position and pressure feedback has indicated that the mechanisms are based on optics, with pattern-reading principles applied to translate linear motion to digital electronic signals.

The optical/digital transducers rely on their mechanical alignment, but also on their true mechanical movement linearly. Some, because the digital scale is not referenced to zero, require initialization. The optical connectors and optical system used require space and alignment which to date has not yielded the same degree of compactness as existing devices.

The present position transducer (LVDT) relies on the accuracy of coil winding and the mechanical precision of the armature to the stator. It's scale factor can be compensated for by means of the

electronics which excites and demodulates it, as long as its mechanics are linear throughout. It can be made small for servo valve spool monitoring, or large to monitor long actuator strokes. It can withstand the actuator environment.

Perhaps the biggest deficiency of the present LVDT is in the number of interconnections between it and its excitation and demodulating electronics in the servo processor, and the wire weight required when the servo processor is located in the avionics bay. This objection can be ameliorated when the servo processor is located at the actuator. In addition, digital excitation and demodulation techniques have been developed to effectively "digitize" the existing LVDT devices.

G. DIGITAL CONTROL PROCESSOR SAMPLING RATE

A design issue, first observed in Configuration I, was the effect of the waveform emanating from the digital control processor on the electrohydraulic servovalve. As this discussion will show, these effects were countered by the use of notch filter tuned to the sampling frequency. However, the notch filter introduced a gain change and phase lag which were a strong function of the sampling rate selected.

In any configuration where a digital control processor feeds digital commands to an analog servo processor, the signal will be of a staircase waveform, with steps at the command sampling rate of the computer. The rate selected for evaluation was 100 Hz (command update every 0.01 seconds). The effect of this waveform on the actuation device was evaluated using a ramp command.

Figure 18 shows the response of the second stage of the servovalve and the ram to a digitized ramp command. The command consists of a series of small amplitude steps.

These steps are so small that their effect on ram position is insignificant. However, the servovalve spool is almost constantly in motion at this frequency, and such a condition may cause undue wear and fatigue of the servovalve spool and of the hydraulic lines, producing premature failure. However, tests of a pulse-width modulation drive on a direct-drive actuator, a system with similar oscillation-producing effects on the valve spool, produced no variations in wear of the spool bands from that of a sine-wave driven spool at the same frequency over a 300-hour life test. This latter was reported by Dynamic Controls Inc. in connection with Air Force Contract F33615-75-C-3068.

The transfer function characteristics of the servoamplifier, servovalve, actuator, LVDT, and demodulator all contribute to the effect. The digital command signal is held constant for one sample period, but the linear feedback signal continues to change. Therefore, the resultant error summation is correct only at the instant of command

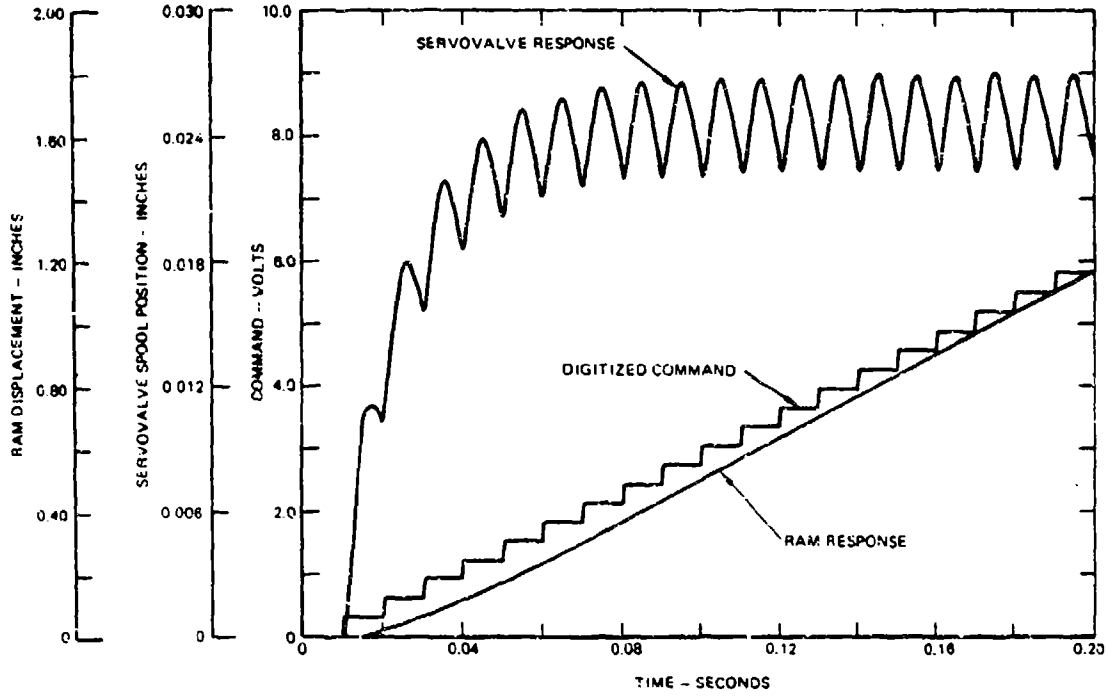

Figure 18. Effects of 100 Hz Sample Rate on Unfiltered Ramp Input

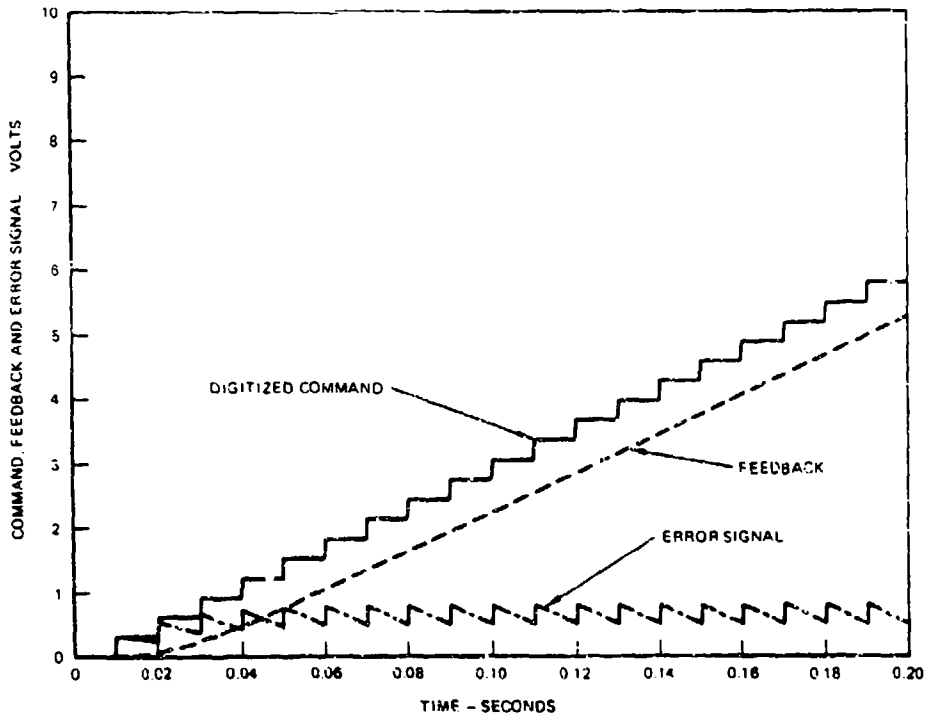

Figure 19. Effects of 100 Hz Sample Rate on Unfiltered Ramp Input

update, developing a sawtooth waveform. The error waveform as shown in figure 19 will pulse the servovalve at the system digital sample rate.

The use of a notch filter to alleviate this problem is discussed below. However, another solution is to sum the feedback and command signals in a digital format, either by converting the analog feedback signal or employing a digital feedback transducer. The digital summation results in an error signal waveform as depicted in figure 20.

The addition of a notch filter in the command path to suppress the sampling frequency has the transfer function:

$$\frac{e_{in}}{e_{out}} = \frac{S^2 + \omega^2}{S^2 + 4\omega^2 + \omega^2} \qquad \text{where } \omega = 2\pi \quad 100$$

Its frequency response is displayed in figure 21.

The effect of this filter for a ramp command is shown in figure 22, which indicates that the filter is effective in reducing the servo valve spool response to the sampling frequency. The ram position is the same as before.

Since data bus capacity is directly related to frequency, a study was made for two other sampling rates (40 and 10 Hz).

In examining the effects of the unfiltered 10 Hz sampling rate on the servovalve spool, it was noted that the servovalve opened and closed at a rapid rate, which could cause the following problems in a hydraulic system:[1]

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[1] This condition existed at all sampling rate frequencies investigated.

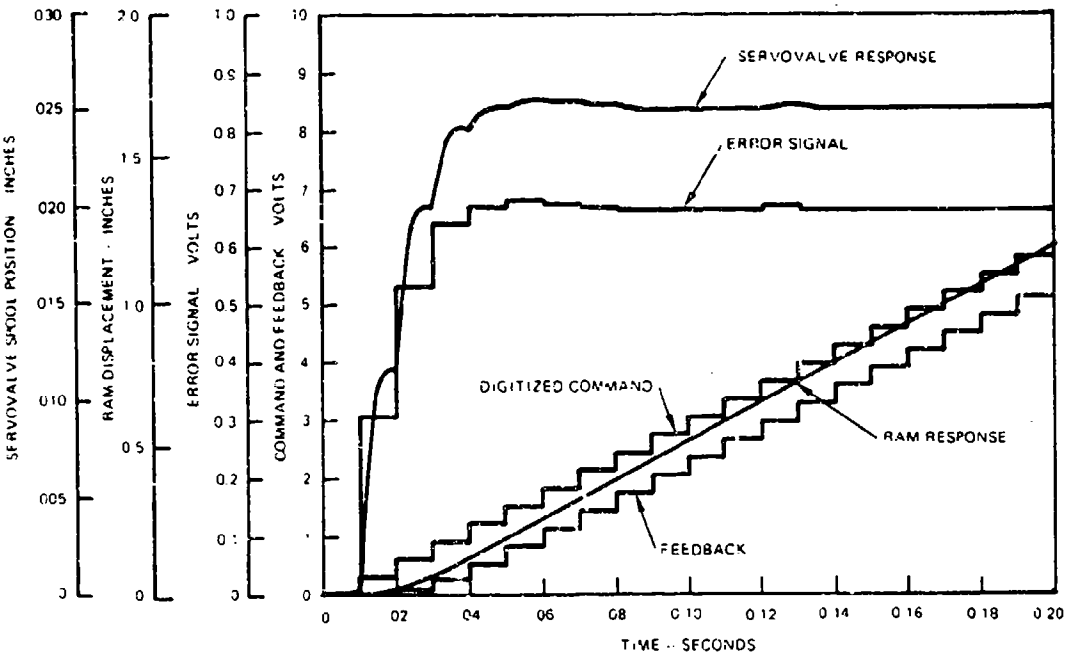

Figure 20. Effects of Digital Summation

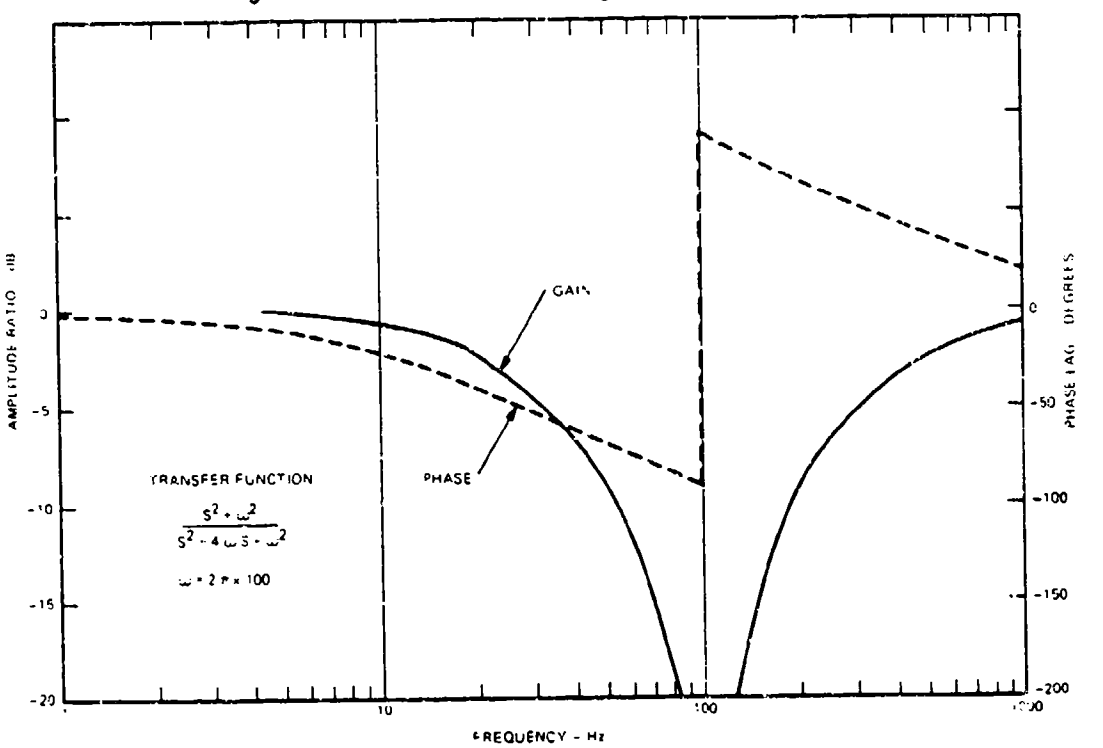

Figure 21. Frequency Response, 100 Hz Notch Filter

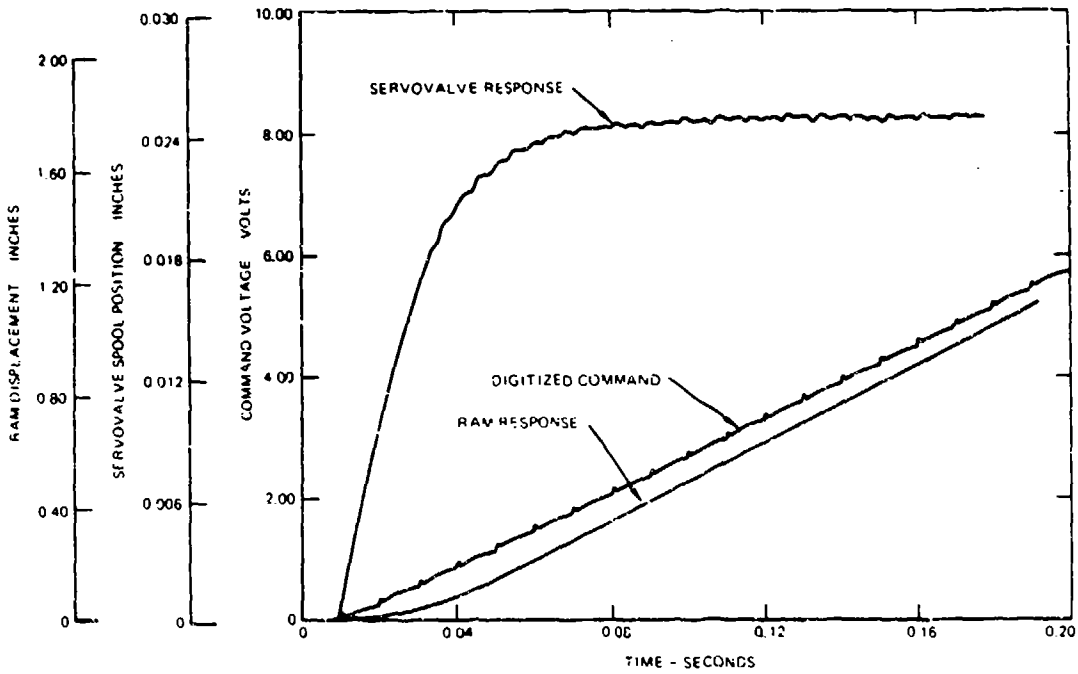

Figure 22. Effects of 100 Hz Sample Rate Input With Notch Filter

- Induce pressure transients in the hydraulic components and transmission lines, causing potential fatigue problems and affecting the overall performance of the complete system.
- Create interaction between the lines and associated components.
- Limit power transmission of the fluid lines.
- Induce oscillations in hydraulic components.

An extensive analysis is required to evaluate all of the above problems, but in order to examine one of the potential problems, a fifteen-foot supply line was added to the servoactuator nonlinear dynamic model. A nonlinear distributed parameter analysis was conducted on the line while the servoactuator was being subjected to a 10 Hz sample rate (no filter). The effects of the 10 Hz sample rate on the supply line are shown in figures 23 and 24. The figures show that the

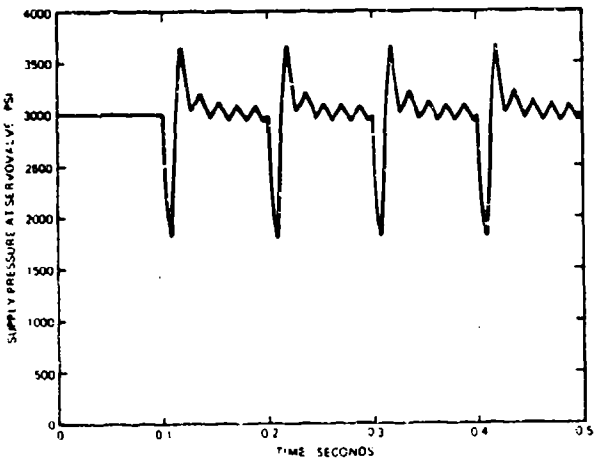

Figure 23. Servovalve Inlet Pressure

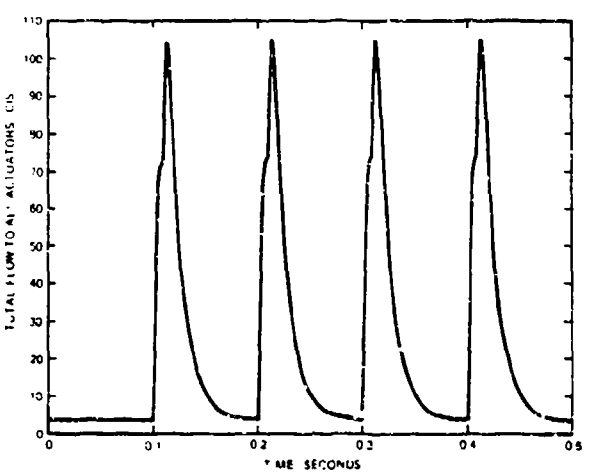

Figure 24. Servovalve Inlet Flow

supply pressure at the servovalve drops down to 1800 psi, peaks up to 3700 psi, and oscillates; the flow surges to 105 cubic inches per second. It should be noted that the pressure and flow performance has the period of the 10 Hz sample rate.[2] This is an undesirable characteristic, and if the analysis were expanded to include the complete aircraft hydraulic actuation system, the problem would be more pronounced.

A detailed evaluation of the 10 Hz and 40 Hz sampling rate problem is contained in Appendix D. A study of notch filters is made, and the results using these and compensated notch filters is displayed in figure 25, showing acceptable performance at 40 Hz and unsatisfactory performance at 10 Hz.

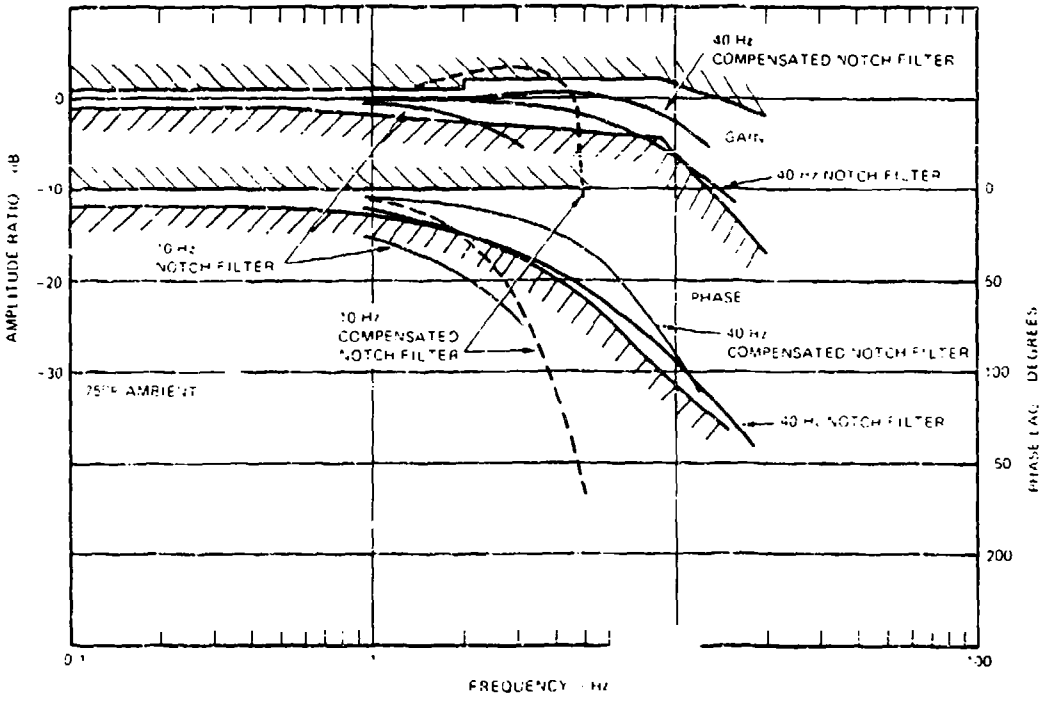

Figure 25. Large Signal Frequency Response 10 and 40 Hz Sampling Rate

[2] 20 Hz at null.

SECTION IV
DETAIL CONFIGURATION MECHANIZATIONS

In Section II the elements and six configurations were defined. In Section III the design issues derived from these configurations are discussed.

This section will describe the six configurations in detail in terms of:

- Physical Location of Elements
- Power Supply
- Interconnections
- Triplex Channel Mechanization
- Servo Processor Mechanization
- Design Trade-Offs.

A. BASELINE SYSTEM

The general block diagram of the baseline triplex actuator system is shown in figure 26. The system is analog fly-by-wire, with three analog computers controlling triplex servo actuators. The redundancy management, failure detection, and loop closure computations take place in the servo processor (element C). Details of the active-on-line concept are described in Section III, "Redundancy Architecture."

1. Physical Location of Elements - The flight control computer complex consists of three enclosures, (one for each channel) within the avionics bay, a temperature-controlled environment. Each enclosure contains a pair of analog control (law) processors and all the servo processors for surface control.

2. Power Supply - The electrical power supply system for each enclosure (channel) is organized into two separate sections - one to power

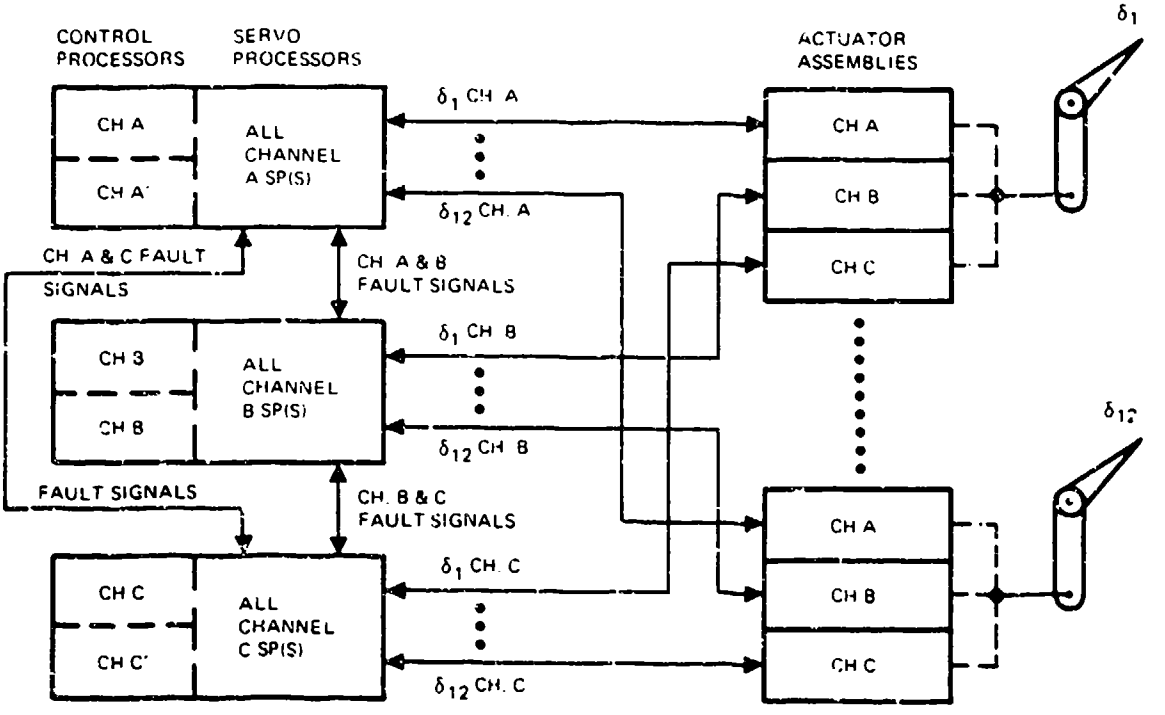

Figure 26. Block Diagram Baseline Multiactuator System

one control processor and the driver sections of each servo processor and the other to power the monitoring section of the control processor and the modeling-monitoring sections of the servo processors.

3. Interconnections - Connections between the control processors and the servo processors are made by means of a motherboard. There are approximately 10 per servo processor, or 120 within each enclosure for an aircraft with 12 controlled surfaces. Connections between the servo processors and each actuator complex are 49 in number or 588 for 12 controlled surfaces.

4. Triplex Channel Mechanization - Figure 27 shows the triplex channel mechanization for one actuator. Control processor (A, A', etc.) is that part of each computer complex which generates the specific command to the actuator-associated servo processor circuitry. Reset logic is in place for use in initial reset, and for retry after a detected fault condition, if this mode is required as part of the cockpit-controlled redundancy management concept.

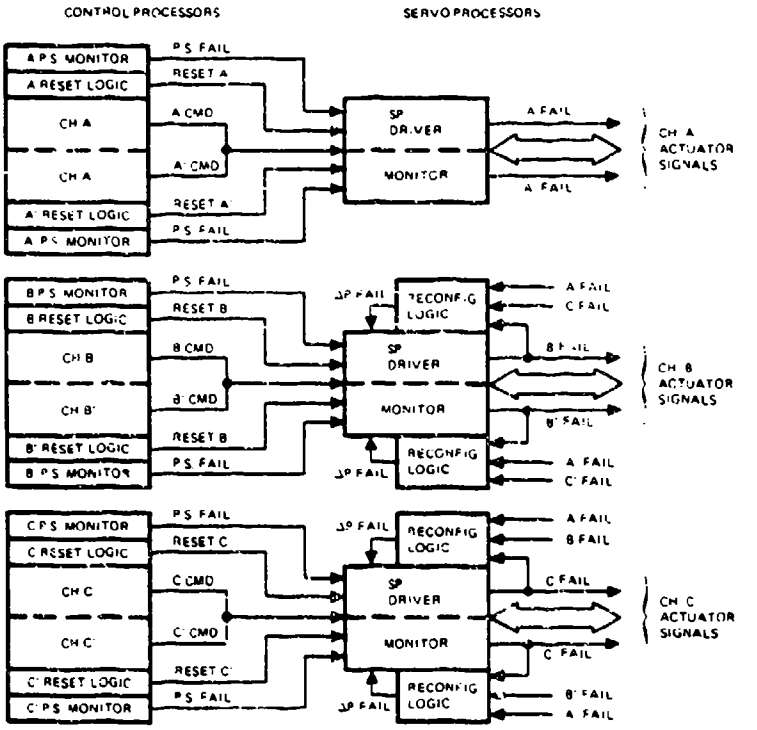

Figure 27. Block Diagram Baseline Triplex Channels

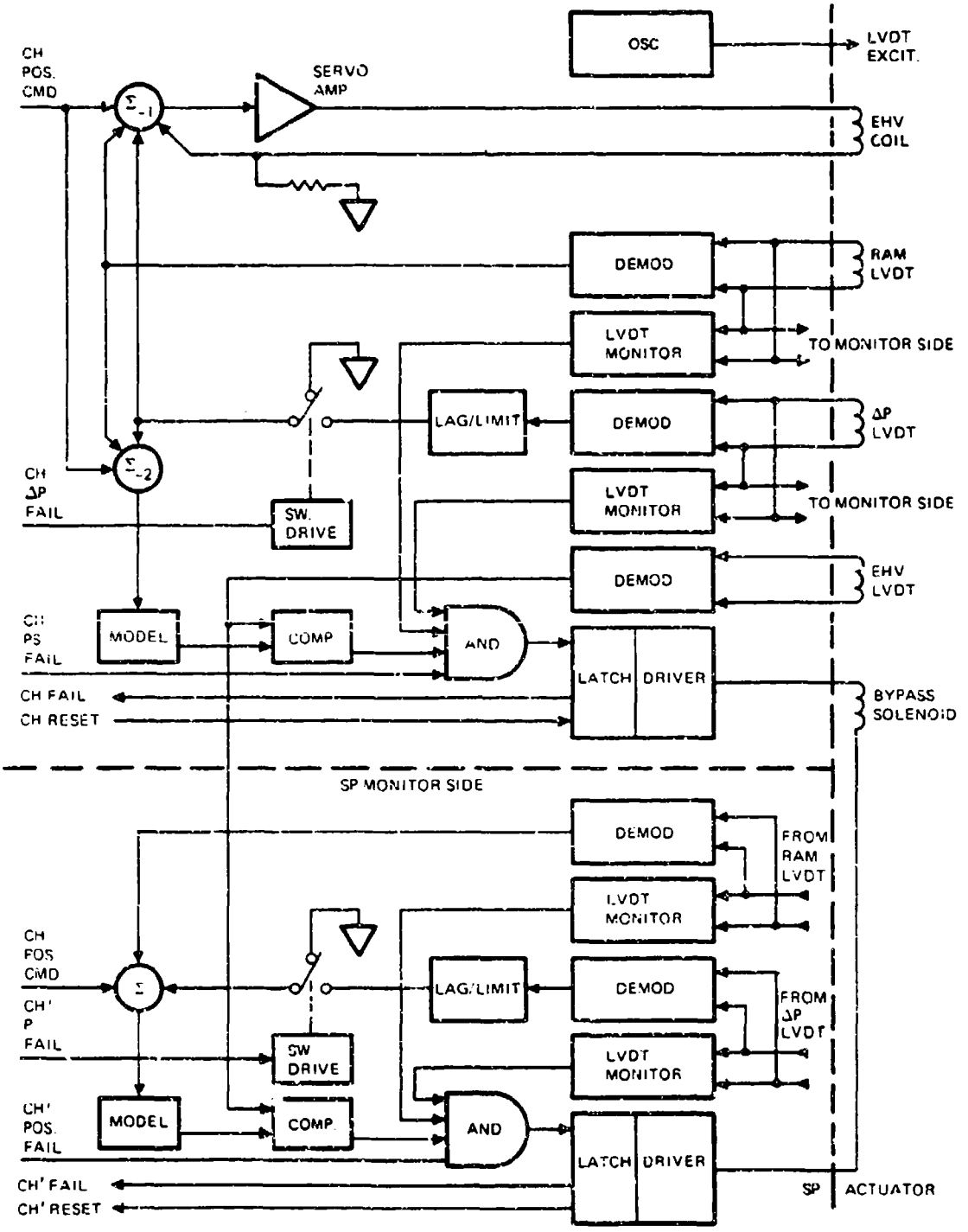

Figure 28. Block Diagram Baseline SP Channel

If the difference between the model output and the actual EHSV position is greater in magnitude than a preset level, a fault signal is sent to the "and" circuit, which in turn drives a "latch." If the "latch" is driven to a fault state, the "Channel Fail" output will change state to tell the other servo processor channels that this channel is in a fault condition. The latch also will deactivate the bypass "driver" circuit, which will bypass the ram and remove hydraulic pressure from the servovalve. The "and" circuit may also be activated by the "Channel Power Supply Fail" signal or by a fault detected by the LVDT monitor.

All of the failure detection circuits used in the driver side of the servo processor are duplicated in the monitor side of the servo processor. Inputs and outputs are also duplicated. Only one of the bypass solenoid coil drivers is required to operate for a bypass of the related actuator. A detected failure in either side, driver or monitor, can bypass the actuator and set the next in-line servo processor to active operation. Therefore, a "good state failure" of the failure circuitry in one side of a servo processor will still allow detection of operational failures in the servo processor channel.

On-Line Channel Servo Processors - If the servo processor is an "on-line" rather than a normally "active" unit, ΔP circuits and redundancy management switching (shown as dotted lines and boxes) are added to the unit. During "on-line" operation, the ΔP signal, conditioned by the "lag/limit" circuits, is also summed with the command and ram position. This allows the "on-line" actuator to be statically passive but to dynamically share the load.

If a "Ch. ΔP Fail" signal is received from the servo processor reconfiguration logic, the ΔP signal is removed from all summations and the "on-line" servo processor will function like the normally "active" servo processor described in the previous paragraph.

5. Design Trade-offs

Command Comparison Monitoring - This was not required with this configuration. The dual monitors in the servo processor provide fault detection of the separately generated position commands. Discrepancies between the command channels, Ch and Ch' will fail the model-EHSV comparison and bypass the actuator.

Dual versus Single Failure Detection in the Servo Processor - If, in the failure detection circuitry of the servo processor, a function or component fails to the "good" output state, it is possible to have an undetected operational failure. Duplicating failure detection circuits allows detection of operational failures. Also, some command monitoring circuits are saved due to the overlap of functions.

Dual Bypass Coil Drivers - Since the bypass of an actuator must be very reliable for fail-safe operation, dual drivers were used in all servo processors. High reliability bypass valves in the on-line units are necessary since they may become an active channel during some fault conditions.

B. CONFIGURATION I - "DIGITAL CONTROL PROCESSOR"

This configuration deals with a control processor feeding a digital command signal into an analog servo processor, which inputs in turn to an electrohydraulic servo valve.

The command signal is a 12-bit digital word transmitted once during every sampling period. To minimize the effects of this staircase shaped signal, a notch filter was added to the servo processor. Without the notch filter this signal would cause the servovalve spool to be almost in constant motion, resulting in undue fatigue of hydraulic system components. This design issue is discussed in Section III, "Digital Control Processor Sampling Rate."

This configuration is represented in figure 29. It is the same as the baseline except that dual digital processors replace the analog control processors in each of the three channels. This necessitates the addition of digital-to-analog (D/A) converters and notch filters in the analog servo processors, which are otherwise similar to the baseline. D/A conversion, loop closure, failure detection, and redundancy management are accomplished in the servo processors as in the baseline.

1. Physical Location of Elements

As with the baseline, all servo processors associated with one channel (A, B or C) are physically located with their control processor pairs, within an enclosure, and each of the three enclosures is dispersed within the avionics bay.

2. Power Supply

As in Configuration I, the power supply for each enclosure (channel) is organized into two sections.

3. Interconnections

Communications between the control processor and its associated servo processors are by means of two digital parallel buses, both common to all servo processors within the specific channel enclosure. The

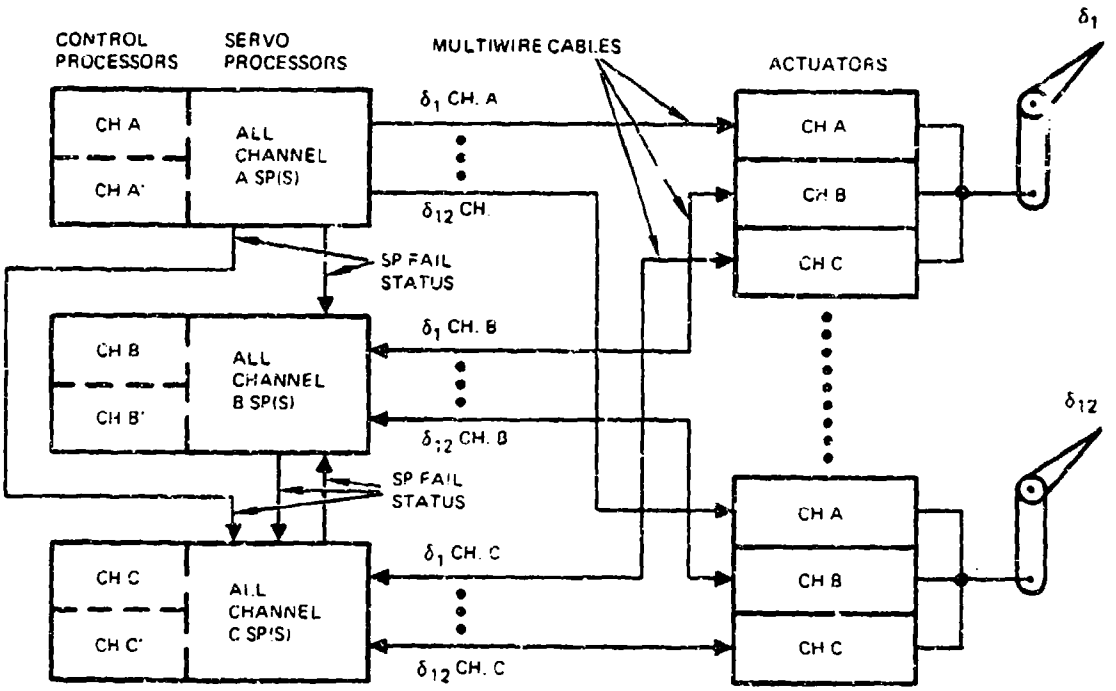

Figure 29. Block Diagram Configuration I Multiactuator System

buses operate in a broadcast format. Servo processor fail status is communicated to the other two servo processors for that surface via discrete wires. Connections between servo processors and actuators are aircraft group A and identical to the baseline.

4. Triplex Channel Mechanization

Figure 30 shows the system for one triplex actuator. The servo processor acts as a monitor of each control processor bus as well as for the integrity of the control processor pair. Each of the monitor outputs is logically "anded" with one of the dual outputs of the power supply monitors, then sent via 2 discrete wires to all servo processors in the enclosure. These two status signals are also sent to the other two control processor enclosures for redundancy management purposes.

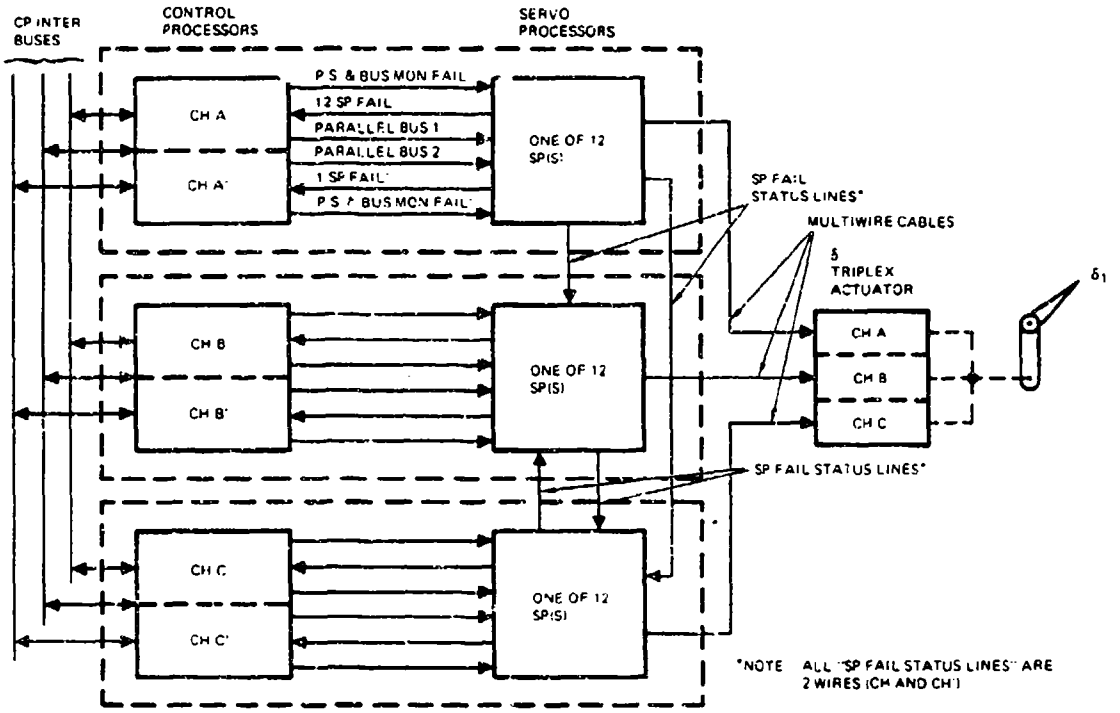

Figure 30. Block Diagram Configuration I Triplex Actuator System

5. Servo Processor Mechanization

Figure 31 shows the detailed block diagram of a servo processor channel. Dotted connecting lines and boxes show the reconfiguration and ΔP functions that are not used in any normally "active" servo processor channels but are used in all "on-line" servo processor channels. Solid lines and boxes show circuits that are identical in all servo processors. Servo processor functions include D/A conversion, servo loop closure, servo loop failure detection, and servo processor redundancy management.

Each servo processor has added functions for control processor interface: two D/A's, two registers, two command filters and two sets of bus interface logic to interface with the parallel buses from the control processors.

The analog implementation of the servo loop closure, failure detection, and active/on-line operation of the servo processor are unchanged from baseline operation.

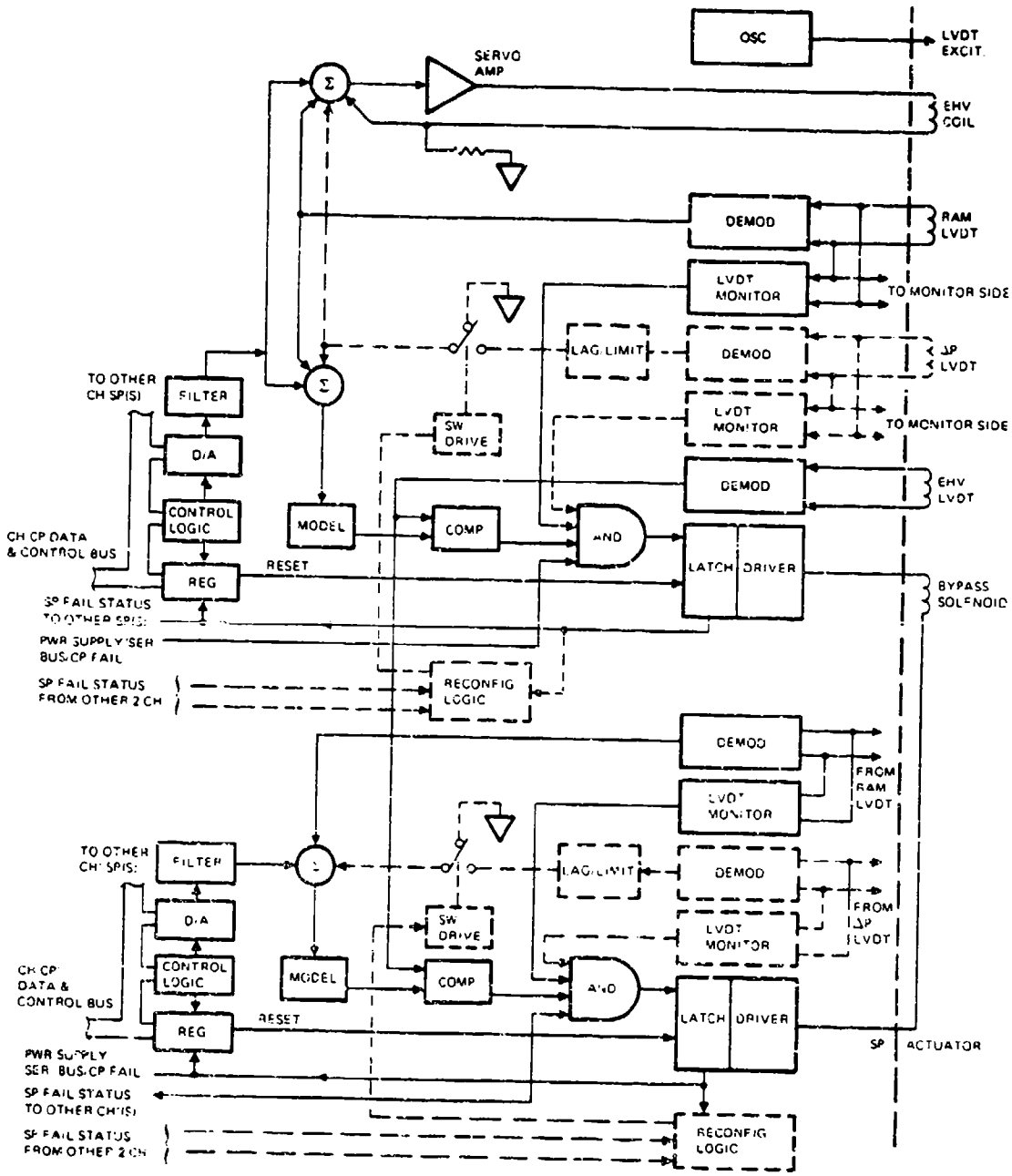

Figure 31. Block Diagram Configuration I SP Channel Mechanization

6. Design Trade-offs

Analog Servo Processor Functions versus Digital Implementation - The complexity of the servo processor when implemented in analog is less than in digital. The complexity added to each servo processor by parallel bus interface is minimal. Complexity for a serial bus interface is greater, as will be seen in Configuration II.

Parallel versus Serial Control Processor Buses - Since the control processor/servo processor data link is all within the same enclosure, the parallel bus structure requires the least hardware to implement and is the least complex interface.

C. CONFIGURATION II - "SERIAL DATA BUS"

This system is functionally the same as Configuration I except that a serial bus is used to communicate between the control processor and its servo processors (figure 32).

1. Physical Location of Elements

The servo processors are now remote from their corresponding control processor and are housed together (by channel) in three separate enclosures in a separate, temperature-controlled bay. The control processor pairs are located in three dispersed enclosures in the avionics bay.

2. Power Supply

Each servo processor enclosure now has its own power supply which is common to all servo processors within the enclosure.

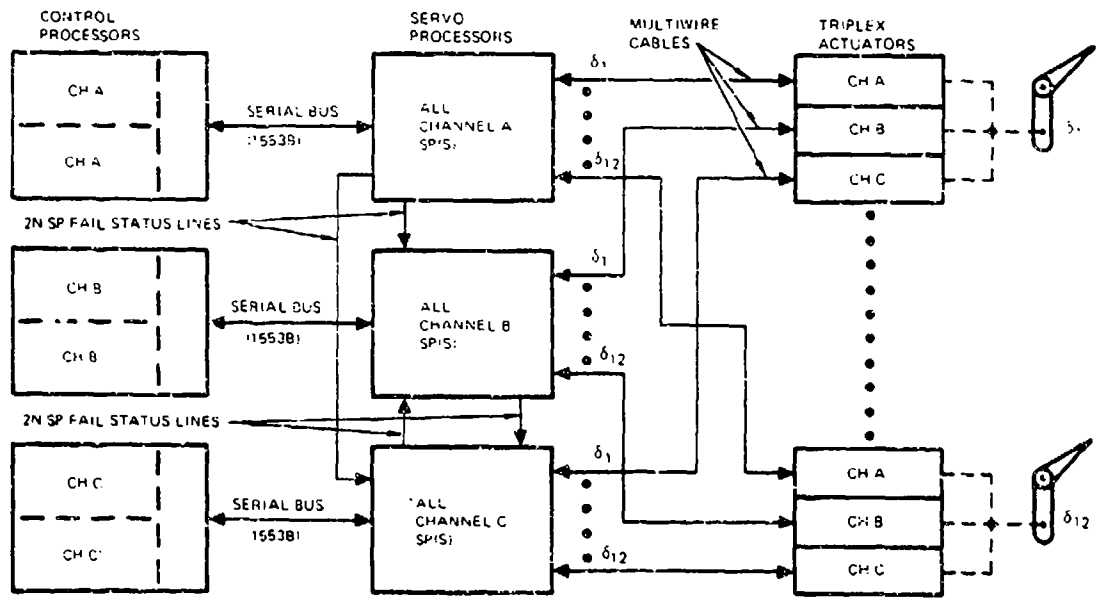

Figure 32. Block Diagram Configuration II Multiactuator System

3. Interconnections

The control processor/servo processor link is now a serial bus between control processor-servo processor enclosures. Parallel bus data distribution is used within servo processor enclosures. Connections (group A) from servo processors to actuator are the same as in the baseline and Configuration I, although shorter due to the servo processor locations.

4. Mechanization within the Servo Processor Enclosures

Figure 33 is a block diagram of the serial bus interface and power supply within each servo processor enclosure. All serial bus interfaces and parallel data bus control is implemented only once in each servo processor enclosure. Two "All channnel fail" lines represent the fail status of functions common to all servo processors within the enclosure (i.e., control processor pair, enclosure, power supply, or serial bus). These two lines are inputs to all servo processors within

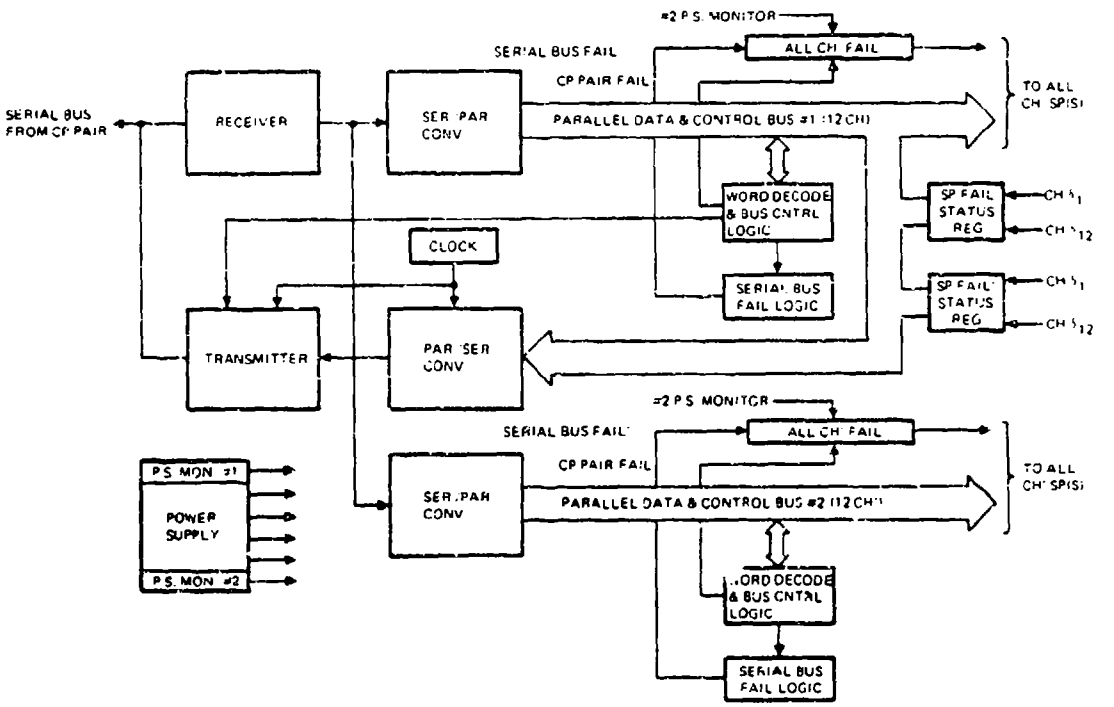

Figure 33. Block Diagram Configuration II SP Enclosure Serial Bus Interface and Power Supply

the enclosure, and a fault signal on either line will disable all servo processors within the enclosure.

5. Servo Processor Mechanization

Figure 34 is the block diagram of a servo processor in Configuration II. The dotted lines and boxes show functions that are added for normally "on-line" servo processors (same as Configuration I). The parallel data bus control interface and dedicated status lines used in this configuration are all functionally identical to the servo processor interface lines in Configuration I.

6. Design Trade-Offs

Control Processor/Servo Processor Serial Bus - When the control processor and servo processor are in separate enclosures, bus timing, connector size and least number of interface wires all favor using a serial bus as the control processor/servo processor data link

To assess the applicability of the MIL-STD-1553B serial bus, the following assumptions were made.

- All servo processors require 100 Hz update.
- Data words are 20 bit length.
- Servo processor address imbedded in the servo processor command data word.
- All servo processor input commands are sent in one transmission that is preceded by a control processor status word.
- After each update, two data words are sent to the control processor and contain the status of all servo processors.
- 70% serial bus utilization is assumed for nonfail operation.
- The servo processor enclosure contain 12 servo processors.
- The serial bus is functionally dedicated to servo processor interface.

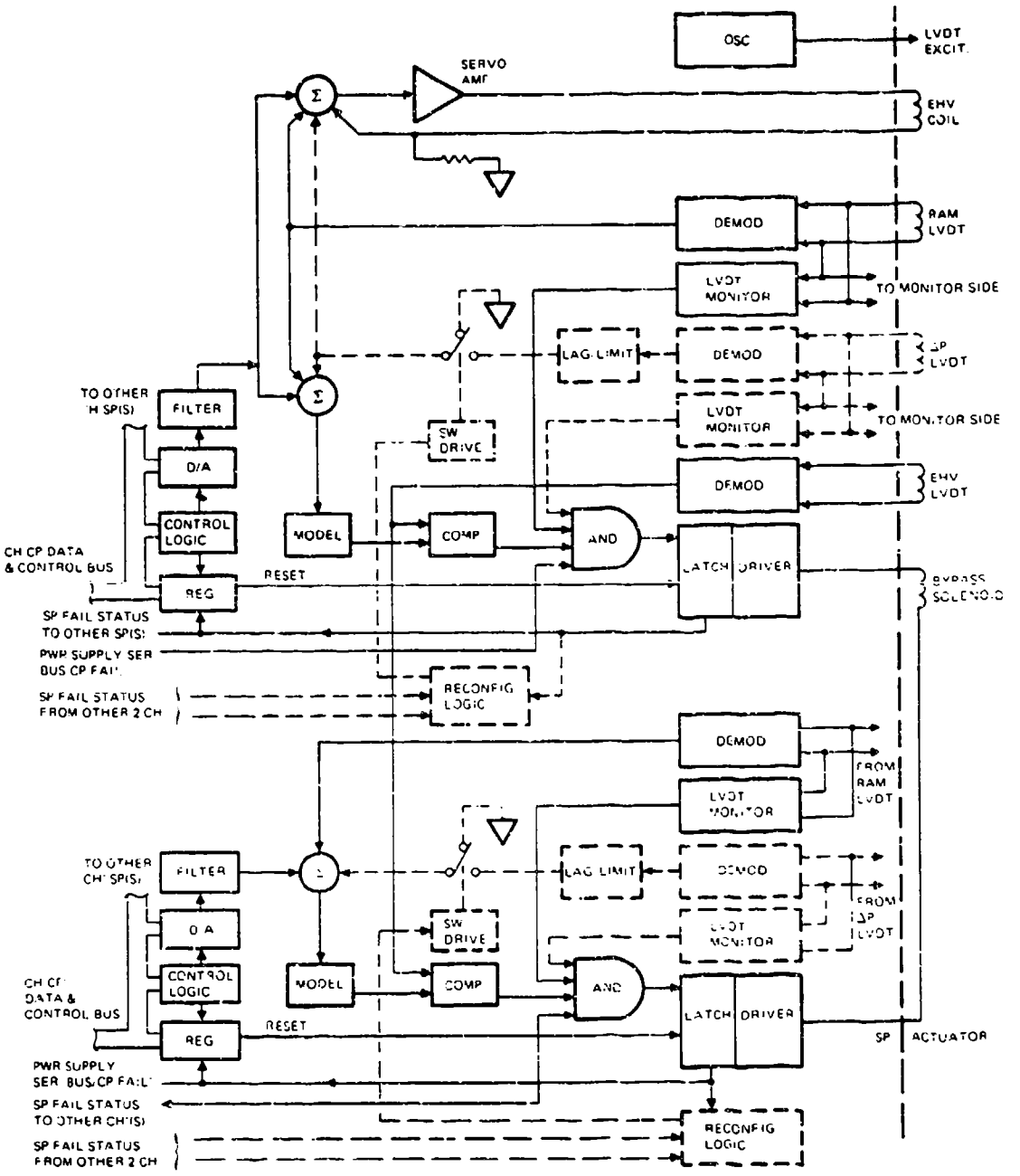

Figure 34. Block Diagram Configuration II SP Channel Mechanization

Configuration II - Bus Utilization[3] - Transmissions per sample data period required for Configuration II, assuming that redundancy management and loop closure are performed in the servo processor, are as follows:

Transmissions	Data Words
1 (CP → SP) of:	1 - CP fail status 12 - position commands
1 (SP → CP) of: 2	2 - SP fail status 15

Using equation 1 shows:

$$\% \text{ Bus Utilization} = \frac{(2 \times 108) + (15 \times 20)}{10{,}000} \times 100 = 5\%$$

Since only one update cycle is required, the bus has 14 times the capacity required (70% being the upper limit).

A calculation was made to evaluate the data bus load if a function, such as redundancy management, were performed in the control processor instead of in the servo processor. This would require sending all required data to the control processor.

Since a given transmission is limited to 32 words, the redundancy management data words are split up into four separate transmissions.

Transmission	Data Words
1 (CP → SP) of:	1 - CP fail-status 12 - position commands

[3] Developed in Section III "Serial Data Bus, Format, Protocol and Application"

Transmission (Contd)	Data Words (Contd)
4 (SP ⟶ CP) of:	32 - (4x8) redundancy mgmt, inputs
5	13+(32x4) = 141

Using equation (1) shows:

$$\% \text{ Bus Utilization} = \frac{(5\times108)+(141\times20)}{10{,}000} \times 100 = 34\%$$

This calculation shows that the data bus would accommodate this data traffic. However, this illustration bears out the benefits of proper functional distribution as discussed in Section II under "Functional Partitioning" since data bus utilization has increased from 5% to 34%. For Configuration II the MIL-STD-1553B serial data bus is an overkill in terms of capacity and hardware cost.

Parallel Data Distribution Within the Servo Processor Enclosures - The addition of a parallel bus and control logic make it possible to utilize only one serial- parallel translation circuit for all servo processors. Weight, cost and power system, complexity favor this approach.

Servo Processor Fail Status to Control Processor; Serial Data Bus versus Discrete Dedicated Wires - To use the bus for this function requires a serial bus bidirectional remote terminal (RT). This involves very little more circuitry at the remote terminal than a receive-only RT. It also requires the addition of control logic and registers to process the status of all servo processors in one circuit per enclosure. This approach was superior to the extra wire, connector pins, and line drivers required in each servo processor of the enclosure.

Analog versus Digital Servo Processor Mechanization - Since the serial bus interface was required only once, the servo processor mechanization still favors an analog approach.

D. CONFIGURATION III - "ACTUATOR INTEGRATED SERVO PROCESSOR"

1. Physical Location of Elements

The servo processors are now located at the actuator itself (figure 35). It should also be noted that contrary to Configurations I and II, where the servo processors were collected in three groups of 12 (for 12 surfaces), they are now collected in 12 groups of three. For the purposes of this study, the mechanization of the servo processors will be similar to Configurations I and II, employ analog techniques for servo loop closure, redundancy management modeling, etc.

2. Power Supply

Each servo processor will also have its own dedicated power supply and monitors. Here again the functions are unchanged, but a power supply is required for each servo processor rather than one for all servo processors of a particular channel.

3. Interconnections

The actuator/servo processor multiwire interface is now very short. The control processor/servo processor serial bus is now distributed to all actuator locations. All data exchanged between servo processors and control processors is by means of the serial digital buses. Servo processor fail status is still exchanged by means of dedicated wires between servo processor channels with each servo processor having its own reconfiguration logic.

4. Servo Processor - Bus Interface Mechanization

Figure 36 shows the block diagram of the serial bus interface resident in each servo processor. The serial bus is bidirectional. The fail status of each side of the servo processor is transmitted back to the control processor. This interface differs from Configuration II in that each servo processor must have a dedicated bus interface. The functions of the bus interface have now been slightly reduced. The "word decode and control" function now has only the input for one servo

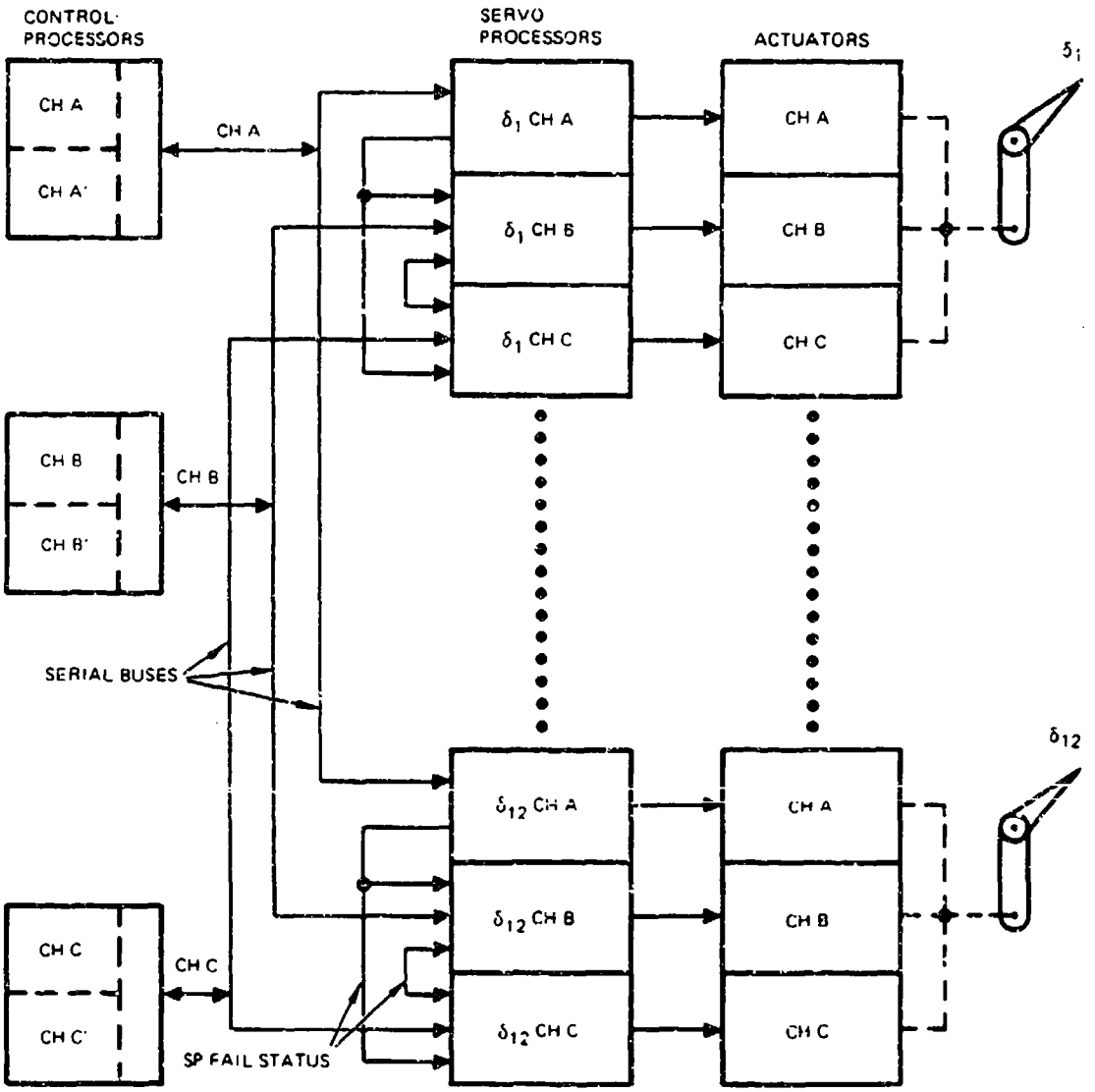

Figure 35. Block Diagram Configuration III Multiactuator System

processor to control, rather than all servo processors of the same channel.

With Configuration III the economy of common bus transceivers and power supplies has been lost. However, the possibility of some single point failures, which could disable one-third of all the actuator channels, has also been eliminated.

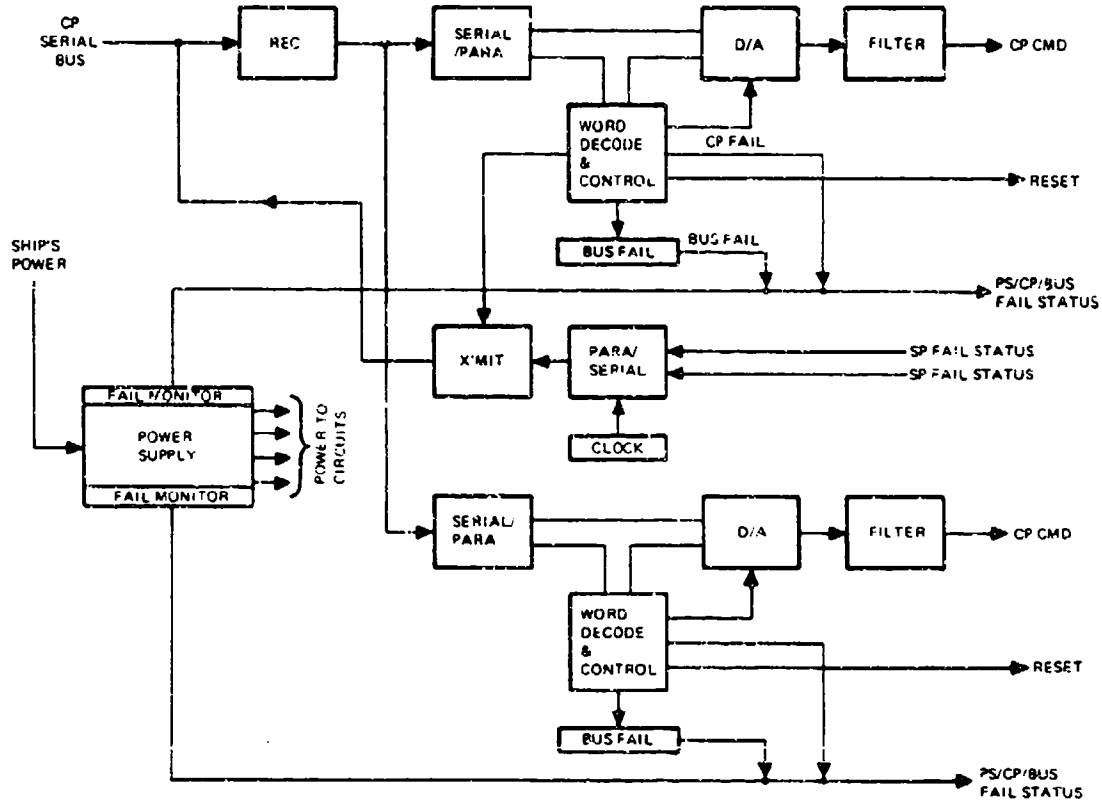

Figure 36. Block Diagram Configuration III Serial Bus Interface

5. Servo Processor Mechanization

Figure 37 shows the servo processor mechanization of Configuration III. The analog implementation of the servo functions remain unchanged from Configuration II. The dotted lines and blocks show functions that are only implemented in normally "on-line" servo processors.

6. Design Trade-offs

Dedicated Bus Interface and Power Supply for Each Servo Processor - If all control processor commands were transmitted via the same bus, any bus failure would totally disable the actuator - an unacceptable single point failure. Each servo processor channel of an actuator must interface with a different control processor. Therefore, even though all three channels are in close proximity, each servo processor must have its own bus interface with a physically different serial bus.

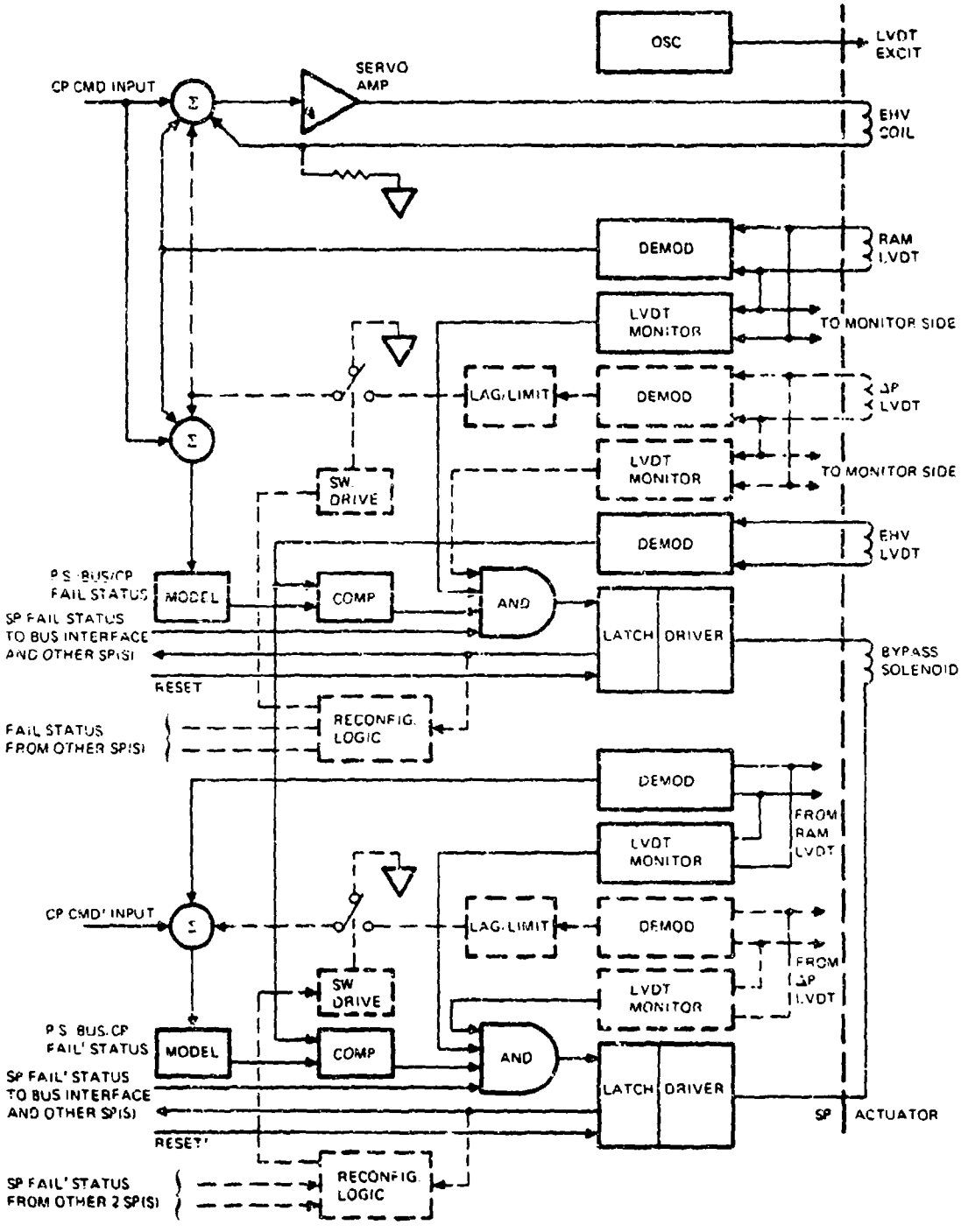

Figure 37. Block Diagram Configuration III Servo Processor

The same case may be made for dedicated power supplies to each servo processor. Anyone power supply failure will not disable the actuator, only one of three channels of that actuator.

Control Processor/Servo Processor Serial Bus Choices - A transformer-coupled serial bus that cannot be disabled by failure of one of its remote terminals is part of the MIL-STD-1553B specification. Under 1553B specifications there must also be a bus controller. In Configura-tion III there would be two choices for the bus controller:

- Each control processor pair could be a bus controller. This would have an undesirable effect on the control processor's task to accomplish nonservo-processor-related tasks. It also decreases the number of data words available on each transmission.
- An autonomous bus controller could be utilized that treats both the control processor pair and each servo processor as a remote terminal. This increases the bus overhead slightly.

Trade-offs will involv effects on redundancy management and the time required to process the bus traffic. For the purposes of this study, the second option is assumed. However, the bus controller is physically integrated with the control processor.

One of the advantages of a "functionally complete" servo processor is that very little data exchange is required between it and the control processor pair for actuator control.

Remote Location Environments - The servo processor of Configuration III will be remotely mounted in locations where space is limited. This will require special high temperature components and the use of hybrid microelectronic packaging techniques. Th transmitter, receiver, and MIL-STD-1553B protocol functions, when implemented with hybrid technology and screened to MIL-STD-883B, have costs approaching $1000 per bus interface unit.

A trade-off should be made between hardware and bus protocol. That, along with the integration of the terminal with the servo processor, should provide a lower cost product.

Configuration III Bus Utilization[4] - Transmissions per sample data period, assuming that redundancy management and loop closure are performed in the servo processors, are as follows:

Transmission	Data Words
12 (CP ⟶ SP) of:	1 - CP fail status
	1 - position command
12 (SP ⟶ CP) of:	1 - SP fail status
24	3 x 12 = 36

However, there are now 12 servo processors to be dealt with separately, calling for 24 transmissions per sample data period.

Using equation (1) shows:

$$\% \text{ Bus Utilization} = \frac{(24 \times 108) + (36 \times 20)}{10{,}000} \times 100 = 33\%$$

If it were now intended to perform redundancy management in the control processor.

Transmissions	Data Words
12 (CP ⟶ SP) of:	1 - CP fail status
	1 - position command
12 (SP ⟶ CP) of:	1 - SP fail status
	8 - redundancy mgmt inputs
24	11 x 12 = 132

[4] Developed in Section III "Serial Data Bus"

Using equation (1) shows:

$$\% \text{ Bus Utilization} = \frac{(24 \times 108) + (132 \times 20)}{10{,}000} \times 100 = 52\%$$

The bus can handle this traffic. This example illustrates the strong effect of the overhead protocol of the MIL-STD-1553B bus capacity when a high number of transmissions are required, since adding the redundancy management data words had less effect than in Configuration II.

7. Reliability - High Temperature Effects

For purposes of this study, no reliability degradation due to environmental effects upon the circuit components is assumed in Configuration III. This, of course, neglects the high-temperature environment of the actuator as is discussed in Section III, "High Temperature Electronics." There, the discussion developed the need for three techniques and technologies (1) switching circuit techniques to drive the servovalve and to excite and demodulate the LVDT's; (2) application of high-temperature semiconductor devices capable of meeting this environment; and (3) use of special micro-electronic packaging techniques to efficiently dissipate the internal heat generated by the semiconductor devices.

E. CONFIGURATION IV - "SERVO PROCESSOR VOTING PLANE"

This configuration demonstrates an approach to retaining high reliability of the actuation system when the reliability of the servo processor may be degraded because of the high-temperature enviroment of the actuator.

This is accomplished by employing a microprocesor pair in the servo processor units and connecting all serial buses to each servo processor, thus creating a voting plane at the servo processor/actuator location.

1. Physical Location of Elements

The three servo processors associated with each actuator are grouped at that actuator location.

2. Power Supply

As in Configuration III, each servo processor has its own dedicated power supply.

3. Interconnections

Control processors are now linked to all servo processors via three serial buses. Interconnections between servo processors and their actuator complexes are by means of short wire interconnects.

4. Triplex Channel Mechanization

Figure 38 shows the block diagram of Configuration IV as a multiactuator system. As may be seen, all servo processors have access to the serial buses of all control processors. This creates a system which allows full system performance with any control processor pair and any actuator servo processor. In previous configurations, for an actuator to be operational, the control processor and servo processor in the same channel (A, B, or C) had to be operational.

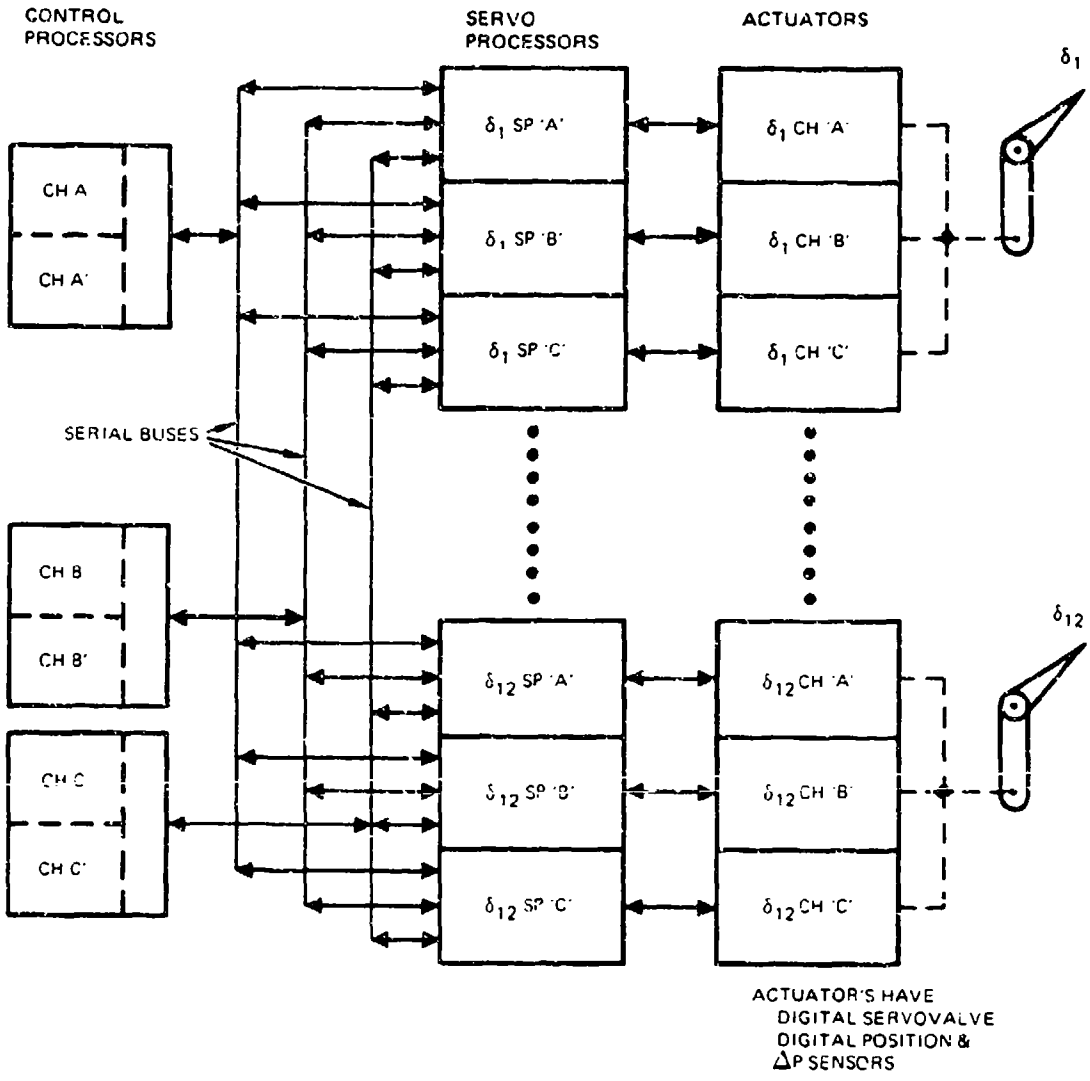

Figure 38. Block Diagram Configuration IV Multiactuator System

Since each servo processor now is connected to all control processor/servo processor buses, the failure status of servo processors for channel reconfiguration purposes is now provided via the buses, rather than by means of dedicated wires between servo processor channels. As in previous configurations, the servo-processor-to-actuator link is by means of short wire interconnects.

5. Serial Bus Interface

Figure 39 shows a block diagram of each servo processor's interface to the serial buses. The receiver from each bus feeds

dual-buffered serial-to-parallel converters and dual-word detectors, a set for each internal microprocessor bus. Each word detector drives its associated interrupt controller and each serial-to-parallel converter feeds its associated internal bus through a buffered register. A transmitter for each serial bus is supplied from both internal buses with data. The transmitter control arbitrates access to the transmitter.

Each servo processor in Configuration IV now receives the control processor commands and the status for all three actuator channels. The mid value of the three commands is used as the position input command for the actuator servo loop closure. Each servo processor's fail status is transmitted at each update cycle to each control processor. This status transmission is monitored by the other servo processor channels of the actuator to implement reconfiguration in the event of a servo processor failure.

6. Servo Processor

Figure 40 shows a block diagram of a servo processor mechanization in Configuration IV. The oscillator for LVDT excitation, amplifier for servo loop closure, and all LVDT demodulation and monitoring are still accomplished with analog circuitry. Functions that are under program control of the servo processor microprocessor (μP) are:

- Control processor command and status storage
- Other servo processor's status storage
- Command voting and determination of servo command to be used
- Failure detection within the servo processor
- Configuration management (active on-line operation in channels where applicable)
- Servo modeling and comparison to actual electrohydraulic servovalve (EHSV)
- Control of transmission and reception of all serial bus information

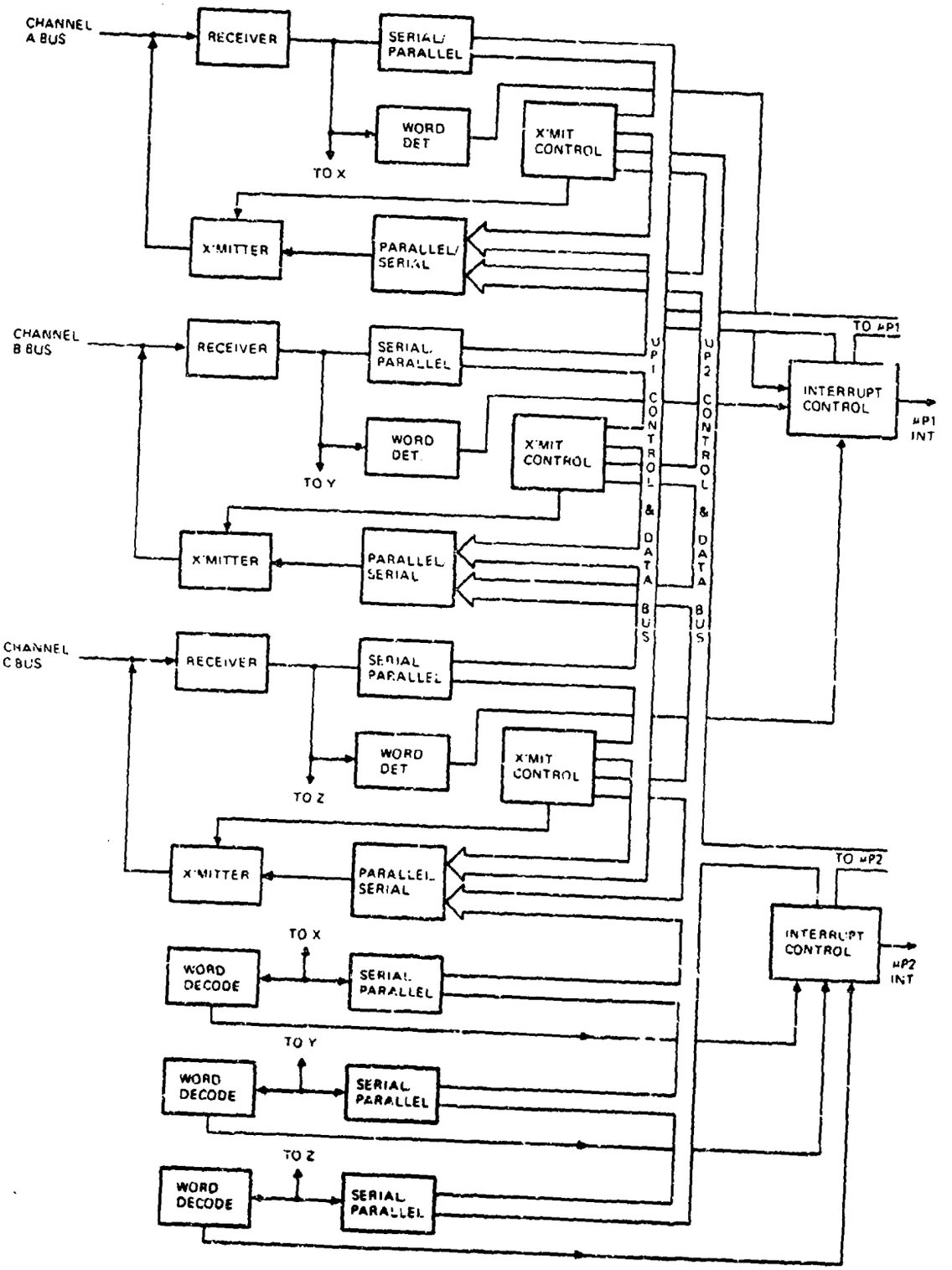

Figure 39. Block Diagram Configuration IV Serial Bus Interface

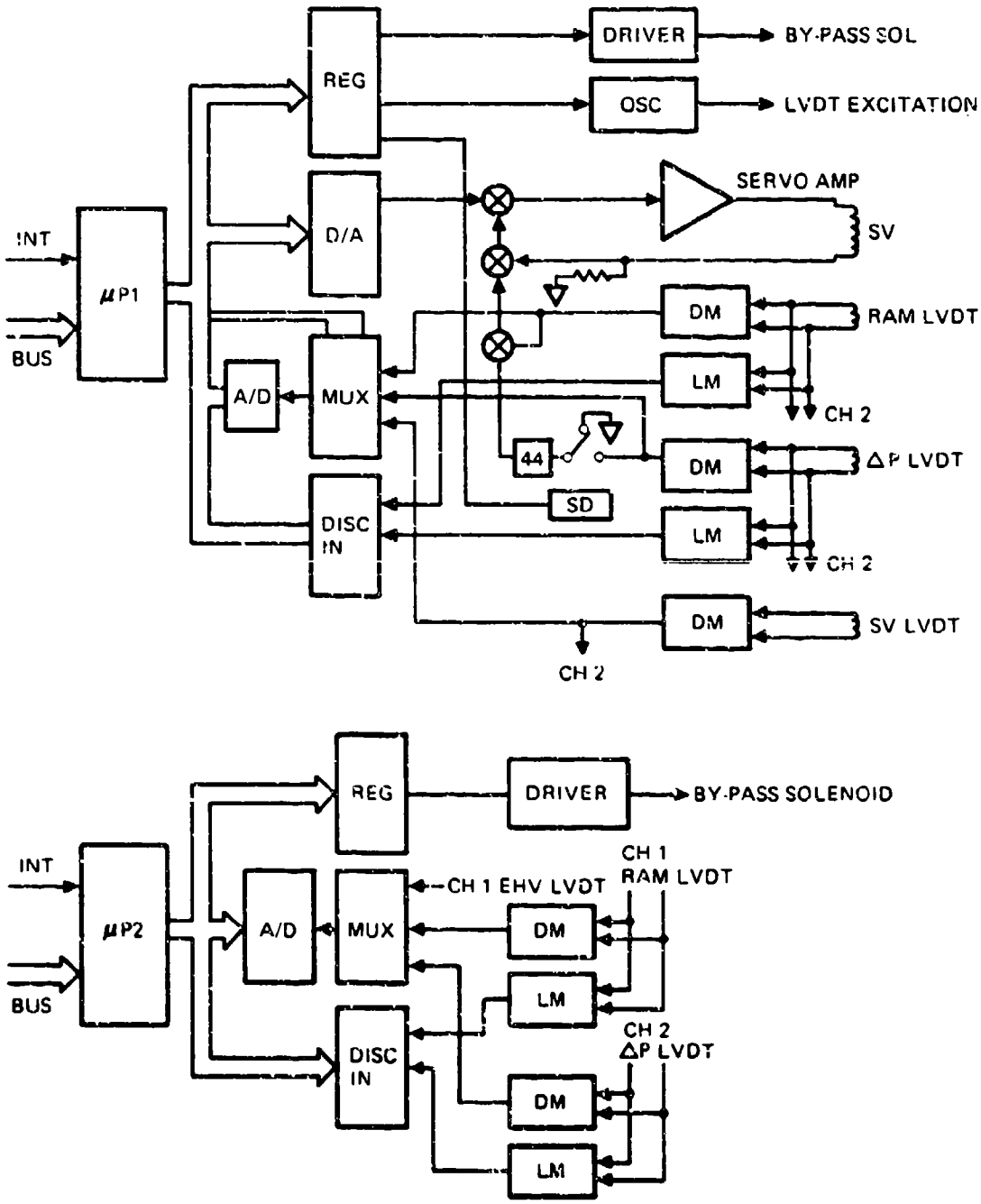

Figure 40. Block Diagram Configuration IV SP Mechanization

- Controlling the bypass driver of the servo processor
- Monitoring all serial buses for a bus failure
- All decisions involving a logical operation

All analog values of the ram, EHSV, and ΔP LVDT's (in normally on-line servo processor) are multiplexed into one analog-to-digital converter and fed into the μP. The discrete outputs of the LVDT monitors are combined in a buffer register and also fed into the μP. With this information, and the last command output from the μP known, the EHSV model may be implemented and the results compared to the actually sensed EHSV position in the μP. The μP program then decides the status to be sent to its "driver" register, in light of the (1) model comparison, (2) serial bus fail status, and (3) power supply fail status.

7. Design Tradeoffs

Use of μP's in the Servo Processors - In previous configurations, the tasks were simple enough that a μP's extra complexity and cost could not be justified. However, the added interface capability required in Configuration IV, coupled with the requirement of command input voting at each servo processor, translated the required functions to a domain which would favor use of μP's over analog circuits since much of the added requirement was either logical or mathematical.

Dual versus Single μP in Each Servo Processor - The concept of a circuit not being able to detect faults within itself, hence the need for parallel functions for comparison and fault detection, is applicable to Configuration IV. Even though the command output that will be computed in μP-2 is not used to position the servo loop, all of the monitor functions should compare with μP-1's control. If a discrepancy exists between μP-1 -2, either has the capability to bypass the actuator channel and transmit the servo processor fail status back on the control processor serial bus.

Configuration IV Bus Utilization[5] - Transmissions per sample data period for one bus are as follows:

Transmission	Data Words
12 (CP broadcast to each surface's SP's)	1 - reset 1 - position command 1 - CP fail status
12 (SP"A" broadcast to CP A and to all SP's)	1 - SP"A" fail status
12 (SP"B" broadcast to all SP's)	1 - SP"B" fail status
12 (CP"C" broadcast to CP C and to all SP'S)	1 - SP"C" fail status
48	(6 x 12) = 72

Using equation (1)

$$\% \text{ Bus Utilization} = \frac{(48 \times 108) + (72 \times 20)}{(10{,}000)} \times 100 = 66\%$$

This shows that the bus has the capacity. However, it should be noted that this is only possible because the "broadcast" mode of MIL-STD-1553B is employed. What is sacrificed is the verification that transmission have been received.

There was no need to consider redundancy management at the control processor in view of the use of microprocessors in the servo processors.

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[5] Developed in Section III "Serial Data Bus"

Analog versus μP Functions - Since each servo processor must communicate with three serial buses, and delay times on the serial buses should be relatively small, separate word detection circuits were used to interrupt-drive the μP's, rather than have word detectors under program control.

Reception and storage of the three control processor's commands and statuses, mathematical comparison of control processor commands, and logical operations on status inputs and on control of binary data flow to and from the serial bus interface are all operations that favor a μP. Because of the large amount of data storage, comparison, and voting, a μP is very well suited for this application in Configuration IV. Here the program control and storage capability of a μP is a more effective mechanization than performing the same functions with logic elements and analog circuitry.

The LVDT oscillator, servo loop closure, demodulation of the LVDT secondaries, and monitoring the LVDT secondaries are still basically analog functions. Accomplishing these functions in the μP would require a much more complex μP program with significantly higher operation speed. The added design difficulty and minor, if any, parts count improvement favors leaving these functions to be done with analog circuitry.

Multiplexed Analog-to-Digital (A/D) Converters versus Dedicated - Since any incorrect data from the A/D Converters into the μP will set conditions to disable the servo processor channel, the fewer parts in the A/D "feedback" the more reliable, assuming approximate equality of MTBF of the parts. Dedicated A/D's would require three A/D's while using the multiplexer would require only two integrated circuits.

F. CONFIGURATION V - "ALL DIGITAL SYSTEM"

This configuration is included to study the use of a digital servovalve and digital transducers. Except for the actuator (ram) the system is totally digital. The servo valve in this configuration is a parallel wire, binary servovalve (figure 41) which was designed, built and tested under United States Air Force contract AF33(657)-8644. This valve had an 8-bit (8 coils) torque motor. For the purpose of this study a 12-bit torque motor is assumed. Also, the binary servovalve is assumed to have the same performance as the jet pipe servovalve used on the baseline actuation device.

It should be noted that neither the 12-bit digital servovalve or the digital encoder is qualified for flight. Presently both only exist as laboratory units. These elements are discussed in Section III, "Digital Actuation Elements."

This configuration, like Configuration IV, uses microprocessors in the servo processor unit as a voting plane to enhance the reliability of the system. This consideration may be required if "high temperature electronics" cannot achieve the required high degree of reliability required.

The multiactuator block diagram is shown in figure 42. Each channel of the actuation devices (element E) consists of a 12-bit digital servovalve; self-monitoring digital encoders for servovalve spool position, ram position and the ΔP transducer; a solenoid bypass valve; and a ram.

The control processors send control surface commands to the servo processor and monitor the servo processor failure status. Loop closure, loop gain, redundancy management, failure detection, and input command voting computations are accomplished in the servo processor microprocessors.

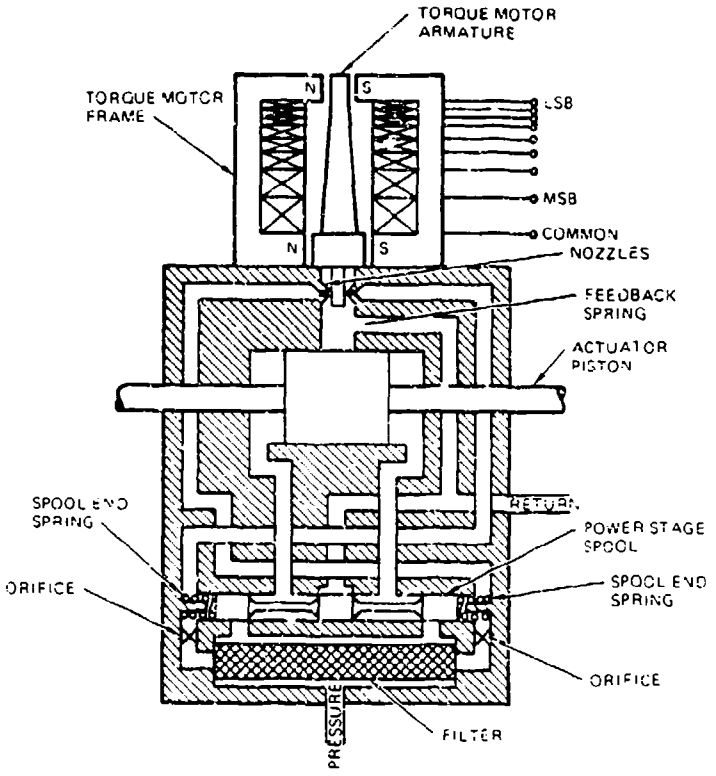


Figure 41. Parallel Binary Servo Actuator, Multicoil Torque Motor Schematic

1. Physical Location of Elements

Servo processors are mounted on or near their respective actuators, as in Configuration III. The servo processor environment is uncontrolled.

2. Power Supply

As in Configuration III and IV, each servo processor has its own dedicated power supply.

3. Interconnections

Interconnection between the servo processors and actuator elements are short wire interconnects. The number of connections is

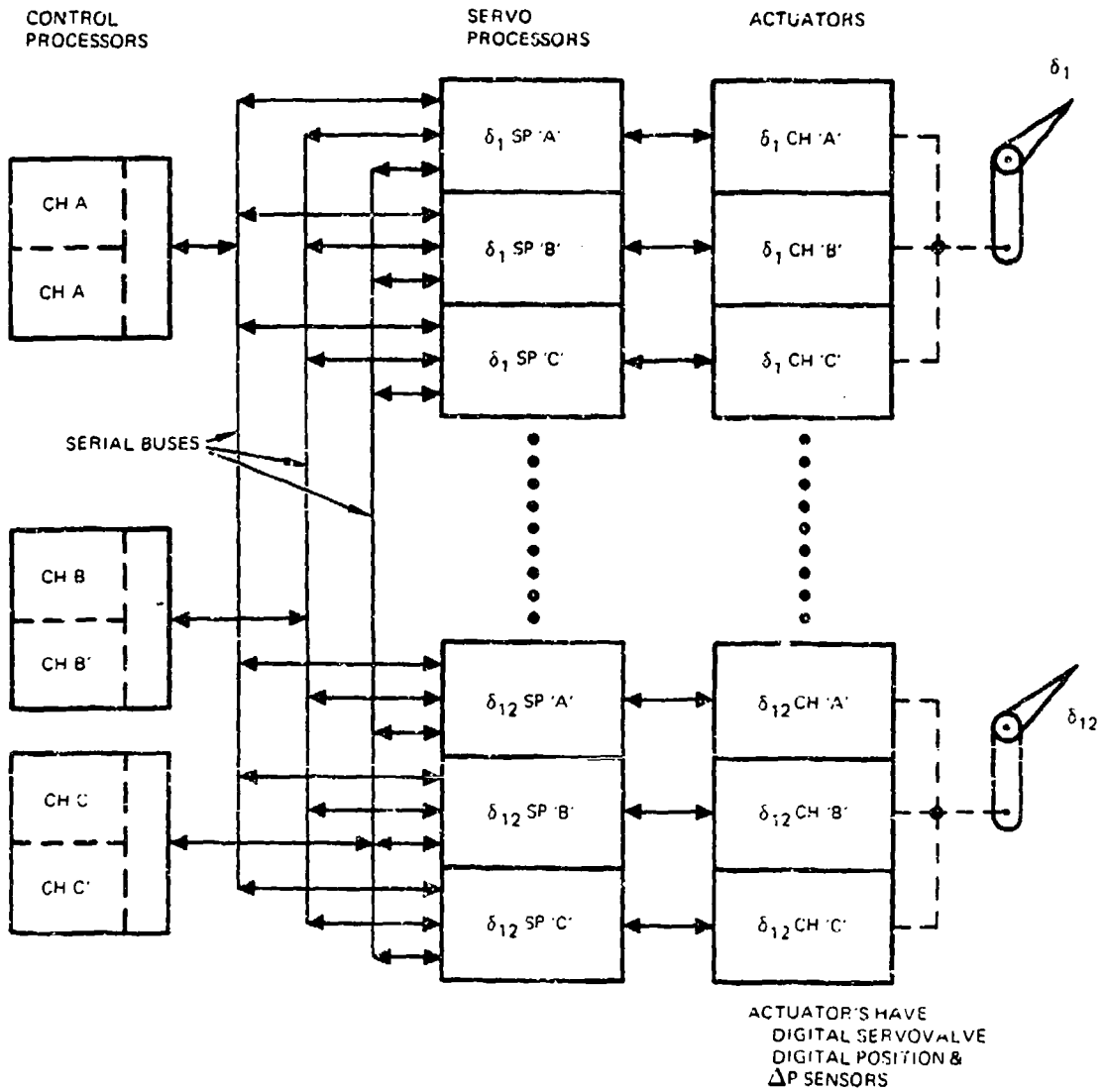


Figure 42. Block Diagram Configuration V Multiactuator System

significant because the actuator devices are parallel-digital, requiring a connection per bit.

4. Servo-Processor Mechanization

Serial bus interface (figure 43) shows a block diagram of the control processor serial bus interface in the servo processor. Each serial bus has one transmitter and one receiver. Each μP bus has a dedicated serial-to-parallel converter and word detector that is fed from the common serial bus receiver. Both buses access the

parallel-to-serial converter and transmitter control. The transmitter control arbitrates availability of the parallel-to-serial converter to the μP parallel buses. The word-decode of each serial bus interrupt-drives its respective μP to receive either commands or data from the serial bus.

The Microprocessors and Actuator Interface - Figure 44 shows a block diagram of the dual ΔP's and actuator channel interface in each servo processor. Dotted lines and boxes show functions and circuits that are only utilized in normally "on-line" servo processors.

All three servo processors of an actuator will receive the position command and control procesor status from all control processor pairs. Each servo processor shall send its failure status to all three control processors. The normally "active" servo processors monitor the status transmission of the other two servo processors of the same actuator. This servo processor status information exchange enables the "on-line" servo processors (two per triplex set) to reconfigure themselves in the event an "active" servo processor fails, without added serial data transmissions.

During each command update frame, three position and three control processor statuses are sent to each triplex servo processor set. Each servo processor of the set compares the three commands and picks a medium value. This value will be the position command for the update frame. The present ram position is then subtracted from the position command.

Once the loop closure computation is accomplished, the digital error (loop gain computation) is amplified and sent to a 12-bit register. Each register location is connected to a switch, which is turned on and off by a 1 or 0 bit signal. If a switch is turned on, current is passed to its coil. Hence, the connections between the servo processor and the actuation device are parallel, hard wires.

If the setup input to each coil creates digital noise to which the servovalve spool responds, twelve filters must be added to the interface electronics, or the microprocessor's sample rate must be increased to minimize this effect.

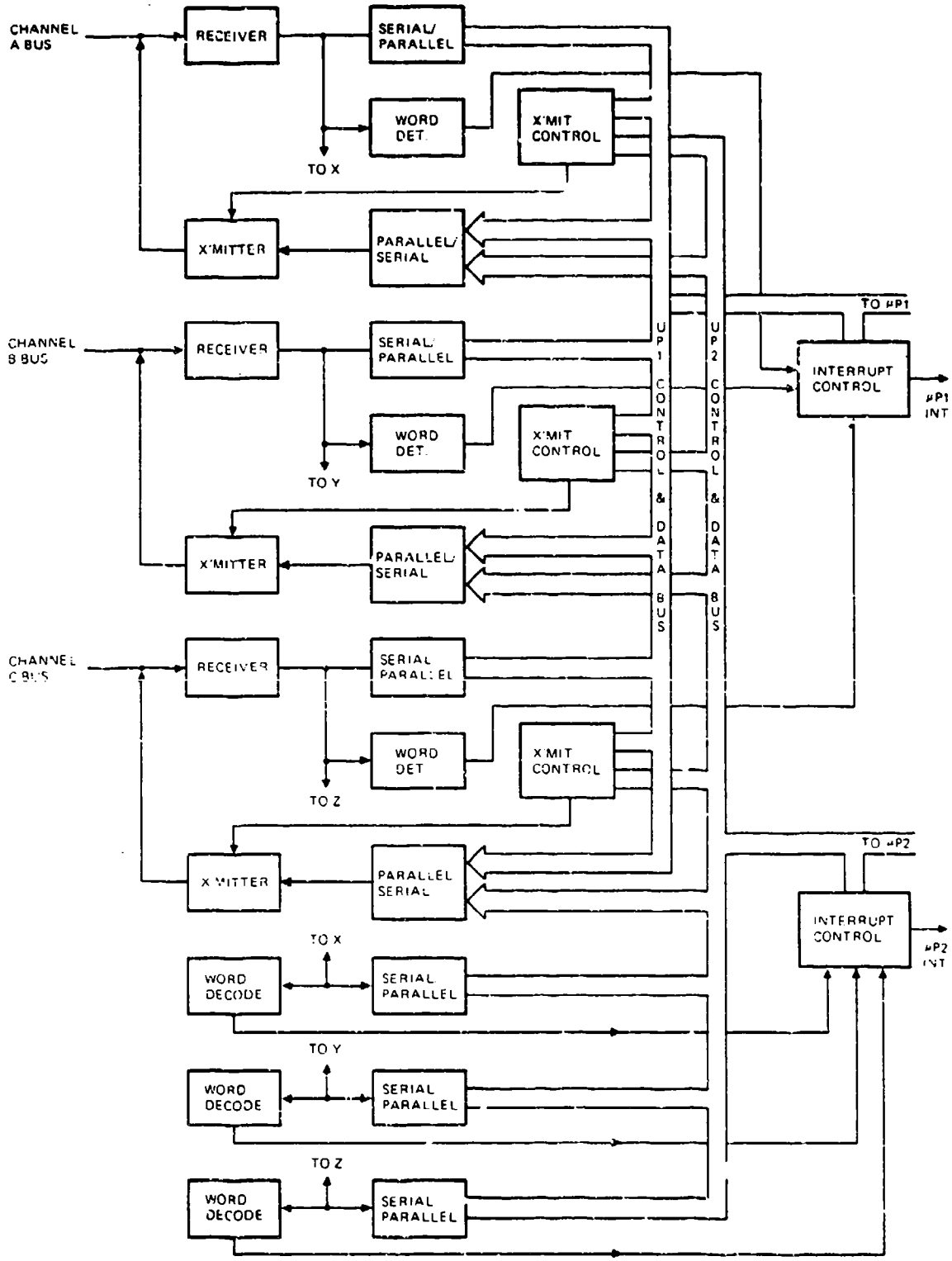


Figure 43. Block Diagram Configuration V Serial Bus Interface

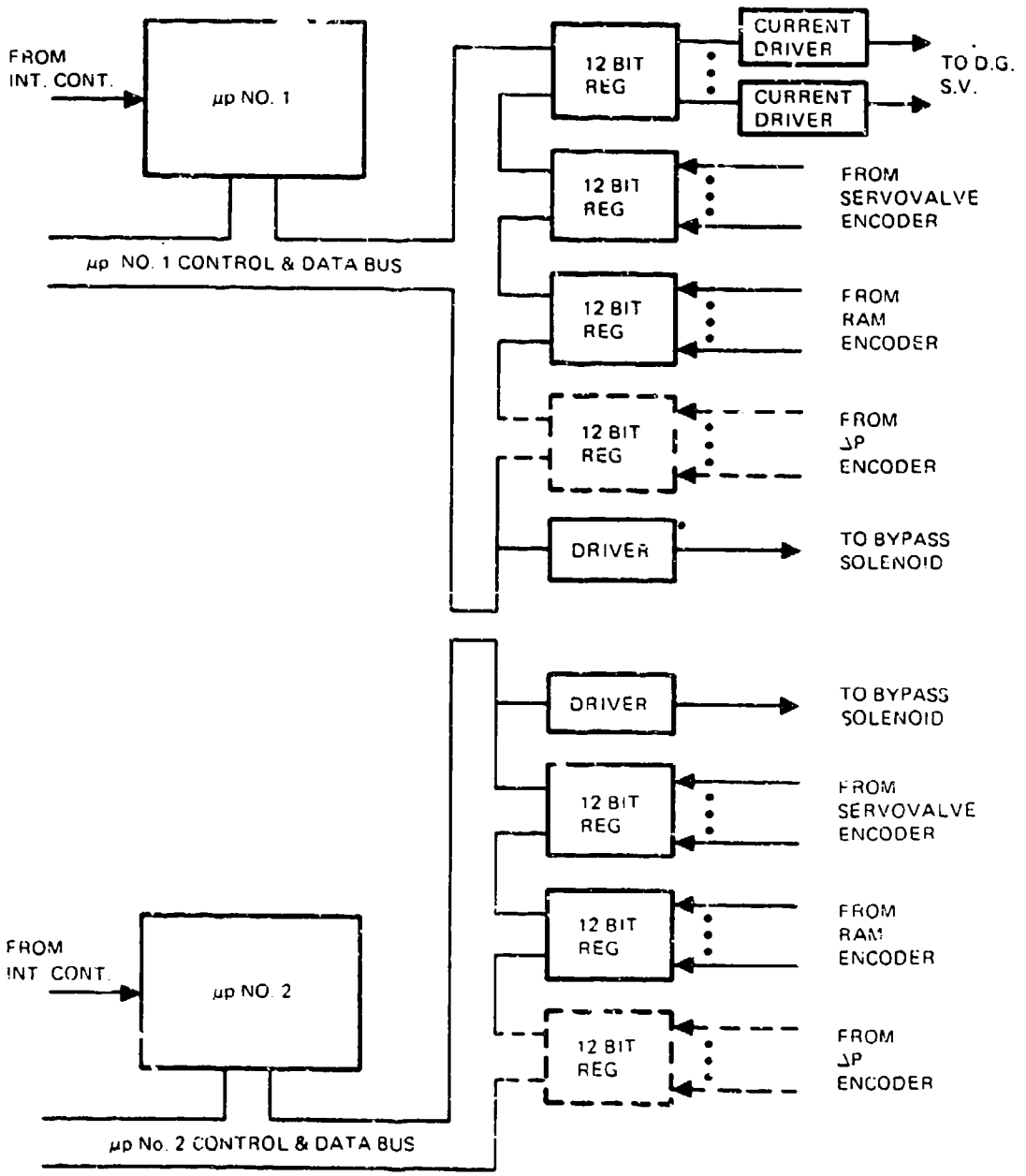


Figure 44. Block Diagram Configuration V SP Microprocessors and Interface to Actuators

SECTION V
CONFIGURATION COMPARISONS

Comparisons were made for performance and physical characteristics of the baseline and five configurations. Figure 45 "Configuration vs. Element Design" is repeated from Section II for reference.

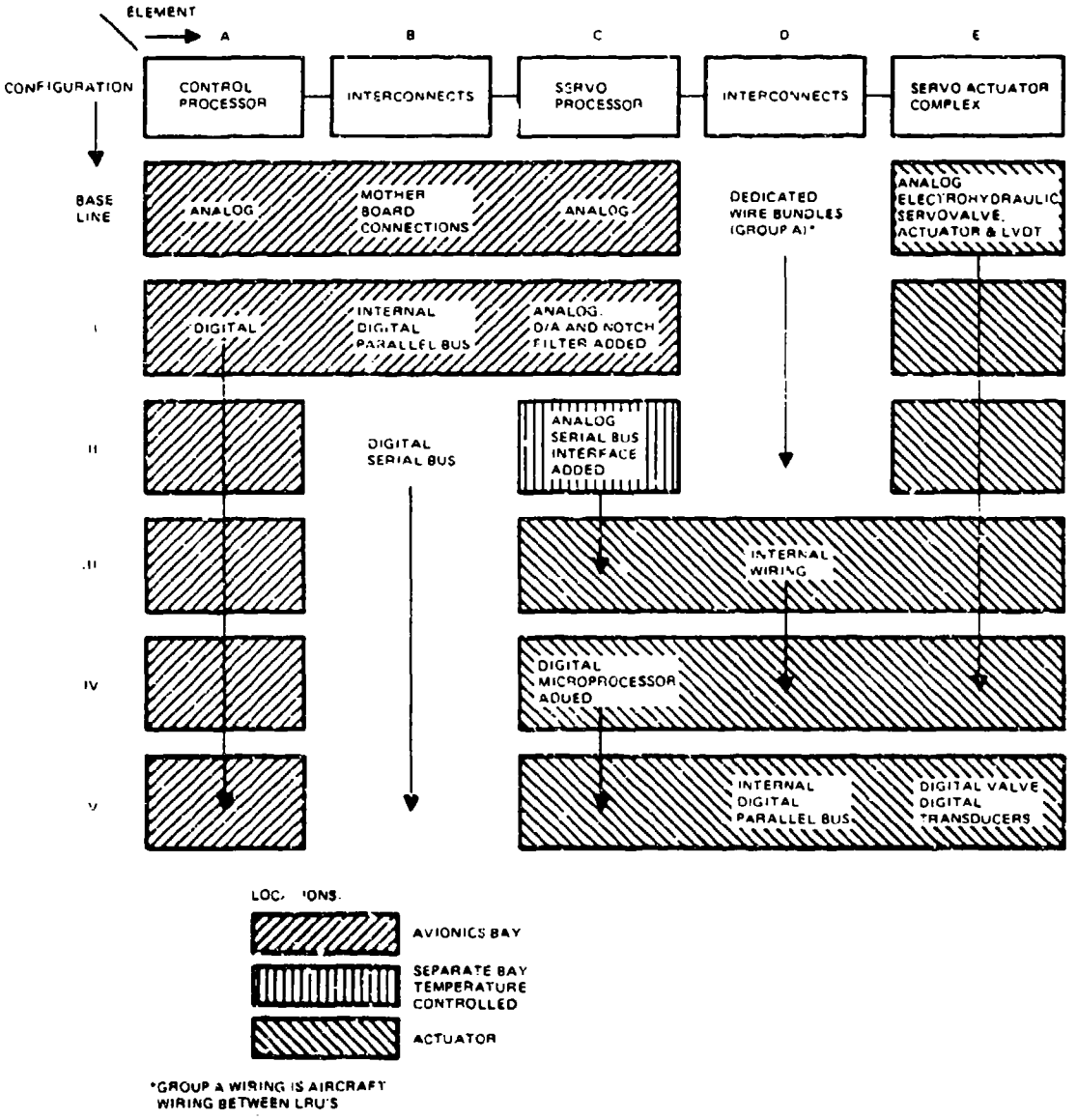


Figure 45. Configuration Vs. Element Feature

A. FUNCTIONAL PERFORMANCE COMPARISON

Performance characteristics of the baseline and four of the five developed configurations were evaluated using an HR Textron non-linear analysis computer program (Appendix C). The results are tabulated in table 1, with frequency response comparisons displayed in figures 46 and 47. Configuration V was not evaluated because the hardware was not developed.

Baseline - The baseline all-analog system characteristics listed indicate that all specification requirements are met. Baseline characteristics are detailed in Appendix B.

Configuration I - This actuation system is functionally similar to the baseline scheme. The only performance differences observed were a slight increase in positional error and a minor degradation in frequency response due to the addition of a notch filter and the digital-to-analog converters.

Configuration II vs. I - No change in performance was noted.

TABLE 1. FUNCTIONAL PERFORMANCE

CONFIGURATIONS	FILTER REQUIRED AT 100 Hz SAMPLING RATE	FREQUENCY RESPONSE (Hz)	STEP RESPONSE-OVERSHOOT (%)	FAILURE TRANSIENTS (%)	POSITIONAL ERROR AT 75°F (%)
BASELINE	NO	10	NONE	9.0	.32
CONFIGURATION I	YES	9	NONE	9.0	.35
CONFIGURATION II	YES	9	NONE	9.0	.35
CONFIGURATION III	YES	9	NONE	9.0	.35
CONFIGURATION IV	YES	10	5%	10.8	.35
CONFIGURATION V	NO	NOT EVALUATED			

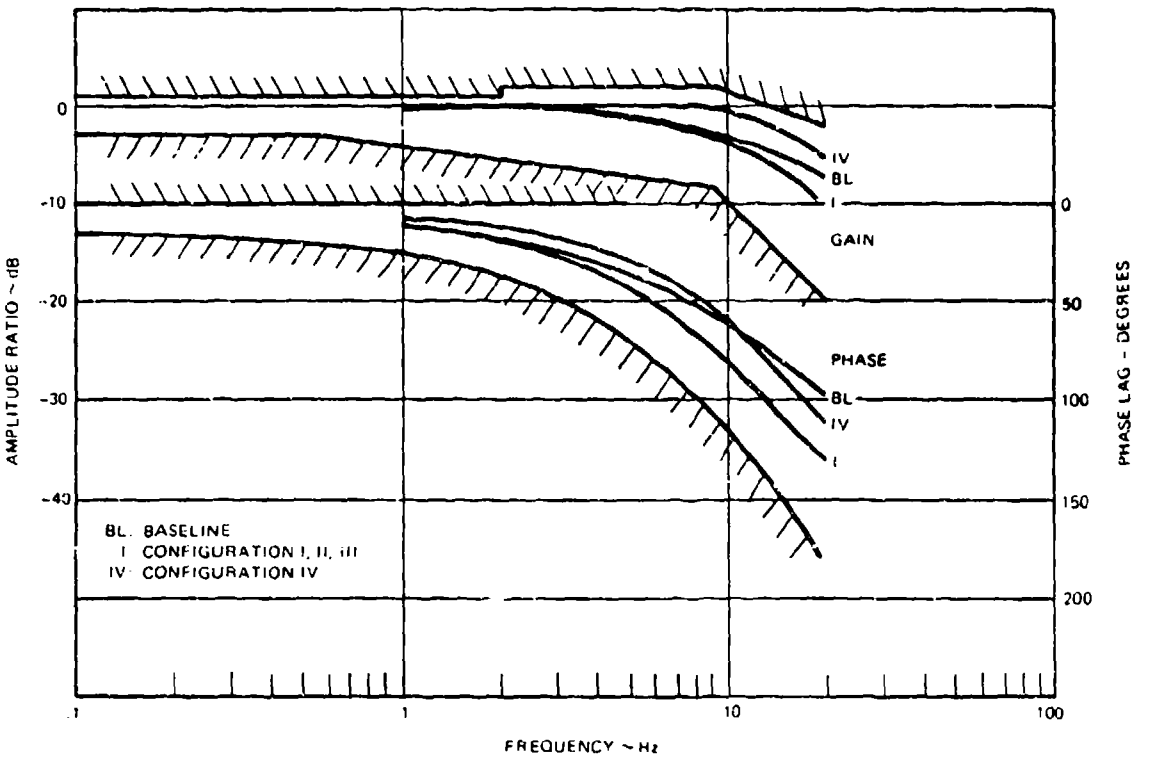


Figure 46. Configuration Comparison - Small Signal Frequency Response

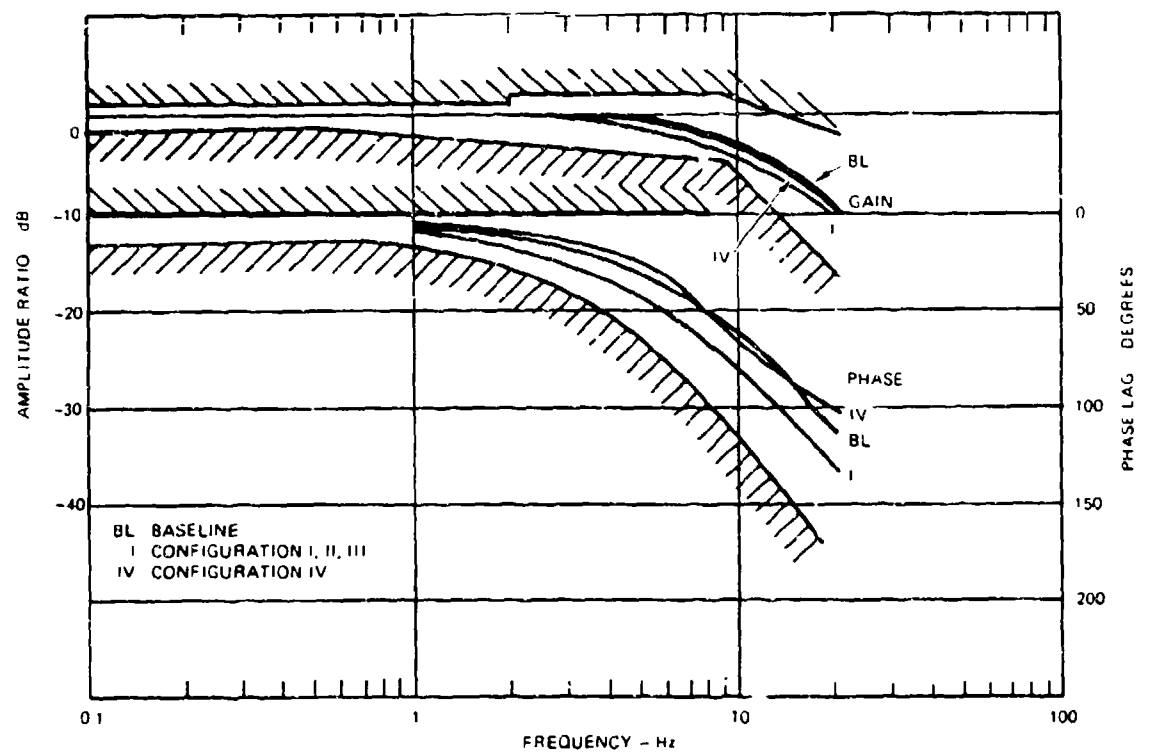


Figure 47. Configuration Comparisons - Large Signal Frequency Response

Configuration III vs. I - A performance analysis at elevated temperatures (250°F) was conducted on Configuration III electronics. A slight degradation in frequency response was observed when the performance of the electronics was derated for operation at 250°F (figure 48). However, at 75°F, no degradation overall of Configuration III was noted.

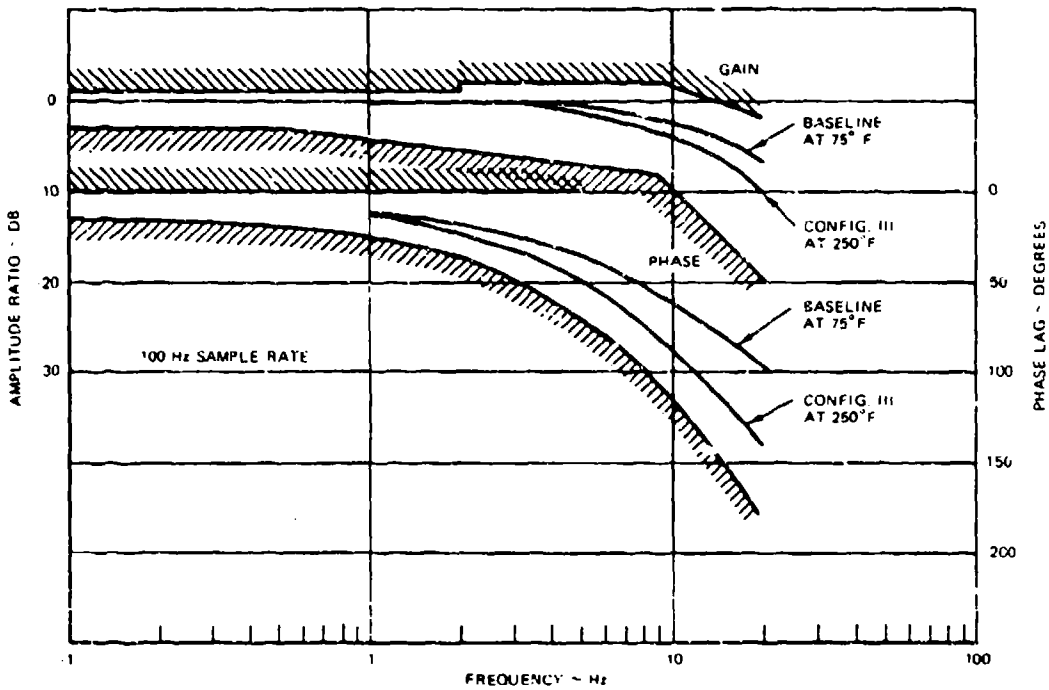


Figure 48. Configuration III, Small Signal Frequency Response

Configuration IV vs. I - Configuration IV's microprocessor in the servo processor added an additional sampling delay in the control loop to that of the digital control processor. However, its sampling rate can be set independently from that of the control processor. All performance specifications were essentially identical for the inner loop, except for small overshoot in step response. Evaluation of the outer loop was not included in the study.

Configuration V vs. I - In this configuration, the actuator control loop was commanded by a staircase, or discontinuous function, as with Configuration I, but in this case the position feedback was of a similar characteristic. A time-history plot of a ramp input is shown in figure 49. It was not necessary to add the notch filter since the

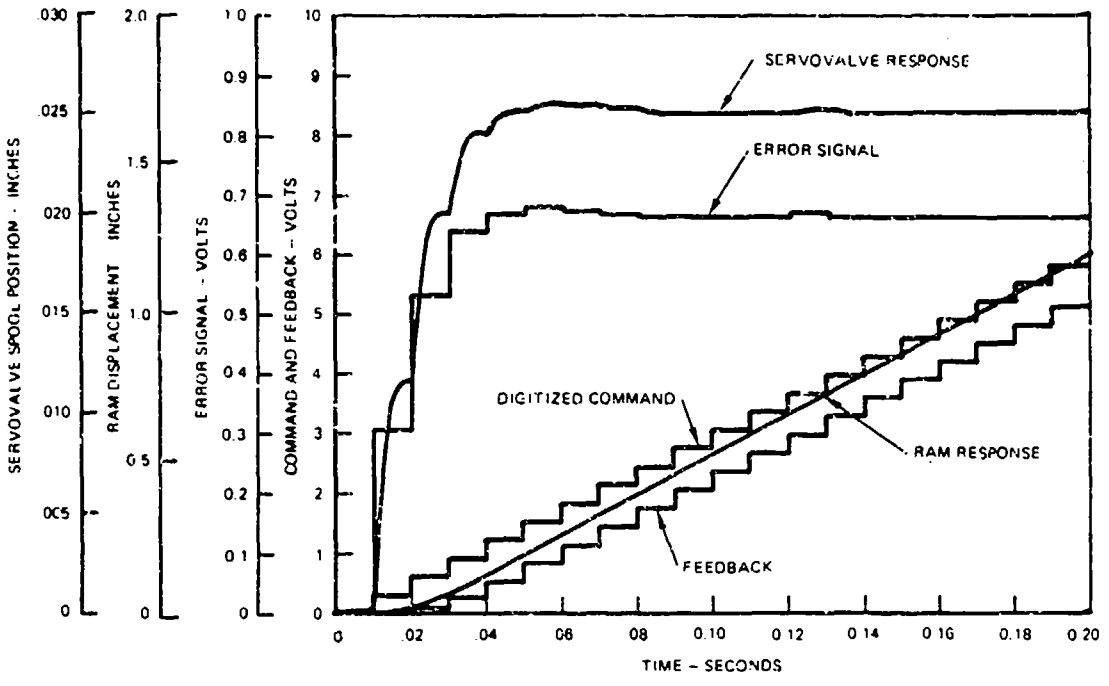


Figure 49. Effects of 100 Hz Sample Rate on Unfiltered Ramp Input

sampling rate of the position transducers were synchronized with that of the command signal. With the mechanization studied, an increase in frequency response was attributed to the way in which feedback from the transducer was implemented. However, a slight overshoot in step response and failure transients was also observed. The interaction of discontinuous command feedback signals has effects which required further study.

B. PHYSICAL COMPARISONS

Estimates of factors affected by the physical design are presented in table 2. Detailed analysis of the baseline is presented in Appendix B. It should be noted that this analysis does not include the control processor. However, the control processor's functions may be significantly reduced as servo processor functions increase.

Configuration I vs. Baseline- Notch filters and digital-to-analog converters were added to the servo processors. Dual parallel buses were exchanged for motherboard interwiring. This increased the component count of the servo processor by an estimated 9%, however, because of digital implementation of the control processor, the overall complex of control processors and servo processors represents a distinct improvement in total component count, reliability, flexibility, and capability.

Configuration II vs. I - No change was required functionally. There is a 10% increase in component count in the servo processor due to conversion from a dual parallel bus structure in Configuration I to a MIL-STD-1553B serial data bus in II. This component count increase is the reason for the similar small increases in cost, weight, and

TABLE 2. SERVOACTUATOR SYSTEM PHYSICAL CHARACTERISTIC SUMMARY PER ACTUATOR

CHARACTERISTIC		BASELINE	CONF. I	CONF. II	CONF. III	CONF. IV
COMPONENT COUNT (%)		100	109	119	186	205
COST ($)	SERVO PROCESSOR	10K	10.5K	12K	36K	48K
	SYSTEM	44K	45K	46K	70K	82K
WEIGHT (lbs)	SERVO PROCESSOR WIRES AND BUSES	493	496	505	225	230
	SYSTEM	1093	1096	1105	825	830
RELIABILITY	SERVO PROCESSOR	$50X10^{-6}$	$55X10^{-6}$	$80X10^{-6}$	$125X10^{-6}$	$867X10^{-6}$
	SYSTEM	$1.39X10^{-9}$	$1.41X10^{-9}$	$1.50X10^{-9}$	$1.72X10^{-9}$	$1.34X10^{-9}$
POWER (VA)		693	713	722	794	1030

decrease in reliability. Depending on the location of the servo processors, a significant weight reduction is possible by virtue of serial bus substitution for aircraft group A wiring.

Configuration III vs. II - No change is required functionally. There is a 56% increase in component count over Configuration II. This increase is due to three factors which come into play when servo processors are grouped by 12 groups of three (Configuration III) rather than three groups of 12 (Configuration II). Configuration III requires a power supply and a MIL-STD-1553B serial bus interface unit for each servo processor. (In Configuration II, one power supply was required for 12 servo processors and a dual parallel bus fed the servo processors from one serial bus interface.) In addition it was assumed that linear components capable of meeting actuator-location temperatures were available, but at premium prices. Costs therefore increased by 52% overall, but weight decreased by 25% overall, due principally to the substitution of serial data bases for 49 aircraft group A wires per surface, or 588 total.

It should be recognized, however, that Configuration III would actually be designed and produced in hybrid microelectronic technology wherein component count and reliability would be calculated based on MIL-HDBK-217C for hybrid microelectronic circuits - a significant improvement in reliability.

Configuration IV vs. III - Component count increased by 10% (including dual microprocessors) due to the introduction of a voting plane in the servo processors located at the actuator. The effect was to increase overall channel costs by 17% (86% over baseline). However, a significant increase in reliability was achieved from 1.72×10^{-9} for Configuration III to 1.34×10^{-9} for IV.

Configuration V - Configuration V is an all-digital configuration. Forward loop digital-to-analog conversion takes place in the flux-summing of the binary digital servovalve torque motor.

Analog-to-digital conversion in the position feedback loop takes place in the linear motion-to-binary readout of the encoder. Its feasibility is based on the development of a digital encoder and a digital valve. The feasibility of this development is not functional but rather physical and economic.

Size, weight, and cost factors dictate digital-to-analog or analog-to-digital conversions at the lowest possible power and simplest mechanical levels. Thus, Configuration V is not expected to be competitive with configurations which perform these conversions electronically and by flux summing, respectively. (See Section III, "Digital Mechanization of Servoactuator Elements.)

SECTION VI
OVERALL FINDINGS AND CONCLUSIONS

In Section III the design issues were discussed in detail. This was followed by a detailed description of the con igurations in Section IV and their comparisons in Section V. This section will describe the findings of these sections in terms of both the issues and the configurations. Recommended configurations for today's technology and for future technology are provided under conclusions.

A. FINDINGS

Performance - All configurations (I-V) were theoretically able tc match the performance requirements of the baseline. All physical components were not, however, readily available. Thus, some failed to meet physical, cost, and multiple source requirements.

Redundancy Architecture - The active-on-line system analyzed in these configurations lends itself to a concept of in-line failure detection throughout. Distributed servo processors are able to effectively monitor the failure status of the control processor, the interconnecting data bus, and the servcactuator complex. Failure and reconfiguration communications between channels can be readily handled between servo processors by dedicated wires when they are located at the actuator (Configuration III), but become a tradeoff between that approach and using the data bus between control processors, in Configuration II.

Configuration IV provides an insight which is important to cross-channel monitoring systems (e.g., forcesharing). This is a voting or switching plane at the actuator, employing microprocessor chips in the servo processors. This feature, while increasing component count by 10% over Configuration III, improved system reliability over Configuration III by 22%. It also has an advantage in reducing the vulnerability of the bus distribution system to battle damage. However, it has a

disadvantage in complicating the in-line failure detection logic of the active-on-line concept.

This study of configurations suggests that in overall flight control system redundancy architecture design, the integrated servo processor-actuator should be the future optimal point for actuation system failure monitoring.

Functional Distribution - Computational load in the control processor and simplified data bus interfaces between the control processor and servo processors are the two factors to be considered in deciding on where to perform the loop closure, failure detection, and redundancy management functions. By these rules, all these functions should be performed in the servo processor.

Physical Distribution - Physically it was noted that the most significant difference in the actuation configurations appeared in Configuration III where weight (for one channel of three servo processors plus actuator) decreased by 25%, due principally to reduction in aircraft group A wiring.

Other factors which favor Configuration III are its potential for providing interference-free signals to the actuators as well as providing a "smart actuator." This concept, by providing the actuator with a "functional completeness," yields a simpler interface. This, in turn, provides:

- Simpler fault isolation to an actuator LRU
- Simple procurement specifications
- Potential for standardization
- A trade of 588 aircraft wires for a serial data bus system - an aircraft weight savings estimated at 450 lb

- Reduction of servo loop noise

- Improved dispersement and simplification for battle damage avoidance and repair

- A potential for long-term improved performance at lower cost through a multidisciplinary technology (electronic-hydraulic-mechanical) approach to the actuation function.

Data Bus Format, Protocol, and Application - The MIL-STD-1553B serial data bus was able to handle all channel traffic between the 12 servo processors and their control processor pairs. When all functions of loop closure, failure detection, and redundancy management are performed in the servo processor, MIL-STD-1553B is a distinct overkill in terms of complexity and cost.

For distributed control loop applications requiring high iteration rates (100 Hz) the MIL-STD-1553B is not recommended for the following reasons:

- Protocol is data word-limited due to its high overhead-to-data-word ratio of approximately 1 to 1 for control loop applications.

- Hardware is too complex for the limited space available at the actuator and cannot withstand the high temperature environment.

High-Temperature Electronics - This technology involves three developments all of which are now available:

- I^2L semiconductor technology capable of 10^{-9} system failure rates at 200°C.

- High temperature packaging, employing eutectically mounted semiconductor chips in a hybrid microelectronics packaging concept.

- Digital switching circuit design concepts to avoid internal heat generation.

The availability of high-temperature electronics completes the process initiated by the microprocessor (functional distribution), and the digital serial data bus (physical distribution), allowing the development of the smart actuator.

Digital Servoactuation Elements - In Configuration V, digital electrohydraulic valves driving analog actuators were considered. A parallel binary servovalve driven by a microprocessor register through current drivers involves extensive parallel wiring if digital transducer encoders are also employed. A preferred approach is pulsewidth modulation of electrohydraulic servovalves, providing performance equivalent to the baseline system. This approach can be coupled with the use of similar digital circuit techniques to excite and demodulate flux-summing LVDT's. Employing newly developed high-temperature electronics to allow locating the servo processor circuits at the actuator offers the best present solution to a digital actuation system.

In general it was found that digital-to-analog conversions are most efficiently performed (weight, volume, cost) at the lowest possible power and simplest mechanical levels, thus ruling out digital actuators. Stepper motor systems do not have frequency responses in the range of servohydraulic systems for flight control applications with high force levels. Since the baseline system requirements of this study could not be satisfied with a stepper motor, it was not pursued.

With respect to pressure and position transducers it also appears that flux-summing may be a more efficient process than optical-mechanical techniques. Technology surveys have shown there to be

several digital circuit techniques available which are compatible with flux-summing transducers.

Digital Sampling Rate - The results of this analysis suggest that a minimum frequency criteria can be established based on several performance factors. These factors are compensation required to alleviate excessive wear of valves or fatigue of hydraulic lines while maintaining performance requirements of the actuator system. The rate selected was 100 Hz. If the data bus is shared and the sampling rate of other systems is to be considered, it would appear that the rule-of-thumb minimum sample rate should apply. This is at least five times the actuator band pass (9 Hz) or 45 Hz.

As suggested in Configuration V, the use of a microprocessor in the servo processor, or switching circuit techniques (PWM) for driving the servovalve with similar techniques for the LVDT's, can provide digital summing - a technique which may eliminate the need for a notch filter.

Servo Processor Configuration - Over the range of configurations, it was found that the analog circuits, which interface with the analog actuation elements, remained fairly constant, and changes in the servo procesor were due to the requirement to condition incoming signals by adding front-end circuits such as (1) serial data bus interface circuits (2) digital-to-analog circuits, and (3) notch filters.

These analog circuits are fairly standard for existing servo valves, feedback transducers and for given redundancy schemes, although many performance, maintainability, and cost-saving tradeoffs are possible when the design of the servo processor is in the same house as that of the actuator itself.

However, when the servo processor and actuator are integrated as in Configurations III and IV, some distinct changes are possible leading to a higher use of digital techniques, and requiring the introduction of semiconductor technology capable of high operating temperatures.

The first of these is in Configuration III where digital switching techniques would be substituted for the analog circuits, still permitting the use of standard analog servo valves, feedback transducers, and actuators without any penalty to system performance. (Note that in the configuration studies, Configuration III employed analog circuits, since digital switching circuits developed on HR Textron internal R&D funds are in the process of patent application.)

An architecture, not considered in the configuration studies, is the use of the microprocessor, as in IV, but with the analog actuation elements of III. This configuration is a major change in the redundancy management scheme and has possible major system advantages for force-sharing redundancy management schemes.

B. CONCLUSIONS

- In a digital flight control system, digital-to-analog conversion, required in the actuation subsystem, can be most effectively and efficiently made when it is accomplished in the servo processor.

- High temperature semiconductor technology permits locating the servo processor circuits at the actuator in a digital configuration, hence future designs could have the electronics integrated with the actuator. The only limitations to the design of an integral electronics actuator is the capability of the electronics to withstand the environment.

- Semiconductor technology, capable of providng system reliability of 10^{-9} failures/hour at junction temperatures of $200^{o}C$, has been developed on a government sponsored program.

- The use of digital switching techniques in the servo processor permits the use of standard linear (analog) servo valves and feedback transducers without any penalty to system performance. This is of particular value since R&D programs for digital servovalves, actuators, and transducers have not been successful, nor have they produced any useful hardware for this type of application.

- The advantages to be derived from an integral electronics actuator are summarized in Table 3, page 110. With a microprocessor incorporated, the resulting "smart actuator" includes a potential for new redundancy management concepts.

- Sufficient technology has been derived and generated on this program to allow the design and fabrication of digital actuation equipment that could demonstrate the validity of the analytical results of this program.

TABLE 3. ADVANTAGES OF A "SMART", ACTUATION SYSTEM

- SYSTEM PERFORMANCE
  - IMPROVED PERFORMANCE
  - COORDINATED ENGINE AND FLIGHT CONTROL
  - FLEXIBILITY AND MULTIMODE CONTROL AND RECONFIGURATION ON FAILURE
  - IMPROVED CHECKOUT AND SELF-MONITORING FOR FAILURE ASSESSMENT AND CORRECTION
  - COMPENSATION FOR DEGRADATION
- EQUIPMENT
  - MULTITECHNOLOGY APPROACH TO PRODUCT IMPROVEMENT
  - RELIABILITY ADVANTAGES OF DIGITAL CIRCUITS
    - LOW POWER CIRCUITRY
    - ARRAY DEVELOPMENT POTENTIAL
  - INTEGRATED ELECTRONIC FAILURE DETECTION CIRCUITS
  - ORDER-OF-MAGNITUDE REDUCTION IN WIRING
  - MANAGEABLE EMI, EMP CONFIGURATION
- PROCUREMENT
  - SIMPLIFIED INPUT-OUTPUT SPECIFICATION
  - REDUCTION IN INTERFACE PROBLEMS
  - SIMPLIFIED ASSIGNMENT OF VENDOR RESPONSIBILITIES
- MAINTENANCE, LOGISTIC SUPPORT OF ACTUATION SUBSYSTEM
  - AUTORIGGING OF SYSTEM
  - SELF CALIBRATION, SELF ADJUSTMENT OF NULLSHIFTS
  - ADJUSTMENT FOR OUT-OF-TOLERANCE CONDITIONS
  - DEPOT-LEVEL DIAGNOSTICS AT FLIGHT-LINE
  - REDUCTION IN TEST EQUIPMENT

- No insurmountable problem exists in the area of digital actuation that cannot be solved if sound engineering practices are used.

SECTION VII
RECOMMENDATIONS FOR FUTURE DEVELOPMENT

The R&D programs recommended to achieve and optimize a digital actuation system, in the order of priority, are as follows:

- a program to design an actuator which would have the servo processor as an integral part. Hybrid mi oelectronic packaging techniques and high temperature electronic semiconductors would be included in this design.

- a program to design, construct and test a flight worthy "smart actuator" in order to demonstrate the unique concepts that have been derived. Included in this design would be requirements for small volume, low power, and a high temperature capability.

- a study program to develop standards for serial busses, including format and protocol, optimized for control loop applications. These would be applicable to all types of military aircraft.

- a study program to determine the improved reliability and redundancy requirements of flight control system architectures using "smart actuator" concepts.

APPENDIX A

FLIGHT CONTROL ACTUATION SYSTEM SPECIFICATIONS

TABLE A-1. SYSTEM SPECIFICATIONS

HYDRAULIC PRESSURE	– 3000 psi STATIC – 85 psi RETURN 2500 psi DYNAMIC – 500 psi RETURN
OUTPUT FORCE	– 13,100 lb. COMPRESSION 13,000 ±250 lb. TENSION
OUTPUT RAM VELOCITY	– 6.70 ins./sec. @ 2000 psi EXTEND AND RETRACT
ACTUATION DEVICE STROKE	– ±2.25 inches
LOOP GAIN	– 40 rad/sec/@ 2900 psi
FREQUENCY RESPONSE	– NOMINALLY -3 dB AT 9 Hz (SEE FIGURES A-1 AND A-2 FOR LIMITS)
HYSTERESIS	– 0.1% OF RAM STROKE
THRESHOLD	– 0.05% OF RAM STROKE @ 0.1 Hz
NULL BIAS	– 0.25 ma.
DIGITAL SAMPLING RATE	– 100 Hz
BACKLASH	– 0.002 in.
FAILURE TRANSIENTS (NO INPUT SIGNAL AND NO LOAD)	– 1ST FAILURE -8% OF FULL STROKE 2ND FAILURE -8% OF FULL STROKE 3RD FAILURE -16% OF FULL STROKE
SURFACE LOAD	– I = 1.80 SLUG ft^2 K = 1.35×10^6 in-lb/rad
OUTPUT POSITION TRANSDUCER	– 5 VRMS @ FULL SCALE 0 - 15° LEADING PHASE SHIFT
SERVOVALVE	– 8 ma. – 1000 ohms
BYPASS VALVE	– @ 300 psi – BLOCK VALVE CYLINDER PORTS AND INTERCONNECT RAM PORTS @ 400 psi – OPPOSITE TO ABOVE
SOLENOID VALVE	– NORMALLY OFF POWER – 0.4a @ 24 VDC
ACTUATION DEVICE WEIGHT	– DRY WEIGHT – 18 lbs. MAX.
SERVOELECTRONICS WEIGHT	– 32 lbs. MAX.
RELIABILITY (SERVOACTUATION SYSTEM)	– PROBABILITY OF FAILURE PER 10 HOUR MISSION 2.0×10^{-9}
TEMPERATURE	AMBIENT AIR TEMPERATURES • -65°F TO 160°F CONTINUOUS • 220°F FOR 10 minutes • 240°F FOR 2.5 minutes HYDRAULIC OIL TEMPERATURES • -40°F TO 275°F SYSTEM OPERATING TEMPERATURE • -40°F TO 250°F
ALTITUDE	– TO 70,000 ft @ 40,000 ft./min.
EMI SPIKES	– DC + 50 TO -150% NORMAL AC + 50% NORMAL

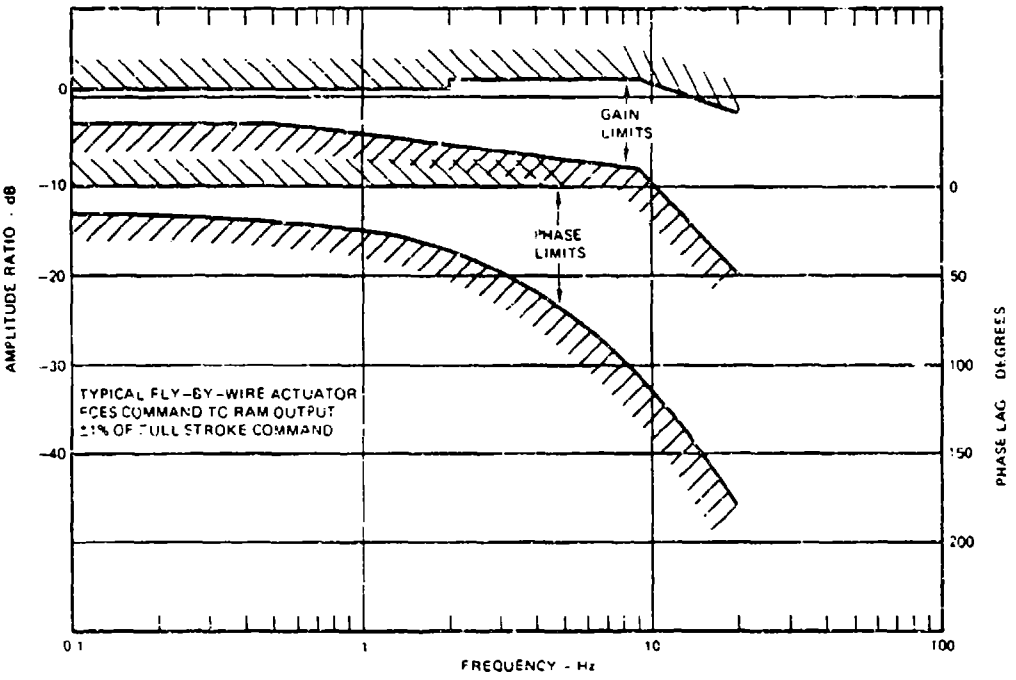


Figure A-1. Small Signal Frequency Response Limits

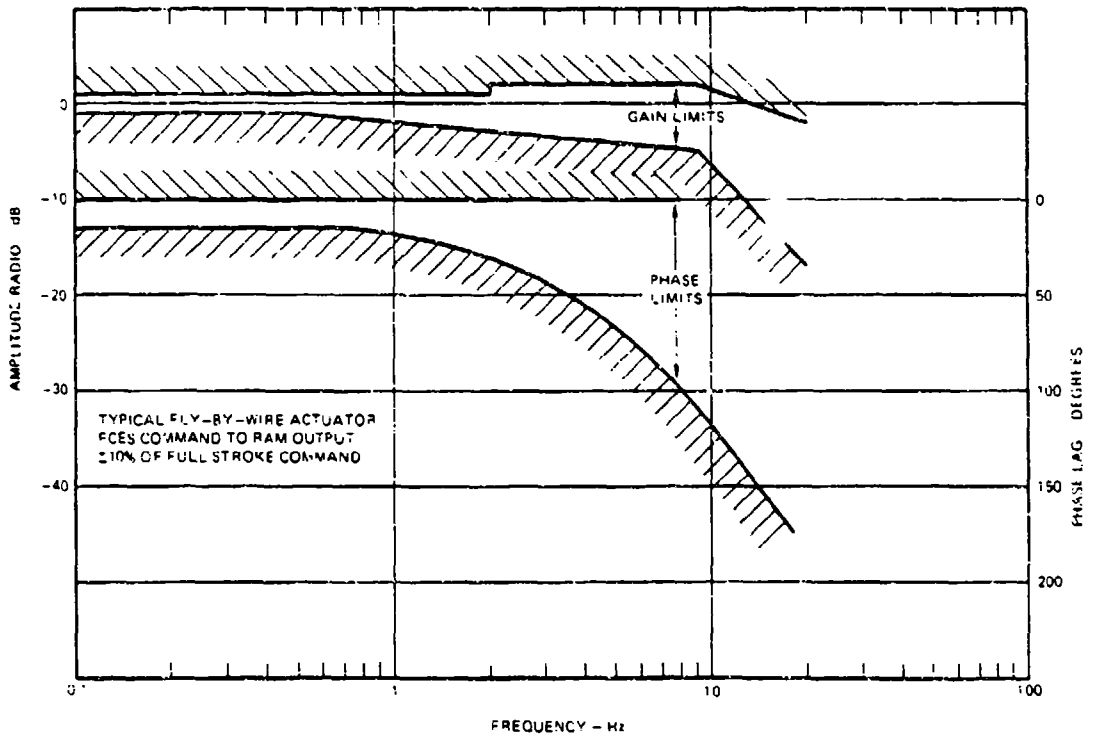


Figure A-2. Large Signal Frequency Response Limits

APPENDIX B

BASELINE CONFIGURATION CHARACTERISTICS AND PERFORMANCE

1. Performance Characteristics

Frequency Response

Small and large amplitude (1 percent and 10 percent of ram full stroke) frequency response runs were made utilizing the dynamic model. The results shown in figures B-1 and B-2 indicate that the frequency response meets required limits (nominally -3 db at 9 Hz).

Step Response

Figure B-3 shows the step response of the system for a 5 percent of full stroke input and demonstrates that the system exhibits excellent positional stability.

Failure Transients

Failure transient analyses were conducted to determine the effects of a hardover servovalve failure on the master and on-line channels. Since a hardover servovalve failure is the most severe servovalve failure, it is the only failure mode considered. The failures were induced with no input command applied to the control loop and no load applied to the control surface. The failure transients for the hardware servovalve failure, shown in figure B-4 indicated that the failure transients of 0.3, 1.2, and 9.0 percent respectively did not exceed the requirement of 8.0 percent of ram full stroke for the first and second failure and 16.0 percent of ram full stroke for the third failure.

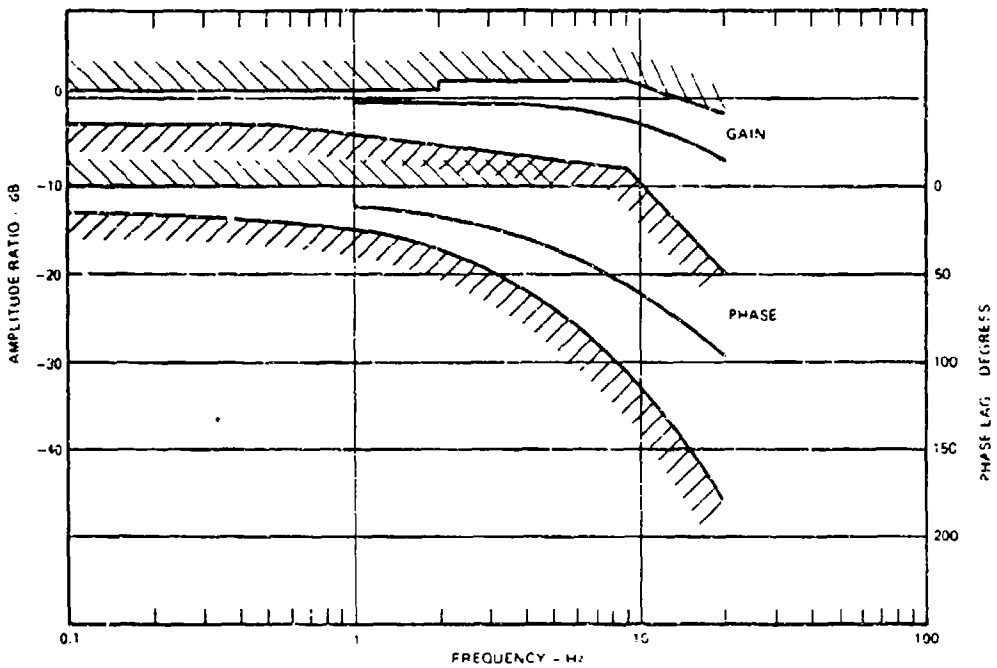


Figure B-1. Baseline System, Small Signal Frequency Response

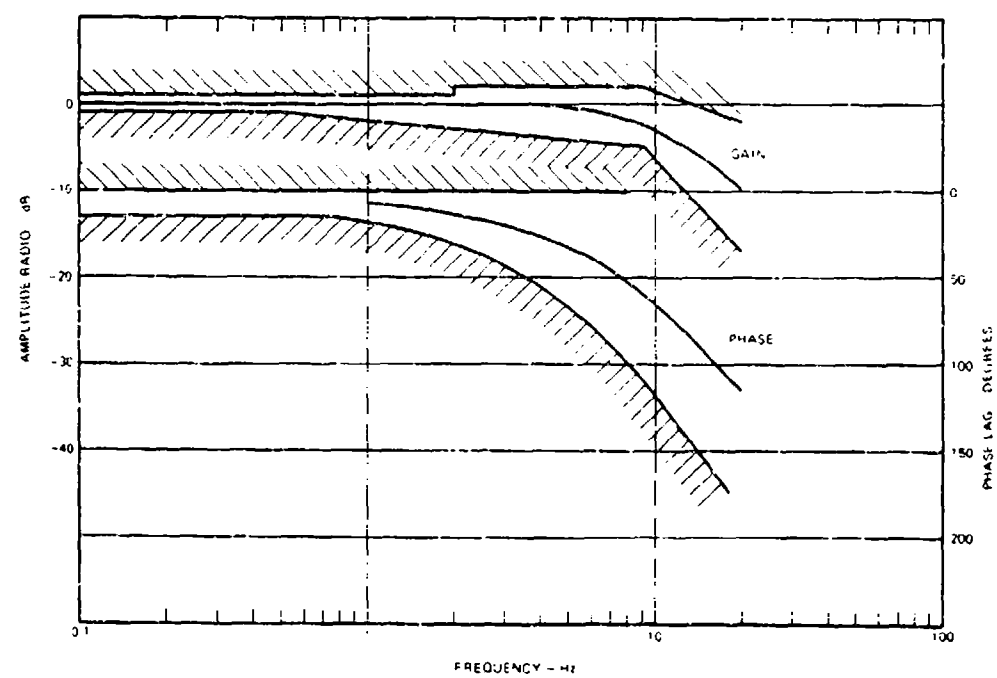


Figure B-2. Baseline System, Large Signal Frequency Response

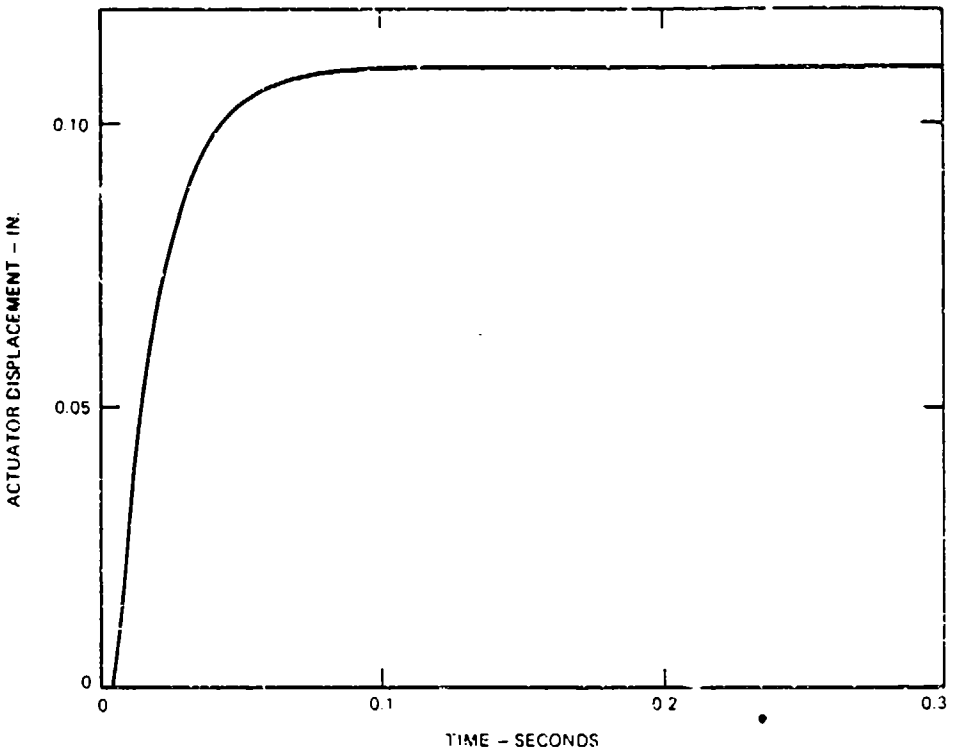


Figure B-3. Baseline System, 5% Step Response

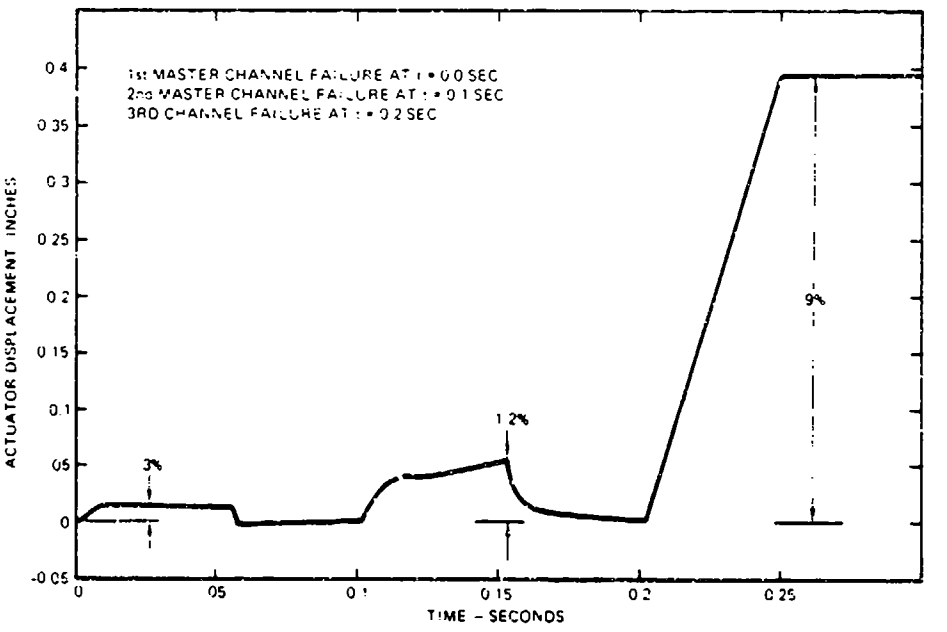


Figure B-4. Baseline System, Hardover Servovalve Failure Transients

Positional Accuracy

System accuracy is determined by analyzing the effects of the control loop component tolerances on the actuation device positional accuracy. The closed loop transfer function is written for the control loop and the component tolerances are treated as biases superimposed on the transfer function (denoted by an "X" in the figure B-5 equation). In considering the design issues for physical partitioning, only the servoelectronics change location and environment. For example, the servovalve is not included because it is the same for the baseline and configurations I through IV. The electronics were analyzed at an ambient temperature of 75 Deg. F.

As stated above, the actuation device positional accuracy is found from the steady state position equation defined in figure B-5. This equation is incorporated into a computer program which uses a random number generator routine to account for tolerance effects and a statistical routine for performing a statistical summary on the sampled population of 1000. Individual errors and tolerances are assumed to be normally distributed. The results show that the maximum error is $\pm$0.32%

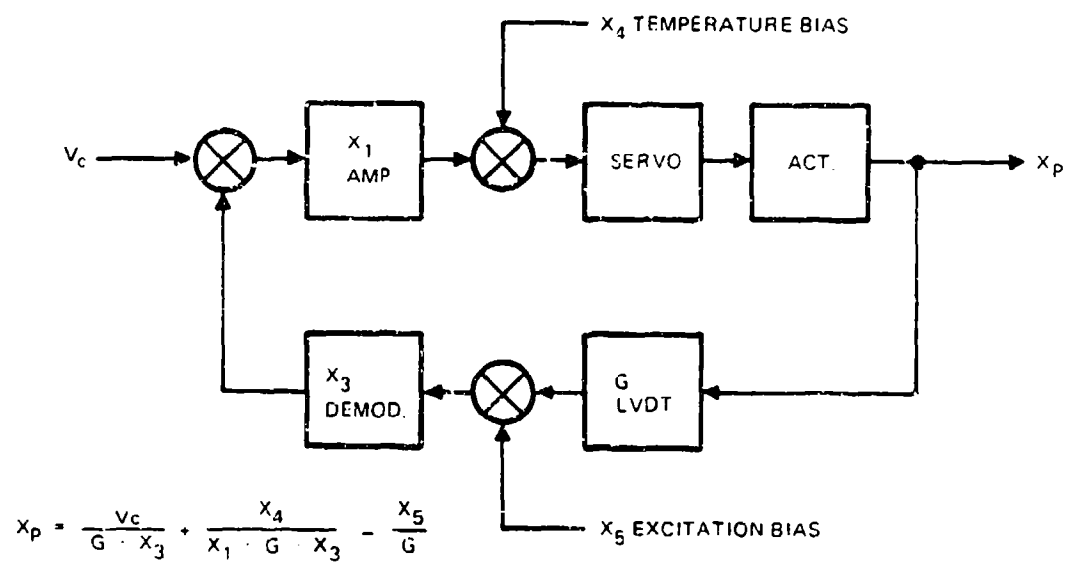


Figure B-5. Baseline System Steady State Position Equation

of full stroke and are summarized in terms of 99.7 percentile positional error, meaning that 99.7 percent of all samples will have a smaller value.

Nonlinearities, Dead Zone, Hysteresis, and Resolution

The nonlinearities, dead zone, hysteresis, and resolution of the baseline system were obtained by applying a 0.1 Hz sinusoidal input to the model and increasing its amplitude until main ram motion was observed. The resolution of the system is 0.035 percent of ram stroke, which is less than the requirement of 0.05 percent.

2. Physical Characterisitcs

Power

The power consumption of the major system elements is 54.2 Va for three (3) channels. The element break-down is shown in table B-1.

Environment

The system meets the specified operational temperature requirements which are:

System	-40 Deg F to 250 Deg. F
Hydraulic Oil	-40 Deg. F to 275 Deg. F
Ambient Air	-65 Deg. F to 160 Deg. F continuously 220 Deg F for 10 minutes 240 Deg. F for 2.5 minutes

Weight/Volume

The total weight of the servo processor, actuation devices, and associated cabling for three channels is 72.76 lbs. (See table B-2).

TABLE B-1. BASELINE SYSTEM POWER REQUIREMENTS

	SINGLE CHANNEL (Va)	THREE CHANNELS (Va)
SERVOVALVE (SV)	0.064	0.192
SV LVDT	0.1	0.3
RAM LVDT	0.1	0.3
ΔP LVDT (2)	0.1	0.2
SOLENOID (4)	9.6	38.4
SERVO AMP.	0.4	1.2
SV LVDT DEMODULATOR	0.3	0.9
RAM LVDT DEMODULATOR	0.3	0.9
MODEL RAM LVDT DEMODULATOR	0.3	0.9
RAM LVDT MONITOR (4)	0.2	0.8
ΔP LVDT DEMODULATOR (4)	0.3	1.2
ΔP LVDT MONITOR (2)	0.2	0.4
MODEL ΔP LVDT DEMODULATOR	0.3	0.9
SOLENOID DRIVER (4)	0.6	2.4
SWITCH DRIVERS (4)	0.1	0.4
EXCITATION	0.6	1.8
MODEL	0.3	0.9
GATE CIRCUITRY	0.2	0.6
COMPARATOR	0.3	0.9
LATCH	0.2	0.6
TOTAL	14.5	54.19

The servoelectronics volume for these channels is 120 cubic inches and the actuation device is 163 and 173 cubic inches with the piston retracted and extended respectively.

The baseline actuation device was designed for this study and is depicted in figure B-6. This design is based on the F-18 actuator with modifications to meet the weight/volume characteristics and to exclude components not application to the study. Three actuators are used in parallel.

Parts

The total number of parts for the three (3) channels is 63, comprised of the following:

TABLE B-2. WEIGHT SUMMARY IN POUNDS (BASELINE SYSTEM)

ACTUATION DEVICE	QTY	WEIGHT-POUNDS
ACTUATOR	3 @ 15.23	45.69
ACTUATOR LVDT	3 @ 0.61	1.82
BYPASS SOLENOID VALVE	3 @ 0.52	1.56
SERVOVALVE WITH LVDT	3 @ 0.90	2.70
DIFF. PRESS. TRANSDUCER WITH LVDT	2* @ 0.34	.68
	SUB-TOTAL	52.46
*NONE REQUIRED FOR CHANNEL A		
SERVO PROCESSOR	QTY	WEIGHT-POUNDS
POWER SUPPLY MODULES	3 @ 0.5	1.5
CARDS	9 @ 0.3	2.7
INTERCONNECT CARD	1	0.8
CHASSIS	1	1.0
CARD GUIDES, BRACKET, ETC.	1	1.0
	SUB-TOTAL	7.0
CABLING	SUB-TOTAL	13.3
	TOTAL	72.76 lbs.

Servo Processor	Actuation Device
4 Switch driver	3 Servovalve with LVDT
3 Servoamplifiers	3 Actuator with LVDT
3 Threshold detectors	2 Differential pressure transducers with LVDT
3 Solenoid drivers	3 Bypass solenoid valves
13 Demodulators	
12 Logic gates	11
3 Delay latch	
3 Excitation	
5 Monitor circuit	
3 Model	
52	

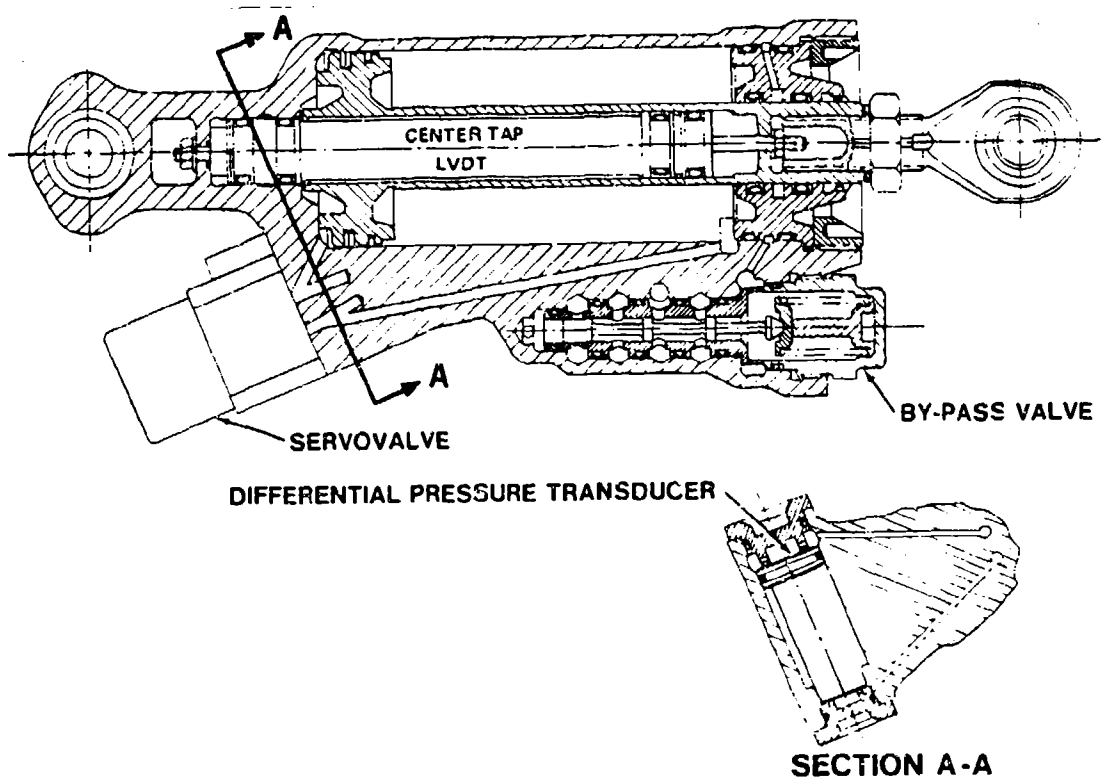


Figure B-6. Actuation Device

Cost/Availability

Based on 1980 dollars, the estimated cost of the three (3) channel system is $45,031.00. The cost breakdown is:

- Servoprocessor $10,500.00
- Cabling 481.00
- Actuation Device 34,050.00

It is concluded that the system would be readily available since current state-of-the-art components are used.

Bus Type/Wiring

Hardwiring is used to interconnect the elements in the baseline system. Thirty-two (32) wire pairs and five (5) triples are required for a total of 79 wires as follows:

Command to servoprocessor	- 3 pair
Servoprocessor to servovalve	- 3 pair
LVDT excitation (RAM)	- 3 pair
LVDT secondary to electronics (RAM)	- 3 triple
Electronics to solenoids	- 3 pair
SV LVDT excitation	- 3 pair
SV LVDT secondary	- 3 pair
Δp LVDT excitation	- 2 pair
Δp LVDT secondary	- 2 triple*
28 VDC	- 3 pair
Computer channel fail	- 3 pair
Δp/FB disable	- 3 pair*
Actuation device fail	- 3 pair

All wiring is 26 AWG shielded twisted pair with two (2) exceptions. The power supply wires are 16 AWG shielded twisted pair and the Ram LVDT and the differential pressure LVDT wires are 26 AWG shielded twisted triple conductor.

The following criteria were used to estimate the weight of the wiring in the system:

Wire Type		lb/1000 ft.
26 AWG	Shielded twisted pair	14.11
26 AWG	Shielded twisted triple	18.52
16 AWG	Shielded twisted triple	41.37

*Channel C has redundant Δp FB disable lines.

Noise

The system is capable of operation under the following types of power spikes:

DC: +50% to -150% of normal
AC: +50% of normal

Shielded twisted pair and triple conductors were selected to minimize internally and externally generated EMI effects.

Reliability

A redundancy management model for predicting failure rates was developed for the baseline. This model was used to design the servo-actuation system to achieve the required reliability of 2×10^{-10}/hr. The system has three parallel channels with failure detection in each channel and the ability to transfer control to a healthy channel, hence, the "system failure rate" (probability of system loss for a one hour mission) is several orders of magnitude smaller than the failure rate for each channel.

Three single point failures have been identified as follows:

Ram - Stuck
Bypass Valve Spool - Moves to bypass position
Command Signal Wires - Open or shorted

The design of these components is such that there is low probability of these failure modes. A failure rate of 10^{-13} and 10^{-14} are assigned to the first two items. The command signal wires are very short runs between cards and are located in the controlled environment of the control processor. A failure rate of 4.4×10^{-12} is assigned to these two wires.

There are several components which have an "undetectable" failure mode. This type of failure in Channel A is of great concern because it prevents the two fail operation. These items can be made redundant but for this study they were not in order to demonstrate that the Redundancy Management Model can predict the reliability and the effects of the thresholds.

The servoactuation system failure rate for the baseline is 1.42 x 10^{-10} per hour which is less than the requirement. The calculated mean time between failure (MTBF) was 6902 hours.

APPENDIX C

SERVOACTUATOR DYNAMIC ANALYSIS

An HR Textron Inc. developed nonlinear dynamic simulation mathematical model was used to analyze the performance of the various flight control system configurations. the model was used to evaluate dynamic performance in the following areas: system stability, transient step response (includes slew rate, overshoot, settling time), frequency response, resolution, and failure transients.

1. DYNAMIC SIMULATION MODEL

Figure C-1 shows a schematic illustration of the physical system used in the development of the nonlinear model, along with some of the significant parameters and variables. Figure C-2 is a block diagram illustration of the overall nonlinear simulation and table C-1 presents a description of the parameter constants used in the nonlinear simulation.

A detailed description of the nonlinear model is as follows:

a. Inputs

System transient input variables are command voltage and externally applied torque on the surfaces.

b. Initial Conditions

The simulation contains an "initial conditions" routine that solves for the initial steady state conditions of the system by iteration before the integration process begins. The initial conditions may include the effect of an initial command voltage, an externally applied torque on the surface and a servovalve static null bias.

c. Servovalve

Servovalve dynamics, illustrated in figure C-2 are simulated by relating input torque motor current to output spool position, using a second order linear differential

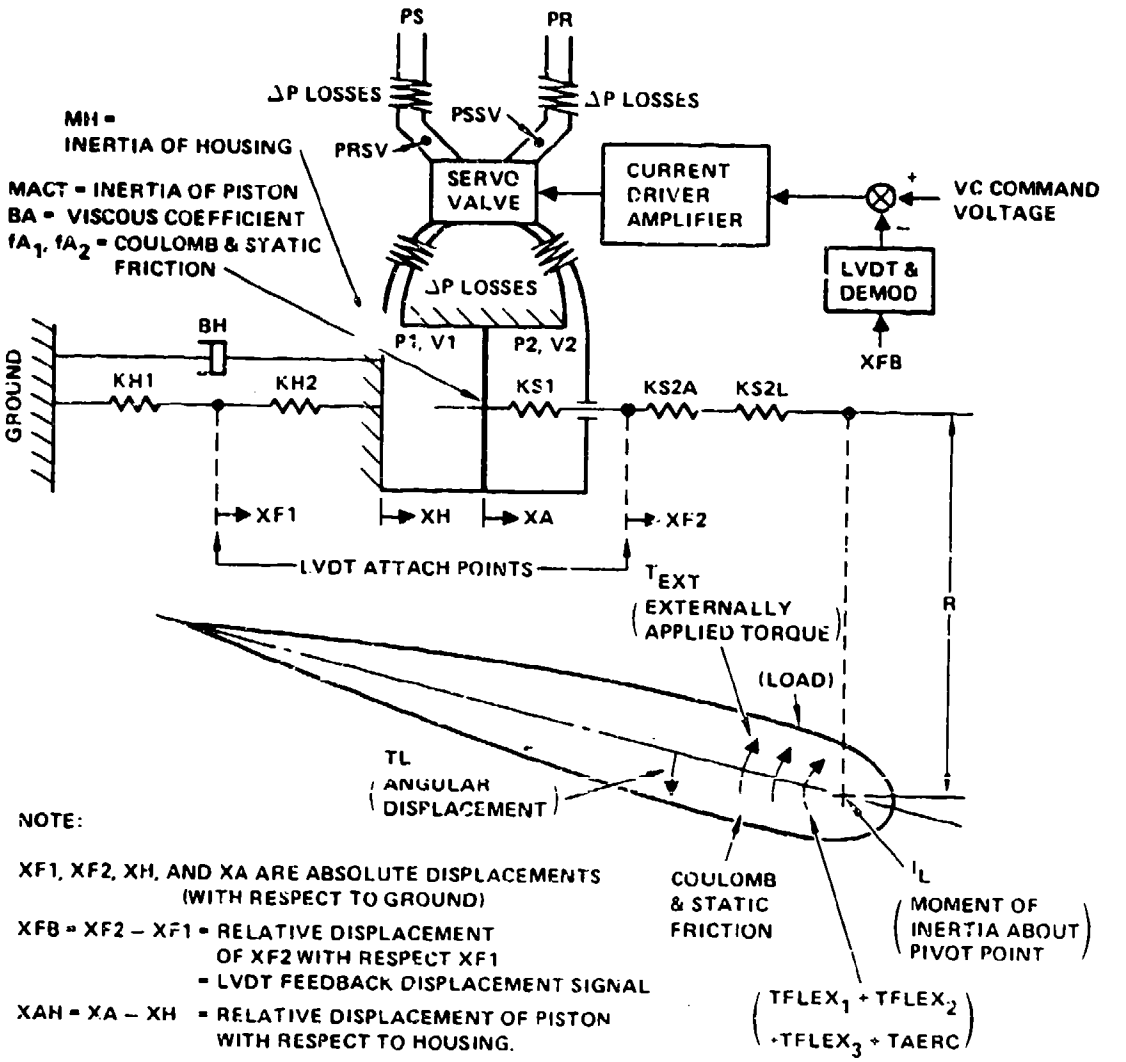


Figure C-1. Schematic Showing Lumped Parameter Representation of System for Nonlinear Dynamic Simulation

equation. The nonlinear effect of second stage saturation is simulated by limiting spool displacement and the first stage saturation is simulated by limiting second stage spool velocity. The effects of a static null bias on spool position and servovalve hysteresis are also simulated.

The servovalve second stage spool flows illustrated in figure C-3 are calculated in the nonlinear simulation at

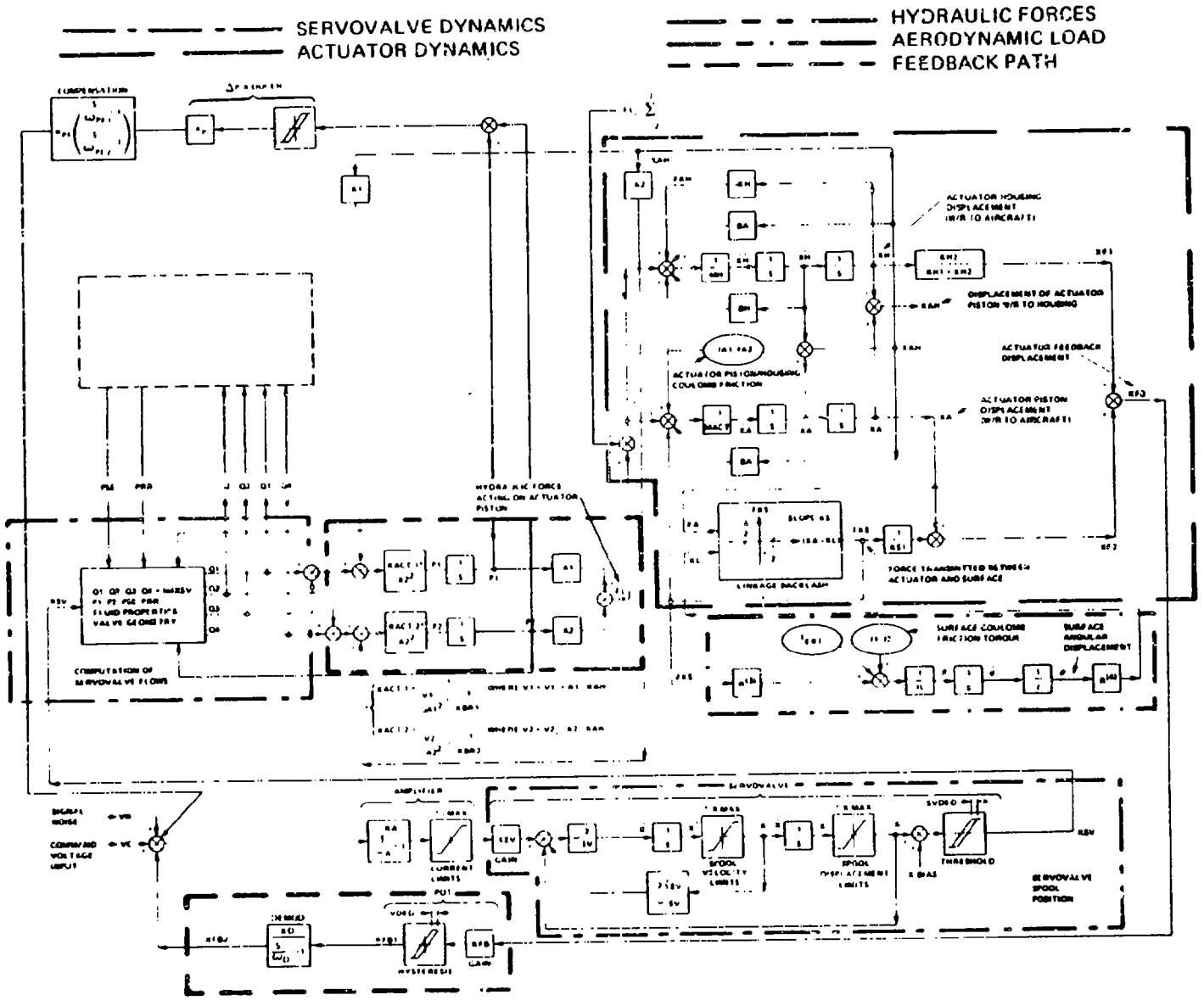
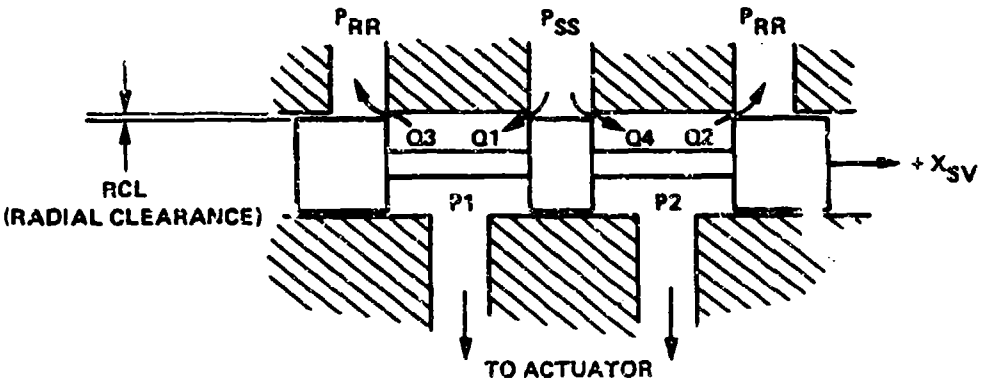


Figure C-2. Block Diagram of Nonlinear Simulation

TABLE C-1. DESCRIPTION OF PARAMETER CONSTANTS

SYMBOL	UNITS	DESCRIPTION
A1, A2	in^2	ACTUATOR PISTON EFFECTIVE AREAS, SIDES 1 AND 2
BA	lbf/sec/in	VISCOUS DAMPING COEFFICIENT, PISTON TO HOUSING
BH	lbf/sec/in	VISCOUS DAMPING COEFFICIENT, ACTUATOR HOUSING TO AIRCRAFT
f1	in-lbf	STATIC FRICTION TORQUE, SURFACE TO GROUND
f2	in-lbf	RUNNING FRICTION TORQUE, SURFACE TO GROUND
fA1	lbf	STATIC FRICTION, PISTON TO HOUSING
fA2	lbf	RUNNING FRICTION, PISTON TO HOUSING
IL	$in\text{-}lbf\text{-}sec^2$	SURFACE MOMENT OF INERTIA ABOUT PIVOT POINT
KA	ma/volt	AMPLIFIER GAIN
KBR1	lbf/in	ACTUATOR BREATHING STIFFNESS, SIDE 1
KBR2	lbf/in	ACTUATOR BREATHING STIFFNESS, SIDE 2
KD	v/v	DEMODULATOR GAIN
KFB	v/in	LVDT GAIN
KH	lbf/in	SERIES SPRING COMBINATION OF KH1 AND KH2
KH1	lbf/in	ACTUATOR HOUSING COMPLIANCE OUTSIDE LVDT ATTACH POINT
KH2	lbf/in	ACTUATOR HOUSING COMPLIANCE INSIDE LVDT ATTACH POINT
KP	v/psi	DIFFERENTIAL PRESSURE TRANSDUCER GAIN
KPF	v/v	PRESSURE FEEDBACK COMPENSATION GAIN
KS	lbf/in	SERIES SPRING COMBINATION OF KS1, KS2A, AND KS2L
KS1	lbf/in	ACTUATOR ROD COMPLIANCE INSIDE LVDT ATTACH POINT
KS2A	lbf/in	ACTUATOR ROD END COMPLIANCE OUTSIDE LVDT ATTACH POINT
KS2L	lbf/in	SURFACE COMPLIANCE BETWEEN SURFACE AND ACTUATOR
KSV	in/ma	SERVOVALVE SPOOL POSITION GAIN
MACT	$lbf\text{-}sec^2/in$	ACTUATOR PISTON + ROD END MASS
MH	$lbf\text{-}sec^2/in$	ACTUATOR HOUSING MASS
P1	psi	PRESSURE IN CYLINDER, SIDE 1
P2	psi	PRESSURE IN CYLINDER, SIDE 2
PR	psi	RETURN PRESSURE AT PUMP
PRSV	psi	SERVOVALVE RETURN PRESSURE
PSSV	psi	SERVOVALVE SUPPLY PRESSURE
QLK1	c·s	SERVOVALVE FIRST STAGE LEAKAGE FLOW
R	in	MOMENT ARM, SURFACE PIVOT POINT TO ACTUATOR CENTERLINE
TAERO	in-lbs	AERODYNAMIC LOAD
V1	in^3	OIL VOLUME AT NULL, SIDE 1
V2	in^3	OIL VOLUME AT NULL, SIDE 2
VS	in^3	OIL VOLUME, PUMP TO SERVOVALVE, SUPPLY SIDE
β	psi	BULK MODULUS OF HYDRAULIC OIL



Q1, Q2, Q3, Q4 = FLOWS THROUGH SPOOL/SLEEVE VALVE ORIFICES

= fn [XSV, P1, P2, SUPPLY & RETURN PRESSURES, FLUID PROPERTIES (DENSITY AND VISCOSITY), AND VALVE GEOMETRY (WINDOW WIDTHS & LENGTHS, SPOOL-SLEEVE CLEARANCE, SPOOL DIAMETER, OVERLAP AND/OR UNDERLAP LENGTHS)].

Figure C-3. Servovalve Spool Valve Flows

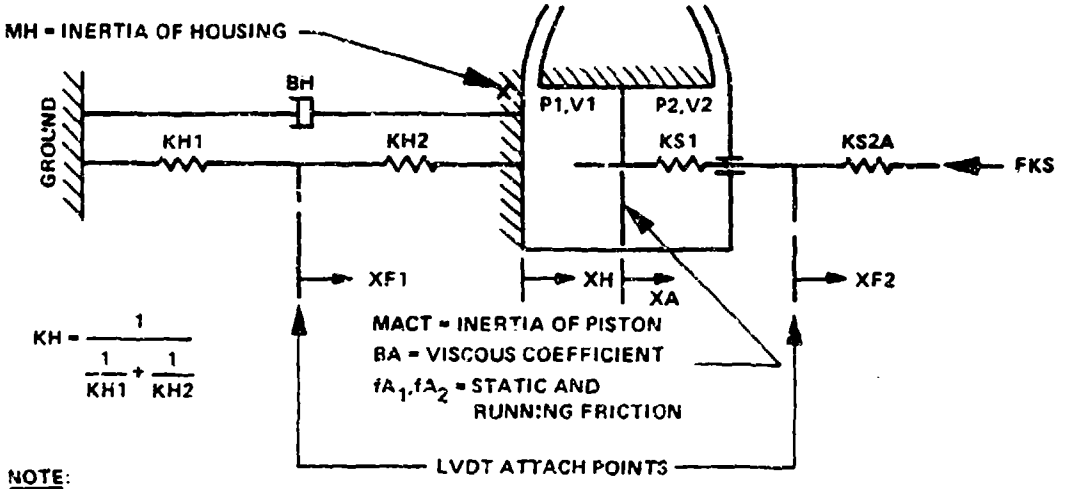
each increment in time as a function of spool displacement, the cylinder pressures, the supply and return geometry (i.e., window widths, window lengths, spool/sleeve clearances, spool diameter, overlap and/or underlap lengths). The method utilizes sharp-edged orifice equations and equations for flow between concentric cylinders, with entrance region effects taken into account. Reynolds number effects (i.e., laminar, transitional, and turbulent flow considerations) are accounted for.

d. Parasitic Pressure Losses

Parasitic pressure drops within the actuator passageways are simulated, as illustrated in figure C-4. The pressure drop coefficients were computed from a pressure drop analysis of the actual system, for various fluid temperatures.

e. Actuator

Compliances are distributed according to whether they occur inside or outside the LVDT attach points. The inertias of



$$KH = \frac{1}{\frac{1}{KH1} + \frac{1}{KH2}}$$

NOTE:

XF1, XF2, XH, AND XA ARE ABSOLUTE DISPLACEMENTS WITH RESPECT TO GROUND

$XFB = XF2 - XF1$ = RELATIVE DISPLACEMENT OF XF2 WITH RESPECT XF1 (1)

= LVDT FEEDBACK DISPLACEMENT SIGNAL

$XAH = XA - XH$ = RELATIVE DISPLACEMENT OF PISTON WITH RESPECT TO HOUSING. (2)

REGIME I, $\dot{XAH} \neq 0$ (ie, PISTON IS IN MOTION RELATIVE TO HOUSING)

A FORCE BALANCE ON THE ACTUATOR HOUSING GIVES

$$MH\frac{d^2(XH)}{dt^2} + BH\frac{d(XH)}{dt} + KH \cdot XH = -\sum_{i=1}^{3}(P1 \cdot A1 - P2 \cdot A2) + BA\frac{d(XAH)}{dt} \mp fA_2 \quad (3)$$

A FORCE BALANCE ON THE ACTUATOR PISTON AND ROD END GIVES

$$MACT\frac{d^2(XA)}{dt^2} = \sum_{i=1}^{3}\left(P1 \cdot A1 - P2 \cdot A2\right)_i - FKS - BA\frac{d(XAH)}{dt} \mp fA_2 \quad (4)$$

ELIMINATING THE VARIABLE XA FROM EQUATION 4 USING EQUATION 2, THEN SUBSTITUTING IN FOR THE SECOND DERIVATIVE OF X USING EQUATION 3 RESULTS IN

$$MACT\frac{d^2(XAH)}{dt^2} + BA\frac{d(XAH)}{dt}\left(1 + \frac{MACT}{MH}\right) = \left(FORCE_A \mp fA_2\right)\left(1 + \frac{MACT}{MH}\right) \quad (5)$$

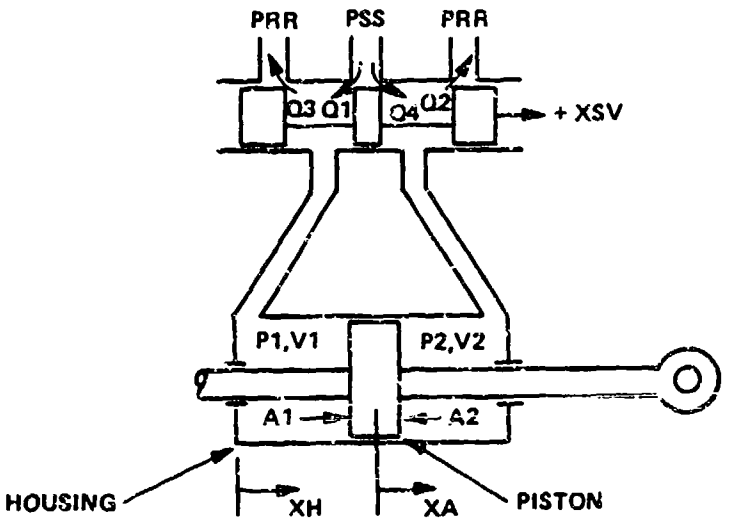
WHERE:

$$FORCE_A = \sum_{i=1}^{3}\left(P1 \cdot A1 - P2 \cdot A2\right) + \frac{-FKS + \frac{MACT}{MH}\left(KH \cdot XH + BH\frac{d(XH)}{dt}\right)}{1 + \frac{MACT}{MH}} \quad (6)$$

NOTE: THE SUMMATION FROM i = 1 TO 3 REFERS TO THE THREE FORCE-SHARING ACTUATORS

Figure C-4. Force Balance Equations for Actuator

the housing and the ram piston, and the coulomb friction between them, are simulated. The force balance equations applied to the actuator housing and piston are given in figure C-4. The result is two second-order differential equations, one for the displacement of the housing (XH) and one for the displacement of the piston with respect to housing (XAH). The application of the mass continuity relationships to the control volumes of fluid in the actuator cylinder chambers is illustrated in figure C-5.



XAH = XA − XH = DISPLACEMENT OF PISTON RELATIVE TO HOUSING

SIDE 1:
$$\frac{A1^2}{KACT_1}\,\frac{d(P1)}{dt} = Q1 - Q3 - A1 \cdot \frac{d(XAH)}{dt}$$

SIDE 2:
$$\frac{A2^2}{KACT_2}\,\frac{d(P2)}{dt} = Q4 - Q2 + A2 \cdot \frac{d(XAH)}{dt}$$

WHERE
$$KACT_1 \equiv \frac{1}{\frac{V1}{\beta A1^2} + \frac{1}{KBR1}} \qquad KACT_2 \equiv \frac{1}{\frac{V2}{\beta A2^2} + \frac{1}{KBR2}}$$

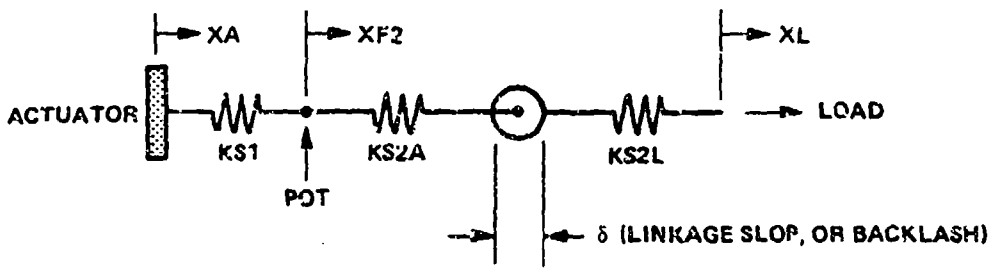
AND
$$V1 = V1t + A1 \cdot XAH \qquad V2 = V2t - A2 \cdot XAH$$

Figure C-5. Continuity Equations for Actuator Fluid Chambers

Fluid compressibility is accounted for. Thus, the continuity equations result in a first order differential equation for each cylinder pressure (P1 and P2).

f. Structural Backlash

Structural backlash or linkage free play between the actuator and the load is simulated. Figure C-6 shows the equations relating the force transmitted between the actuator and the load (FKS) and linkage free play.



δ = TOTAL BACKLASH IN LINKAGE

KS = TOTAL SPRING RATE = $\dfrac{1}{\frac{1}{KS1} + \frac{1}{KS2A} + \frac{1}{KS2L}}$

LET "FKS" BE THE FORCE TRANSMITTED BETWEEN THE ACTUATOR AND THE LOAD.

$$FKS = \begin{cases} KS\left[\left(XA - \frac{\delta}{2}\right) - XL\right] & \text{if } (XA-XL) > \frac{\delta}{2} \\ 0 & \text{if } (XA-XL) < \frac{\delta}{2} \text{ AND } (XA-XL) > -\frac{\delta}{2} \\ KS\left[\left(XA + \frac{\delta}{2}\right) - XL\right] & \text{if } (XA-XL) < -\frac{\delta}{2} \end{cases}$$

Figure C-6. Force Transmitted Between Actuator and Load

If the velocity d(XAH)/dt passes through or reaches zero at any time throughout the integration process, then "Regime II" is entered, described as follows:

Regime II: XAH = 0 (i.e., piston is in striction to housing)

A force balance on the actuator housing and piston combined gives:

$$(MH + MACT)\frac{d^2(XH)}{dt^2} + BH \frac{d(XH)}{dt} + KH \times XH = FKS$$

$$\frac{d^2(XAH)}{dt^2} = 0, \frac{d(XAH)}{dt} = 0$$

If the quantity "$FORCE_A$" defined on the previous page exceeds magnitude of the known breakaway friction force, then relative motion between the piston and housing will result, and "Regime II" described previously will be entered.

Additional Relationships (independent of which of the above 2 regimes the system is functioning within)

$$XF1 = \left(\frac{KH2}{KH1+KH2}\right) \cdot XH$$

$$XF2 = XA - \frac{FKS}{KSI}$$

$$XFB = XF2 - XF1$$

$$XAH = XA - XH$$

APPENDIX D
EFFECT OF 40 Hz AND 10 Hz SAMPLE RATES

As discussed in Section III, Configuration I was evaluated for a sample rate of 100 Hz. The same system was also subjected to analysis with sample rates of 40 Hz and 10 Hz.

The results of the 40 Hz analysis are shown in figures D-1 through D-4. As can be seen, the uncompensated servovalve dither is quite pronounced and if operated under this condition the servovalve would be subjected to undue wear. When a 40 Hz notch filter is inserted, the wear situation is essentially alleviated.

However, the notch filter introduces a significant amount of phase lag at the control frequencies and the frequency response plots of figures D-5 and D-6 indicate that the system response is below the specified limits.

At 10 Hz the situation becomes further aggravated as shown in figures D-7 through D-10. The frequency response becomes meaningless at frequencies higher than a theoretical value of 5 Hz. Practically, no meaningful data can be obtained beyond a frequency of 3 Hz and the response up to this value is shown in figures D-5 and D-6.

It is quite clear that the system response is definitely outside the allowable limits.

As indicated above the filtering was accomplished with a simple notch filter. Other filter configurations are available and the effect of one such filter is discussed below.

As indicated above, the performance of Configuration I at sample rates of 40 Hz and 10 Hz is unacceptable due to the fact that the filter required to suppress the servovalve dither degrades the systems frequency response.

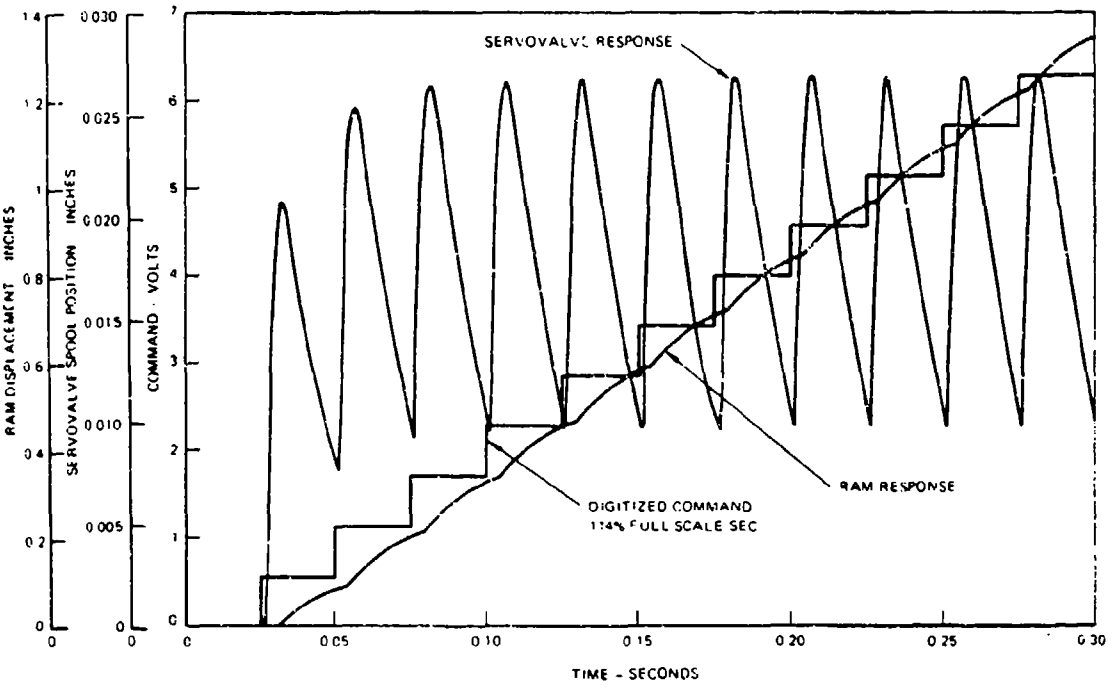


Figure D-1. Effects of 40 Hz Sample Rate on Unfiltered Ramp Input

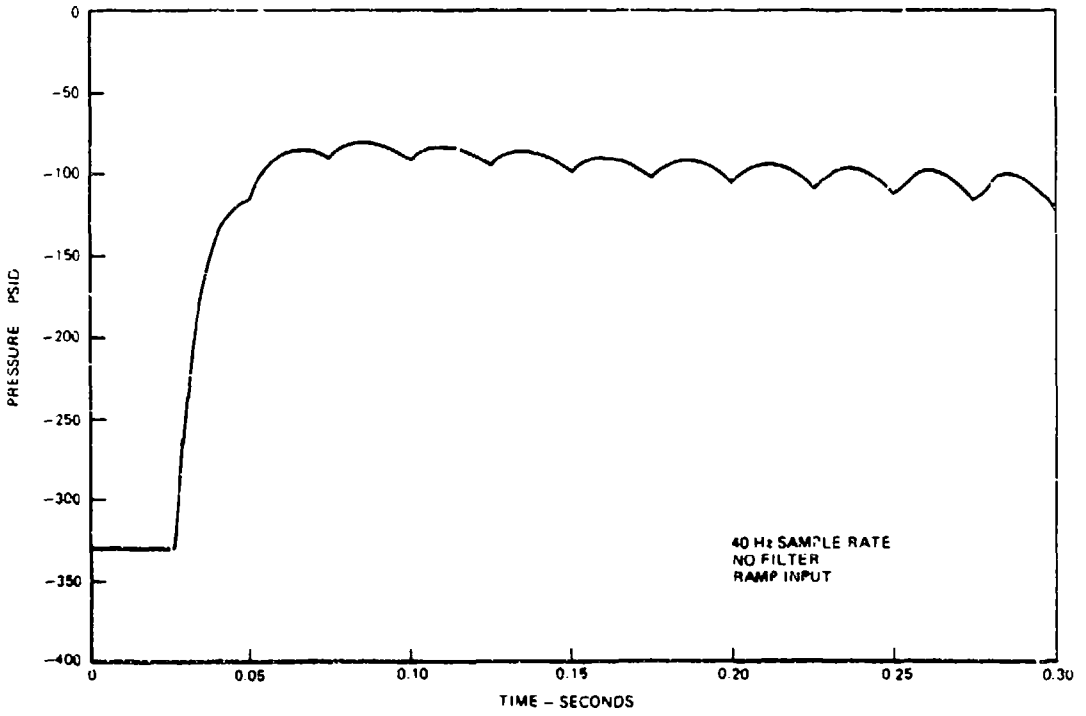


Figure D-2. Differential Pressure on Master Channel

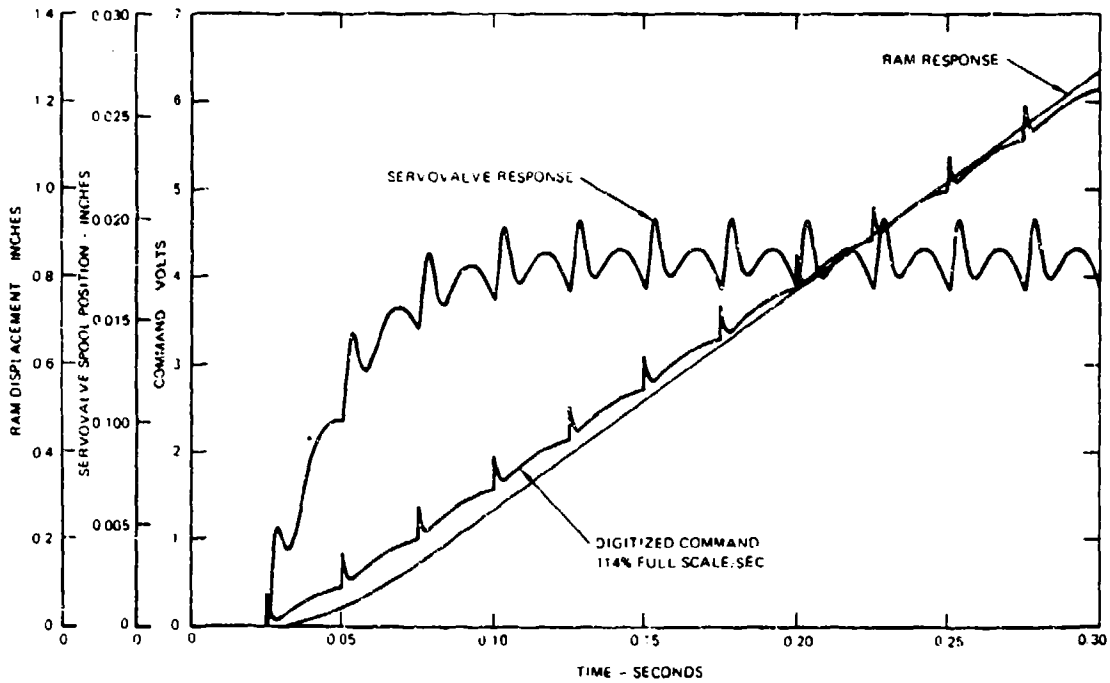


Figure D-3. Effects of 40 Hz Sample Rate on Ramp Input With Notch Filter

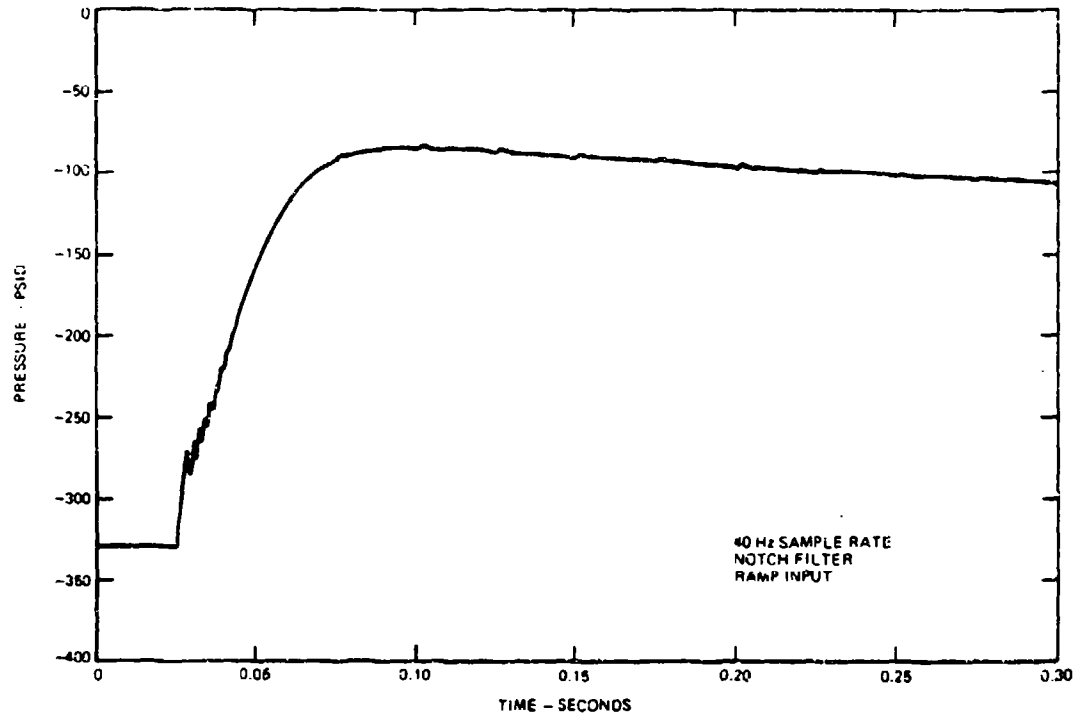


Figure D-4. Differential Pressure on Master Channel

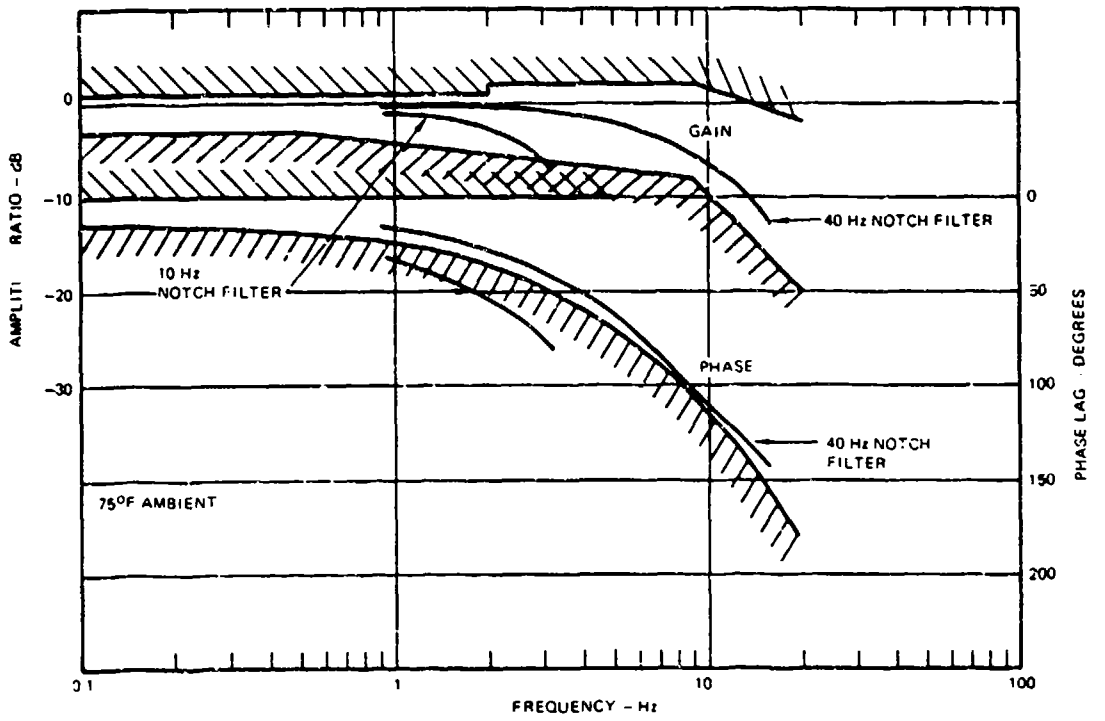


Figure D-5. Small Signal Frequency Response 10 and 40 Hz Sample Rate

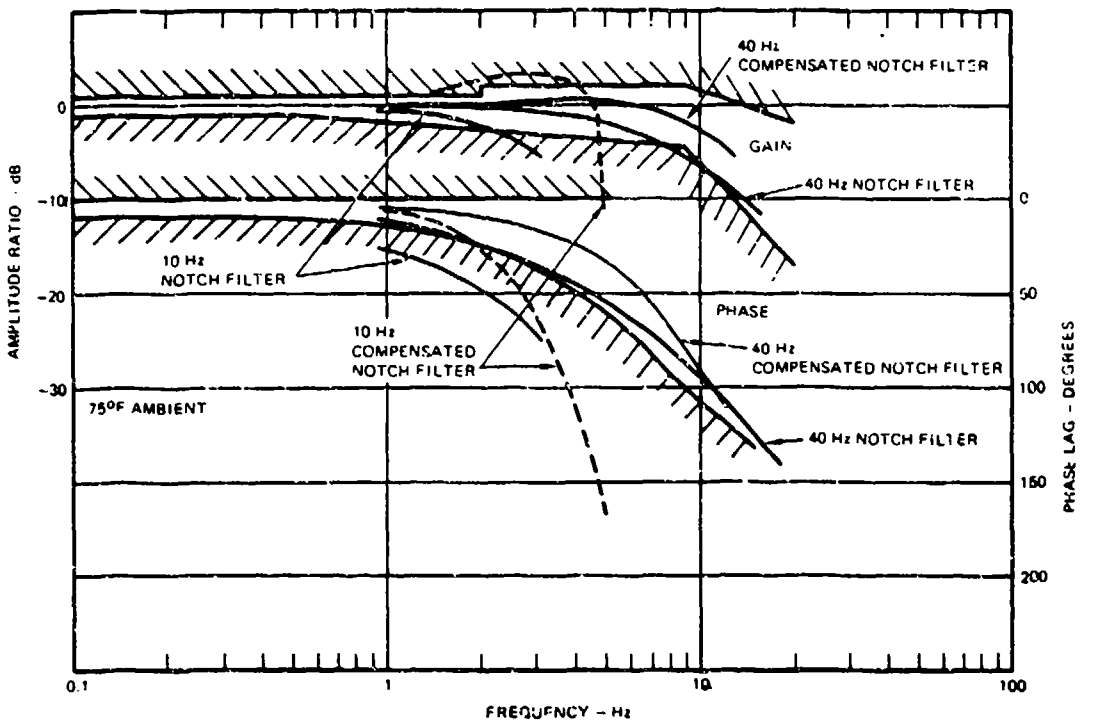


Figure D-6. Large Signal Frequency Response 10 and 40 Hz Sample Rate

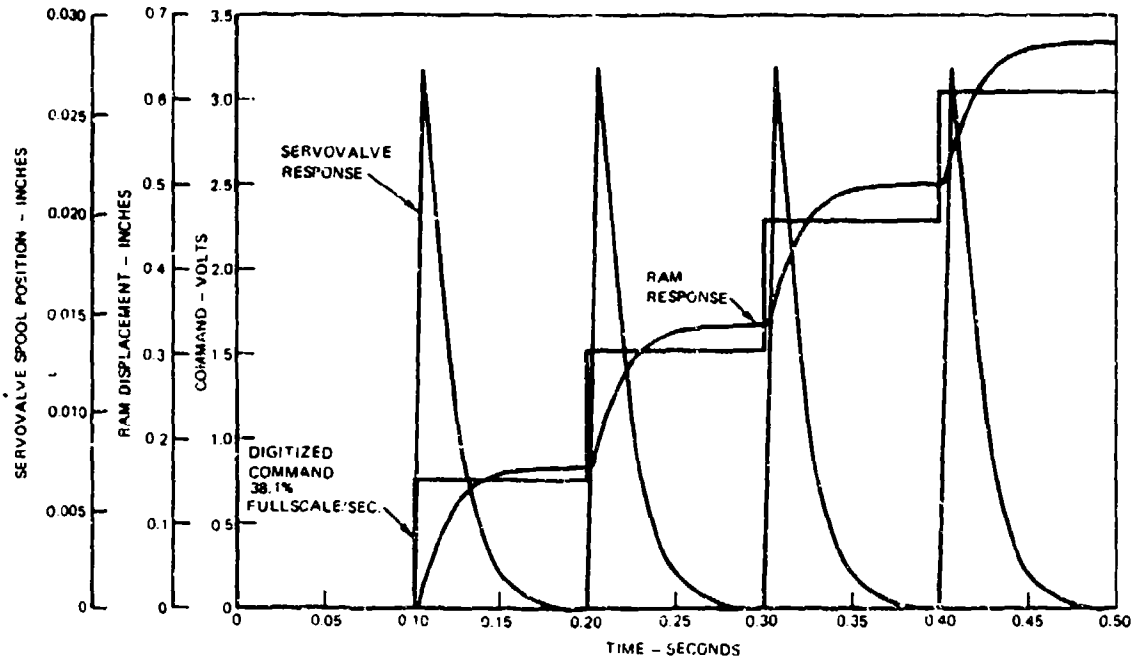


Figure D-7. Effects of 10 Hz Sample Rate on Unfiltered Ramp Input

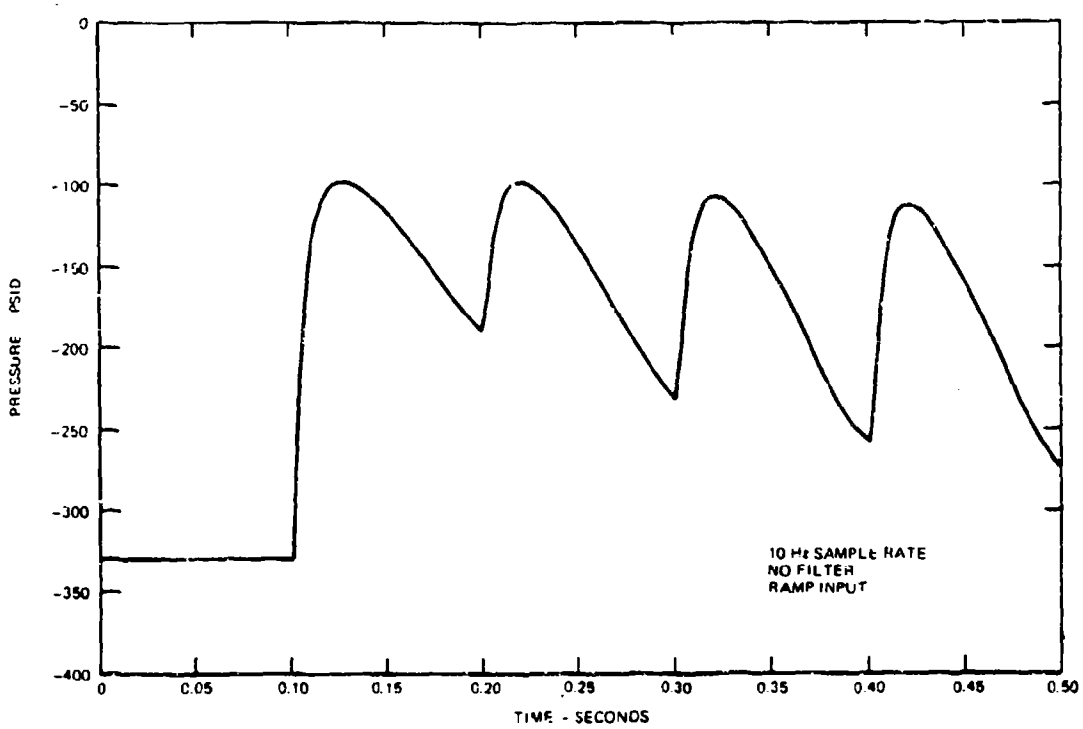


Figure D-8. Differential Pressure on Master Channel

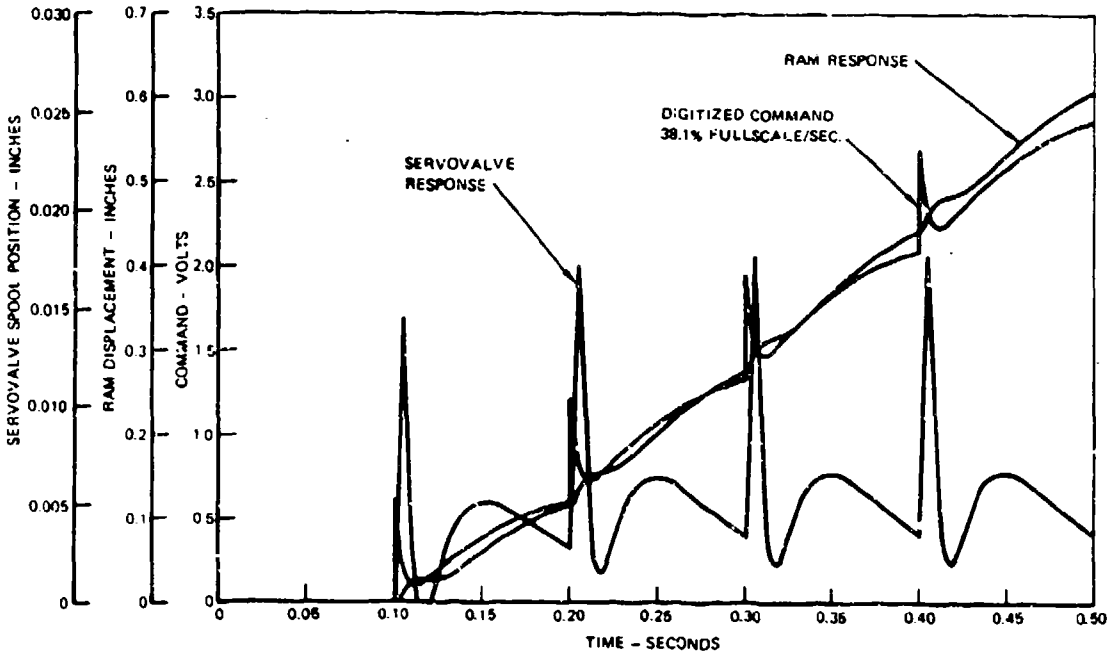


Figure D-9. Effects of 10 Hz Sample Rate on Ramp Input With Notch Filter

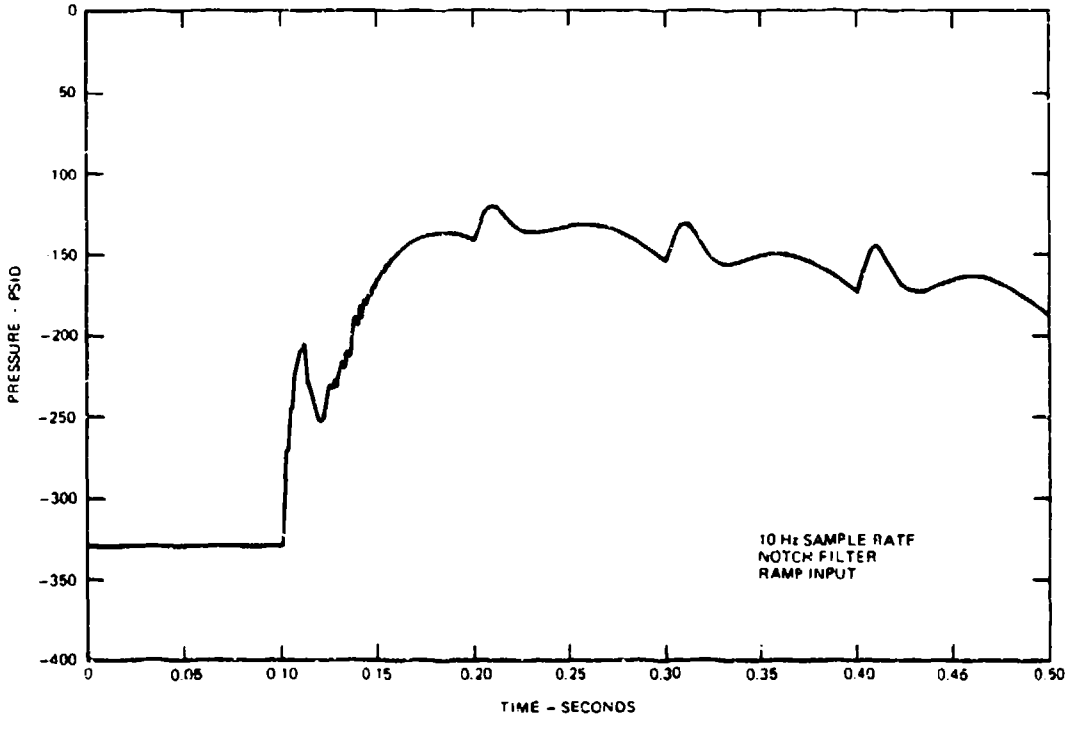
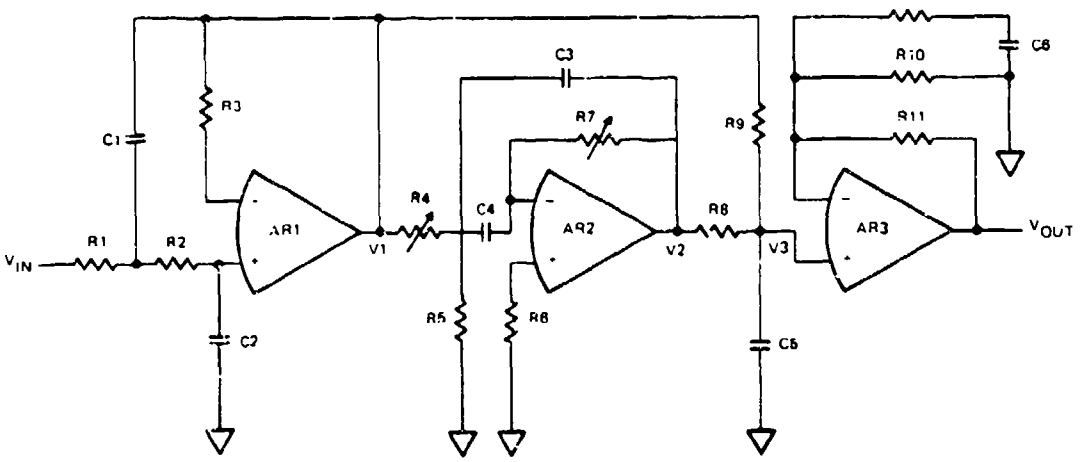


Figure D-10. Differential Pressure on Master Channel

The filter used in each of these cases was a notch filter with the notch set at the sample frequency. It was decided to evaluate different types of filters and the one which was most promising was a compensated notch filter as shown in figure D-11. It consists of a notch network and additional lead and lag networks. This filter was incorporated into the system simulation and evaluated for 40 Hz and 10 Hz sample frequencies.

The results for the 40 Hz sample rate are shown in figure D-12 and D-13. As can be seen from figure D-6, the compensated notch filter improves the frequency response results, but the phase lag exceeds the phase limit at frequencies above 11.0 Hz.

The results for the 10 Hz sample rate are shown in figures D-14 and D-15. As can be seen from the figures, the compensated notch filter is more effective in reducing the servovalve dither but it introduces an objectionable peak in the frequency response gain. The phase lag exceeds the phase limit at frequencies above 2.0 Hz. (See figure D-6.)



$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + 2\zeta_1 T_1 S + T_1^2 S^2} \cdot \frac{1 + T_2^2 S^2}{1 + 2\zeta_2 T_2 S + T_2^2 S^2} \cdot \frac{1 + T_3 S}{(1 + T_4 S)(1 + T_5 S)}$$

SECOND ORDER LOW PASS | NOTCH AT SAMPLE FREQUENCY | LOW FREQUENCY DIFFERENTIATOR

Figure D-11. Compensated Notch Filter

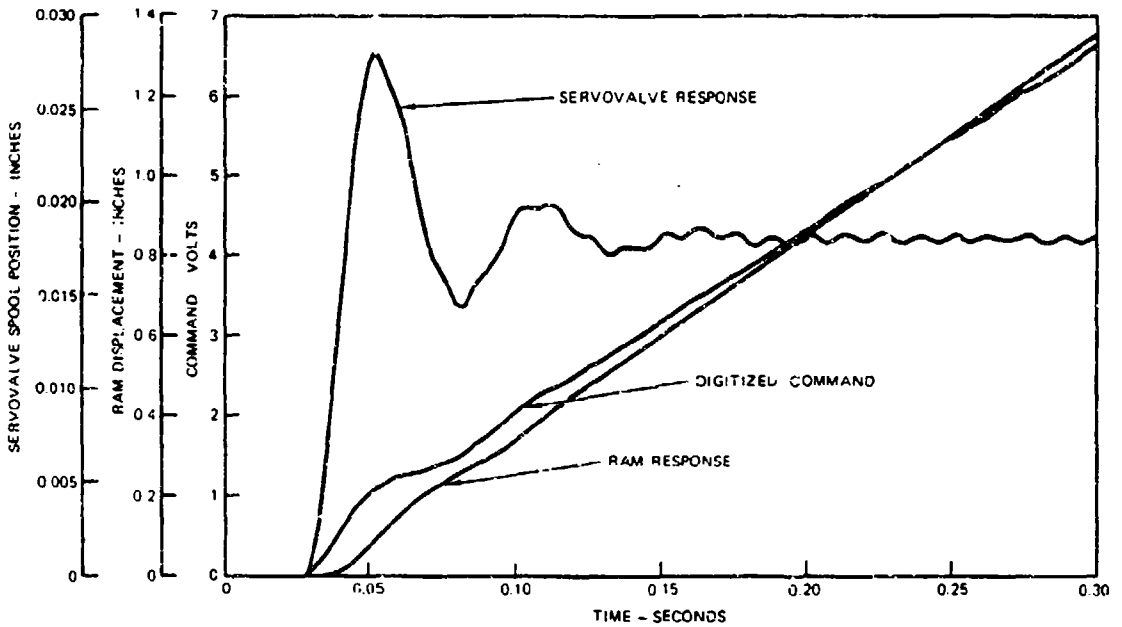


Figure D-12. Effects of 40 Hz Sample Rate on Ramp Input With Compensated Notch Filter

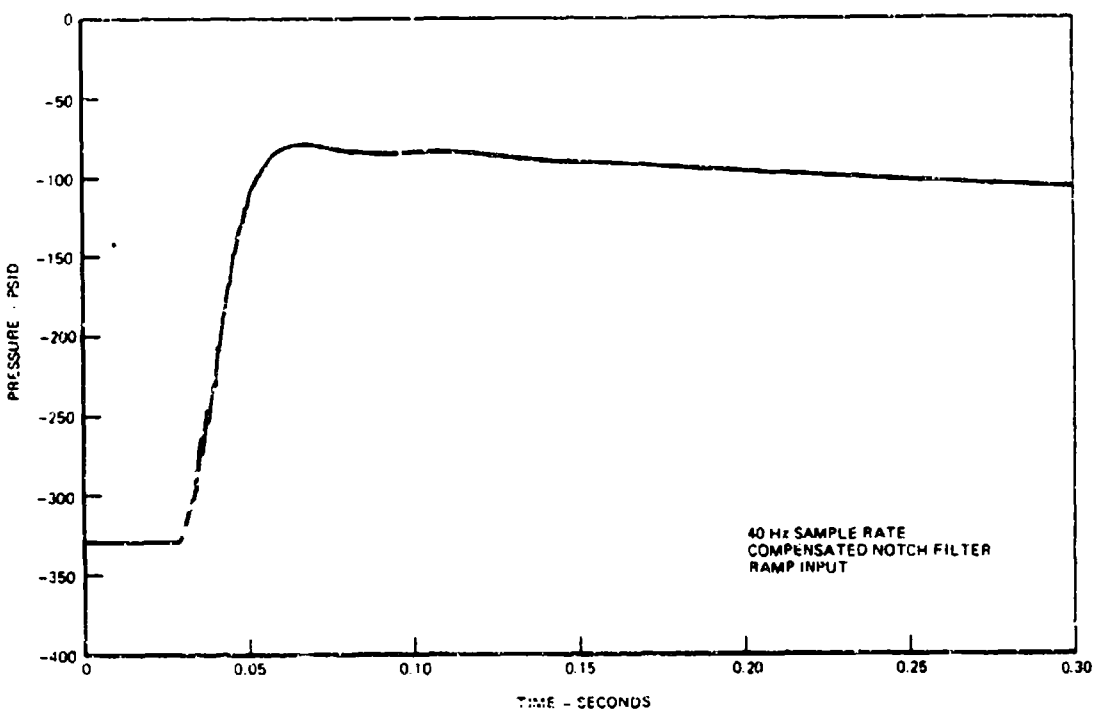


Figure D-13. Differential Pressure on Master Channel

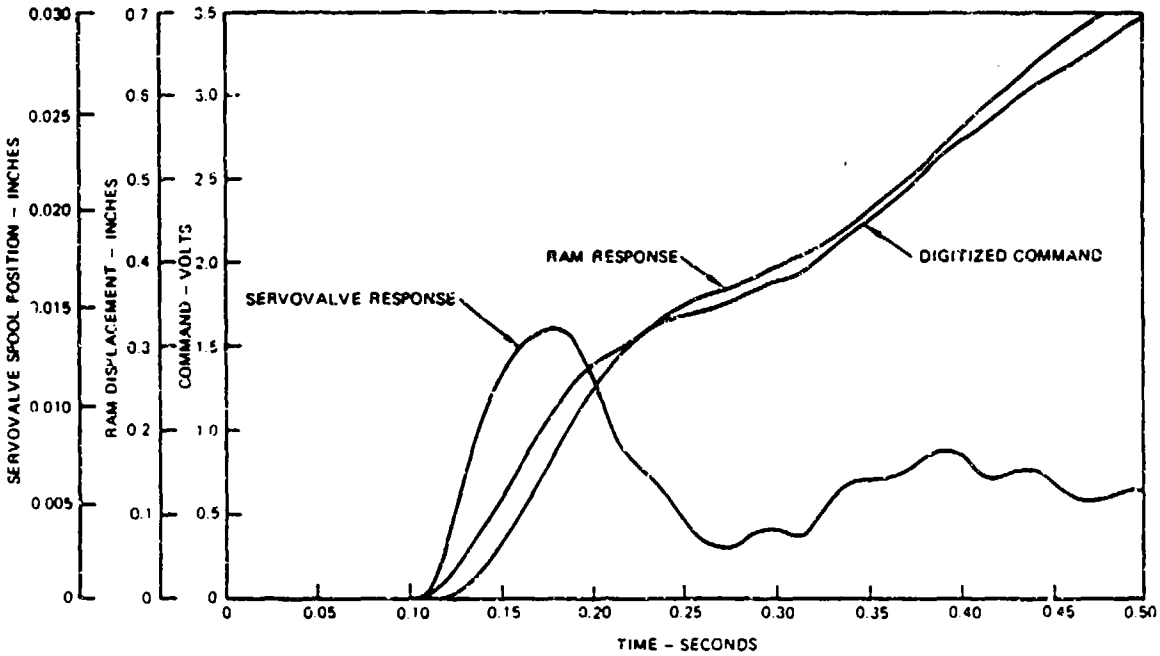


Figure D-14. Effects of 10 Hz Sample Rate on Ramp Input With Compensated Notch Filter

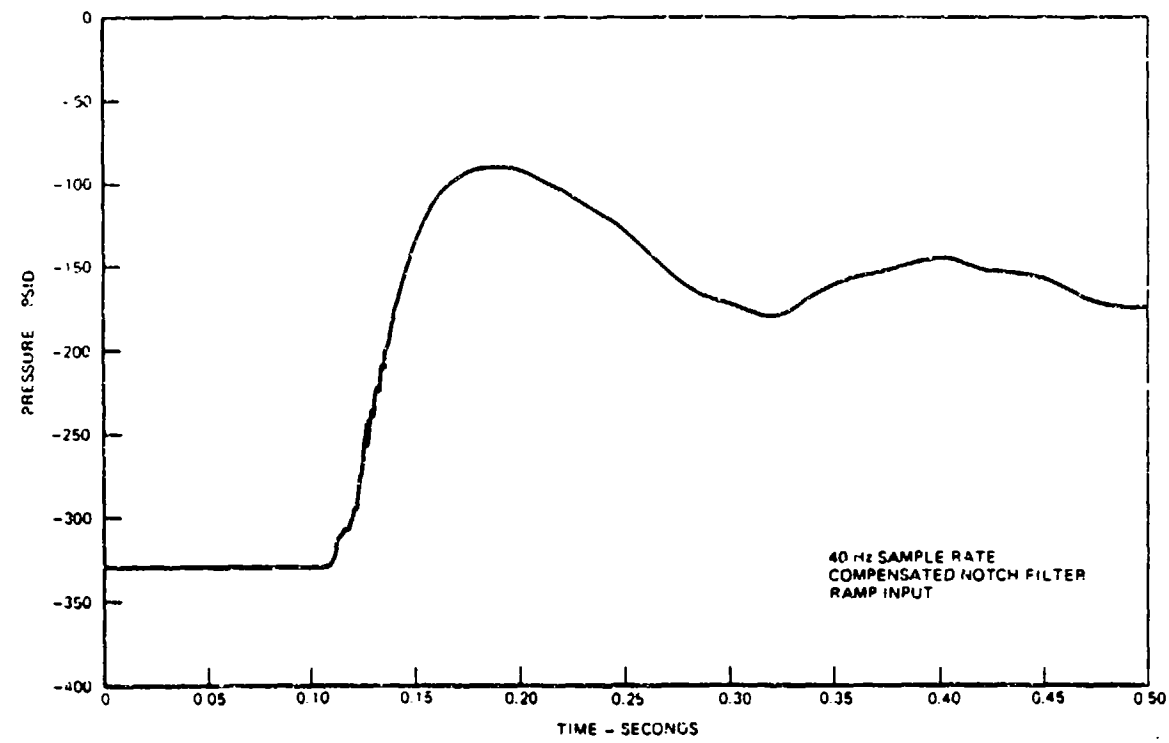


Figure D-15. Differential Pressure on Master Channel

* USGPO: 1983-659-062-1101