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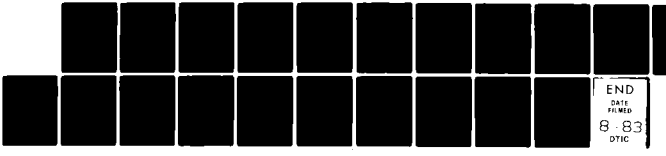

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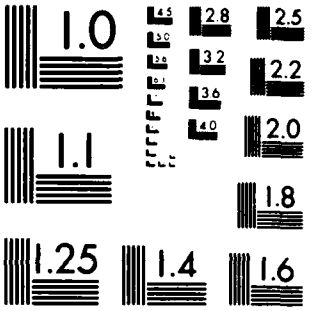

TRANSPORT IN SUBMICRON MOSFETS

FINAL REPORT

D.K. Ferry

August 1, 1983

U.S. ARMY RESEARCH OFFICE
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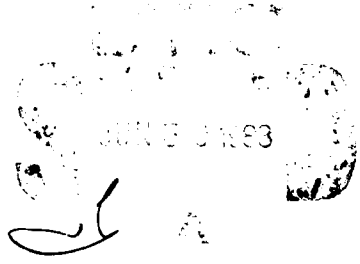
COLORADO STATE UNIVERSITY
FORT COLLINS, CO 80523



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A program of research into the transient dynamic response of silicon MOSFETs is described.

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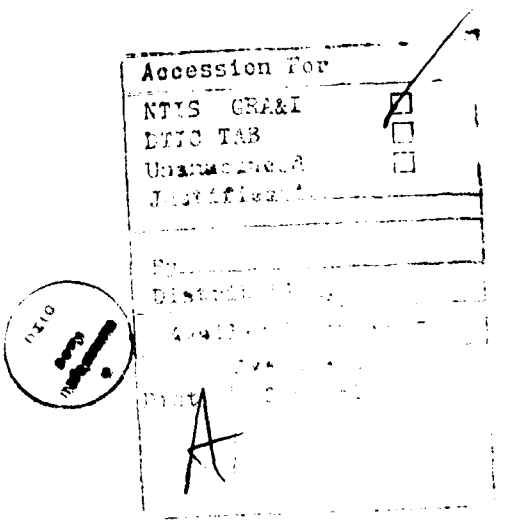
CONTENTS



I. INTRODUCTION

One of the main driving forces in solid-state electronics is the thrust to develop smaller and faster active devices, which dissipate very little power, for eventual use in large-scale integrated circuits. In most situations, however, the actual power-delay product of the device itself is not as important as constraints of charging the interconnection capacitances of the wiring. In this introduction, we show that there is a fundamental lower bound to the delay time itself. This limit arises from the necessity for heat removal, the necessary requirements for signal propagation, as well as the speed-power product itself. At the fundamental limit, the delay time is insensitive to modest variations in the actual speed-power product. At the opposite extreme, in the wire-dominated chip, the cell size is determined by wiring constraints rather than device constraints and the delay time is also independent of the speed-power product.

Power-Delay Products

Integrated circuit technologies are often compared to each other through the speed-power product of a single gate, typically an inverter, and these are measured through the construction of analog circuits such as ring oscillators. Such comparisons rely upon the fact, that when properly defined and measured, the speed-power product can be equated with the minimum energy needed to perform a logic operation.[1] Although the power-delay product is typically viewed as being a technology determined parameter, several authors have recently argued that there are fundamental limits to how small the energy dissipation (and therefore the speed-power product) can be made. Landauer[2] calculated a thermodynamic limit for switching of a single particle in a bistable potential

well and found a value of $kT \cdot \ln(2)$. Bate[3], on the other hand, considered the switching of a group of particles between two collisionally broadened, quantum mechanical energy levels and found that the minimum energy cannot be reduced below 10^{-19} Joule for an error probability of 10^{-30}. This is not an unrealistically conservative design goal for an error probability, although it is considerably beyond current technology. On the other hand, computer simulations of Josephson junction logic elements have yielded power-delay products of 10^{-18} Joule[4]. While the model of Bate is abstract, it is hard to see how the additional complexities present in real inverter circuits would either increase the speed or decrease the power dissipation. Indeed, the limit is conservative in many respects. First, the possibility of gain is neglected. Gain is characteristic of all real logic gates and requires additional energy dissipation for e.g., the charging of interconnecting lines. Secondly, the limit proposed assumes rapid operation or short delays. The cross-over to the thermodynamic limit, similar to that of Landauer for slow operation lies in a range of 10-1000 GHz clock frequency.

The power-delay product discussed above would actually be associated with an inverter circuit composed of the bare devices themselves. However, a practical integrated circuit also has lines or wires associated with each gate. These lines have a power-delay product associated with them and generally dominate the actual energy dissipation in the logic gate.[5,6] The extreme arises when the necessity for wiring dominates the cell size and the device is no longer critical for setting energy dissipation. This latter case is referred to as the wire-dominated chip.[6] We return to this latter case below.

There are other constraints that must also be placed on the power dissipation and the delay time in an integrated circuit. To illustrate these, we consider a square array of N logic cells of area A each. If we can remove Q Watts of heat per unit area, we must require that the dissipated power P satisfies

$$P < QA. \tag{1}$$

However, this condition only establishes the fact that a steady-state temperature exists and does not insure that this temperature will be low. Thus, this is a "worst case" limit. A second limit that must be invoked is that, in the worst case, a signal must be able to propagate across the entire chip in the delay time t_d. This signal propagation requirement is expressed as

$$(NA)^{\frac{1}{2}} \leq ct_d \ , \tag{2}$$

where c is the speed of propagation and is typically lower than the speed of light due to the dielectric properties of the semiconductor chip.

From the above discussion, we can now define a fundamental limit on the delay time itself. The argument is similar to one proposed earlier by Keyes,[7] but differs in that a firm limit on t_d is set.[8] This limit apparently has not previously been recognized. Equations (1) and (2) imply a range of areas that must satisfy the joint inequalities

$$P/Q < A < c^2t_d^2/N \ . \tag{3}$$

These inequalities illustrate that the requirement of signal propagation leads to such a small system for a given delay time that the heat can no longer be removed. However, there is another constraint set by the

energy dissipation, or $Pt_d = E_m$. Using this quantity in (3) leads to the final limit[8]

$$NE_m/Qc^2 < t_d^3 \quad . \tag{4}$$

The inequality in (4) appears to be a fundamental lower bound on the delay time itself. It is interesting to note that the degree of integration represented by N and the heat removal rate Q are as important as the power-delay product of the individual cells in determining how fast the overall chip can be operated. In particular, we note that it requires a three order-of-magnitude reduction in E_m to reduce the minimum t_d by a single order-of-magnitude. Increasing the integration level actually tends to worsen the minimum delay time that can be achieved, although this minimum is well below the levels discussed in today's technology. Using the above limit found by Bate of 10^{-19} Joule, a value of Q of 20 W/cm^2 (appropriate to a Freon cooled computer), and N = 1, a lower limit of 0.01 picosecond is found. The clock frequency corresponding to this is in the optical range, yet seems to be a fundamental limit.

The Wire-Dominated Chip

In some applications, such as gate array chips, the chip itself is dominated by the interconnection wiring and is referred to as a wire-dominated chip.[6] In these chips, the cell size is determined not by the devices but by the number of wires that must run through the cell itself. When this limit occurs, further reductions in the active area of the devices themselves will not significantly increase the number of logic cells per unit area of chip. In these situations, the actual power-delay product of the device itself is not as important as constraints of charging the interconnection capacitances of the wiring.

Keyes[6] has argued that the power-delay product of such a wire-dominated chip is

$$Pt_d = C_w f K^2 w V_B V_S / M \ , \tag{5}$$

where P is the power dissipation, t_d is the delay time, M is the number of metallization or wire layers in the chip, K is the number of wire channels of width w required per logic cell, and f is the fraction of these channels occupied by wires with capacitance C_w per unit length of wire. Here, V_B and V_S are the supply and signal voltages, respectively. The form of (5) is easily understood, as the right-hand side is just the energy stored in the capacitance of the wires, if the average length of a wire is K/M and the average number of wires per cell is $w \cdot f \cdot K$.

Since the cell area is dominated by the interconnection wiring, the cell size itself is approximately given by

$$A = (Kw/M)^2 \ . \tag{6}$$

The ability to dissipate the heat generated by the input power P must also be included in the discussion. This can be done through the incorporation of (1) and (5). The other fundamental limit, mentioned above, is that a signal must be able to propagate across the entire chip in the delay time t_d, as discussed above. This leads to (2). Thus, for a chip containing N square cells, this signal propagation limit is expressed by combining (1), (2), (5), and (6) as[8]

$$t_d^2 > N^{\frac{1}{2}} f K C_w V_B V_S / Qc \ . \tag{7}$$

As above, this constraint is essentially independent of geometrical factors such as w, although these latter factors do affect C_w slightly.

Using (7), a lower limit to the delay time can also be obtained by taking the appropriately most favorable limits on the individual parameters. Heller et al.[9] have shown that a value of $K = 20$ is typical for a system of 1000 gates. Master slices with this number of gates have been reported[10] and do approach the wire-dominated limit. Heat dissipation rates from above will be used. The question of line capacitance is more arguable, but for future small chips, the fringing and interline capacitances will probably limit the lower value of C_w to 0.1 fF/micron.[11] Using these values and setting c to the speed of light, a lower limit of about 0.2 nonoseconds is obtained for the delay time.

The significance of this result is obvious. Even if the individual logic gates in a wire-dominated chip are fast, the chip itself cannot have a delay time shorter than 0.2 nanoseconds, corresponding to a clock frequency of about 1.0 GHz. While the constraints used here are appropriate to a master slice chip, the conclusion is expected to be more general and apply to a wide variety of array type logic designs in which each cell must be able to communicate with each other cell or with cache memories at some distance.

Current Technologies

Midway between the two limiting cases discussed above are those cases pertaining to current efforts to obtain high speed logic. It is of interest to try to set practical limiting values of the expected delay times for these logic families. While no direct methods along the lines of the above discussions are available, we can however use the above results to infer some practical values. This can be done in the following way. First, we use (5) to determine the smallest value of K

for which the speed-power product of the active devices is smaller than the right-hand side of (5) for some appropriate technological parameters. Using the results of Heller et al.,[9] the maximum number of gates which can be integrated on the chip without it becoming wire-dominated (in a power-delay sense) can be then estimated. Finally, these values can be used in (4) to determine an appropriate delay time. We apply this below to a high-speed GaAs implementation.

For the case of GaAs, we can take typical values as $M = 2$, $V_B = V_S = 5$ V, $f = 0.5$, and $w = 1$ micron (increasing w will lead to a reduction in the resulting N for high-speed operation). We also can take the lower limit on C_w to be 0.1 pF/micron as discussed above. For these values, (5) becomes

$$E_{wire} \cong 6 \times 10^{-16} K^2 . \tag{8}$$

Experimental values of the speed-power product for GaAs MOSFETs are on the order of 0.05 picojoule for the above parameters,[12] which gives a K of about 10 as the maximum. The results of Ref. 9 suggests that this corresponds to an N of about 200, which yields a delay time of about 6.5 picosecond from (4). The driving function on this limit is of course the experimental energy dissipation in the logic gates themselves. Lowering this value by for example using HEMT technology leads to a slightly lower value for the delay time.

In summary, we have considered the limits imposed by heat dissipation and signal propagation velocity in integrated circuit chips. The two contradictory limits of large area for power dissipation and small area for signal propagation have set a limiting constraint on the

achievable delay time in real thermodynamically irreversible computers. Considerations of the fundamental energy dissipation limits suggested by quantum mechanical calculations lead to a lower limit on the delay time of about 0.01 picoseconds. On the other hand, constraints imposed on a master slice type chip are more general and lead to a limit on the achievable delay time of about 0.2 nanoseconds, corresponding to a clock frequency of the order of 1 GHz or less, due to the domination by the interconnection wiring. These latter are more general, n that any array type logic, in which each cell must communicate wi each other cell or with large cache stores of memory at some dista will also likely be wire dominated and show the same limitations. ' , implies that designs for fast logic must be prepared in such a manner that the cell area is not dominated by the requirements of necessary wiring interconnections if the speed is to be achieved. Considerations of fast logic, such as GaAs technology, lead to intermediate delay times in the 1-10 picosecond range, if wire dominance can be avoided.

These results are significant. In particular, it is readily apparent that one can expect delay times in future logic circuitry to get down to the time scale of energy and momentum relaxation times themselves, especially in alternate materials such as GaAs or InP. Moreover, the time scale is on the order of the duration of overshoot velocities themselves,[13-15] so that higher drive currents can be expected from future devices. It is thus imperative that we begin to fully understand the transport in the transient dynamic response (TDR) regime appropriate to these future VLSI technologies.

II. SUMMARY OF RECENT RELEVANT WORK

In recent years, much interest has centered upon the transient dynamic response of electrons as it impacts carrier transport through small spatial regions of high electric field. With recent improvements in technological fabrication of very-short-channel devices, this problem has become not only of theoretical interest but of practical interest as well. For instance, in the pinch-off region of a short-gate field-effect transistor, the carriers injected at the source move by a combination of drift and diffusion in a very high electric field. Then the transit time of the carriers under the gate can be shorter than, or of the same order of magnitude as, the time needed to establish a steady-state high-field distribution function. In fact, a condition for this to occur is that the transit-time in the high-field region be comparable to the momentum relaxation time thus causing the velocity to increase, but much shorter than the energy relaxation time. Thus, on average the carriers may transit through a considerable portion of the high-field region with almost their low field mobiility even though the applied field corresponds to the saturated velocity range.[16] This is true not only for the first-order moment of the distribution function of the carriers (drift velocity), but also is true for higher order moments, and especially for diffusion (related to the second moment). The diffusion coefficient is one of the most important parameters required in modeling semiconductor devices, it is not only necessary for evaluating operating characteristics and frequency characteristics but it provides also fundamental characterization of velocity fluctuations in the system and their contribution to noise in the device.[17] Diffusion actually is a process depending upon velocity correlation and the relationship

between diffusion and drift, as expressed by the Einstein relation, is a steady-state relation. Indeed, tractable results for the steady-state hot electron problem have only recently been achieved. The problem in the transient region is complicated by the fact that the random-walk equations governing transient diffusion do not reduce to normal Fick's law behavior on time scales comparable to the relaxation process, a result of the general non-Markovian and nonstationary nature of transport on these time scales. We have addressed some of these problems with the help of a Retarded Langevin Equation (RLE) as well as with ensemble Monte Carlo (EMC) techniques in order to approach the random walk of the carriers. In the former case, we define a nonstationary two-time correlation function for the velocity fluctuations which can be related to a transient diffusion coefficient. The formal solution of the RLE allows us to derive a general expression for the correlation function.

Retarded Langevin Equation

We consider an ensemble of carriers initially at equilibrium with the crystal lattice. The ensemble is represented by a Maxwell-Boltzmann distribution in v-space ($\langle v \rangle = 0$ and $\langle v^2 \rangle = 3k_B T_L/m$ with T_L the lattice temperature). At a certain time, referred as $t = 0$, we apply a macroscopically homogeneous and steady electric field whose amplitude corresponds to hot carriers. These conditions give rise to a TDR regime in which the system relaxes toward a nonequilibrium, steady-state and often exhibits a velocity overshoot.

The motion of the particles is governed by a Retarded Langevin Equation for the velocity of the carriers, and is written as[18,19]

$$m \frac{dv}{dt} = -m \int_o^t \dot{\gamma}(t-u)\, v(u)du + R(t) + qE_o h(t) \ , \qquad (9)$$

where $R(t)$ is a random force symbolizing the random (nonregular) part of the collisions of the carriers with the lattice (no carrier-carrier interaction is considered here), E_o is the external field, and $h(t)$ is the Heavyside function. $\dot{\gamma}(t)$ is the memory function of the system and is related to the correlation function of the total force applied to the system. For instance, in the case of an equilibrium regime, we would have $\dot{\gamma}(t) = \langle R(0)R(t)\rangle / m^2 \langle v^2(0)\rangle$, in absence of external forces.

Equation (9) is a non-Markovian form of the Langevin equation, since the rate of change of the velocity at t not only depends on the velocity at that time but also depends on all past time. Further, it is a nonstationary equation, since the lower bound in the intergral refers to that time where the disturbing field was applied. It is generally admitted by now that only an equation such as (9) can describe very-fast processes, and in particular the TDR regime can be described in this way. This equation can be readily manipulated to lead to the generalized Kubo form[20]

$$v_d(t) = \frac{qE_o}{m\langle v^2(0)\rangle} \int_o^t \phi_{\Delta v}(0,t')dt' \ . \qquad (10)$$

This relationship existing between the first and second moment of the velocities of the carriers is a direct intrinsic property of the RLE used to describe the TDR regime, and is a statement of the familiar Kubo formula found in equilibrium statistical mechanics.

Ensemble Monte Carlo Technique

The ensemble Monte Carlo used here has been developed by Lebwohl and Price[21] and subsequently used and described in great detail by the

principal investigator.[22] An ensemble of >5000 electrons, initially in equilibrium, is subjected to a strong electric field step at $t = 0$, and the transient response is studied. This procedure is applied to n-Si, biased along the <111> directions. Nonparabolicity is included with $\alpha = 0.5\ eV^{-1}$.

Both sides of (10) have been calculated in the simulation and are compared in Fig. 1. The agreement is within the accuracy of the EMC method and leads to the conclusion that the RLE can correctly describe the motion of hot carriers in the TDR regime. From (10) we see that a linear increase of the velocity ($\langle v(t)\rangle = eFt/m^*$), as expected for ballistic transport, can only occur when $\phi_{\Delta v}$ is constant in time. In Fig. 2, we show the temporal evolution of $\phi'_{\Delta v}(t,t_o)(t > t_o)$ for three different values of t_o, including $t_o = 0$. It is evident from this figure that the time duration over which $\phi_{\Delta v}$ is constant, corresponding to a ballastic rise of the velocity, is exceedingly short, perhaps only a few femtoseconds, even though the mean free time is much longer. We also note that the MC results show a general trend in that $\phi_{\Delta v}(t,t_o)$ decays more rapidly for longer t_o, corresponding to a higher temperature and more rapid randomization of the ensemble as time increases.

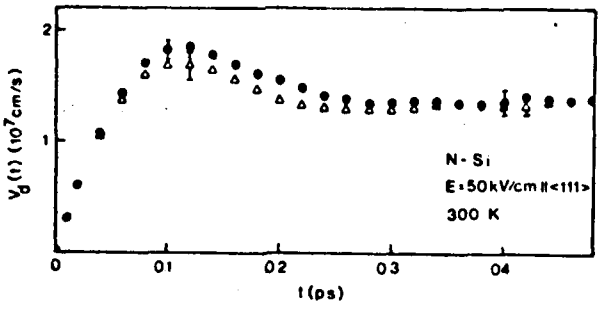


Figure 1. Comparison of the ensemble drift velocity (Δ) and integral of the velocity autocorrelation function (·) as a function of time.

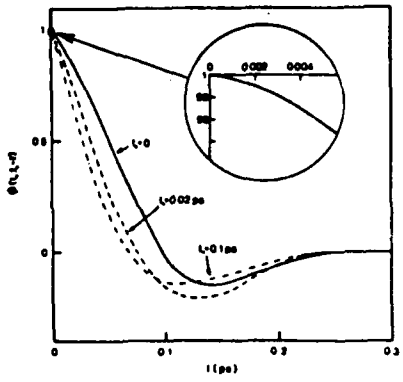


Figure 2. Normalized velocity autocorrelation function $\phi_{\Delta v}(t,t_o)$ for three initial times t_o.

Another problem in the usual treatment of ballistic transport is related to the energy balance equation. Normally, the contribution of the thermal energy, due to the random motion of carriers, is completely neglected. But, this can be shown to be the dominant term. A qualitative explanation[23] of the processes on very short-time scales is the following: when an electric field is turned on at $t = 0$, the ensemble of electrons begins to respond instantaneously by a shift in momentum space, causing an instantaneous rise of the velocity. However, we don't have an instantaneous increase of velocity fluctuations, that is a spreading of the ensemble in momentum space. Only when the collisions begin to break up the correlation of the ensemble with the initial state can the energy begin to evolve. The memory effect in the evolution of the energy is not taken into account in the equations normally used for ballistic transport. A first attempt to express this in a formal way leads to the following equation[24]

$$\frac{d\bar{E}}{dt} = qFv_d(t)[1 - \phi_{\Delta v}(t,0)] - \int_o^t dt'[\bar{E}(t-t') - E_o]x_e(t') \ , \qquad (11)$$

where $x_e(t)$ is a decay function related to the energy correlation function. In Fig. 3 we plot the initial increase of the energy as calculated by the EMC. For comparison, we also show a curve corresponding to the forcing term in (11) (continuous curve) and to a ballistic regime (dashed curve). It is evident that at very short times, the role of the memory function is significant, and that collisions effects are already evident in the EMC data for $t \gtrsim 0.04$ psec. Equation (11) was derived under the assumption that the energy associated with the drift of the ensemble is much smaller than the thermal energy. Unfortunately, this is not the case for Si for times shorter than 0.1 ps, as shown in Fig. 4 where the two energies are calculated from the EMC for a field of 50 kV/cm ($E_d \equiv m^* v_d^2/2$). Thus, in order to formally solve the problem of TDR, we will have to go back to the original equations and try to obtain decoupled equations for energy and momentum.

It has been shown that a time dependent diffusion coefficient can be defined in the nonstationary regime as

$$D(t) = \frac{1}{2}\frac{d}{dt}\langle[\Delta x(t)]^2\rangle = \int_0^t \phi_{\Delta v}(t',t)dt' \quad . \tag{12}$$

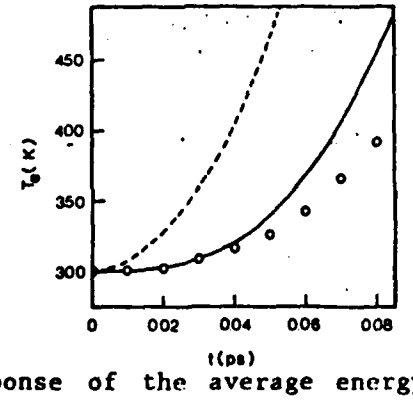


Figure 3. Response of the average energy (in degrees K) of the ensemble. The data point are EMC results, the continuous curve represent the forcing term of Equation (11) and the dashed curve represents the ballistic rise.

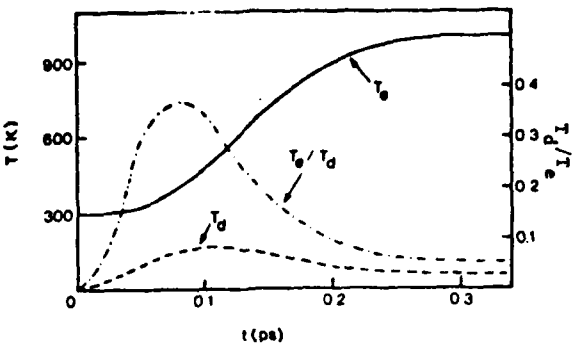


Figure 4. Evolution of the drift (T_d) and thermal (T_e) energy of the ensemble (left scale) and the ratio of the two (right scale) as a function of the time.

Using the EMC method, $\phi_{\Delta v}(t',t)$ and $\langle(\Delta x(t))^2\rangle$ can be calculated independently and the validity of (12) can be checked. In the present work, the integral is calculated by computing 25 correlation functions at equally spaced times in the range 0-0.4 psec. This result is illustrated in Fig. 5, where the two sides of (12) have been calculated for an electric field of 50 kV/cm. The agreement is good, within the error due to the numerical integration and differentiation performed.

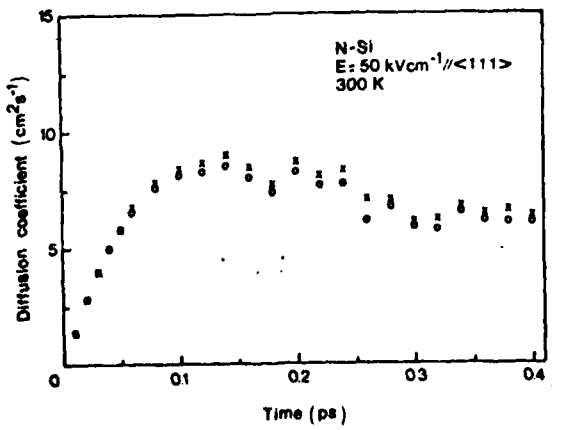


Figure 5. Comparison of the diffusion coefficient as a function of time, obtained from the correlation function (x) and from the time derivative of the average square displacement (·).

Since the steady-state diffusion coefficient can be obtained as a limiting case of (12), this expression can be assumed to be a general definition of the diffusion coefficient for both stationary and non-stationary regimes. The time evolution of D(t), as obtained from EMC methods and from the RLE approach, is shown in Fig. 6, for two different electric fields. The most important feature is that the diffusion coefficient exhibits an overshoot. This is related to the oscillatory shape of the correlation function $\phi_{\Delta v}(t',t)$, which arises from a combination of momentum and energy relaxation. This also leads to a velocity overshoot effect. This is present both in the theoretical and MC results, which are found to be in fairly good qualitative agreement.

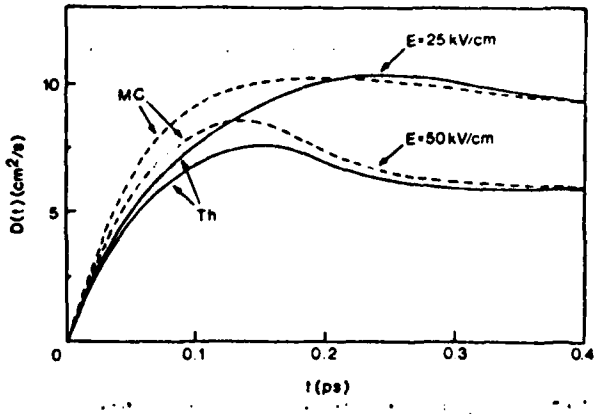


Figure 6. Diffusion coefficient as a function of time for two electric fields as obtained from EMC results (dashed curves) and RLE results (solid curves).

III. List of Publications

1. P. Lugli, J. Zimmermann, and D.K. Ferry,"Non-Equilibrium Hot-Carnier Diffusion Phenomenon in Semiconductors. II. An Experimental Monte Carlo Approach," Journal de Physique. 42 (Suppl. 10), C7-103 (1981).

2. G. J. Safrate, D. K. Ferry, and R. K. Reich,"Lateral (Two-Dimensional) Superlattices: Quantum-Well Confinement and Change Instabilities,"Surface Science 113, 485 (1982).

3. D. K. Ferry, J. Zimmermann, P. Lugli, and H. Grubin,"Limitations to Ballistic Transport in Semiconductors," IEEE Electron Device Letters EDL-2, 228 (1981).

4. P. Lugli and D. K. Ferry,"Effect of Electron-Electron Scattering on Monte Carlo Studies of Transport in Submicron Semiconductor Devices," Physicu 117/118B, 251 (1982).

5. P. Lugli, R. O. Grondin, and D. K. Ferry,"in Proc. Conf. in Physics of Submicron Devices, Ed by H. L. Grubin et al. (Plemum, New York, in Press).

6. R. O. Grondin and P. Lugli,"Ballistic Transport in Semiconductors," IEEE Electron Device Letters EDL-3, 373 (1982).

7. R. O. Grondin, W. Porod, and D. K. Ferry,"Delay Time and Signal Propagation in Large-Scale Integrated Circuits," IEEE J. Solid State Circuits, in press.

IV. REFERENCES

1. R. Müller, H.-J. Pfleiderer, and K.-U. Stein, IEEE J. Sol.-State Circuits SC-11, 657 (1976).

2. R. W. Landauer, IBM J. Res. Develop. 5, 183 (1961).

3. R. T. Bate, in VLSI Microelectronics: Microstructure Science, Ed. by N. Einspruch (Academic Press, New York, 1982).

4. T. Gheewala, Proc. IEEE 70, 26 (1982).

5. P. M. Solomon, Proc. IEEE 70, 489 (1982).

6. R. W. Keyes, Int. J. Theor. Phys. 21, 263 (1982).

7. R. W. Keyes, Proc. IEEE 63, 740 (1975).

8. R. O. Grondin, W. Porod., D. K. Ferry, submitted for publication.

9. W. R. Heller, W. F. Mikhail, and W. E. Donath, Proc. 14th Design Automation Conference, 1977, p. 32.

10. R. J. Blumberg and S. Brenner, IEEE J. Sol.-State Circuits SC-14, 818 (1979).

11. D. K. Ferry, in Adv. in Electronics and Electron Physics, Vol. 58, Ed. by C. Marton (Academic Press, New York, 1982), p. 311.

12. S. T. Long, B. M. Welch, R. Zucca, P. M. Asbeck, C.-P. Lee, C. G. Kirkpatrick, F. S. Lee, G. R. Kaelin, and R. C. Eden, Proc. IEEE 70, 35 (1982).

13. D. K. Ferry and J. R. Barker Sol.-State Electron. 23, 545 (1980).

14. H. L. Grubin and D. K. Ferry, J. Vac. Sci. Technol. 19, 540 (1981).

15. D. K. Ferry and H. L. Grubin, Microelectron. 12(2), 5 (1981).

16. H. Kroemer, Sol.-State Electron. 21, 61 (1978).

17. J.-P. Nougier, in Physics of Nonlinear Transport in Semiconductors, (Plenum Press, New York, 1979) p. 415.

18. R. Zwanzig, J. Chem. Phys. 40, 2527 (1966).

19. H. Mori, Progr. Theor. Phys. 33, 423 (1965).

20. J. Zimmermann, P. Lugli, and D. K. Ferry, J. Physique 42 (Suppl. 10), C7-95 (1981).

21. P. A. Lebwohl and P. J. Price, Appl. Phys. Lett. 19, 530 (1971).

22. D. K. Ferry and J. R. Barker, Phys. Stat. Sol. (6) 100, 683 (1980).

23. D. K. Ferry, J. Zimmermann, P. Lugli, and H. Grubin, IEEE Electron Dev. Letters EDL-2, 228 (1981).

24. D. K. Ferry, J. Physique 42 (Suppl. 10), C7-109 (1981).

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