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July 1977

STUDY OF THE PHYSICS OF INSULATING FILMS AS RELATED TO THE RELIABILITY OF METAL-OXIDE SEMICONDUCTOR (MOS) DEVICES

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The enclosed paper discuss the trapped hole location and annihilation in Si, current and C-V instabilities in SiO_2 at high fields, annealing of neutral electron traps in irradiated oxides, Al implanted into the SiO_2 layer of MOS structures, electron trapping as a result of Al implanation, the initial oxidation regime of silicon oxidation and the electronic structure of SiO_2, $Si_xGe_{1-x}O_2$, GeO_2.

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INTRODUCTION

The importance of the charge transport and charge storage properties of SiO_2 relative to the reliability of modern MOSFET technologies and Si bipolar transistor technologies has been emphasized in earlier reports. We are continuing to use the sophisticated new techniques that are now available to study these important effects. Some of these techniques are:

1. The photo IV technique for determining charge location.
2. The avalanche injection technique for studying charge trapping.
3. The use of various types of radiation to inject charge and to create hole-electron pairs.
4. The automatic insitu ellipsometer to measure SiO_2 growth kinetics.
5. Advanced silicon processing and ion implantion facilities to construct samples as needed.

The equipment mentioned above are highly automated which enables us to make accurate measurements and process the results using a computer. Our emphasis continues to be placed in the following areas:

1. To study the effect of ion implantation using species of particular interest, on the electron trapping characteristics of SiO_2.
2. To determine the effect of SiO_2 processing conditions on hole and electron trapping in SiO_2.
3. To investigate the effect of various types of radiation, as used in modern devices construction on the electron trapping characteristics of SiO_2.
4. To evaluate the possibility of using electron trapping regions deliberately introduced into the SiO_2 to improve the electrical breakdown characteristics.
5. To study the effect on the Si-SiO_2 interface of non-penetrating radiation applied to the outside surface of the SiO_2.
6. To study the growth kinetics of SiO_2 as influenced by the substrate doping and also to study the growth of SiO_2 on polycrystalline silicon as required by new silicon gate technologies.

The information resulting from the studies described above is vital to the development of improved technologies in the future and will also result in new, important, fundamental understandings of charge transport mechanisms in SiO_2.

The work on the effect of Al implantation on the electrical trapping characteristics of SiO_2 has been completed and has been submitted to the Journal of Applied Physics as two papers entitled:

Electron Trapping Resulting from Aluminum Implantation into SiO_2: Trap Characterization

D. R. Young, D. J. DiMaria, W. R. Hunter, and C. M. Serrano

Electron Trapping Resulting from Aluminum Implantation into SiO_2: Charge Location

D. J. DiMaria, D. R. Young, W. R. Hunter, and C. M. Serrano

The work using P implantation is almost complete and we expect to have these results written up for publication in the near future. This will be described in a later report. We have had a problem with inconsistent results at the lower energies. This is throught to be due to a charge exchange problem in the ion implanter that is being investigated. The work on As implantation is underway and we expect these results will also be available soon. Our preliminary results indicate a much larger trap cross section for As as compared with P. Dr. Roger J. DeKeersmaecker, from The *Catholic University of Leuven*, has joined our group and is working on the As implantation.

We have discovered an error in our previous calculations of the profiles of implanted species with respect to the sign of the third moment term. Our results have been corrected in this respect.

The work on E-Beam Enhanced Electron Trapping in SiO_2 has been extended and a copy of a paper that has been submitted to the Journal of Applied Physics is enclosed. This paper is entitled

E-Beam Enhanced Electron Trapping in SiO_2

J. M. Aitken, D. R. Young, and K. Pan

A paper is enclosed entitled:

Avalanche Injection of Holes into SiO_2

J. M. Aitken and D. R. Young

This paper was presented at the IEEE Annual Conference on Nuclear and Space Radiation Effects, July 1977 and will be published in IEEE TRANS ON NUCL SCI DEC 1977.

Some important new work has been done using an electron trapping region deliberately introduced to improve the electrical breakdown characteristics with particular application to the oxide grown above polycrystalline Si. This oxide is known to have in an inferrior breakdown characteristic and spectacular improvements have been observed. This work is described in a paper that is included in this report that has been submitted to the Journal of Applied Physics entitled:

Use of Electron Trapping Region to Reduce Leakage Currents and Improve Breakdown Characteristics of MOS Structures

D. J. DiMaria, D. R. Young, and D. W. Ormond

The relatively high leakage currents observed for the polysilicon are thought to be due to asperities in the polysilicon resulting in high fields and large current densities. The charging of electron traps will occur readily locally due to these large current densities and the trapped charge will lower the field and inhibit the effect.

The photo IV technique has been used to study the migration of Na in the SiO_2 and has verified earlier results that this transport is interface limited. This has been submitted to the *Journal of Applied Physics* as a paper entitled:

Room Temperature Conductivity and Location of Mobile Sodium Ions in the Thermal Silicon Dioxide Layer of a Metal-Silicon Dioxide-Silicon Structure

D. J. DiMaria

A copy of this paper is enclosed.

Work is continuing on understanding the cause of positively charged surface states generated at the Si-SiO_2 interface under illumination with VUV photons of energy larger than 9eV. These photons are thought to be absorbed within the first 100-200 Å of the SiO_2. The surface states are generated under negative gate bias applied to the gate, hence hole and positive ion transport toward the Si-SiO_2 interface are ruled out. The effect is observed at low bias (e.g. 1 MV/cm and decreases when the bias is increased, a fact which rules out an explanation in terms of hot electron and impact ionization of traps etc.

The remaining possible explanations of the effects are: a) the illuminating light reaching the interface with sufficient intensity; b) fluroluminescence yielding band-gap photons that can penetrate to the interface; c) excitons diffusing to the interface and leaving a hole trapped there. Preliminary experiments indicate that the (c) is the likely explanation.

To further separate between these explanations experiments are planned on 3 device structures: Free standing SiO_2 films for studying transmission and luminescence directly; MOS structures for studying the accumulation of positive charge at the Si-SiO_2 interface the field dependence of the photoconductivity; and a buried shallow junction diode underneath the SiO_2 that can detect both photons and excitons (by separating the hole-electron pair) which are absorbed in the Si.

The temperature, SiO_2 thickness, and photon energy dependencies in these experiments should be sufficient to fully understand this effect.

Experiments are also planned to measure: 1) the band-gap of SiO_2 by measuring the barrier between Al or Au electrodes and the valence band of SiO_2 for hole injection; 2) hole motion at low temperature will be measured by combining hole injection with VUV photons and detection with the photo I-V technique (with D. DiMaria); and 3) the field-dependence o the cross section for electron capture on trapped holes (hole-electron annhiliation or recombination).

The effect of silicon doping on the oxidation rate has been studied by E. Irene and D. Dong for low resistivity wafers (.001Ωcm). For temperatures greater than 1040°C the oxidation rate for boron doped substrates is greater temperature than for P doped substrates. The rate of the P doped substrates is similiar to that of lightly doped (2Ωcm) wafers at temperatures between 780°C and 1000°C. The rate for P doping is greater that for B doping and the results for B doping are similar to the lightly doped case. Data analysis in terms of the linear-parabolic model shows that the linear rate constant is always greater for P doped material. The linear constant is related to the surface reaction. The reversal in the order of the oxidation rates is due to the parabolic rate constants which are controlled by the diffusion of oxidant through the growing SiO_2 film.

A practical application of this data is to enhance the oxidation of N^+ regions relative to lightly doped regions by using low oxidation temperatures.

A paper entitled:

Dielectric Breakdown Phenomena in SiO_2

T H. DiStefano and M. Shatzkes

is enclosed. This paper explains dielectric instabilities in thin SiO_2 on the basis of a model involving impact ionization and a negative resistance runaway due to the build up of positive charge resulting from the impact ionization. This paper has been published in

Proceedings of the Third International Symposium on

Silicon Materials Science and Technology

The Electrochemcial Society

Vol. 77-2 March, 1977, Page 332

Another paper on the electronic structure of $Si_xGe_{1-x}O_2$ is enclosed. This paper is entitled:

The Electronic Structure of SiO_2 and Intermediate $Si_xGe_{1-x}O_2$ Compositions: Experiment and Theory

Sokrates T. Pantelides, Bernard Fischer, Roger A. Pollak, and Thomas H. Di Stefano

This paper has been published in:

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RC 6606 (#28479) 6/28/77
Solid State Physics 7 pages

ELECTRON TRAPPING RESULTING FROM ALUMINUM IMPLANTATION INTO SiO_2: TRAP CHARACTERIZATION *

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Abstract:

Johnson, Johnson and Lampert (1) have studied the effect of Al implantation on the trapping behavior of SiO_2. The large fluence that they used (1×10^{14} cm^{-2}) and the low annealing temperatures (up to 600°C) resulted in a trapping efficiency of 1 and made it impossible to characterize the traps. We have used a lower fluence and higher annealing temperatures to reduce the trapping efficiency and enable us to characterize the traps. The predominant trap cross sections are 1.26×10^{-16} and 1.40×10^{-17} cm^2. In a companion paper by DiMaria, Young, Hunter and Serrano the location of the trapped charge is discussed.

*** This research was supported in part by the Defense Advanced Research Projects Agency, the Department of Defense and was monitored by the Deputy for Electronics Technology (RADC) under Contract No. F19628-76-C-0249.**

I. INTRODUCTION

The effect of Al implantation on the electron trapping behavior of SiO_2 has been studied by Johnson, Johnson and Lampert (1) using MOS structures. They used a fluence of 1×10^{14} at/cm^2 at 20 keV with a SiO_2 thickness of 1400 Å. This work indicated that most of the traps were due to displacement damage. The maximum annealing temperature was 600°C. In a recent talk given by D. R. Young (2) some data were presented showing that annealing temperatures up to 1050°C result in a substantial reduction in the trapping rate. This data is given in Fig. 1. It was hoped that these high temperature anneals would eliminate the displacement damage and enable us to study the trapping associated with the Al sites. We have also varied the SiO_2 thickness from 490 to 1400 Å and the implantation energy from 15 keV to 40 keV. The location of the trapped charge has been studied on the same samples by DiMaria, Young, Hunter and Serrano using the photo I-V technique and these results are given in the companion paper.

II. EXPERIMENTS

A. Sample Preparation

Silicon p-type wafers are used with a resistivity of 0.1 to 0.2 ohm-cm. The SiO_2 is grown at 1000°C in a dry oxygen environment. The samples are ion implanted and then cleaned. A heat treatment of 1050°C for 30 minutes in N_2 is used. As soon as possible after the heat treatment, Al metallurgy is applied in the form of dots, .080 cm, in diameter, by evaporation followed by a post metallization annealing treatment of 400°C for 30 minutes in N_2.

B. Measurement Technique

The electron current is induced in the SiO_2 using avalanche injection from the Si (3, 4). A feedback circuit is used between the output of the electrometer and the 500 khz square wave generator to control the amplitude of the square waves and keep the current in the SiO_2 constant at a value that is preset as desired. As trapping occurs, the square wave amplitude is automatically increased to compensate for the effect of the trapped charge. The square waves are interrupted periodically to measure automatically the flat-band voltage as a means for monitoring the trapped charge build up in the SiO_2. In the course of a typical run 400 - 600 measurements are made. These data are fed into a computer and the results are analyzed to provide information concerning the trap cross sections and the trap densities. The computer program can resolve two different traps if their cross sections are separated by at least a factor of 2. The analysis of the results follows the same proceedure followed by DiMaria, Aitken and Young (5). The SiO_2 current used depends on the cross sections of interest and in this particular experiment the range was 9×10^{-10} to 9×10^{-9} A. The largest current is used for the small cross section traps. The change in flat band voltage is given by

$$\Delta V_{FB} = \frac{Q_T \overline{X}}{C_{ox} D_{ox}} \tag{1}$$

where C_{ox} is the SiO_2 capacity D_{ox} is the SiO_2 thickness, Q_T is the trapped charge and $\overline{X}$ is the centroid of the trapped charge as measured with respect to the Al-SiO_2 interface. The flat-band voltage measurement does not enable us to determine Q_T and $\overline{X}$ independently and as a result we refer to an effective charge given by

$$Q_E = \frac{Q_T \overline{X}}{D_{ox}} \tag{2}$$

Ning (6) has shown that these considerations do not effect our measurements of the trap cross sections.

We obtain the cross sections and the effective trap densities by fitting exponentials to our data. The cross section is given by

$$\sigma = \frac{q}{\tau I} \tag{3}$$

where τ is the time constant of the exponential, I is the current density and q is the charge on the electron.

The magnitude of the exponentials gives us the effective density of the traps. The charge centroid correction must be used to obtain the actual density.

The implanted Al profiles have been calculated using the LSS range statistics of Gibbons, Johnson and Mylroie (7). Their data have been corrected for the lower density of our SiO_2 as compared with fused silica. The factor used is .84. These profile calculations are shown in Fig. 2. It can be seen that for our thinnest sample (D_{ox}=490 Å) penetration of the Al into the Si should be appreciable for an implantation energy of 20 keV. Results are presented indicating that substantial penetration actually occurs even for the 15 keV implantation.

If we substitute the expression for the SiO_2 capacity into eq. 1, we obtain for the flat band voltage shift

$$V_{FB} = \frac{Q_T \bar{X}}{\epsilon_{ox}} \tag{4}$$

where ϵ_{ox} is the dielectric constant of SiO_2. This relationship is independent of D_{ox} and thus we see that V_{FB} should not depend on D_{ox} if Q_T and $\bar{X}$ are independent of D_{ox}. We assume that this is the case if the implanted Al does not reach the Si-SiO_2 interface.

C. *Experimental Results*

We have compared our trapping results on implanted samples with non implanted, but otherwise identical, samples and we find a large increase in the trapping rate, indicating that we can neglect the traps present in the non-implanted SiO_2.

The experimental results are given in Fig. 3 for D_{ox} = 1400 Å, Fig. 4 for D_{ox} = 730 Å and Fig. 5 for D_{ox} = 490 Å. In the case of Fig. 3 (1400 Å), we see a large increase in the trapping (ΔV_{FB}) as the implantation energy increases, a significant but smaller increase is noted in Fig. 4 (730 Å) and in Fig. 5 (490 Å), it is seen that the trapping actually decreases for implantation energies above 20 keV. The change in these results with D_{ox} is due to the penetration of the Al into the Si. This is shown by Fig. 6 where ΔV_{FB} is seen to be a function of D_{ox} and not independent of D_{ox} as predicted by eq. 5. This penetration occurs for D_{ox} = 730 Å at 30 keV.

The large increase in trapping with the implantation energy (V_I) shown by Fig. 3 (D_{ox} = 1400 Å) is a surprising result. The average shift (ΔV_{FB})AVG taken from these data is plotted as a function of implantation energy (V_I) on a log-log plot in Fig. 7 and we see that the slope is 2 indicating that the trapping varies as V_I^2. The increase in the charge centroid ($\bar{X}$) has been shown by DiMaria to be proportional to V_I and our result can not be explained solely on this basis.

A summary of the measured trap densities and cross sections is given in Table I. The total effective trap concentration observed is 3.5 x 10^{12} cm^{-2}. The charge centroid measurments of DiMaria et al. indicate the $\bar{X}/D_{ox}$ = .44 for this case. Using this correction results in an actual trap density of 8.33×10^{12} cm^{-2} as compared with the implanted fluence of 1×10^{13} cm^{-2}.

III. Discussion of Results

Our results for the thick SiO_2 ($D_{ox} = 1400$ Å) which does not allow penetration of the Al through the SiO_2 into the Si shows that the trapping varies as the square of the implantation energy. The charge centroid measurements suggest a first power dependence. As a result, we conclude that the number of traps is proportional to the implantation energy. This leads to the conclusion that the trapping we are observing is related to implantation damage in the SiO_2 even though we have annealed our samples at temperatures of 1050°C.

The trap cross sections associated with this damage have been characterized and the predominant cross sections observed are 1.26×10^{-16} and 1.40×10^{-17} cm^2.

ACKNOWLEDGEMENTS

The authors are indebted to A. B. Fowler and M. I. Nathan for reading the manuscript, to E. J. Petrillo and J. A. Kucza for growing the oxides, to E. D. Alley and A. Cramer for applying the electrodes, to H. F. Lazzari for the Al implantation.

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TABLE I

Trap cross sections (σ) and effective densities (N_t) for the traps resulting from a 30 keV Al implant with a fluence of 1×10^{13} at/cm^2 and $D_{ox} = 730$ Å.

σ(cm^2)	N_t(cm^{-2})
1.60×10^{-15}	4.60×10^{11}
1.26×10^{-16}	1.14×10^{12}
1.40×10^{-17}	1.40×10^{12}
1.26×10^{-18}	5.00×10^{11}

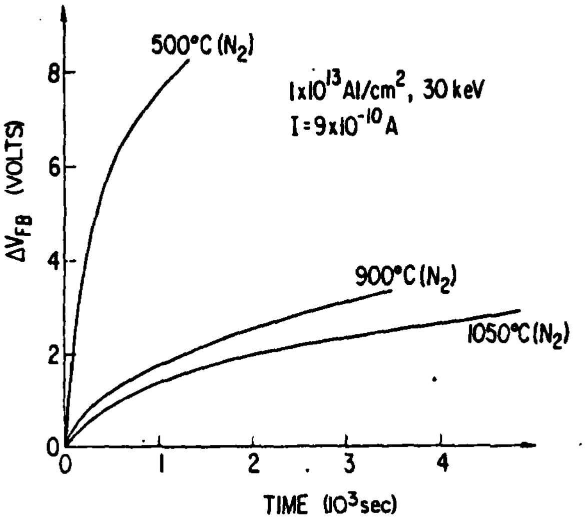

Figure 1 Flat-band voltage shift as a function of time for various annealing temperatures. The annealing time is 30 minutes.

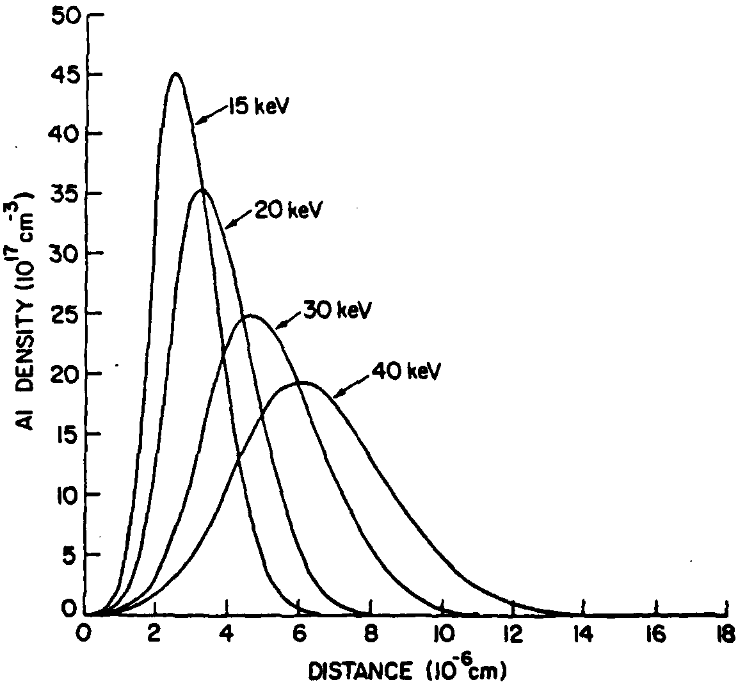

Figure 2 **Aluminum concentration profiles calculated using LSS theory for various implantation energies. The fluence is 1 x 10^{13} at/cm^2.**

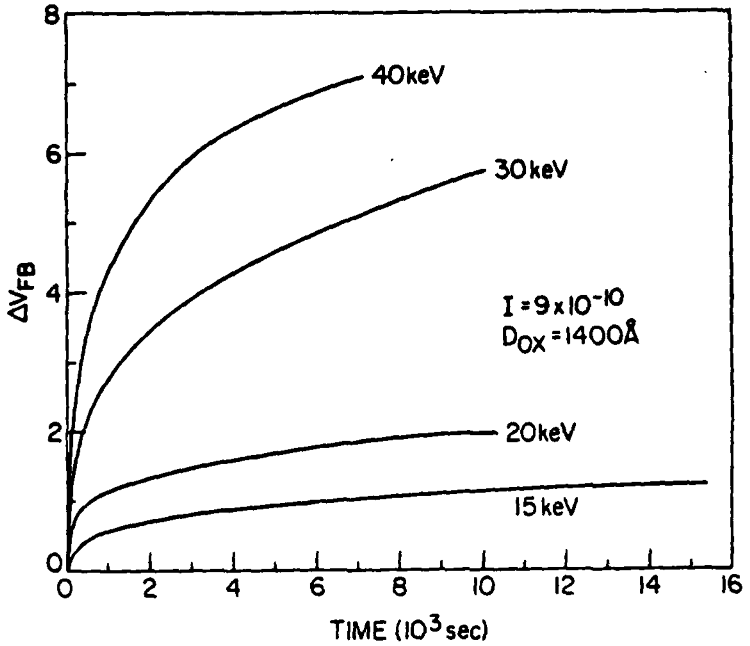

Figure 3 Flat-band voltage shift as a function of time for various implantation energies.

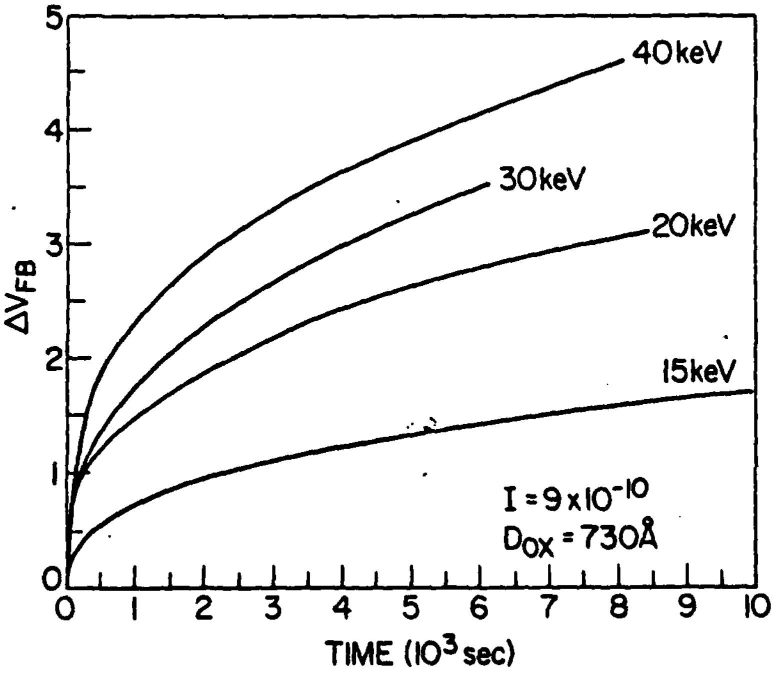

Figure 4 Flat-band voltage shift as a function of time for various implantation energies.

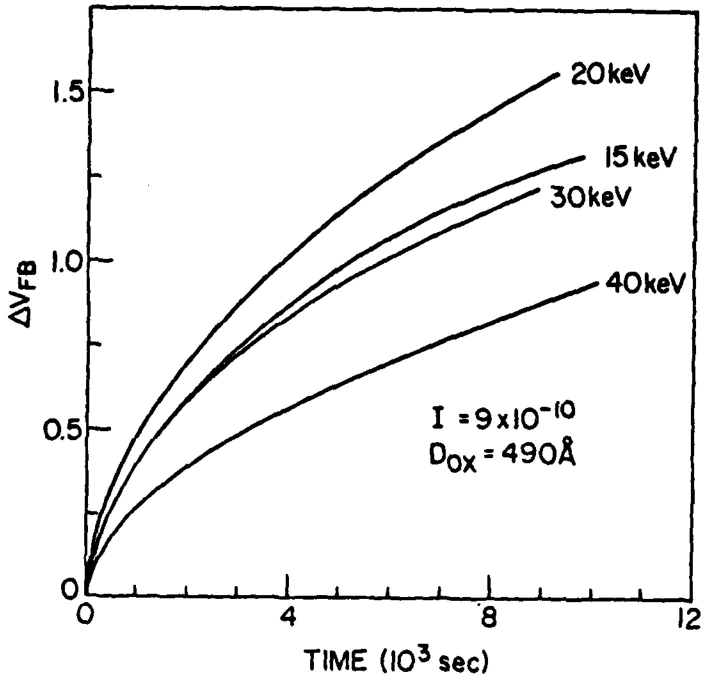

Figure 5 Flat-band voltage shift as a function of time for various implantation energies.

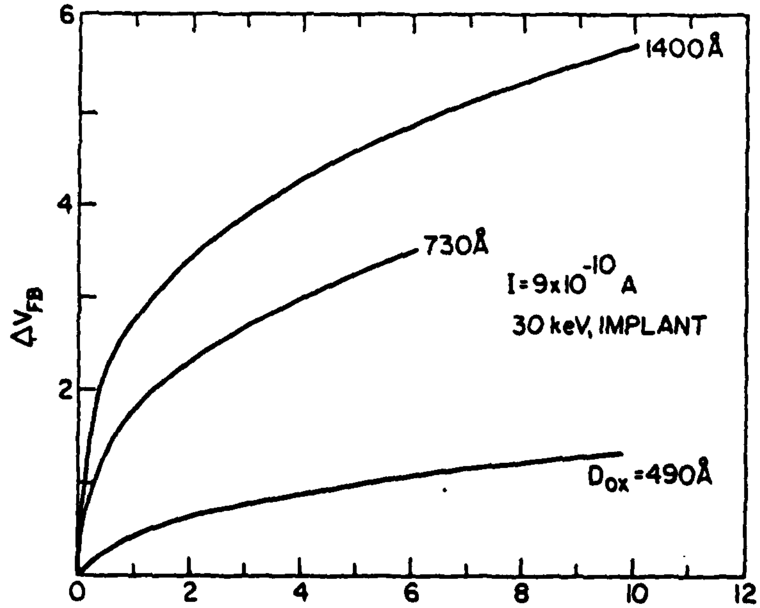

Figure 6 Flat-band voltage shift as a function of time for various SiO_2 thicknesses.

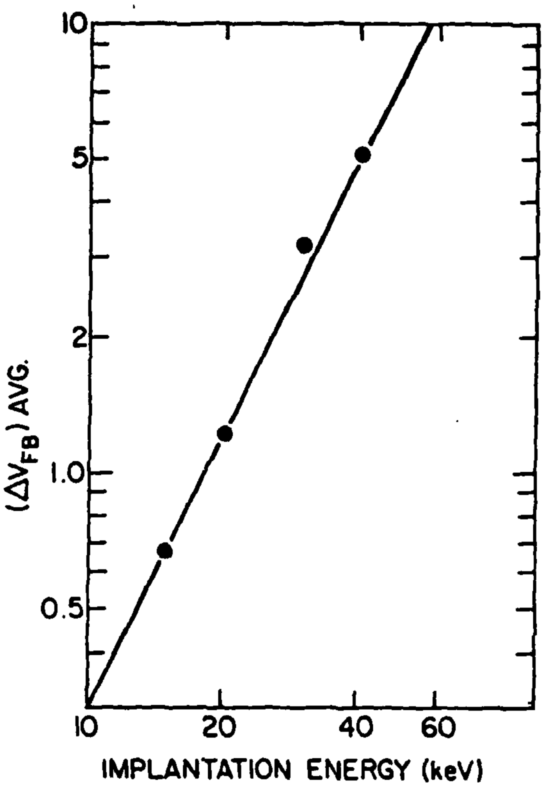

Figure 7 Log-Log plot of the average flat-band voltage shift taken to 6500 sec. as a function of implantation energy.

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ELECTRON TRAPPING RESULTING FROM ALUMINUM IMPLANTATION INTO SiO_2: CHARGE LOCATION *

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Abstract:
The centroid of electrons trapped on sites resulting from aluminum implantation into SiO_2 has been measured using the photo I-V technique for energies from 15-40 keV, oxide thicknesses from 490-1400 Å, and pre-metalization annealing temperatures from 600-1050°C in N_2 for 30 minutes. The centroid and the distribution of the trapped electrons were found to be identical to those of the implanted aluminum from SIMS measurements, regardless of annealing temperature from 600 to 1050°C, and in shallower from the Al-SiO_2 interface by < 90 Å than predicted from the LSS calculations of Gibbons, Johnson, and Mylroie. The trapping behavior of these sites is discussed in the previous paper by Young et al.

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* This research was supported in part by the Defense Advanced Research Projects Agency, the Department of Defense and was monitored by the Deputy for Electronic Technology (RADC) under contract No. F19628-76-C-0249.

The centroid of trapped electronic charge resulting from traps introduced by Al implanted into the SiO_2 layer of metal-oxide-semiconductor (MOS) structures has been investigated using the photo I-V technique developed by DiMaria (1). The technique is nondestructive and has a sensitivity of less than 10^{11} trapped charges/cm^2. The MOS structures had SiO_2 thicknesses of 490 Å, 730 Å, and 1400 Å. Implantation energies of 15, 20, 30 and 40 keV and post-implantation annealing conditions from 600°C to 1050°C in N_2 for 30 minutes were used.

The Al implanted MOS structures are in approximately a net neutral charge state after the processing described in the previous article by Young et al. [2]. To use the photo I-V technique which depends on the internal fields due to trapped insulator charge, the traps in the SiO_2 layer must be charged. This is accomplished by injecting electrons using avalanche of the Si substrate (3) or internal photoemission (4) from either the Si or semi-transparent metal contacts. As described previously [2], some of these electrons are trapped on sites related to the implanted Al. Without the implanted Al, no noticeable electron trapping is seen under similar injection conditions.

The photo I-V technique has been discussed in detail in recent publications [1, 5-7], and only the principle features and their application to this problem will be discussed here. Figures 1 and 2 show typical photo I-V data for both polarities on a control and charged MOS structure with a 1400 Å SiO_2 layer implanted with a fluence of 1×10^{13} Al/cm^2 at 20 keV and annealed at 1050°C in N_2 for 1/2 hour prior to metallization. From the parallel voltage shifts for postive gate bias ΔV_g^+ and for negative gate bias ΔV_g^- between the I-V curves in Figs. 1 and 2, the centroid $\bar{x}$ and trapped negative charge/cm^2 Q/e were determined from the photo I-V relations [1] $\bar{x}/L=[1-(\Delta V_g^-/\Delta V_g^+)]^{-1}$ and $Q/e=\varepsilon(\Delta V_g^- - \Delta V_g^+)/(eL)$ where L is the SiO_2 thickness, e is the electronic charge, and ε is the static dielectric constant of SiO_2. For the data of Figs. 1 and 2, the centroid and trapped charge density were determined from the photo I-V relations to be 330 Å and 3.4×10^{12} electrons/cm^2, respectively.

The photo I-V data were reproducible on any given sample and from sample to sample. Displacement current effects were negligible. These effects have been discussed in detail in recent publications [1, 5]. These displacement currents can arise from additional charge trapping or from photodetrapping while performing the photo I-V measurements. Because of the low capture probability (defined as the product of the capture cross section and the number of empty traps per unit area) which is $<10^{-3}$ for sites related to the implanted Al discussed in the previous article by Young et al. [2], charge trapping effects were negligible. Photodetrapping effects were negligible (except in one case) for the energies used here (4.5 or 5 eV) and will be discussed later. Complete capacitance-voltage (C-V) curves were recorded prior to and after both the charging and the photo I-V measurements. Flat-band voltage shifts deduced from these C-V curves were identical to the positive gate bias photo I-V shift ΔV_g^+ to within a few tenths of a volt. This is consistent with a bulk trapped charge distribution since C-V measurements are more sensitive to charge at the Si-SiO_2 interface than photo I-V measurements [1, 8].

The sample preparation was discussed previously [2]. However, in this study only thin (100 - 150 Å) Al electrodes were used to allow penetration of the incident light through the Al into the Si substrate so that internal photoemission currents (on which the photo I-V technique is based) were generated. The experimental set-up for the photo I-V measurements has been reported before [9].

In Figure 3, the centroid measured from the metal-oxide interface ($\bar{x}$) is plotted as a function of Al implant energy in the range of 15-40 keV for oxides with thicknesses of 490 Å, 730 Å, and 1400 Å. The points in this figure connected by dashed lines are deduced for the *negative trapped charge* from the photo I-V experimental technique. All samples in this figure were charged by avalanche injection from the Si substrate at current levels of 9×10^{-10} or 9×10^{-9} A [2]. The other lines are calculated for the *implanted Al* using LSS theory (10). Each experimental point in Figure 3 represents the average of $\bar{x}$ over many samples. For all samples in Figure 3, the fluence was 1 x 10^{13} Al/cm^2 and the post-implantation annealing was carried out at 1050°C for 30 minutes in N_2. As seen in this figure, there is some discrepancy between the experimental results and the LSS calculations for all energies and oxide thicknesses (the photo I-V results show the centroid closer to the Al except for $\bar{x}$ at 15 keV on the 730 Å and 1400 Å samples). The roll-off and pinning of $\bar{x}$ at the higher energy implants on the thinner oxide samples (for all energies on the 490 Å samples and for 30 and 40 keV on the 730 Å samples) is due to a significant fraction of the Al penetrating into the Si substrate which is not sensed by the photo I-V technique. Otherwise, the data points should be independent of SiO_2 thickness. In addition to the pinning effect, the loss of Al to the Si also reduces the trapping that is observed as discussed in the companion paper by Young et al. in this issue [2]. The LSS theoretical plots also show deviations when Al is lost to the Si substrate, but this occurs at higher implantation energies than the experimental results.

The experimental conditions were varied to see what effect they had on the centroid of the negative trapped charge. These centroids were found largely independent of the following experimental variables:

1. *Amount of trapped charge* - in the range from 10^{11} to 10^{12} electrons/cm^2.
2. *Injection mechanism to fill traps* - avalanche or internal photoemission from the Si substrate, or internal photoemission from the Al electrode; except for a small anomolous effect observed for the sample with a 40 keV implant into a 1400 Å oxide which will be discussed later.
3. *Post-implant annealing conditions* - from 600°C to 1050°C for 1/2 hour in N_2.
4. *Fluence of Al* - from 5 x 10^{12} to 2 x 10^{13} Al/cm^2.
5. *Oxide thickness* - in the range from 490 Å to 1400 Å if the Al does not penetrate into the Si substrate.

Items (1) and (4) were anticipated from the low capture probabilities (less than one out of every thousand electrons injected into the SiO_2 layer is captured) of the implanted Al related trapping sites as discussed in Young et al. [2]. Item (3) was not expected. Since much more trapping under identical injection conditions was observed on the 600°C annealed samples as compared to the 1050°C annealed samples [2], it was expected that part of the additional trapping would be caused by atomic displacement damage and move the centroid towards the Al-SiO_2 interface. This was not the case. Annealing from 600°C to 1050°C, only removes some of the trapping sites surrounding the implanted Al distribution as will be discussed next.

The photo I-V experiments presumably sensed *negative charge trapped* on sites *related* to the *implanted Al* . To confirm this experimentally and also profile the *implanted Al* distribution in the oxide layer, secondary ion mass spectroscopy (SIMS) was employed where the primary ion beam was O^+ and a sputtering rate of ≈ 2 Å/sec was used on the SiO_2 layer. The samples were 770 Å of thermal SiO_2 on Si implanted with an Al fluence of 1×10^{13} cm^{-2} at 20 keV. The SIMS measurements showed that the profile of the implanted Al was largely independent of post-implant annealing conditions (unannealed as compared to a 1050°C anneal in N_2 for 30 min.). Figure 4 shows a profile of the implanted Al as measured using SIMS and compares it to the profile calculated from LSS theory. $\bar{x}$ determined from the SIMS data of Figure 4 is given in Table 1 for 490 Å and 730 Å thick SiO_2 layers and is compared with values determined from the photo I-V measurements and the LSS calculations. The centroids determined from the photo I-V and SIMS measurements are in good agreement for the two different oxide thicknesses to within the sample to sample variation. This implies that the distribution of the negative trapped charge (from photo I-V) is the same as the implanted Al (from SIMS). Figure 4 also shows that the full width at half maximum for the SIMS data is $\approx$ twice as large as calculated. This is consistent with observations of Chu et al. for heavier ions at higher energies in thermal SiO_2 layers using He^+ ion backscattering techniques [11, 12]. This broadening of the distribution implies that more Al should be lost to the Si substrate on thinner SiO_2 samples and that the measured values of $\bar{x}$ should progressively deviate more with the LSS calculations as the oxide is made thinner. As mentioned previously, the former trend is seen in Figure 3 where the roll-over due to Al penetration into the Si substrate is predicted by the LSS calculations to occur at somewhat higher implantation energies than observed experimentally. The latter trend is seen in Table 1 and Figure 3. In Figure 3, the largest deviations with the LSS calculations for all energies occur on the 490 Å thick SiO_2 samples (≈ 70 Å to 90 Å from 15 keV to 40 keV).

Attempts were made to photodetrap electrons trapped on the sites related to implanted Al with energies below the conduction band edge in the range from 1 - 5.5 eV. As discussed in a previous publication [1], the gate and substrate were grounded and the internal field of the negative trapped charge was used to favor photodetrapping and block internal photoemission of electrons from the contacts at energies >3 eV which would repopulate discharged trapping sites. Neither the full spectrum of a 900 watt xenon high pressure lamp nor the spectrum of a 60 watt deuterium lamp (which has a broad peak at ≈5.5 eV) with a 5.5 eV low frequency pass filter (to prevent possible hole injection from the contacts and trapping) for times as long as hours were successful in removing many trapped electrons in any of the samples discussed here. In the most extreme case on the MOS structure with a 1400 Å SiO_2 layer and implanted at 40 keV, ≈16% of the total trapped charge which was 2.9×10^{12} cm^{-2} was removed with the deuterium lamp. The centroid of the charge removed was ≈70 Å in deeper from the Al-SiO_2 interface than the charge remaining, originally trapped under avalanche injection conditions from the Si. As mentioned earlier (see item 2-*injection mechanism*), only this sample (1400 Å SiO_2, 40 keV implant) showed a pronounced dependence of the centroid position on injection mechanism. The centroid moved up to ≈ 125 Å closer to the Al-SiO_2 interface for trapped electron densities from 1×10^{11} to 1×10^{12} cm^{-2} when photoinjecting from this interface with 4.5 eV light to fill traps. These two experimental observations are consistent with each other and imply that photodetrapping can explain the anomaly mentioned in item 2. This photodetrapping was observed to be influenced by the local fields [13-15] and optical interference patterns [15] and/or the light energy in the SiO_2 layer since the centroid measured by the photo I-V technique varied somewhat under photoinjection conditions (injecting interface and light wavelengths used).

Our results can not be compared readily with those of Johnson et al. [16] (Al implanted at 20 keV with a fluence of 10^{14} cm^{-2} into a 1400 Å SiO_2 layer) since most of their measurements and analysis of flat-band voltages and photocurrents were on *unannealed* MOS structures. They deduced a centroid for trapped space charge injected from the Si-SiO_2 interface at 670 Å from the Al-SiO_2 interface and observed that this space charge could be photodetrapped at energies ≥ 4 eV. They correctly concluded that the centroid was in deeper from the Al-SiO_2 interface than expected because every injected electron from the Si-SiO_2 interface was captured (capture probability of unity). This favors charge build up near the injecting interface regardless of the overall spatial distribution of oxide traps. They also concluded that a substantial fraction of the electron traps were due to displacement damage. Our use of high temperature annealing treatments and lower fluences avoided the problems encountered by Johnson et al. [16].

In summary, the centroid of electrons trapped in the SiO_2 layer of an MOS structure resulting from aluminum implantation has been located by the photo I-V technique. This centroid and the trapped electron distribution are essentially identical to those of the implanted Al as determined by SIMS measurements and independent of annealing temperature from 600°C to 1050°C. For implantation energies from 15-40 keV, the centroid was found to be in fair agreement with those predicted by the LSS calculations of Gibbons, Johnson, and Mylroie [10]. Similar studies to those presented here and in the previous paper by Young et al. on other ions with different masses should further increase our understanding of the interactions of ion beams with amorphous solids on the scale of angstroms.

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TABLE I

Centroid Comparison for a 20 keV Al implant into SiO_2.

OXIDE THICKNESS (Å)	CENTROID (Å)		
	PHOTO I-V	SIMS	LSS
490	265	274	335
730	320	346	367

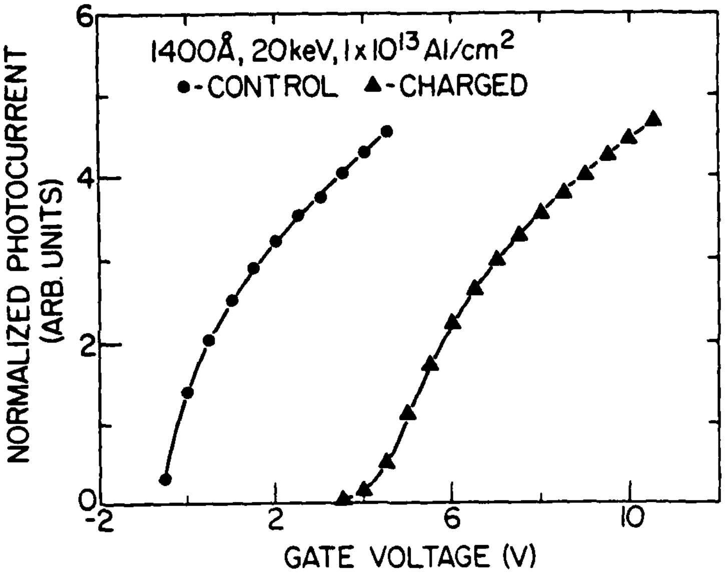

Figure 1 Normalized photocurrent (photocurrent divided by area and intensity) for 5 eV light as a function of positive gate voltage (Si injecting): •-control, ▲- charged by electron avalanche injection from the Si substrate. The MOS structure had a 1400 Å SiO_2 layer, 20 keV and 1 x 10 ^{13} Al/cm^2 implant, and was annealed at 1050°C for 1/2 hour in N_2 prior to metallization.

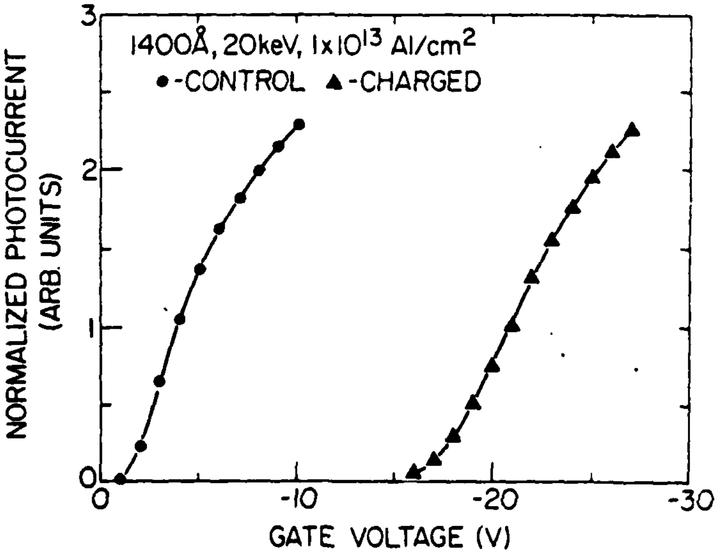

Figure 2 Normalized photocurrent for 4.5 eV light as a function of negative gate voltage (Al injecting). Samples are the same as in Figure 1.

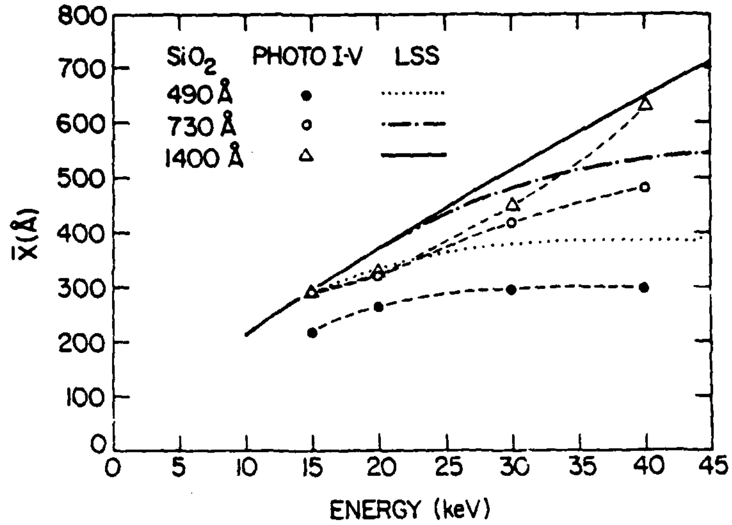

Figure 3 $\bar{x}$ as a function of Al implantation energy from 15-40 keV for 490 Å, 730 Å, and 1400 Å thick SiO$_2$ layers. The points •, o, and Δ are experimental values for the trapped negative charge distribution using the photo I-V technique and the lines ••••, •-•-•, and ——— are the values predicted by LSS theory for the implanted Al distribution. All samples were charged by avalanche injection of electrons from the Si substrate.

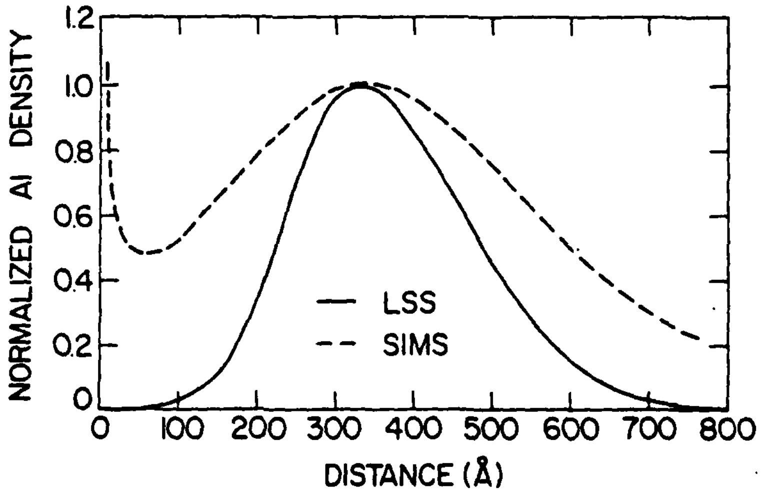

Figure 4 Normalized Al density for a 20 keV implant energy and a fluence of 1×10^{13} cm^{-2} as a function of distance from the air-oxide interface into a 770 Å thick SiO$_2$ film. The normalization factor was the peak value of the Al density in the film. The dashed and solid lines are the profiles determined from SIMS measurements and LSS theory, respectively.

E-BEAM ENHANCED ELECTRON TRAPPING IN SiO$_2$[*]

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ABSTRACT

Electron irradiation of MOS capacitors with 25 KeV electrons is reported to introduce additional uncharged electron traps into the oxide layer. These traps persist after most of the positively charged defects introduced by the ionizing electrons have been removed by the usual low temperature ($\leq$400 C) anneals. Their presence in the oxide is determined by avalanche injection of hot electrons. Observed electron capture cross-sections range between 10^{-15} to 10^{-18}cm^2. Effective trap densities increase with increasing dosage of 25 KeV electrons and are reduced by forming gas anneals at temperatures in excess of 550 C. After a 400 C post-irradiation anneal, oxides exposed to 10^{-4} coul-cm^{-2}. of 25 KeV electrons exhibit a total additional effective trap density of ~ 5 x 10^{11} distributed over these cross-sections. The traps are possibly associated with dipolar defects formed when valence electrons localize around an ion after the bonds are broken.

[+] work done as M. I. T. summer co-op student.

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I. INTRODUCTION

Studies of radiation damage in MOS devices are concerned usually with the rate at which the oxide layer traps positive charge or accumulates surface states in a given radiation environment.[1, 2] This information is required to know how long a given device with its unique processing history will operate reliably in such an environment. However, when ionizing radiation (electron beam fabrication, lithography reactive ion etching, etc., RIE, ion implantation) is used repeatedly in the processing steps themselves to fabricate the device, the concern is that the damage can be completely eliminated at each stage in the fabrication. This is particularly important in conjunction with the enhanced hot-electron emission probability in the projected small geometry (~ 1μ) devices fabricated by these processes. Additional oxide defects may act as electron traps leading to shorter device lifetimes. Studies of damage by ionizing radiation in bulk glasses show that it consists partly of structural damage to the SiO_2 lattice.[3, 4] The positive charge associated with some of these centers is removed by low temperature[5, 6] (<400 C) anneals. Until now it has been assumed that with the removal of this charge, the oxide has been restored to its original state. Data presented here will show that in addition to these positively charged defects, neutral defects which act as electron traps are introduced into the oxide by irradiation. These centers persist despite anneals at temperatures in excess of 550 C leading to enhanced trapping of hot-electrons in the SiO_2 layer of MOS capacitors.

The presence of additional neutral electron traps in the oxide layer of MOS devices exposed to ionizing radiation has only recently come to light.[7] Low energy electrons or photons ($\leq$ 1 MeV) lose energy in the SiO_2 layer principally by promoting SiO_2 valence electrons to excited states.[8] Momentum transfer at these energies is not sufficient to cause lattice displacements, but if these excitations are larger than the SiO_2 band gap (9 ev), bonds may be broken. Both the electrons[9] and holes[10] created in such an event are quite mobile and drift toward the interfaces where the holes are trapped at pre-existing process-related sites.[11, 12]

Although the events and energies involved in the production of positively charged defects are well-understood, little is known about the generation of neutral defects in the oxide. Positively charged centers in MOS devices are obvious from careful measurements of flat-band (capacitors) or threshold (FET) voltages. But these charged defects are almost completely removed by low temperature anneals and are not the prime concern. Since the charge state of the neutral defect after anneal precludes observation by capacitance-voltage measurement alone, electrons are injected into the oxide where a small fraction are captured by the defects resulting in an observable voltage shift in the C-V curve. The shift of the capacitance curve on the voltage axis as electrons are injected is analyzed to determine the cross-section for electron capture, and the effective trap density. The dependence of the effective trap density on electron beam fluence, annealing temperature, and injection temperature is also studied.

II. EXPERIMENT DESCRIPTION AND SAMPLE PREPARATION

These experiments were performed on aluminum gate MOS capacitor structures which remained intact throughout the irradiation and annealing processes. Aluminum dots 33 mils in diameter were evaporated from an r-f heated crucible through a shadow mask onto a 440 Å thick layer of $Si0_2$, grown in dry 0_2 at 1000 C on a .2 ohm-cm p type <100> silicon substrate. After metal deposition the capacitors received a 400 C, 20 minute anneal in a 90% N_2, 10% H_2 *forming* gas mixture for 20 minutes. After fabrication some of the wafers from this batch were irradiated in an electron-beam lithography system while others were kept as unirradiated controls. Individual capacitors on the same wafer were subjected to a fluence of 25 KeV electrons. The dosage was varied between 10^{-5} to 10^{-4} coul-cm^{-2} and was calculated from the known beam current, exposure area and exposure time. At this energy, the maximum range of electrons in aluminum is ~ 5 μ so that a substantial portion of the incident electrons penetrate into the $Si0_2$[13]

The samples were given a post-irradiation anneal in forming gas at temperatures in excess of 400 C. Flat-band voltages and surface state densities were checked after this step. Within the limits of accuracy for absolute flat-band determination (± 50 mV) the flat-band voltage had been restored to its pre-irradiation value. A comparison of quasi-static C-V measurements before and after post-irradiation anneal showed that surface state densities at mid-gap had been reduced to slightly below their original value. This is consistent with previous experiments on irradiated MOS capacitors and FET's.[1, 2, 14] Following the anneals, some of the electrons generated in the avalanche plasma of the substrate by a positive voltage pulse at the gate are injected into the oxide where a small fraction of them ($\leq 10^{-4}$) are captured by the existing defects. The resulting shift in flat-band voltage is a direct measure of the effective densities of the traps and the rate at which the shift occurs is determined by their electron capture cross-section.

The particular techniques[15, 16] and apparatus[7, 11] used to inject electrons has been described previously. A constant average electron current is maintained by a feed-back loop which automatically raises the amplitude of the high frequency (> 10 KHZ) sawtooth voltage waveform on the gate compensating for the change in the field at the injecting interface caused by the trapped charge. Periodically the current injection process is stopped and the flat-band voltage is measured by an automatic circuit in less than 4 seconds. The data are recorded directly into an IBM VM168 computer via an IBM Research Device Coupler. Each individual experiment consists of several hundred to a thousand data points. This allows very accurate determination of cross-sections and trap densities from the time evolution of the flat-band shift at a particular current level. Data analysis will be discussed in a subsequent section.

Experimentally the total effective number of traps occupied by electrons after a charge Q has been passed through the oxide (or after a time t at a current density j) is

$$N_{EO} = \frac{C_{OX} \Delta V_{FB}}{e} \qquad (1)$$

where $Q = \int_0^t j \, dt'$, e is an elementary electronic charge, C_{ox} is the oxide capacitance per unit area, and ΔV_{FB} is the measured shift in flat-band voltage caused by the injected charge. The effective charge density is defined by

$$N_{EO} = \frac{\bar{X}\,N}{L} \tag{2}$$

where $\bar{X}$ (measured from the aluminum interface) is the centroid of the total charge density N and L is the oxide thickness.[17] Separate experiments can be done to determine $\bar{X}$ but they will not be discussed here.[18] Only the product of $\bar{X}$ N is measured in these experiments. The data presented here are displayed in the format described by equation (1).

III. EXPERIMENTAL RESULTS

Increasing the total fluence of 25 KeV electrons from 10^{-5} to 10^{-4} coul-cm^{-2}, results in increased effective densities of filled traps at any given value of avalanche injected charge. This is illustrated in figure 1 for capacitors which were irradiated to the indicated dosage, annealed and subjected to electron injection at room temperature. The increase in N_{EO} exists despite the fact that these samples were given a 400 C, 30 minute post-irradiation forming gas anneal. (All the anneals described here were performed in a forming gas ambient). Over this range of dosages the density of unannealed radiation-induced traps was proportional to the dosage. Background trapping typical of these oxides is shown for an unirradiated control wafer. The control was not annealed further after the post-metal anneal used in fabricating all these capacitors. (Anneals at 400 C had negligible effect on the background trapping in the controls although some additional decrease in surface states occurred.) Reproducibility of these results on other *similarly treated wafers from* the same batch was excellent. The graphical format using the logarithm of injected charge is necessary to display the data because the additional electron traps created by irradiation have a range of cross-sections between 10^{-13}cm^2 and 10^{-18}cm^2. These trapping cross-sections are listed along with the appropriate effective trap densities in Table I and will be discussed later. Since the flat-band shifts observed here are considerably larger than the 50 mV upper limit for positive charge *established by initial* capacitance measurements, the extra traps introduced by irradiation are neutral. Two more accurate measurements in these samples show that no more than 2.2 x $10^{10}cm^{-2}$ (40 mV) of the unannealed trapping centers are positively charged. These will be discussed at a later time.

The curves in figure 1 were obtained by first injecting charge at low currents into the oxide and measuring the flat-band shifts. When the shift rate decreased sufficiently at this current level (indicating that traps in this range had saturated), the current was increased. Samples were avalanched first at 4 x 10^{-8} A-cm^{-2} for approximately 20,000 seconds and then at 4 x 10^{-5} A-cm^{-2} for approximately 10,000 seconds.

Low temperature (77 K) and room temperature (295 K) trapping behavior is shown in figure 2 for two capacitors given identical exposures (10^{-4} coul-cm^{-2} at 25 KeV) and post-irradiation anneals (400 C for 30 minutes in forming gas). These capacitors are contrasted with those for unirradiated controls subjected to electron injection at these two temperatures. At room temperature the samples were avalanched at two current levels to speed the filling of the lower cross-section traps and allow accurate tracking of flat-band voltages. These current levels were 2 x 10^{-7} A-cm^{-2} and 1 x 10^{-5} A-cm^{-2}. At liquid nitrogen temperature because both the irradiated and control samples contain large densities of shallow traps which fill rapidly at 77 K a lower current of 1 x 10^{-7} A was used.

Note that in both cases the total density of traps in the irradiated capacitor at any given value of injected charge is greater than in the appropriate control capacitor. The flat-band voltages for all four capacitors were checked at 77 K by monitoring the voltage at which the freeze-out dip in the high frequency C-V characteristic[19], readily visible on such highly doped samples, appeared. The particular samples from which the data in figure (2) were obtained had flat-band voltages of -.940 volts while the control samples had flat-band voltages of -.900. All samples measured were within this range (as were the others measured on these wafers) but no more than .040 volts of the excess trap density in figure 1 or 2.2 x $10^{10}cm^{-2}$ is due to this additional positive charge. Previous measurements on radiation-induced positive[12] and on oxide charge[20] present in as-grown films indicate that the positively charged defect captures electrons with a field-dependent cross-section of 10^{-12} to $10^{-15}cm^{-2}$ Since a maximum field of 4 MV/cm was present across the oxide during the 295 K measurement, the cross-section for electron capture is greater than $10^{-15}cm^2$. All the positive charge will have been annihilated when 5×10^{15} electrons cm^{-2} have been injected. The excess total effective filled trap density (difference between the trap density of the irradiated and annealed sample and the control sample) at this charge level is $6 \times 10^{10}cm^{-2}$ indicating that some neutral traps with this cross-section are also filling. The situation is similar for 77 K but since the current was lower than that used at 295 K, the oxide field was no greater than 3 MV/cm and the electron capture cross-section for positive charge was greater than $5 \times 10^{-15}cm^2$. In this case, positively charged centers are 87% filled when a charge of $1 \times 10^{15}cm^{-2}$ is injected. Again the number of filled traps at this level is substantially greater than that expected from positive charge alone.

As seen in figure 2, the traps introduced into the oxide by irradiation span a large range of known electron trapping cross-sections in SiO_2, i.e., from $10^{-13}cm^{-2}$ to $10^{-18}cm^{-2}$. The total effective density of filled traps at a given value of injected charge is then[17]

$$N_{EO} = \sum_i N^i_{ES} (1 - \exp(-\sigma_i Q))$$

where N^i_{ES} is the saturated effective density of the i^{th} trap and σ_i is its cross-section. By analyzing the rate at which the effective trap density shifts with time over a limited range of Q, curves such as those shown in figure 1 and 2 may be analyzed for N^i_{ES} and σ_i. This is possible since a large number of data points (~ 500) are taken on each of these curves. The details of this procedure are described elsewhere[7, 11] but the analysis is performed by a computer program which iteratively chooses values of N^i_{ES} and σ_i for two exponentials to minimize the standard deviation between the actual data and the calculated curve. Standard deviations of less than 5×10^9 traps-cm^{-2} are typical of the results. Such an analysis was performed on the four capacitors from which the data in figure 2 were obtained and others like them. Reproducibility between these samples was excellent, although a small field dependence was noted. This is consistent with the reported field dependence of positive and neutral centers generated during e-beam aluminum deposition in polysilicon gate FET's reported by Ning.[21] The cross-sections and effective trap densities derived in the analysis are displayed in Tables I and II for trapping at room temperature and liquid nitrogen temperature respectively. These results were obtained from data generated at the lowest currents feasible for measuring the cross sections of interest in a reasonable time. Traps A and B have been noted previously in irradiated but unannealed samples of this type.[7] Traps D and E have been discussed previously by many authors[15] and are thought to be related to water in the oxide.[22] The trap densities of all these centers are increased by the irradiation and not removed by this anneal at 400 C.

Generally, the traps in the irradiated and control capacitors can be characterized at both temperatures by the same cross-sections. The increase in the effective trap density caused by irradiation is given in the last column of the table. Note that in Table I and II this increase ΔN^{i}_{ES} is approximately temperature independent. In this respect the radiation induced neutral traps differ dramatically from the traps (D and E) which exist in the native oxide prior to irradiation. This is an indication that radiation induced traps are fundamentally different from those in the as-grown oxide. The native oxide traps also exhibit an unusual phenomena in both irradiated and unirradiated samples. Although they capture 3-4 times more charge at 77 K than at 295 K, the traps do not empty when warmed to room temperature. After 16 hours at room temperature with the gate grounded less 10% of the traps had released electrons.

Extending the period of anneal at 400 C had little further effect on reducing the number of traps generated in the oxide by exposure to 10^{-4} coul-cm^{-2} of 25 KeV electrons. After the thirty minute anneal at 400 C, successive isochronal anneals at 450 C and 500 C were given similarly irradiated capacitors on the same wafer so that the third capacitor measured had seen heat treatments at three temperatures. After each anneal the effective density of filled traps was measured as a function of injected charge and the wafer re-annealed. The results are presented in figure 3. The three curves are labelled by the maximum temperature *in the anneal* history seen by the particular capacitor. A general decrease in the number of traps is noted but even the 500 C anneal does not reduce trapping to pre-irradiation (control) levels. No higher temperature anneals were attempted with these samples, since aluminum begins to react with and diffuse through the oxide more rapidly at higher temperatures. From similar results on polysilicon gate capacitors on which no aluminum is present over the gate oxide, an anneal temperature of around 600 C appears necessary to remove these defects completely. This point has significant technological importance since real devices fabricated by electron-beam lithography are limited to low temperature anneals after deposition of the aluminum metallurgy.

IV. DISCUSSION

The nature of the uncharged defects caused by ionizing radiation is unknown. However, measurements of the residual stresses on SiO_2 films on silicon substrates by EerNisse and Norris[22] have shown that stresses induced by ionizing radiation are removed in a well-defined stage at 650 C. These authors attribute this component of the damage to broken bonds in SiO_2 tetrahedra. In these experiments the temperatures required to anneal these defects leads to a similar model and possibly an identification of these same defects as trapping sites. When bonds are broken, valence electrons can localize primarily at one site leading to a light relaxation of the surrounding lattice. This has been speculated for E′ defect centers in SiO_2[23] and defects in polar materials.[24] This forms an automatically compensated dipole-like defect. To re-establish the original bonds, additional thermal energy is required to remove the lattice deformation. Capture cross-sections for this defect would be lower than those for a strictly coulombic center, due to the shorter affective range of the dipole potential and increase as the separation between the poles. The effective capture radius of a trapping center is related to its capture cross-section by $r=(\sigma/\pi)^{1/2}$. Using the cross-section of 1.6 x 10^{-5}cm^2 as representative of traps with maximum distance between poles we arrive at a capture radius of 2.3 Å.

Separation between the poles can be estimated from the theoretically derived expression for a dipolar electron trap. On the basis of a distance of active attraction model Belmont[25] has derived the expression

$$\sigma \simeq \frac{e^2\delta}{32kT\varepsilon}$$

where e is an elementary electronic charge, δ is the separation between poles, k is Boltzmann's constant, T is the absolute temperature and ε is the dielectric constant of the medium. Substituting the appropriate values for SiO_2 at room temperature and using the largest value for σ ($2 \times 10^{-15} cm^2$) as representative of the dipole with largest separation we arrive at $\delta \simeq .4$ Å. Since the Si-O bond distance is approximately 2 Å, this number is certainly reasonable.[26] It should not, however, be taken too seriously since the theory predicts a temperature dependence to σ which is not observed. However, it does indicate that displacements on the order of .5 Å or less can explain the observed cross-sections. These displacements are also consistent with the residual stresses observed in irradiated MOS structures.[22]

As mentioned earlier, the temperature independence of the electron-induced traps sets them apart from those present in the oxide prior to irradiation which tend to be "shallow" at least as far as electron capture is concerned. The electron re-emission from the native oxide traps is not understood but is speculated to be due to lattic relaxation around the shallow electron trap once it has captured an electron at 77 K. These relaxations tend to self-trap the electron at the site.[24]

The exact atomic nature of the defect is unclear but a doubly charged oxygen vacancy may be responsible. The evolution of atomic oxygen from SiO_2 has been noted previously.[26, 27] If such a vacancy were to capture a doubly negative charge, it could act as a neutral electron trap. Whatever the nature of defect, it may be associated with structural or chemical imperfections in the SiO_2 existing prior to irradiation. If this is indeed the case some process optimization may be used to control them. This will be the subject of another publication. However, the phenomena do appear to be quite general in nature, appearing in both poly-silicon and aluminum gate devices.

V. CONCLUSIONS

We have shown that residual radiation damage in the form of neutral electron traps exist in the oxide layer of MOS capacitors even after most of the trapped positive charge introduced by irradiation has been removed. The density of these traps increases with total electron-beam exposure over the range of electron beam dosage necessary to expose e-beam resists (10^{-5} - 10^{-4} coul-cm^{-2}). The traps are possibly associated with dipole-like defects introduced into the oxide by the irradiation. Anneal temperatures in excess of 550 C are required to remove all evidence of damage from the oxide after irradiation. This presents a significant problem in cases where aluminum metallurgy is in place as part of the device structure during irradiation.

ACKNOWLDGEMENTS

The authors wish to express gratitude to Drs. T. H. P. Chang, W. Grobman and the Electron Beam Lithography Application Group for irradiating these samples and to Drs. C. Osburn, J. Blum and the Silicon Process Studies Group for fabrication of the samples. Drs. A. B. Fowler, and B. L. Crowder are thanked for a critical reading of the manuscript.

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TABLE I - TRAPPING PARAMETERS AT 295 K

		IRRADIATED$^+$ & ANNEALED^{++}		CONTROL		
TRAP	CHARGE	σ_i(cm^2)	N^i_{ES}(cm^{-2})	σ_i(cm^2)	N^i_{ES}(cm^2)	ΔN^i_{ES}(cm^{-2})
A	+	1.2x1o^{-14}	~2.0x10^{10}	~1.0x10^{-14}	~.5x10^{-10}	1.5x10^{10}
B	0	1.6x10^{-15}	4.4x10^{10}	——	——	4.4x10^{10}
C	0	2x10^{-16}	8.4x10^{10}	——	——	8.4x10^{10}
D	0	7x10^{-18}	2.58x10^{11}	3x10^{-17}	1.88x10^{11}	7.0x10^{10}
E	0	1x10^{-18}	4.7x10^{11}	1.4x10^{-18}	2.6x10^{11}	2.1x10^{11}

+ 10^{-4} 10^{-4}coul-cm^{-2} at 25 KeV

+ + 400°C 30 min in 90%N_2, 10%H_2

TABLE II - Trapping Parameters at 77 K

		IRRADIATED$^+$ & ANNEALED^{++}		CONTROL		
TRAP	CHARGE	σ_i(cm^{+2})	N^i_{ES}(cm^{-2})	σ_i(cm^{+2})	N^i_{ES}(cm^{-2})	ΔN^i_{ES}(cm^{-2})
A	+	$1x10^{-14}$	$3x10^{10}$	$1.6x10^{-14}$	$1x10^{10}$	$2x10^{10}$
B	0	$1.7x10^{-15}$	$9.3x10^{10}$	$1.6x10^{-15}$	$4.7x10^{10}$	$4.6x10^{10}$
C	0	$1.4x10^{-16}$	$6.1x10^{11}$	$1.0x10^{-16}$	$5.2x10^{11}$	$8.7x10^{10}$
D	0	$1.9x10^{-17}$	$8.9x10^{11}$	$1.7x10^{-17}$	$7.9x10^{11}$	$1.0x10^{11}$
E	0	$1.0x10^{-18}$	$10.6x10^{11}$	$1.0x10^{-18}$	$7.8x10^{11}$	$2.8x10^{11}$

\+ 10^{-4}coul-cm^{-2} at 25 KeV

++ 400°C, 30 min in 90%N_2, 10%H_2

FIGURE CAPTIONS

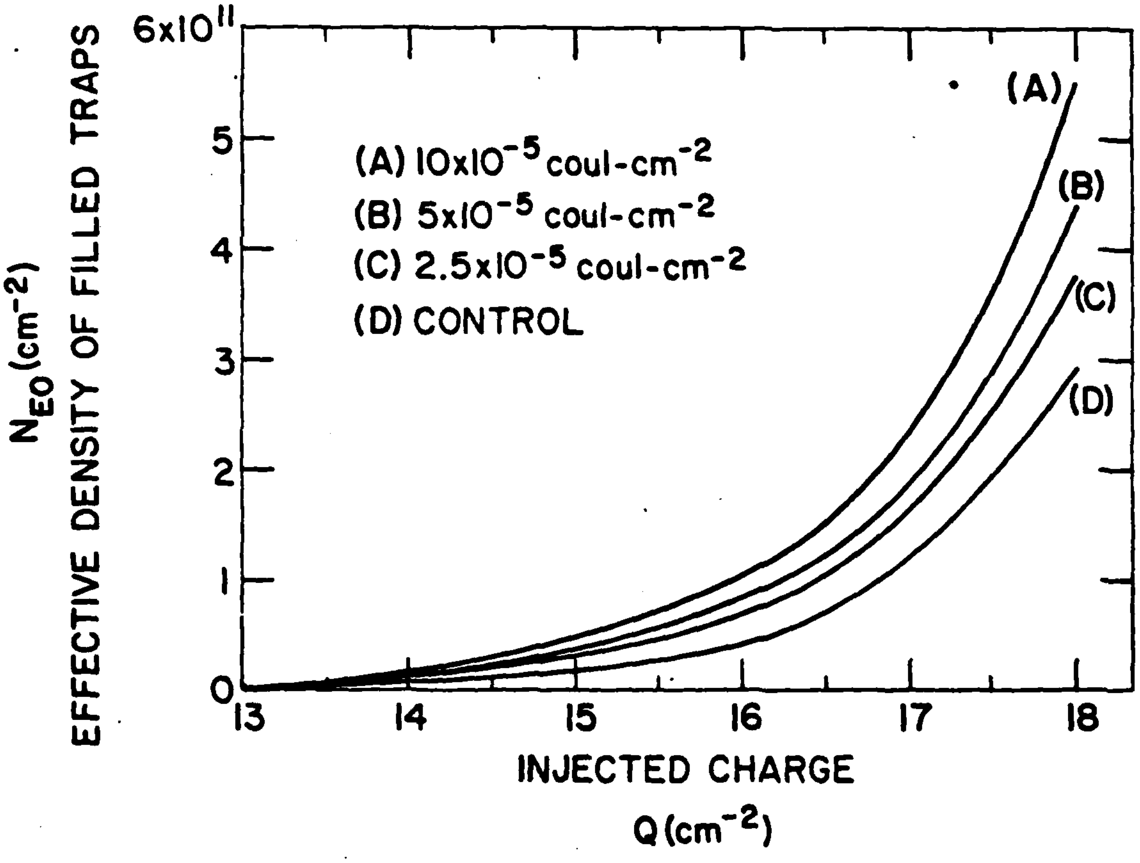
Figure 1 Effective density of filled traps plotted as a function of injected charge for aluminum gate capacitors with an oxide thickness of 440 Å which had been subjected to various fluences of electron-beam irradiation and then annealed at 400 C for 30 minutes in a forming gas ambient.

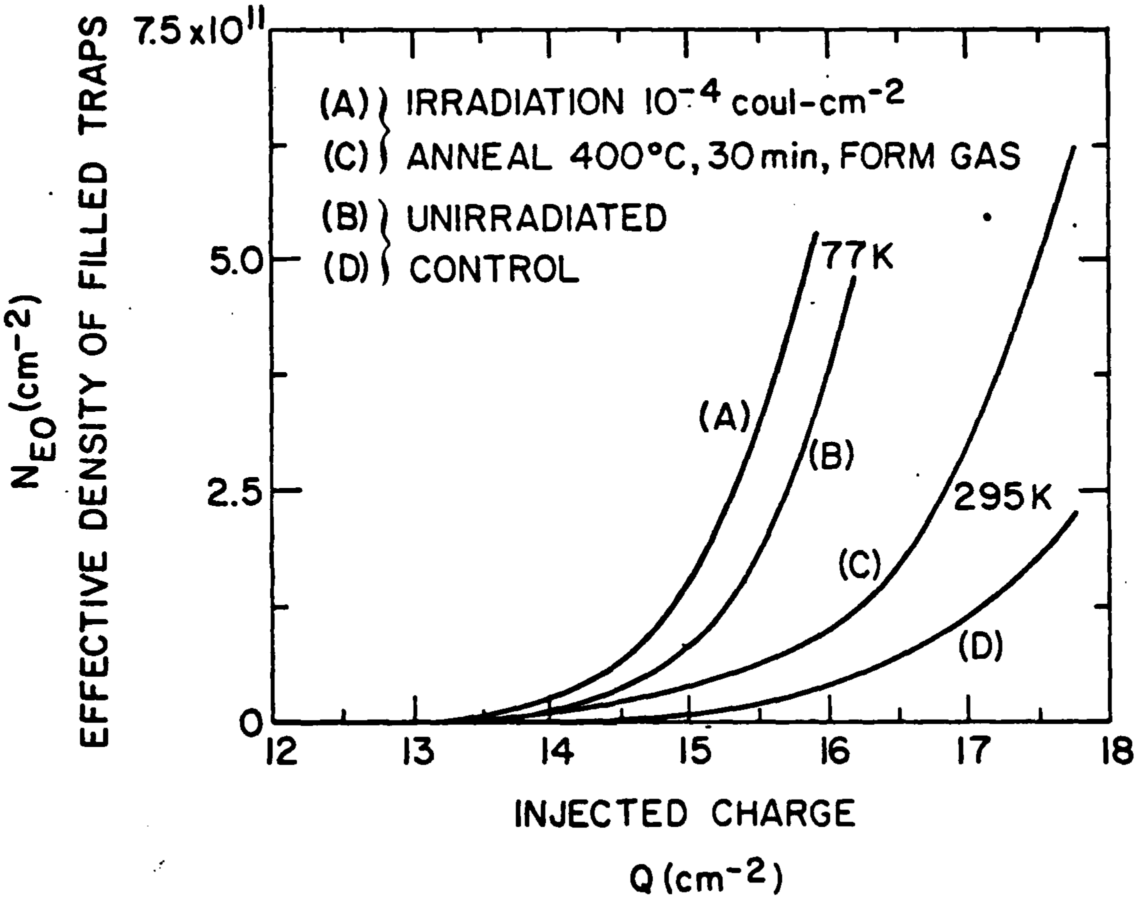
Figure 2 Effective density of filled traps plotted as a function of injected charge for aluminum gate capacitors with an oxide thickness of 440 Å which had been (1) irradiated with 10^{-4} coul-cm^{-2} of 25 KeV electrons; (2) annealed at 400 C for 30 minutes in forming gas; (3) injected with electrons at either 295 K or 77 K. A control sample was also injected at each of these two temperatures for comparison.

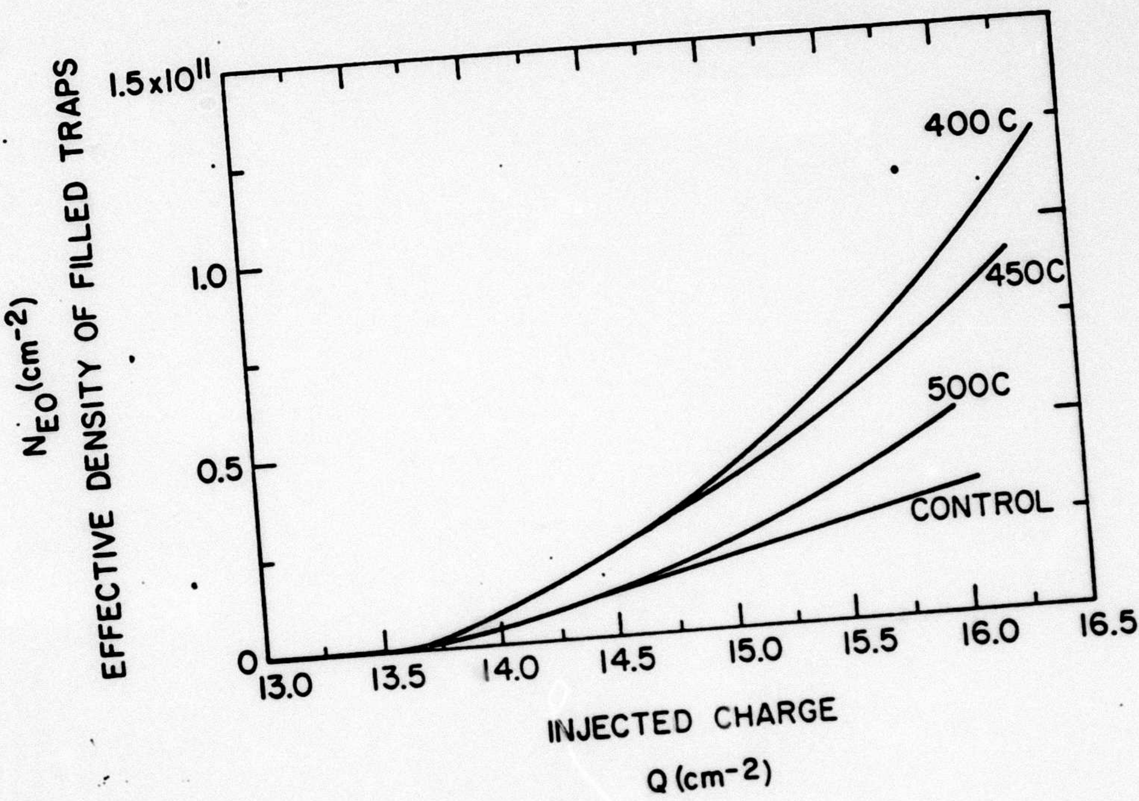
Figure 3 Effective density of filled traps plotted as a function of injected charge for aluminum gate capacitors with an oxide thickness of 440 Å. After irradiation with 10^{-4}coul-cm^{-2} 25 KeV electrons, the capacitors were given cummulative anneals at successively higher temperatures to reduce the density of neutral traps. The anneal history for the samples is as follows:

400 C	30 min	forming gas
400 C	30 min	forming gas
450 C	30 min	forming gas
400	30 min	forming gas
450	30 min	forming gas
500	30 min	forming gas

The highest temperature in the anneal history was used to label the data in the figure.


6x10^11
5
4
3
2
1
0
N_EO (cm^-2)
EFFECTIVE DENSITY OF FILLED TRAPS
(A) 10x10^-5 coul-cm^-2
(B) 5x10^-5 coul-cm^-2
(C) 2.5x10^-5 coul-cm^-2
(D) CONTROL
(A)
(B)
(C)
(D)
13
14
15
16
17
18
INJECTED CHARGE
Q (cm^-2)


7.5 x 10^11
5.0
2.5
0
12
13
14
15
16
17
18
(A) IRRADIATION 10^-4 coul-cm^-2
(C) ANNEAL 400°C, 30 min, FORM GAS
(B) UNIRRADIATED
(D) CONTROL
77 K
295 K
(A)
(B)
(C)
(D)
N_EO (cm^-2)
EFFECTIVE DENSITY OF FILLED TRAPS
INJECTED CHARGE
Q (cm^-2)


N_{EO} (cm^{-2})
EFFECTIVE DENSITY OF FILLED TRAPS
1.5x10^{11}
1.0
0.5
0
13.0
13.5
14.0
14.5
15.0
15.5
16.0
16.5
INJECTED CHARGE
Q (cm-2)
400 C
450C
500C
CONTROL

RC 6609 (#27899) 3/31/77 (Rec'd 6/29/77)
7 pages

USE OF ELECTRON TRAPPING REGION TO REDUCE LEAKAGE CURRENTS AND IMPROVE BREAKDOWN CHARACTERISTICS OF MOS STRUCTURES *

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Abstract:
A trapping layer of W ($\approx 10^{14}$ atoms/cm^2) has been deposited between 70 Å of thermal silicon dioxide grown grown from a polycrystalline silicon substrate and 520 Å of deposited pyrolytic silicon dioxide in an MOS structure to reduce high leakage currents and low voltage breakdowns associated with asperities at the polycrystalline Si-thermal SiO_2 interface. MOS structures without the W layer but with the pyrolytic SiO_2 layer were also found to be effective. This improvement is ascertained to be due to localized electron trapping in the W or pyrolytic oxide layer at low average fields which reduces the locally high fields and therefore high dark currents associated with the asperities. At higher average fields uniform trapping is believed to be dominant. This uniform effect can also enhance the breakdown characteristics if the trapped charge is not detrapped by the applied field.

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Asperities or defects on the silicon surface are generally thought to increase insulator leakage current and lead to low voltage breakdowns in metal-oxide-semiconductor (MOS) devices. This has been dramatically shown for thermal oxides grown on top of polycrystalline silicon [1, 2, 3] which are important for various types of devices based on Si technology, such as the Floating Avalanche Injection MOS (FAMOS) [4], Rewritable Avalance Injection Device (RAID) [5], and Charge Coupled Device (CCD) [6]. It is believed that these asperities cause locally high fields to occur which in turn lead to localized high dark current densities (via interface limited, Fowler-Nordhiem tunneling) [1, 2] and low voltage breakdown. By reducing the high field points or their effect, an improvement in leakage current and breakdown voltages is expected [3]. One way to accomplish this is to incorporate a charge trapping layer in the structure. This layer would capture some of the electrons injected at the high field points, thereby reducing the local field and current in turn. We report here a series of experiments using a charge trapping layer on top of thermal oxides grown on polycrystalline silicon which we believe show this concept.

The metal-oxide-semiconductor (MOS) structures used here were the following, and will be designated by A, B, and C:

A: Al-thermal SiO_2(450 Å)-poly Si(3.5×10^{-3} Ωcm n)

B: Al-pryolytic SiO_2(520 Å)-thermal SiO_2(70 Å)-poly Si(3.5×10^{-3} Ωcm n)

C: Al-pyrolytic SiO_2(520 Å)-W($\approx 10^{14}$ atoms/cm^2)-thermal SiO_2(70 Å)-poly Si(3.5×10^{-3} Ωcm n)

The deposition of the polycrystalline silicon on degenerate n single crystal silicon, doping of the polycrystalline silicon, and subsequent thermal oxidation, has been described previously [1]. The deposition of the tungsten (W) trapping layer and the pyrolytic oxide layer have also been described in detail in current publications by the authors [6, 7]. The circular aluminum gate electrodes had areas of 1.3×10^{-2} cm^2 and were approximately 3000 Å in thickness. No post-metallization annealing was performed. All oxide thicknesses were determined by MOS capacitance.

The dark current-applied gate voltage characteristics were measured on virgin samples using a constant voltage ramp or by stepping the voltage. For the constant voltage ramp experiments, ramp rates of $5.1\text{x}10^{-2}$ MV/cm-sec or $9.5\text{x}10^{-3}$ MV/cm-sec were used with a Keithley No. 29000 logarithmic picoammeter. Voltage was ramped in the direction of increasing the magnitude of either positive or negative bias until a current level of $8 \text{ x } 10^{-7}$ A/cm^2 was reached and then the ramp direction was reversed (see direction of arrows on data in Figures 1 and 2). The data of Figures 1 and 2 have been corrected for the displacement current ($\approx 3.5 \text{ x } 10^{-9}$ A/cm^2) due to the time rate of change of the gate voltage. The initial starting voltage for the ramp experiments was when electronic conduction currents began to dominate over the displacement current. In the voltage step experiments, the magnitude of the average field was increased from 0 V in 1 MV/cm steps for both gate polarities until the sample suffered destructive breakdown. Currents, measured using a Keithley 417 high speed picoammeter, were recorded 1 minute after each step increase. Although there were some detailed differences in the current-voltage characteristics due to differences in trapped negative charge buildup in the structures, the two experimental techniques yielded the same general results that are discussed here. I-V data were reproducible from capacitor to capacitor. Some voltage breakdown measurements were performed (see Figures 3 and 4) using the voltage ramping techniques of Osburn and Ormond [8].

Figures 1-4 clearly show that a charge trapping layer removes the effect of locally high fields due to asperities at the polycrystalline silicon-thermal silicon dioxide interface. In Figures 1 and 2, the magnitude of the average field (gate voltage magnitude divided by the total oxide thickness of the structure) required for a given current measured in the external circuit is larger when an electron trapping layer is present for either voltage polarity. Note that structure C (with the W layer) is better than structure B (without the W layer). This is consistent with the experimental observation that the trapping efficiency of the structure with the W layer (C) is greater than the structure with just the pyrolytic oxide (B) [6, 7]. I-V characteristics for both structures B and C which have a 520 Å pyrolytic silicon dioxide layer are shifted to much higher average fields than structure A. The increased trapping efficiency of the structure with the pyrolytic oxide layer on the thermal oxide layer (B) over the structure with just thermal oxide (A) grown on the polycrystalline silicon substrate is thought to be related to the water content of the pyrolytic oxide. The I-V characteristics of structures B and C are in the range of those for MOS structures which have thermal oxides grown from silicon crystal silicon substrates [1, 9, 10].

The sequence of events occurring in structures B and C to reduce the effect of asperities is believed to be as follows:

(1) At low applied gate voltages, localized trapping occurs to rapidly remove the effect of the asperities.

(2) As the field is increased, uniform trapping occurs which shifts the I-V characteristics to higher average fields.

From the step voltage I-V measurements, localized trapping appeared to occur for structures B and C at very low current levels ($\leq 7.9 \times 10^{-12}$ A/cm^2) and low applied fields (≤ 2 MV/cm) for either polarity. Near this current level, there was a pronounced departure of the I-V characteristics for structures B or C from that of A. This departure appeared as a ledge (1.5 to 2 MV/cm wide) where the current increased very slowly up to a level of between 7.9×10^{-12} A/cm^2 and 3.9×10^{-11} A/cm^2. This ledge was wider for structure C (with the W layer) than for structure B. After these ledges, uniform trapping appears to be the dominant factor in controlling the I-V characteristic. The data of Figures 1 and 2 are representative of this uniform trapping behavior.

The hysterisis in these data is due to electron trapping. Data similar to Figures 1 and 2 on an MOS structure with a 563 Å thermal oxide grown from a single crystal n-degenerate silicon substrate showed less hysterisis for either voltage polarity than that observed for negative gate polarity on structure A (see Fig. 2). The amount of hysterisis for either polarity is greatest for structure C, next is B, and smallest for A. The hysterisis for positive gate bias on the structure A (see Fig. 1) has been reported before [1, 5] and is thought to be due to enhanced local trapping in the thermal oxide layer near the high field points due to the large local current densities [1, 2]. In subsequent voltage ramp cycles, all structures showed a memory effect in which negative charge trapping in the previous cycle pushed the I-V characteristic out to higher average fields at the start of the next cycle. The rapid current increase for positive gate bias on structure C, is indicative of the beginning of current runaway near destructive breakdown [8, 9].

If the differences between the I-V data of structures B and C (see Figs. 1 and 2) is due to uniform negative charge trapping in the W layer, one should in principle be able to determine the position of this layer from the voltage shifts between B and C using a technique similar to that recently described for photocurrent-voltage measurements [6]. This photo I-V relationship is [6]

$$\bar{x}/L=[1+(|\Delta V_g^-|/L)/(|\Delta V_g^+|/L)]^{-1} \quad (1)$$

where $\bar{x}$ is the centroid measured from the Al-pyrolytic SiO_2 interface, L is the total oxide thickness of the structure, and $|\Delta V_g^+|$ and $|\Delta V_g^-|$ are the gate voltage shift magnitudes at a constant current level for positive and negative gate bias, respectively. Using equation (1) and the experimental values of $|\Delta V_g^+|/L$ and $|\Delta V_g^-|/L$ from the data of Figs. 1 and 2, the W layer was located at a distance of 72 Å from the poly Si-thermal SiO_2 interface which is in excellent agreement with the measured value of 70 Å. Only the data for current levels less than 3 x 10^{-8} A/cm^2 were used in order to avoid the current runaway region on structure C for positive gate bias (see Fig. 1).

Figures 3 and 4 show the self-healing and the destructive breakdown distributions for positive gate bias (poly-Si injecting) on structure A and C. Both distributions for sample C in Fig. 4 show very few low average field breakdowns which are characteristic of thermally oxided polycrystalline silicon surfaces as shown for sample A in Fig. 3. These histograms in Fig. 4 are in fact very tightly distributed around an average field of ≈8.8 MV/cm for such large area capacitors when compared to thermally oxidized single crystal Si MOS structures [8, 11].

The position of the W trapping layer was picked close to the polycrystalline Si -thermal SiO_2 interface to maximize the field reduction between the negative trapped charge and this interface while simultaneously minimizing the possibility of discharge by field-assisted thermal emission or field emission to the pyrolytic oxide conduction band in the field enhanced region in the pyrolytic oxide layer. However, the W region was chosen far enough away from the polycrystalline Si-thermal SiO_2 interface (>50Å) to prevent back tunneling to the poly-Si.

As seen with structure B, other trapping layers besides W can be used to achieve the current reductions and increases in breakdown voltage presented here. These trapping layers could be formed by ion implantation, evaporation, or chemical vapor deposition. This technique of using a trapping layer to increase breakdown voltages could be used on other capacitor structures besides MOS structures.

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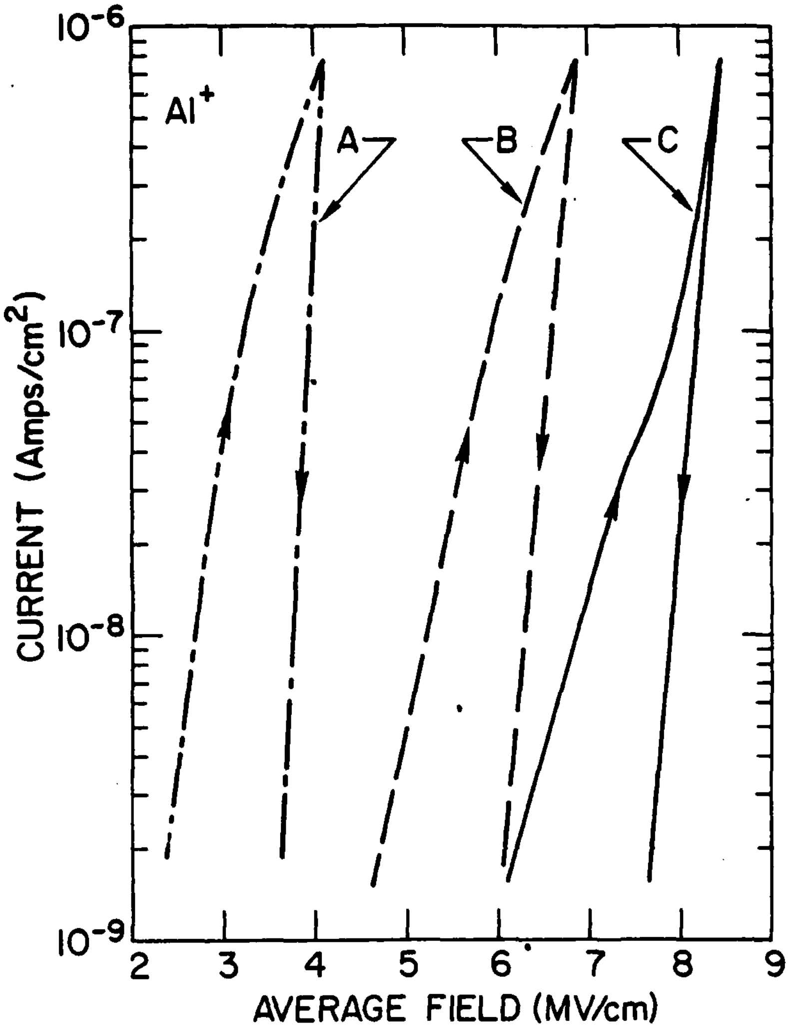

Figure 1 Dark current density measured in the external circuit as a function of the magnitude of the average field for positive gate bias and a ramp rate of 9.5×10^{-3} MV/cm-sec. Composition of samples A, B, and C is described in the text.

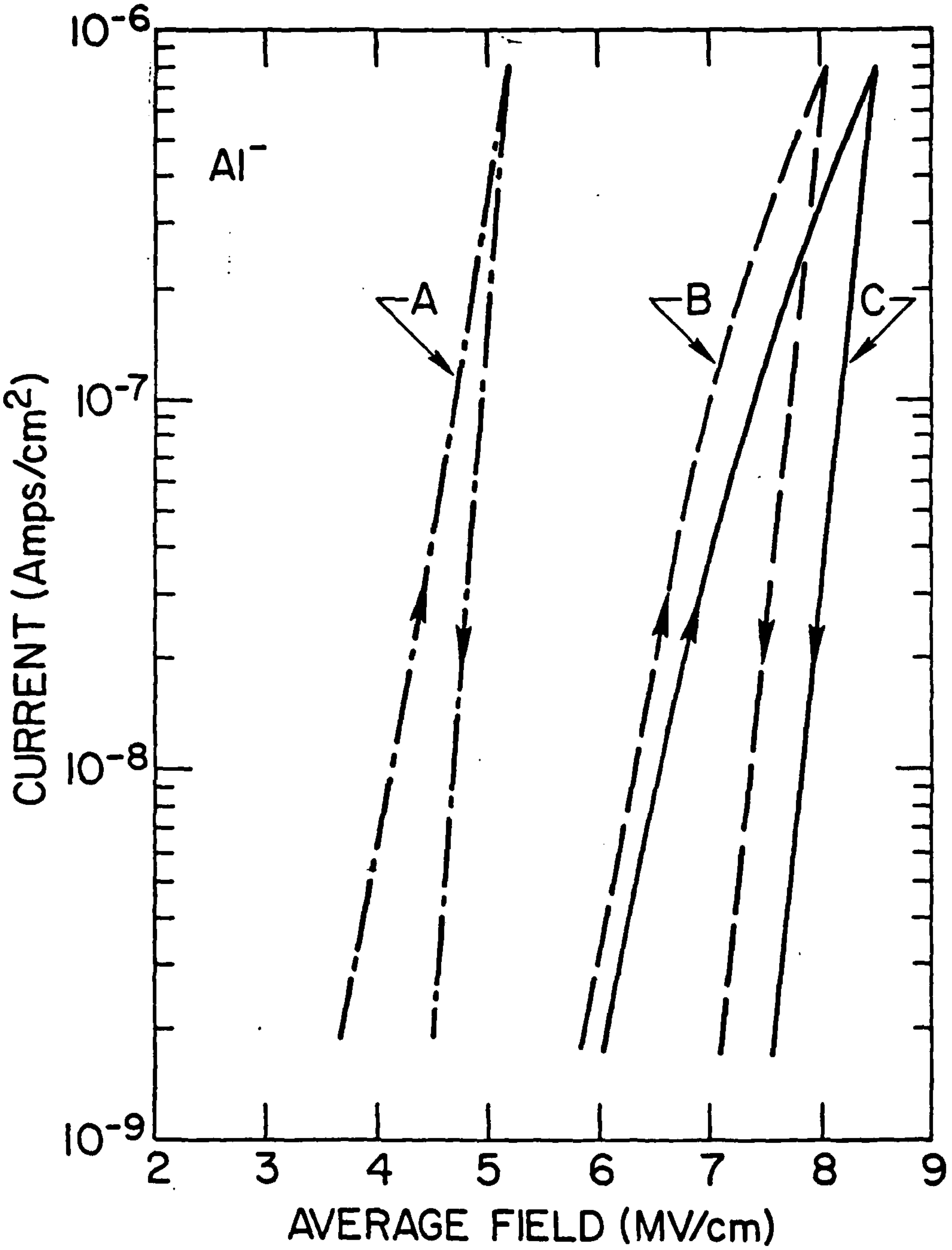

Figure 2 Dark current density measured in the external circuit as a function of the magnitude of the average field for negative gate bias and a ramp rate of 9.5×10^{-3} MV/cm-sec.

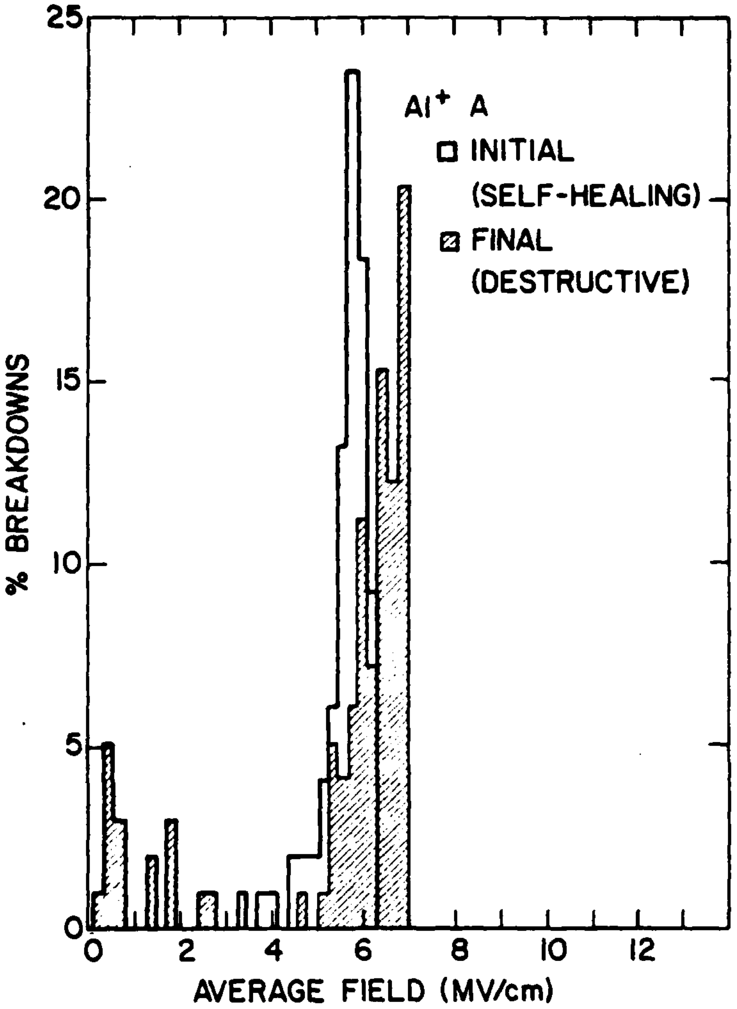

Figure 3 Histogram for sample A of the percentage of dielectric breakdown events as a function of the magnitude of the average field under positive gate bias. For this histogram, 98 virgin samples were tested at a ramp rate of 1 MV/cm-sec.

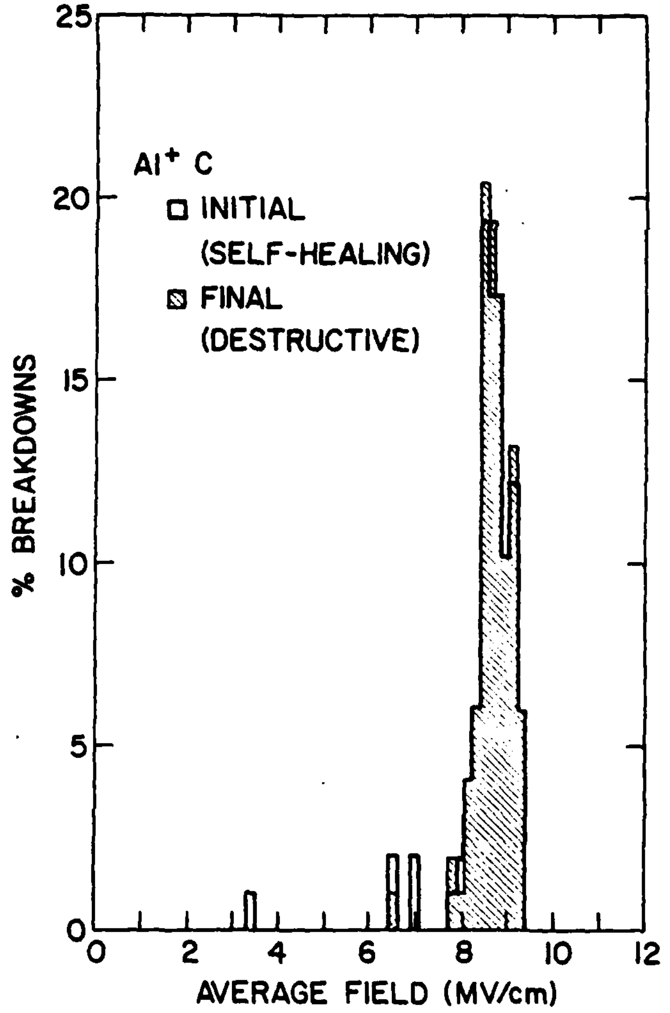

Figure 4 Histogram for sample C of the percentage of dielectric breakdown events as a function of the magnitude of the average field under positive gate bias. For this histogram, 98 virgin samples were tested at a ramp rate of 1 MV/cm-sec.

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Solid State Physics 8 pages

ROOM TEMPERATURE CONDUCTIVITY AND LOCATION OF MOBILE SODIUM IONS IN THE THERMAL SILICON DIOXIDE LAYER OF A METAL-SILICON DIOXIDE-SILICON STRUCTURE*

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Typed by Barbara Fiore on CMC (dd.1054)

ABSTRACT

Room temperature conductivity of mobile Na^+ ions in the SiO_2 layer of a MOS structure is directly shown to be interface-limited by use of the photo I-V technique. Na^+ ions were found to be located within ≈ 50 Å of the interfaces regardless of field stressing conditions (2-4.5 MV/cm), temperature (20-40 °C), number of ions drifted (up to 2.6×10^{12} cm^{-2}), or number of temperature-bias cycles used to move Na^+ ions back and forth between the interfaces.

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Room temperature conductivity of mobile Na^+ ions in the thermal SiO_2 layer of a metal-silicon dioxide-silicon (MOS) structure is investigated in this study using the photo I-V technique [1-4]. In this report, the location of the mobile Na^+ ions as they are moved around in the oxide layer of the MOS structures under different temperature-bias stressing conditions directly shows that the ions are always found near the interfaces (within about 50 Å) regardless of temperature between 20-40 °C, field stressing conditions between 2-4.5 MV/cm, the number of Na^+ ions drifted (up to 2.6×10^{12} cm^{-2}), or number of temperature-bias stressing cycles. This clearly shows that room temperature mobile Na^+ ion conductivity is interface-limited as opposed to bulk-limited. This observation is consistent with those of others who used more indirect capacitance-voltage (C-V) measurements [5,6] which are only sensitive to the charge-centroid product [7,8].

The MOS samples (Al—SiO_2(500Å)—.1 Ωcm p-Si(<100>)) used for the photocurrent measurements were similar to those described in a previous publication [9] except that the Al gate electrode was semitransparent (130 Å) surrounded by a frame region for contacting purposes which was ≈ 17% of the device area. *The rectangular device area was* 3.83×10^{-3} cm^2, and samples where mounted on TO-5 headers. Prior to metallization $\geq 10^{13}$ Na^+ ions/cm^2 were evaporated from NaCl salt onto the outer SiO_2 surface [9]. Na^+ ions can readily move through the SiO_2 layer, but the compensating Cl^- ions are expected to remain at the Al-SiO_2 interface because of their larger size.

The photo I-V technique [1-4] and the experimental set-up [10] have been described in detail in other publications. Na^+ ions were drifted back and forth between the interfaces at temperatures between 20-40 °C, at fields of 2-4.5 MV/cm, and for times from minutes to hours. Flat-band voltage shifts from C-V measurements of 0 to -5.5 V were typical corresponding to Na^+ ion densities up to 2.6×10^{12} cm^{-2}. After temperature-bias stressing, the samples were cooled under bias and vacuum ($\leq 10^{-5}$ Torr) conditions to liquid nitrogen temperature (77 °K) in order to freeze-out any further ionic motion [9] which would interfere with the photo I-V measurements. All photo I-V measurements were performed at 77 °K using an Air Products Heli-Tran low temperature dewar with an optical port and a sample holder for the TO-5 headers made from sapphire (good thermal conductivity, but electrically insulating). The sample holder also had a field shield plate which could be biased if necessary to surpress any extraneous currents due to vacuum external photoemission from any surface exposed to the light beam. Samples were cycled back and forth between 77 °K and 20-40 °C to shift varying amounts of Na^+ back and forth in the SiO_2 layer. Photo I-V measurements were done using 5 eV light for positive gate bias and either 4.5 or 5 eV light for negative gate bias. All results reported here were reproducible on a given sample and from sample to sample. Typical results of any of the measurements are shown in Figs. 1 and 2.

Figures 1 and 2 are photo I-V characteristics [11] after various amounts of Na^+ had been drifted towards the Si-SiO_2 interface or back towards the Al-SiO_2 interface in subsequent cycles at temperatures between 20 °C to 40 °C at fields of $\approx$ 3 MV/cm for times from 5 min. to 40 min. The corresponding flat-band voltage shifts (ΔV_{FB}) deduced from capacitance-voltage (C-V) measurements are listed in the figure captions. These data are characteristic of a given ΔV_{FB} regardless of the number of temperature-bias cycles the sample had undergone or the order in which they were done.

The data in Figs. 1 and 2 are consistent with Na^+ ions distributed near the Si-SiO_2 interface [2-4, 12] for any of the stressing conditions. Fig. 1 (Si photoinjecting) shows increased changes in the shape of the photo I-V characteristic as compared to the control ($\Delta V_{FB}=0$) with increasing flat-band voltage shift magnitude and hence with increasing Na^+ ion concentration. The photo I-V curves in this figure for $\Delta V_{FB} < 0$ are splitting and shifting with increasing field towards lower applied gate bias as has been seen before for positive charge (trapped holes) distributed near the Si-SiO_2 interface [2-4]. Fig. 2 (Al photoinjecting) shows very little difference of the photo I-V curves for any of the cases listed. At higher voltages there is a slight splitting with increasing field of the photo I-V curves where the characteristics are shifted towards more negative voltages. This could be due to negative charge (probably from the uncompensated immobile Cl^- ions) very near the Al-SiO_2 interface or the absence of the Na^+ ions that have been drifted to the Si-SiO_2 interface. Nevertheless, the pronounced differences between Figs. 1 and 2 imply that Na^+ at the Si-SiO_2 interface has a different effect (due to location and possible lack of compensating ions) on the photo I-V characteristic for Si injecting (Fig. 1) than Na^+ at the Al-SiO_2 interface for Al injecting (Fig. 2). Na^+ appears to be approximately at the Al-SiO_2 interface as compared to being distributed near the Si-SiO_2 interface [2-4].

An estimate of the position of the Na^+ centroid from the Si-SiO_2 interface can be obtained by using the low field region of Fig. 2 (oxide voltage drop $\lesssim -4$ V) which is not as sensitive to charge near the Al-SiO_2 interface and by using the photo I-V relation $\Delta V_g^- = (1 - L/\bar{x})\Delta V_{FB}$ as discussed in previous publications [1-4]. Using $\Delta V_{FB} = -3.05$ V, a photo I-V shift ΔV_g^- for Al photoinjecting of $\approx .34$ V or $\approx .16$ V should be observed for a centroid distance from the Si-SiO_2 interface $L-\bar{x}$ of 50 Å or 25 Å, respectively. Clearly, the centroid is closer than 50 Å from the Si-SiO_2 interface from the data of Fig. 2.

Displacement current effects [1,2] due to electron capture at 77°K by Na^+ ions or traps present in the as grown oxide [9] were negligible under the conditions of the photo I-V measurements and had no influence on the shape of the photo I-V characteristics [1,2]. It is interesting to note that because of the very low electron trapping probability of the Na^+ ions (which is $\leq 10^{-3}$ for capture cross sections $\leq 10^{-15}$ cm^2 and Na^+ related trap areal densities of $\leq 10^{12}$ cm^{-2} [9]) dips seen in data similar to Fig. 2 for the case of trapped holes near the Si-SiO_2 interface [2,3] are absent. These dips appeared in the vicinity of the flat-band voltage and were attributed to a displacement current effect as the Si surface potential changed in time due to electron annihilation of trapped holes (trapping probability of ≤ 1 for a field dependent coulombic capture cross section of 10^{-12} - 10^{-15} cm^2 over the range of electric fields of interest and for trapped hole densities of $\leq 10^{12}$ cm^{-2} [2,4]).

For reasons of discreteness of charge and dependence on the internal photoemission model [2, 12-13], the Na^+ ion charge distribution near the Si-SiO_2 interface was not profiled using the data of Fig. 1 and the Powell-Berglund technique [12]. For 10^{12} trapped charges/cm^2 (average separation of 100 Å), discreteness effects become important if these charges are < 20 Å from the photoinjecting interface because of a three-dimensional distribution of the potential near the interface.

Figs. 1 and 2 directly show that there are no significant numbers of Na^+ ions in the bulk of the SiO_2 film for the ion drift conditions studied here. This implies that the transport process of mobile sodium in these MOS structures at temperatures from 20 °C to 40 °C for the stressing times, stressing fields, and amounts of drifted ions is limited by the escape of the Na^+ ions from the interfacial region (interface-limited as opposed to bulk-limited ionic conductivity). This interpretation is also consistent with the experimental observations, using flat-band voltage shifts, that Na^+ ions moved back towards the Al-SiO_2 interface more easily than towards the Si-SiO_2 interface. This interface-limited conductivity is also in agreement with the results of others (for the experimental conditions used here) from more indirect C-V measurements which used flat-band voltage shifts as a function of time and applied voltage to investigate the ionic conduction mechanisms [5,6]. At higher temperatures (>40 °C), there is much experimental evidence for interface limited conductivity using many techniques [14]. All these techniques (thermally stimulated ionic conductivity, charge-time, C-V, threshold voltage shifts of field effect transistors, current-voltage using a slow linear ramp, and radioactive tracers [14]) indicate that Na^+ ions move more readily from near the Si-SiO_2 interface towards the metal-SiO_2 interface (at least for Al or Au gate electrodes) than in the oppositive direction.

Finally in view of the results presented here which imply Na^+ ions are near the interfaces, data interpretation in a previous publication [9] on similar samples which had undergone similar temperature stressing conditions can be further extended. In Figs. 2 and 3 of reference 9, effective electron trap density as a function of effective Na^+ density were shown where the effective density is defined as the first moment (centroid multiplied by the total number of traps or ions per unit area) divided by oxide thickness. For the Na^+ related trapping sites, these figures now are indicative of the actual trap densities as a function of actual Na^+ density.

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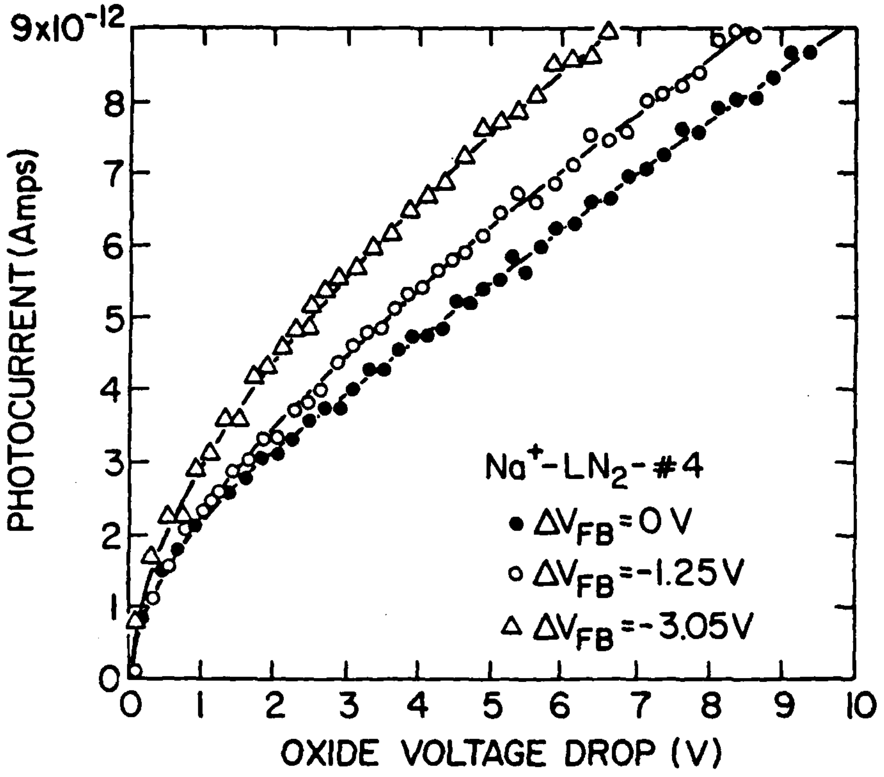

Figure 1: Photocurrent at 77 °K using 5 eV light as a function of the oxide voltage drop for positive gate polarity (Si injecting) and various flat-band shifts (ΔV_{FB}) associated with Na^+ ions.

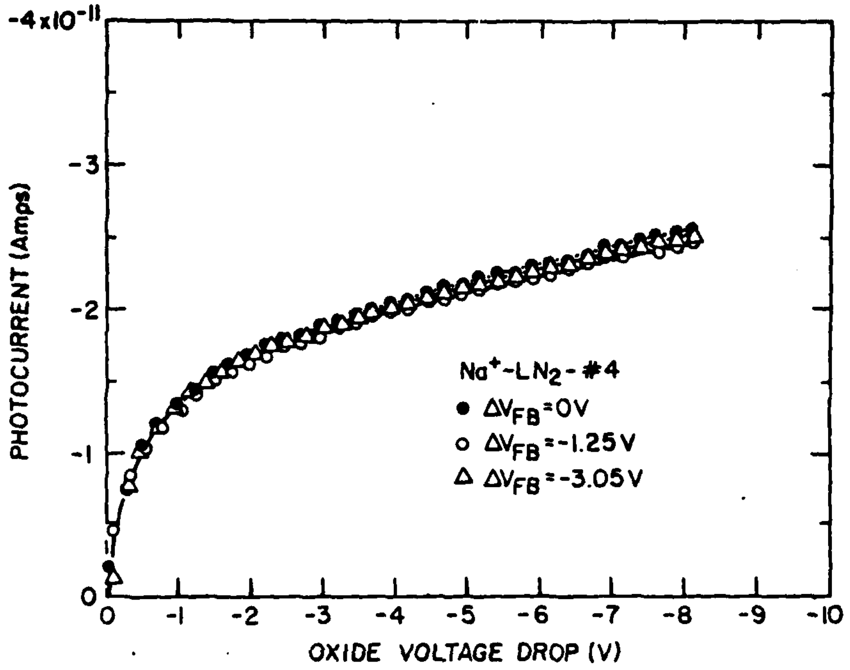

Figure 2: Photocurrent at 77 °K using 5 eV light as a function of the oxide voltage drop for negative gate polarity (Al injecting). The sample and the flat-band shifts are the same as in Fig. 1.

AVALANCHE INJECTION OF HOLES INTO SiO_2

by

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ABSTRACT

Avalanche injection techniques are used to provide hole currents through MOS capacitors and study the trapping of holes in the oxide layer. Although radiation is not in anyway involved in these experiments, the trapped positive charge and surface states resulting from hole injection are similar to those obtained using radiation. The processing and oxide thickness dependence of hole trapping phenomena are also investigated. Prolonged post-oxidation annealing treatments are shown to lead to enhanced hole trapping in "hardened" oxides. Hole trapping cross-sections between 10^{-13} and 10^{-14} cm^2 and trap densities between 10^{12} - 10^{13} cm^{-2} are measured depending on the processing conditions. The effective charge density is studied over the range of oxide thickness between 200 Å and 600 Å as a function of post-oxidation anneal in these "hardened" oxides. While the effective charge density is only weakly dependent on oxide thickness in unannealed oxides, in annealed oxides it exhibits a strong linear *dependence of trapping on oxide thickness. The dependence on post-oxidation anneal time* and ambient are also discussed. These results indicate a strong similarity between hole trapping induced by avalanche injection and by radiation.

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I. INTRODUCTION

The lifetime and reliability of MOS devices operated in radiation environments depends on the rate at which these devices trap holes when exposed to penetrating ionizing radiation. This effect has been studied in detail by numerous authors.[1-3] These traps exist in the oxide prior to irradiation and are filled when holes are created by the radiation in the vicinity of the interfaces or are driven there by internal or external electric fields. These traps have also been populated using non-penetrating radiation[4,5] and high-field stressing under negative bias.[6,7,8] Various processing steps have been determined empirically which minimize the density of these traps producing "radiation-hardened oxides".[9] The picture which emerges from these studies is a process-dependent concentration of neutral hole traps located near to the interfaces.[10] In addition the flat-band voltage shift induced by penetrating radiation has been found by various authors to be proportional to the square[11] or cube of oxide thickness[12] while non-penetrating radiation exhibits as flat-band shift proportional to the first power[11] of oxide thickness.

In all the previous work, the oxide has served as the site where holes are generated by radiation and the site where they are trapped. Complete understanding of these results requires some knowledge of energy loss profiles and of the mechanisms by which electron-hole pairs are created in the oxide. The purpose of this work is to describe a new technique for injecting holes into the oxide which eliminates the need for radiation to produce them. In addition it localizes the hole generation in the silicon and separates it from the trapping in the oxide. Such a study serves to clarify the role played by holes in radiation phenomena by eliminating the complications associated with ionizing radiation. The general features of hole injection and trapping will be discussed. Measurements of hole trapping in oxides of various thickness subjected to different post-oxidation anneals are also presented. Both the general phenomena and the dependencies of trapping on oxide thickness and on post-oxidation anneal are analogous to results reported using radiation to provide hole currents.

II. AVALANCHE INJECTION OF HOLES

As mentioned previously other techniques involving either ionizing radiation[1-5] or high oxide fields[6-8] have been used to generate positive charge in the oxide. Techniques which rely solely on hot-carrier generation in the substrate have also been reported. Optically excited hot holes from the the silicon substrate have been injected into the gate oxide of a poly-silicon gate FET.[13] Holes introduced into the oxide from an avalanche plasma surrounding an oxide-covered p-n junction[14] and from the avalanche plasma in the depletion region of the substrate have already been reported by other authors.[15, 16] The last technique, which is used in this paper, is particularly attractive from a practical point of view since the carrier injection rate can be controlled by the voltage and frequency of the exciting gate pulse and the carrier injection is uniform across the sample.

The general principles of avalance injection are illustrated schematically in figure 1 which depicts the non-equilibrium energy-band diagram of an MOS capacitor driven into deep depletion. Such a situation can occur if the period of the exciting gate voltage is shorter than the semiconductor minority carrier generation time, usually greater than 100ms.[16] If a sufficiently large negative gate voltage V_G is applied to an n-type substrate, the surface potential will be pinned at the value V_A at which avalanche multiplication of carriers begins to occur in the substrate. Electron-hole pairs created by avalanche multiplication in the depletion layer under the gate will be separated and move in opposite directions. Holes approaching the $Si\text{-}SiO_2$ interface under the influence of the field in the silicon are not in thermal equilibrium with the lattice. A small portion,[15] approximately one out of every million, of these "hot" carriers are energetic enough to overcome the barrier at the interface and pass into the oxide, where a fraction of them are trapped at defects.

Whether charge injection occurs principally by tunnelling of hot carriers through the top of the barrier or by passage of these hot carriers over this barrier is not known. Empirically, however, the field in the oxide near the silicon interface controls the average d.c. current passing across the interface. This situation is analogous to that reported for electron injection via avalanche techniques[18]; presumably the additional oxide field reduces the width of the tunnelling barrier or the height of the image force barrier at the interface. A feedback circuit exploits this field dependence to maintain a constant average hole current through the oxide by automatically adjusting the gate voltage until a set current level is reached.

Prior to any charge build-up in the oxide, the magnitude of the current depends only on the oxide field and is independent of oxide thickness. As positive charge density builds up in the oxide, the decrease in field near the injecting interface is compensated for by a corresponding increase in gate voltage, maintaining the set current level. The measured change in gate voltage tracks the change in flat-band voltage closely. When deviations do occur the flat-band voltage change exceeds that of the gate voltage but by less than 20%. Such behavior is consistent with the build-up of interface states. Charge located on the interface is exactly compensated by its image in the silicon so that while it is reflected in the flat-band shift it does not alter the field in the oxide or the voltage necessary to maintain the current.

Positive charge generated by high field (~ 10 MV/cm) emission has been postulated to arise from tunnelling of electrons from neutral centers into the oxide conduction bands[6] or from the impact ionization of neutral centers in the oxide bulk.[6,7] In contrast, avalanche injection charges the oxide with fields in the range 3 MV/cm; this field is not sufficiently high to allow electron tunnelling from neutral bulk traps[6] and is below the observed threshold for impact ionization of traps in the oxide.[7]

It should be noted that hole trapping exhibits dependence on both the peak oxide field and excitation frequency used in the avalanche pulse train. The field dependence is as yet unexplained, the frequency dependence is believed to have its origins in back-tunnelling of holes into the silicon. These aspects of the injection will be treated in another publication. Comparisons between various oxides were always done at a fixed frequency and current level to keep both factors constant.

III. EXPERIMENTAL DETAILS

Two types of samples were measured. In the portion of this work which deals with the general features of avalanche injection, samples were given a 10 minute in situ post-oxidation anneal in nitrogen after growth. In those sections which deal with processing dependence of hole trapping, the wafers were pulled from the hot zone of the furnace and allowed to cool at the end of the furnace tube after oxide growth. This latter annealing procedure follows the recommendations of Aubuchon[9] for producing radiation-hardened oxides. Some of the unannealed wafers were *given a subsequent post-oxidation* anneal in a separate step to determine its effects on hole trap concentrations. Post-oxidation anneal[19] and oxide thickness[11, 12] were chosen as process variables for study because of their importance in determining the radiation hardness of oxides.

All the oxides were grown on .1 Ω-cm n type phosphorous doped silicon in a dry oxygen ambient at 1000 C. This highly doped substrate ($9 \times 10^{16} cm^{-3}$) is required to avoid edge injection effects, lower the substrate breakdown voltage and the field across the oxide during the injection process.[15] The samples were given the post-oxidation annealing procedures just described. Afterwards, circular aluminum gates 32 mils in diameter were deposited from an r-f heated crucible. The majority of the wafers were then sintered in forming gas at 400 C for 20 minutes. Some wafers were intentionally not sintered after aluminum deposition but this anneal did not strongly influence the trapping. The flat-band voltages of the capacitors were within .100 mV of their theoretical value and the wafers showed no evidence of mobile sodium.

A summary of the processing variations examined on the wafers to date is given in Table I. A batch of wafers consists of a series of oxides of different thicknesses grown at approximately the same time (on the same day) *in the same furnace*; four separate batches were grown. Each run in the batch had a specified nominal oxide thickness and consisted of approximately six to twelve wafers. Nominal thicknesses are given in the table and ranged between 200 Å and 600 Å. After all the wafers in a batch were grown, some from each run were given the specified post-oxidation anneal. Time, temperature and ambient were varied in the post-oxidation anneal matrix. The variables in a given run are indicated by the crosses in the appropriate columns of Table I. Argon or nitrogen was used as the ambient, and anneal times were varied between 6 minutes and 180 minutes. Wafers from batch 1 were used in early characterization runs of hole trapping phenomena while batches 2 through 4 were used in the process-related studies. Results from wafers within a batch and run were quite reproducible.

The experiment is accomplished using an apparatus which automatically switches the sample at specified intervals between two circuits which alternately inject holes at a constant current and measure the flat-band voltage of the capacitor. A feedback circuit automatically adjusts the peak gate voltage to maintain a constant average hole current through the oxide. These circuits are the same ones used for electron injection[20]; converting the apparatus to the hole injection mode requires only reversing the substrate and gate connections.

Unlike operation in the electron injection mode, however, the shape of the voltage applied at the gate is critical to hole injection. Following the experiments of Nagai et al.,[16] we observed hole trapping in the oxide when sawtooth waveforms were used. No hole trapping was evident when a square wave pulse was used. The competing processes of hole injection from the substrate and electron injection from the gate make hole trapping particularly sensitive to the details of pulse shape. Because the barriers for electron injection from the gate (3.2 eV) are lower than those for hole injection from the substrate (4.7 eV) care must be taken to minimize electron injection during the avalanche injection pulse. Since only a small fraction[15] ($\sim 10^{-6}$) of the holes from the substrate are energetic enough to enter the oxide, the avalanche current in the substrate is very nearly equal to the displacement current in the oxide from current continuity requirements. The hole current through the oxide is proportional to the product of the avalanche current and a factor which is an increasing function of the field at the silicon interface. Hole injection occurs then only when there is a displacement current through the oxide and a high field at the injecting interface. However, if such a field is present across the oxide when no displacement current exists, electrons from the gate will be injected instead. The sawtooth waveform presents a high field at the silicon interface when the displacement current exists and removes it abruptly when this current has ceased, reducing the electron injection into the oxide. On the other hand, the square wave pulse subjects the oxide to high fields when no such current is present, resulting in electron injection and annihilation of any holes which may have been trapped in the oxide.[10]

Data are recorded directly into an IBM VM-168 computer via an IBM Research Device Coupler. This allows several hundred readings of flat-band voltage to be taken during a typical experiment. This large number of points facilitates determination of trap cross-sections and densities with fitting routines to be described later.

IV. RESULTS

A) GENERAL FEATURES

Typical behavior of an MOS capacitor stressed by passage of an avalanche-generated hole current through the interface is illustrated in Fig. 2. The 1 MHz and quasi-static[21] C-V curves are displayed before and after injection. Note the build-up of both positive charge and surface states similar to that observed when capacitors are exposed to penetrating and non-penetrating radiation.[5] Many of the surface states are too slow to respond to the 1 MHz measurements and give rise to the hysteresis in the post-injection C-V curves. Tunnelling of electrons out of slow states accounts for the sense of the hysteresis. In the avalanche injection experiments the voltage shift ΔV_{FB} between the 1 MHz C-V curves is measured as indicated in the figure. This quantity includes the contribution to the silicon surface potential of fixed positive charge in the oxide and surface states fast enough to respond to the 1 MHz signal. Although the densities of positive charge and surface states vary with processing these features are common in all the capacitors measured. This particular capacitor was from batch 1 and was avalanched for 2500 seconds at a current density of 1.7 x 10^{-8} A-cm^2. Quasi-static C-V measurements were done with a linear voltage ramp changing at a rate of .1 V-sec^{-1}.

The observed increase in positive charge and surface states is clearly a result of hole transport through the interface and not due to any incident radiation. Other researchers have reached this same conclusion.[4,5,10,11] The results differ from those usually presented in discussions on radiation induced charge since this trapping occurs under a negative bias as holes are drifted toward the gate from the silicon interface. Mobile sodium can be eliminated as the source of the observed shift since it is pinned under the gate by the field during the avalanching pulses. The shapes of these quasi-static and high frequency C-V curves are consistent with a density of surface states near the upper half of the band gap removed somewhat from the interface itself or a density of surface states close to mid-gap in the silicon.

After injection the trapped charge and surface state densities are quite stable. Except for a small relaxation in the beginning (~ 10%), the flat-band voltage did not change for months when the capacitor was left, gate floating at room temperature. Application of a positive field of 5 MV/cm did result in rapid relaxation. This is probably due to recombination of the trapped holes with electrons which can tunnel through the barrier at the Si-SiO_2 interface because of the high density of positive charge and the high fields which exist there.

Figure 3 shows how the flat-band voltage changes with time as holes are injected into the oxide. These particular capacitors were from the same wafer in batch 1 and were injected at an average current of 4 x 10^{-9} A-cm^{-2} with a 45 KHz injection waveform at liquid nitrogen and at room temperatures. The shape of these curves is typical of all the data taken; the slope of the curve gradually decreases as injection proceeds, approaching some saturation value of flat-band shift. These curves are approximately exponential in shape as would be expected from a process where the probability of capture at any time is proportional to the number of unfilled traps in the oxide.[22] Such models are oversimplified since they ignore detrapping and back-tunnelling in the oxide but provide a convenient framework for characterizing the traps.

They have been discussed previously[22] and result in expressions for the flat-band shift with the effective saturated charge density N_{eff} and the trapping cross-section σ as parameters. On the basis of this model the shift in flat-band voltage is given by the expression

$$\Delta V_{FB} = \frac{eN_{eff}}{C_{ox}} (1-\exp(-\sigma jt/e) \tag{2a}$$

where e is an elementary electronic charge, C_{ox} is the oxide capacitance per unit area and j is the current density. The effective trap density is defined by

$$N_{eff} = \frac{\bar{x}}{t_{ox}} N \tag{2b}$$

where N is the total number of traps in the oxide per unit area, $\bar{x}$ is the centroid of their distribution measured from the Al-SiO_2 interface, and t_{ox} is oxide thickness. As is apparent from figure 3, more positive charge is trapped in the oxide at any given time at 77 K than at 295 K. Similar results have been reported for positive charge induced by low temperature irradiations.

The cross-sections and saturated trap densities which best characterize the data presented in figure 3, were determined by a computer program which fits the actual experimental data to an expression with the form of equation (2a) involving the sum of two such exponentials. The program iteratively chooses values for σ_1, σ_2 and N_1, N_2 until the root-mean squared deviation between the measured and calculated curves is minimized. Deviations of less than 50 mV are typical of the data presented here. The values for these parameters for the data in figure 4 are presented in Table II. Capacitors on the same wafer from batch I were used to obtain this data. Average avalanche current was 4 x 10^{-9} A-cm^2 at a frequency of 45 KHz. Trap densities and capture cross-sections are composed of a temperature dependent and a temperature independent portion. The additional traps filled at 77 K have a coulombic capture cross-section of 1 x 10^{-13} cm^{-2} but are associated with shallow traps in the oxide since they detrap on warming to room temperatures. The initial trapping probability η at t=0, given by

$$\eta(0) = \sigma_1 N_1 + \sigma_2 N_2$$

is displayed in the last column of the table. The hole trapping probability is around 5% at room temperature and 11% at 77 K, in these samples. Trapping efficiency is however a strong function of processing; different batches of wafers exhibit different trapping probabilities depending on their post-oxide growth thermal history. Hole trapping probabilities were usually less than 20% at room temperature in all the samples measured.

Curtis et al.[23] using electron-beam injection and Nagai[16] et al using avalanche injection have also reported a 10% capture probability for holes in SiO_2 at room temperature. These results are in conflict with those of Ning[13] reporting a 100% capture probability for holes optically injected into the SiO_2 insulator of silicon gate FET's. Differences in processing may be responsible for such discrepancies. The capture probability is influenced by the oxide field present during avalanche injection, decreasing with increasing oxide field but even at the lowest peak fields used for injection (1.5 MV/cm) it never exceeded 20% at room temperature. This aspect of the problem is being studied further.

Field-dependent hole capture cross-sections of 10^{-13} cm^2 to 10^{-14} cm^2 are indicative of a coulombic center yet this center appears neutral or compensated. Whether or not the shallow traps which are populated at 77 K are in the oxide bulk is as yet unknown. Photo I-V experiments are planned to directly address this question.

B) PROCESSING DEPENDENCE

Processing variations and their effect on hole trapping will be discussed in the remainder of this section. Wafers from batches 2-4 were used for these measurements as discussed in section III. The observations reported here were checked for consistency in at least two of these three batches.

Capacitor to capacitor variations on a given wafer, and wafer to wafer variations in a given run were minor. The major discrepancy arose between wafers of similar oxide thickness and processing history from different batches and involved the density of hole traps present in the oxides after pulling from the furnace in oxygen. The variation between batches is shown in Fig. 4 where the flat-band shift is plotted against injection time at a current of 9.6 x 10^{-9} A-cm^{-2}. These oxides were 350 Å thick and given a 400 C, 20 minute forming gas anneal prior to the measurement to reduce surface state densities. Experiments showed that this sintering step reduces the trap concentration in the oxide by 10%. Contamination of the furnace or oxygen gases or variations in the cooling rate after growth may be responsible for the batch to batch variation.

Despite this, the effects of extended post-oxidation anneals were consistent between batches. In three separate batches of wafers, 90 minute post-oxidation anneals at 1000 C resulted in enhanced hole trapping in the oxides. This point is illustrated in figure 5, where the flat-band shift due to hole trapping on oxides processed in batch 4 is plotted as a function of injection time at a current density of 9.6 x 10^{-9} A-cm^{2} for two different ambients.

The influence of the ambient used in the 90 minute post-oxidation anneal is also illustrated in this figure. Note the increase in the sample annealed with a nitrogen ambient. This ambient dependence was observed in two batches of wafers despite large differences in the hole trap density existing in the oxides prior to any post-oxidation annealing treatment. Possible explanations for such behavior might be water contamination of gas sources or incorporation of nitrogen in the form of silicon nitride at the interface.[24] Better control of gas purity is needed to determine the reason.

In Fig. 6 the flat-band voltage shift is plotted as a function of post-oxidation anneal time for samples from batch 3 having oxide thicknesses of 200 Å and 350 Å. The anneal was at 1000 C in an argon ambient and the shift after injection for 4000 seconds at a current of 9.6 x 10^{-9} A-cm^{-2} was used. Figure 6 indicates that for this batch, the pre-anneal hole trap density is decreased by short anneal times but eventually increases with prolonged annealing. This is similar to the behavior reported by Schlesier et al. on wet oxides.[19] Note that the degree to which the flat-band shift is affected by the anneal depends on the sample thickness. Prior to annealing, the shifts scale with the ratio of the oxide thicknesses; after a 90 minute annneal it scales with the square of this ratio. Other batches of wafers showed a monotonic increase of trap concentration with anneal time. The hole trap concentration present in the wafers prior to post-oxidation anneal is probably related to this behavior. But again despite inconsistencies in the short-term annealing, long term anneals reproducibly caused an increase in the hole trap concentrations measured by this technique.

A more complete study of the inter-relation between the long term anneals and the oxide thickness was planned in batch 4. Wafers with various oxide thicknesses, subjected to 3 different post-oxide anneals were fabricated in batch 4. Growth and pulling conditions were as previously described. One third of the wafers were annealed for 90 minutes in argon, one third for 90 minutes in nitrogen and one-third were left unnanealed. Because flat-band shifts became too large to measure in the thickest samples after 500 seconds of injection at a current of 9.6×10^{-9} A-cm^{-2}, the unsaturated flat-band voltage shift at this particular time was chosen for comparison among the various thicknesses. The effective trap density associated with the flat-band voltage change is a convenient physical quantity to compare since it automatically adjusts for the increase in flat-band voltage associated with increased oxide thickness. It is defined by the relation

$$N_{eff} = \frac{\varepsilon}{e\, t_{ox}} \Delta V_{FB}$$

where t_{ox} is the oxide thickness, ε is the dielectric constant of SiO_2 and e is an elementary charge, and is porportional to the product of the centroid and density of this charge distribution as in Eq. (2b).

Figure 7 summarizes the behavior of the effective density of trapped charge as a function of oxide thickness for the three annealing conditions. The effective charge density in the unannealed oxides is small and weakly dependent on oxide thickness. In fact the saturated effective trap density (after injection for 4000 seconds) for the three thinnest oxides is thickness independent but exhibits a large increase for the thickest (590 Å) sample. On the other hand after the ninety-minute anneal, the effective charge density shown in figure 7 is increased in magnitude and exhibits a strong linear dependence on oxide thickness. In the annealed samples, the rate of change of charge density with thickness does not depend on the ambient but only on the anneal time and temperature. There is, however, an ambient dependent contribution to the effective charge density which is thickness independent. This component is much larger for the nitrogen annealed samples than for those annealed in argon.

If the same amount of charge is trapped in these oxides and localized at the interface, equation (2b) predicts a thickness independent effective charge density. This apparently is not the case for these oxides. Hole traps distributed uniformly through the bulk of the oxide can explain the observed linear dependence of effective charge density on oxide thickness. However, this picture is in contradiction with experimental observations of a centroid close to the silicon interface.[6,10] The effect of the high temperature treatments involved with growing thicker oxides or annealing an oxide after it is grown must be to increase the number of active trapping sites in the vicinity of this interface. How this is accomplished is not known but such behavior is consistent with the two models postulated to explain the thickness dependence of the trap densities, the viscious flow model[25] and diffusion model.[26] In both these situations extended exposure to high temperatures can lead to an increased trap density near the interfaces which increases with oxide thickness. In the first case, extended annealing times allow additional bonds to be broken as viscous flow occurs near the interface to relieve the thickness dependent shear stresses. In the second model, thicker oxides have already seen longer times at high temperature in their growth process so that additional diffusion of excess silicon may have already occured from the substrate.

Neither model, however, accomodates the observed dependence of trap density on ambient in its framework. These results indicate that some species in the annealing gases per se lead to traps close to the interface. The identity of these species is as yet unknown.

Effective trap densities which are independent of thickness[11] or which depends linearly on thickness[12] have been reported in studies on thicker oxides where radiation was used to provide the carriers. It should be emphasized that in this study the effective charge density is directly measured without adjusting for the thickness dependence of radiation-generated holes in the oxide. The hole trapping processes are entirely independent of the generation processes, giving a clearer interpretation of the hole trapping properties of the oxide. Direct comparison with these earlier studies is difficult because of the difference in the oxide thicknesses used in the experiments.

V. DISCUSSION

Avalanche injection of holes provides an alternative to the use of ionizing radiation to study hole trapping in SiO_2. The positive charge and surface states created by passing avalanche generated currents are identical to the phenomena observed in experiments using radiation. In addition, the same trends in trapping behavior are produced when process variables important to radiation hardening of oxides are examined using this technique. As mentioned previously these studies separate the aspects of hole generation from those of hole trapping leading to a better understanding of both. Since highly doped n-type substrates are required for the technique, it cannot be used conveniently as a hardness test for off-the-shelf MOS products. It is used to best advantage in surveys of processing effects and in studies of the physical properties of hole trapping phenomena.

Holes transported to the silicon interface and not the radiation itself are responsible for the creation of positive charge and surface states. This reaffirms the conclusion that radiation does not create these traps but only provides the carriers to fill them.[5]

Despite variations in processing batches, the effects of oxide thickness and post-oxidation annealing are clear. The protracted post-oxidation anneals can introduce additional interface traps and enhance the thickness dependence of the effective charge density. Better control of annealing ambient, oxygen gases, and cooling rates after pull are required to further clarify these results. Conflicting reports on the oxide thickness dependence of the effective trap density may have their origins in the type of post-oxidation anneals received after growth. Apparently the details of time, temperature and ambient are important in determining how strong this dependence is.

Polysilicon gate capacitors were reported previously[20] to be more sensitive to ionizing radiation than aluminum gate capacitors. As shown here, the extended thermal anneals necessary to dope the gate material probably increase the hole trapping near the Si-SiO_2 interface. Drive-in anneals should be optimized to reduce this component of trapping.

VI. SUMMARY

Avalanche injection of holes has been shown as a new and valuable tool for the study of hole trapping in oxides. Characteristics of the trapped charge injected by this method are almost identical with those of charge induced by radiation. Process control of the trap density has been linked to the conditions of post-oxidation anneal in terms of ambient, time and temperature. The trends in these variables follow those necessary for hardening oxides to ionizing radiation. This annealing step has also been shown to control the extent to which the effective charge density depends on the oxide thickness.

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TABLE I

			POST-OXIDATION ANNEAL CONDITIONS			
BATCH	RUN	t_{ox}(Å)	O_2PULL	AMB.	TEMP.	TIME
1	H	500	NO	N_2	1000 C	10 min
2	1-2	500	YES	Ar	"	15-180 min
3	3-4	200,350	YES	Ar-N_2	"	6-90 min
4	6-9	200,350 500,600	YES	Ar-N_2	"	90 min

TABLE II

Hole Trapping Parameters

T(K)	$\sigma_1(\mathrm{cm}^2)$	$N_1(\mathrm{cm}^{-2})$	$\sigma_2(\mathrm{cm}^2)$	$N_2(\mathrm{cm}^{-2})$	$\eta(0)$
295	——	——	$2.7\mathrm{x}10^{-14}$	$1.7\mathrm{x}10^{12}$	5%
77	$1.0\mathrm{x}10^{-13}$	$7\mathrm{x}10^{11}$	$1.9\mathrm{x}10^{-14}$	$2.0\mathrm{x}10^{12}$	11%

FIGURE CAPTIONS

Figure 1 Schematic band diagram of MOS capacitor driven into avalanche conditions in deep depletion. The Fermi levels are indicated by the dashed lines in the equilibrium regions of the device.

Figure 2 Typical MOS quasi-static (dotted lines) and high-frequency (solid line) C-V characteristics before and after avalanching at a current of 1.7×10^{-8} A-cm^{-2} for 2500 sec. Note the build-up of slow interface states and positive charge with injection.

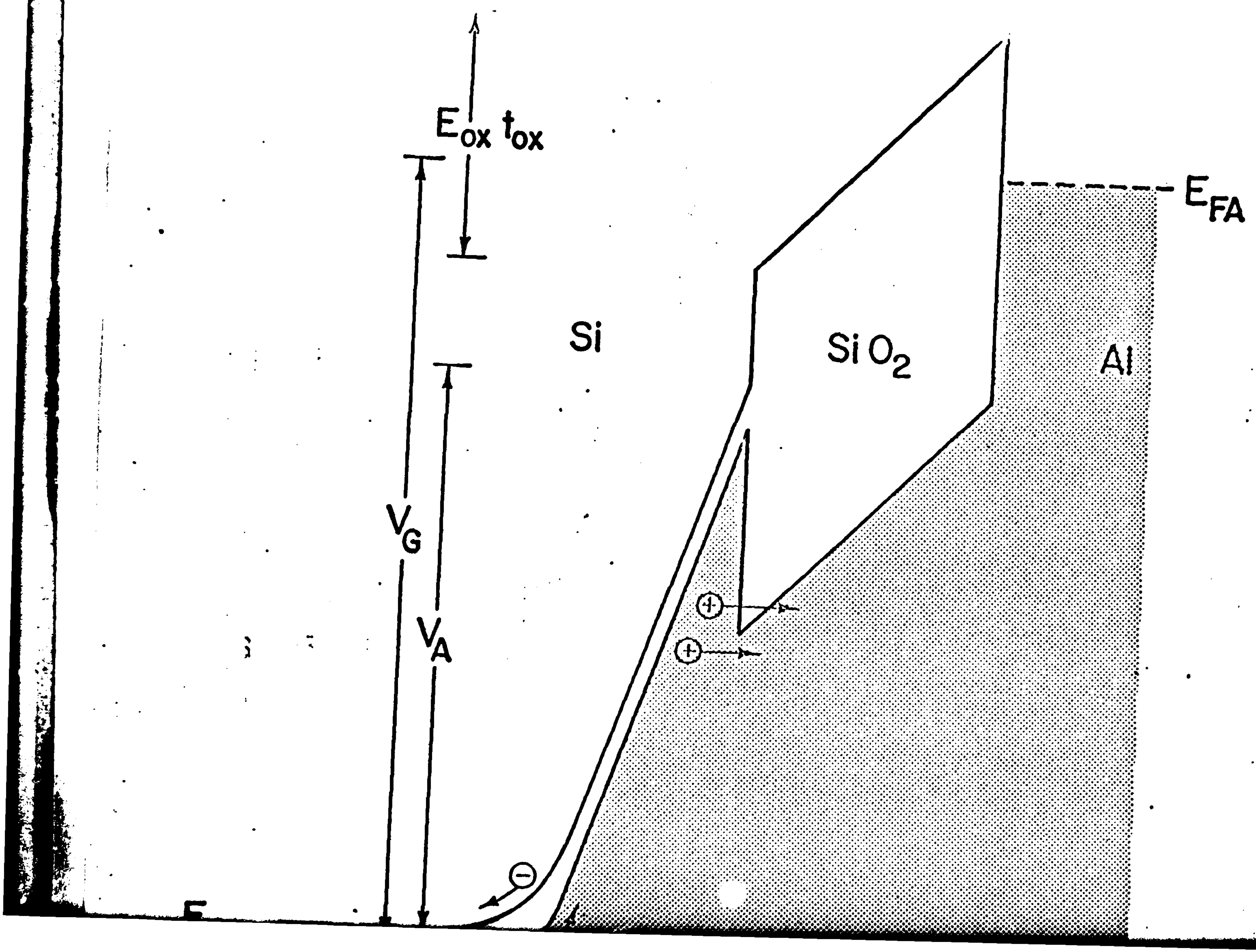
Figure 3 Flat-band voltage shift as a function of injection time at a current of 4×10^{-9} A-cm^{-2} for capacitors on the same wafer. Injection was carried out at two different temperatures, 77 K and 295 K. Additional trapping at shallow centers accounts for the increase at 77 K.

Figure 4 Comparison of the flat-band shift with injection time for wafers of the same thickness from two different processing batches. Both wafers were pulled in oxygen after growth at 1000 C and injected at a current of 9.6×10^{-9} A-cm^{-2}

Figure 5 Comparison of the flat-band shift with injection time for wafers from batch 4 injected at a current of 9.6×10^{-9} A-cm^{-2}. The bottom curve is from a wafer which had no subsequent post-oxidation anneal. The middle and upper curves are results from wafers with 90 minute post-oxidation anneals in argon and nitrogen respectively.

Figure 6 The flat-band voltage shift after 4000 seconds of injection at a current of 9.6×10^{-9} A-cm^{-2} is plotted as a function of post-oxidation anneal time in argon for wafers from batch 3.

Figure 7 The effective density of charge trapped after 500 seconds of injection at a current of 9.6×10^{-9} A-cm^{-2} is plotted as a function of oxide thickness for three different post-oxidation annealing conditions seen by wafers in batch 4, i.e., no post-oxidation anneal, or a 90 minute post oxidation anneal in either nitrogen or argon.


$E_{ox}\,t_{ox}$
E_{FA}
Si
SiO_2
Al
V_G
V_A
⊕
⊕
⊖

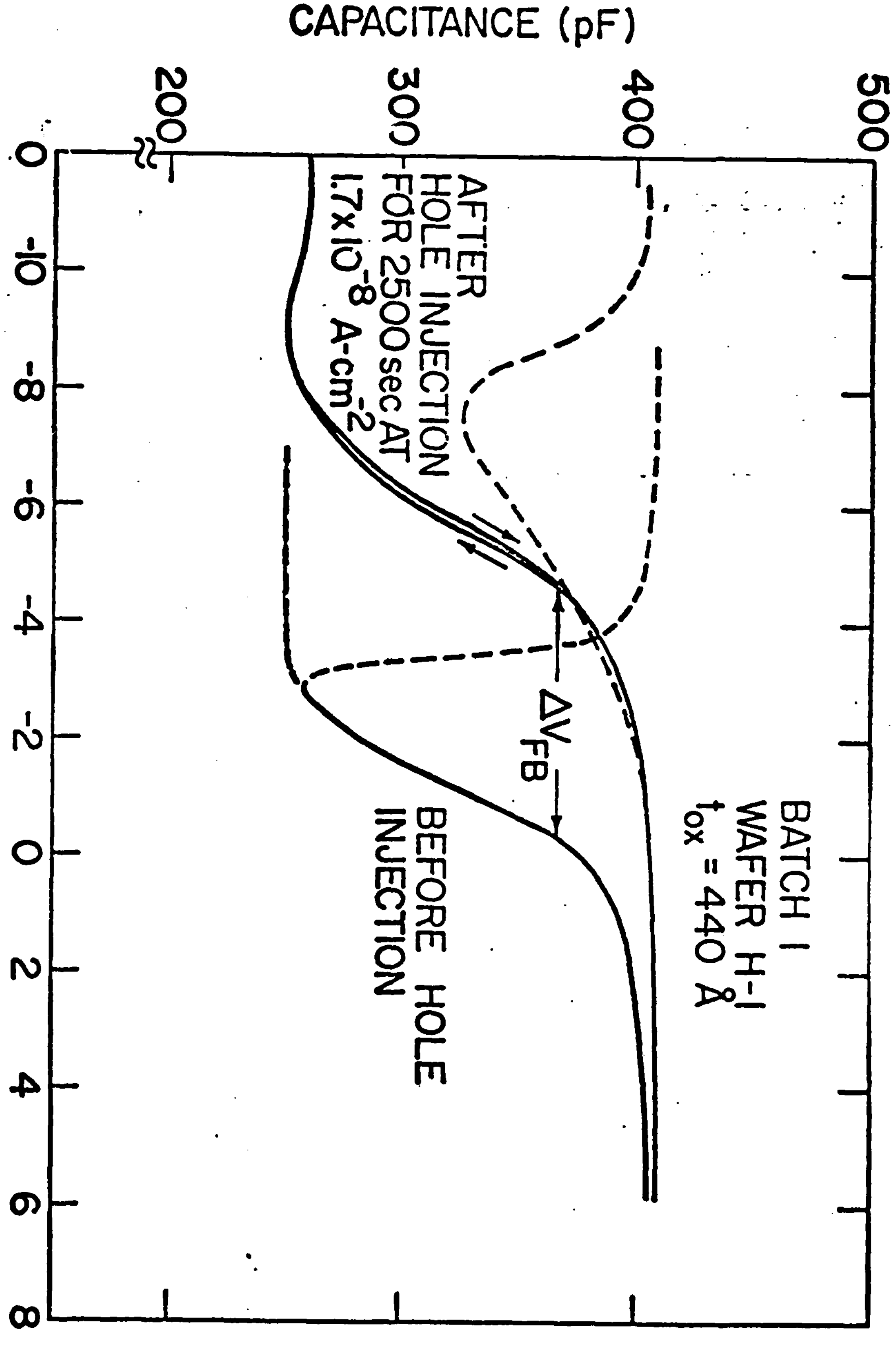

CAPACITANCE (pF)
200
300
400
500
0
-10
-8
-6
-4
-2
0
2
4
6
8
GATE VOLTAGE (V)
AFTER
HOLE INJECTION
FOR 2500 sec AT
1.7x10^{-8} A-cm^{-2}
BEFORE HOLE
INJECTION
ΔV_{FB}
BATCH I
WAFER H-I
t_{ox} = 440 Å

fig 2

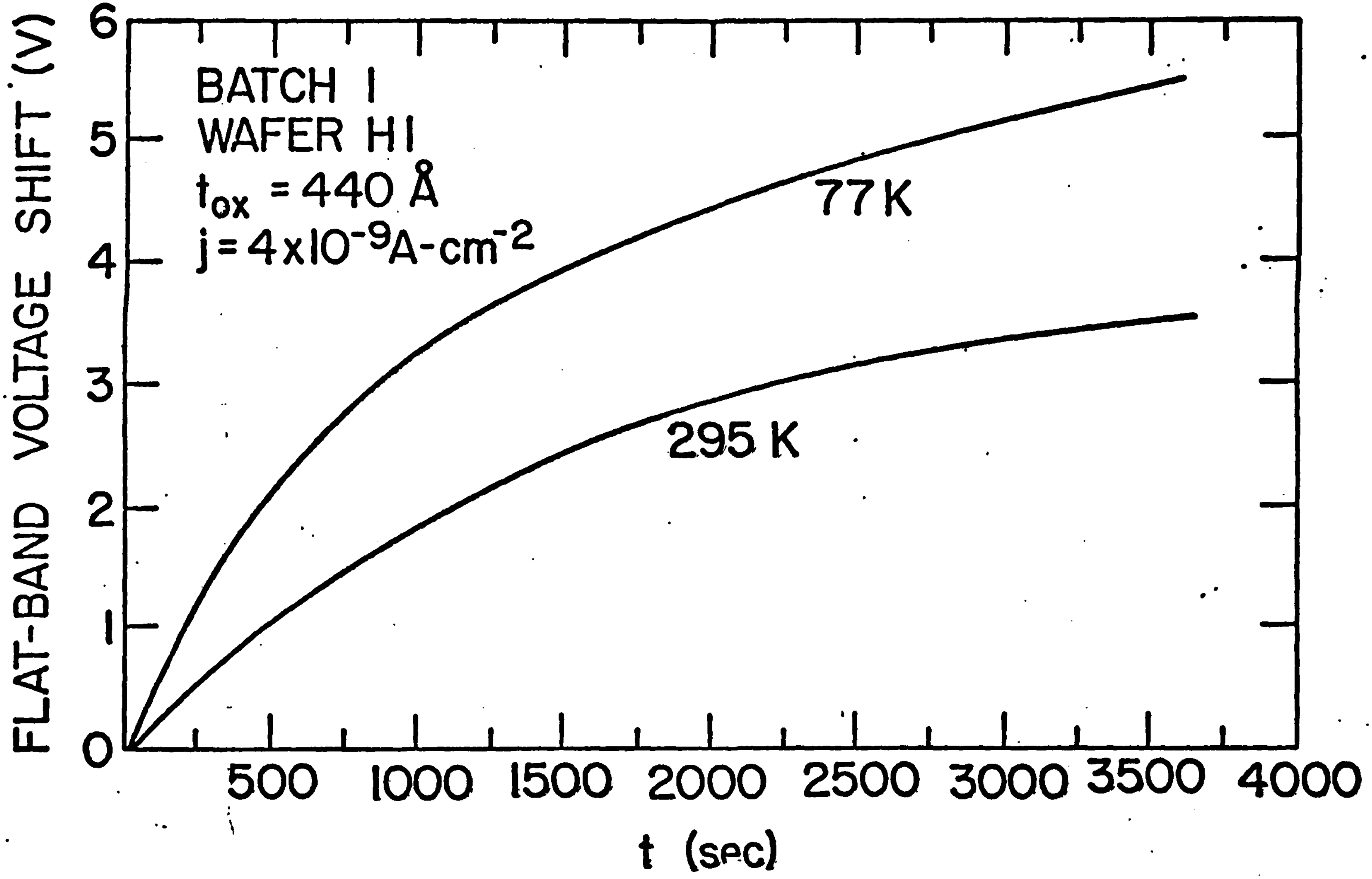
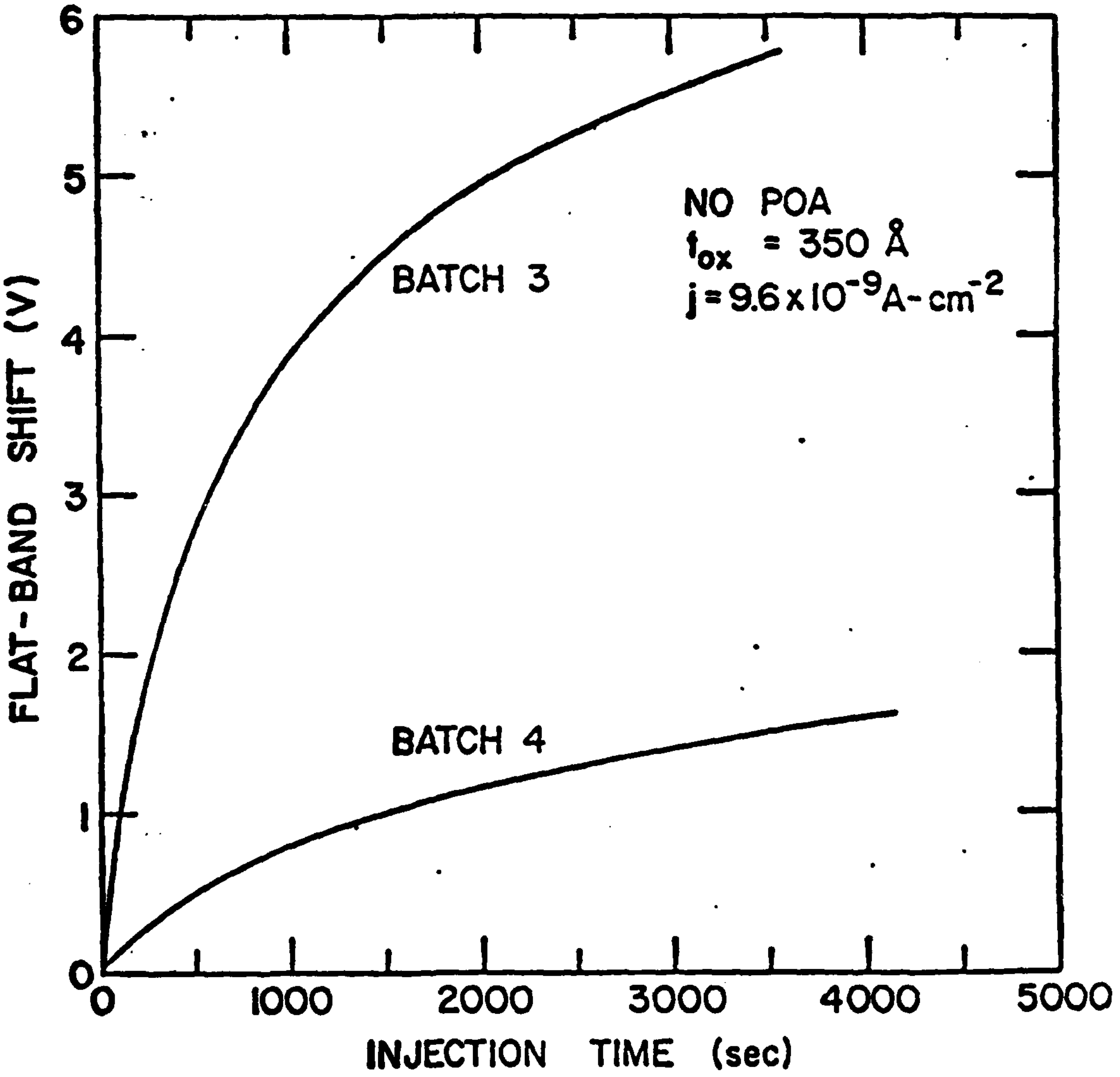

FLAT-BAND VOLTAGE SHIFT (V)
0
1
2
3
4
5
6
BATCH I
WAFER H1
$t_{ox} = 440$ Å
$j = 4 \times 10^{-9}$ A-cm^{-2}
77 K
295 K
500
1000
1500
2000
2500
3000
3500
4000
t (sec)

Fig 8



FLAT-BAND SHIFT (V)
0
1
2
3
4
5
6
INJECTION TIME (sec)
0
1000
2000
3000
4000
5000
BATCH 3
BATCH 4
NO POA
t_{ox} = 350 Å
$j = 9.6 \times 10^{-9}$ A-cm^{-2}

Fig 4

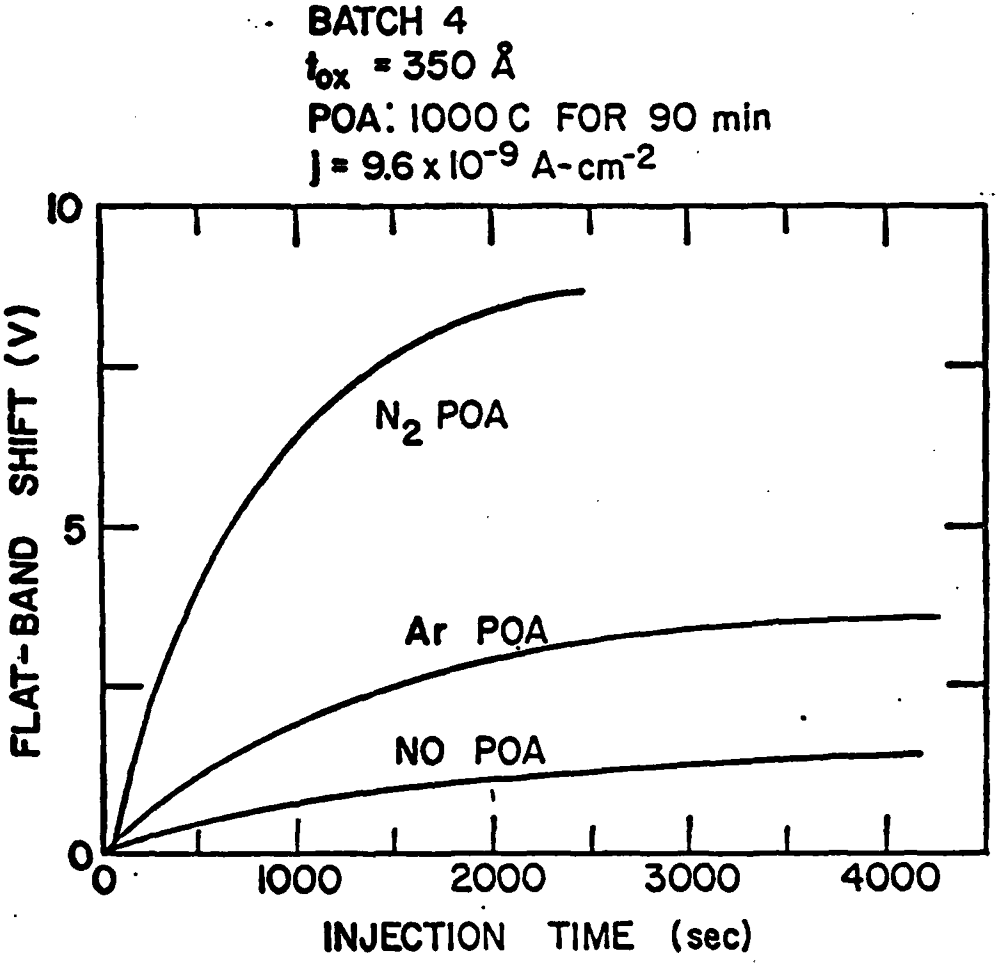
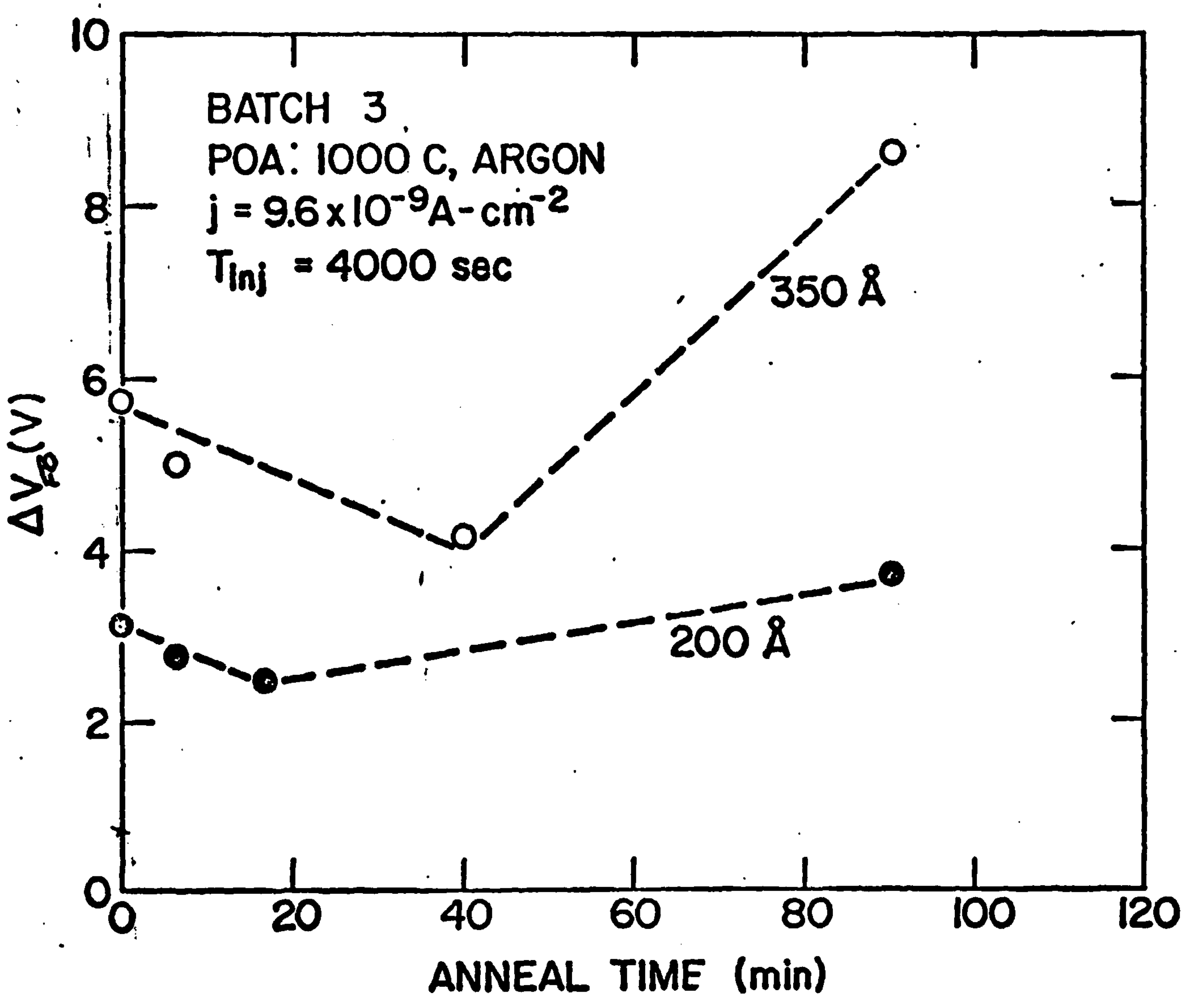

BATCH 4
t_{ox} = 350 Å
POA: 1000 C FOR 90 min
J = 9.6×10^{-9} A-cm^{-2}
FLAT-BAND SHIFT (V)
10
5
0
N$_2$ POA
Ar POA
NO POA
0
1000
2000
3000
4000
INJECTION TIME (sec)

Fig 5


BATCH 3
POA: 1000 C, ARGON
$j = 9.6 \times 10^{-9} A\text{-}cm^{-2}$
T_{inj} = 4000 sec
350 Å
200 Å
ΔV_{FB}(V)
0
2
4
6
8
10
0
20
40
60
80
100
120
ANNEAL TIME (min)

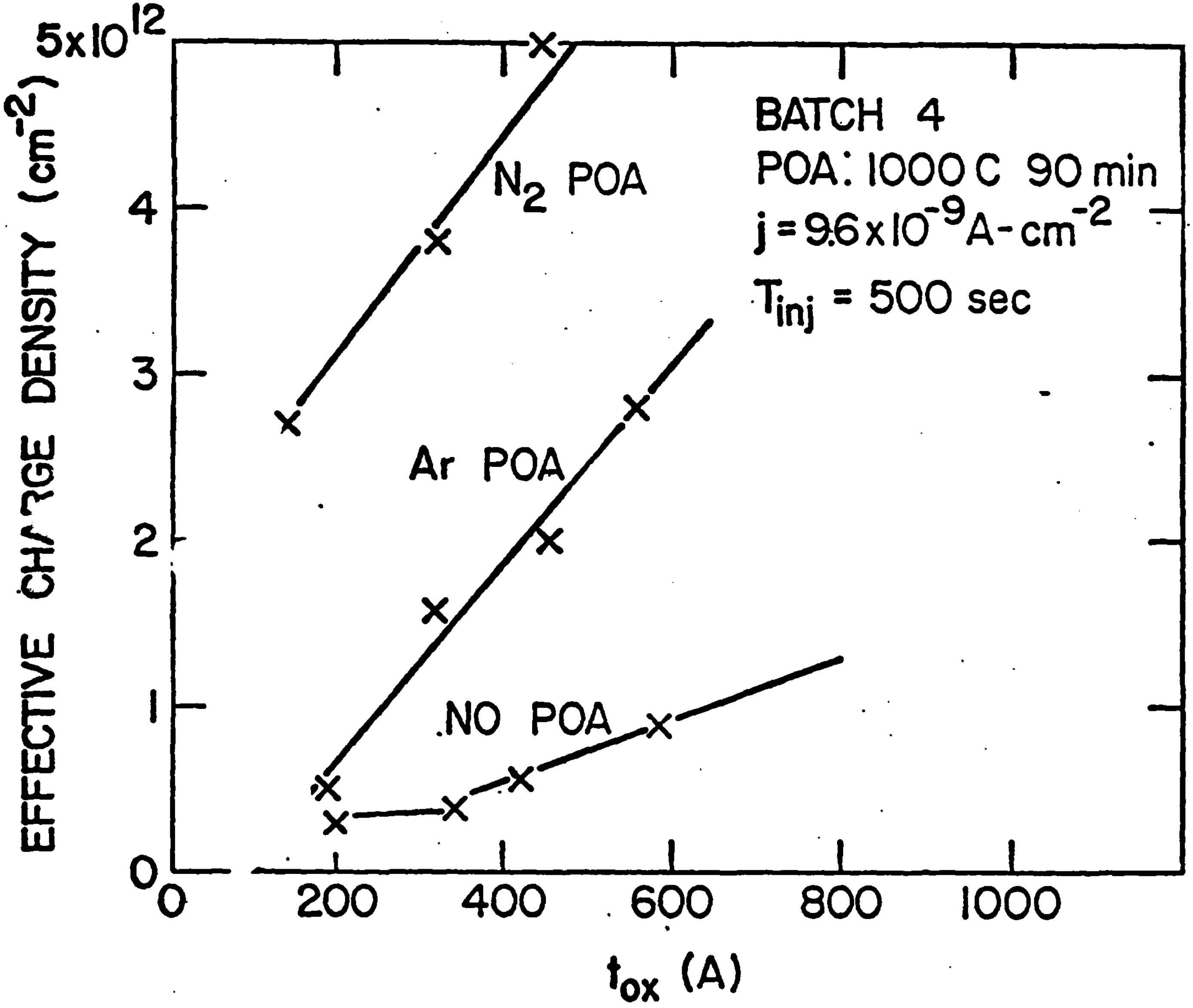

5x10^{12}
4
3
2
1
0
0
200
400
600
800
1000
EFFECTIVE CHARGE DENSITY (cm^{-2})
t_{ox} (A)
N$_2$ POA
Ar POA
NO POA
BATCH 4
POA: 1000 C 90 min
$j = 9.6 \times 10^{-9}$ A-cm^{-2}
T_{inj} = 500 sec

Fig 7

DIELECTRIC BREAKDOWN PHENOMENA IN SiO_2*

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Dielectric instability and breakdown in thin SiO_2 films are explained by a mathematical model involving impact ionization and a resulting negative resistance type of runaway. Electrons injected from the cathode are accelerated by an electric field to a point where some small fraction of them produce hole-electron pairs by impact ionization. Holes left in the SiO_2 produce a field distortion which leads to a further enhancement of the impact ionization, and so on to an electronic runaway. The model is sensitive to two key parameters, the ionization band-gap and the electron-phonon scattering length. Quantitative explanations are given for thickness dependence, contact barrier dependence, and time dependence of breakdown.

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+ On leave to Technion, Haifa, Israel

I. Introduction

In the development of semiconductor technology, dielectric instability and breakdown in insulators such as SiO_2 have become increasingly significant in limiting both performance and reliability. Because of the importance of insulating thin films of SiO_2 in the integrated circuit industry, and because of the new information available on the properties of this material, it is fruitful to reexamine the physical processes which occur at high electric fields in order to gain insight into the possible intrinsic breakdown mechanisms. Reliable data is available on the dependence of breakdown upon insulator thickness[1,2], electrode work function[3], and ionizing radiation[4] as well as on several material parameters of SiO_2 including ionization rate[5], effective hole mobility[6,7], and recombination cross section[8]. The problem of sorting out the details of the breakdown process in SiO_2 is considerably facilitated by the development of materials technology as well as the wealth of data on electronic properties which has become available. The fundamental phenomena which occur during intrinsic dielectric breakdown in thin films of SiO_2 can be explained and understood in a way that is consistent with available data.

Historically, dielectric breakdown in insulators was described as an electronic avalanche process[9-12], in which the field is high enough that one initial electron is capable of producing a destructively large cascade of ionizing events. A serious deficiency of avalanche models, the neglect of the field distortion produced during the avalanche, was recognized by O'Dwyer,[13,14] who included the effect of hole charge produced during the initial stages of a breakdown. O'Dwyer was able to predict a negative resistance type of instability in which electrons are injected from a cathode electrode by a field enhanced process, a portion of the electrons is accelerated to produce impact ionization, and the slow moving holes left behind cause an enhancement of the cathode field which leads to an increased injection current, and so on, ad infinitum. A negative resistance results from the nonlocal feedback produced by the drift of holes to the cathode. The O'Dwyer model resolves the question of why a low rate of avalanche multiplication is measured in insulators[5,15] near the breakdown field. The O'Dwyer model characterizes breakdown quite well in semiconductors and in selected insulators, but it cannot be applied directly to insulators such as SiO^2 in which hole mobility is extremely small; holes produced by impact ionization in SiO_2 are removed predominantly by recombination in the insulator.

We have proposed[16] a simple O'Dwyer type of model based on impact ionization and field distortion that is appropriate to describe breakdown in SiO_2, a material in which holes have a relatively low mobility. All of the physically significant processes are shown schematically in Fig. 1. Electrons are injected by field enhanced emission from a cathode, accelerated in the electric field, and scattered by phonon emission. A small fraction of these electrons create hole-electron pairs when they reach the ionization energy at approximately twice the bandgap E_g=9.0 eV[18], leaving behind a cloud of relatively slow moving positive charge. Holes are removed largely by recombination, with hole drift apparently playing only a minor role in the breakdown event. The net positive charge cloud leads to a larger current of more energetic electrons, leading to a negative resistance instability. A position dependent ionization rate is necessary to provide the nonlocal feedback essential for negative resistance. Although physical reality lies somewhere between the two extremes of hole annihilation by recombination and removal by drift, we find that the model based on recombination best describes the breakdown process in SiO_2. The impact ionization-recombination model, based on the most recent experimentally determined material parameters, is able to explain thickness, electrode, and radiation dependence of dielectric breakdown in thin films of SiO_2. The model is sensitive to only two key parameters, the bandgap of the insulator and the electron-phonon scattering length.

II. Impact Ionization - Recombination Model

A model calculation is based on steady state impact ionization and recombination in order to determine the J-V characteristic of a thin film of SiO_2. Dielectric breakdown in this one dimensional model occurs at the critical point at the onset of negative resistance, where $dV/dJ=0$. At currents above the critical point, the one dimensional model is generally inapplicable. Electron current is injected from the cathode electrode into the SiO_2 by the strongly field dependent process of Fowler-Nordheim tunneling[19]. The injected electrons gain energy from the field and lose it to the lattice, primarily by phonon emission. In developing a nonlocal rate of impact ionization, it is assumed that a one dimensional projection of the electron-phonon scattering events is a Poisson process, illustrated in Fig. 2, in which the probability of emitting a phonon is $(1/\lambda)$ per unit length in the X direction. The λ in this model is assumed to be energy independent. In each phonon emission event, the electron is allowed to lose the energy of an LO phonon for which $\hbar\omega = .153$ eV[20].

Based on the Poisson model, the electron energy distribution is found as a function of distance from the cathode. This distribution is obtained in terms of a single adjustable parameter λ. The probability that a given electron will have energy $\varepsilon = -n\hbar\omega$ with respect to the cathode Fermi level as it passes the point x is P, where

$$P(\varepsilon,x) = \frac{1}{(\varepsilon/\hbar\omega)!}\left(\frac{x}{\lambda}\right)^{-\varepsilon/\hbar\omega} e^{-x/\lambda} \quad .$$

We allow an electron to ionize the lattice as soon as it attains an energy of ε_i above the conduction band bottom; the rate of impact ionization is then

$$\left.\frac{\partial p^+}{\partial t}\right|_i = J\frac{\partial}{\partial x}\sum_{0}^{n = -\left(\frac{e\phi+\varepsilon_i}{\hbar\omega}\right)} P(n\hbar\omega, x),$$

where $\phi(x)$ is the energy at the bottom of the conduction band. In equilibrium, the rate of generation of holes equals that for hole recombination, leading to a charge density which is independent of the injected current J,

$$\rho_+ = \frac{e}{\langle\sigma\rangle} \frac{\partial}{\partial x} \sum_{0}^{n<-\left(\frac{e\phi+\epsilon_i}{h\omega}\right)} P(n\hbar\omega, x),$$

where $\langle\sigma\rangle$ is the weighted average recombination cross section. The potential $\phi(x)$ is then found by a double numerical integration of Poisson's equation with the initial cathode field as a boundary condition.

The material parameters used in the calculation for SiO_2 are the phonon energy $\hbar\omega=.153$ eV, $\epsilon=3.8$, and the bandgap $\epsilon_g=9$ eV. Recent evidence[21] indicates that a coulomb capture cross section is reasonable for the case of electron recombination with a trapped hole in SiO_2. The model calculations were based on a cross section[22]

$$\sigma(\epsilon) = \frac{1}{\pi}\left(\frac{3e^2}{16\epsilon\epsilon_o\epsilon}\right)^2,$$

which is $2.5 \times 10^{-13}\,cm^2$ at the electron saturation velocity in SiO_2. The electron-phonon scattering length λ was chosen to be $\lambda=1.74$ Å in order to fix the calculated breakdown voltage at $V_b=92.5$ V for a 1000 Å thick film, in agreement with the available experimental data[1,2,23,24].

The impact ionization - recombination model is used to determine the average field E and the cathode field E_c for several SiO_2 film thicknesses, from which the J-V characteristic of Fig. 3 is obtained. The one adjustable parameter λ is chosen to place the breakdown instability at 92.5 V for 1000 Å of SiO_2. For all film thicknesses above about 150 Å, a shallow negative resistance region appears above a critical point, defined by $\partial V/\partial J=0$, at which dielectric breakdown occurs. The calculated breakdown voltage was found to be relatively insensitive to the hole recombination cross section, the cathode condition, and the effective hopping mobility of the holes. The one-dimensional model calculation is strictly valid only for current densities J below the critical point; in the negative resistance regime above the critical point, a filamentary instability develops, as illustrated in Fig. 4, in which the high current associated with the negative resistance regime flows only in a small area of the film. It is the discharge of the film capacitance through the negative resistance filament which leads to a thermally destructive breakdown event.

III. Results

A. Thickness Dependence

The critical point of instability was found by numerical solution of our impact ionization-recombination model and the calculated dielectric strength was related to the SiO_2 film thickness. The thickness dependence of the experimentally determined dielectric strength[1,3,23,24] is shown in Fig. 5, along with that calculated on the basis of our ionization-recombination model (solid curve) and the O'Dwyer model (dashed curve). The sharp rise in the experimentally determined breakdown strength for thickness below ∿400 Å is well explained by the ionization-recombination model. The reason for this increase is that no ionization is possible for a region within $x_o=(\varepsilon_i+\Phi)/E$ of the cathode, so our model predicts no intrinsic breakdown for voltages less than $(\varepsilon_i+\Phi)$ or ∿12 volts. The O'Dwyer type of model shows a logarithmic dependence upon thickness, in part reflecting the use of a local ionization rate in that model. The increase in dielectric strength found in very thin films is valid, of course, only for the intrinsic type of breakdown; other types of instabilities tend to dominate in the very thin films.

B. Electrode Dependence

The experimentally determined breakdown strength[3] shows no systematic dependence upon the cathode contact barrier Φ as seen in Fig. 6. Here, the experimental uncertainty in each point is of the order of $\pm 0.5\times10^6$ V/cm. The calculated dielectric strength based on our ionization-recombination model shows a very weak dependence on the barrier Φ, in agreement with the general trend of the experimental findings. Calculations, based on an O'Dwyer type of model show a stronger dependence on Φ at the injecting contact. This difference in barrier dependence results directly from the mechanism of clearing holes from the insulator. Based on the data available, it seems that recombination is the dominant mechanism in SiO_2. The Φ independence in the dielectric strength of SiO_2 is not expected to extend to the case of low work function contact structures, in which a thermal instability may be the dominant breakdown mechanism.

C. Time Dependence

A finite time is necessary for an intrinsic breakdown instability to develop because of the time required for the buildup of the positive charge cloud. Although, the exact solution for the time lag is difficult because of the nonlinear equations involved, an estimate can be made for the case of a relatively thick film. Neglecting recombination at fields above breakdown, on estimate τ, is,

$$\tau \sim \frac{Q_c}{\alpha L J} ,$$

where Q_c is the critical charge density, α is the continuum ionization rate, L is the film thickness, and J is the initial tunneling current. Then,

$$\tau \sim \frac{Q_c v}{b L A E^2} e^{\frac{\beta + H}{E}}$$

where b, H, and Ω determine the electron ionization rate[5,14] and A and β determine the Fowler-Nordheim tunneling. It is seen that the time lag in the breakdown process is strongly dependent upon field.

D. Radiation Sensitivity

Since intrinsic dielectric breakdown in SiO_2 involves the development of a positive charge cloud in the insulator, it may be possible to initiate the breakdown process by creating the positive charge by means of exposing the sample to an ionizing beam of radiation. MOS capacitors which were exposed to UV radiation at $\hbar\omega = 9.7$ eV show a dramatic and repeatable reduction of dielectric strength[4]. The breakdown strength, measured by a self-healing technique, shows a reduction with increasing radiation intensity down to a saturation level which is approximately half the intrinsic dielectric strength. Figure 7 shows the results for a film of 6920Å thickness.

E. Trapped Charge

Based on the ionization-recombination model of the breakdown process in SiO_2, we would expect a stable charge cloud to form at fields below that at which breakdown takes place. Recently Shatzkes and Av-Ron[25] have been able to measure this charge Q and its centroid X; they used a combination of field emission and C-V measurements, performed at low field, to determine the remnant charge left from a previous high field pulse. Their results for charge density Q are shown in Figure 8 for SiO_2 films of thickness 263 Å and 493 Å. The charge Q calculated on the basis of the ionization-recombination model for 1000 Å of SiO_2 is shown as the solid curve in the figure. The reasonably good overall agreement with experiment indicates the existance of a stable charge cloud which behaves in a way predicted by the ionization-recombination theory.

IV. Discussion

The impact ionization-recombination model for dielectric breakdown seem to be in reasonably good agreement with available data for SiO_2. From the model, a picture can be formulated of the significant processes which occur during breakdown. The electrons are field emitted into the SiO_2 from the cathode electrode. The hottest of the electrons ionize the lattice, leaving behind slow moving holes. A cloud of positive charge formed by ionization and recombination leads to an increased current of hotter electrons. The result is that a negative resistance type of instability develops in which a local charge cloud leads to an enhanced current. The small fillament of current drains charge from the capacitor in a destructive breakdown event.

During the electronic breakdown process, the experimental evidence indicates that recombination is the most important mode of removing holes produced by impact ionization. Hole drift to the cathode seems to play a relatively minor role in determining the conditions leading to dielectric breakdown. One piece of experimental evidence, the dependence, of dielectric strength on the cathode contact barrier, shows no systematic variation which would be expected if drift were the dominant mechanism of clearing holes from the insulator. The problem of hole transport in SiO_2 is a rather complex one, with some evidence[7] that these are two modes, one relatively fast and one trap limited and slow. In the model, we are concerned with only the slow holes, since the fast holes contribute little to the field distortion. A more accurate model, including the complexities of hole transport, is expected to show the same general characteristics as our simple model.

V. Acknowledgment

The authors wish to acknowledge A. A. Levi for the numerical computation involved in the model and M. Av-Ron for use of his unpublished data.

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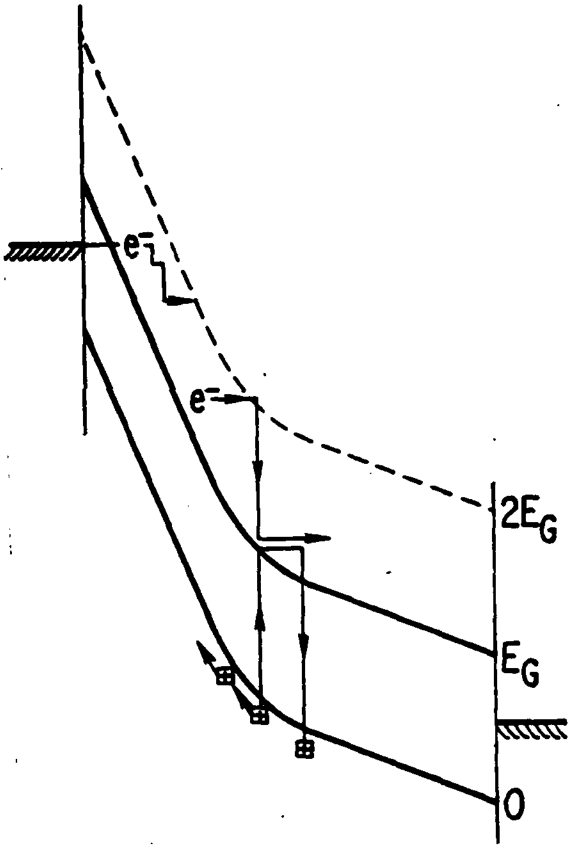

Figure 1: A schematic representation of the events which occur in the beginning stages of dielectric breakdown in SiO_2.

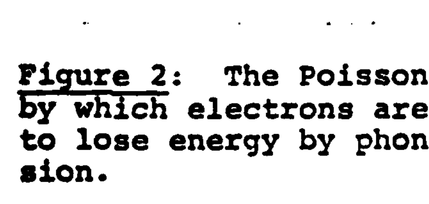

Figure 2: The Poisson process by which electrons are assumed to lose energy by phonon emission.

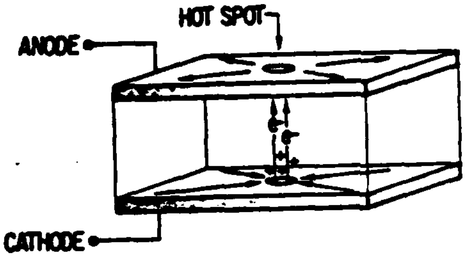

Figure 4: A destructive dielectric breakdown in an SiO_2 capacitor. Electronic current through a negative resistance filament drains charge from the electrodes and heats a local region of the capacitor.

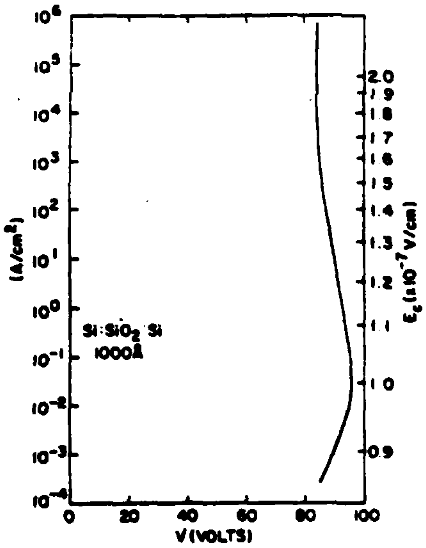

Figure 3: Calculated current density vs. voltage for 1000 Å of SiO_2 showing the existence of a negative resistance region.

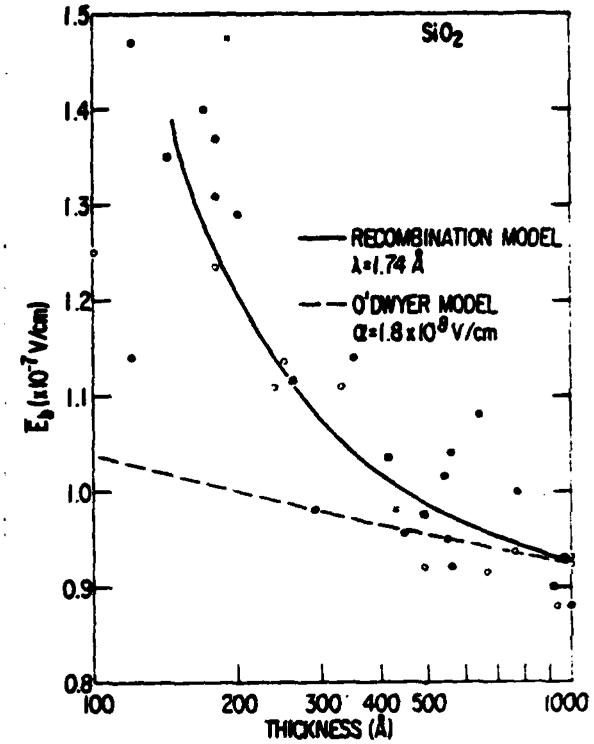

Figure 5: Calculated dielectric strength of SiO_2 as a function of thickness, with experimentally determined points.

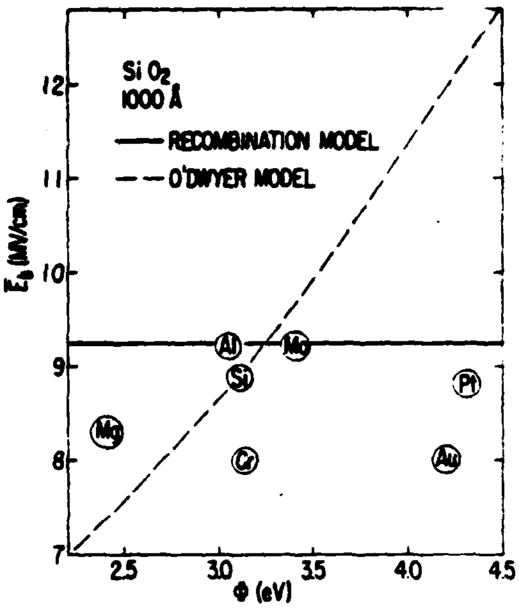

Figure 6: Calculated dielectric strength of 1000 Å of SiO_2 as a function of electrode work function, for the recombination model and the O'Dwyer model. Experimental points from Ref. (3).

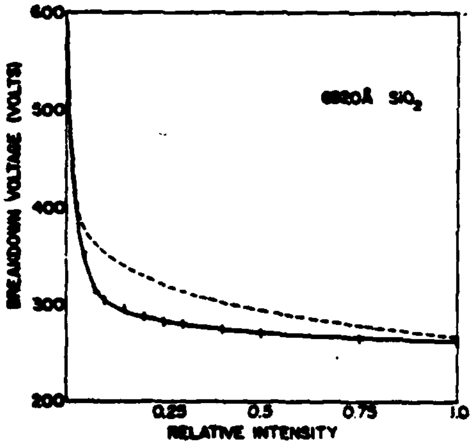

Figure 7: The dielectric breakdown voltage of 6920 Å of SiO_2 as a function of intensity of irradiating energy 9.7 eV, from Ref. (4).

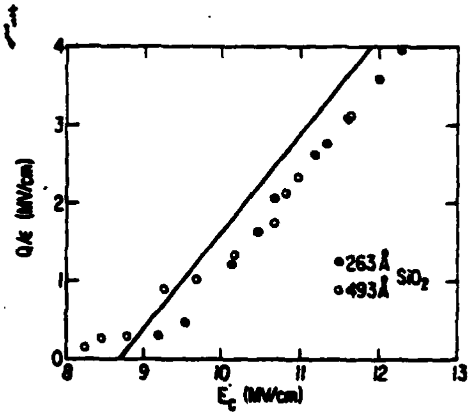

Figure 8: Total remnant charge Q left in SiO_2 capacitor by a voltage pulse producing cathode field E_c. Solid line is predicted by theory.

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Solid State Physics 8 pages

ROOM TEMPERATURE CONDUCTIVITY AND LOCATION OF MOBILE SODIUM IONS IN THE THERMAL SILICON DIOXIDE LAYER OF A METAL-SILICON DIOXIDE-SILICON STRUCTURE*

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ABSTRACT

Room temperature conductivity of mobile Na^+ ions in the SiO_2 layer of a MOS structure is directly shown to be interface-limited by use of the photo I-V technique. Na^+ ions were found to be located within ≈50 Å of the interfaces regardless of field stressing conditions (2-4.5 MV/cm), temperature (20-40 °C), number of ions drifted (up to 2.6×10^{12} cm^{-2}), or number of temperature-bias cycles used to move Na^+ ions back and forth between the interfaces.

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Room temperature conductivity of mobile Na^+ ions in the thermal SiO_2 layer of a metal-silicon dioxide-silicon (MOS) structure is investigated in this study using the photo I-V technique [1-4]. In this report, the location of the mobile Na^+ ions as they are moved around in the oxide layer of the MOS structures under different temperature-bias stressing conditions directly shows that the ions are always found near the interfaces (within about 50 Å) regardless of temperature between 20-40 °C, field stressing conditions between 2-4.5 MV/cm, the number of Na^+ ions drifted (up to 2.6×10^{12} cm^{-2}), or number of temperature-bias stressing cycles. This clearly shows that room temperature mobile Na^+ ion conductivity is interface-limited as opposed to bulk-limited. This observation is consistent with those of others who used more indirect capacitance-voltage (C-V) measurements [5,6] which are only sensitive to the charge-centroid product [7,8].

The MOS samples (Al—SiO_2(500Å)—.1 Ωcm p-Si(<100>)) used for the photocurrent measurements were similar to those described in a previous publication [9] except that the Al gate electrode was semitransparent (130 Å) surrounded by a frame region for contacting purposes which was ≈ 17% of the device area. The rectangular device area was 3.83×10^{-3} cm^2, and samples where mounted on TO-5 headers. Prior to metallization $\geq 10^{13}$ Na^+ ions/cm^2 were evaporated from NaCl salt onto the outer SiO_2 surface [9]. Na^+ ions can readily move through the SiO_2 layer, but the compensating Cl^- ions are expected to remain at the Al-SiO_2 interface because of their larger size.

The photo I-V technique [1-4] and the experimental set-up [10] have been described in detail in other publications. Na^+ ions were drifted back and forth between the interfaces at temperatures between 20-40 °C, at fields of 2-4.5 MV/cm, and for times from minutes to hours. Flat-band voltage shifts from C-V measurements of 0 to -5.5 V were typical corresponding to Na^+ ion densities up to 2.6×10^{12} cm^{-2}. After temperature-bias stressing, the samples were cooled under bias and vacuum ($\leq 10^{-5}$ Torr) conditions to liquid nitrogen temperature (77 °K) in order to freeze-out any further ionic motion [9] which would interfere with the photo I-V measurements. All photo I-V measurements were performed at 77 °K using an Air Products Heli-Tran low temperature dewar with an optical port and a sample holder for the TO-5 headers made from sapphire (good thermal conductivity, but electrically insulating). The sample holder also had a field shield plate which could be biased if necessary to surpress any extraneous currents due to vacuum external photoemission from any surface exposed to the light beam. Samples were cycled back and forth between 77 °K and 20-40 °C to shift varying amounts of Na^+ back and forth in the SiO_2 layer. Photo I-V measurements were done using 5 eV light for positive gate bias and either 4.5 or 5 eV light for negative gate bias. All results reported here were reproducible on a given sample and from sample to sample. Typical results of any of the measurements are shown in Figs. 1 and 2.

Figures 1 and 2 are photo I-V characteristics [11] after various amounts of Na^+ had been drifted towards the Si-SiO_2 interface or back towards the Al-SiO_2 interface in subsequent cycles at temperatures between 20 °C to 40 °C at fields of ≈ 3 MV/cm for times from 5 min. to 40 min. The corresponding flat-band voltage shifts (ΔV_{FB}) deduced from capacitance-voltage (C-V) measurements are listed in the figure captions. These data are characteristic of a given ΔV_{FB} regardless of the number of temperature-bias cycles the sample had undergone or the order in which they were done.

The data in Figs. 1 and 2 are consistent with Na^+ ions distributed near the Si-SiO_2 interface [2-4, 12] for any of the stressing conditions. Fig. 1 (Si photoinjecting) shows increased changes in the shape of the photo I-V characteristic as compared to the control ($\Delta V_{FB}=0$) with increasing flat-band voltage shift magnitude and hence with increasing Na^+ ion concentration. The photo I-V curves in this figure for $\Delta V_{FB} < 0$ are splitting and shifting with increasing field towards lower applied gate bias as has been seen before for positive charge (trapped holes) distributed near the Si-SiO_2 interface [2-4]. Fig. 2 (Al photoinjecting) shows very little difference of the photo I-V curves for any of the cases listed. At higher voltages there is a slight splitting with increasing field of the photo I-V curves where the characteristics are shifted towards more negative voltages. This could be due to negative charge (probably from the uncompensated immobile Cl^- ions) very near the Al-SiO_2 interface or the absence of the Na^+ ions that have been drifted to the Si-SiO_2 *interface*. Nevertheless, the pronounced differences between Figs. 1 and 2 imply that Na^+ at the Si-SiO_2 interface has a different effect (due to location and possible lack of compensating ions) on the photo I-V characteristic for Si injecting (Fig. 1) than Na^+ at the Al-SiO_2 interface for Al injecting (Fig. 2). Na^+ appears to be approximately at the Al-SiO_2 interface as compared to being *distributed* near the Si-SiO_2 interface [2-4].

An estimate of the position of the Na^+ centroid from the Si-SiO_2 interface can be obtained by using the low field region of Fig. 2 (oxide voltage drop $\lesssim$ - 4 V) which is not as sensitive to charge near the Al-SiO_2 interface and by using the photo I-V relation $\Delta V_g^- = (1 - L/\bar{x})\Delta V_{FB}$ as discussed in previous publications [1-4]. Using $\Delta V_{FB} = -3.05$ V, a photo I-V shift ΔV_g^- for Al photoinjecting of $\approx .34$ V or $\approx .16$ V should be observed for a centroid distance from the Si-SiO_2 interface $L-\bar{x}$ of 50 Å or 25 Å, respectively. Clearly, the centroid is closer than 50 Å from the Si-SiO_2 interface from the data of Fig. 2.

Displacement current effects [1,2] due to electron capture at 77 °K by Na^+ ions or traps present in the as grown *oxide* [9] were negligible under the conditions of the photo I-V measurements and had no influence on the shape of the photo I-V characteristics [1,2]. It is interesting to note that because of the very low electron trapping probability of the Na^+ ions (which is $\leq 10^{-3}$ for capture cross sections $\leq 10^{-15}$ cm^2 and Na^+ related trap areal densities of $\leq 10^{12}$ cm^{-2} [9]) dips seen in data similar to Fig. 2 for the case of trapped holes near the Si-SiO_2 *interface* [2,3] are absent. These dips appeared in the vicinity of the flat-band voltage and were attributed to a displacement current effect as the Si surface potential changed in time due to electron annihilation of trapped holes (trapping probability of ≤ 1 for a field dependent coulombic capture cross section of 10^{-12} - 10^{-15} cm^2 over the range of electric fields of interest and for trapped hole densities of $\leq 10^{12}$ cm^{-2} [2,4]).

For reasons of discreteness of charge and dependence on the internal photoemission model [2, 12-13], the Na^+ ion charge distribution near the Si-SiO_2 interface was not profiled using the data of Fig. 1 and the Powell-Berglund technique [12]. For 10^{12} trapped charges/cm^2 (average separation of 100 Å), discreteness effects become important if these charges are < 20 Å from the photoinjecting interface because of a three-dimensional distribution of the potential near the interface.

Figs. 1 and 2 directly show that there are no significant numbers of Na^+ ions in the bulk of the SiO_2 film for the ion drift conditions studied here. This implies that the transport process of mobile sodium in these MOS structures at temperatures from 20 °C to 40 °C for the stressing times, stressing fields, and amounts of drifted ions is limited by the escape of the Na^+ ions from the interfacial region (interface-limited as opposed to bulk-limited ionic conductivity). This interpretation is also consistent with the experimental observations, using flat-band voltage shifts, that Na^+ ions moved back towards the Al-SiO_2 interface more easily than towards the Si-SiO_2 interface. This interface-limited conductivity is also in agreement with the results of others (for the experimental conditions used here) from more indirect C-V measurements which used flat-band voltage shifts as a function of time and applied voltage to investigate the ionic conduction mechanisms [5,6]. At higher temperatures (>40 °C), there is much experimental evidence for interface limited conductivity using many techniques [14]. All these techniques (thermally stimulated ionic conductivity, charge-time, C-V, threshold voltage shifts of field effect transistors, current-voltage using a slow linear ramp, and radioactive tracers [14]) indicate that Na^+ ions move more readily from near the Si-SiO_2 interface towards the metal-SiO_2 interface (at least for Al or Au gate electrodes) than in the oppositive direction.

Finally in view of the results presented here which imply Na^+ ions are near the interfaces, data interpretation in a previous publication [9] on similar samples which had undergone similar temperature stressing conditions can be further extended. In Figs. 2 and 3 of reference 9, *effective* electron trap density as a function of *effective* Na^+ density were shown where the *effective* density is defined as the first moment (centroid multiplied by the total number of traps or ions per unit area) divided by oxide thickness. For the Na^+ related trapping sites, these figures now are indicative of the *actual* trap densities as a function of *actual* Na^+ density.

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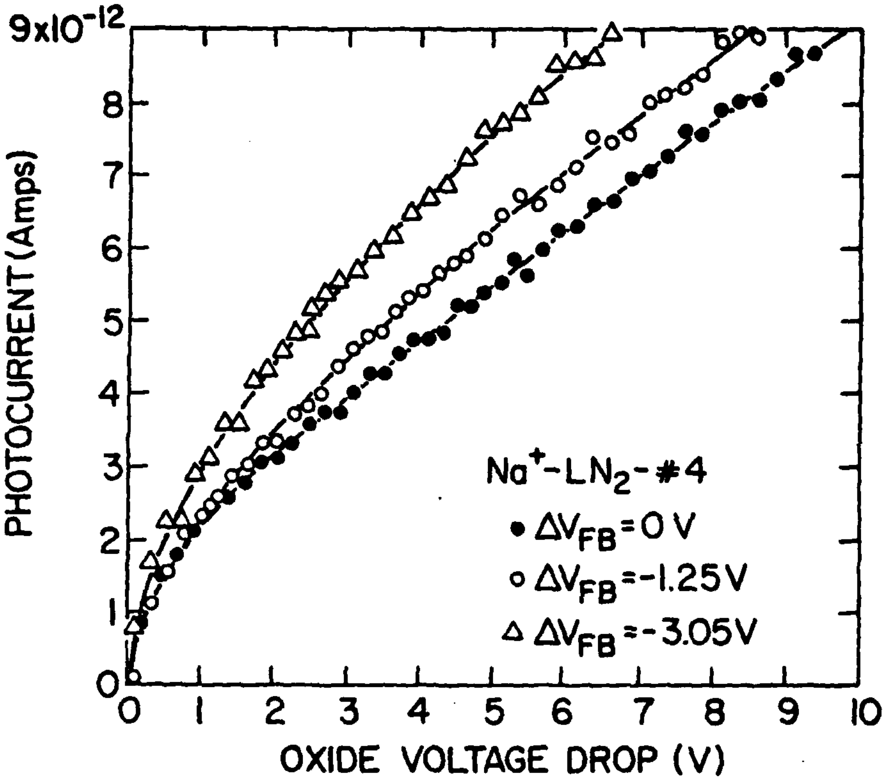

Figure 1: Photocurrent at 77 °K using 5 eV light as a function of the oxide voltage drop for positive gate polarity (Si injecting) and various flat-band shifts (ΔV_{FB}) associated with Na^+ ions.

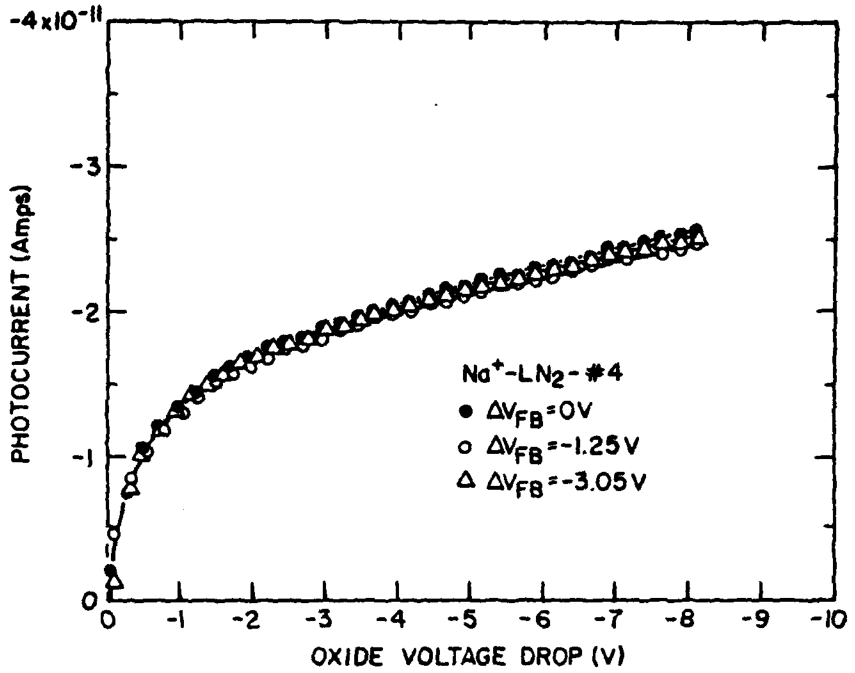

Figure 2: Photocurrent at 77 °K using 5 eV light as a function of the oxide voltage drop for negative gate polarity (Al injecting). The sample and the flat-band shifts are the same as in Fig. 1.

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THE ELECTRONIC STRUCTURE OF SiO_2, GeO_2 AND INTERMEDIATE $Si_xGe_{1-x}O_2$ COMPOSITIONS: EXPERIMENT AND THEORY*

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Theoretical calculations are reported for SiO_2, GeO_2 and the intermediate composition $Si_{.5}Ge_{.5}O_2$ which reproduce the main observed features and trends in experimental photoemission spectra. The agreement between the two establishes the importance of band theory in understanding the electronic structure of these materials, and demonstrates that detailed quantitative predictions are feasible for such complex materials in terms of the empirical tight-binding method. The calculations further establish that the structure in the valence bands is determined mainly by nearest-neighbor oxygen-oxygen interactions.

The electronic structure of SiO_2 and GeO_2 has been the subject of considerable attention in the literature. Most attempts have, however, mainly focused on *interpreting* experimental data (optical absorption, x-ray absorption, x-ray emission, photoemission, etc.) in terms of simple "molecular-orbital" energy levels. Such assignments have worked well for certain experimental spectra, but at the same time were incompatible with other spectra.[1,2] Furthermore, several assignment schemes, based on similar ideas, differ substantially from each other. One difficulty arises from the fact that the crystal structures of these materials are complex, with low symmetry and many atoms in a primitive unit cell. This complexity has inhibited the successful application of band-theoretic techniques which have in the past proven very powerful for simpler materials. Recently, Pantelides and Harrison[2] (PH) and Schneider and Fowler[3] (SF) performed energy band calculations for SiO_2 and independently pointed out the importance of energy-band theory for a systematic interpretation of the data. PH went beyond SF in calculating densities of states (DOS) but both used the band results only as *guides* to interprete the data, leaving a host of questions unresolved. The nature of the electronic states in these materials has not therefore thus far been conclusively determined due to the inability of theory to directly and unambiguously reproduce the observed spectra.

In the present paper we present theoretical calculations of the photoemission spectra of SiO_2, GeO_2, and the intermediate composition $Si_{.5}Ge_{.5}O_2$, which reproduce the important features and trends in the observed spectra. The results show that a molecular-orbital picture about a single oxygen atom is inadequate. They also establish the importance of band theory for these materials and show that quantitative predictions are feasible for materials of such high complexity and low symmetry. Finally, they establish that the bandwidth and much of the internal structure are largely determined by the nearest-neighbor oxygen-oxygen p-orbital interactions, a factor which should be central in understanding the electronic propeties of all the silicate glasses.

The ultraviolet photoemission spectroscopy (UPS) measurements were performed using a cylindrical mirror electrostatic-deflection type electron energy analyzer (resolution 0.25 eV) and 40.8 eV photons from a He-discharge lamp. The x-ray photoemission spectroscopy (XPS) measurements were performed with a Hewlett-Packard x-ray photoelectron spectrometer which has a monochromatic Al $K\alpha_{1,2}$ x-ray source (1486.6 eV) and a resolution of 0.6 eV. First, Si_xGe_{1-x} films several thousand Ångstroms thick were deposited on sapphire substrates by DC sputtering from targets formed by melting high-purity polycrystalline silicon and germanium onto a molybdenun substrate. The $Si_xGe_{1-x}O_2$ films which were studied with UPS were oxidized *in situ* in the spectrometer by heating to 450° C for 15 minutes in 10^{-5} torr of oxygen. The films studied with XPS were oxidized by heating in oxygen to 650° C for two hours in a tube furnace and then immediately transferred to the spectrometer vacuum. The compositions of the films used in the UPS experiments were determined by electron microprobe analysis and the compositions of the films used in the XPS experiments were estimated from the relative internsities of XPS spectra from the Ge 3d, Si 2p, and O 1s core levels. The oxide films were thicker than the escape depth of the photoelectrons, as evidenced by the absence of unoxidized Si or Ge core levels in the spectra. More experimental details are given in Ref. 4. The experimental spectra are shown in Fig. 1.

The theoretical calculations were carried out in terms of the empirical tight-binding model employed by PH. The basis orbitals are the tetrahedrally-oriented sp^3

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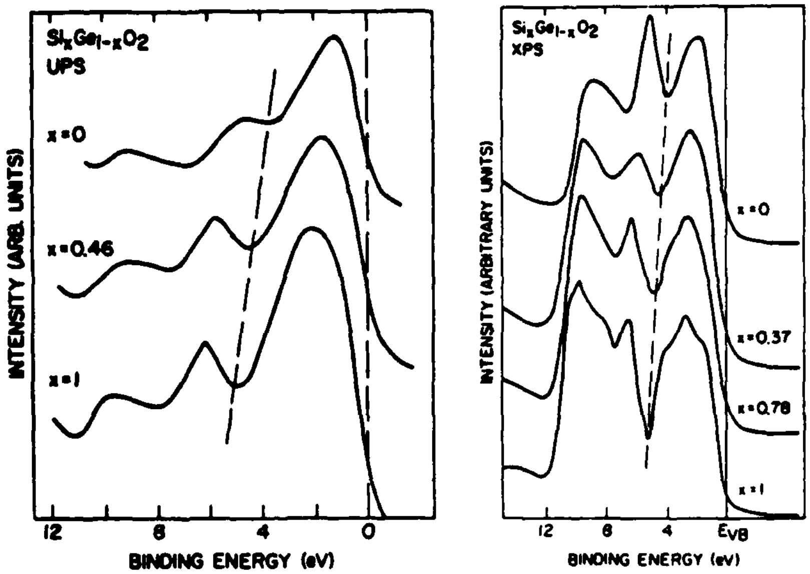

Fig. 1. Experimental UPS and XPS spectra for $Si_xGe_{1-x}O_2$ films.

hybrids on the Si/Ge atoms and the p orbitals on the oxygens. These orbitals (Fig. 2) are allowed to interact, giving rise to five types of orbitals: (1) a bonding orbital B_z comprized of p_z and the odd combination of the hybrids, (2) an orbital B_x comprized of p_x and the even combination of the hybrids ($B_x = p_x$ for the ideal cubic structure, Fig. 2a), (3) a non-bonding orbital $B_y = p_y$, and (4,5) two corresponding antibonding orbitals A_z and A_x. The B's are occupied, giving rise to the valence bands while the A's are empty, giving rise to the conduction bands. For the intermediate $Si_{.5}Ge_{.5}O_2$ composition, the main additional[5] effect is a mixing between B_x and B_z.

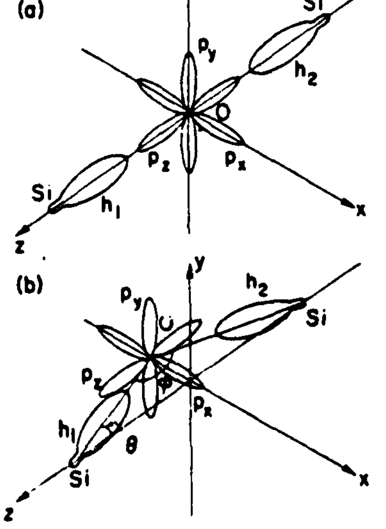

Fig. 2. The tight-binding orbitals employed in the calculations. (a) For the ideal cubic structure, and (b) for the general case.

The precise composition of the various A's and B's, as well as their energy positions are entirely determined in terms of two parameters, the hybrid--p-orbital interaction W_2 and the hybrid--p-orbital energy separation W_3. These have been fixed by making use of the optical spectrum of SiO_2 (see Ref. 2). The parameters for GeO_2 and the intermediate compositions are then determined by making use of the relative hybrid energies of Si and Ge and the d^{-2} rule, where d is the bond length.[2] With the basis orbitals just defined, a tight-binding energy band calculation is carried out by retaining only nearest-neighbor interactions. This introduces two new parameters, a hybrid hybrid interaction V_1 (carried over from previous work on the tetrahedral semiconductors) and the oxygen-oxygen ppσ interaction V_p. The latter is adjusted to the observed total width of the valence bands of SiO_2. For GeO_2 and the intermediate compositions V_p is scaled with the d^{-2} rule. The valence bands obtained for cubic SiO_2 with these choices are in very good accord with the first-principles bands of SF. We are now in position, however, to bend the Si-O-Si chains to the observed angles (144°) and repeat the calculations and obtain the valence bands and corresponding DOS for the various cases of interest. The latter are then broadened by convoluting with a gaussian of width 0.5 eV. This broadening turns out to be extremely important as it eliminates most of the sharp spiked structures in the DOS (see Fig. 3) which precluded PH from carrying out more than a qualitative analysis of the observed spectra.

The final broadened DOS curves for SiO_2, GeO_2 and $Si_{0.5}Ge_{0.5}O_2$ (or $SiGeO_4$), are shown in Fig. 4 for direct comparison with Fig. 1. In view of the fact that the calculation did not include photoemission matrix elements, the comparison must be limited to the overall trends among the various compositions and to the positions of dips and peaks in the individual spectra. No comparison can be made of the relative heights of peaks.

It is seen that the overall trends present in the data are reproduced by the theory. In particular, the total width decreases as one goes from SiO_2 to GeO_2. Also the main dip at about 4 eV fills up slowly and moves to higher energies in both the experimental and theoretical curves, as shown by the dashed lines in Figs. 1 and 4.

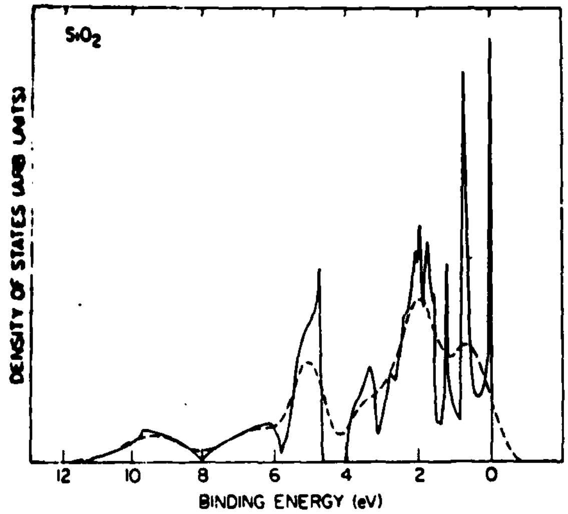

Fig. 3. Density of States (DOS) and broadened DOS for the valence bands of SiO_2.

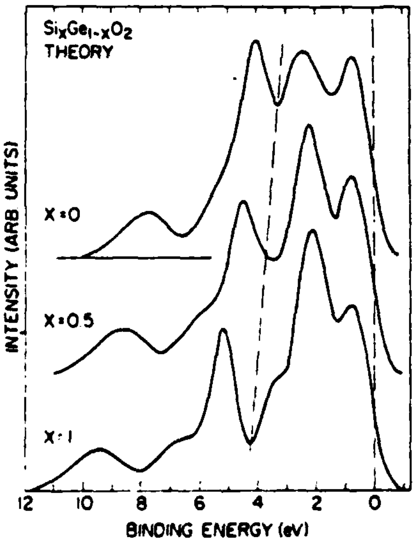

Fig. 4. Theoretical photoemission spectra for $Si_xGe_{1-x}O_2$ films. Compare with Fig. 1.

For more detail comparison between theory and experiment, the positions of the peaks and dips in the theoretical and experimental curves of SiO_2 and GeO_2 are listed in Table I. For the purposes of this Table, the zero of energy in the theoretical curves was redefined by the technique employed in obtaining the zero of energy in the experimental spectra, namely by linear extrapolation of the descending curve. The main discrepancy in both materials is peak 1 which appears as a double peak in the theoretical curves. The agreement between *experiment*[6] *and theory for the remaining features* is better than 15%.

TABLE I

Experimental and theoretical positions (in eV) of peaks and dips in the photoemission spectra of SiO_2 and GeO_2. The numbering refers to Fig. 1 in order of increasing binding energy.

Feature	XPS	UPS	Theory
SiO_2			
dip 1	5.3	5.3	4.7
dip 2	7.6	8.1	8.5
peak 1	2.8	2.6	1.2,2.5
peak 2	6.5	6.4	5.7
peak 3	9.8	9.8	9.9
total width	11.5	11.2	11.7
GeO_2			
dip 1	4.0	4.0	3.7
dip 2	6.6	6.9	7.0
peak 1	1.9	1.8	1.2,2.9
peak 2	5.1	5.0	4.5
peak 3	8.7	9.3	8.3
total width	10.4	10.1	10.0

The empirical tight-binding method employed in the calculations presented above allows a detailed analysis of the results in terms of simple physical concepts. For example, it has long been suggested that the top of the valence bands, in particular the broad feature from 0 to about 4 eV, arises from the non-bonding oxygen p orbitals, whereas the remainder of the bands arises from the bonding orbitals. The present calculations show this separation to be an oversimplification of reality. First note that the Si-O interaction (W_2) is responsible for the formation of the bonding orbitals. It is the O-O interaction V_p alone that causes the banding of the non-bonding orbitals, and it is V_p together with V_1 that cause the banding of the bonding orbitals. The same V_p, however, is also responsible for the admixture between the bonding and non-bonding orbitals, the net result being a strong hybridization between the bonding and non-bonding bands. The nature of the hybridization is particularly interesting. If it is turned off, the pure non-bonding bands overlap considerably with the pure bonding ones. When the hybridization is turned on, the two sets of bands push strongly on each other, opening up a gap at 4 eV (Fig.3). This is opposite to what a molecular-orbital picture would suggest, since the presence of a gap between two levels would be viewd as a consequence of hybridization.

In conclusion, we have presented new experimental spectra which help establish the electronic structure of SiO_2 and GeO_2. Theoretical calculations in terms of the empirical tight-binding method (ETBM) have proved successful in reproducing the experimental spectra and establishing the validity of the band picture for these rather complex materials. It should be emphasized that only the total width of the bands of SiO_2 was used as an input in performing the calculations. The internal structure in the spectrum of SiO_2, as well as the other spectra in their entirety, were *predicted* and found to be in good agreement with experiment. This demonstrates the capability of the ETBM to yield quantitative predictions for materials for which other methods may not be too convenient to apply due to low symmetry and complicated lattices.

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6. The small discrepancies between XPS and UPS in Table are attributed to differences in the intrinsic broadening of the curves in the two types of experiments.