



القائب فحد معادمة وداموا محدور المترجان المتراعة فالاتفاق فالتعاني كالألير لالالتريز وربعا والعظ

MICROCOPY RESOLUTION TEST CHART NATIONAL BUREAU OF STANDARDS-1963-A

MTR-8768

# P

# CONCEPTUAL HARDWARE DESIGN FOR THE DRAMA SERVICE CHANNEL CONTROLLER

By D. E. PAULEY

MAY 1983

AD A129346

Prepared for DEPUTY FOR TACTICAL SYSTEMS ELECTRONIC SYSTEMS DIVISION AIR FORCE SYSTEMS COMMAND UNITED STATES AIR FORCE

Hanscom Air Force Base, Massachusetts





**IIC** FILE COPY

Approved for public release; distribution unlimited. Project No. 4920 Prepared by THE MITRE CORPORATION Bedford, Massachusetts Contract No. F19628-82-C-0001

006 83 63 24

When U.S. Government drawings, specifications, or other data are used for any purpose other than a definitely related government procurement operation, the government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise, as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

Do not return this copy. Retain or destroy.

# **REVIEW AND APPROVAL**

This technical report has been reviewed and is approved for publication.

Robert E. Merten 65-12

**ROBERT E. NEIFER, GS-12** 

FOR THE COMMANDER

hn Emign

JOHN E. MEYN, Maj. USAF DEB Program Manager

UT CAP

KARLIN B. JESSEN, 2Lt, USAF

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
REPORT NUMBER 2. GOVT ACCESSION NO	A RECIPIENT'S CATALOG NUMBER
FSD_TR_83_133 A129 31	6
I. TITLE (and Subtitle)	5 TYPE OF REPORT & PERIOD COVERED
CONCERTING MADDIARE DECISION FOR MILE	
CONCEPTUAL HARDWARE DESIGN FOR THE	
DRATE SERVICE CHANNEL CONTROLLER	6. PERFORMING ORG. REPORT NUMBER
	MIK-8700
D. E. PAULEY	F19628-82-C-0001
PERFORMING ORGANIZATION NAME AND ADDRESS	10. PROGRAM ELEMENT. PROJECT, TASK AREA & WORK UNIT NUMBERS
The MITRE Corporation	
Bedford MA 01730	Project No. 4920
Derute for Techical Custome	MAY 1983
Electronic Systems Division AFSC	13. NUMBER OF PAGES
Hanscom AFB, MA 01731	100
4. MONITORING AGENCY NAME & ADDRESS(it different from Controlling Office)	15. SECURITY CLASS. (of this report)
	UNCLASSIFIED
	150 DECLASSIFICATION DOWNGRADING
	SCHEDULE
Approved for public release; distribution unlimit	ed.
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different for	ed.
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different for	ed . rom Report)
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different h	ed . rom Report)
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, 11 different for 8. SUPPLEMENTARY NOTES	ed.
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, 11 different for 8. SUPPLEMENTARY NOTES	ed . rom Report)
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different for 8. SUPPLEMENTARY NOTES	ed . rom Report)
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, 11 different for 8. SUPPLEMENTARY NOTES	ed . rom Report)
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different for 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block numbe COMMINICATIONS NETWORK	ed . rom Report)
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different for 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block number COMMUNICATIONS NETWORK DCS SERVICE CHANNEL NETWORK	ed . rom Report)
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, 11 different for 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block numbe COMMUNICATIONS NETWORK DCS SERVICE CHANNEL NETWORK PACKET SWITCHING	ed . rom Report)
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different for 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block number COMMUNICATIONS NETWORK DCS SERVICE CHANNEL NETWORK PACKET SWITCHING SYSTEM CONTROL	ed . rom Report)
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the obstract entered in Block 20, if different for 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block number COMMUNICATIONS NETWORK DCS SERVICE CHANNEL NETWORK PACKET SWITCHING SYSTEM CONTROL	ed . rom Report) r)
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, 11 different for 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block number COMMUNICATIONS NETWORK DCS SERVICE CHANNEL NETWORK PACKET SWITCHING SYSTEM CONTROL 0. ABSTRACT (Continue on reverse side if necessary and identify by block number	ed . rom Report) r)
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, 11 different for 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block number COMMUNICATIONS NETWORK DCS SERVICE CHANNEL NETWORK PACKET SWITCHING SYSTEM CONTROL 0. ABSTRACT (Continue on reverse side if necessary and identify by block number The need for a survivable, flexible DCS serv	ed.
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different for 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block number COMMUNICATIONS NETWORK DCS SERVICE CHANNEL NETWORK PACKET SWITCHING SYSTEM CONTROL 0. ABSTRACT (Continue on reverse side if necessary and identify by block number The need for a survivable, flexible DCS serv network has been established. This report presen	ed.
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the obstract entered in Block 20, 11 different for 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block number COMMUNICATIONS NETWORK DCS SERVICE CHANNEL NETWORK PACKET SWITCHING SYSTEM CONTROL 0. ABSTRACT (Continue on reverse side 11 necessary and identify by block number The need for a survivable, flexible DCS serv network has been established. This report presen design for a communications processor that can be the communications of multiple subsystems using t	ed. Tom Report) Tom Report) Tice channel communications ts a conceptual hardware to used to efficiently control the DRAMA Radio service
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the obstract entered in Block 20, 11 different for 8. SUPPLEMENTARY NOTES 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block number COMMUNICATIONS NETWORK DCS SERVICE CHANNEL NETWORK PACKET SWITCHING SYSTEM CONTROL 0. ABSTRACT (Continue on reverse side if necessary and identify by block number The need for a survivable, flexible DCS serv network has been established. This report presen design for a communications processor that can be the communications of multiple subsystems using t channel. The cost of a network implemented with	ed. Tom Report) f) fice channel communications its a conceptual hardware is used to efficiently control the DRAMA Radio service the processor is comparable
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the obstract entered in Block 20, 11 different for 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block number COMMUNICATIONS NETWORK DCS SERVICE CHANNEL NETWORK PACKET SWITCHING SYSTEM CONTROL 0. ABSTRACT (Continue on reverse side II necessary and identify by block number The need for a survivable, flexible DCS serv network has been established. This report presen design for a communications processor that can be the communications of multiple subsystems using t channel. The cost of a network implemented with to a less survivable, and less flexible, network	ed. rom Report) r) r) r) r) r) r) r)
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the obstract entered in Block 20, if different in 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block number COMMUNICATIONS NETWORK DCS SERVICE CHANNEL NETWORK PACKET SWITCHING SYSTEM CONTROL 0. ABSTRACT (Continue on reverse side if necessary and identify by block number The need for a survivable, flexible DCS serv network has been established. This report presen design for a communications processor that can be the communications of multiple subsystems using t channel. The cost of a network implemented with to a less survivable, and less flexible, network multiplexers and bridges.	ed. Tom Report) Tom Report Tom Report To a conceptual hardware Tom set a conceptual hardware To
Approved for public release; distribution unlimit 7. DISTRIBUTION STATEMENT (of the obstract entered in Block 20, 11 different for 8. SUPPLEMENTARY NOTES 8. SUPPLEMENTARY NOTES 9. KEY WORDS (Continue on reverse side if necessary and identify by block number COMMUNICATIONS NETWORK DCS SERVICE CHANNEL NETWORK PACKET SWITCHING SYSTEM CONTROL 0. ABSTRACT (Continue on reverse side 11 necessary and identify by block number The need for a survivable, flexible DCS serv network has been established. This report present design for a communications processor that can be the communications of multiple subsystems using to channel. The cost of a network implemented with to a less survivable, and less flexible, network multiplexers and bridges.	ed. Tom Report) The channel communications the channel communications the second to efficiently control the DRAMA Radio service the processor is comparable implemented with conventional

# ACKNOWLEDGMENTS

This document has been prepared by The MITRE Corporation under Project 4920, Contract F19628-82-C-0001. The contract is sponsored by the Electronic Systems Division, Air Force Systems Command, Hanscom Air Force Base, Massachusetts.

States and Street States and States



a astar

# TABLE OF CONTENTS

Section			Page
	LIST	OF ILLUSTRATIONS	4
1	INTRO	DDUCTION	5
2	SYST	EM CONCEPTS	7
	2.1	DCS Requirements	8
	2.2	Hardware Concepts	9
	2.3	Packet Switch Implementation	13
3	SERVI	ICE CHANNEL CONTROLLER	15
	3.1	Hardware Architecture	15
	3.2	Network Interface Processor	17
	3.3	Redundancy Considerations	23
	3.4	Voice Transmission Considerations	23
4	COST	COMPARISON	26
5	RECON	MMENDATION	27
APPENDIC	ES		28
A DRA	MA Muli	tiplexer Implementation Data	28
B Har	dware 1	Data Sheets	35
C Ser	vice Cl	hannel Controller Cost Data	92

# LIST OF ILLUSTRATIONS

Figure		Page
1	Service Channel Controller	10
2	Statistical Multiplexer Concept	12
3	Fixed Multiplexer Implementation	14
4	SCC Hardware Configuration	16
5	Network Interface Processor	19
6	Design Detail of Network Interface Processor	21
7	Redundancy Techniques	25

#### SECTION 1

#### INTRODUCTION

The transition of the terrestrial Defense Communications System (DCS) from analog to digital transmission has required revisions in the concepts for operation, maintenance and control. The new concepts are being developed under a variety of programs. A common feature of the subsystems being developed by these programs is the distribution of automated data collection and processing throughout the DCS. Each subsystem requires a communications network to interconnect its elements. In addition, some subsystems will need to exchange information with other subsystems.

The radio service channel has traditionally been used to provide the communications network needed for operations and maintenance support. An analog service channel can easily be configured to provide a voice orderwire and a low capacity data network. A digital service channel is more difficult to configure into an effective network.

Concurrent with the transition to digital transmission, the DCS has instituted a policy of minimizing the number of technical personnel required to operate and maintain the system. Many sites will be unattended, or attended for a limited time. The Transmission Monitoring and Control (TRAMCON) System will be the critical source of information concerning the equipment operation at the unattended sites. That system, and its communications network, must be highly survivable to ensure the continuous operation of the DCS transmission system.

This report presents a hardware design concept for a service channel controller. The concept is based on statistical multiplexing techniques for a communications processor. A service channel controller would be located at each DCS transmission site to provide a survivable, distributed communications network.

The service channel controller will require software development. That development is not explicitly discussed in this report. However, the hardware concept, which is presented herein, does presume certain features of the software. Those features will be described briefly.

System concepts and DCS requirements are discussed in Section 2. The design concept is presented in Section 3. Section 4 compares the cost of implementing the service channel controller network with the cost of a network implemented with conventional multiplexers and bridges. A recommendation to develop the service channel controller is presented in Section 5.

6

#### SECTION 2

#### SYSTEM CONCEPTS

The communications requirements for DCS operations, maintenance and control subsystems are frequently separated, physically and functionally, into several categories. TRAMCON is a representative subsystem that separates communications into the following categories:

- o Polling of remote station unit
- o Inter-processor (master) communications
- o Remote maintenance terminals
- System control coordination

If separate channels were to be used between each pair of communicating terminals, the number of channels required would proliferate beyond any reasonable bound. Even when the subsystem communications networks are organized as regional multi-drop systems, the necessary communications channels can exceed the capacity of the service channel if conventional multiplexers are used. Some of the subsystems currently being planned will have to use mission channels, rather than the service channel, to configure communications networks.

A basic assumption used in this study is that the service channel should carry all of the communications for operations, maintenance and control. The DRAMA (Digital Radio and Multiplex Acquisition) Radio's 192 kb/s service channel certainly has sufficient capacity to support the anticipated requirements. However, conventional multiplexing techniques cannot guarantee access to the service channel for the numerous terminals of the multiple subsystems. The service channel controller, described herein, can grant the necessary access.

The number of stations in the digital DCS will rapidly change over the coming years. The digital segments of the European DCS, contained in the implementation plans as of August 1981, are used as a baseline for this design and analysis of the service channel network. The distribution of the number of radio links for these stations is shown in Appendix A.2. The implementation schedule for these segments extends through 1989. Revisions and additions will increase the number of sites and extend the schedule.

#### 2.1 DCS Requirements

Many of the subsystems that may use the service channel are still in the planning stage. A summary of those requirements is included in this report.

<u>Voice Orderwire</u> - Each DCS site requires a voice orderwire terminal. The voice terminal must be able to communicate with all DCS sites within a limited region. Each site is assigned a unique voice orderwire call number.

Data Terminals - Data terminals are grouped into subsystems. Each data terminal must communicate with some set of other terminals within its assigned subsystem. Some terminals may need to communicate with terminals within other subsystems. The maximum required data transmission speed of any subsystem presently identified is 2400 b/s. Most of the terminals will operate at some fixed standard speed between 150 and 1200 b/s. The electrical interfaces for those terminals correspond to either MIL-STD-188-100 or MIL-STD-188-114.

Radio Service Channel - The primary digital radios in the DCS will come from the DRAMA family of radios (AN/FRC-170 through 173). The DRAMA service channel operates at 192 kb/s for all radios in the family. The service channel controller must be able to operate at this speed while controlling the service channels for several radios. The service channel controller should be able to operate at any lower speed, to utilize other transmission resources that may be available. The electrical interface is synchronous.

<u>Availability</u> - The availability of the service channel communications network must be greater than the availability of the PCS transmission system.

<u>Reliability</u> - The reliability of the service channel communications network should exceed the reliability of the DCS transmission system and the subsystems using the network.

<u>Survivability</u> - The communications network should be at least as survivable as the DCS transmission system. Alternate routing over non-DCS circuits may be used to enhance that survivability.

<u>Flexibility</u> - The implementation of new subsystems that use the service channel should not require substantial alteration of the communications network.

<u>Maintainability</u> - The network should be easy to maintain. Special test equipment or special training for personnel should not be required.

## 2.2 Hardware Concepts

The concept for the service channel controller is a single hardware item that will satisfy all DCS requirements. The concept is illustrated in Figure 1. The service channel controller interfaces several digital service channels on the network side and several different terminals on the user side. All of the processing necessary for a terminal to communicate with another terminal, most likely at another site, is performed within the controller.

Any of a variety of technologies could be used to implement the service channel controller. The technology selected for presentation in this report is based on statistical multiplexing. To provide a comparison, an implementation using fixed multiplexing is also discussed.

Statistical multiplexing refers to techniques for allocating the capacity of a communications channel to a terminal based on demand. The channel is utilized only when a message is being transmitted. Information from a terminal is assembled into a message packet, with framing and header data appended. When the channel is available, the packet is transmitted. The receiver strips off the framing and header, disassembles the packet, and passes the information to a terminal.

Many implementations are possible for framing of statistical multiplexers; however, most commercial implementations use CCITT Recommendation X.25/LAPB (link access procedures, balanced). The LAPB frame consists of:

|flag|address|link control|logical channel number
|packet control|information|frame check sequence|flag|

The flag (binary 0111110) is a special symbol that is used to start and end a packet. Bit stuffing techniques are used to prevent the occurrence of a flag pattern within a packet. The address identifies the multiplexer. The link control word identifies the type of packet and maintains an orderly flow of information packets. Special control packets are used for initialization, acknowledgment and error recovery. The logical channel number identifies the terminal. The packet control word is used to establish the initial connection between terminals. The frame check sequence is a



Land and the second

i

-----

Figure 1. SERVICE CHANNEL CONTROLLER

10

IA-65 917

checksum that is used for error detection. When the ending flag is received, the frame check sequence is tested to determine if an error has occurred. Errors are corrected by retransmission.

The flags, address, link control word, and frame check sequence, along with the special control packets, are classed as level two protocol. The logical channel number and packet control word are classed as level three protocol.

The simple statistical multiplexer has only one trunk port which transmits and receives multiplexed data; it may have many terminal ports. A more complex multiplexer could have several trunk ports. If a packet that is received on one trunk port can be transmitted on another trunk port, the multiplexer is called "switching." A switching statistical multiplexer does not necessarily have terminal ports; all of the ports may be trunk ports. Many commercial systems use separate modules for supporting; terminals and trunks.

A system of switching statistical multiplexers, with the trunk ports interconnected through communications channels, does not necessarily constitute a communications network. Virtual circuits must be established between pairs of terminals before communication is possible. The mechanism for establishing the virtual circuits may be static or dynamic. Static implies a manual operation to establish each virtual circuit; dynamic implies a control function associated with each multiplexer that establishes virtual circuits.

At the basic level, a packet switch is a switching statistical multiplexer with a control function. However, packet switches contain many features not present in the basic switching statistical multiplexers. Few of these additional features would be useful in the DRAMA service channel network.

The statistical multiplexing concept for a service channel controller is illustrated in Figure 2. The service channel controller consists of three functional modules. The number of physical modules can be greater or less. A statistical multiplexer module interfaces with the user terminals. It multiplexes the separate data streams into one composite stream and demultiplexes a composite stream into separate user terminal data streams. The switching statistical multiplexer module accepts composite data streams from the radio service channels and from the statistical multiplexer module, and transmits the data for each terminal over the appropriate link specified for the virtual circuit of the message. The controller module establishes the virtual circuits



Figure 2. STATISTICAL MULTIPLEXER CONCEPT

IA-65 914

i

between terminals and supervises the operation of the other modules. The supervision function includes error recovery procedures and collection of performance statistics.

A typical fixed multiplexer implementation is illustrated in Figure 3 for the AN/FCC-100 multiplexer with digital bridging equipment. An implementation using the three-channel version of the AN/FCC-98 would be identical, except for the number of channels. The AN/FCC-98 is limited to three channels; the AN/FCC-100 can support up to 16 channels. Each radio link requires a separate multiplexer; each channel requires a digital bridge. Each user subsystem must either operate on a separate channel or use common data rates and protocols. The cost of implementing a service channel network using either the three-channel AN/FCC-98 or the AN/FCC-100 is derived in Appendix A for a baseline DCS consisting of 160 stations.

#### 2.3 Packet Switch Implementation

The statistical multiplexing functions are identical to the functions of a packet data switch. Since packet data switches are commercially available, it might appear feasible to implement the service channel controller with an existing packet switch. A survey of available packet switches was presented in Mini-Micro Systems magazine in March 1981. Of the nine switches available, only one, the BBN Pluribus, is capable of operating at the speed of the DRAMA service channel. The other packet switches would require a multiplexer (such as the AN/FCC-100) for each radio service channel. A data sheet describing the BBN C/30 packet switch processor is provided in Appendix B.1. The C/30 operates at a maximum trunk speed of 56 kb/s, typical of other commercial packet switches. The BBN Pluribus packet switch processor operates at any trunk speed up to 230 kb/s. Hence, a DRAMA service channel network could be configured using the Pluribus packet switch processor. The cost, however, appears to be prohibitive. When configured as a service channel controller, with redundant modules for reliability, the Pluribus would cost between \$220,000 and \$250,000 for each station. A data sheet describing the BBN Pluribus is provided in Appendix B.2.



#### SECTION 3

#### SERVICE CHANNEL CONTROLLER

The service channel controller is the heart of an envisioned service channel communications network. The basic concept is to use a single hardware unit to interface several users to the DRAMA radio service channels. At any DCS site, the maximum number of identifiable users is less than ten. The design goal is for a service channel controller to accept sixteen users.

The distribution of the number of radio links is provided in Appendix Table A.2. Only two sites have more than six links. The design goal is to support six radio service channels with a single service channel controller. The two DCS sites with more than six radios would each have two service channel controllers.

This section contains a hardware architecture for a service channel controller that, with the exception of one special module, is implemented with commercial hardware. A design of the critical elements of that additional module is presented.

#### 3.1 Hardware Architecture

The basic hardware configuration of the service channel controller is shown in Figure 4. This configuration is a physical implementation of the statistical multiplexer concept that was illustrated in Figure 2. The terminal interface processor is a statistical multiplexer; the network interface processor is a switching statistical multiplexer. The control processor is a controller. Each processor has a private memory area. The system memory can be accessed by all processors.

This architecture is based on the XYCOM 180+ family of industrial control processors. Descriptions of the XYCOM modules are contained in Appendix B. The 1842+ processor has four programmable USART (universal synchronous/asynchronous receiver/ transmitter) ports. Each port can operate asynchronously, at speeds up to 19.2 kb/s, or synchronously, at speeds up to 500 kb/s. However, the speed of its internal Zilog Z80 processor limits the 1842+ to an aggregate speed of less than 32 kb/s, when operated full duplex. The private memory space of the 1842+ contains 8 kbytes of read only memory (ROM) and 8 kbytes of random access memory (RAM). Since the 1842+ supports only four terminals, the terminal interface processor consists of up to four 1842+ modules. Each 1842+ operates independently. The 1862+ is identical to the 1842+, except that two



Figure 4. SCC HARDWARE CONFIGURATION (USING XYCOM MODULES)

•

Ť

- -----

, 1

IA-65 913

والمستقلفة والمتحد والمحمد والمحمد والمتعادي والمحمد و

USART ports are replaced by an optional floating point arithmetic processor. The USART electrical interface operates at TTL signal levels. XYCOM level converter modules transform the TTL levels to the appropriate standard levels for data interfaces. The 1815+ system memory contains 64 kbytes of RAM memory. 1813+ or 1814+ memory modules could be used to provide a mixture of RAM and ROM in the system memory. The network interface processor requires the design of a new module, to achieve the speed of the DRAMA service channel.

Messages arriving at the network interface processor from a radio serivce channel port are routed to the appropriate location. Data messages addressed to users at this site are transferred to the system memory; control flags are passed to appropriate terminal interface processors. Messages addressed to other users are transmitted on other radio service channels. Level two supervisory messages are processed within the network interface processor. Level three supervisory messages are routed to the control processor. Level three messages include call setup and flow control.

The terminal interface processor assembles messages into packets, and disassembles packets into messages. The packet length is variable, but the available memory precludes very long packets. A maximum length of 128 information bytes is imposed by the hardware design. Protocols appropriate to the individual terminals are supported. A parallel user interface (IEEE-488) could be supported by using a XYCOM 1843+ module as one of the terminal interface processors.

#### 3.2 Network Interface Processor

The design of a new module is required for the implementation of the network interface processor. The design shown in this report utilizes two critical elements: The XYCOM 1842+ (or 1862+) processor and the Western Digital WD2511 Packet Interface processor. Modules functionally equivalent to the 1842+ can be procured or fabricated from other sources. The WD2511, however, is unique and still not readily available. If Western Digital should withdraw the WD2511 from production, the design presented herein would be unworkable. A redesign using available technology would be very difficult. Vendor literature for these items is included in Appendix B. A simplified block diagram of the network interface processor is shown in Figure 5. The design uses the CPU, external bus buffer, memory (8 kbytes RAM and 8 kbytes ROM), and counter/timer blocks of an 1842+ processor module. The USARTs on the 1842+ are removed and functionally replaced by a module containing the WD2511s, packet memory, bus separator, and priority controller. Fabrication of the network interface processor module would require two or three circuit boards of the same size as the XYCOM modules.

The WD2511 packet interface processor uses CCITT Recommendation X.25/LAPB for the transmission link protocol. This protocol is implemented entirely within the WD2511 integrated circuit. The WD2511 also contains a memory management system that permits reception and transmission of packets without intervention by the CPU (after initialization). The packets are transferred between each WD2511 and buffers in the packet memory under DMA control. Each WD2511 can have eight receive and eight transmit buffers. The priority controller and the bus separator grant a WD2511, or the CPU, access to the packet memory. Also, they can grant CPU access to a WD2511 for initialization. Separation of the buses permits uninterrupted processing by the CPU until an access of the packet memory by the CPU is necessary.

The hardware implementation of the priority controller and the bus separator is much more complex than would be inferred from the block diagram. A design detail of the new parts for the network interface processor is shown in Figure 6. The parts derived from the XYCOM 1842+ module are not shown. The design is not complete; several minor modifications must be made to the 1842+ to permit interconnection with this part of the design.

Integrated circuits U1 through U6 are the WD2511 packet interface processors. U7 through U19, and U21 through U34, constitute the bus separator. Each WD2511 has a unique bus separator, both for access to the packet memory and for access from the CPU. Integrated circuits U35 through U42 constitute the packet memory. All of the other integrated circuits can be considered parts of the priority controller.

The priority controller operates by sequencing through service requests from the WD2511s and the CPU at an 8 MHz rate. U45 decodes requests from the WD2511s to write into the packet memory; U46 decodes requests to read from the packet memory. U57A decodes the CPU requests for access to the packet memory. U49 acknowledges the memory requests; U47 enables the bus separator circuits. U48 decodes the memory address and enables one of the memory circuits.

SYSTEM BUS COUNTER EXTERNAL BUS BUFFER MEMORY 8K RAM 8K ROM CPU 280A DATA ADDRESS PRIORITY CONTROLLER BUS SEPARATOR PACKET MEMORY 16K RAM 120 ns DATA ADDRESS PACKET INTERFACE #6 WD2511 PACKET INTERFACE #5 WD2511 PACKET INTERFACE#3 WD2511 PACKET INTERFACE #4 WD2511 PACKET INTERFACE #2 WD2511 PACKET INTERFACE #1 WD2511 IA-65 912 STRO9 JENNAHS ENVICE CHANNEL PORTS

----



\_\_\_\_\_

.

19

1

---

U20 decodes the CPU requests for access to a WD2511. If the designated WD2511 is not ready for an access, U56, U58, U59, and U60 generate a wait signal to the CPU. While the CPU is accessing a WD2511, U43 will force the priority sequencer to skip that WD2511 for one cycle.

U51 through U55, plus the associated gates, form a timing chain that generates the read, write and chip access signals to the packet memory. The timing chain is optimized to minimize the time required to access memory. A WD2511 read from memory requires 625 nanoseconds; a WD2511 write to memory requires 375 nanoseconds; a CPU access (read or write) requires 500 nanoseconds.

The maximum time required to sequence through a read and a write operation for each device is 7.0 microseconds. With the service channel operating at 192 kb/s, a WD2511 will both receive and transmit a byte every 41.6 microseconds. At the beginning and end of a packet, an additional five bytes must be transferred from the packet memory to update the WD2511 memory management function. Since level two protocol bytes (LAPB) are not placed in the packet memory, the WD2511 has at most three byte times to complete this transfer. The worst case timing occurs if receive and transmit packets end for all WD2511s simultaneously. The time required to complete the transfers would be 70 microseconds. The available time is 125 microseconds.





ľ

6£



9\_\_\_\_

.....

•

#### 3.3 Redundancy Considerations

Availability, reliability and survivability are critical requirements for the service channel communications network. The service channel controller must be constructed to satisfy them. The requirements probably will dictate that redundant hardware be used.

Redundant hardware can be implemented either on a unit basis or on a modular basis. The two types of implementations are illustrated on Figure 7. Theoretically, modular redundancy has higher reliability than unit redundancy, but requires more complicated transfer switching hardware. Maintenance is easier with unit redundancy since a complete unit can be tested off-line without affecting the on-line unit. Unit redundancy is normally preferred, due to maintenance considerations.

Modular redundancy permits partial redundancy. Only the most critical modules would require redundant units. For example, redundant power supply and network interface processor modules may provide adequate availability for the service channel controller. Reliability, maintainability, and availability analyses would be necessary to select the final redundancy configuration for the service channel controller.

#### 3.4 Voice Transmission Considerations

The statistical multiplexing function of the terminal interface processor segments a continuous data stream into packets that are transmitted separately. Since each packet is subject to a statistical delay, the received packets cannot always be assembled into a continuous stream. This feature can sometimes produce unacceptable degradation in voice circuits. The traffic distribution on the service channel network permits the use of algorithms that should prevent excessive degradation of the voice orderwire.

The basic assumption is that voice traffic will represent a small number of virtual circuits at any instant in time. The routing algorithms will not establish more than two virtual voice circuits over any radio link. The voice orderwire is normally used to communicate with nearby sites only. It is assumed that the maximum span of a voice circuit will be ten radio links. The voice encoding is assumed to be 16 kb/s CVSD (Continuous Variable Slope Delta modulation). The digital voice data stream is converted into packets, whose lengths are 40 bytes, for transmission over the service channel network. Therefore, each packet contains 20 milliseconds of speech. With packet header information, the transmission time for a voice packet over one link is 2 milliseconds. The processing time required to switch a packet to a new link is about one millisecond. If the voice circuit were the only active circuit in the network, the delay would be 3 milliseconds per link or 30 milliseconds for a 10-link path. This is the minimum delay for one packet.

If the network is loaded with data users and two voice users per link, the delay can increase. The switching algorithm gives voice packets priority over data packets, but a voice packet will not abort a data packet that is being transmitted. The greatest delay occurs when two voice packets arrive, just as transmission of a data packet starts. The time required to transmit a data packet with a maximum length of 128 information bytes, plus 8 header bytes, is 5.7 milliseconds. The maximum delay for the second voice packet, including the transmission time for two voice packets, is 9.7 milliseconds per link or 97 milliseconds for 10 links. (Processing time is not included, since the processing overlaps the transmission of the previous packet.) Therefore, the maximum differential delay between two consecutive voice packets is 67 milliseconds for 10 links. Thus, if all voice data were delayed at least 67 milliseconds by the destination terminal interface processor, a continuous data stream could be maintained.

Transmission data errors can produce greater delays, since packets containing errors must be retransmitted over one link. The worst case estimates are 40 milliseconds for an error recovery and  $10^{-4}$  for a transmission bit error rate. With these assumptions, a packet traversing a 10-link path would have a 99 percent probability of experiencing errors on three or fewer links. This could increase the delay from 97 to 217 milliseconds for a 10-link path. The differential delay would be 187 milliseconds for consecutive packets.

The algorithm that is contemplated for the service channel controller would delay voice packets at the destination terminal interface processor for up to 200 milliseconds, to ensure a continuous data stream on the voice circuits. This delay is equivalent to the transmission delay over a single satellite link.



---

والمحافظة والمحافظ

å

---

Figure 7. REDUNDANCY TECHNIQUES

#### SECTION 4

#### COST COMPARISON

The costs of implementing the service channel network using fixed multiplexers are contained in Appendix A. The costs of implementing the network using the service channel controller are contained in Appendix C. The network implementation costs for the 160 stations in the DCS baseline are:

	Cost (\$ million)
8 Port SCC, Partially redundant	2.7
AN/FCC-100, Non-redundant	3.3
8 Port SCC, Fully redundant	4.2
16 Port SCC, Fully redundant	5.4
Dual AN/FCC-100	6.6 + ?

The dual AN/FCC-100 implementation requires a transfer switch and control logic that is not included in the cost figure.

#### SECTION 5

#### RECOMMENDATION

The conceptual design of the service channel controller indicates that a feasible unit can be developed. The implementation cost of a service channel network using the controller is comparable to the cost using conventional multiplexers. The logical approach to developing the service channel network is:

- o Develop a hardware unit using XYCOM modules.
- o Develop routing algorithms and software.
- o Implement the network in a test bed.
- o Procure an operational system.

## APPENDIX A

## DRAMA MULTIPLEXER IMPLEMENTATION DATA

		Page
A.1	DRAMA Equipment Cost	29
A.2	DCS Site Distribution	30
A.3	Station Service Channel Cost: Analog AN/FCC-98 Implementation	31
A.4	Station Service Channel Cost: Digital AN/FCC-98 Implementation	32
A.5	Station Service Channel Cost: AN/FCC-100 Implementation	33
A.6	Service Channel Network Cost	34

1215

(n) - 10 - 10

i mini

S. D. CARRIER

and the second se

ķ

à

# DRAMA Equipment Cost Service Channel Support

Equipment Type	Unit Cost (\$1000)
AN/FCC-98 (3 analog channels)	14.0
AN/FCC-98 (1 analog and 2 digital)	17.5
AN/FCC-100 (LSTDM)	7.3
Analog conference bridge	0.4
Digital conference bridge (mainframe)	0.3
Digital conference bridge (termination)	0.2
Modem	1.0

#### DCS Site Distribution

Station Size (links)	Number of Sites	Estimated Number of Data Terminals		
1	25	2		
2	88	2		
3	26	3		
4	11	3		
5	4	4		
6	4	5		
9	1	5		
10	1	5		

The data terminals include a digital voice terminal. The number at any site is variable. The numbers shown are based on a very limited implementation of assumed system control features beyond TRAMCON.

# Station Service Channel Cost Analog AN/FCC-98 Implementation

Station Size	Multiplexer		Bridge		Modem		(\$1000)
	Units	Cost (\$1000)	Units	Cost (\$1000)	Units	Cost (\$1000)	
1	1	14.0	2	0.8	2	2.0	16.8
2	2	28.0	3	1.2	2	2.0	31.2
3	3	42.0	3	1.2	3	3.0	46.2
4	4	56.0	6	2.4	3	3.0	61.4
5	5	70.0	6	2.4	4	4.0	76.4
6	6	84.0	6	2.4	5	5.0	91.4
9	9	126.0	9	3.6	5	5.0	134.6
10	10	140.0	9	3.6	5	5.0	148.6

The bridge and modem quantities are based on the number of radio links and number of terminals shown in Table A.2.

# Station Service Channel Cost Digital AN/FCC-98 Implementation

Station Size	Multiplexer		Analog Bridge		Digital <u>Bridge</u>		Station Cost (\$1000)
	Units	Cost (\$1000)	Units	Cost (\$1000)	Units	Cost (\$1000)	
1	1	17.5	1	.4	2	1.4	19.3
2	2	35.0	1	.4	2	1.8	37.2
3	3	52.5	1	.4	2	2.6	55.5
4	4	70.0	2	.8	2	3.0	73.8
5	5	87.5	2	.8	2	3.4	91.7
6	6	105.0	2	.8	2	4.2	110.0
9	9	157.5	3	1.2	2	5.4	164.4
10	10	175.0	3	1.2	2	5.8	182.0

The bridge and modem quantities are based on the number of radio links and number of terminals shown in Table A.2.
### Table A.5

### Station Service Channel Cost AN/FCC-100 Implementation

Station Size Mult:		tiplexer B		ridge	Station Cost (\$1000)
	Units	Cost (\$1000)	Units	Cost (\$1000)	
1	1	7.3	3	2.1	9.4
2	2	14.6	3	2.7	17.3
3	3	21.9	3	3.9	25.8
4	4	29.2	3	4.5	33.7
5	5	36.5	3	5.1	41.6
6	6	43.8	3	5.7	49.5
9	9	65.7	3	7.5	73.2
10	10	73.0	3	8.1	81.1

The bridge and modem quantities are based on the number of radio links and number of terminals shown in Table A.2.

33

### Table A.6

### Service Channel Network Cost Multiplexer Implementations (\$1000)

			plementation	Technology
Station Size	Stations	Analog	Digital	16 Channel
1	25	420.0	482.5	235.0
2	88	2745.6	3273.6	1522.4
3	26	1201.2	1443.0	670.8
4	11	675.4	811.8	370.7
5	4	305.6	366.8	166.4
6	4	365.6	440.0	198.0
9	1	134.6	164.4	73.2
10	1	148.6	182.0	81.1
Tot	al	5996.6	7164.1	3317.6

#### APPENDIX B

#### HARDWARE DATA SHEETS

This appendix contains manufacturers' data sheets for hardware that may be used in configuring the service channel controller. The data sheets are:

	P	a	g	е
--	---	---	---	---

B.1	BBN C/30 Packet Switch Processor	36
B.2	BBN Pluribus Packet Switch Processor	38
B.3	XYCOM 1813+ Memory Module	40
B.4	XYCOM 1842+ Communications Controller	44
B.5	XYCOM 1843+ IEEE-488 Bus Controller	50
B.6	XYCOM 1862+ Microcomputer Module	56
B.7	XYCOM 1891+ Breadboard Kit	62
B.8	XYCOM 180+ Chassis/Power Supply	66
B.9	XYCOM 980X Communications Adaptors	70
B.10	XYCOM 9680 Communications Adaptor Rack	76
B.11	Western Digital WD2511 Packet Network Interface	80

B.1 and B.2 describe commercial packet switch processors that could be used as service channel controllers. B.3 through B.10 are industrial processor modules that could be configured into a packet switch processor. B.11 would be used to modify B.4, to achieve the speed of the DRAMA service channel.

### **BBN Computer**

### C/30 Packet Switch Processor

#### Features

- 130 packets/second full duplax communication line throughput
- Plus 200 packets/second full duplex host computer throughput
- ARPANET network technology
- 135 ns powerful microprogrammable architecture
- Supports up to 6 X.21, X.21 (bis), BI-Sync or ARPANET Sync Ports
- Also supports up to 4 1822/ARPANET Host Ports
- Also supports up to 64 Medium-speed Async/Sync Terminals
- Self-configuring on start-up



Summary	The C/30 packet switch processor was designed specifically for high-speed communications environ- ments. A very fast, powerful, microprogrammed CPU architecture provides raw speed and basic com- munication instruction sets.			
	Much of the complicated I-0 logic is performed by the central microprocessor which both reduces I-0 component count by a factor of 3 or 4 and allows one basic I-0 device to be microcode configured as many different devices. For example, the basic serial communications-line device can handle Asyn- chronous devices from 50 to 19,200 baud, with or without moderm control, Synchronous, or Binary Synchronous devices up to 56 kbaud, all by simply changing microcode.			
	J-0 devices are supplied with several microcode routines to allow them to handle a variety of devices. A basic micro-assembler and micro-loader are available as well.			
	Optionally, the C/30 is supplied with the ARPANET Interface Message Processor software, or the ARPANET Terminal Interface Processor software. Tens of man-years have been invested in this code to allow it to operate the world's biggest packet switch network.			
Central Processor	The C/30 CPU is based around a fast microprogrammed CPU with an instruction set designed for communications environments. The basic elements are a 1k x 20-bit register file, a 512 x 32-bit microcode ROM containing the loader, debugger and console logic, and a microcode memory in sizes of 2k, 4k or 8k x 32 bit which contains the macro-instruction set and I-0 emulation. Microcode has the ability to run in either the 16-bit or 20-bit mode at the macro-instruction level. Microcode memory is loaded from a microcasette holding up to 100kb.			
	The BASIC C/30 also includes 2 serial async H0 ports, (one for the console terminal, the other for the micro-cassette loader), a 4-slot chassis with battery backup power supply, and 32k words of 20-bit 405ns semiconductor memory. An Error Detection and Correction system is also standard.			
	An EXPANDED C/30 provides an 8-slot chassis and larger power supply system.			
	C/30 systems are provided with microcoded emulation of a minicomputer's instruction set, providing simple access to ARPANET packet switch network software.			
1.O System	The I-D system is greatly simplified compared to most current minicomputers. Most C/30 I-D devices consist of only voltage conversion devices, serial to parallel conversion, and a variably sized FIFO (first- in, first-out) buffer. All complicated logic is performed in the CPU			
	This approach produces low-cost I-0 devices because very little hardware is actually used, and one hardware design can function as many different devices by changing microcode			
	For example, a single design of serial communications port can support any kind of Asynchronous Device, with speeds from 50 baud to 19,200 baud, Synchronous Device, or Binary Synchronous Device with speeds to 56k baud. Different microcode is required, but this is kept in RAM memory (baded from microcassette) and allows the system's OEM to use a very small number of interface designs for a very large number of different applications.			
	Most C/30 I/0 devices use small daughter boards to customize the voltage conversion for different line disciplines, for example, RS-232, Bell 303, RS-422, MIL-188-114, etc			

PN 153-3

## C/30 Packet Switch Processor

## **BBN Computer**

Memory	The C/30 includes the 32kw of 20-bit memory Additional memory is available in sizes of 32kw. Ail memory is RAM, 105ns access time. Maximum memory is 128k words. Error Detection and Correction (EDAC) is standard. This provides 6 additional bits of checking, allowing detection of all single- and double-bit failures.			
	C/30 Memory is currently based on 16k memory	iCs .		
Communications	The C/30 has four basic communication I-0 desig			
I-O Devices	<ul> <li>Medium-speed Async/Sync Interfaces</li> </ul>	<ul> <li>High-speed HDLC/SDLC Interfaces</li> </ul>		
	<ul> <li>High-speed Async/Sync Interfaces</li> </ul>	<ul> <li>High-speed 1822/ARPANET Interfaces</li> </ul>		
	Each design has a number of daughter-boards, w associated microcode to handle the interface for	hich provide voltage conversion as required and a specific line protocol		
	The following currently exist			
	<ul> <li>For Async Interface Design</li> </ul>			
	- 20-ma current loop			
	<ul> <li>EIA interfacing to terminals (modem control not included)</li> </ul>	<ul> <li>EIA interfacing to modems (modem control included)</li> </ul>		
	All of the above can handle devices at spee 4800, 9600, 19,200 baud. Full duplex, half di and 2 stop bits, even/odd/none/marking par	ds of 50, 75, 110, 134.5, 300, 600, 900, 1200, 2400, uplex, 5/6/7/8 bit data bytes, 1, 1,1,2 ity are all supported		
	The microcode supplied includes the ability to support auto-speed detection. IBM 2741 terminais can also be supported.			
	For High-speed Async/Sync Design			
	- Bell 303 modern support	- Mil-188-114 support		
	<ul> <li>RS-232C modern support</li> </ul>	- V 28 support		
	<ul> <li>RS-422/423 modern support</li> </ul>			
	<ul> <li>For High-speed HDLC/SDLC         <ul> <li>X 21 support</li> </ul> </li> </ul>			
	Eor 1822/Arpanet			
	- Local 1822 Host support	- Very Distant Host (VDH) support (same as		
	- Distant 1822 Host support	Bell 303)		
	The various communication line designs are availations	able on 14x18 logic cards in a variety of combina-		
	5401 4 1822 Ports, 6 High-speed Async/Sync 5410 32 Async Ports, 1 1822 Port, 1 Sync/SDLC/HDLC Port			
	For complete details, refer to the price list			
Other I-O Devices	Also available is a disk controller designed to handle up to 2 Storage Module Disk (SMD) drives. Man- manufacturers offer a variety of disk drives that interface to the SMD bus			
Power	The BASIC C/30 requires 300 watts of power, which can be supplied at 115v or 230v. or 50 or 60 Hz			
Physical Construction	The BASIC C/30 fits in a standard 19-inch-wide rack and uses 12.5 inches of vertical space (20 inches deep)			
	The microcassette occupies $3^{5}2$ inches of vertical space (12 inches deep). Most communication 1-0 boards include connector panels that use $3^{5}2$ inches of vertical space in the rear of the cabinet normally behind the microcassette.			
	The EXPANDED C/30 requires 173/4 inches of vertical space. All other dimensions are the same			
Environmental Operating 2°C to 32°C. humidity 0-90% (noncondensing) Storage -15°C to 65°C, humidity 0-98% (noncondensing), alt: 0-7000 ft				

BBN Computer Corporation 33 Moulton Street Cambridge, Massachusetts 02238 (617) 491-1850 Ext.3765

## **BBN** Computer

### **PLURIBUS Packet Switch Processor**

#### Features

- 900 packets/second full duplex host computer throughput
- 750 packets/second full duplex communications line throughput
- ARPANET network technology
- Supports up to 16 trunk lines
- Supports up to 20 1822/ARPANET host ports
- Supports up to 420 medium-speed async/sync terminals
- 2 to 14 CPUs

قدمه والانتقاد ومحافظ والاسترام والمراكل

20.0

Å

- Self-configuring on start-up
- Can be configured for hot-standby operation



Summary	The Pluribus Processor is a fault-folerant multi-processor designed to operate as a highly reliable, high- speed packet switch processor. Multiple I-0/memory busses and processor busses allow the use of redundant resources and provide physical and electrical isolation of functional units. Critical I-0 devices can be dualported to different I-0 busses in a hot standby configuration.		
	The PLURIBUS software does load-sharing on a dynamically assigned job basis, and can handle very large throughputs, as much as 1.8 megabits/second of store and forward throughput. All processors are equal, so any processor can run any code module and access all of the global memory in a system. The PLURIBUS system provides for smooth system upgrading. Increasing the number of pro- cessors and the memory size can result in substantial throughput increases.		
	Approximately 30 PLURIBUS systems are installed as packet switching processors in various net- works. Many of them include terminal concentrator hardware and software. The largest PLURIBUS system contains 8 CPUs and handles 420 terminals and 20 hosts.		
	Optionally, a PLURIBUS system is supplied with the ARPANET Interface Message Processor (IMP) software or the ARPANET Terminal interface Processor (TIP) software. Tens of man-years have been invested in this code, which operates the world's largest packet switch network.		
System Architecture	Memory is located both on processor busses, where it is local to the processors on the bus, and on I-0/memory busses, where it is globally addressed. The maximum amount of global memory is 1 megabyte. Global memory is used for all buffers and for infrequently used routines. This memory is distributed over the available non-CPU busses in equal amounts.		
	I-0 interfaces, in a Pluribus configured for fault-tolerant operation, are typically duplicated and con- nected to different I-0 busses. Only one of the two interfaces services the device or line at a time. The PLURIBUS switches between I-0 interfaces using tri-state logic.		
	The PLURIBUS achieves load-sharing by maintaining a hardware interrupt register which defines the code modules needing service. All modules are designed for a maximum run-time of 2 milliseconds before they must check the interrupt system for a higher priority module. Before checking the interrupt system a module may post itself as a module needing service. This establishes an average maximum time a task will have to wait for servicing and ensures that each processor is as busy as possible.		
Softwarg	In a PLURIBUS, two processors and local memory are normally placed on one bus. This functional unit holds the basic operating software kernel called STAGE. STAGE dynamically determines the hard- ware configuration present, agrees on it with all the other processors configures the device tables, and begins executing the IMP software. STAGE always runs periodically to ensure that the con- figuration has not changed.		
	The IMP software has many features which no other system can offer. Network failures are detected automatically and network performance is not affected by the failure of any single network element. Changes in the network configuration are detected automatically and are immediately incorporated into the network databases. Sophisticated flow control and positive acknowledgment ensure that data are sent correctly.		
	The TIP software has all of the features of the IMP plus a virtual host process which controls the ter- minals. The TIP software allows a user to access network facilities without using a host computer.		

PN 154-1

## **PLURIBUS Packet Switch Processor**

والمتحد والمتحرين والمتلك فالمتحد والمتحد والمتحد والمحالي والمحالي والمحالي والمحالي والمحالي والمحالي والمحال

i

### **BBN Computer**

Reliability	A bus may be powered off or a device on the bus may fail in such a way as to disable the bus. When this happens the IMP may shut down for 20 to 30 seconds while STAGE reconfigures the system, then the Node is restarted if necessary and error messages are sent to the Network Monitoring Center (NMC). When a failure occurs the NMC is automatically informed of the apparent cause and can down-line load diagnostics to further isolate the problem before dispatching field service technicians. Similarly, when a b is or device becomes operable again, STAGE discovers this event and reconfigures the system to include the repaired component. When an I-0 device failure is detected. STAGE will cause the alternate device to be used, usually with no impairment of throughput or efficiency. When STAGE detects a processor rule essitem throughput do exclude that resource. The loss of a processor may reduce the system throughput, depending upon the load. The loss of global memory will reduce buffer space and thus may reduce throughput under heavy load. A fault-tolerant system can be configured with sufficient memory and processing power that failures rarely affect performance. Code modules and data structures are constantly verified by STAGE and the IMP software. Redundant information is built into the data structures and code modules. The redundant information is built into the data structures and code modules and stack overflows. Timeouts are used to detect dead processes residure locks which were never unlocked, and data structure entries which should have been updated.			
Communications	The PLURIBUS has four basic communication	ns I-0 designs		
I-O Devices	<ul> <li>Medium-speed async interfaces</li> </ul>			
	<ul> <li>High-speed sync interfaces</li> </ul>			
	<ul> <li>Medium-speed HDLC Interfaces</li> </ul>			
	<ul> <li>High-speed 1822/ARPANET interfaces</li> </ul>			
	The following communications support curren	ity exists		
	<ul> <li>For medium-speed async interface design</li> </ul>	.,		
	- 20-ms current loop			
	- EIA interfacing to terminals			
	<ul> <li>EIA interfacing to modems</li> </ul>			
	Ali of the above can handle devices at s 2400, 4800, 9600 baud. Full duplex half even/odd/none/mark parity are all suppo	peeds of 50, 75, 110, 134,5, 300, 600, 900, 1200 duplex, 5/6/7/8 bit data bytes, 1, 112, and 2 stop bits orted		
	The software supplied includes the ability	y to support auto-speed detection		
	For high-speed sync design			
	- Bell 303 modern support	- V/35 modern support		
	<ul> <li>RS-232C modem support</li> <li>MIL-188-114 support</li> </ul>	- RS-422/423 modern support		
	For medium-speed HDLC			
	- X21 support	<ul> <li>X 21 (bisync) support</li> </ul>		
	For 1822/ARPANET			
	- Local 1822 Host support	- Very Distant Host (VDH) support		
	Distant 1822 Host support	(same as Bell 303)		
	The basic configuration for a communications device is 1-line per device with the exception of the following			
	<ul> <li>The medium speed HDLC unit handles 4 lines at 9.6 KB or 1 line at 40 KB</li> <li>The medium-speed async unit handles 63 lines</li> </ul>			
	For complete details, refer to the price list			
Power	A typical 1 rack PLURIBUS system with 4 busses requires 2000-2400 watts of power which be supplied at 115 V and 50 or 60 Hz. A PLURIBUS system includes battery power sufficien power the complete memory system for 60 minutes during power transients or short outages			
Physical Construction	The PLURIBUS system is delivered with 1 or more 19-in x 61-in racks (inside measurements). The exact number of racks necessary depends on the size of the system.			
Environmental Operating 2°C to 30°C, humidity 0-90% (noncondensing) Storage -15°C to 65°C, humidity 0-98% (noncondensing) Alt, 0-7000 ft				

BBN Computer Corporation 33 Moulton Street Cambridge, Massachusetts 02238 (617) 491-1850 Ext. 3765



## 1813+ BANKSWITCHED EPROM/STATIC RAM MEMORY

#### FUNCTION

The 1813+ bankswitched memory module supports a variety of userinstalled, byte-wide, single +5 Vdc supply EPROM devices. In addition, the 1813+ can optionally support factory-installed 450ns static NMOS RAM.

#### FEATURES

- o Four (4) 16Kb blocks of software bank switchable memory
- Optionally available one (1) 16Kb block NMOS static RAM
- o 64Kb total memory capacity o Independent assignment of each bank base address
- o Multiple banks can occupy the same direct address space
- o Banks can be selected/deselected under software control
- o Memory write protection, enabled/disabled through switch or software control
- Powerup configuration separately selectable from run-time configuration



#### DESCRIPTION

The 1813+ is a high-density memory module which supports EPROM and, optionally, RAM resources for any XYCOM 180+ microcomputer system. Memory is divided into segments called banks, and bankswitching capability allows a bank to be exclusively selected for data read/write operations. Each bank contains up to 16Kb of memory, and the base address of each bank can be independently set to any 16Kb boundary.

#### BLOCK DIAGRAM DESCRIPTION

#### MEMORY CONFIGURATION

The 1813+ module is equipped with 16 sockets to accommodate user-installed EPROM, and a variety of memory devices can be employed. Depending on the density of EPROM devices employed, differing numbers must be installed to fully configure 16Kb banks. Banks are numbered 0, 1, 2, and 3, and permissible configurations are shown below:

Memory Device	Bytes/ <u>Device</u>	Devices/ 16K Bank	Total EPROM Bytes/ Module
TMS 2516 EPROM	2КЬ	8	32КЪ
Intel 2716 EPROM	2КЬ	8	32КЪ
Intel 2316E PROM	2КЬ	8	32КЬ
TMS 2532 EPROM	4КЬ	4	48Kb
Intel 2732 EPROM	4Kb	4	48Kb
TMS 2564 EPROM	8Kb	2	48Kb
Intel 2764 EPROM	8Kb	2	48Kb

i



Note that 2516, 2316E, and 2716 devices can be intermixed in a module, while the higherdensity devices cannot. In addition, only two EPROM banks (Nos. 0 and 2) are employed when 2Kb devices are installed. A bank always occupies 16Kb of address space even if populated with less than 16Kb memory, and the total number of addressable memory locations is 64Kb.

#### **RAM OPTIONS**

One optional version of the 1813+ module is available in which bank No. 3 contains factoryinstalled 450ns static NMOS RAM. It provides 16Kb RAM. The RAM option limits the amount of EPROM which can be installed using 4Kb or 8Kb EPROM devices to 48Kb.

#### ADDRESSING

The base address of each bank can be independently set to any 16Kb boundary (0000H, 4000H, 8000H, C000H) with user-installed jumpers.

#### BANKSWITCHING

Default bank selection is accomplished according to user-installed jumpers. After system initialization, banks can be selected through software control using the 1813+'s control register, which can also be read to determine which bank is currently selected. Bankswitching capability allows system memory capacity to be extended beyond system address capacity by permitting alternate selection of multiple memory banks which occupy the same direct address space.

#### MEMORY WRITE PROTECTION

The 1813+ includes a memory write protect feature. When enabled, it prevents data from being written into RAM. Memory write protect can be enabled/disabled through software control using the 1813+'s control register. The control register can also be read to determine if memory is write protected or not. A userinstalled jumper determines whether memory write protect is enabled or disabled on powerup. In addition, a switch mounted at the front edge of the 1813+ allows assignment of master write protection to all RAM on the module.

#### CONTROL REGISTER OPERATION

As previously mentioned, software control of bank selection and enabling/disabling of memory write protect are accomplished by writing a control byte to the module's control register, which is located at I/O address FF(Slot Code)0H. Writing a logic 1 to a bit position of

the control register enables the module characteristic associated with that bit position. Writing a logic 0 disables the characteristic.

#### JUMPER FEATURES

- Density of byte-wide EPROM devices installed (2Kb, 4Kb, or 8Kb)
- Type of EPROM devices installed o
- Assignment of bank No. 3 to EPROM or RAM
- Whether RAM draws +5 VDC from the 0 backplane LOG supply line only or from both the backplane LOG and MEM supply lines
- Base address of each memory bank ο
- Memory write protect default state Default memory bank selection
- 0
- Whether or not memory control is allowed 0 through the control register

#### MODULE SPECIFICATIONS

Power Required (Max.): +5VDC @ 3A (16Kb RAM) +5VDC @ 1A

#### FAMILY SPECIFICATIONS

- TEMPERATURE Operating: 0° to 65°C (32° to 149°F) Non-Operating: -40° to 85°C (-40° to 185°F)
- HUMIDITY 0 0 to 100% RH Non-condensing (Note, extreme low humidity conditions may require special protection against static discharge.)
- ALTITUDE

Operating: Sea level to 20,000 ft. (6096 m) Non-Operating: Sea level to 50,000 ft. (15240 m)

**VIBRATION** 

0.1 in (2.5 mm) pp,	i0 to 30 Hz
5.0 g,	30 to 500 Hz
0.036 in (.9 mm) pp,	50 Hz
0.024 in (.6 mm) pp.	60 Hz

- PHYSICAL SPECIFICATIONS Standard Board Envelope 8.5"H x 10.5"L x 0.6"Profile (21.6 cm x 26.7 cm x 1.5 cm)
- o AMBIENT ATMOSPHERE The design, fabrication, and protective sealant procedures used are consistent with those of the petro-chemical and

other contaminated-atmosphere manufacturing environments. Specifically, 180+ modules have a significantly increased chemical resistance to:

Hot water vapor Hydraulic oil Lubricating oil VM and P Naphtha Trichloroethylene Carbon Tetrachloride Fungus Oxidation

and a standard and a

i

Partial protection is provided against: Dilute Sulfuric acid mist Salt spray Gasoline Benzene, Toluene Xylene Ammonium Hydroxide

o SHOCK 30g, 11 ms, 1/2 sine

#### ORDERING INFORMATION

Number	Description
1813+	Bankswitched EPROM
1813+/16K	EPROM/16Kb Static RAM



PO Box 984 • Ann Arbor, Michigan 48106 • Phone (313) 429-4971 • TWX 810-223-8153



## 1842+ USER-PROGRAMMABLE INTELLIGENT SERIAL CONTROLLER

#### FUNCTION

The 1842+ is a user programmable intelligent communications module. The 1842+ can perform a variety of serial communication functions.

#### FEATURES

- o 4 MHz 280A CPU
- o 8Kb of private onboard RAM
- o Provides two (2) sockets for EPROM
- o Accepts 2716 (2Kb x 8 bit) or 2732 (4Kb x 8 bit) EPROMs
- o Direct Memory Access to all of system memory
- Can operate as a standalone processor or as either a master or slave processor in a multiprocessor system
- Four channels of serial communication capability provided by 280A SIO's
- o Full Modem control
- Support for Async, Byte Sync, or Bit Sync protocols
- o Programmable Async baud rates up to 9600 baud
- o Programmable Synchronous baud rates up to 500K baud
- o Supports bankswitched memory
- o Supports powerfail interrupts
- Provides a user programmable watch-dog timer to disable card, thus releasing the 180+ System bus in a multiprocessor environment



#### DESCRIPTION

The 1842+ is a self contained, 280A microprocessor based, serial communication controller module. The 1842+ has 8Kb of RAM memory and sockets for up to 8Kb EPROM. This memory is local to the 1842+ and is for exclusive use of the onboard 280A. The 280A, in addition to the on-board memory, is capable of directly accessing the system memory. There is also an 8 bit handshake port which can be used for communication between the 1842+ and other processors.

The 1842+ contains four independent channels of serial communication capability implemented with Z80A SIO's. Each channel can be individually configured for Asynchronous, byte-synchronous, or bit-synchronous operation at data rates up to 500K bits/second. Each channel features automatic control character insertion and deletion, software controlled baud rates, parity/ overrun/framing error detection, break detection and generation, and CRC generation and checking. The serial I/O signals of the module are TTY compatible. Separate level-shift modules are available to meet 20mA current loop, RS-232C, RS-422A, RS-423 and fiber optics specifications.



#### BLOCK DIAGRAM DESCRIPTION

The 1842+ contains a 280A microprocessor with a 16-bit program counter for direct addressing of up to 64K bytes of memory. There are two identical sets of general purpose registers, accumulators, and flag registers in the Z80A; a main register set, and an auxiliary set of registers. Either set of registers or accumulators and flags can be selected, at any time, by using one exchange command. This feature permits fast storage of registers needed for interrupt service routines or subroutine servicing. An external stack located within any portion of read/write memory may be used as a last-in, first-out buffer to restore the contents of the program counter, flags, accumulator, all six general purpose registers, and the auxiliary register set (accumulator, flags, and six general purpose registers). The CPU includes an 8-bit bidirectional data bus, 16-bit address bus, and 158 different instructions. These 158 instructions include all of the 8080A instructions.

Four independent full duplex serial channels provide serial communications

capability. Data rates up to 500K bits-persecond are software selectable on a per port basis; each port's receive and transmit clocks The receivers are are tied together. quadruple-buffered and the transmitters are dual-buffered. Some of the features of the serial ports are programmable sampling rates, parity/overrun/framing error detection, programmable CRC insertion/deletion plus break detection and generation. The SIO supports asynchronous, bit synchronous, and byte synchronous software protocols. Either an internal or external clock is jumper selectable for each port. Both serial input/ output ports are TTL compatible signals. Separate termination level shift modules and interconnect cable assemblies (communication adapters) are available to meet 20mA current loop, RS-232C, RS-422A, RS-423A, and Fiber Optic specifications.

The Counter-Timer Circuit (CTC), provides four independent channels of counting and timing functions.

The user can configure the 1842+ so that CTC channel 0 either generates a clock for SIO channel A or for both SIO channels (A and B). CTC Channel I can be used to generate a clock for SIO Channels A and B of the second SIO.

CTC channel 2 can be used to:

- a. generate a clock for SIO channel B or
- b. release the 180+ System Bus Latch, or
- c. release the 180+ System Bus Latch and generate a non-maskable interrupt to the 1842+'s processor or,
- d. release the 180+ System Bus Latch and generate a reset of the 1842+'s processor.

CTC channel 3 can be used to generate an interrupt from the backplane's interrupt request pin's signal (IREQ).

An alternative to the above options is to use any of the channels as a counter or timer. In either case, the 1842+'s processor can examine the state of the counter before the timer or clock reaches zero. When the timer or clock reaches zero it can interrupt the processor, if interrupts are enabled. The timer or clock will reload the time constant and repeat the count down process.

The standard 1842+ comes with IK bytes of RAM memory (450 nanosecond memory cycle 2114L RAM chips, with no wait states required).

The 1842+ can contain up to 8K bytes of non-volatile read only memory. Various types of EPROM/ROM chips may be inserted into the six sockets provided. Non-volatile read only memory may be added in 2K byte increments (up to 4K bytes), using TMS 2516 EPROMs, or Intel 2716 EPROMs; in 4K byte increments (up to 8K bytes), using TMS 2532 EPROMs.

The External Processor Interface provides the 1842+ with an eight (8) bit bidirectional hand shake port between the on board Z80A and other processor modules on the 180+ system bus.

The Interface with System Memory allows direct access, by the 1842+, to system memory.

Bankswitch and full memory mapping schemes are available and each is jumper controlled. Both memory mapping schemes allow the 1842+ to access all the 180+ memory and I/O space.

The full memory mapping scheme allows several memory mapping variations onboard; EPROM/ROM, RAM and system (off-board) memory under software control. Four software controlled configurations are available to the user. Memory Map 1 is initialized on a power-up condition.

	MAP I	MAP 2	MAP 3	MAP 4
FFFFH	180+			
	System	180+	180+	
	Memory	System	System	
4000H		Memory	Memory	180+
	Onboard			System
	RAM		1 1	Memory
2000H				
	Onboard	Onboard	Onboard	
	EPROM	EPROM	EPROM	i i
0000H				
	Power-up			
	Condition			

The bank switch memory mapping scheme allows the user to access half the 180+ address space at a time. The half of system memory being accessed is under software control.



The Bus Buffers circuitry provides the necessary buffering of Address and Data information between the 1842+ private bus and the 180+ system bus.

#### JUMPER FEATURES:

- o Master/Slave Select o EPROM Type Select o Global Memory Access -Bankswitch/Full Access
- o External/Internal Serial clocks o Watchdog Timer (Reset or NMI)

#### **PIN OUTS**

Serial Connector\*

Signal	Function
TD	Transmit Data from 1842+
RD	Receive Data to 1842+
тс	Transmit Data Clock (external)
RC	Receive Data Clock (external)
RTS	Request To Send Output
CTS	Clear To Send Input
DCD	Data Carrier Detect Input
DTR	Data Terminal Ready Output
SYNC	External Sync Input
GNE	Logic Ground

\* These signals are repeated four times

#### RESET CONNECTOR

RESET	1842+ Reset Input
GND	Logic Ground

#### CONNECTORS

(2 each) 50 pin ribbon socket

T&B/Ansley	#609-5000N
Winchester	#51-1150-00
AMP	#88379-8

#### 2 pin crimp ramp lock

*Molex	#09 50 3021
- MOIEX	#07-3021

\*requires flat crimp terminal

Molex	#08-50-0107 (chain)
or	
Molex	#08-50-0108 (loose)

#### MODULE SPECIFICATIONS

Serial Port

All input and output lines are TTL levels.

Power Required (Niax.)

+5VDC @ 3.0A

#### FAMILY SPECIFICATIONS

- o TEMPERATURE Operating: 0° to 65°C (32° to 149°F) Non-Operating: -40° to 85°C (-40° to 185°F)
- HUMIDITY
   to 100% RH Non-condensing
   (Note, extreme low humidity conditions may require special protection against static discharge.)
- ALTITUDE
   Operating: Sea level to 20,000 ft.
   (6096 m)
   Non-Operating: Sea level to 50,000 ft.
   (15240 m)
- v
   VIBRATION

   0.1 in (2.5 mm) pp,
   10 to 30 Hz

   5.0 g,
   30 to 500 Hz

   0.036 in (0.9 mm) pp,
   50 Hz

   0.024 in (0.6 mm) pp,
   60 Hz
- PHYSICAL SPECIFICATIONS Standard Board Envelope
   8.5"H x 10.5"L x 0.6"Profile
   (21.6 cm x 26.7 cm x 1.5 cm)

AMBIENT ATMOSPHERE
 The design, fabrication, and protective
 sealant procedures used are consistent
 with those of the petro-chemical and
 other contaminated-atmosphere manufac turing environments. Specifically, 180+
 modules have a significantly increased
 chemical resistance to:

Hot water vapor Hydraulic oil Lubricating oil VM and P Naphtha Trichloroethylene Carbon Tetrachloride Fungus Oxidation Partial protection is provided against: Dilute sulfuric acid mist Salt spray Gasoline Benzene, Toluene Xylene Ammonium Hydroxide

o SHOCK 30g, 11 ms, 1/2 sine

### ORDERING INFORMATION

Number

Description

1842+

والمتحافظ والمراجع والمحافظ

User Programmable Intelligent Serial Controller (4 Channels)



P.O. Box 984 • Ann Arbor, Michigan 48106 • Phone (313) 429-4971 • TWX 810-223-8153

5858 1847 4 8



#### FUNCTION

The 1843+ is an intelligent, user programmable module with a primary function of serving as an IEEE 488 GPIB Interface. In addition to the GPIB controller interfacing, the 1843+ has two serial communication channels to perform a variety of serial communication functions.

#### FEATURES

- o 4 MHz 280A CPU
- o Provides two sockets for EPROM
- Accepts 2716 (2Kb x 8 bit) or 2732 (4Kb x 8 bit) EPROM's
   8Kb of private RAM
- o 8Kb of private RAM
   o Direct Memory Access to all of system memory
- Can operate as a stand-alone processor or as either a master or slave processor in a multiprocessor system
- o One channel of IEEE 488-1978 Instrumentation Bus (Subset of GPIB) capability
- o User programmable to operate as a Controller, Talker, or Listener
- Two channels of serial communications capability provided by 280A SIO
- o Full Modern Control
- Support for Async, Byte Sync, or Bit Sync protocols
- o Programmable Async baud rates up to 9600 baud
- o Programmable Synchronous baud rates up to 500K baud
- o Supports bankswitched memory
- o Supports powerfail interrupts o Software programmable baud
- rate for Async up to 9600 baud. o Packaged cable and communica-
- tion adapter included for direct instrumentation hookup

## 1843+ USER-PROGRAMMABLE INTELLIGENT IEEE 488 BUS INTERFACE



#### DESCRIPTION

The 1843+ is a self contained, microprocessor based IEEE-488-1978 GPIB interface module. There are also two programmable serial communication channels provided. The 1843+ contains a 280A, 4MHz, 8 bit microprocessor; 8Kb of static RAM; and sockets for up to 8K of EPROM. The on-board memory is local to the 1843+ but the module has the capability of directly accessing any location in system memory. There is an 8 bit handshake port available for communications between the 1843+ and other processors.

The 1843+ contains a TMS 9914 GPIB controller chip. This chip can be programmed to allow the 1843+ to be connected to a IEEE-488 bus as either a talker, listener, or a controller. This capability will allow XYCOM systems to become part of a GPIB network as an intelligent peripheral device under the control of some other network controller, or as the network controller itself.

Bit-synchronous mode at baud rates up to 500K baud. These serial channels will allow the 1843+ to act as a bridge between a GPIB network and serial network.

The 1843+'s GPIB signals are standard TTL level signals and a buffered by the GPIB Interface adapter module which is included

with the 1843+. The output of the interface adapter meets IEEE-488-1978 specifications. Likewise, the two serial communication channels are brought off the 1843+ at TTL levels. These channels may be connected to user selectable communications modules to provide for 20mA current loop, RS-232C, RS-422, or RS-423 compatible communications or Fiber Optics.



#### BLOCK DIAGRAM DESCRIPTION

The 1843+ contains a Z80A microprocessor with a 16-bit program counter for direct addressing of up to 64K bytes of memory. There are two identical sets of general purpose registers, accumulators, and flag registers in the Z80A; a main register set, and an auxiliary set of registers. Either set of registers or accumulators and flags can be selected, at any time, by using one exchange command. This feature permits fast storage of registers needed for interrupt service routines or subroutine servicing. An external stack located within any portion of read/write memory may be used as a last-in, first-out buffer to restore the contents of the program counter, flags, accumulator, all six general purpose registers, and the auxiliary register set (accumulator, flags, and six general purpose registers). The CPU includes an 8-bit bidirectional data bus, 16-bit address bus, and 158 different instructions. These 158 instructions include all of the 8080A instructions.

Two independent full duplex serial channels provide serial communications capability. Data rates up to 500K bits-per-second are software selectable on a per port basis; each port's receive and transmit clocks are tied together. The receivers are quadruplebuffered and the transmitters are dualbuffered. Some of the features of the serial ports are programmable sampling rates, parity/overrun/framing error detection. programmable CRC insertion/deletion plus break detection and generation. The SIO supports asynchronous, bit synchronous, and byte synchronous software protocols. Either an internal or external clock is jumper selectable for each port. Both serial input/ output ports are TTL compatible signals. Separate termination level shift modules and interconnect cable assemblies (communication adapters) are available to meet 20mA current loop, RS-232C, RS-422A, RS-423A, and Fiber Optic specifications.

The Counter-Timer Circuit (CTC), provides four independent channels of counting and timing functions.

The user can configure the 1843+ so that CTC channel 0 either generates a clock for SIO channel A or for both SIO channels (A and B).

CTC channel I can be used to:

- a. generate a clock for SIO channel B or
- b. release the 180+ System Bus Latch, or
- c. release the 180+ System Bus Latch and generate a non-maskable interrupt to the 1843+'s processor or,
- d. release the 180+ System Bus Latch and generate a reset of the 1843+'s processor or,
- e. generate an interrupt from the Trigger signal of the TMS 9914.

CTC channel 2 can be used to generate an interrupt from the (INT) signal of the TMS 9914.

CTC channel 3 can be used to acknowledge an interrupt from the backplane's interrupt request pin's signal (IREQ).

An alternative to the above options is to use any of the channels as a counter or timer. In either case, the 1843+'s processor can examine the state of the counter before the timer or clock reaches zero. When the timer or clock reaches zero it can interrupt the processor, if interrupts are enabled. The timer or clock will reload the time constant and repeat the count down process.

The standard 1843+ comes with IK bytes of RAM memory (450 nanosecond memory cycle

2114L RAM chips, with no wait states required).

The 1843+ can contain up to 8K bytes of non-volatile read only memory. Various types of EPROM/ROM chips may be inserted into the six sockets provided. Non-volatile read only memory may be added in 2K byte increments (up to 4K bytes), using TMS 2516 EPROMs, or Intel 2716 EPROMs; in 4K byte increments (up to 8K bytes), using TMS 2532 EPROMs.

The External Processor Interface provides the 1843+ with an eight (8) bit bidirectional hand shake port between the on board 280A and other processor modules on the 180+ system bus.

. The Interface with System Memory allows direct access, by the 1843+, to system memory.

Bankswitch and full memory mapping schemes are available and each is jumper controlled. Both memory mapping schemes allow the 1843+ to access all the 180+ memory and I/O space.

The full memory mapping scheme allows several memory mapping variations onboard; EPROM/ROM, RAM and system (off-board) memory under software control. Four software controlled configurations are available to the user. Memory Map 1 is initialized on a power-up condition.

	MAP 1	MAP 2	MAP 3	MAP 4
FFFFH	180+			1
	System	180+	180+	
	Memory	System	System	t l
4000H		Memory	Memory	180+
	Onboard			System
	RAM		] ]	Memory
2000H				
	Onboard	Onboard	Onboard	
	EPROM	EPROM	EPROM	1 1
0000H	1 1	1 1	1	1 1
	Power-up	·	·	
	Condition			

The bank switch memory mapping scheme allows the user to access half the 180+ address space at a time. The half of system memory being accessed is under software control.



The Bus Buffers circuitry provides the necessary buffering of Address and Data information between the 1843+ private bus and the 180+ system bus.

#### JUMPER FEATURES

- o Master/Slave Select
- o EPROM Type Select
- Global Nemory Access Bankswitch/Full Access
- o External/Internal Serial clocks
- c Watchdog Timer (Reset or NMI)

#### **PIN OUTS**

Serial Connector\*

Signal	Function
тэ	Transmit Data from 1843+
RD	Receive Data to 1843+
тс	Transmit Data Clock (external)
RC	Receive Data Clock (external)
RTS	Request To Send Output
CTS	Clear To Send Input
DCD	Data Carrier Detect Input
DTR	Data Terminal Ready Output
SYNC	External Sync Input
GND	Logic Ground

\* These signals are repeated two times

GPIB Connector			
Signal	Function		
DIO	Data Input/Output Lines		
SC	System Controller		
TE	Talk Enable		
CONT-	Controller		
SRQ	Service Request		
ATN	Attention		
EOI	End or Identify		
DAV	Data Valid		
NRFD	Not Ready for Data		
NDAC	No Data Accepted		
IFC	Interface Clear		
REN	Remote Enable		

#### Reset Connector

RESET	1843+ Reset Input
GND	Logic Ground

#### CONNECTORS

IEEE-488 GPIB Connector

The 1843+ is connected to the GPIB interface adapter via a 50 wire ribbon calle. The output of the interface adapter is a standard 24 pin GPIB connector including 8 bidirectional data lines (DIO1-DIO8), 8 bidirectional control and handshake lines, 7 logic ground, and 1 shield.

#### CONNECTORS

Serial (50 pin flat ribbon)

T&B/Ansley	#609-5000M
Winchester	#51-1150-00
AMP	#88379-8

#### Reset (2 pin crimp ramp lock)

*Molex	Molex #09-50-3021				
*requires flat cr	imp terminal				
Molex	#08-50-0107 (chain)				
or Molex	#08-50-0108 (loose)				

#### MODULE SPECIFICATIONS

Power Required (Max.)

+5VDC @ 3.0A

#### FAMILY SPECIFICATIONS

١

- o TEMPERATURE Operating: 0° to 65°C (32° to 149°F) Non-Operating: -40° to 85°C (-40° to 185°F)
- HUMIDITY
   to 100% RH Non-condensing
   (Note, extreme low humidity conditions may require special protection against static discharge.)
- ALTITUDE
   Operating: Sea level to 20,000 ft.
   (6096 m)
   Non-Operating: Sea level to 50,000 ft.
   (15240 m)
- o VIBRATION 0.1 in (2.5 mm) pp, 10 to 30 Hz 5.0 g, 30 to 500 Hz 0.036 in (0.9 mm) pp, 50 Hz 0.024 in (0.6 mm) pp, 60 Hz
- PHYSICAL SPECIFICATIONS Standard Board Envelope
   8.5"H x 10.5"L x 0.6"Profile
   (21.6 cm x 26.7 cm x 1.5 cm)

- AMBIENT ATMOSPHERE The design, fabrication, and protective sealant procedures used are consistent with those of the petro-chemical and other contaminated-atmosphere manufacturing environments. Specifically, 180+ modules have a significantly increased chemical resistance to:
  - Hot water vapor Hydraulic oil Lubricating oil VM and P Naphtha Trichloroethylene Carbon Tetrachloride Fungus Oxidation Partial protection is provided against: Dilute sulfuric acid mist Salt spray Gasoline Benzene, Toluene Xylene Ammonium Hydroxide
- SHOCK
  - 30g, 11 ms, 1/2 sine

#### ORDERING INFORMATION

Description

Number

1843+

ź

User Programmable Intelligent IEEE-488 Bus Interface

# xycom

P O Box 984 • Ann Arbor, Michigan 48106 • Phone: (313) 429-4971 • TWX: 810-223-8153

SP 5N 1843 4 8.

.....



## 1862+ Z80A 8-BIT MASTER/SLAVE MICROCOMPUTER

#### FUNCTION

The 1862+ is a 280A based CPU module which can be programmed by the user to perform as a master or a slave CPU in a 180+ system.

#### **FEATURES**

- o Z80A 4MHz eight (8) bit CPU
- Optional hardware APU, 9511 or FPU 9512
- o 8Kb private RAM
- o Up to \$Kb private EPROM
- o Two (2) channels of either ASYNC or high speed synchronous communication with full modern control
- o Software programmable baud rate for ASYNC, up to 9600 baud
- Capable of 500K baud rate for synchronous communications
- Operates independently or in a multiprocessor environment, as either a master or slave
- o Two sockets for EPROM o Supports flexible mapping
- of private memory o Supports bankswitched memory
- o Hardware powerfail interrupts support
- o User programmable watchdog timer to disable module and release the 180+ system bus in a multiprocessor environment



#### DESCRIPTION

The XYCOM 1862+ is a self-contained, single board microcomputer that interfaces with a variety of memory, digital I/O, analog I/O, processor, and communications modules. Interfacing is done through XYCOM's chassis/backplane assemblies to form a complete microcomputer system. The 1862+ is capable of operating in a multiprocessor environment as the master or slave CPU. The 1862+ features a 280A processor, 8Kb of Random Access Memory for data storage and retrieval, sockets for up to 8Kb of non-volatile Read-Only Memory, two independent full duplex serial ports, and an optional arithmetic processor unit or floating point processor unit.



#### BLOCK DIAGRAM DESCRIPTION

and the second second

The 1862+ contains a 280A microprocessor with a 16-bit program counter for direct addressing of up to 64K bytes of memory. There are two identical sets of general purpose registers, accumulators, and flag registers in the 280A; a main register set, and an auxiliary set of registers. Either set of registers or accumulators and flags can be selected, at any time, by using one exchange command. This feature permits fast storage of registers needed for interrupt service routines or subroutine servicing. An external stack located within any portion of read/write memory may be used as a last-in, first-out buffer to restore the contents of the program counter, flags, accumulator, all six general purpose registers, and the auxiliary register set (accumulator, flags, and six general purpose registers). The CPU includes an 8-bit bidirectional data bus, 16-bit address bus, and 158 different instructions. These 158 instructions include all of the 8080A instructions.

The Arithmetic Processor Unit (APU) performs high-speed fixed- or floating-point calculations. The APU operates on 16- or 32bit fixed-point numbers and on 32-bit floatingpoint numbers. A wide range of instructions can be performed which include: add, subtract, multiply, divide, trigonometric functions, inverse trigonometric functions, logarithms, natural logarithms, exponentiation, and square root. Completion of a calculation can be determined either by interrupts or polling.

The Floating Point Processor Unit (FPU) performs floating-point single (32-bit) and double (64-bit) precision calculations. The Floating Point Processor Unit offers the full range of arithmetic functions: add, subtract, multiply, divide, and IEEE format (IEEE standard rounding algorithm). Current command execution resulting in an error condition can generate an interrupt. Some of the error conditions are: an attempt to divide by zero, exponent overflow and exponent underflow. Completion of a calculation can be determined either by interrupts or polling.

Two independent full duplex serial channels provide serial communications capability. Data rates up to 500K bits-per-second are software selectable on a per port basis. The receivers are quadruple-buffered and the transmitters are dual-buffered. Some of the features of the serial ports are programmable sampling rates, parity/overrun/framing error programmable detection. CRC insertion/deletion plus break detection and generation. The SIO supports asynchronous, bit synchronous, and byte synchronous software protocols. Either an internal or external clock is jumper selectable for each port. Both serial input/output ports use TTL compatible signals. Separate termination level shift modules and interconnect cable assemblies (communication adapters) are available to meet 20mA current loop, RS-232C, RS-422A, RS-423A, and Fiber Optic specifications.

The Counter-Timer Circuit (CTC), provides four independent channels of counting and timing functions.

The user can configure the 1862+ so that CTC channel 0 either generates a clock for SIO channel A or for both SIO channels (A and B).

CTC channel I can be used to:

- a. generate a clock for SIO channel B or
- b. release the 180+ System Bus Latch, or
- c. release the 180+ System Bus Latch and generate a non-maskable interrupt to the 1862+'s processor or,
- d. release the 180+ System Bus Latch and generate a reset of the 1862+'s processor or,
- e. generate an interrupt from the ERR signal from an optional FPU.

CTC channel 2 can be used to generate an interrupt from the END signal from an optional APU or FPU.

CTC channel 3 can be used to acknowledge an interrupt from the backplane's interrupt request pin's signal (IREQ).

An alternative to the above options is to use any of the channels as a counter or timer. In either case, the 1862+'s processor can examine the state of the counter before the timer or clock reaches zero. When the timer or clock reaches zero it can interrupt the processor, if interrupts are enabled. The timer or clock will reload the time constant and repeat the count down process. The standard 1862+ comes with 8K bytes of RAM memory (450 nanosecond memory cycle 2114L RAM chips, with no wait states required).

The 1862+ can contain up to 8K bytes of non-volatile read only memory. Various types of EPROM/ROM chips may be inserted into the six sockets provided. Non-volatile read only memory may be added in 2K byte increments (up to 4K bytes), using TMS 2516 EPROMs, or Intel 2716 EPROMs; in 4K byte increments (up to 8K bytes), using TMS 2532 EPROMs.

The External Processor Interface provides the 1862+ with an eight (8) bit bidirectional hand shake port between the on board 280A and other processor modules on the 180+ system bus.

The Interface with System Memory allows direct access, by the 1862+, to system memory.

Bankswitch and full memory mapping schemes are available and each is jumper controlled. Both memory mapping schemes allow the 1862+ to access all the 180+ memory and I/O space.

The full memory mapping scheme allows several memory mapping variations onboard. Four software controlled configurations are available to the user. Memory Map 1 is initialized on a power-up condition.

	MAP 1	MAP 2	MAP 3	MAP 4
FFFFH	180+			
	System	180+	180+	
	Memory	System	System	[
4000H		Memory	Memory	180+
	Onboard		1 1	System
	RAM	1 1	1 1	Memory
2000H	1 1	1 1	1 1	
	Onboard	Onboard	Onboard	
	EPROM	RAM	EPROM	
0000H	1 1	1 1		1
	Power-up	·		
	Condition			

The bank switch memory mapping scheme allows the user to access half the 180+ address space at a time. The half of system memory being accessed is under software control.



The Bus Buffers circuitry provides the necessary buffering of Address and Data information between the 1862+ private bus and the 180+ system bus.

#### JUMPER FEATURES

- o Master/Slave Select
- o EPROM Type Select
- o Global memory access -Bank Switch/Full Access
- Internal/External Serial clocks ο
- Watchdog Timer (Reset or NMI) 0

#### **PIN OUTS**

State of the second sec

Serial Connector\*

Signal	Function
TD	Transmit Data from 1862+
RD	Receive Data to 1862+
TC	Transmit Data Clock (external
RC	Receive Data Clock (external)
RTS	Request To Send Output
CTS	Clear To Send Input
DCD	Data Carrier Detect Input
DTR	Data Terminal Ready Output
SYNC	External Sync Input
GND	Logic Ground

\* These signals are repeated twice

#### **Reset Connector**

Signal	Function
RESET	1862+ Reset Input
GND	Logic Ground

#### CONNECTORS

Serial (50 pin flat ribbon)

Winchester #51-1150-00 Amp #88379-8
--

Reset (2 pin crimp ramp lock)

*Molex	#09-50-3021		
*requires flat crimp terminal			

Molex	#08-50-0107 (chain)
Molex	#08-50-0108 (loose)

#### MODULE SPECIFICATIONS

Serial Port

All lines are TTL levels to and from the module. XYCOM communications Adapters are required for proper interfacing.

#### Power Required (Max.)

- +5VDC @ 3.0A +12VDC @ 100mA

#### FAMILY SPECIFICATIONS

- o TEMPERATURE Operating: 0° to 65°C (32° to 149°F) Non-Operating: -40° to 85°C (-40° to 185°F)
- HUMIDITY
   to 100% RH Non-condensing
   (Note, extreme low humidity conditions may require special protection against static discharge.)
- ALTITUDE Operating: Sea level to 20,000 ft. (6096 m) Non-Operating: Sea level to 50,000 ft. (15240 m)
- o
   VIBRATION

   0.1 in (2.5 mm) pp,
   10 to 30 Hz

   5.0 g,
   30 to 500 Hz

   0.036 in (.9 mm) pp,
   50 Hz

   0.024 in (.6 mm) pp,
   60 Hz
- PHYSICAL SPECIFICATIONS Standard Board Envelope 8.5"H x 10.5"L x 0.6"Profile (21.6 cm x 26.7 cm x 1.5 cm)

AMBIENT ATMOSPHERE
 The design, fabrication, and protective sealant procedures used are consistent with those of the petro-chemical and other contaminated-atmosphere manufacturing environments. Specifically, 180+ modules have a significantly increased chemical resistance to:

Hot water vapor Hydraulic oil Lubricating oil VM and P Naphtha Trichloroethylene Carbon Tetrachloride Fungus Oxidation Partial protection is provided against: Dilute sulfuric acid mist Salt spray Gasoline Benzene, Toluene Xylene Ammonium Hydroxide

o SHOCK

30g, 11 ms, 1/2 sine

#### ORDERING INFORMATION

Number	Description
1862+	280A 8-Bit Master/Slave Microcomputer
00X	<u>Select one only</u> -001 APU (Arithmetic Processing Unit) -002 FPU (Floating Point Processor Unit)



P.O. Box 984 • Ann Arbor, Michigan 48106 • Phone: (313) 429-4971 • TWX: 810-223-8153

SP 5M 1862 4 81 Litho in U S A

61

.



## 1890+ AND 1891+ BREADBOARD KITS

mmmuum

#### FUNCTION

The 1890+ and 1891+ breadboards are implementation tools for any user doing custom designing of special purpose modules.

#### FEATURES

- o PC land patterns will accept 14, 16, 18, 20, 22, 24, 28 and 40pin IC's.
- o Standard Flexibus III connectors
- o Two 36pin user I/O connectors
- o Bussed  $\pm 5$ ,  $\pm 12$ VDC, and grounds
- o Pads for decoupling capacitors



#### DESCRIPTION

The XYCOM 1890+ and 1891+ Breadboards are printed circuit board, prototyping modules, especially designed to conveniently implement custom designed, special purpose modules. Both include the standard Flexibus III bus interface connectors as used in Superpac and Micropac 180 Series systems. The 1891+ also includes the Flexibus III Interface circuitry.

#### **XYCOM 1890+ CAPABILITIES**

The XYCOM 1890+ is extremely convenient for generating custom circuitry to work in conjunction with the XYCOM Microcomputer modules in the 180+ series. Standard Flexibus III connectors are provided, but the user can design his own interface circuitry providing maximum flexibility. This feature is particularly useful when designing a special bus interface.

The 1890+ will accommodate up to 72, 16pin IC's. However, the land pattern will also accept 14, 18, 20, 22, 24, 28 and 40 pin devices.

#### **XYCOM 1891+ CAPABILITIES**

The XYCOM 1891+ is similar to the 1890+ board but includes Flexibus III circuitry, in addition to the backplane connector. When standard bus circuitry can be used, this feature saves substantial design time while prototyping special function modules. The 1891+ is furnished in kit form and the user need only mount components on the board, add his custom circuitry, and insert in a 180+ Series chassis for operation.

The 1891+ will accommodate 48, 16 pin IC's. However, the land pattern will also accept 14, 18, 20, 22, 24, 28 and 40 pin devices.

#### **PIN OUTS**

There are 36 pins available for use in the specific design.

#### CONNECTORS

- (2) 18 position double sided edge
  - o Molex #09-50-6185
  - Requires flat crimp terminal Molex #08-05-0302

#### MODULE SPECIFICATIONS

DC Input Power Required (Max.):

+5Vdc +5%
+5Vdc +5%
+12Vdc+5%
-5Vac +3%
-12Vdc +5%

Current loads determined by device and circuit configurations

#### FAMILY SPECIFICATIONS

- o TEMPERATURE Operating: 0° to 65°C (32° to 149°F) Non-Operating: -40° to 85°C (-40° to 185°F)
- HUMIDITY
   to 100% RH Non-condensing
   (Note, extreme low humidity conditions may require special protection against static discharge.)
- ALTITUDE
   Operating: Sea level to 20,000 ft.
   (6096 m)
   Non-Operating: Sea level to 50,000 ft.
   (15240 m)
- o
   VIBRATION

   0.1 in (2.5 mm) pp,
   10 to 30 Hz

   5.0 g,
   30 to 500 Hz

   0.036 in (0.9 mm) pp,
   50 Hz

   0.024 in (0.6 mm) pp,
   60 Hz
- PHYSICAL SPECIFICATIONS Standard Board Envelope
   8.5"H x 10.5"L x 0.6"Profile
   (21.6 cm x 26.7 cm x 1.5 cm)

كورها المريقة فيتوجز والارار

AMBIENT ATMOSPHERE
 The design, fabrication, and protective sealant procedures used are consistent with those of the petro-chemical and other contaminated-atmosphere manufacturing environments. Specifically, 180+ modules have a significantly increased chemical resistance to:

Hot water vapor Hydraulic oil Lubricating oil VM and P Naphtha Trichloroethylene Carbon Tetrachloride Fungus Oxidation Partial protection is provided against: Dilute sulfuric acid mist Salt spray Gasoline Benzene, Toluene Xylene Ammonium Hydroxide

o SHOCK 30g, 11 ms, 1/2 sine

### ORDERING INFORMATION

Number	Description
1890+	Breadboard Kit
1891+	Breadboard Kit with Bus Logic



P.O. Box 984 • Ann Arbor, Michigan 48106 • Phone: (313) 429-4971 • TWX: 810-223-8153

Copyright 1981 by XYCOM Hic Specifications subject to change without notice

A REAL PROPERTY AND A REAL

5P 5M 1890 1891 4 81 Litho in U S A



## **180 Chassis/Power Supply**

## **180 Product Line**

#### **FEATURES**

- ٠ Industrial service housing
- 4-, 8-, 12-, or 20-slot chassis 106, or 175 watt power .
- ٠
- supply Flexibus II printed circuit board backplane interconnect 16-bit address bus 8-bit bidirectional data bus Shielded analog bus
- **Control** lines Power
- integral, card-edge connectors . • Hardwired slot address

#### **APPLICATIONS**

- OEM Designs .
- Modular Systems .
- Custom Requirements .
- System Development



#### DESCRIPTION

XYCOM 180 Series Microcomputer Systems are configured modular chassis designed for use in industrial environments. An integral, Flexibus II backplane in the chassis includes card-edge connectors for all operational system modules and provides all intermodule power, control and data bussing on a printed circuit board.

Chassis/backplane assemblies are available in 4-, 8-, 12- and 20-slot versions to accommodate different system requirements. This choice permits considerable flexibility in system design for specific applications, and in planning for future system expan-sion. Because the 4-, 8-, 12- and 20-slot chassis are interchangeable, a basic system can be easily adapted to changing requirements by adding, removing, or changing system modules.

#### Chassis

Four chassis sizes are available for mounting and protecting the system module cards. A 4-slot, 8-slot, 12-slot, or 20-slot version may be chosen, depending on system specifications. All are of rugged, durable construction and have been designed for use on the shop floor in a manufacturing environment. While the chassis may be mounted in any orientation, vertical mounting is recommended to allow proper air circulation between card modules. Chassis dimensions are listed in the specifications

#### Flexibus II Backplane

FLEXIBUS II SIGNAL LIST

The Flexibus II backplane provides all internal communication circuits between system modules and includes a 16-bit address bus, an 8-bit bidirectional data bus, and control in and out lines. A two-wire shielded analog bus is also provided to allow bussing of analog signals to an A/D converter module after multiplexing for large capacity data acquisition systems

The backplane consists of a printed circuit board etched to provide parallel bus lines to distribute functional signals to all module pin connectors. The pin connectors are mounted on the backplane perpendicular to the bus lines to ensure that the pin assignment of functional signals remains the same for each pin connector. Since the functional signal assignment is duplicated for each connector, any module can be installed in any desired chassis slot for proper module operation.

All backplanes have address line ADCR0 through ADRC3 hardwired using +5VLOG and LGND to obtain a hexadecimal slot code address. In the 4-, 8-, and 12-slot chassis, all slots are directly addressable and corresponding modules may be selected by user programming for functional operations. For the 20slot chassis, slots 5 through 20 are addressable by hexadecimal code. The first four slots which will not accept an I/O address signal, are used for memory and CPU modules. This construction ensures system flexibility and expansion capability by providing interchangeable board connections with module slot selection during operation being made entirely by user software programming

The backplane printed circuit board is 1/8 inch epoxy-glass with conductors for typical loads anticipated for each size assembly. The etched board is mounted on the rear wall of the chassis with the pin connectors and chassis slots aligned to ensure convenient and reliable module mounting and connection. Load limits for the backplane circuits are listed in the specifications

#### Pin Pin Signal Signal 1 ADRCO 90 DATA6 2 ADRC1-30 DATA7 READ-3 ADRC2-31 WRITE ADRC3-32 4 LGND 33 STRBE 5 34 35 h LGND IOCMP-MCLR-ADRO 7 WAIT-ADR1-36 37 8 9 ADR2-IREQ-38 39 10 ADR3-OSC HOLD 11 ADR4 40 ADR5-BUSYI+ 12 ADR6-41 BUSYO+ 13 42 43 44 ADR7-PWRF-14 -12V15 ADR8-+20V 16 17 ADR9. ADR10-45 AGND ADR11-46 -20V 18 19 ADR12-47 -5V + 12V 20 21 22 ADR13 49 +5VMEM ADR14-ADR15 50+5VMEM 23 24 25 51 52 53 DATA0 +5VLOG DATA1 +5VLOG SHLDO 26 27 54 55 ABHI DATA3 DATA4 ABL() 28 DATA5 56 SHLD1



#### 180 SERIES BACKPLANE TIMING DIAGRAM (WRITE)















\_**T**-
# SPECIFICATIONS

# Electrical

Electrical +5V (± 5%) -5V (± 5%) +12V (± 2%) -12V (± 5%) *Total not to exceed 175 Watts		1885A (106 Watt) 1 to 12A 0 to 1.5A .5 to 2A 0 to 1A	1886A* (175 Watt) 20A 5A 5A 1.5A		
Mechan	ical				
	1894A (4-Slot)	1895A (8-Slot)	1896A (12-Slot)	1897A (20-Slot)	
Height Width Depth	4.43 in. (11.25 cm.) 11.7 in. (29.72 cm.) 9.23 in. (23.44 cm.)	7.43 in. (18.87 cm.) 11.7 in. (29.72 cm.) 9.23 in. (23.44 cm.)	11.22 in. (28.50 cm.) 11.25 in. (28.58 cm.) 8.75 in. (22.23 cm.)	12.21 in. (31.01 cm.) 16.99 in. (43.16 cm.) 11.62 in. (29.52 cm.)	

#### Environmental

Operating Storage  $0^\circ$  to 60°C; 0 to 90% relative humidity (noncondensing) -40 $^\circ$  to 85°C; 0 to 85% relative humidity (noncondensing)

1885A Power Supply and External Pin List (P1)			1886A Power Supply Pin List (P1)			)	
Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	PWRF	7	+12V	1	AC IN	7	NC
2	+HV	8	+ 5V MEM	2	AC COMM	8	-5V
3	+20V	9	+ 5V MEM	3	GROUND	9	LGND
4	AGND	10	+ 5V LOG	4	LGND	10	LGND
5	-20V	11	+5V LOG	5	NC	11	+12V
6	– 5V	12-20	LGND	6	+5V	12	-12V
						13	LGND

### Ordering Information

Model No.	Option	Description
1885 A		Power Supply, 106 Watt
	001	Add Power Cord and Connector Kit
1886A		Power Supply, 175 Watt
1894A		Chassis, 4-Slot
1895A		Chassis, 8-Slot
1896A		Chassis, 12-Slot
1897A		Chassis, 20-Slot
180A-M		Chassis/Power Supply Manual

Note: Specifications subject to change without notice.



PC Box 984 Ann Arbor Michigan 48106

Phone (313) 429 4971 •

TWX: 810-223-8153

SP Rev BI0780 Lehoin USA

69



# 960X COMMUNICATION **ADAPTERS**

### FUNCTION

The 960X series of modules are used to interface XYCOM's serial communication capabilities to industry standard communications lines.





#### FEATURES

- o Adapt data and control signals from a XYCOM communication module to fit the requirements of a particular type of communication environment.
- Adapters available: Δ
  - 20mA current loop (9601) RS232 (9602) RS422 (9603)
  - -

  - RS423 (9604)
- Adapters may be changed with-0 out affecting communications software
- Inputs are TTL compatible 0
- Full modern support 0





#### DESCRIPTION

All of XYCOM's intelligent 180+ modules which have serial communication capability provide this capability via a 12 wire ribbon cable. The signal levels carried on this ribbon cable are TTL compatible. Each of the 960X communications adapters convert these TTL signals to and from various industry standard signal levels. This method gives the user the most flexibility in meeting a particular communication requirement. Communication adapters are changed without modifications to the 180+ systems hardware or software.







#### BLOCK DIAGRAM DESCRIPTION

This module converts the system's TTL Transmit Data (TD) signal into a 20mA current source (SOH). This is the same current source signal for TTOUT except that it is current limited. The (DTR) signal is used as the reader control signal (RCTRL) and is buffered for a tape reader. The SOL line is used as the return for either SOH or TTOUT according to the user configuration.

The adapter takes the SIH input optically, isolates it, and then converts it to the TTL Level (RD) signal.

#### The 9602/9603/9604 Modules

These three modules are very similar in their operation. The 9602 adapts TTL to RS232, the 9603 adapts TTL to RS422, and the 9604 adapts TTL to RS423 compatible equipment. All three modules can be jumpered to allow the transmit and receive clocks to be supplied externally. The transmit clock is also sent to peripheral equipment, and can be looped back on-board to the receive clock. Data Terminal Ready (DTR), Request to Send (RTS), Clear to Send (CTS) and Data



Carrier Detect (DCD) modem control signals are supported on all three modules. The three types of modules can be used with ASYNC or synchronous communication protocols.

The SYNC pin can be used in either direction. The SYNC pin signal can be generated by a synchronous modem, or the SYNC pin signal can be generated by the 180+ series SIO serial 1/O chip. This pin is used to synchronize "byte boundaries" in synchronous communications.

#### JUMPER FEATURES:

#### 9601

- o Receive Data polarity
- o Transmit Data polarity
- o Receiver supplies current
- o Transmitter power supplied externally or internally

9602, 9603, 9604

- o Receiver clock externally supplied
- o Receiver clock looped back from transmit clock

. ....

o Transmit clock externally supplied

## PIN OUTS:

20mA Current-Loop

Name	Description
SOL	Serial Output,Low
SOH	Serial Output,High
TTOUT	20mA Output
+SEXT	External +5V
VCC	Vcc
RCTRL-	Reader Control
SIL	Serial Input,Low
SIH	Serial Input,High

## RS-232

ľ

Name	Description	Direction (with respect to XYCOM System)
AA	Equipment Ground	
BA	Transmitted Data	output
BB	Received Data	input
CA	Request to Send	output
СВ	Clear to Send	input
CC	Data Set Ready	input
AB	Logic Ground	
CF	Data Carrier Detect	input
(Reserved)		
(Reserved)		
(Spare)	New Signal	
SCF		input
SCB		input
SBA		output
DB	Transmit Clock	input
SBB		input
DD	Receive Clock	input
(Spare)	Synchronization	either (3)
SCA		input
CD	Data Terminal Ready	output
CG		input
CE	Incoming Call	input
СН	Signal Rate	output
DA	Transmit Clock	output
(Spare)	Select Standby	

RS-422/423

Name	Description	Direction (with respect to XYCOM System)
Shield	Equipment Ground	
S1		input
(Spare)	Synchronization	either
SD+	Transmitter Data	output
ST+	Transmit Clock	input
RD++	Receive Data	input
RS+	Request to Send	output
RT+	Receive Clock	input
CS+	Clear to Send	input
LL		output
DM+	Data Set Ready	input
TR+	Data Terminal Ready	output
RR+	Data Carrier Detect	input
RL		output
IC	Incoming Call	input
SF/SR		output
TT+	Transmit Clock	output
ТМ		input
SG	Logic Ground	output
RC		input
(Spare)	Synchronization	either
SD-	Transmit Data	output
ST-	Transmit Clock	input
RD-	Receive Data	input
RS-	Request to Send	output
RT-	Receive Clock	input
CS-	Clear to Send	input
15		output
DM-	Data Set Ready	input
TR-	Data Terminal Ready	output
RR-	Data Carrier Detect	input
SS		output
SG	Logic Ground	input
NS	New Signal	output
TT-	Transmit Clock	output
SB		input
SC	Logic Ground	output

73

:

1.15

#### **CONNECTORS**

9601	
20mA 9 pin plug assembly Crimp pin	AMP 205204-1 AMP 66507-4 (28-24 ga. chain)
9602	
RS232 25 pin plug assembly Crimp pin	AMP 205208-1 AMP 66507-4 (28-24 ga. chain)
9603/04	
RS422/23 37 pin plug assembly Crimp pin	AMP 205210-1 AMP 66507-4 (28-24 ga. chain)
Comm. Adapters/Internal Conn. 20mA, RS232, RS423/24	
20 pin ribbon socket	3M 3421 Winchester 51-1120-00 AMP 88377-4
6 circuit DC power	Molex 22-26-2066

#### MODULE SPECIFICATIONS

Power Required (Max.):

9601		<u>9602</u>	9603	9604
+5VDC (	0 120mA	+5VDC @ 70mA	+5VDC @ 300mA	+5VDC @ 375mA
+12VDC	@ 20mA	+12VDC @ 50mA -12VDC @ 20mA	-5VDC @ 125mA	-5VDC @ 210mA

## FAMILY SPECIFICATIONS

o TEMPERATURE Operating: 0° to 65°C (32° to 149°F) Non-Operating: -40° to 85°C (-40° to 185°F)

 HUMIDITY
 to 100% RH Non-condensing
 (Note, extreme low humidity conditions may require special protection against static discharge.)

- ALTITUDE
   Operating: Sea level to 20,000 ft.
   (6096 m)
   Non-Operating: Sea level to 50,000 ft.
   (15240 m)
- o VIBRATION 0.1 in (2.5 mm) pp, 10 to 30 Hz 5.0 g, 30 to 500 Hz 0.036 in (0.9 mm) pp, 50 Hz 0.024 in (0.6 mm) pp, 60 Hz
- PHYSICAL SPECIFICATIONS Standard Board Envelope
   8.5"H x 10.5"L x 0.6"Profile
   (21.6 cm x 26.7 cm x 1.5 cm)

- **o** AMBIENT ATMOSPHERE
  - The design, fabrication, and protective sealant procedures used are consistent with those of the petro-chemical and other contaminated-atmosphere manufacturing environments. Specifically, 180+ modules have a significantly increased chemical resistance to:

Hot water vapor Hydraulic oil Lubricating oil VM and P Naphtha Trichloroethylene Carbon Tetrachloride Fungus Oxidation Partial protection is provided against: Dilute Sulfuric acid mist Salt spray Gasoline Benzene, Toluene Xylene Ammonium Hydroxide

o SHOCK 30g, 11 ms, 1/2 sine

# ORDERING INFORMATION

## Number Description

A Contract of the second s

9601 9602 9603 9604	20mA Current Loop Communication Adapters RS232C Communication Adapters RS422 Communication Adapters RS423 Communication Adapters
	OPTIONAL ACCESSORIES
Number	Description
9670	Communications Adapter Connector Kit - 20 pin Ribbon cable plug - 6 pin Discrete wire power connector
9671	Connector for 9601
9672	Connector for 9602
9673	Connector for 9603
9674	Connector for 9604, same as 9673
9690	4 Channel Communication Controller Cable to 960X's
9691	2 Channel Communications Controller Cable to 960X's



P.O. Box 984 • Ann Arbor, Michigan 48106 • Phone: (313) 429-4971 • TWX: 810-223-8153

SP 5M 960X 4 81 Litho in U S A



# 9680 COMMUNICATIONS ADAPTER RACK

## FUNCTION

The 9680 Communications Adapter Rack provides a power supply for XYCOM's 960X series of communications adapters and rack space for mounting up to five adapters.



#### FEATURES

- o 19 inch rack mountable
- o Holds up to five 960X series communication adapters
- o Four linear supply outputs +5V, -5V, +12V, -12V

#### DESCRIPTION

The 9680 Communications Adapter Rack can contain up to four linear power supplies for powering 960X communication adapters. The supplies provided are +5 volts, -5 volts, +12 volts, and -12 volts.

The 9680 is a 19 inch rack mountable unit. Across the front are spaces for mounting five single width 960X communications adapters. The fiber optics 9605 module takes two spaces when used.

.

# **PIN OUTS**

Name	Description
+5	Positive 5 volt supply
-5	Negative 5 volt supply
+12	Positive 12 volt supply
-12	Negative 12 volt supply
GND	Chassis ground (for 9680)
EQPT GND	External equipment ground

## CONNECTORS

and the second second second second second

فتقلقان وينحددهم

Terminal strip

# MODULE SPECIFICATIONS

Mechanical		
Overall Dimensions	Length 19.00"	
	Height 5.25"	
	Depth 7.00"	
Weight	Approximately 12 Lbs.	
Input Power	115/230 VAC ±10% 50-400 Hz	
	1.3 Amp @ 115 VAC	
	0.65 Amp @ 230 VAC	
Line Fuse Rating	2 Amp Slo-Blo 3AG	
Output Power	(0 to 50 <sup>0</sup> C)	
	+5VDC @ 3 Amp	
	-5VDC @ 3 Amp	
	+12VDC @ 0.7 Amp	
	-12VDC @ 0.7 Amp	
Derate 2-per cent/ C above 2	50 Celsius	
Voltage Regulation	Line Regulation <u>+</u> .1%	
	Load (0 to Full) +.1%	
Ripple	.1% (typically .5 to 2 mVRMS)	
Response Time	50 Micro-seconds	
Output Voltage Temp. Coefficient	.02%/ C	
Output Short Circuit Protection:		

+5 VDC Supply - Adjustable foldback from 20% to 120% of full load

+12 VDC Supply - Fixed foldback at 250 % full load

## FAMILY SPECIFICATIONS

- o TEMPERATURE Operating: 0° to 65°C (32° to 149°F) Non-Operating: -40° to 85°C (-40° to 185°F)
- HUMIDITY
   to 100% RH Non-condensing
   (Note, extreme low humidity conditions may require special protection against static discharge.)
- o ALTITUDE Operating: Sea level to 20,000 ft. (6096 m) Non-Operating: Sea level to 50,000 ft. (15240 m)
- o VIBRATION 0.1 in (2.5 mm) pp, 5.0 g, 0.036 in (.9 mm) pp, 0.024 in (.6 mm) pp, 60 Hz
- PHYSICAL SPECIFICATIONS Standard Board Envelope 8.5"H x 10.5"L x 0.6"Profile (21.6 cm x 26.7 cm x 1.5 cm)
- o SHOCK 30g, 11 ms, 1/2 sine

1.11

### ORDERING INFORMATION

Number

Description

9680

Communications Adapter Rack -00X Power Supply Requirements -000 No Power Supply -001 +5V @ 3A -002 +5V @ 3A, +12V @ .7A -004 +5V @ 3A, +12V @ .7A



PO, Box 984 • Ann Arbor, Michigan 48106 • Phone: (313) 429-4971 • TWX: 810-223-8153

79

 $1 \le 1$ 





# LSI PACKET NETWORK INTERFACE WD2501/11 SHORT FORM DATA SHEET

#### FEATURES

- · PACKET SWITCHING CONTROLLER COMPATIBLE WITH CCITT RECOMMENDATION X.25, LEVEL 2, LAP (2501) or LAPB (2511)
- · PROGRAMMABLE PRIMARY TIMER (T1) AND RE-TRANSMISSION COUNTER (N2)
- PROGRAMMABLE A FIELD WHICH PROVIDES A WIDER RANGE OF APPLICATIONS THAN DEFINED BY X.25. THESE INCLUDE: DTE-TO-DTE CONNECTION. AND LOOP-BACK TESTING
- DIRECT MEMORY ACCESS (DMA) TRANSFER: TWO CHANNELS; ONE FOR TRANSMIT AND ONE FOR RECEIVE SEND/RECEIVE DATA ACCESSED BY IN-DIRECT ADDRESSING METHOD. NO EXTERNAL AD-DRESS LATCHES REQUIRED. SIXTEEN OUTPUT AD DRESS LINES
- · ZERO BIT INSERT AND DELETE
- AUTOMATIC APPENDING AND TESTING OF FCS . FIELD
- · COMPUTER BUS INTERFACE STRUCTURE: 8 BIT BI-

DIRECTIONAL DATA BUS. CS, WE, RE-FOUR INPUT ADDRESS LINES 8

- DC TO \*300K BITS/SEC DATA RATE
- TTL COMPATIBLE
- 48 PIN DUAL IN-LINE PACKAGES

 HIGHER BIT RATES AVAILABLE BY SPECIAL ORDER APPLICATIONS

X.25 PACKET SWITCHING CONTROLLER PART OF DTE OR DCE PRIVATE PACKET NETWORKS LINK LEVEL CONTROLLER

#### **GENERAL DESCRIPTION**

The WD2501/2511 is a MOS/LSI device which handles bitoriented, full-duplex serial data communications with DMA, which conforms to CCITT X.25 with programmable enhancements.

The device is fabricated in N-Channel silicon gate MOS technology and is TTL compatible on all inputs and outouts.



WD2501/2511 BLOCK DIAGRAM



### INTERFACE SIGNAL DESCRIPTION

PIN NUMBER	SYMBOL	NAME	FUNCTION
48	vcc	Power Suppiy	+ 5VDC power supply input.
42	VDD	Power Supply	+ 12VDC power supply input
18	vss	Ground	Ground
6	CLK	Clock	Clock input used for internal timing. Must be square wave from 1.0 to 3.0 mHz.
7	MR	Master Reset	Initialize on active low. All registers reset to zero, except control bits MDISC and LINK are set to 1. DACK must be stable high before MR goes high.
4	ଞ	Chip Select	Active low chip select for CPU control of I/O registers.
8-15	DALO-DAL7	Data Access Lines	An 8 bit bi-directional three-state bus for CPU and DMA controlled transfers.
5	RE	Read Enable	The contents of the selected register are placed on DAL when CS and RE are low.
3	ŴE	Write Enable	The data on the DAL are written into the selected register when CS and WE are low. RE and WE must not be low at the same time.
2	REPLY	Reply	An active low output to indicate that either a CS•WE or CS•RE input is present.
43	INTR	Interrupt Request	An active low interrupt service request output, and returns high when Status Register #1 is read.
47-44	1 <b>40-1</b> 43	Address Lines In	Four address inputs to the 2501/11 for CPU controlled read/write operation with registers in the 2501/11. If ADRV = 0, these may be tied to A0 - A3.
28-41	A0-A15	Address Lines Out	Sixteen address outputs from the 2501/11 for DMA op- eration. If the control bit ADRV is 1, the outputs are TTL drives at all times. If ADRV is 0, the outputs are 3-state, and are HI-Z whenever DACK is high. (ADRV is in Con- trol Register #1.)
23	DROO	DMA Request Out	An active low output signal to initiate CPU bus request so that 2501/11 can output onto the bus.

*PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
24	DROI	DMA Request in	An active low output signal to initiate CPU bus request so that data may be input to the 2501/11. DRQI and DRQO cannot be low at the same time.
25	DACK	DMA Acknowledge	An active low input from the CPU in response to DRQO or DRQI. DACK must not be low if CS and RE are low or if CS and WE are low.
20	ТD	Transmit Data	Transmitted serial data output
16	RD	Receive Data	Receive serial data input
19	ŤĊ	Transmit Clock	A 1X clock input. TD changes on the falling edge of $\overline{TC}$ .
17	RĈ	Receive Clock	This is a 1X clock input, and RD is sampled on the rising edge of RC.
			Adjustment of the sample is by quandrant. The sampling may be monitored by the RCO output.
21	RTS	Request-To-Send	An open collector (drain) output which goes low when the 2501/11 is ready to transmit either flags or data. May be hard-wired to ground.
22	CTS	Clear-To-Send	An active low input which signals the 2501/11 that transmission may begin. If high, the TD output is forced high. May be hard-wired to ground.
L		l	

\*Pin numbers are preliminary.

Ě





The WD2501/11 is controlled and monitored by sixteen I/O registers. Control, status, and error bits will be referred to as CR, SR, or ER, respectively, along with two digits. For example, SR16 refers to status register #1 and bit 6, which is "XBA."

REG. #	IA3	IA2	IA1	IAO	REGISTER	REGISTER GROUPING
0	0	0	0	0	CRO	
1 1	0	0	0	1	CR1	OVERALL CONTROL
2	lo	0	1 1	0	* SRO	AND
3	1 0	0	1	1 1	'SR1	MONITOR
4	0	1	0	0	• SR2	
5	0	1	0	1	*ER0	
6	0	1	1	0	CHAIN MONITOR	RECEIVER
7	0	1	1	1	* RECEIVED C-FIELD	MONITOR
8	1	0	0	Ō	T1	TIMER
9	1	0	0	1 1	N2/T1	}
A	1	0	1	0	TLOOK H1	1
в	1	0	1	] 1	TLOOK LO	DMA SET-UP
i c	1 1	1	0	0	CHAIN/LIMIT	1
D	1	1	0	1	(UNUSED)	
E	1	1	1	0	XMT COMMAND "E"	"A" FIELD
F	1 1	1	1	1 1	XMT RESPONSE "F"	]

\* CPU READ ONLY. (Write not possible)

Sector Sector

i

---

1.11.12

REGISTER	7	6	5	4	3	2	1	0
CRO	A DISC.	0	HALF/ FULL	ACTIVE/ PASSIVE	LOOP TEST	RAMT	RECR	MDISC
CR1	тхмт•	TRCV*	x۱۰	ADRV	RRT1	0	0	SEND
SRO	NA2	NA1	NAO	RNRR	NB2	NB1	NBO	RNRX
SR1	<sup>1</sup> PKR	<sup>1</sup> XBA	<sup>1</sup> ERROR		NE2	NE1	NEO	
SR	TIOUT	IRTS	REC IDLE				RANC	LINK
ERO	ER07	ER06	ER05	ER04	ER03	ER02	ER01	ER00

### CONTROL, STATUS, ERROR REGISTERS

<sup>1</sup>Causes Interrupt (INTR Goes Low).

ľ

And a second second

A STATE

ŀ

ŀ

Ĩ,

\*Used on 2511, only.

6IT	DESCRIPTION
CROS	Unuesd control bits, like CR06, should remain at 0.
CR04	This bit will cause the 2501/11 to initiate link set-up if CR04 = 1, or to welt for a link set-up from the remote device if CR04 = 0.
CR03	The LOOP TEST bit will connect the transmitted data output to the receiver input. The receiver input pin, RD, is gated-out. The "E" and "F" registers of the A-field should be equal.
CR01	This bit is RECR which defines the CPU's receiver buffer as Ready (CR01 = 1) or as Not Ready (CR01 = 0). (If RECR = 0, this bit indicates that the CPU has a temporary inability to accept more i-frames, or packets, and the 2501/11 will transmit an RNR 8-frame.
CROO	MDISC is a mandatory disconnect command. MDISC will cause a logical disconnect in the DTE/DCE link. No DMA accessed data may be transferred as long as MDISC $\approx$ 1. After Master Reset (MR pin transition from low to high), MDISC will be set. The 2501/11 will neither transmit nor accept received data until MDISC $\approx$ 0.
CR14	The ADRV bit (CR14) is the control for the 16 bit output addresses (AOA15). If ADRV = 0, the outputs are 3-state and are in Hi-2, except when DACK goes low. If ADRV = 1, the outputs are always low impedance (TTL), and are high when DACK is high.

84

---

BIT	DESCRIPTION
CR13	RRT1 will cause the 2501/11 to transmit an RR (RECR = 1) or RNR (RECR = 0) at T1 intervals provided the 2501/11 is not sending a command or waiting for an acknowledgement.
CR10.	The SEND bit (CR10) is used to command the 2501/11 to send the next packet or packets. If SEND = 1, the 2501/11 will read from TLOOK the BRDY bit of the next segment for trans- mission. If BRDY = 0, the 2501/11 will clear SEND and no action occurs. If BRDY = 1, the 2501/11 will then read TSADR and TCNT, followed by the transmission of that buffer. After transmission, the 2501/11 clears BRDY of the segment just transmitted, and reads BRDY of the next segment. If 1, the next segment is transmitted. If 0, the SEND bit is cleared, and trans- mission of packets is stopped.
8R07-SR05*	NA2-NA0. Next block of transmitted data to be Acknowledged.
8R04	RNRR. An RNR has been received.
8R03-8R01*	NB2-NB0. Next block to be transmitted.
SROO	RNPDL As a result of RECR (CR01) = 0, an RNR has been transmitted.
SR17	The PKR bit stands for Packet Received. This means that a packet has been received error-free and in correct sequence according to the received N (S) count. The data (I-field) has been placed in the CPU's RAM memory. NE is advanced.
	The three interrupt-causing bits are SR17, SR16, and SR15. Any of the three will cause an in- terrupt request (INTR goes low) when that bit goes to a 1. After SR1 is read, all three bits are reset to 0, and INTR returns high.
8R16	The XBA bit means that a previously transmitted Block, or Blocks, have been acknowledged by the remote device. Upon acknowledgement, the ACK ED bit is set to "1" for each segment in TLOOK which was acknowledged.
8R15	The ERROR bit indicates: 1) An error has occurred which is not recoverable by the 2501/11, or 2) A significant event has occurred. The "significant events" are: change in link status (link-up or down), the 2501/11 is progressing to the next segment in a chained receive buffer, or one- direction of the link has been reset. The event exture of the reset for the ERBOR bit is change in EBD.
0012.0011	ME2.NE2. Next Expertent particle accordent autober of ELOOK
6827	T10177 bit means that times T1 has times out. This bit returns to 0 when T1 is an elected
	The start of the s
5718)	tents summer for the internet request-to-send on, and indicates that the transmitter is al- tempting (successful or not) to send either data or flags. If the RTS pin is not tied to ground or WIRE-ORED with another signal, then IRTS = RTS.
8R25	REC IDLE indicates that the 2501/11 has received at least 15 contiguous 1's.
8 <b>7</b> 21	RANC means that the Received Address field is Not Correct. Either the A-field was from "E" but should have been "F" or vice verse. A CMDR will be transmitted if link was in the in- formation transfer phase. (2501 ONLY) NOTE: If an A-field is neither "E" nor "F," the entire packet is disregarded and not brought into memory by DMA. No action is taken.
SR20	If the link is established, $LINR = 0$ . If the link is logically disconnected, $LINR = 1$ .

"See "Memory Access Method" Section

ę

111,0

#### ERROR REGISTER (ERO)

ER07	ER06	ER05							
0	0	0	:R00 = NOSFR (2501 only) :R01 = ROR :R02 = TUR :R03 = Not Used :R04 = RLNR						
0	0	1	ER04         ER03         ER02         ER01         ER00           0         0         0         1         LINK is up. (Was down)           1         0         0         0         Received DISC while LINK up.           0         0         1         0         DISC sent, sent SARM sent N2 times without UA.           0         0         1         0         DISC sent, REC IDLE for T1xN2.						
0	1	0	CHAIN STATUS ER00 = GNCS ER01 = CNR						
1	0		LINK RESET RECEIVED if ER05 $\cdot$ ER00 = 000000 LINK RESET TRANSMITTED if ER05 $\cdot$ ER00 = non-zero ER00 similar to W ER01 similar to X ER02 similar to X ER03 similar to Z ER05 means received F = 1, but did not send P = 1 ER05 means t-frame was sent N2 times without acknowledge						
1	1		COMMAND REJECT RECEIVED if ER05 · ER00 = 000000 TRANSMITTED if ER05 · ER00 = non-zero ER00 = W ER01 = X ER02 = Y ER03 = Z ER04 = Z1 (2501 ONLY)						

••• •••

#### NOTES:

1. Whenever a command reject (CMDR) is received, the I-field will have been placed in appropriate memory by DMA, and a link reset SARM will be transmitted. The NB is not advanced.

2. Definitions of W, X, Y, Z as stated in CCITT X.25. Z1 indicates received N(S) is invalid (not part of X.25).

#### TERMS USED IN ERROR REGISTER

GNCS Going to Next Chain Segment

RLNR RLOOK Not Ready. REC RDY bit of next segment is 0.

ROR Receiver Over-Run. The Receiver Register (RR) had a character to load into the FIFO, but the FIFO was full.

- TUR Transmitter Under-Run. The Transmitter Register (TR) needed a character from the Transmitter Holding Register (THR), but the THR was not ready.
- NOSFR No S-frame received for T1 x N2. Used only if RRT1 = 1.

#### MEMORY ACCESS METHOD

The memory access method, which includes DMA, is designed to take full advantage of the bit-oriented protocol which allows up to 7 l-frames to be outstanding (i.e., unacknowledged) in each direction of a communications link. The memory access method used two "look-up" tables: One for transmit and one for receive. These tables contain addresses and control for the individual send/receive packets. Thus, packet data are DMA addressed indirectly. This method is best suited for most software applications.

The 16 bit starting address for the look-up table TLOOK is loaded into the 2501/11 by the CPU. (I/O Registers "A" and "B"). RLOOK must immediately follow TLOOK in contiguous fashion. TLOOK and RLOOK are in the RAM memory external to the 2501/11. There are a total of 8 segmented control sections for each table. Each segment contains eight bytes. Four bytes are used for

data memory starting address and length, two bits of one byte are used for control, one byte defines variable bit length and residual, and the other two bytes are open for user definition.

In transmit, the 2501/11 will have read from TLOOK the starting address and length of the first packet to be transmitted. The 2501/11 will automatically transmit the flag, address, and control fields. Next, the information field data will be transmitted using DMA from the "SEND #0 PACKET" memory. At the end of the information field, the 2501/11 will automatically send the FCS and closing Flag. The 2501/11 will then move on to the next packet.

If retransmission of one or more (up to seven) packets becomes necessary, the 2501/11 will automatically retrace the previous transmissions through the TLOOK table. The user's CPU software does not become involved in the retransmission. However, an ERROR COUNTER is incremented. (See Error Counter Section.)

To receive, each frame is checked for correct address and FCS fields and for type of control field. If the frame is a packet, the information field is placed in the assigned memory location in a method similar to that used in transmit. After the packet is received error-free and in proper N(S) sequence count, an interrupt is generated, and the 2501/11 is ready for the next packet which will be placed in the next location.



#### MEMORY ACCESS SCHEME

#### "DEADLY EMBRACE" PREVENTION

A "deadly embrace" can occur when two processors reach a state where each is waiting for the other. In this case, the two processors are the user's CPU and the micro-controller inside the 2501/11. Therefore, to prevent the "deadly embrace," the following rule is obeyed by the 2501/11 and should also be obeyed by the user's CPU. This rule applies to TLOOK, RLOOK, and to the I/O registers. The Error Counters do not apply to this rule.

RULE: If a bit is set by the CPU, it will not be set by the 2501/11, and vice versa. If a bit is cleared by the 2501/11, it will not be cleared by the CPU, and vice versa.

As an example, the BRDY bit in the TLOOK segment is set by the CPU, only, but cleared by the 2501/11 only.

and significant sure

ないため

**ERROR COUNTERS** 

Following continguously after RLOOK is ten 8-bit error counters. The 2501/11 will increment each counter at the occurrence of the defined event. However, the 2501/11 will not increment past 255 (all 1's). The CPU has the responsibility of clearing each counter. The first counter past RLOOK is #1, etc.

#### ERROR COUNTER

#### COUNT

1344 4 7.50

112

- 1 Received Frames with FCS Error or Aborted
- 2 Received Short Frames (less than 32 bits)
- 3 Number of times T1 ran-out (completed)
- 4 Number of I-Frame Retransmissions
- 5 REJ Frames Received
- 6 REJ Frames Transmitted
- 7 Number of Null Packets Received (2501 ONLY)

BYTE#IN SEGMENT	7	6	5	4	3	2	1	0	
1	ACK'ED			RESER	/ED			BRDY	
2		TSADR HI							
3		TSADR LO							
4	R	ESERVED		TCNT HI					
5		TCNT LO							
6.	SPARE.								
7.	SPARE								
8.	SPARE"								

\* Spare. Must be present, User may use these bytes.

TLOOK SEGMENT

BYTE # IN SEGMENT	7	6	5	4	3	2	1	0	
1	FRCML		RESERVED		RES2	REST	RES0	REC RDY	
2		RSADR HI							
3	RSADR LO								
4	RESERVED				RCNT HI				
5		RCNTLO							
6*	SPARE								
7.	SPARE								
8.	SPARE								

RES2, RES1, RES0 describes number of received residual bits.

\* Spare. User may use these bytes.

#### RLOOK SEGMENT

BRDY means that the transmit buffer is ready. The 2501/11 will send the block only after the CPU makes BRDY = 1. (BRDY is used in conjunction with the SEND bit.) At the completion of the transmission, the 2501/11 will make BRDY = 0, and then read the BRDY of the next segment.

After transmitting a packet, an acknowledgement must be received from the remote device. The acknoledgement is contained in the received N (R) count of an i-frame, RR frame, ORNR frame. Upon acknowledgement, the 2501/11 will make ACK'ED = 1, and generate a block-acknowledged interrupt. Before assigning a new block to a segment in TLOOK, the CPU must make sure that the previous block which used that segment number has been acknowledged.

REC RDY informs the 2501/11 that the receive buffer is ready. The 2501/11 will not receive a packet into a buffer referenced by a particular segment until REC RDY = 1. If the 2501/11 progresses to a segment which has REC RDY = 0, an error interrupt will be generated.

After receiving an error-free packet in proper sequence, the 2501/11 will set FRCML, clear REC RDY, and generate a Packet Received Interrupt. The 2501/11 will also write the value of the binary length of the received packet in RCNT HI and RCNT LO. The NE count is advanced. The 2501/11 will acknowledge received packets at the first opportunity. This will be in either the next transmitted I-frame, or by an RR frame if RECR = 1, or by an RNR frame if RECR = 0. (RECR is in CRO.)

In the address bytes, HI represents the upper 8 bits and LO represents the lower 8 bits. In the count bytes, HI represents the upper 4 bytes.

TSADR is the starting address of the buffer to transmit and TCNT is the binary count of the number of characters in the l-field.

RSADR is the starting address of the receive buffer. After successfully receiving the packets, the 2501/11 will write the value of RCNT which is the binary count of the number of characters in the l-field.

Whether the 2501/11 accesses a look-up table or a memory block a DMA Cycle is required for each access.

#### TLOOK AND RLOOK POINTERS

There are three 3-bit counters for the status of the segments in TLOOK and RLOOK. Status Register #0 (SRO) contains counters NA and NB which are used in conjunction with TLOOK. NB is the segment number of the next block to be transmitted, and is advanced at the end of each DMA transmission. NA is the value of the segment of the next block which will be acknowledged. If all transmitted blocks have been acknowledged, then NA  $\approx$  NB.

In SR1 is a 3-bit counter, NE, used with RLOOK. NE is the value of the segment number where the next received packet will be placed.

# PRELIMINARY TIMING SPECIFICATIONS

فالقان ومستحد تحتاز محتمدين وترجعني معتكما فلنن القرور بالانتقاع والمريز وتركيس وتطلقه ومحموما والانتريز ومرور معلما

2

. 44

SYMBOL	PARAMETER	MIN. (NS)	MAX. (NS)	COMMENT
TAR	Input Address Valid to RE	0		
TRD	Read Strobe (or DACK Read) to Data Valid	200 375		C (DAL) = 50 pf C (DAL) = 100 pf
THD	Data Hold Time from Read Strobe		80	
THA	Address Hold Time from Read Strobe	80		
TAW	Input Address Valid to Trailing Edge of WE	200		
Tww	Minimum WE Pulse	200		
TDW	Data Valid to Trailing Edge of WE or Trailing Edge of DACK for DMA Write	100		
TAHW	Address Hold Time after WE	80		
TDHW	Data Hold Time after WE or after DACK or DMA Write	80		
T <sub>DA1</sub>	Time from DRQO (or DRQI) to Output Address Valid if ADRV = 1		80	C (ADDRESS) = 100 pf
T <sub>DA0</sub>	Time from DACK to Output Address Valid if ADRV = 1		360	C (ADDRESS) = 100 pf
TDD	Time from Leading Edge of DACK to Trailing Edge of DROO (or DROI)	1	200	C (DRQ) = 50 pf
TDAH	Output Address Hold Time from DACK		120	
TDMW	Data Hold Time from DACK for DMA Read	ļ	80	
T <sub>RP1</sub>	REPLY Response Leading Edge		160 240	C <sub>LOAD</sub> = 50 pf C <sub>LOAD</sub> = 100 pf
T <sub>RP2</sub>	REPLY Response Trailing Edge	_	200 260	CLOAD = 50 pf CLOAD = 100 pf









CPU WRITE TIMING (CS IS LOW)



DMA WRITE (AO-A15 SAME AS DMA READ)



WD2501 CERAMIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed

Information furnished by Western Digital Corporation is believed to be accurate and reliable. However, no responsibility is assumed by Western Digital Corporation for its use, nor any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patient or patent rights of Western Digital Corporation. Western Digital Corporation reserves the right to change said circuity at anytime without notice.



TO DS ODDER A RELEIM

91

ł

# APPENDIX C

ŀ,

and the second second

Ę

÷

4

# SERVICE CHANNEL CONTROLLER COST DATA

C.1	Service Channel Controller Cost Derivation: 16 User Ports	93
C.2	Service Channel Controller Cost Derivation: 8 Üser Ports	94
C.3	Special Purpose XYCOM Modules	<b>9</b> 5
C.4	Redundant Service Channel Controller Configuration	96
C.5	Service Channel Network Costs	97

Page

1 1 4 1 4 1 A

1

# Service Channel Controller Cost Derivation XYCOM Hardware 16 User Ports, Non-Redundant

Module Number	Number Used	Description	Cost (\$)
1862+	1	Master Processor	950
1813+	1	Memory Module	1350
1842+	4	Terminal Communication Processor	4780
1897+	1	Cabinet	895
1887+005	1	Power Supply	1295
9672	4	Interface Cable	300
9673	1	Interface Cable	65
9680-004	1	Cabinet	750
9601	4	Interface Adaptor - 20 ma	500
9602	4	Interface Adaptor - MIL-STD-188-100	600
9603	4	Interface Adaptor - MIL-STD-188-114	760
2732	12	32K PROM IC	340
(1849+)	1	High Speed Interface Module	2875
(9690+)	1	Interface Adaptor/Protection Switch	375

15835

-

# Service Channel Controller Cost Derivation XYCOM Hardware 8 User Ports, Non-Redundant

Module Number	Number Used	Description	Cost (\$)
1862+	1	Master Processor	950
1813+	1	Memory Module	1350
1842 <del>+</del>	2	Terminal Interface Processor	2390
1897+	1	Cabinet	895
1887+005	1	Power Supply	1295
9672	2	Interface Cable	150
9673	1	Interface Cable	65
9680-004	1	Cabinet	750
9601	2	Interface Adaptor - 20 ma	250
9602	3	Interface Adaptor - MIL-STD-188-100	450
9603	3	Interface Adaptor - MIL-STD-188-114	570
2732	10	32K PROM IC	280
(1849+)	1	High Speed Interface Module	2875
(9690+)	1	Interface Adaptor/Protection Switch	375
			12645





MICROCOPY RESOLUTION TEST CHART NATIONAL BUREAU OF STANDARDS-1963-A

 $\mathcal{M}_{\mathbf{k}}$ 

# Special Purpose XYCOM Modules

1849+

STREET, ST

Contraction of the second second

High Speed Packet Interface Module Consists of:

Туре	Number	Description	Cost(\$)
1862+	1	Processor	950
1890+	1	Prototype Board	175
WD2511	6	Packet Interface IC	1380
6116	8	16K RAM IC	170
		Miscellaneous ICs	200
			2875

High Speed Interface Adaptor/Protection Switch 9690+ Consists of:

1890+	1	Prototype Board	175
		Miscellaneous ICs	200
			375

9691+	Protection	Switch	
Const	lsts of:		
1890-	- 1	Prototype Board	175
		Miscellaneous ICs	200
			375

# Redundant Service Channel Controller Configuration

Fully Redundant	16	Channels	Cost (\$)
Non-Redundant SCC (9691+)	2 4		31670 1500
			33170
Fully Redundant	8	Channels	
Non-Redundant SCC (9691+)	2 2		25290 750
			26040
Partially Redundant	16	Channels	
Non-Redundant SCC	1		15835
(1849+) 1887+005	1		2875 1295
			20005
Partially Redundant	8	Channels	
Non-Redundant SCC	1		12645
(1849+) 1887+005	1		2875 1295
			16815

96

- 11 (Y -

The second s

# Service Channel Network Costs SCC Implementation

Station Size	Number of Stations	Fully Redundant 16 Channels 8 Channels		Partially Redundant 16 Channels 8 Channels	
1	25	829.3	651.0	500.1	420.4
2	88	2919.0	2291.5	1760.4	1479.7
3	26	862.4	677.0	520.1	437.2
4	11	364.9	286.4	220.1	185.0
5	4	132.7	104.2	80.0	67.3
6	4	132.7	104.2	80.0	67.3
9	1	66.3	52.1	40.0	33.6
10	1	66.3	52.1	40.0	33.6
		5373.6	4218.5	3280.7	2724.1

Cost (\$1000)

and the second second

