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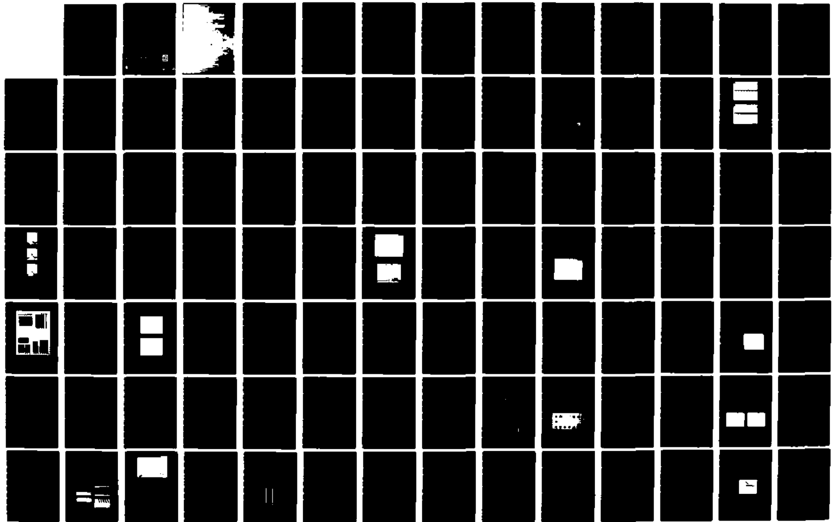

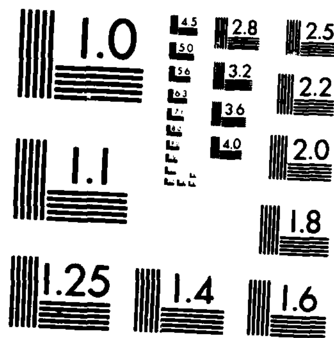

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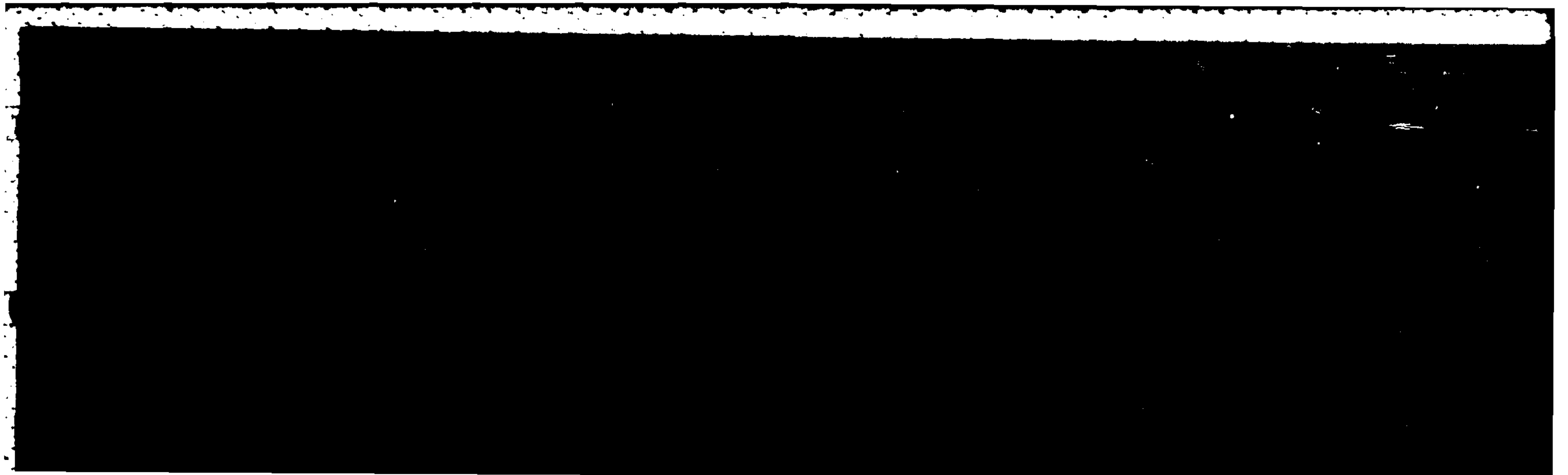

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

SOLID STATE RESEARCH

QUARTERLY TECHNICAL SUMMARY REPORT

1 AUGUST — 31 OCTOBER 1982

ISSUED 11 FEBRUARY 1983

Approved for public release; distribution unlimited.

LEXINGTON MASSACHUSETTS

ABSTRACT

This report covers in detail the solid state research work of the Solid State Division at Lincoln Laboratory for the period 1 August through 31 October 1982. The topics covered are Solid State Device Research, Quantum Electronics, Materials Research, Microelectronics, and Analog Device Technology. Funding is primarily provided by the Air Force, with additional support provided by the Army, DARPA, Navy, NASA, and DOE.

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SUMMARY

1. SOLID STATE DEVICE RESEARCH

An electrooptic analog-to-digital converter has been demonstrated at 1 gigasample per second. This converter uses a $LiNbO_3$ Ti-indiffused waveguide interferometric array for conversion, a pulsed GaAlAs diode laser for sampling, a Si avalanche photodiode for detection of the sampled waveform, and a special 1-GHz Si integrated circuit for digital processing. Individual bit channels of this 2-bit device have been tested by a beat-frequency with a 499.2-MHz test signal. This represents the highest frequency conversion of an analog waveform reported to date.

The optical properties of the integrated optics Y-junction, which can function as a power combiner or power divider, and of the Mach-Zehnder interferometric modulator have been analyzed using the four-port scattering matrix. The interferometric properties of the Y-junction are found to be relatively insensitive to fabrication and design errors of a magnitude that would make the use of the Y-junction in the reverse direction as a 3-dB power divider very marginal.

P-type HgCdTe photoconductors operating at high temperatures have been investigated for wide-bandwidth (>100 MHz) heterodyne and direct detection at 10 µm. Measured 10.6-µm heterodyne sensitivities of 9×10^{-20} W/Hz at 195 K and 1×10^{-17} W/Hz at 300 K and direct sensitivity of 7×10^{-10} $W/Hz^{1/2}$ at 300 K, which are in excellent agreement with a detailed theoretical analysis, are the highest observed for detectors in this temperature range.

2. QUANTUM ELECTRONICS

The $Ni:MgF_2$ and $Co:MgF_2$ transition metal laser systems have been mode-locked. Autocorrelation measurements give a pulse width of 21 ps for $Ni:MgF_2$ and 64 ps for $Co:MgF_2$.

Ultrashort optical pulses of 28- to 55-ps duration have been generated with a GaAlAs laser diode using gain-switched excitation. One of the diode facets was irradiated with protons in order to provide a region of saturable absorption.

Optoelectronic crosscorrelation measurements have been made of the temporal response of proton-bombarded, interdigitated-electrode-structure InP photodetectors. Using a CW mode-locked dye laser producing 3-ps pulses, a typical full-width half-maximum (FWHM) response of 65 ps was found.

Optoelectronic switches have been fabricated from evaporated Si layers, and electrical pulses of less than 40-ps duration have been produced using ultrashort laser pulses for excitation. The switches exhibit a very low dark current and return to their high off-state resistivity in less than 50 ps.

The production of surface ripple structures on semiconductor materials by stimulated polariton scattering has been extended into the vacuum ultraviolet; ripple periods of 65 nm have been produced on Ge using a 157-nm F_2 laser source. The spectral dependence of the ripple period provides information on the optical properties of the dynamic liquid semiconductor layer formed during laser annealing.

The rotational temperature of expanding H_2O vapor has been measured with a heterodyne radiometer by observing the absorption of the 557-GHz transition against a hot background. A carcinotron at 279 GHz was used as the local oscillator in conjunction with a GaAs Schottky diode second-harmonic mixer.

3. MATERIALS RESEARCH

A complementary metal-oxide-semiconductor (CMOS) test circuit chip has been designed for evaluating silicon-on-insulator wafers prepared by using the graphite strip-heater technique for zone-melting recrystallization of polycrystalline Si films on SiO_2-coated Si substrates. High yields of good-quality transistor arrays and ring oscillators have been obtained for test chips fabricated on 2-in.-diam wafers.

Films of GaAs with good electrical properties have been grown by molecular-beam epitaxy at substrate temperatures as low as 380°C. The growth of such films, which has not been achieved previously at substrate temperatures below 500°C, was accomplished by reducing the growth rate.

The formation of high-quality p-n junctions in GaAs by diffusion from a spin-on source has been demonstrated. Small shallow-homojunction solar cells with conversion efficiencies of about 14 percent (AM1) have been fabricated by using the spin-on technique. With further development, this technique may permit the simplified fabrication of high-efficiency cells by making it possible to obtain optimum junction depths without the need for thinning the n^+ layer.

4. MICROELECTRONICS

A 16-stage GaAs Schottky-barrier CCD has been designed and fabricated for a demonstration of optical modulation of radiation near the GaAs bandgap edge. The illumination passes through semitransparent, 100-Å-thick Ti gates into the CCD, where optical absorption is dependent on the electric field in the CCD well and can be modulated by varying the charge content of the well. The required high pinch-off voltage combined with low leakage for the CCD is achieved by using a shallow, semi-insulating region formed by a low-energy proton bombardment at the surface of the CCD channel.

Silicon permeable base transistors have been fabricated which exhibit a maximum gain of 11 dB at 2 GHz and a maximum frequency of oscillation of 10 GHz. A deposited W film is used to form a Schottky-barrier base grid at the bottom of a 3200-Å-period etched square-wave groove structure in the Si, as well as the collector contacts at the Si finger tips.

Protection of photovoltaic modules from the "hot-spot" failure mode caused by cracking or shadowing of a single cell in a series string has been achieved by fabricating an isolated, narrow diode with low breakdown voltage around the periphery of the photovoltaic cell. The reverse bypass protection has been achieved both with a conventional diode at the periphery of the cell

connected in antiparallel and with a peripheral backward diode using standard interconnects.

5. ANALOG DEVICE TECHNOLOGY

Nonvolatile storage of analog-signal levels has been demonstrated in discrete floating-gate memory cells. Signal charge tunnels from the p-silicon substrate through a thin silicon dioxide layer to an insulated island of polysilicon, where it is retained. These cells can be integrated with charge-coupled devices to provide integrated analog-signal storage with retention times of months, better than that provided by dual-dielectric storage cells.

A new concept has been defined and experimentally verified which allows a surface-acoustic-wave chirp-transform adaptive filter system to approximate much more closely a true linear filter for CW inputs than was possible with conventional chirp-transform techniques. Transform systems operate on the input in time segments, a trait which in the past has created spurious segmentation artifacts in the output. The new method, which involves overlapping coherent summation of the time-segmented outputs to effectively cancel the artifacts, makes possible the use of such a system as an adaptive excisor of narrowband interference.

REPORTS ON SOLID STATE RESEARCH

15 August through 15 November 1982

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JA No.			
5184	The Nature of the Initial Transient in the Rate of Formation of Nickel Carbonyl	H. Mazurek* R.S. Mehta* M.S. Dresselhaus* G. Dresselhaus* H.J. Zeiger	Surf. Sci. 118, 530 (1982)
5313	Transient Annealing of Selenium-Implanted Gallium Arsenide Using a Graphite Strip Heater	R.L. Chapman J.C.C. Fan J.P. Donnelly B-Y. Tsaur	Appl. Phys. Lett. 40, 805 (1982)
5335	Pulse-Pumped Operation of Divalent Transition-Metal Lasers	P.F. Moulton	IEEE J. Quantum Electron. QE-18, 1185 (1982)
5343	Quantum Electronics at Lincoln Laboratory	P.L. Kelley	Laser Focus 18, 28 (August 1982) and 18, 32 (September 1982)
5346	Low-Dislocation-Density GaAs Epilayers Grown on Ge-Coated Si Substrates by Means of Lateral Epitaxial Overgrowth	B-Y. Tsaur R.W. McClelland J.C.C. Fan R.P. Gale J.P. Salerno B.A. Vojak C.O. Bozler	Appl. Phys. Lett. 41, 347 (1982)
5347	High-Speed Ultraviolet- and X-Ray-Sensitive InP Photoconductive Detectors	T.F. Deutsch F.J. Leonberger A.G. Foyt D. Mills*	Appl. Phys. Lett. 41, 403 (1982)
5352	Graphoepitaxy of Germanium on Gratings with Square-Wave and Sawtooth Profiles	M.W. Geis B-Y. Tsaur D.C. Flanders	Appl. Phys. Lett. 41, 526 (1982)
5354	Deep-Ultraviolet Spatial-Period Division Using an Excimer Laser	A.M. Hawryluk* H.I. Smith* R.M. Osgood* D.J. Ehrlich	Opt. Lett. 7, 402 (1982)
5361	Limitations of Signal Averaging Due to Temporal Correlation in Laser Remote-Sensing Measurements	N. Menyuk D.K. Killinger C.R. Menyuk*	Appl. Opt. 21, 3377 (1982)
5362	Analysis of Integrated-Optics Near 3 dB Coupler and Mach-Zehnder Interferometric Modulator Using 4-Port Scattering Matrix	R.H. Rediker F.J. Leonberger	IEEE J. Quantum Electron. QE-18, 1813 (1982)
5365	Simultaneous Formation of a Shallow Silicon p-n Junction and a Shallow Silicide/Silicon Ohmic Contact by an Ion Implantation Technique	B-Y. Tsaur C.H. Anderson	Appl. Phys. Lett. 41, 877 (1982)

* Author not at Lincoln Laboratory.

JA No.			
5369	Spatial Light Modulation Using Electroabsorption in a GaAs Charge-Coupled Device	R.H. Kingston B.E. Burke K.B. Nichols F.J. Leonberger	Appl. Phys. Lett. 41, 413 (1982)
5370	Lateral Epitaxial Overgrowth of GaAs by Organometallic Chemical Vapor Deposition	R.P. Gale R.W. McClelland J.C.C. Fan C.O. Bozler	Appl. Phys. Lett. 41, 545 (1982)
5377	Time-Resolved Measurements of Stimulated Surface Polariton Wave Scattering and Grating Formation in Pulsed-Laser-Annealed Germanium	D.J. Ehrlich S.R.J. Brueck J.Y. Tsao	Appl. Phys. Lett. 41, 630 (1982)
5378	2-Bit 1 Gsample/s Electrooptic Guided-Wave Analog-to-Digital Converter	R.A. Becker F.J. Leonberger	IEEE J. Quantum Electron. QE-18, 1411 (1982)
5388	Orientation Selection by Zone-Melting Silicon Films Through Planar Constrictions	H.A. Atwater* H.I. Smith* M.W. Geis	Appl. Phys. Lett. 41, 747 (1982)

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MS No.			
5766	Effects of Interface Structure on the Electrical Characteristics of PtSi-Si Schottky Barrier Contacts	B-Y. Tsaur D.J. Silversmith R.W. Mountain C.H. Anderson, Jr.	Thin Solid Films 93, 331 (1982)
5891	Dry Etching of Gold Using SF_6	S.M. Cabral M.E. Elta A. Chu L.J. Mahoney	The Electrochemical Society Extended Abstracts 82-1, Montreal, Canada, 9-14 May 1982, Abstract 216, p. 348
5892	Orientation Selection by Zone-Melting Silicon Films Through Planar Constrictions	H.I. Smith* H.A. Atwater* M.W. Geis	The Electrochemical Society Extended Abstracts 82-1, Montreal, Canada, 9-14 May 1982, Abstract 159, p. 257
5893	The Mechanism of Orientation of Si Graphoepitaxy Using a Strip-Heater Oven	H.I. Smith* M.W. Geis	The Electrochemical Society Extended Abstracts 82-1, Montreal, Canada, 9-14 May 1982, Abstract 155, p. 249
6023A	Si Damage Induced by Dry Etching	S. Pang D.D. Rathman D.J. Silversmith R.W. Mountain P.D. DeGraff	The Electrochemical Society Extended Abstracts 82-2, Detroit, Michigan, 17-22 October 1982, Abstract 184, p. 289

* Author not at Lincoln Laboratory.

UNPUBLISHED REPORTS

Journal Articles

JA No.			
5334	Metal/Si and Silicide/Si Interfaces	B-Y. Tsaur J.M. Mayer*	Accepted as Chapter in Ion-Beam-Induced Silicide Formation (McGraw-Hill, New York)
5357	A Two-Stage Monolithic IF Amplifier Utilizing a Ta_2O_5 Capacitor	A. Chu L.J. Mahoney M.E. Elta W.E. Courtney M.C. Finn W.J. Piacentini J.P. Donnelly	Accepted by IEEE Trans. Microwave Theory Tech.
5375	Be-Implanted GaInAsP/InP Double Heterojunction Laser Diodes	J.P. Donnelly J.N. Walpole Z.L. Liau	Accepted by IEEE J. Quantum Electron.
5383	External Cavity Controlled Operation of a Semiconductor Diode Gain Element in Series with an Optical Fiber	R.H. Rediker R.P. Schloss D. Welford A. Mooradian	Accepted by IEEE J. Quantum Electron.
5386	High-Voltage Two-Dimensional Simulations of Permeable Base Transistors	G.D. Alley	Accepted by IEEE Trans. Microwave Theory Tech.
5390	Transmission Electron Microscopy of GaAs Grown over Submicrometer Period Tungsten Gratings	B.A. Vojak J.P. Salerno	Accepted by Appl. Phys. Lett.
5392	Rate of Ethylene Hydrogenation on $Ni_{1-x}Cu_x$ Catalysts - Effects of Magnetic Ordering	H.J. Zeiger B. Wasserman* M.S. Dresselhaus* G. Dresselhaus*	Accepted by Surf. Sci.
5406	Thin-Film Transistors Fabricated in Solid-Phase-Recrystallized Si Films on Fused Silica Substrates	B-Y. Tsaur J.C.C. Fan G.W. Turner M.W. Geis D.J. Silversmith R.W. Mountain	Accepted by J. Appl. Phys.
5407	SOI/CMOS Circuits Fabricated in Zone-Melting-Recrystallized Si Films on SiO_2-Coated Substrates	B-Y. Tsaur J.C.C. Fan R.L. Chapman M.W. Geis D.J. Silversmith R.W. Mountain	Accepted by IEEE Electron Devices Lett.
5411	IR Detectors: Heterodyne and Direct	D.L. Spears	Accepted for publication in special issue of collected papers in Optical and Laser Remote Sensing (Springer-Verlag, New York)
5415	Q-Switched Semiconductor Diode Lasers	D.Z. Tsang J.N. Walpole	Accepted by IEEE J. Quantum Electron.

* Author not at Lincoln Laboratory.

Meeting Speeches*

MS No.	Title	Authors	Meeting
5707I	Laser Fabrication of Microstructures: Physical Mechanisms of High Resolution Processing	D.J. Ehrlich J.Y. Tsao	1982 Annual Mtg. of Materials Research Society, Boston, 1-4 November 1982
6081	UV Laser Initiated Formation of Si_3N_4	T.F. Deutsch D.J. Silversmith R.W. Mountain	
6084	Submicrometer-Linewidth Laser Doping	J.Y. Tsao D.J. Ehrlich	
6087	Surface Electromagnetic Waves in Laser Material Interactions	D.J. Ehrlich S.R.J. Brueck J.Y. Tsao	
6092	Optical Microanalysis of Small Semiconductor Structures	D.V. Murphy S.R.J. Brueck	
6108	Pulsed Laser Doping of Semiconductors	T.F. Deutsch	
6183	Applications of Laser Direct-Write Processes to Electronic Device Fabrication	J.Y. Tsao D.J. Ehrlich D.J. Silversmith R.W. Mountain	
5905A	Photorefractive Effects in Optical Waveguides	A. Lattes† H.A. Haus† F.J. Leonberger	Electronics Division, American Ceramic Society, Cambridge, Massachusetts, 14 September 1982
6059	$LiNbO_3$ Guided-Wave Interferometric Modulators	F.J. Leonberger	
5934	Thin Films of III-V Compounds and Their Applications	J.C.C. Fan	CNRS Intl. Colloq. on Polycrystalline Semiconductors, Perpignan, France, 2-4 September 1982
5943A	Progress in Laser Sources for Remote Sensing	A. Mooradian P.F. Moulton N. Menyuk	1982 Mtg. of IRIS Specialty Group on Active Systems, White Oak, Silver Spring, Maryland, 7 October 1982
5949	Reduction of Photovoltaic Cell Reverse Breakdown by Using a Peripheral Bypass Diode	C.H. Cox D.J. Silversmith R.W. Mountain	16th IEEE Photovoltaic Specialists Conf., San Diego, California, 28 September - 1 October 1982
5972	Growth and Characterization of Oriented GaAs Bicrystal Layers	J.P. Salerno R.W. McClelland J.C.C. Fan P. Vohl C.O. Bozler	
5999	Efficient GaAs/Ge/Si Solar Cells	B-Y. Tsaur J.C.C. Fan G.W. Turner F.M. Davis R.P. Gale	

* Titles of Meeting Speeches are listed for information only. No copies are available for distribution.

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MS No.			
6002	Junction Formation in GaAs Shallow-Homojunction Solar Cells by the Use of Spin-On Diffusion Sources	G.W. Turner B-Y. Tsaur J.C.C. Fan F.M. Davis R.P. Gale M.K. Connors	16th IEEE Photovoltaic Specialists Conf., San Diego, California, 28 September - 1 October 1982
6008	Optimal Design of High-Efficiency Tandem Cells	J.C.C. Fan B-Y. Tsaur B.J. Palm	
5976B	Entrainment of Subboundaries in Zone-Melting Recrystallized Si Films	M.W. Geis H.I. Smith* B-Y. Tsaur J.C.C. Fan D.J. Silversmith R.W. Mountain	1982 SOS/SOI Technology Workshop, Provincetown, Massachusetts, 5-7 October 1982
6118	Zone-Melting Recrystallization of Si Films on Insulators for Integrated Circuit Applications	B-Y. Tsaur J.C.C. Fan M.W. Geis R.L. Chapman G.W. Turner D.J. Silversmith R.W. Mountain	
6017	Millimeter Wavelength GaAs Permeable Base Transistors	G.D. Alley C.O. Bozler N.P. Economou D.C. Flanders M.W. Geis G.A. Lincoln W.T. Lindley R.W. McClelland R.A. Murphy K.B. Nichols W.J. Piacentini S. Rabe J.P. Salerno B.A. Vojak	Device Research Conf., Colorado State University, Ft. Collins, Colorado, 21-23 June 1982
6034	MeV Ion Implanted Boron Layers in Silicon	E.W. Maby	Ion Beam Modification of Materials Conf., Grenoble, France, 6 September 1982
6051	Q-Switched Semiconductor Diode Lasers	D.Z. Tsang J.N. Walpole	8th Annual Intl. Semiconductor Laser Conf., Ottawa, Canada, 15 September 1982
6054	GaInAsP/InP Heterostructure Laser Mirrors Formed by a Transport and Etching Technique	Z.L. Liau J.N. Walpole	
6067	Laser Photochemical Processing for Microelectronics	D.J. Ehrlich T.F. Deutsch R.M. Osgood, Jr.* D.J. Silversmith	Intl. Conf. on Solid State Devices, Tokyo, Japan, 24-26 August 1982

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MS No.			
6078	Excitation of Surface Optical Waves and Material Ripples by Stimulated Scattering	S.R.J. Brueck D.J. Ehrlich J.Y. Tsao	1982 Annual Mtg. of Optical Society of America, Tucson, Arizona, 18-22 October 1982
6088	Laser Photochemistry in Adsorbed Surface Layers	J.Y. Tsao V. Daneu D.J. Ehrlich	
6085	Lateral Epitaxial Overgrowth of GaAs and GaAlAs by Organometallic Chemical Vapor Deposition	R.P. Gale R.W. McClelland J.C.C. Fan C.O. Bozler	1982 Intl. Symp. on GaAs and Related Compounds, Albuquerque, New Mexico, 19-22 September 1982
6095	RF Magnetron Sputtering of ZnO for SAW: Effects of Magnetic Field Strength and Configuration	A.C. Anderson D.E. Oates	1982 Ultrasonics Symp., San Diego, California, 27-29 October 1982
6096	Adaptive CW Filtering by Chirp Transformation Using Overlap Summation	D.R. Arsenault	
6097	Wideband Analog Signal Processing with Superconductive Circuits	S.A. Reible	
6106	Preparation of High-Quality Silicon Films on Insulators by Zone-Melting Recrystallization	J.C.C. Fan	Seminar, Centre National d'Etudes des Telecommunications, Grenoble, France, 6 September 1982
6109	Crystal Growth and Characterization of HEM-Grown Co:MgF_2 for Laser Application	C.P. Khattak* F. Schmid* P.F. Moulton	Big Sky Laser Conf., Big Sky, Montana, 17-19 August 1982
6110	Advanced SAW-Based Signal Processing for Packet Communications	J.H. Cafarella	1982 MILCOM Conf., MITRE Corporation, Bedford, Massachusetts, 17-20 October 1982
6112	Single Mode Waveguide Submillimeter Frequency Multiplication and Mixing	N.R. Erickson* H.R. Fetterman	4th High Temperature Plasma Diagnostics Topical Conf., M.I.T., 25-27 August 1982
6114	Integrated Optical Devices for Temperature Sensing	L.M. Johnson F.J. Leonberger G.W. Pratt, Jr.*	1st Intl. Congress on Applications of Lasers and Electrooptics, Boston, 23 September 1982
6124	High Resolution Parallel Transfer Lithography	D.C. Flanders	SEMICON East, Boston, 22 September 1982
6136	Low-Threshold Heterostructure Lasers	J.N. Walpole Z.L. Liau	Triservice Workshop on Fiber Optic Sensors and Guided Wave Technology, Ft. Eustis, Virginia, 5-8 October 1982
6140	An Investigation of GaAs Films Grown by MBE at Low Substrate Temperatures and Growth Rates	G.M. Metze A.R. Calawa	4th Annual Molecular Beam Epitaxy Workshop, Urbana, Illinois, 21-22 October 1982

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MS No.			
6144	Lateral MBE Growth of GaAs over Tungsten	A.R. Calawa B.A. Vojak G.M. Metze M.J. Manfra W.D. Goodhue	4th Annual Molecular Beam Epitaxy Workshop, Urbana, Illinois, 21-22 October 1982
6171	Optoelectronic Signal Processing Devices	F.J. Leonberger	Electron Device Activities in Western New York, Rochester, New York, 19 October 1982
6171A	Optoelectronic Signal Processing Devices	F.J. Leonberger	Seminar, University of Rochester, Rochester, New York, 18 October 1982
6180	Electrooptical Device Research at Lincoln Laboratory	F.J. Leonberger	Seminar, Bell Labs, Allentown, Pennsylvania, 26 October 1982
6182	Spectral Properties of Semiconductor Lasers	A. Mooradian	EECS/RLE Seminar Series on Optics and Quantum Electronics, M.I.T., 20 October 1982

ORGANIZATION

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ANALOG DEVICE TECHNOLOGY

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MICROELECTRONICS

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1. SOLID STATE DEVICE RESEARCH

1.1 2-BIT 1-GIGASAMPLE-PER-SECOND ELECTROOPTIC GUIDED-WAVE ANALOG-TO-DIGITAL CONVERTER

We previously reported results on a 4-bit $LiNbO_3$ guided-wave electro-optic A/D converter which operated at 828 MS/s and used a mode-locked Nd:YAG laser as the source of the short optical pulses (see Ref. 1). Here we report a 2-bit device which operates at 1 GS/s and uses a compact GaAlAs diode laser as the source of the short optical pulses. In addition, we also report on improved fabrication techniques for interconnecting the modulators.

The 2-bit A/D converter consists of a comb-generator-driven GaAlAs diode laser,[2] a $LiNbO_3$ Ti-indiffused waveguide interferometric modulator array, a Si avalanche photodiode (APD), wideband DC-coupled amplifiers, and a special 1-GHz Si integrated circuit consisting of a comparator and a 1-to-8 serial-to-parallel (S/P) converter. The comb-generator-driven diode laser emits <120-ps-wide pulses at a 1000-MHz rate. This A/D converter is depicted in Fig. 1-1(a).

The $LiNbO_3$ chip is shown schematically in Fig. 1-1(b). Two interferometric modulators are fed in parallel from a common input via a branching circuit. Y-splitters with 1° branching angles and isolated 0.5° bends are used in the branching circuit as well as in the modulators. DC bias electrodes are included for each modulator to allow for adjustment of any imbalance in the interferometers and to allow for the application of a static $\pi/2$ phase shift to one of the modulators to obtain a Gray code output.

The wire interconnects shown in Fig. 1-1(b) are schematic. The RF signal to be digitized and a DC bias are actually applied to the two modulators via the two-level metallization scheme[3] shown in Fig. 1-2. Figure 1-2(a) is a photomicrograph showing the modulator electrodes and one of the contact strips that distribute the RF signal to the two modulators. Figure 1-2(b) shows an edge view which illustrates how the contacting is accomplished. A SiO_2 layer is used to insulate the contact strips from the

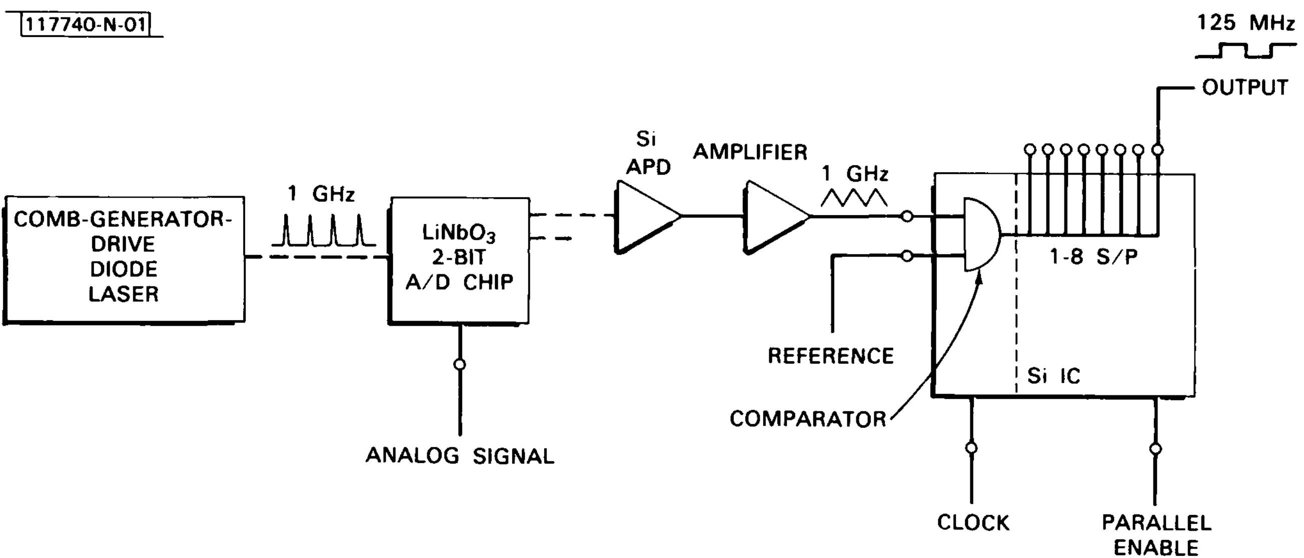

Fig. 1-1(a). Schematic diagram of guided-wave electrooptic A/D converter.

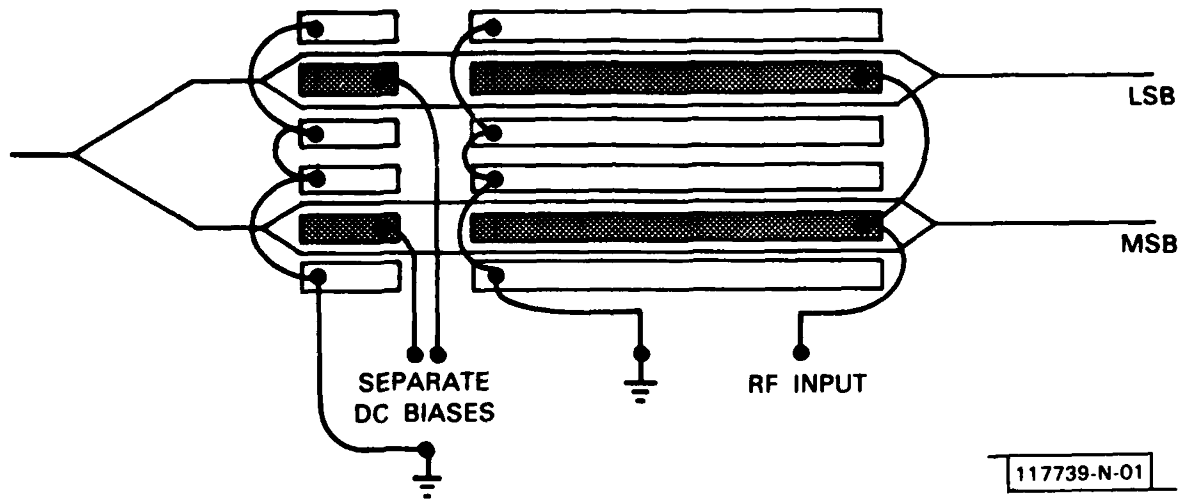

Fig. 1-1(b). Schematic diagram of $LiNbO_3$ guided-wave interferometer array for A/D converter. Waveguides are shown by thin lines. Separate DC biases can be applied to each modulator, and RF signal is applied to all modulators in parallel.

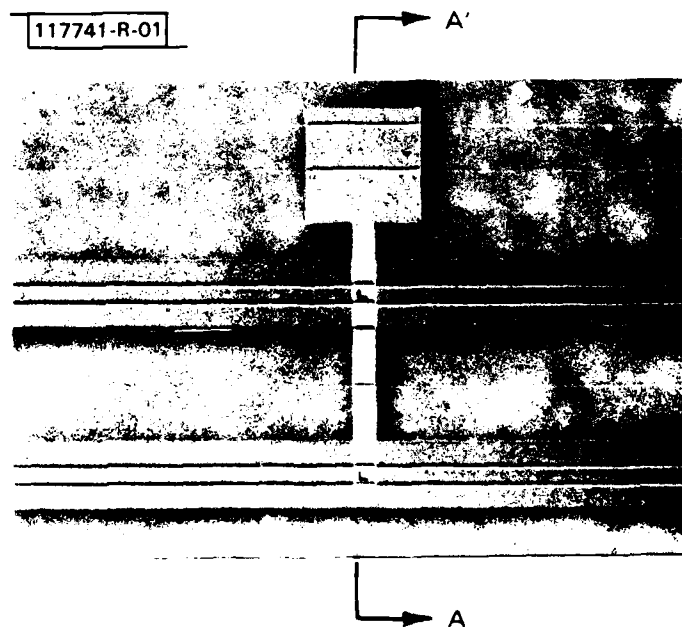

Fig. 1-2(a). Photomicrograph of modulator electrodes and contact strips. Contact is being made in regions where small indented squares are visible.

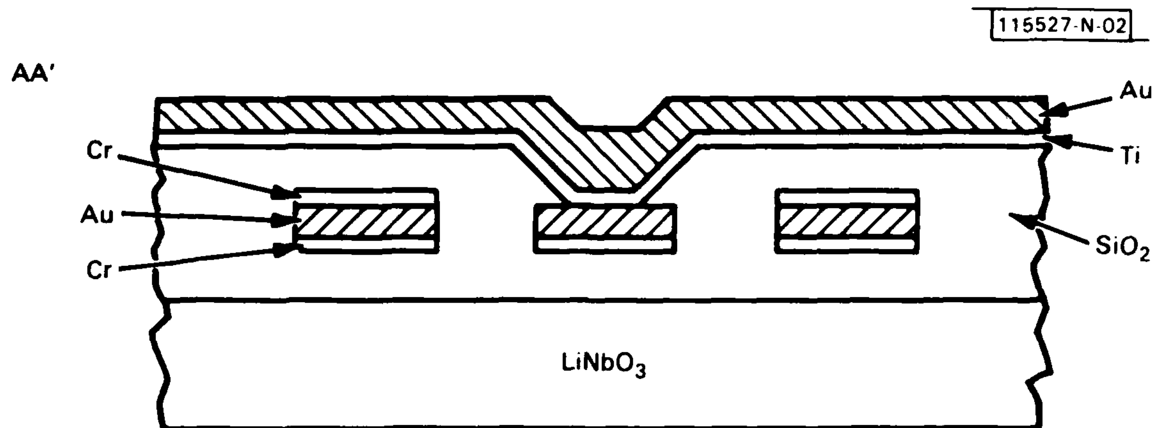

Fig. 1-2(b). Sketch showing use of SiO_2 layer for isolation of two metal layers except where windows in SiO_2 have been opened and contact is allowed.

modulator electrodes except in the regions where windows in the oxide are opened and electrical contact is made. This method allows the RF signal to be delivered to more than one modulator without incurring large inductive losses that might otherwise be present. Although initially only one pair of contact strips has been used, multiple strips could be useful in reducing the effect of finite electrode resistance.[3] The contact strips are connected to 50-Ω striplines via very short wires.

The A/D converter was tested using low-frequency ramp signals and high-frequency sinusoids. The A/D converter response to the ramp drive was very similar to the response reported in Ref. 1, as was expected. The high-speed operation of this A/D converter was demonstrated using beat-frequency tests performed at 1000 MS/s. This is a standard test used on conventional high-speed A/Ds which allows the maximum frequency input signals to be applied

while the device output is monitored at a relatively low frequency. A sinusoidal test signal which was 800 kHz less than one-half the diode-laser sampling pulse rate was applied to the device. Each successive sample of the analog test signal is of opposite polarity (i.e., differing by slightly less than π radians), and every other sample differs slightly in phase. The output of the interferometer is a frequency-modulated signal when the input signal is a sinusoid. If both arms of the interferometer are DC biased in phase, then the interferometer output is an even function of the input signal, and the response of the interferometer to the negative and positive portions of the input sinusoid will be the same. This is the case for the least-significant bit (LSB). However, if the two arms of the interferometer have a $\pi/2$ phase shift between them, then the output will be an odd function of the input. Thus, the response of the modulator to negative and positive portions of the input sinusoid will have opposite polarity. This is the case for the most significant bit (MSB). The S/P converter following the comparator was enabled on every eighth pulse, and two of the parallel channels (Nos. 1 and 8) were monitored.

The results of the beat-frequency test for the LSB at 1000 MS/s are shown in Fig. 1-3(a). The upper trace is an 800-kHz signal, which was derived by mixing the 499.2-MHz test signal with one-half the diode laser's 1000-MHz drive signal. The 800-kHz signal was used to trigger the oscilloscope. The second trace shows the detector output; the envelope of these detected pulses has the expected FM modulated form. The lower traces show the corresponding comparator outputs for channels 1 and 8 of the S/P converter. These comparator outputs are in phase with each other, as is expected.

Figure 1-3(b) is an oscillogram showing the beat-frequency test results for the MSB at 1000 MS/s. Note that for this bit a DC bias equivalent to a $\pi/2$ phase shift is also applied along with the test signal. As in the case of the LSB data, the top trace is an 800-kHz signal used to trigger the oscilloscope. The second trace shows the detector output. Note that the detector output consists of two signals which are 180° out of phase with each other. The lower traces show the corresponding comparator outputs for channels 1 and 8. In this case the comparator outputs are 180° out of

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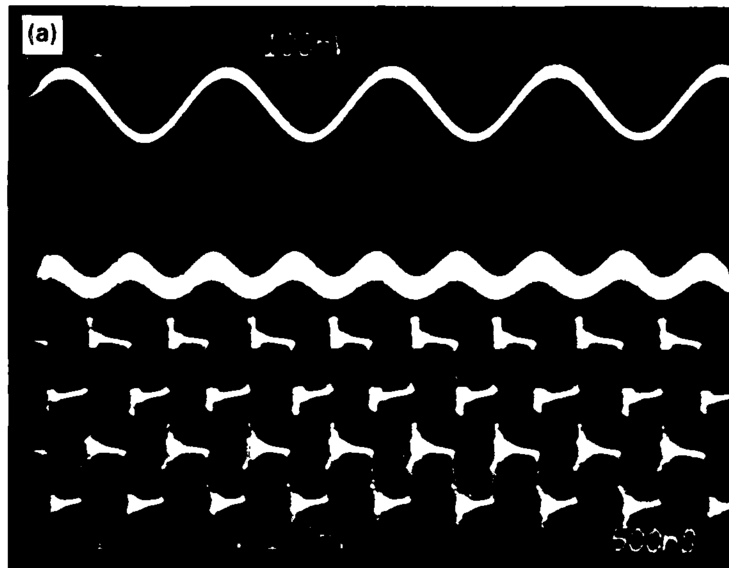

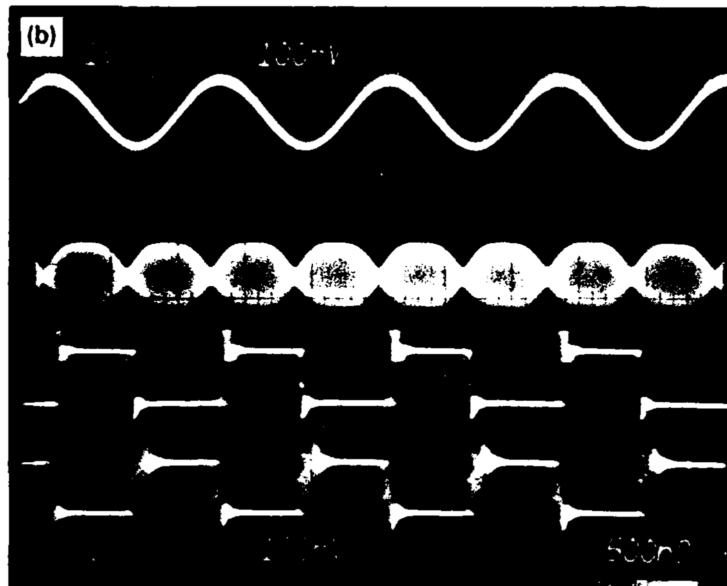

Fig. 1-3. Beat-frequency test of electrooptic A/D converter. Input RF test signal frequency is 499.2 MHz, sampling rate is 1 GHz. Shown are a derived beat signal (top trace), detector output (second trace), and comparator outputs (bottom two traces) for (a) least-significant bit, and (b) most-significant bit. Relative phase of beat signal has not been synchronized to that of detector and comparator.

phase with each other, as is expected, which conclusively demonstrates that the system is performing at the 1000-MHz sampling rate. In this experiment, an externally derived DC signal was used for the comparator reference.

Future development of this device includes optimization of the modulator RF circuit and full bit testing to properly assess conversion accuracy.

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1.2 ANALYSIS OF INTEGRATED-OPTICS Y-JUNCTION AND MACH-ZEHNDER INTERFEROMETRIC MODULATOR USING FOUR-PORT SCATTERING MATRIX

The scattering matrix formalism for a lossless four-port device has been used to describe the performance of the integrated-optics Y-junction and of the guided-wave Mach-Zehnder interferometric modulator which makes use of such junctions. In addition to the ports for the three single-mode dielectric guides forming the Y-junction, a fourth port is incorporated (shown in Fig. 1-4) which takes all the power radiated out of the guided-wave system in the vicinity of the junction. The properties of the scattering matrix of the lossless four-port network - that the matrix is both symmetrical and unitary - are used to advantage to obtain unknown matrix coefficients from those that are known _a priori_, which permits the complete determination of the optical outputs from the Y-junction for arbitrary combinations of inputs.

The interferometric properties of the Y-junction are found to be relatively insensitive to fabrication and/or design errors of a magnitude which would make the use of this junction in the reverse direction as a 3-dB power divider very marginal. A Y-junction with an extinction ratio as an interferometer better than -26 dB corresponds to a power divider which couples 22-percent more power into one arm than the other. The Y-junction used as the output of a Mach-Zehnder interferometric modulator, such as shown in Fig. 1-5, is also similarly insensitive to the inequality of power in the two arms.

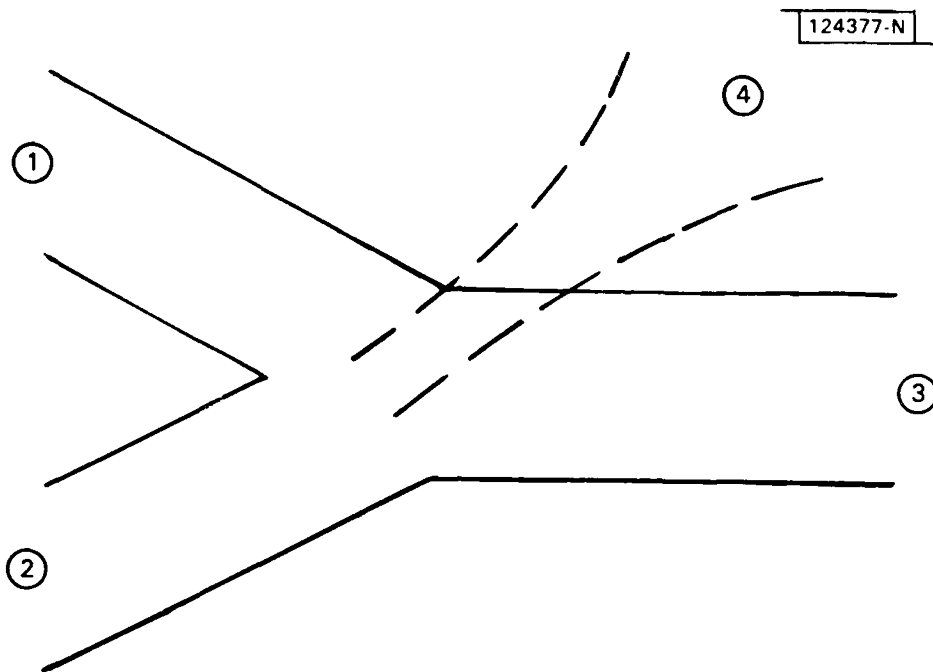

Fig. 1-4. Four-port representation of a Y-junction of single-mode dielectric waveguides. Fourth port takes all power radiated out of guided-wave system in vicinity of Y-junction for input power at port 1 and/or port 2.

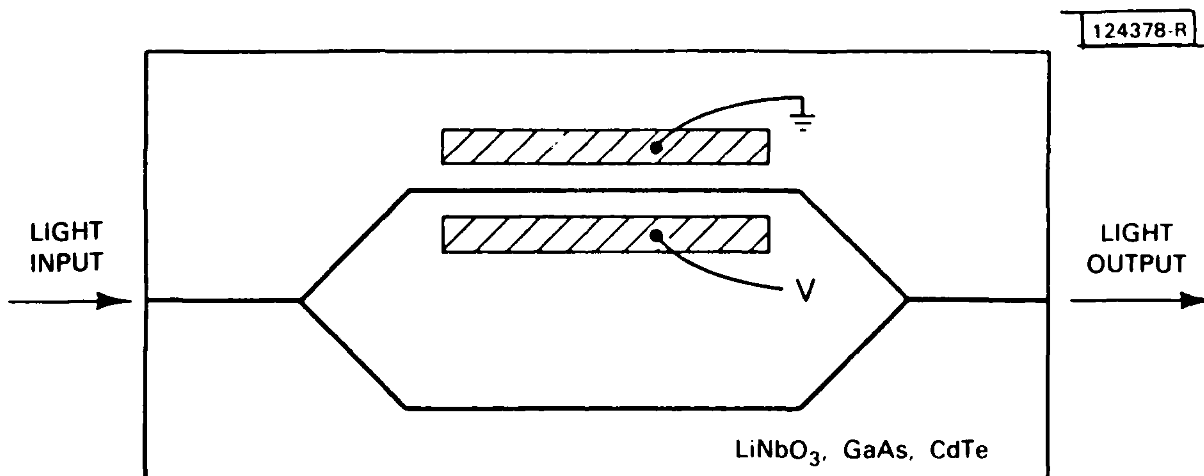

Fig. 1-5. Guided-wave Mach-Zehnder interferometric modulator.

The maximum-to-minimum ratio of the output of the Mach-Zehnder interferometric modulator is shown in Fig. 1-6 as a function of the imbalance factor δ of its output Y-junction. This factor is defined in terms of the output Y-junction being operated in the reverse direction as a power divider, in which case it would couple $1/2(1 + \delta)$ of the input power into one arm and $1/2(1 - \delta)$ of the input power into the other arm. The parameter for the different curves in Fig. 1-6 is the factor Δ which characterizes the inequality in the power from the two interferometer arms to the output Y-junction. This power inequality factor is defined so that the ratio of the power in the two inputs to the output Y-junction is $(1 + \Delta)/(1 - \Delta)$. Contributions to Δ include unequal splitting in the interferometer input Y-junction and differential loss in the two interferometer arms.

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1.3 HETERODYNE AND DIRECT DETECTION AT 10 μm WITH HIGH-TEMPERATURE p-TYPE HgCdTe PHOTOCONDUCTORS

An investigation of p-type HgCdTe photoconductors operating at 200 K for use as CO_2 laser photomixers was reported previously.[4] Here we report an extension of this work which includes a detailed theoretical analysis of HgCdTe photoconductors for direct and heterodyne detection at 10.6 μm, taking into account recent data on the carrier concentration and alloy composition dependence of the optical absorption coefficient[5] and Auger lifetime,[6] as well as heating due to the bias power and local oscillator (LO) power. Maximum performance and optimum device parameters have been established. Devices fabricated using these guidelines have shown the highest reported wide-bandwidth direct and heterodyne sensitivities in the 200 to 300 K temperature range. These sensitivities are in agreement with our calculations.

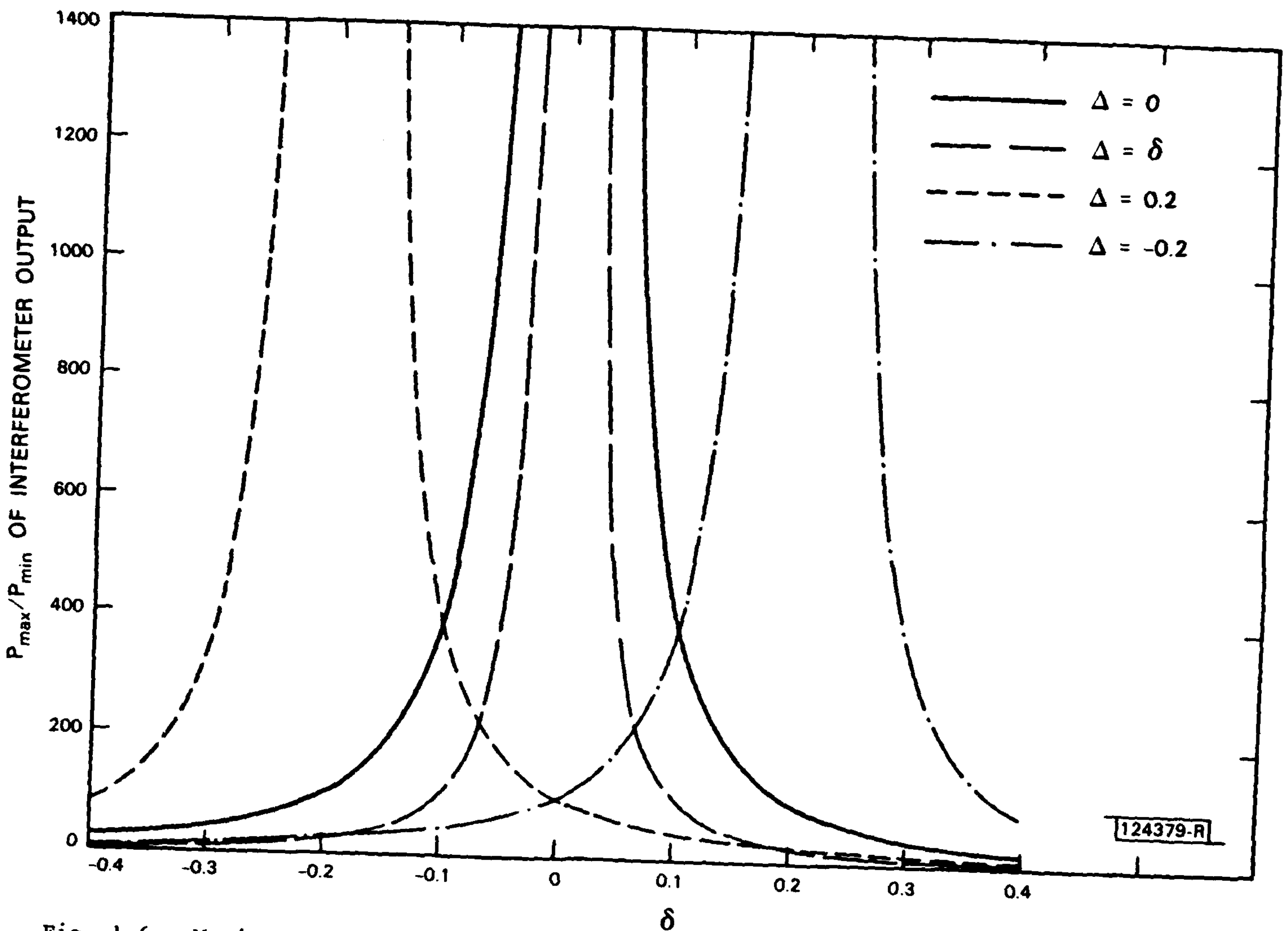

Fig. 1-6. Maximum-to-minimum ratio of output of Mach-Zehnder interferometric modulator as a function of imbalance parameter δ of Y-junction with Δ as parameter. δ is defined in terms of this junction being operated in reverse direction as a power divider, in which case it would couple $1/2(1 + \delta)$ of input power into one arm and $1/2(1 - \delta)$ of input power into other arm. Parameter Δ used to determine various curves is defined so that ratio of power in two inputs to output coupler is $(1 + \Delta)/(1 - \Delta)$.

The sensitivity of a photoconductor is determined by its responsivity and noise level. Johnson (JN) noise, determined by the resistance, dominates at low-bias voltages where the sensitivity is proportional to bias. At high bias, generation-recombination (GR) can become the major noise source. In GR-noise-limited operation the detectivity (D^*) is independent of bias and proportional to the quantity $(\alpha\tau_i/n_i)^{1/2}$, where α is the optical absorption coefficient, τ_i is the intrinsic Auger lifetime, and n_i is the intrinsic carrier concentration, which are all functions of CdTe alloy composition and temperature. In Fig. 1-7 we show $\alpha\tau_i/n_i$ at 10.6 μm as a function of alloy composition at various temperatures from 200 to 325 K. The Kane theory, fit to our absorption data[5] with an exponential phonon tail added, was used to calculate α. Recent published expressions for n_i (Ref. 6) and τ_i (Ref. 7) were used. As expected, there is a different optimum alloy composition for each temperature, ranging from 15 percent at 325 K to 19 percent at 200 K. The numbers in parentheses are the intrinsic Auger lifetimes in units of nanoseconds for the optimum alloy at each temperature. These short lifetimes make it difficult to achieve GR-noise-limited operation before bias-associated heating degrades the performance.

GR-noise-limited operation in direct detection and LO-noise-limited operation in heterodyne detection are more easily achieved with p-type HgCdTe than with intrinsic or n-type HgCdTe because (a) the low mobility of holes gives higher resistivity and lower JN noise, (b) the Auger recombination process is weaker in p-type material,[6] and (c) α is higher in p-type HgCdTe near the absorption edge because of less conduction bandfilling. In Fig. 1-8 we show the ratios of GR to JN noise, D^* to intrinsic D^* (D_i^*) in the GR-limit, LO to JN noise, and LO to GR noise relative to intrinsic HgCdTe as a function of p/n_i for the 16.5-percent alloy at 250 K. The fall-off in the enhancement factor at high values of p/n_i is due to the $1/p^2$ dependence of the lifetime in heavily doped p-type HgCdTe (Ref. 6). From Fig. 1-8 we see that GR-noise-limited operation in direct detection and LO-noise-limited operation heterodyne detection are most readily achieved when p is about $2n_i$,

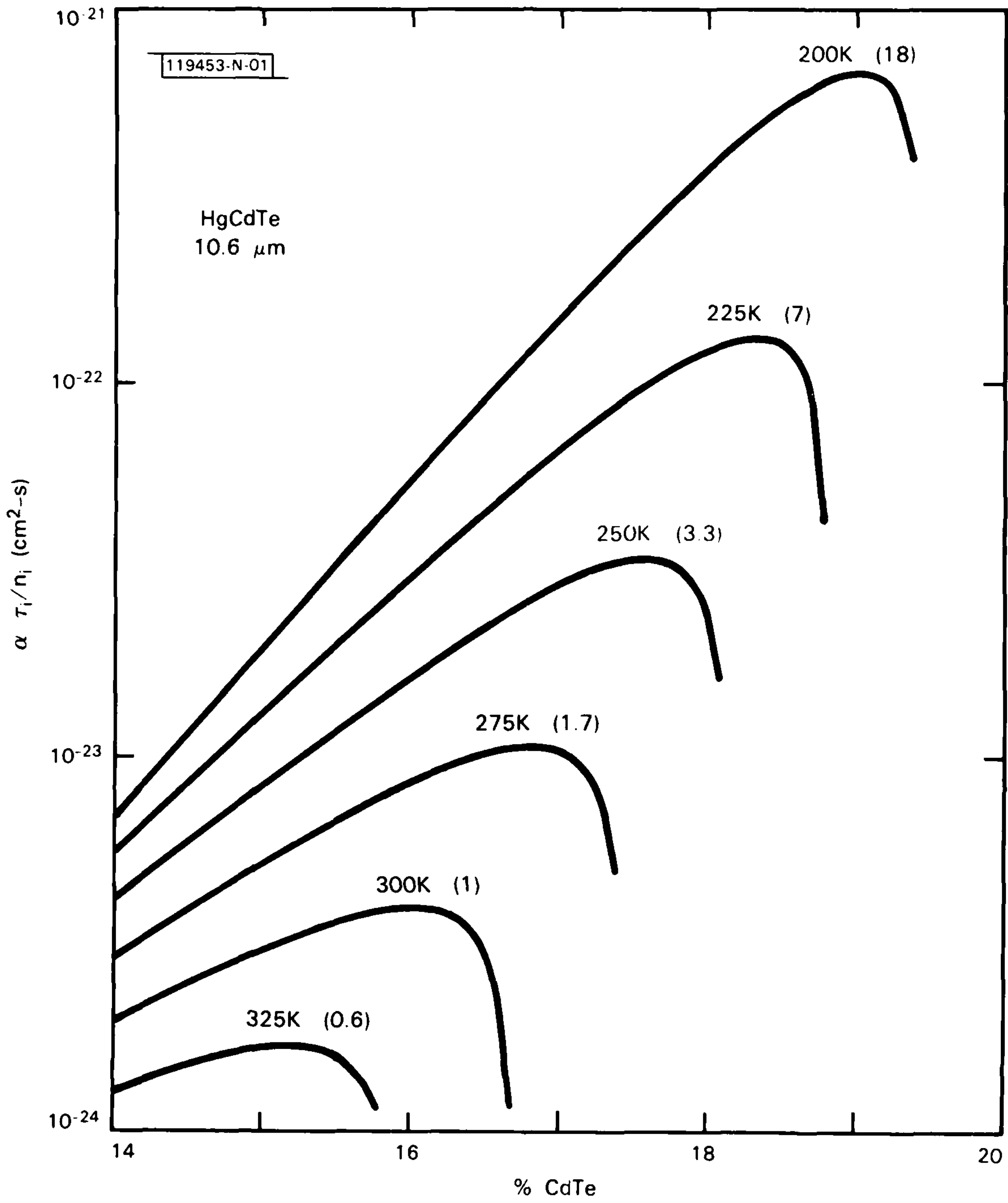

Fig. 1-7. Photoconductor parameter $\alpha\tau_i/n_i$ as a function of CdTe alloy composition at different temperatures.

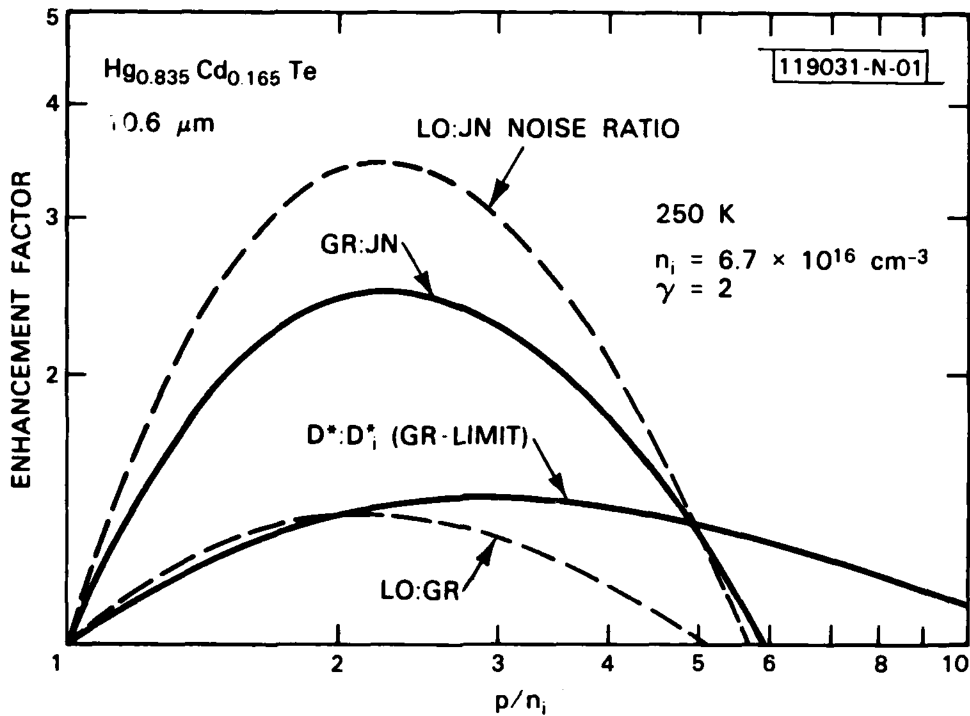

Fig. 1-8. Noise ratios and D* enhancement factors as a function of p/n_i.

and here there is a 50-percent improvement in the GR-noise-limited D* over that of intrinsic HgCdTe. Similar calculations were carried out for 200 and 300 K, and in all cases optimum performance occurred when $p \approx 2n_i$.

Figure 1-9 shows calculated direct detection NEP_D as a function of bias power at 300 K along with reported data[8] for 1- and 300-mm-diam devices and our data for an 80-μm-diam photoconductor. The upturn in NEP_D at high bias powers is a consequence of heating. The calculated NEP_D approaches the GR-noise limit (indicated by the dashed line) only for very small-area devices, where power can be more efficiently dissipated. The theoretical calculations provide a very good fit to the maximum sensitivities measured for these devices. The 80-μm-diam device (although not fully optimized) has the lowest reported NEP_D (7×10^{-10} W/Hz$^{1/2}$) and the highest measured responsivity (1.5 V/W with 20 mW of bias power) of any wideband (500-MHz) room-temperature 10.6-μm detector.

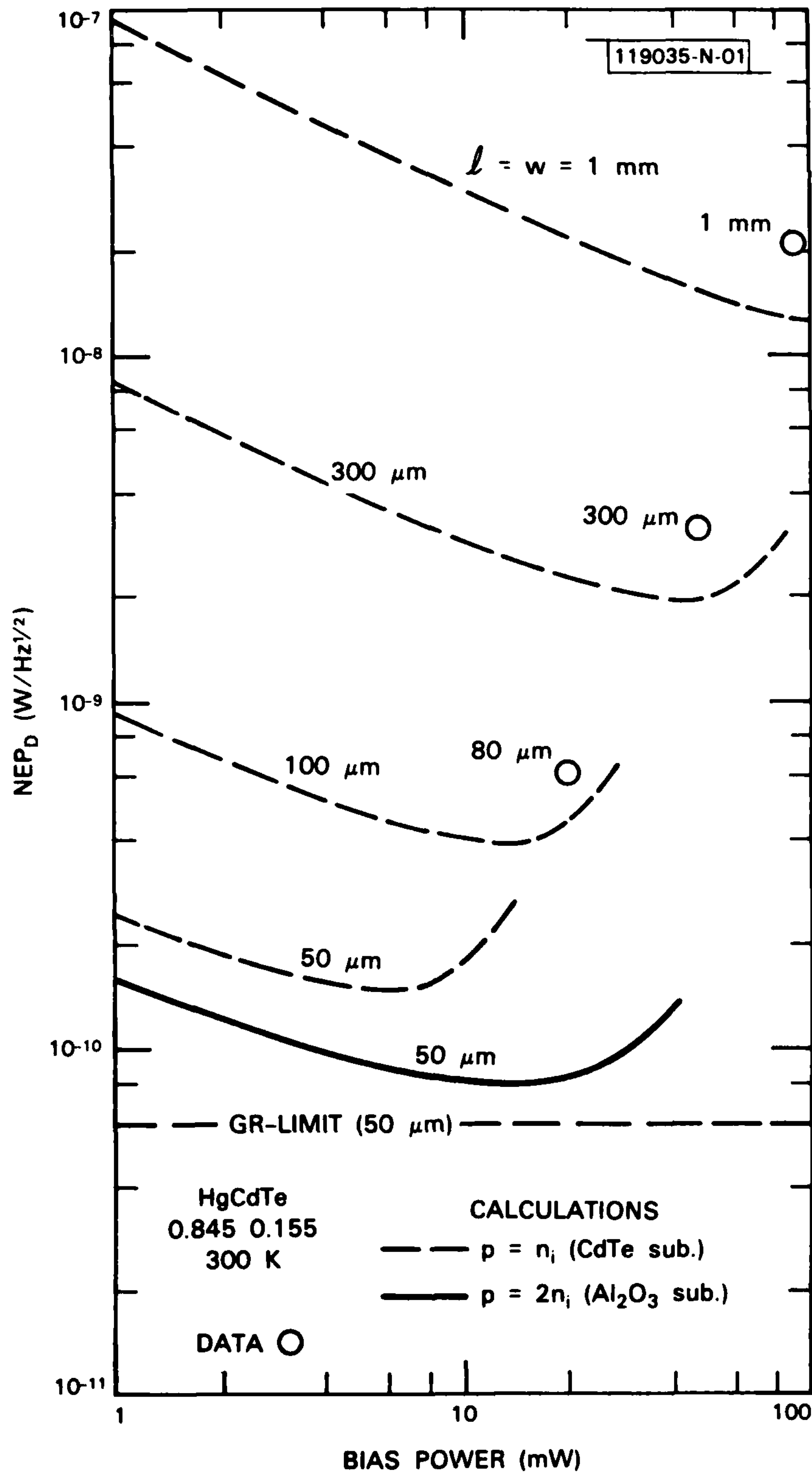

Fig. 1-9. Calculated and measured direct detection NEP_D as a function of bias power at 300 K.

In Fig. 1-10 we show the minimum heterodyne NEP_H we have obtained at 10.6 μm as a function of photoconductor bandwidth B at 77, 195, and 300 K. The best sensitivities at 77 K and at 195 K are in good agreement with those calculated for optimized 100-MHz-bandwidth devices. The value of 9×10^{-20} W/Hz at 195 K is the best reported NEP_H for a 10.6-μm photomixer operating in this temperature region. At very wide bandwidths (>500 MHz), NEP_H varies as B^2, as expected for JN-noise-limited devices. However, none of these devices was fully optimized for 300 K operation, so that with further development we expect to obtain $NEP_H < 1 \times 10^{-18}$ W/Hz at 300 K with 500-MHz bandwidth.

Cooling power is an important consideration for many potential systems applications of these photomixers. Figure 1-11 shows the calculated NEP_H at 100 MHz as a function of required power (bias power plus LO power) times the cooling power factor for state-of-the-art thermoelectric coolers.[9] Maximum performance with minimum power occurs when the bias and LO powers are equal, which is assumed in these calculations. At low powers, NEP_H is approximately the same at all three temperatures because the decreased HgCdTe photomixer performance with increasing temperature is offset by improved TE cooler performance. The two data points for a device tested at 195 K fit the 200 K curve quite well. Figure 1-11 suggests that with a device optimized for 250 K operation, an $NEP_H = 2 \times 10^{-19}$ W/Hz could be obtained with 1/3 the power required for 200 K operation, because between 200 and 250 K the increase in TE cooler performance is much greater than the loss in photoconductor performance. With this low power requirement (~3 mW bias, ~3 mW LO, and ~36 mW cooling), small linear arrays of TE-cooled photomixers appear quite feasible.

D.L. Spears

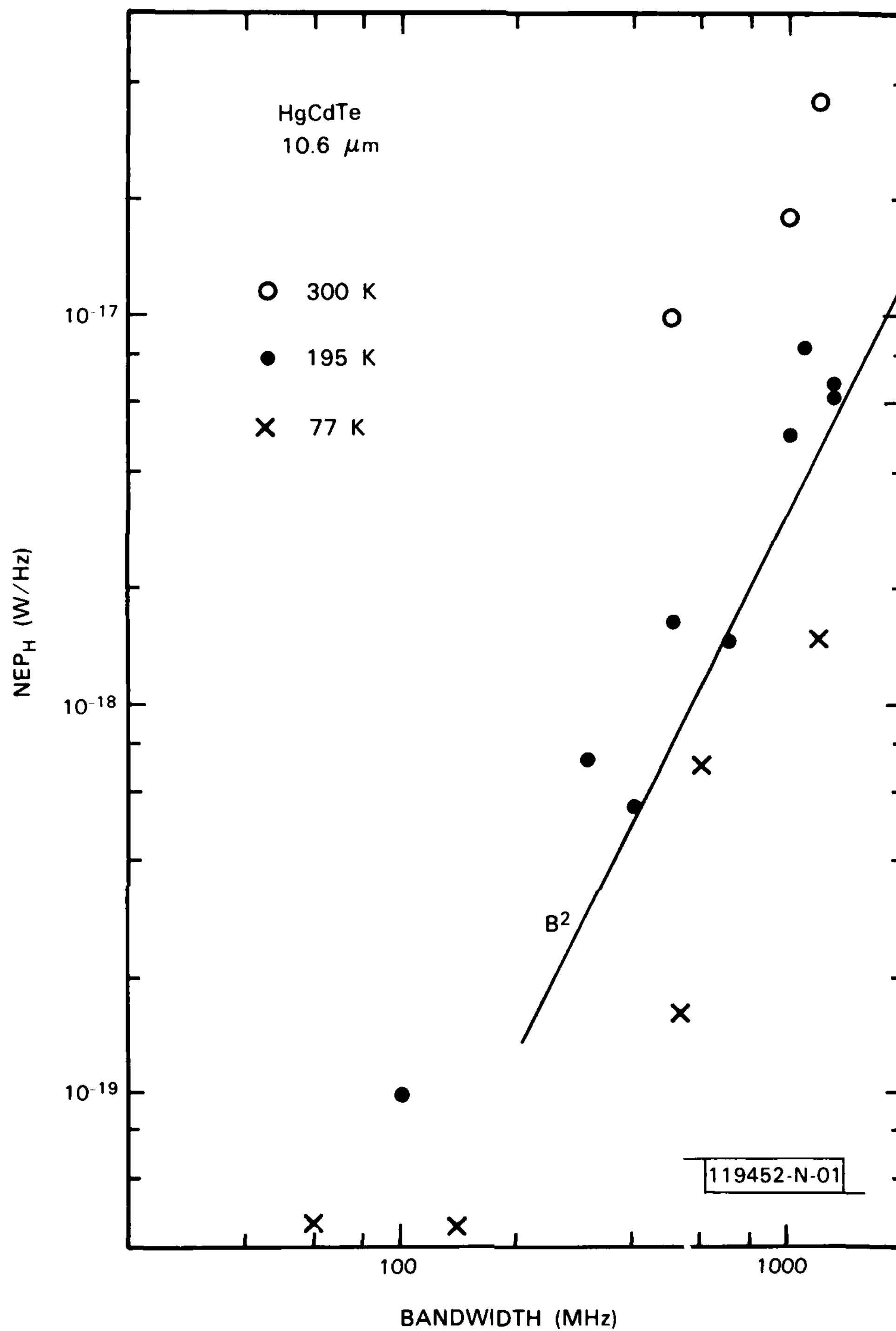

Fig. 1-10. Measured NEP_H as a function of bandwidth for HgCdTe photoconductors at 77, 195, and 300 K. Solid line indicates a B^2 dependence.

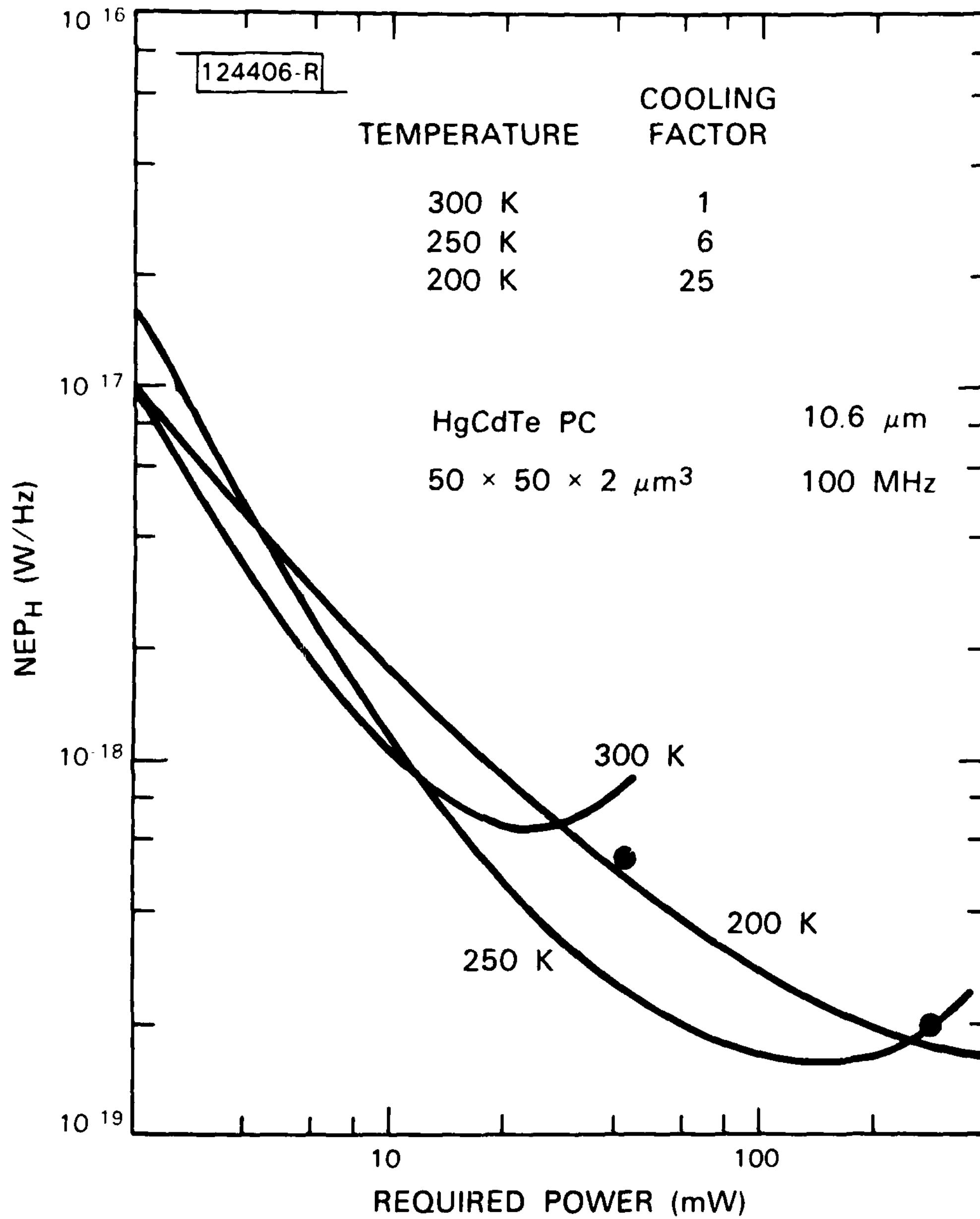

Fig. 1-11. Calculated and measured photoconductor NEP_H at 10.6 μm as a function of required power (bias, LO, and cooling) for 200, 250, and 300 K operation. Data points are for 195 K.

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2. QUANTUM ELECTRONICS

2.1 MODE-LOCKING OF TRANSITION METAL LASERS

Following the preliminary study of a mode-locked Ni:MgF_2 laser,[1] both Ni:MgF_2 and Co:MgF_2 systems have been mode-locked, and autocorrelation pulse-width measurements have been made. Active mode-locking was performed using an acoustooptic loss modulator placed near the output coupler of a three-mirror cavity.

The pulse widths have been measured by the autocorrelation technique (apparatus shown in Fig. 2-1). The train of mode-locked pulses is split into two pulse trains by the beamsplitter and return mirrors, and translation of one of the return mirrors produces a variable time shift. Second-harmonic radiation is produced by the $LiIO_3$ crystal and is detected by the photomultiplier; since the second-harmonic intensity is proportional to the square of the incident fundamental intensity, the second-harmonic signal is greatest when the pulse trains temporally overlap and fall off to a background level when there is no overlap. The physical measurement corresponds mathematically to the autocorrelation function of the pulse intensity profile. An autocorrelation trace of pulses from a mode-locked Ni:MgF_2 laser is shown in Fig. 2-2. The autocorrelation width of 30 ps indicates a pulse duration of ~21 ps assuming a Gaussian pulse shape as predicted by active mode-locking theory. Similarly, 64-ps pulses have been measured in a Co:MgF_2 laser.

Future work will involve demonstration of continuously tunable mode-locked operation through the whole tuning range of these lasers, and a study of pulse-width-limiting mechanisms.

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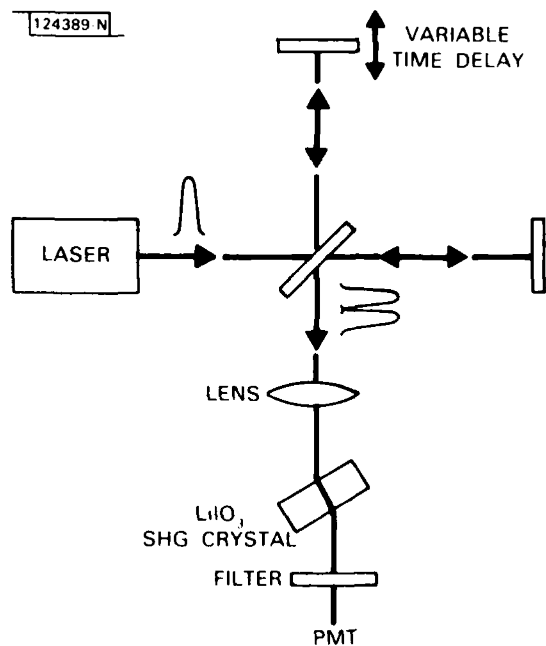

Fig. 2-1. Autocorrelation measurement apparatus.

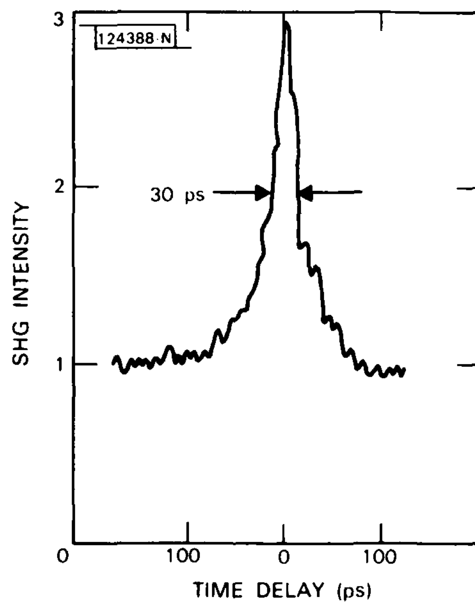

Fig. 2-2. Autocorrelation measurement of Ni:MgF_2 laser pulse width.

2.2 PICOSECOND OPTICAL PULSE GENERATION WITH GaAlAs LASER DIODES

Picosecond optical pulses have been generated with a GaAlAs laser diode using gain switching as the excitation technique. One of the diode facets was irradiated with 400-keV protons in order to produce a region of saturable absorption, which has been found to shorten optical pulses produced in mode-locked external cavity diode lasers. The laser diode was DC-biased below its threshold for CW lasing, and a train of 80-ps-long current pulses generated with the help of a comb generator was injected using a bias T. The comb generator containing a step recovery diode was driven at a RF frequency of 476 MHz.

The laser diode pulses were detected by using a high-speed InP pin photodetector and a sampling oscilloscope. Figure 2-3(a) shows a laser pulse obtained at a DC current of I_o = 46 mA. The 150-ps width of the observed pulse represents the time resolution of the photodetector. At higher DC injection currents, multiple pulses are emitted, as shown in Fig. 2-3(b) and (c). The separation between the first and second pulse decreases with increasing DC current.

A SHG (second-harmonic generation) autocorrelator was used to measure the width of the ultrashort optical pulses. Figure 2-4 is an autocorrelation trace of a pulse at I_o = 46 mA. The achievable time delay of the scan was limited to approximately 180 ps by the 1-in. travel length of the translation stage of the autocorrelator. The autocorrelation trace consists of a pedestal which is superimposed by a series of sharp spikes. These coherence spikes indicate the presence of more than one randomly phased longitudinal mode and are separated by 8 ps, which corresponds to the round-trip time of the 300-μm-long laser diode. The pedestal has a full-width at half-maximum (FWHM) of 41 ps; if one assumes a Gaussian pulse shape, the pulse width is estimated to be 29 ps.

At higher DC injection currents, when more than one pulse is emitted, the autocorrelation traces are dominated by a strong central peak which is the sum of the self-autocorrelations of the pulses. Additional peaks result from the cross-correlation of the multiple pulses and occur when the

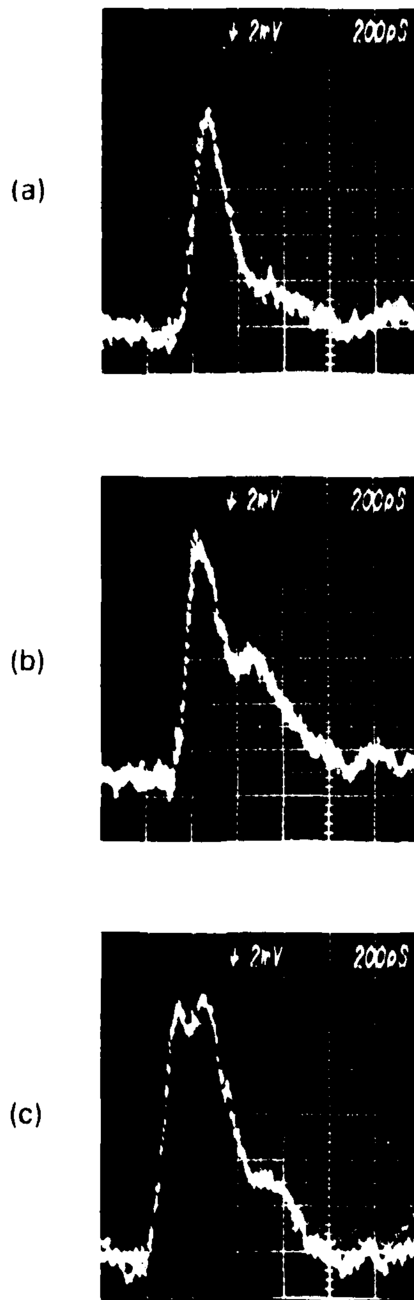

Fig. 2-3. Sampling oscilloscope traces of laser diode pulses detected with a high-speed avalanche photodiode. DC injection current I_o was set to (a) 46 mA, (b) 50 mA, and (c) 60 mA.

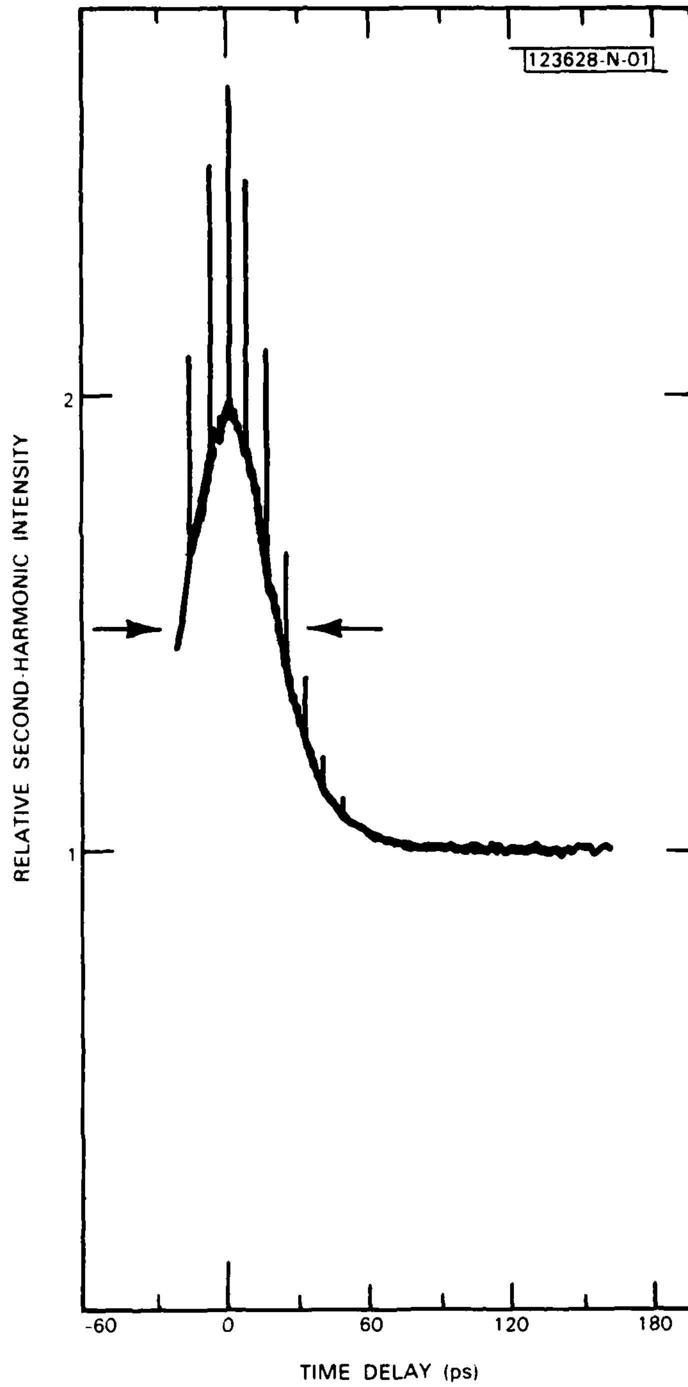

Fig. 2-4. SHG autocorrelation trace of a laser pulse obtained with I_o = 46 mA.

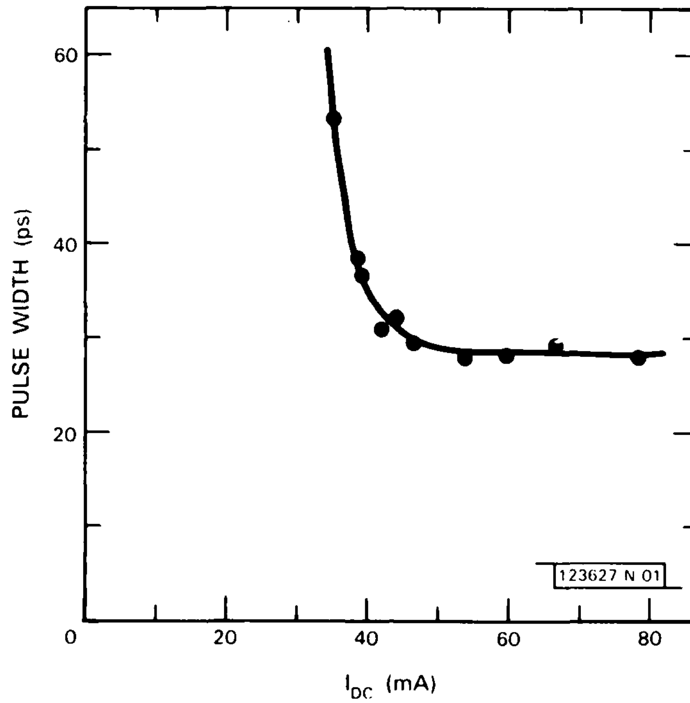

Fig. 2-5. Laser pulse width as a function of the DC injection current.

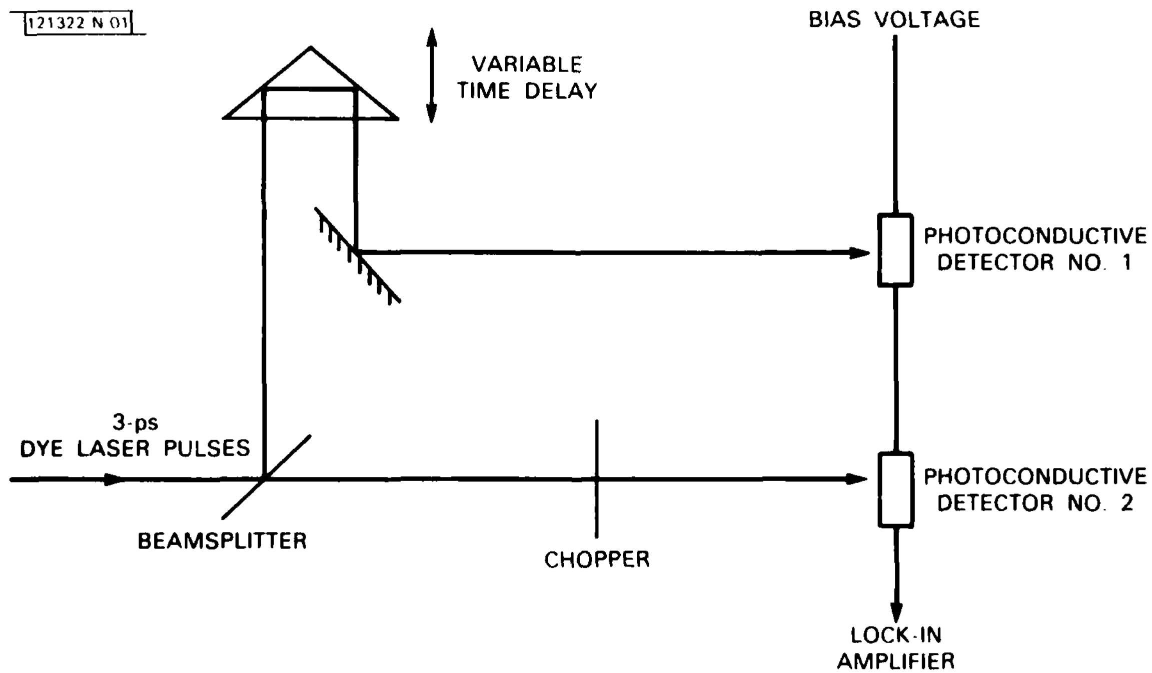

Fig. 2-6. Experimental arrangement for cross-correlation measurements of photodetectors.

correlation delay time corresponds to the pulse separation. The duration of the emitted laser pulses was measured as a function of the DC current I_o, and the result is shown in Fig. 2-5. For $I_o > 54$ mA, where multiple pulses are observed, the pulse width derived from the central autocorrelation peak was plotted. Note that the 29-ps pulse shown in Fig. 2-4 was obtained at I_o = 46 mA, which is below the onset of multiple pulses.

Further investigations are under way to study the influence on the laser pulse width of variations in the energy and dose of the proton bombardment.

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V. Diadiuk
J.D. Woodhouse

2.3 CORRELATION MEASUREMENTS OF PICOSECOND InP PHOTODETECTORS

The use of a conventional sampling oscilloscope (~25-ps rise time) and a mode-locked dye laser (3-ps FWHM pulse duration) to measure the response time of fast photodetectors becomes increasingly inaccurate as the detector response decreases below 100 ps. The implementation of a cross-correlation technqiue, analogous to nonlinear optical autocorrelation techniques, has made it possible to achieve a temporal resolution of 6 ps. The cross-correlation is illustrated in Fig. 2-6; one photodetector is DC-biased, while the transient output in response to a laser pulse is used to bias the second photodetector. The second photodetector acts as a sampling gate for the response signal of the first, the time of sampling being determined by the relative time delay τ between the arrival of the pulse at detector No. 1 and the arrival at detector No. 2. The laser pulse repetition rate was 250 MHz, allowing the use of phase-sensitive detection to measure the integrated charge output of the detectors as a function of the relative pulse time delay. If the outputs of the two photoconductors are $V_1(t)$ and $V_2(t)$, the measured charge $Q(\tau)$ is proportional to the cross-correlation of the two outputs:

$$Q(\tau) \propto \int_{-\infty}^{+\infty} V_1(t)\, V_2(t + \tau)\, dt$$

The devices studied were a pair of proton-bombarded (10^{13} cm^{-2} at 200 keV) InP detectors with a 48 × 48 μm^2 active area composed of 2-μm-wide and 2-μm-spaced interdigital electrodes.[2] The laser was a synchronously mode-locked oxazine 1 dye laser operating at 750 nm, generating 3 ps (FWHM) duration pulses. Figure 2-7 shows the cross-correlation measurement of the detectors; it includes the autocorrelation of the laser pulses to illustrate the 6-ps resolution limit of the technique.

The shape of the correlation either side of zero time delay between pulses is essentially the same for the first 70 to 80 ps; for larger time delays one detector remains fast, while the other exhibits a slow trailing-edge response. Both detectors appeared to be similar when used with a sampling oscilloscope, where the poorer signal-to-noise ratio and package ringing effects obviously obscured the slow trailing edge seen with the

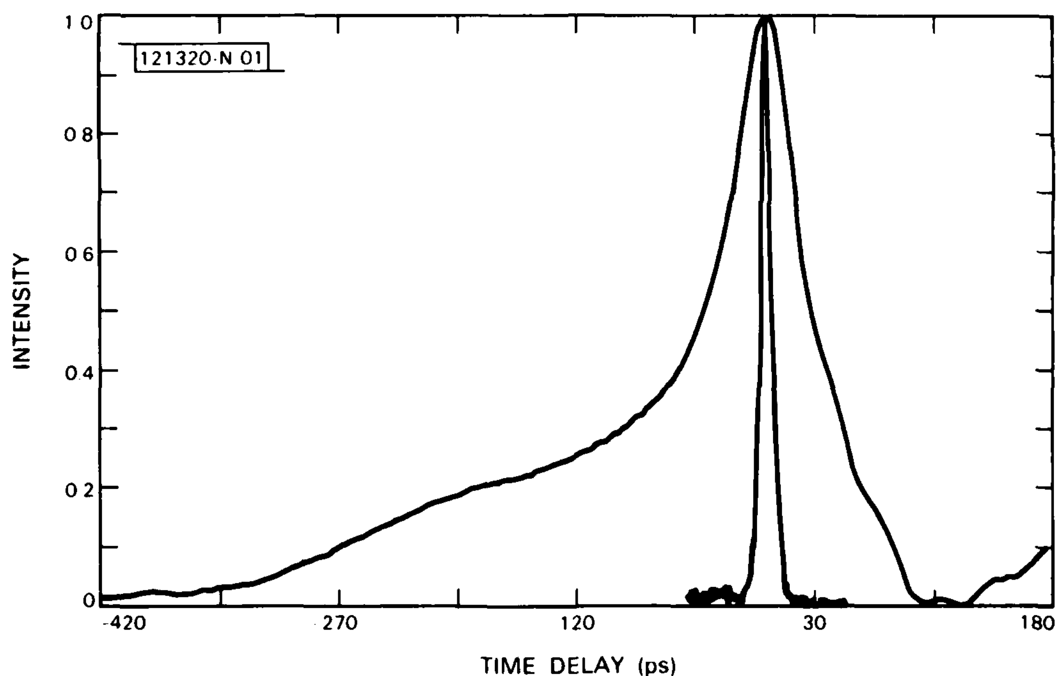

Fig. 2-7. A cross-correlation measurement of temporal response of a pair of InP photodetectors, with autocorrelation of two laser pulses included to illustrate system resolution of 6 ps.

correlation measurement. The data in Fig. 2-7 showed the same temporal response for bias voltages of between 1 and 10 V, and were also unaffected by varying the absorbed laser energy per pulse from 10 to 100 pJ or by tuning the laser wavelength from 720 to 780 nm. The FWHM of both detectors is ~65 ps; this is a factor of ~10 larger than the estimated rise time, which is the incident laser pulse rise time convolved with the package rise time of a few picoseconds. Interpretation of the trailing-edge behavior of the detectors is presently limited by package resonance effects.

D. Welford

2.4 SILICON OPTOELECTRONIC SWITCHES WITH PICOSECOND RESPONSE TIME

Silicon optoelectronic switches have been fabricated and their response time measured using 4-ps laser pulses. The switches were prepared by evaporation of a 1-μm-thick layer of Si onto a 250-μm-thick quartz substrate. A 500-μm-wide, nominal 50-Ω impedance microstrip transmission line (Ti/Au) was evaporated directly on top of the Si layer. The active region of the switch was formed by a 25-μm-wide gap in the stripline electrodes. A metal ground plane evaporated on the underside of the quartz substrate completes the structure. OSM coax-to-microstrip connectors were used to make connections to external circuitry.

The off-state impedance of the switches was measured to be $\sim 10^9$ Ω for bias voltages up to 350 V, resulting in an extremely low dark current. The response time was measured employing 4-ps laser pulses from a synchronously pumped oxazine 750 dye laser operating at a wavelength of 7900 Å. Figure 2-8 shows an autocorrelation trace of the 4-ps optical pulses measured with a rotating plate autocorrelator system. The laser pulses were focused onto the switch (focal spot ~ 100 μm in diameter), and about 10 pJ of pulse energy was absorbed in the active region of the Si layer. Figure 2-9 is a sampling oscilloscope photograph of the photocurrent produced when the laser pulses are incident on the switch. The risetime of the sampling unit was 25 ps, which means that the observed width of the electrical pulse (FWHM ~ 40 ps) is

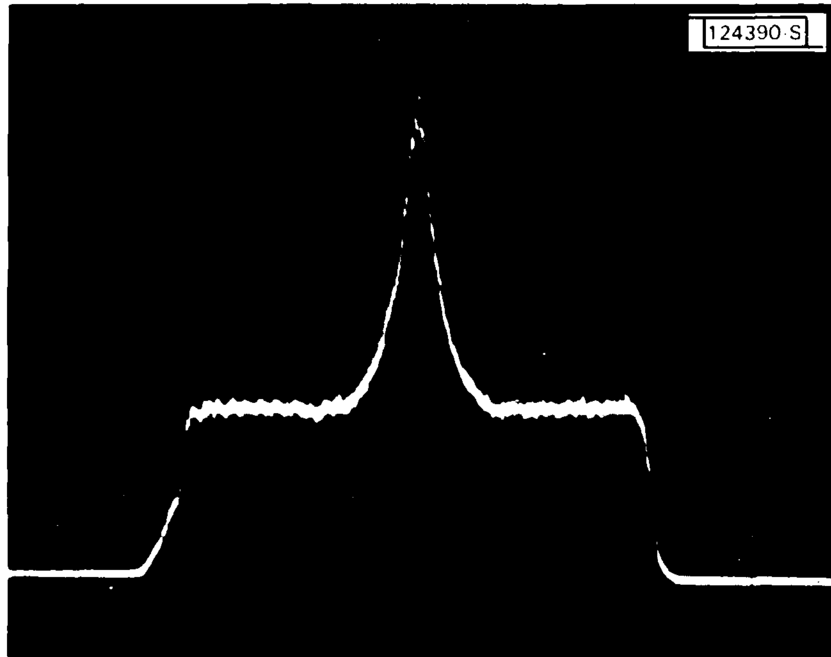

Fig. 2-8. A second-order SHG autocorrelation of 4-ps-duration laser pulses (16.4 ps per horizontal division).

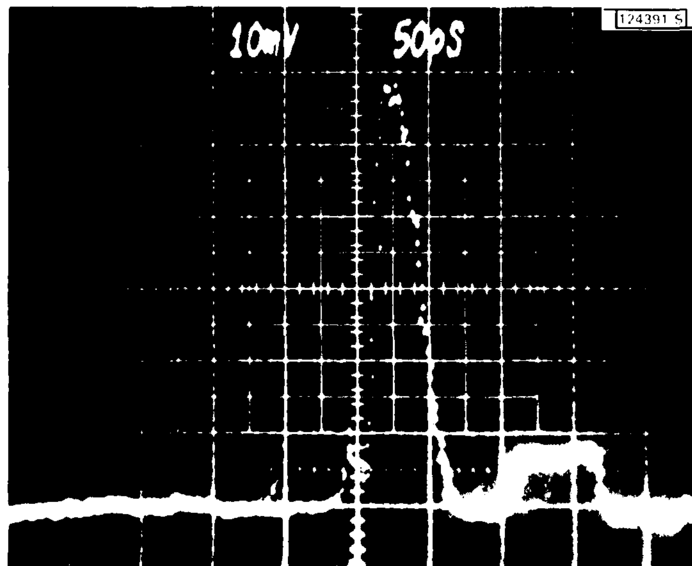

Fig. 2-9. Sampling oscilloscope photograph showing response of Si optoelectronic switch to 4-ps laser pulse. Bias voltage: 67 V; risetime of sampling unit: 25 ps.

clearly instrument limited. Only weak ringing occurs after the main pulse, implying good impedance match between the OSM connections and the 50-Ω transmission line.

From Fig. 2-8 it is evident that the carrier recombination time in these polycrystalline Si films is less than 40 ps. Correlation experiments with a series double-gap structure are presently in progress in order to determine the switch response time to within the 4-ps accuracy limitation implied by the pulse duration of the laser. Similar optoelectronic switches have been fabricated from SOS substrates, and it is planned to reduce the long carrier recombination time in those Si films through introduction of radiation damage.

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2.5 HIGH SPATIAL FREQUENCY GRATING STRUCTURES BY VUV SURFACE ELECTROMAGNETIC WAVE SCATTERING

In recent publications[3,4] we have shown that amplified surface polariton scattering processes play a major role in the formation of the ripple structures that are often observed on semiconductor surfaces following pulsed laser annealing. We have now extended both the experimental measurements and the theoretical model into the vacuum ultraviolet spectral region. The observed ripple periods deviate strongly from the incident laser wavelength in this regime and provide the first measurements of the optical properties of the dynamically produced liquid semiconductor near the electron plasma edge. By using a 157-nm F_2 laser source, ripple patterns with a 65-nm period were formed on Ge surfaces. This represents the highest spatial period structure generated optically on a semiconductor material.

The results of those measurements are summarized in Fig. 2-10, which shows the measured ripple wavevector produced at a number of laser wavelengths ranging from 1.06 μm to 157 nm. Also shown in the figure is the surface polariton dispersion curve calculated for literature values[5,6] of the

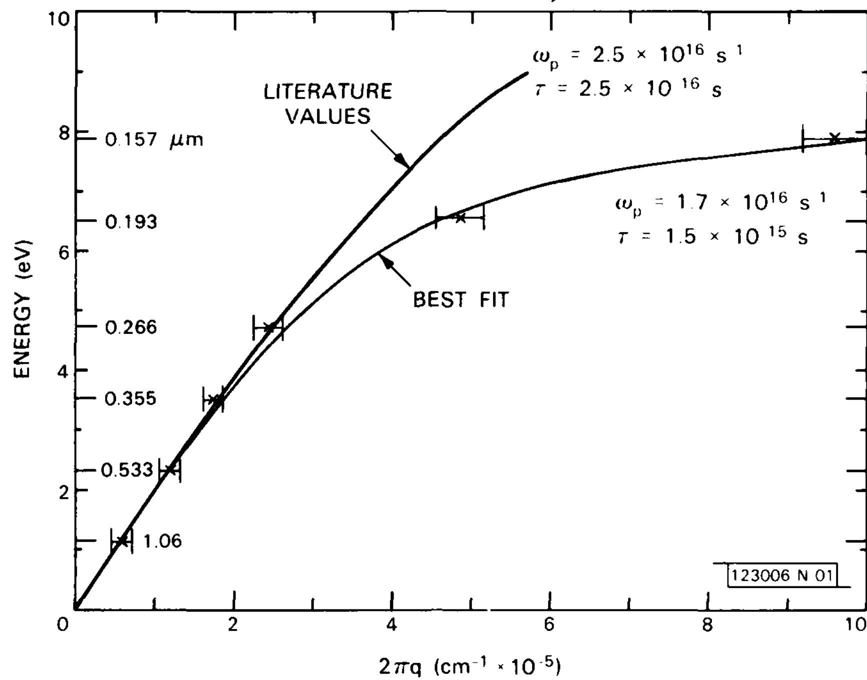

Fig. 2-10. Measured laser-produced ripple dispersion relation for annealing of Ge. Curves correspond to fitting these results to a surface polariton dispersion relation using a free-electron dielectric function to model liquid Ge.

optical properties. The curve labeled "literature values" is an extrapolation based on a free electron plasma dielectric function $[1 - \omega_p^2/\omega(\omega + i/\tau)]$ which is fit to the infrared and visible spectral data with the parameter values $\omega_p = 2.5 \times 10^{16}$ s^{-1} and $\tau = 2.5 \times 10^{-16}$ s. The curve labeled best fit results from using this same expression for the liquid semiconductor optical properties but letting the parameters ω_p and τ vary; the best fit to the data is obtained for $\omega_p = 1.7 \times 10^{16}$ s^{-1} and $\tau = 1.5 \times 10^{-15}$ s. This value for the plasma frequency corresponds to an effective electron density of 9.1×10^{22} cm^{-3} or approximately 2 electrons/Ge atom. The measurement is quite sensitive to the effective electron density since this determines the bend in the curve away from the light line ($\omega/2\pi q = c$). A similar deviation[6] in the optical properties from a free electron plasma

model was found in the previous measurements in the near-UV spectral region. The curve is not as sensitive to the collision parameter; any collision time longer than 1.5×10^{-15} s essentially gives the same curve. However, shorter collision times lead to a curve much closer to the light line and are not consistent with the experimental results. Further work is necessary to fully understand the development of these high spatial frequency ripples and the implications for the optical properties of liquid semiconductors.

Figure 2-11 shows a scanning electron micrograph of a 65-nm ripple in GE. Future extensions of this work may prove useful for generating submicrometer structures for microelectronic applications.

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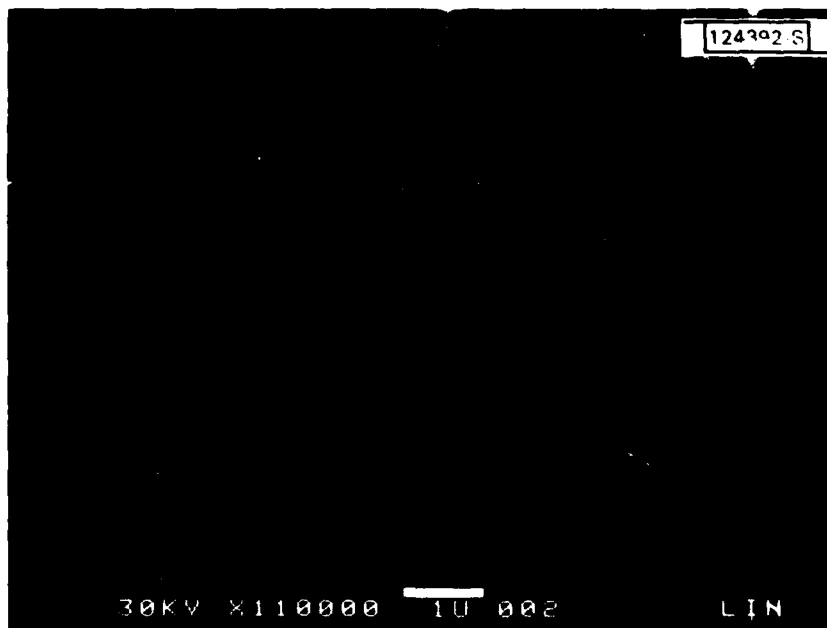

Fig. 2-11. 65-nm ripple produced on a Ge surface by annealing with a 156-nm F_2 laser source.

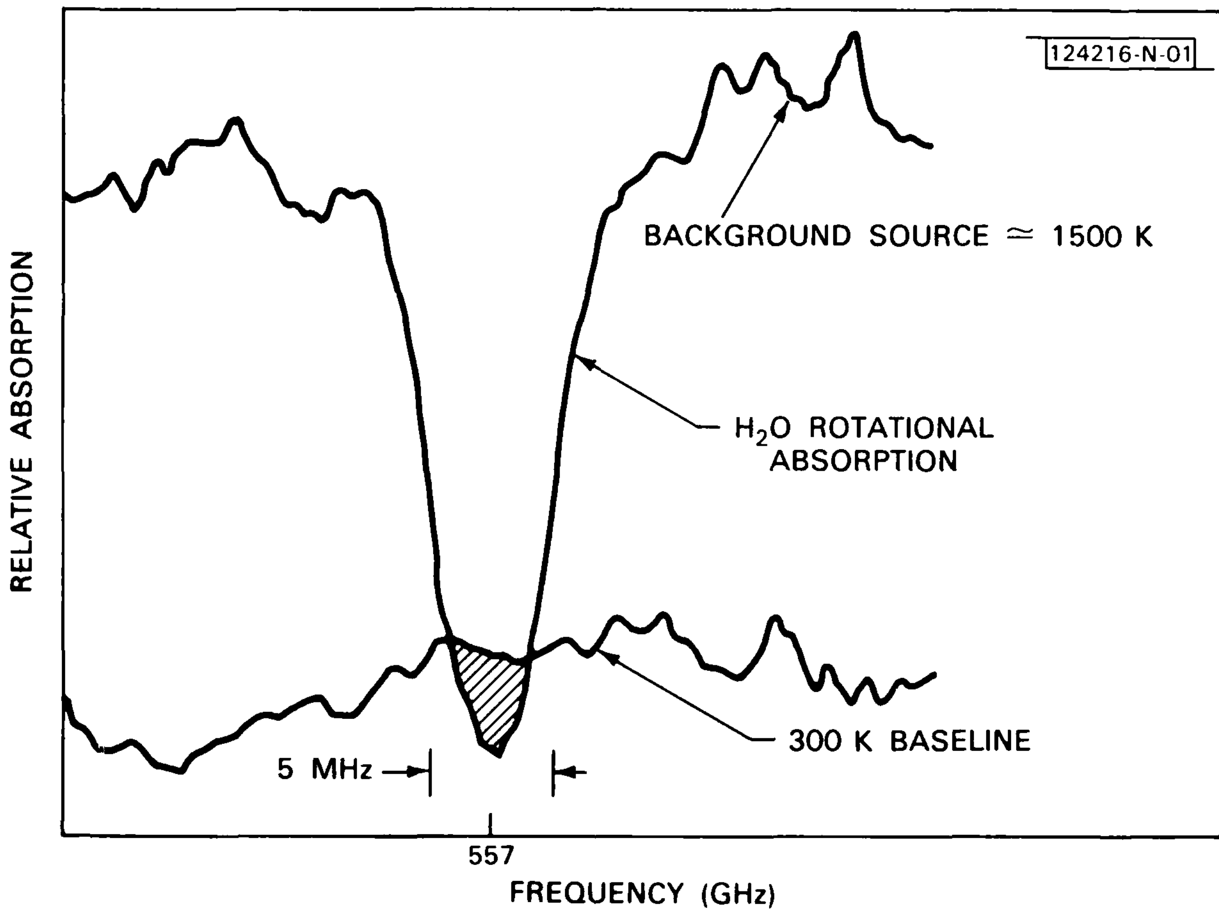

Fig. 2-12. 557-GHz water-vapor absorption line.

2.6 SUBMILLIMETER-WAVE HETERODYNE RADIOMETRY OF EXPANDING WATER VAPOR

Heterodyne radiometry for measuring the temperature of H_2O vapor undergoing isentropic expansion, which was previously demonstrated at 752 GHz (see Ref. 7), has now been carried out at 557 GHz ($1_{10} \leftarrow 1_{01}$ rotational transition). In contrast to the previous experiment, the 1_{01} initial state is strongly populated at the temperature of the expanding gas, which leads to a stronger absorption. In both experiments, water vapor was emitted into a large vacuum chamber by means of a laboratory-scale steam jet. A 280-GHz carcinotron in combination with a second-harmonic GaAs Schottky-diode mixer[8] replaced the HCOOH submillimeter-wave laser used as the first local oscillator (LO) in the original experiment. A double-sideband system noise temperature of approximately 50,000 K was obtained with only 2 mW of LO power (at the fundamental frequency). In the experiments at 752 GHz, 30 mW of LO power was required to obtain a comparable noise temperature.

The measured absorption line is shown in Fig. 2-12. Antenna temperatures at line center indicate that the supersonic flow cools to below 300 K, as expected from adiabatic expansion. Improvements in the receiver frequency resolution are expected to provide a more accurate measurement of the line profile; future experiments will be designed to examine this question, as well as the radiative transfer properties at points further downstream from the jet nozzle.

Since the 557-GHz line can be observed with a relatively modest amount of LO power, the prospect of substituting a combination of solid-state power source at 93 GHz and frequency tripler for the carcinotron appears favorable.

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3. MATERIALS RESEARCH

3.1 CMOS CIRCUITS FABRICATED IN ZONE-MELTING-RECRYSTALLIZED Si FILMS ON SiO_2-COATED Si SUBSTRATES

The utilization of dielectric isolation to achieve improved circuit performance for VLSI has stimulated great interest in the development of Si-on-insulator (SOI) materials. We recently reported[1] the preparation of device-quality SOI films by using graphite strip-heaters for zone-melting recrystallization of poly-Si deposited on SiO_2-coated Si substrates. Uniform SOI films up to 3-in. diameter have been obtained by this technique.[2] N- and p-channel MOSFETs fabricated in the recrystallized films exhibit good electrical characteristics with electron and hole mobilities comparable to those of single-crystal Si devices.[3]

In the present investigation we have designed a CMOS test circuit chip that permits a more critical evaluation of zone-melting-recrystallized SOI films for integrated circuit applications. The test chip, which is based on a 5-μm design rule, contains n- and p-channel transistor arrays, ring oscillators, inverter chains, and various test devices for process control. The objectives of utilizing this circuit design are to assess the uniformity of the SOI films and to determine the speed of SOI/CMOS circuits. In this report, we describe the fabrication of test chips with a good yield of functional transistor arrays and of ring oscillators and inverter chains exhibiting promising speed performance. Uniform operating characteristics are observed for chips covering a significant portion of 2-in.-diam SOI films.

The CMOS circuit chips were fabricated on SOI structures consisting of a 0.5-μm-thick recrystallized Si film, a 1-μm-thick SiO_2 layer, and a 1-Ω-cm p-type Si<100> wafer of 2-in. diameter. No seeding was employed, so that the recrystallized films contain large-angle grain boundaries spaced ~2 mm apart and sub-grain boundaries spaced ~20 μm apart.[1] The CMOS fabrication process involves a total of six photomask steps with poly-Si gate and self-aligned ion-implanted source and drain. The active device regions were first defined by a complete Si island etch isolation. A blanket phosphorous implant was

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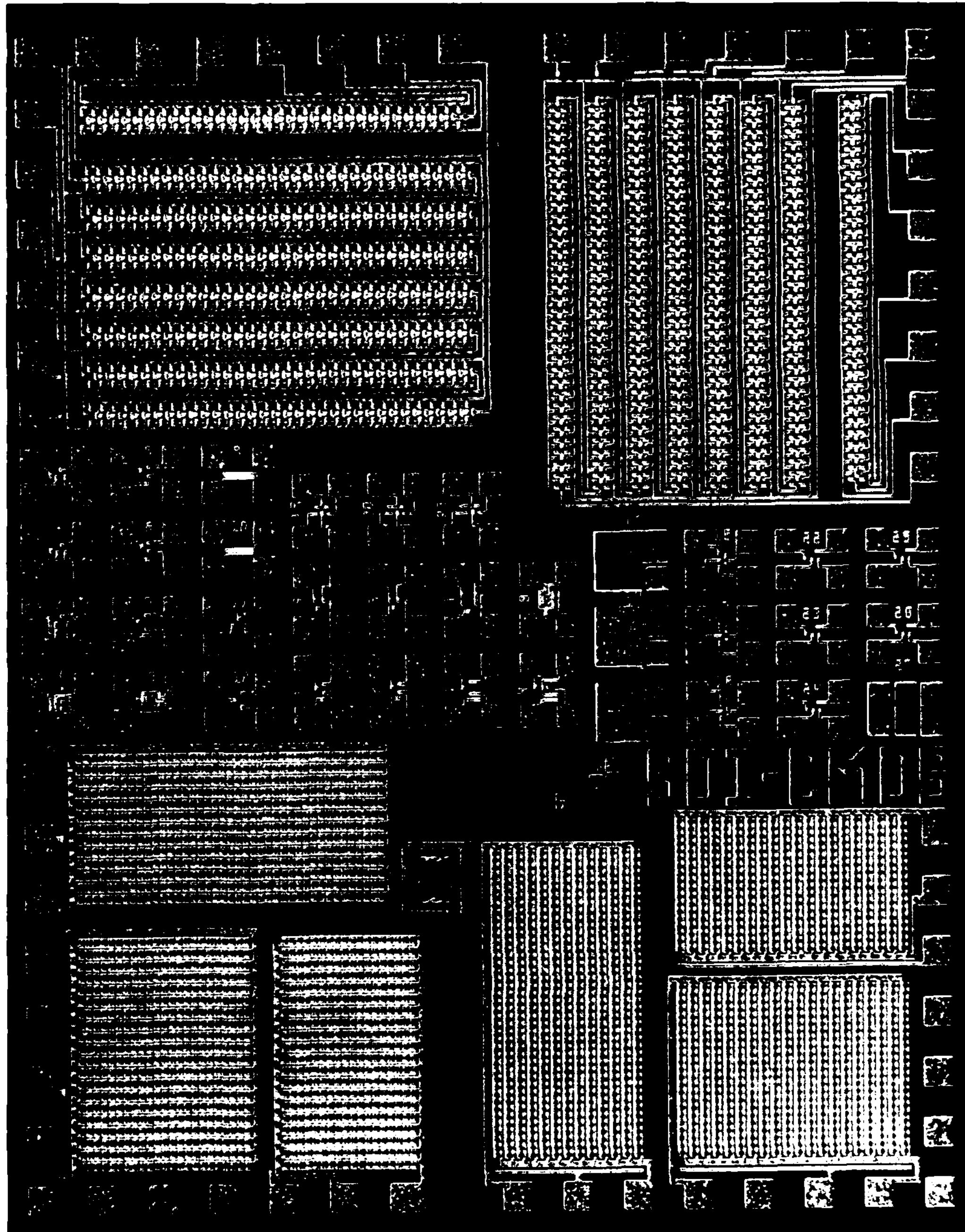

Fig. 3-1. Photomicrograph of SOI/CMOS test chip fabricated in zone-melting-recrystallized Si film.

performed for p-channel doping, while the n-channel devices were doped by a deep selective boron implant which also suppresses the back-channel leakage. The gate oxide was grown at 1000°C to a thickness of 80 nm. Poly-Si gates 0.5 μm thick were deposited by LPCVD, doped by boron diffusion, and then etch defined. N-channel source and drain were formed by a blanket phosphorous implant, and a counterdoping boron implant was then performed selectively to form the p-channel source and drain. The wafers were encapsulated with CVD SiO_2 and annealed at 900°C to activate the implanted dopants. After Al metallization, the finished chips were sintered in H_2 at 450°C.

Figure 3-1 is a photomicrograph of a finished SOI/CMOS chip, which measures about 3 × 4 mm. About 100 such chips were fabricated on each of three wafers. A 31-stage ring oscillator with fan-in and fan-out of one and a 231-stage inverter chain are located at the upper left. A similar circuit, rotated by 90°, is placed at the upper right. The purpose of the rotation is to examine the effects of grain and sub-grain boundaries on circuit performance. Carrier transport is approximately parallel to these boundaries in one circuit, and approximately perpendicular to them in the other. Test transistors, single-stage inverters, gated diodes, capacitors, and test patterns are located in the middle portion of the chip. Two n-channel transistor arrays consisting of 360 or 533 parallel devices and a p-channel array consisting of 460 parallel transistors are located at the lower left. The individual transistors, which have a 5-μm gate length and 20-μm gate width, are spaced 5 μm apart. Three similar arrays, rotated by 90°, are located at the lower right.

To evaluate the uniformity of the SOI films, we have investigated the performance of all the transistor arrays on a wafer with 98 test chips. The area of these arrays is about one-third that of the chips, which occupy approximately 60 percent of the total wafer area. Since the transistors in each array are connected in parallel, failure of a single device results in failure of the entire array. Of the 588 arrays, 490 were functional while 98 failed because of source-to-drain short or open circuits. For 62 of the inoperable devices, localized metallization defects such as incomplete

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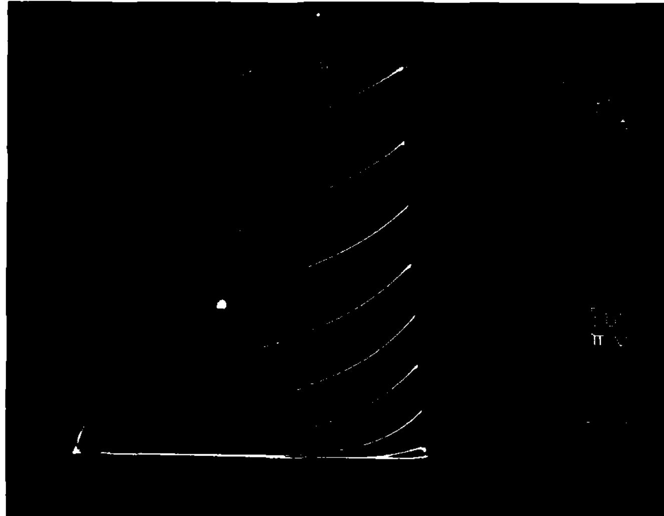
(a)



(b)

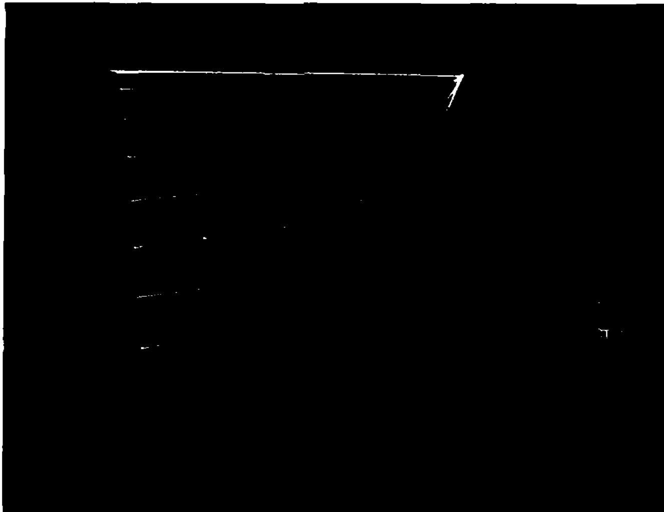


Fig. 3-2. I-V characteristics of typical SOI/CMOS transistor arrays consisting of (a) 360 n-channel transistors in parallel and (b) 460 p-channel transistors in parallel.

etching of the Al or poor contacts were found by microscopic inspection. Thus, the overall yield of functional arrays exceeds 90 percent when the obvious fabrication defects are discounted. The total number of transistors in all the arrays is 2.65×10^5. If it is assumed that each of the failed arrays contains one defective device, the transistor failure rate is 3.7×10^{-4}, or only 1.4×10^{-4} if the known fabrication defects are taken into account.

The operating characteristics of the functional transistor arrays are quite uniform from chip to chip. Figure 3-2(a-b) shows I-V curves for typical n- and p-channel arrays. For the three types of arrays in which carrier transport is approximately parallel to the grain and sub-grain boundaries, the average values and standard deviations for the transconductance are as follows: p-channel (measured at $V_D = V_G = -5$ V), 52 ± 2 mS; 360- and 533-transistor n-channel (measured at $V_D = V_G = +5$ V), 78 ± 2 and 115 ± 3 mS, respectively. The arrays in which carrier transport is perpendicular to the boundaries have similar characteristics, except that the transconductance values are ~5 percent lower.

Measurements have also been made on all 31-stage ring oscillators on the 98-chip wafer. For the two orientations differing by 90°, 82 of the 98 oscillators in each set are functional. Again, most of the failures can be attributed to obvious metallization defects. The operating characteristics of a typical functional oscillator are shown in Fig. 3-3. The circuit starts to oscillate at a supply voltage V_D of 1.5 V. At V_D = 5 V, the switching delay time and dissipated power are respectively 2 ns and 0.13 mW per stage, for a power-delay product of 0.26 pJ. The operating speed can be attributed to the high carrier mobilities in the recrystallized Si films and the reduced parasitic capacitance of the SOI structure. Figure 3-4(a-b) shows the distributions of switching delay time per stage for the two sets of oscillators. Both distributions peak at about 2 ns with a standard deviation of ~0.1 ns. This similarity indicates that the sub-grain boundaries, despite their large numbers, do not have a significant effect on circuit performance. For the oscillators with delay times exceeding 3 ns,

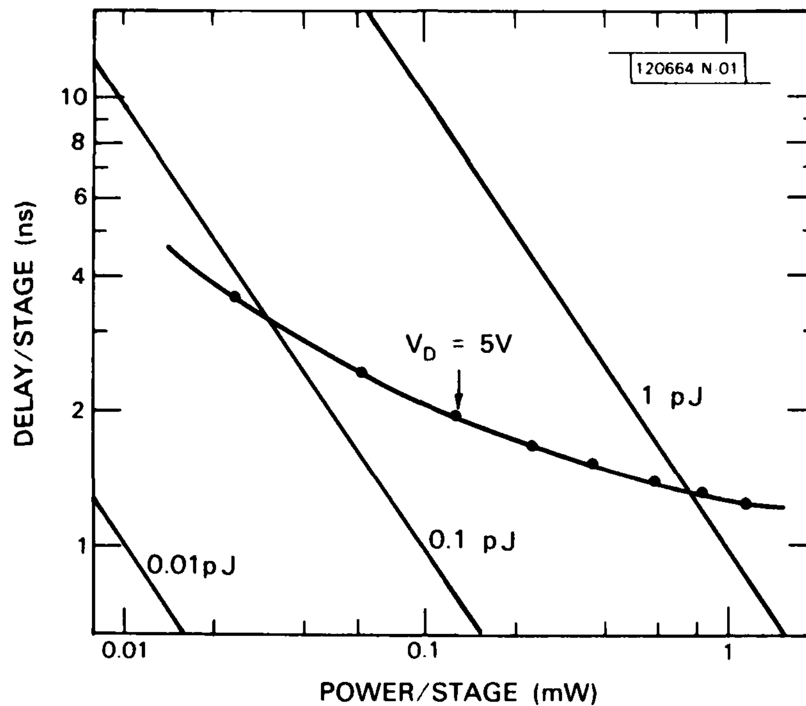


Fig. 3-3. Switching delay time of 31-stage SOI/CMOS ring oscillator as a function of power dissipated per stage.

the metallization appears to be imperfect. The slow speed of these circuits may therefore be due to an increase in contact resistance.

The yield of inverter chains on the test chips is comparable to the yield of ring oscillators. The chains exhibit normal inverter characteristics and switching delay times similar to those measured for the ring oscillator circuits.

For each of the other 2-in.-diam SOI wafers on which CMOS chips were fabricated in this study, we have tested the transistor arrays, ring oscillators, and inverter chains on about 10 chips distributed over the area of the wafer. All the functional circuits measured are comparable in performance to those on the wafer for which all 98 chips were tested.

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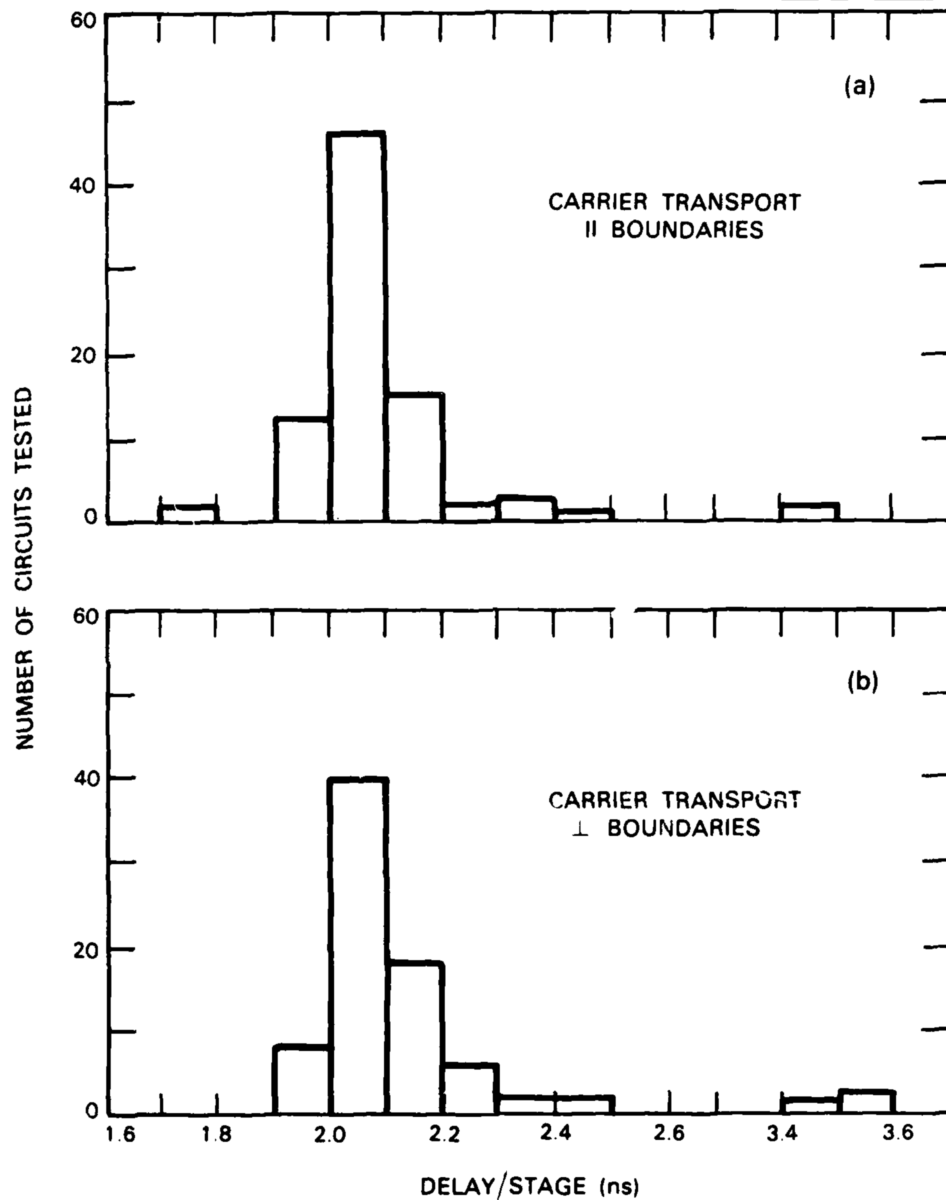

Fig. 3-4. Distribution of switching delay times for 31-stage ring oscillators with carrier transport (a) parallel and (b) perpendicular to sub-grain boundaries.

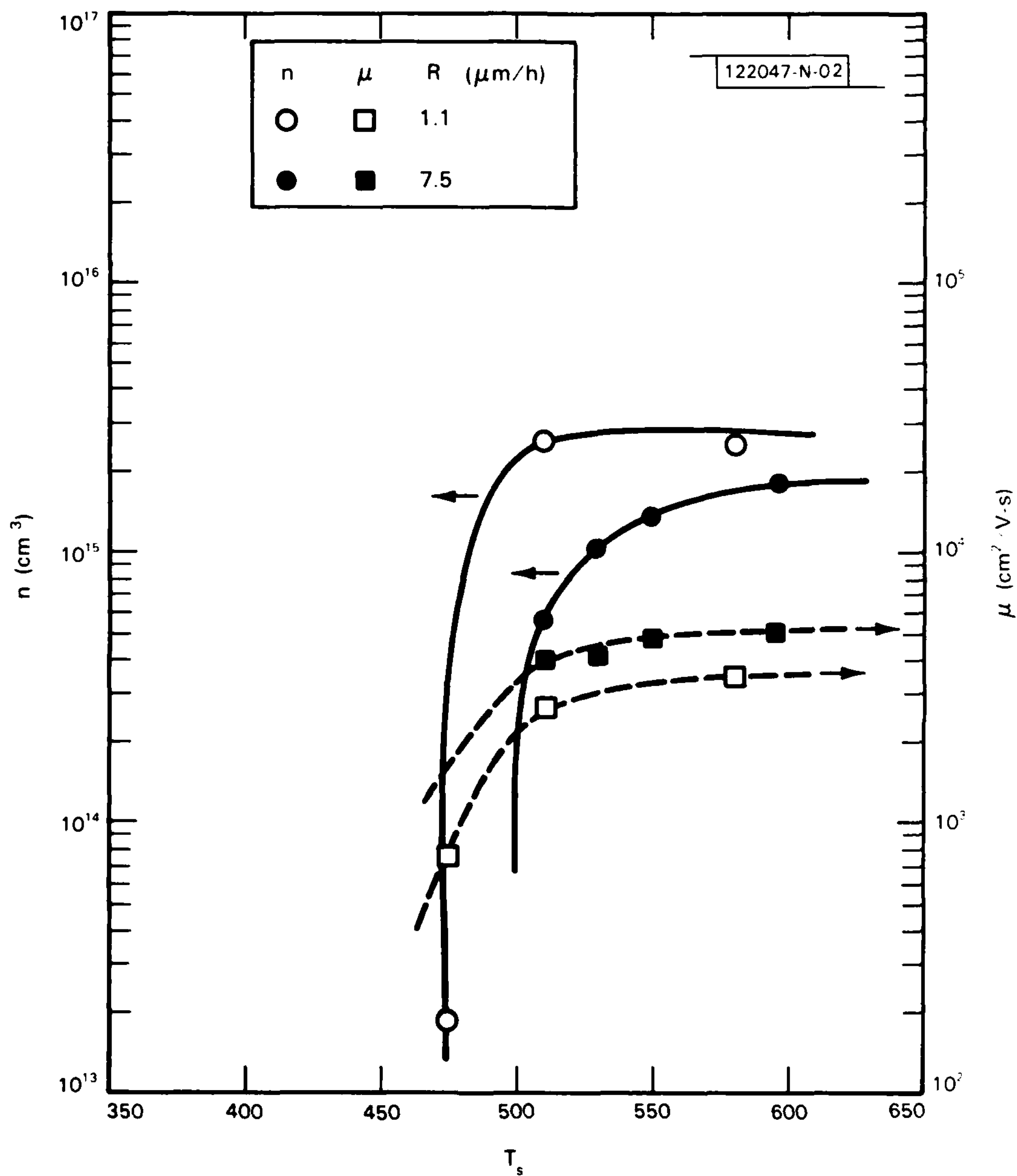

Fig. 3-5. Carrier concentration n and mobility μ at 77 K vs substrate temperature T_s for GaAs films grown by MBE at growth rates of 1.1 and 7.5 μm/h.

3.2 GROWTH OF GaAs FILMS BY MOLECULAR BEAM EPITAXY AT LOW SUBSTRATE TEMPERATURES

Growth of GaAs films by molecular beam epitaxy (MBE) is conventionally performed at substrate temperatures T_s above 500°C because it has been found[4-6] that the properties of films grown at lower temperatures are severely degraded by the formation of carrier traps. In this investigation we have grown MBE GaAs films with good electrical and photoluminescence properties at values of T_s as low as 380°C by reducing the growth rate and As_4 flux. We carried out this study because growth at lower temperatures is expected to result in improved characteristics for many device structures. Since the rate of solid-state diffusion decreases exponentially with decreasing temperature, reducing T_s by only modest amounts should have dramatic effects in increasing the abruptness of doping profiles, reducing outdiffusion of impurities from substrates, and decreasing interdiffusion at heterojunction interfaces.

The adverse effects upon GaAs properties that usually result from MBE growth at values of T_s below ~500°C are illustrated by Fig. 3-5. This figure shows the dependence on T_s of the carrier concentration n and mobility μ determined from Hall-coefficient and resistivity measurements made at 77 K on films about 2 μm thick that were grown at rates of 1.1 and 7.5 μm/h. These films, as well as all the others prepared in this study, were grown in a Varian Gen II MBE system. They were made n-type by doping with Si. The surface stoichiometry during growth was monitored by the *in-situ* electron diffraction pattern, and the As_4 flux during each growth run was adjusted to provide barely As-stabilized conditions. The As_4 flux required for surface stabilization decreases strongly with decreasing T_s for a given growth rate (i.e., given Ga flux). Substrate preparation followed standard procedures.

Figure 3-5 shows that at conventional T_s values of 550° to 600°C, little or no compensation due to traps occurs for the Si doping levels used, which were 2 to 3 × 10^{15} cm^{-3}. However, as T_s is reduced, the trap concentration becomes comparable to and eventually greater than the Si concentration. The

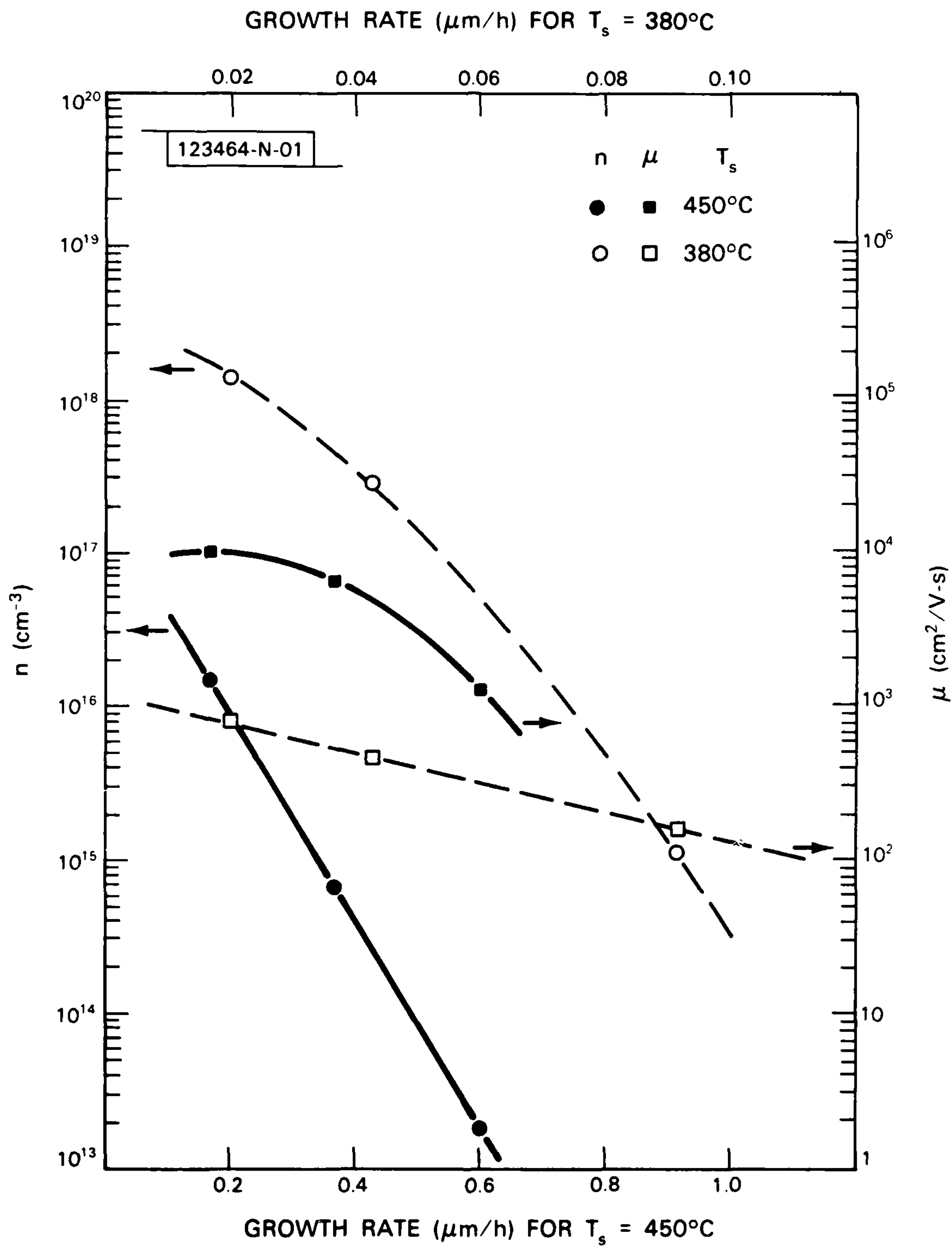

Fig. 3-6. Carrier concentration n and mobility μ at 77 K vs growth rate for GaAs films grown by MBE at substrate temperatures T_s of 450° and 380°C.

Fermi level is then pinned below the conduction band at an energy determined by the activation energy of the traps. Consequently, there is an abrupt decrease in both n and μ, which causes the films to become highly resistive. For the growth rates of 1.1 and 7.5 μm/h, this transition occurs at T_s values of ~470° and 505°C, respectively. Films that were grown below the transition temperatures had such high resistance that no Hall data could be obtained.

The results shown in Fig. 3-5 can be explained by assuming that the traps in the MBE films are crystal defects that are formed because Ga atoms adsorbed on the substrate from the vapor phase are incorporated into the growing film before they reach appropriate lattice sites by surface diffusion. To avoid the formation of such defects, the intervals between the arrival of incident Ga atoms on the GaAs surface should exceed the times required for migration of the adsorbed atoms. Since the surface mobility of the adsorbed atoms decreases strongly with decreasing temperature, if the rate of arrival (i.e., the growth rate) remains constant then the defect concentration will increase as T_s is decreased. This explanation suggests that the crystal quality of films grown at low T_s would be improved by reducing the growth rate. This expectation has been confirmed by the results shown in Fig. 3-6, where n and μ at 77 K are plotted against growth rate R for substrate temperatures of 450° and 380°C.

The films grown at T_s = 450°C were ~1.5 μm thick. For these films the degree of compensation decreases drastically as R is decreased, causing a dramatic increase in both n and μ although the Si flux was kept constant. For R > 0.6 μm/h, the resistance is so high that no Hall data could be obtained. For R ~ 0.2 μm/h, on the other hand, the values of n and μ are comparable to those of films grown under the same conditions at T_s = 575°C. For the films grown at T_s = 380°C, the thickness was only about 0.6 μm, since the growth rates used were so low. In order to avoid any interface depletion problems, the films were doped more highly than those grown at higher values of T_s. This was accomplished by increasing the Si cell temperature sufficiently to provide a carrier concentration of ~5×10^{16} cm^{-3} for R ~ 1 μm/h and T_s ~ 580°C. The films grown at 380°C are heavily compensated for

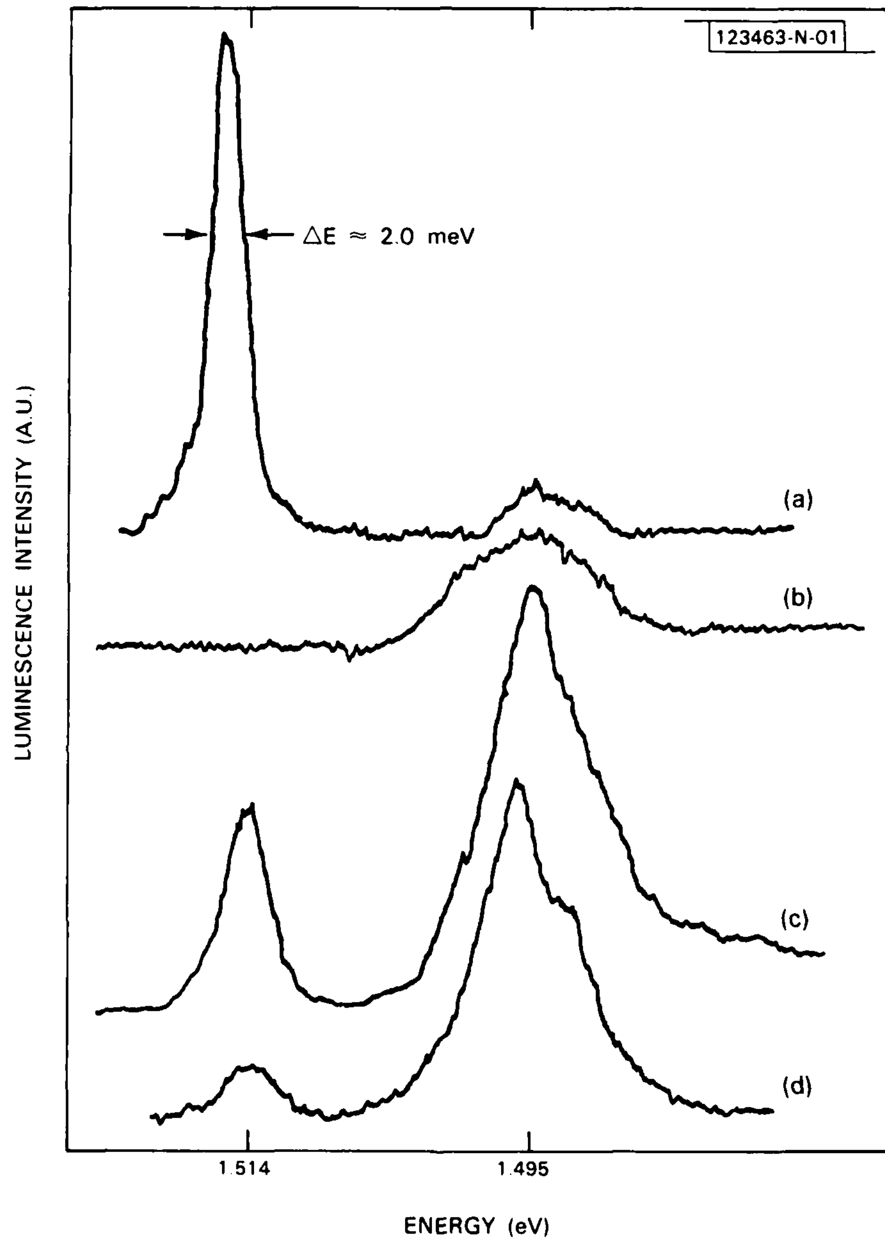

Fig. 3-7. Laser-excited photoluminescence spectra measured at 4.2 K for GaAs films grown by MBE under the following conditions: (a) $T_s \approx 580°C$, $R \approx 1.1$ μm/h; (b) $T_s \approx 450°C$, $R \approx 1.1$ μm/h; (c) $T_s \approx 450°C$, $R \approx 0.2$ μm/h; (d) $T_s \approx 380°C$, $R \approx 0.02$ μm/h.

growth rates much above 0.02 μm/h. At R = 0.02 μm/h, the carrier concentration rises to nearly 2×10^{18} cm^{-3}. This is the Si concentration expected for films grown at this rate, which has been reduced by a factor of 50 from 1.0 μm/h. Because of the increase in Si concentration, the fact that n increases with decreasing R is by itself not sufficient evidence to claim improved crystal perfection. However, the fact that μ increases with increasing n is convincing evidence for this claim.

To obtain further evidence for the improvement in crystal quality achieved at low T_s by decreasing the growth rate, laser-excited photoluminescence spectra at 4.2 K were measured for MBE films grown under various conditions. Representative spectra are shown in Fig. 3-7. Trace (a) was obtained for a film grown under conventional conditions, with $T_s \approx 580°C$ and R ≈ 1.1 μm/h. The more intense peak is due to bound exciton recombination, while the other peak is due to carbon. Trace (b) is the spectrum for a film grown at $T_s \approx 450°C$ and R ≈ 1.1 μm/h. Although the incident laser power was increased from 6 to 45 mW, the exciton peak cannot be detected. Trace (c) is the spectrum obtained at a laser power of 12 mW for another film grown at $T_s \approx 450°C$ but with R decreased to 0.2 μm/h. A distinct exciton peak is observed at 1.514 eV. An exciton peak is also present in trace (d), which was obtained for a film grown at $T_s \approx 380°C$ with R ≈ 0.02 μm/h. Even though the last two spectra are far from ideal, they illustrate the improvement in crystal quality that can be achieved for films grown at low T_s if the growth rate is reduced.

In the course of our investigation, we found that the density of a major surface defect in MBE material, commonly referred to as the oval defect, is strongly correlated with R. In Fig. 3-8 the average oval defect density determined from the results of measurements made in several representative areas across the film surface is plotted against R. (The inset is an optical micrograph of two of these defects taken with a phase contrast microscope.) The defect density increases linearly with R but appears to be independent of substrate temperature, since the films were grown at values of T_s from 380° to 580°C. Although the cause of the oval defects is still in question, a

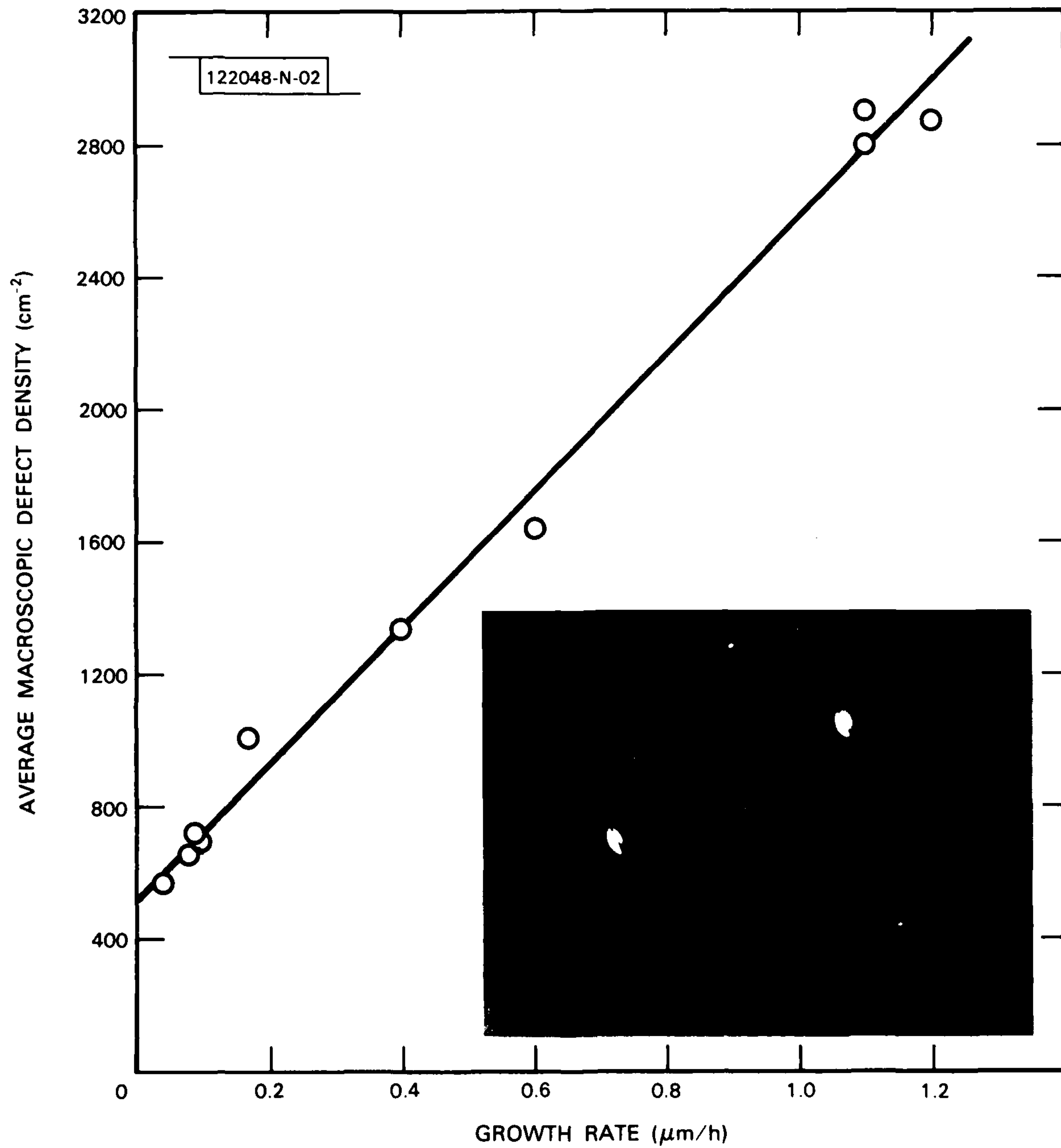

Fig. 3-8. Average density of oval defects vs growth rate for GaAs films grown by MBE.

major role in their formation is apparently played by the Ga source or the Ga cell, since R is proportional to the flux of Ga atoms, which is determined by the temperature of the Ga cell. It has been reported previously that these defects are due to Ga_2O (see Ref. 7). It seems unlikely that this oxide is responsible for the oval defects we have observed, however, since at no time during this investigation was Ga_2O detected by the quadrupole mass spectrometer.

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3.3 JUNCTION FORMATION IN GaAs SHALLOW-HOMOJUNCTION SOLAR CELLS BY THE USE OF SPIN-ON DIFFUSION SOURCES

Fabrication of high-efficiency GaAs solar cells utilizing the shallow-homojunction $n^+/p/p^+$ structure requires the formation of high-quality n^+/p junctions. In addition, the n^+ top layer must be thin ($d < 1000$ Å), uniform in thickness, and degenerately doped. For the best shallow-homojunction GaAs solar cells so far obtained, which have efficiencies of ~20% (AM1), the n^+ layers were grown by vapor-phase epitaxy (VPE).[8] High-efficiency cells have also been obtained[9] with n^+ layers grown by molecular beam epitaxy (MBE).

It is also possible to form junctions in GaAs by high-temperature diffusion. However, the open-tube diffusion methods conventionally employed for Si cannot be used for GaAs because surface degradation is produced by thermal decomposition that occurs at the high temperatures required. Therefore, most diffusions in GaAs have been carried out by sealing the sample in an ampoule containing the dopant source together with a source of As to maintain an As overpressure, which minimizes GaAs decomposition. For such closed-tube diffusions, precise control of dopant incorporation and As overpressure is difficult, and the use of sealed ampoules presents practical problems for large-scale production.

More recently, open-tube diffusions have been carried out in GaAs by using doped layers grown by chemical vapor deposition (CVD)[10] and spin-on layers[11,12] as diffusion sources. These diffusions have yielded shallow,

abrupt dopant profiles, although no data have been reported on the quality of junctions formed. In this investigation, spin-on diffusion has been used to form the n^+ layer in shallow-homojunction $n^+/p/p^+$ GaAs solar cells. This is the first time diffusion has been employed in the fabrication of such cells. The spin-on technique is potentially advantageous because it may permit the formation of n^+ layers of optimum thickness without the need for subsequent thinning, which is currently required for most n^+ layers grown by VPE.

In the basic spin-on diffusion process, a commercial solution† which consists of a soluble silicon compound, the desired dopant, and an inert solvent, is first applied to the surface of the GaAs wafer. We have used Sn as the dopant in our experiments. A thin, uniform coating of the solution is obtained by spinning the wafer for 15 to 30 s at ~1000 rpm. The wafer is prebaked at 200° to 400°C for 10 to 30 min. to decompose the soluble silicon compound, thus forming a Sn-doped SiO_2 layer 0.1 to 0.3 μm thick. The sample is then placed in a fused silica tube and heated to 850° to 1000°C for 10 to 30 min. in forming gas (15% H_2, 85% Ar) to cause diffusion of the Sn from the oxide layer into the GaAs. The oxide acts as an encapsulant to suppress the thermal decomposition of the GaAs. After cooling, an HF etch is used to remove the oxide from the surface of the sample.

In a number of experiments we modified the basic spin-on process by sandwiching the doped oxide layer between undoped SiO_2 layers ~0.1 μm thick, as shown schematically in Fig. 3-9. We found that the undoped layers deposited on the GaAs surface reduced the density of thermal etch pits, and that such layers formed by CVD at 350°C gave more consistent results than those formed from undoped spin-on solutions. All the results reported below were obtained for diffusions in which the GaAs surface was coated with an undoped CVD oxide and then with the Sn-doped spin-on oxide.

To evaluate the spin-on process, we have used the Sn-doped source to form n^+ layers in nominally undoped, semi-insulating GaAs wafers. The sheet resistance values are typically in the range of 10 to 50 Ω/□ , and Hall-effect measurements give sheet carrier concentrations of 5 to 20 × 10^{13} cm^{-2},

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†"Tinsilicafilm," Emulsitone Co., Whippany, New Jersey 07981.

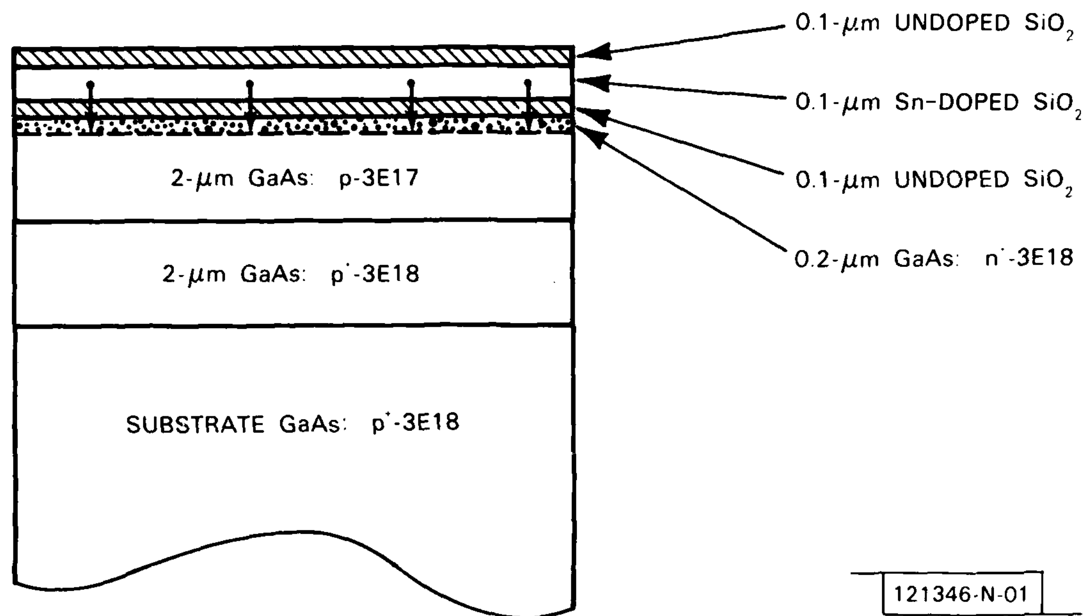

Fig. 3-9. Sample structure for experiments on junction formation in GaAs by spin-on diffusion.

for average mobilities of 2000 to 2200 $cm^2/V\text{-}s$. The values are comparable to published results for spin-on diffusion in GaAs (see Ref. 12). If the diffusion depth is taken to be ~0.2 μm, as indicated by the short-circuit current densities measured for our solar cells, the volume dopant concentrations are ~2 to 10 × 10^{18} cm^{-3}, which are also comparable to the published results.[12]

For solar cell fabrication, GaAs substrates with the structure shown in Fig. 3-9 were prepared by VPE growth of successive p^+(Zn, 3 × 10^{18} cm^{-3}) and p(Zn, 2 × 10^{17} cm^{-3}) layers, each 2 μm thick, on p^+(Zn, 3 × 10^{18} cm^{-3}) GaAs wafers. A shallow n^+/p junction was formed by diffusion of Sn from the spin-on oxide into the p layer. While it would be possible to form junctions directly in GaAs wafers by the spin-on method, in these initial experiments we used the p/p^+ VPE layers in order to minimize the initial surface defect density as well as to maximize the solar cell response by the action of the back surface field.

Solar cells were fabricated on the as-diffused layers containing n^+/p junctions by the procedure previously reported for samples containing an epitaxially grown junction.[8] Both "dot" cells (3.1×10^{-3} cm^2) and small test cells (9.3×10^{-2} cm^2) were fabricated. Figure 3-10 shows the I-V characteristic of our best test cell taken under illumination from an ELH lamp simulator, which was adjusted to produce approximately AM1 ($\approx$100 mW/cm^2) conditions. For the test cell the open-circuit voltage V_{oc} is 0.93 V, the short-circuit current density J_{sc} is ~21 mA/cm^2, and the fill factor ff is 0.73, giving a conversion efficiency η of ~14% (AM1).

Since the as-diffused junctions so far obtained are ~0.2 µm deep, further thinning of the n^+ region is required to obtain the maximum photocurrent from the solar cells. We have investigated the characteristics of cells in which this region was thinned by the anodization and stripping procedure used for cells with an epitaxially grown junction.[8] The increase in I_{sc} with decreasing n^+ thickness is not as great as that observed for the epitaxial junction cells,[13] and the V_{oc} of the diffused cells sometimes decreases with thinning. This behavior may be due to p-type dopant

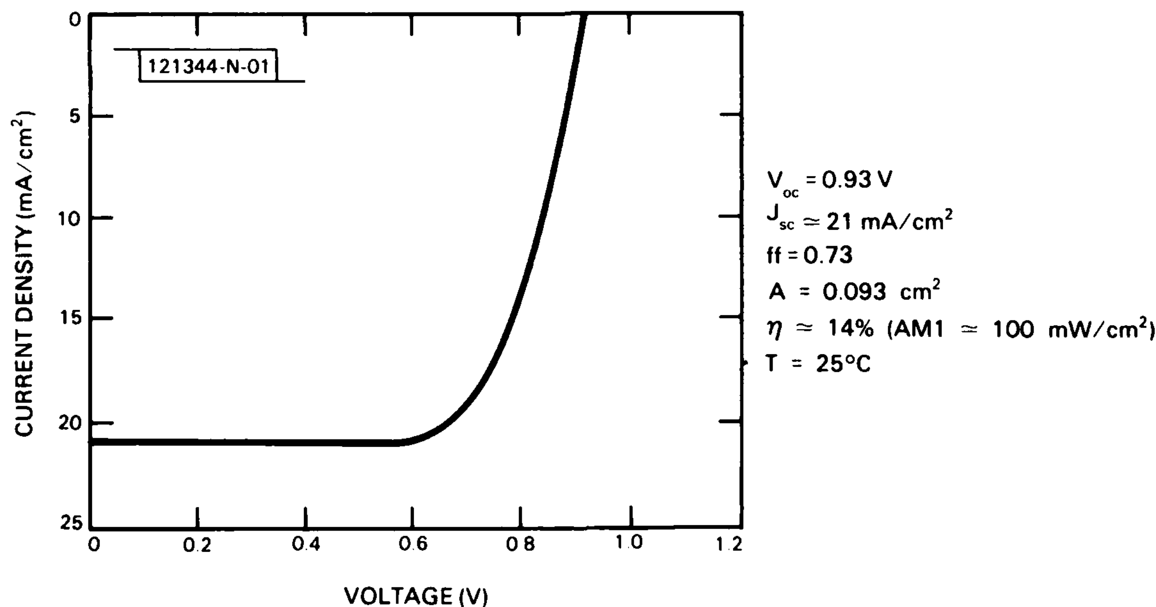

Fig. 3-10. Photocurrent density vs voltage for shallow-homojunction GaAs solar cell with junction formed by spin-on diffusion.

redistribution during the diffusion step, which would reduce the abruptness of the n^+/p junctions.

Figure 3-11 shows the spectral response of a diffused-junction test cell similar to the cell of Fig. 3-10. The long-wavelength response approaches that of a high-efficiency VPE GaAs cell, indicating that the diffusion process did not have a detrimental effect on the base region of the cell. The reduction in quantum efficiency observed at the shorter wavelengths is expected for an n^+ layer that is too thick.[13] Figure 3-12 shows the J_{sc}-V_{oc} data measured for a diffused dot cell with a similar structure to the cell of Fig. 3-10. While the diode factor of 1.5 and dark-current density of 5×10^{-12} A/cm^2 are larger than the values for the best VPE shallow-homojunction solar cells, they are comparable to the values for the best MBE cell.[9]

We have studied the uniformity and reproducibility of the diffused n^+/p junctions formed in GaAs samples by mapping the photovoltaic response of dot cell arrays. For the better diffusions the uniformity of response is good, with low V_{oc} values observed only on the edges of the sample (where the layers are least uniform) or near small areas of surface damage. A more serious problem has been the lack of run-to-run reproducibility of the spin-on diffusions. This problem appears to arise from changes in the properties of the spin-on solution with time. We are presently investigating methods to increase the reproducibility of the process.

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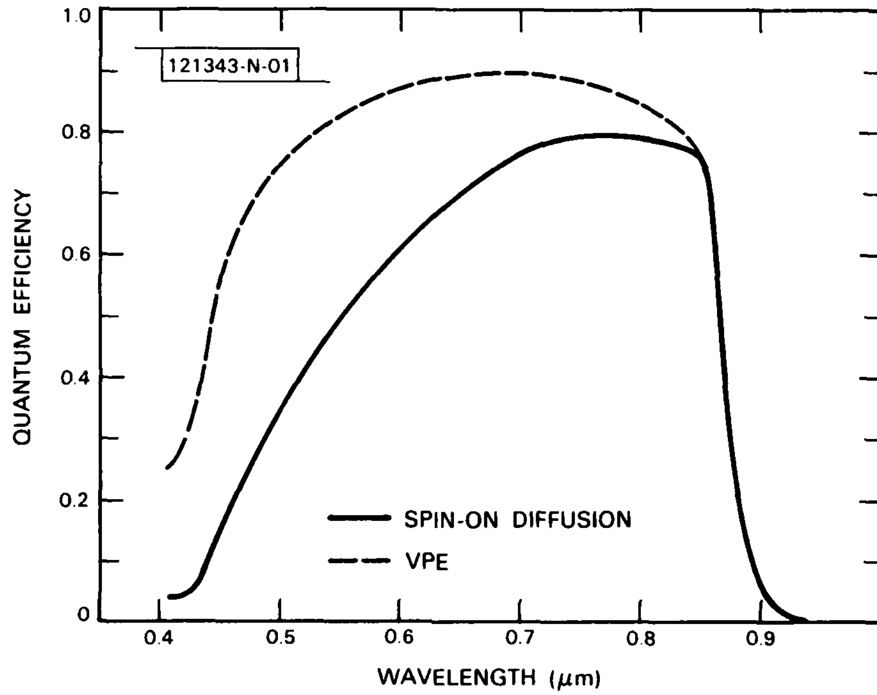

Fig. 3-11. Quantum efficiency vs wavelength for GaAs solar cells with junctions formed by spin-on diffusion or vapor-phase epitaxial growth.

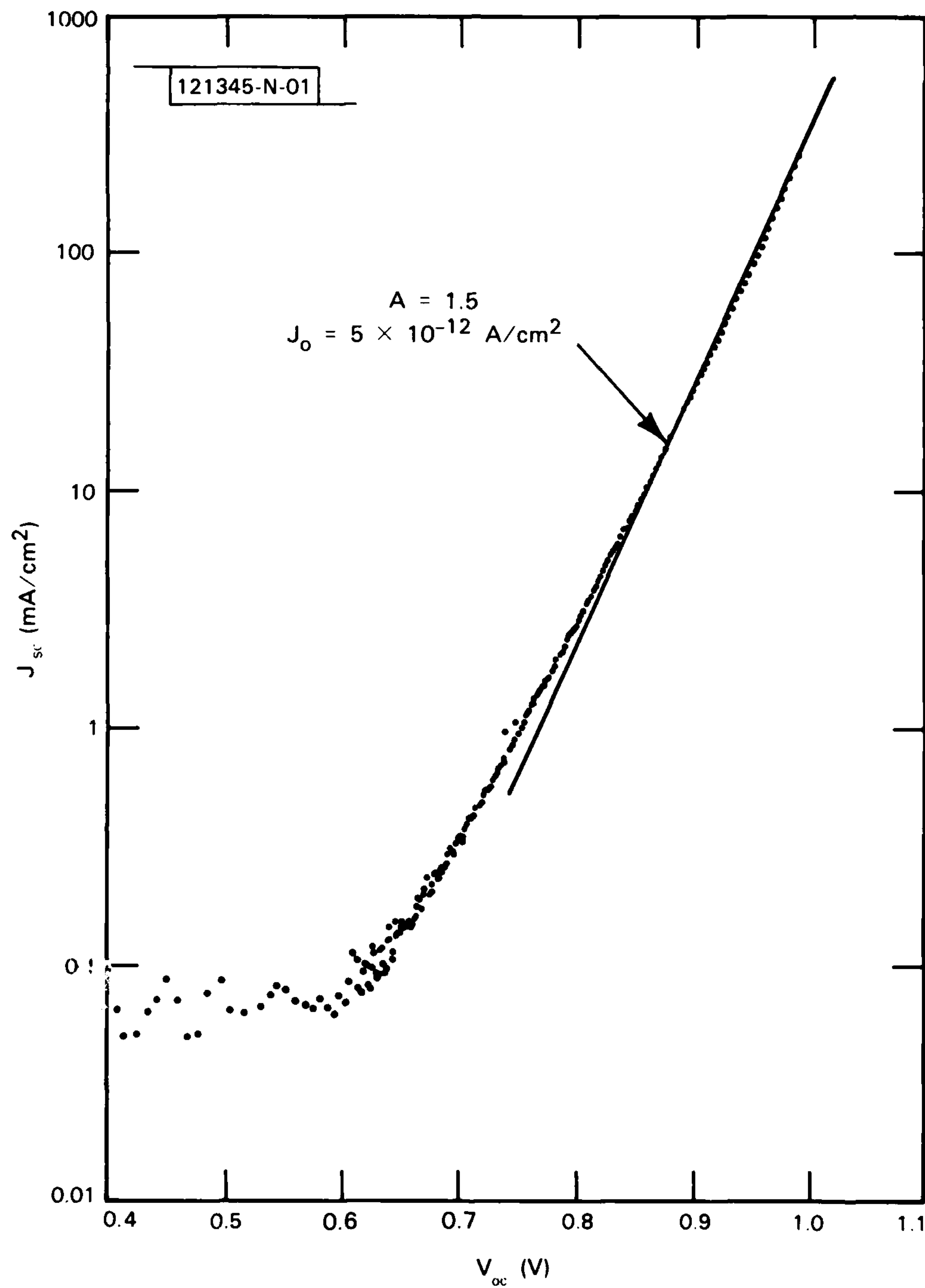

Fig. 3-12. Short-circuit current density J_{sc} as a function of open-circuit voltage V_{oc} for GaAs solar cell with junction formed by spin-on diffusion.

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4. MICROELECTRONICS

4.1 GaAs CHARGE-COUPLED DEVICES FOR SPATIAL LIGHT MODULATORS

A programmable spatial light modulator which uses a GaAs charge-coupled device (CCD) has recently been demonstrated.[1] This modulator is based on the electroabsorption (or Franz-Keldysh) effect, which is the variation of optical absorption with electric field for wavelengths near the bandgap absorption edge. Since the electric field in a CCD well is a function of the amount of charge in the well, the optical absorption of a CCD cell can be modulated by varying the charge content. This report describes the design and fabrication of a 16-stage GaAs Schottky-barrier CCD used to demonstrate optical modulation.

Figure 4-1 is a cross-sectional view of the three-phase GaAs CCD designed for the modulator experiments. The ϕ_1 and ϕ_2 gates are Ti-Au and are opaque to the $\lambda \approx 0.90$-μm radiation to be modulated, while the ϕ_3 gates are thin Ti and are semitransparent at this wavelength. The illumination is incident normal to the device and passes through the ϕ_3 gates. When charge packets are located in the ϕ_3 wells, the amount of illumination absorbed is dependent on the quantity of charge in each well. The modulated radiation then passes through the substrate and is detected.

The device is fabricated using a Cr-doped, semi-insulating (SI) substrate upon which an n-type epitaxial layer is grown using vapor-phase epitaxy. This layer is typically 2 to 3 μm thick and is doped with sulfur to a net donor concentration of about 5×10^{15} cm^{-3}, resulting in pinch-off voltages of 15 to 30 V. Ohmic contact metallization using Ni-Ge-Au is patterned, and the wafer is then bombarded with low-energy protons to produce a shallow SI region (the purpose of this implant is discussed in detail below). A 450°C anneal for 30 s completes the ohmic contact formation. The channel isolation is produced using a 400-keV proton implant at a dose of 1×10^{14} cm^{-2}. The wafer is then metallized by evaporating 100 Å of Ti and 1000 Å of Au. The gate pattern is defined in this metallization by selective

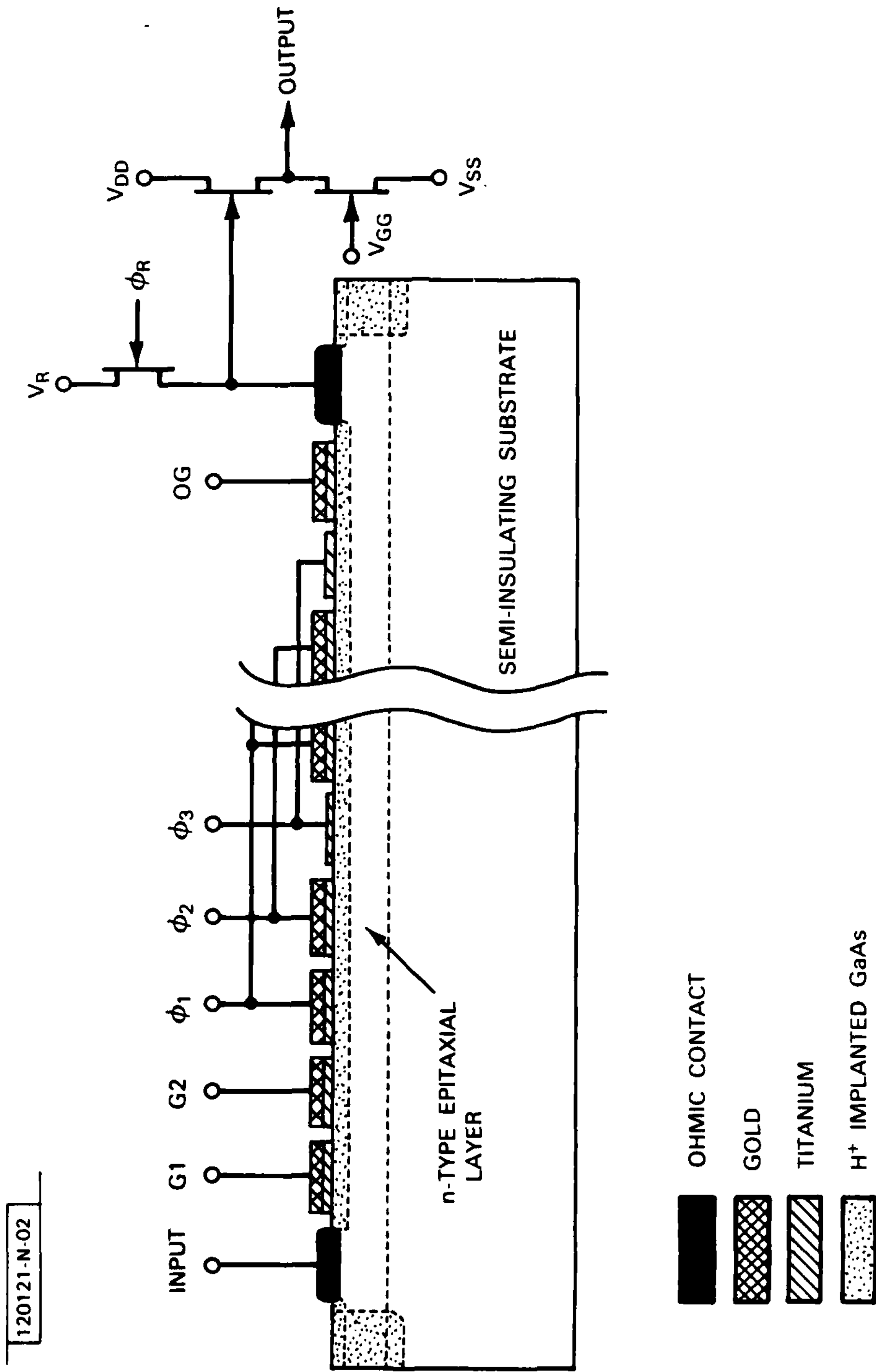

Fig. 4-1. Schematic cross section of a three-phase GaAs Schottky-barrier CCD.

etching, producing gates on 11-μm centers, with the gaps between gates averaging 1.7 μm. The ϕ_3 semitransparent gates are produced by selectively etching the Au from these gates, leaving the thin Ti. The final steps in the fabrication include plasma-assisted deposition of Si_3N_4 for crossover insulation and scratch protection, followed by a second Ti/Au layer for crossovers and bonding pads.

A photograph of a finished 16-stage device is shown in Fig. 4-2. The semitransparent ϕ_3 gates are the darker set of electrodes. The output circuit, shown in Fig. 4-1 as three FETs, can be seen at the right-hand end of the gates. This circuit, common on Si CCDs, is a gated charge integrator, and uses a reset FET to precharge the output ohmic contact to a reset voltage V_R, and two FETs in a source-follower configuration to sense the voltage drop on the ohmic contact when it receives a charge packet.

Two unique requirements for this device are the semitransparent gates and a channel with a high pinch-off voltage. For a transparent gate, we have

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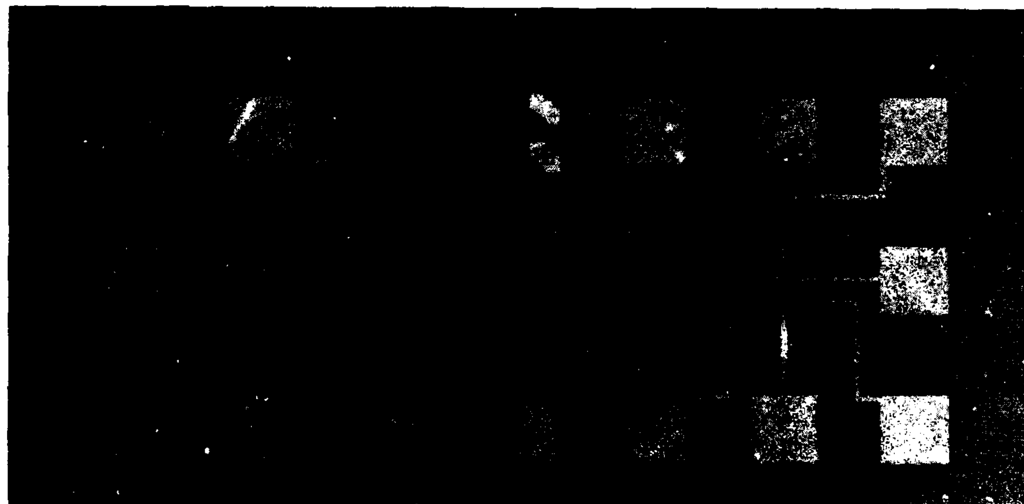

Fig. 4-2. Photograph of a 1 × 16-stage CCD whose cross section is depicted in Fig. 4-1.

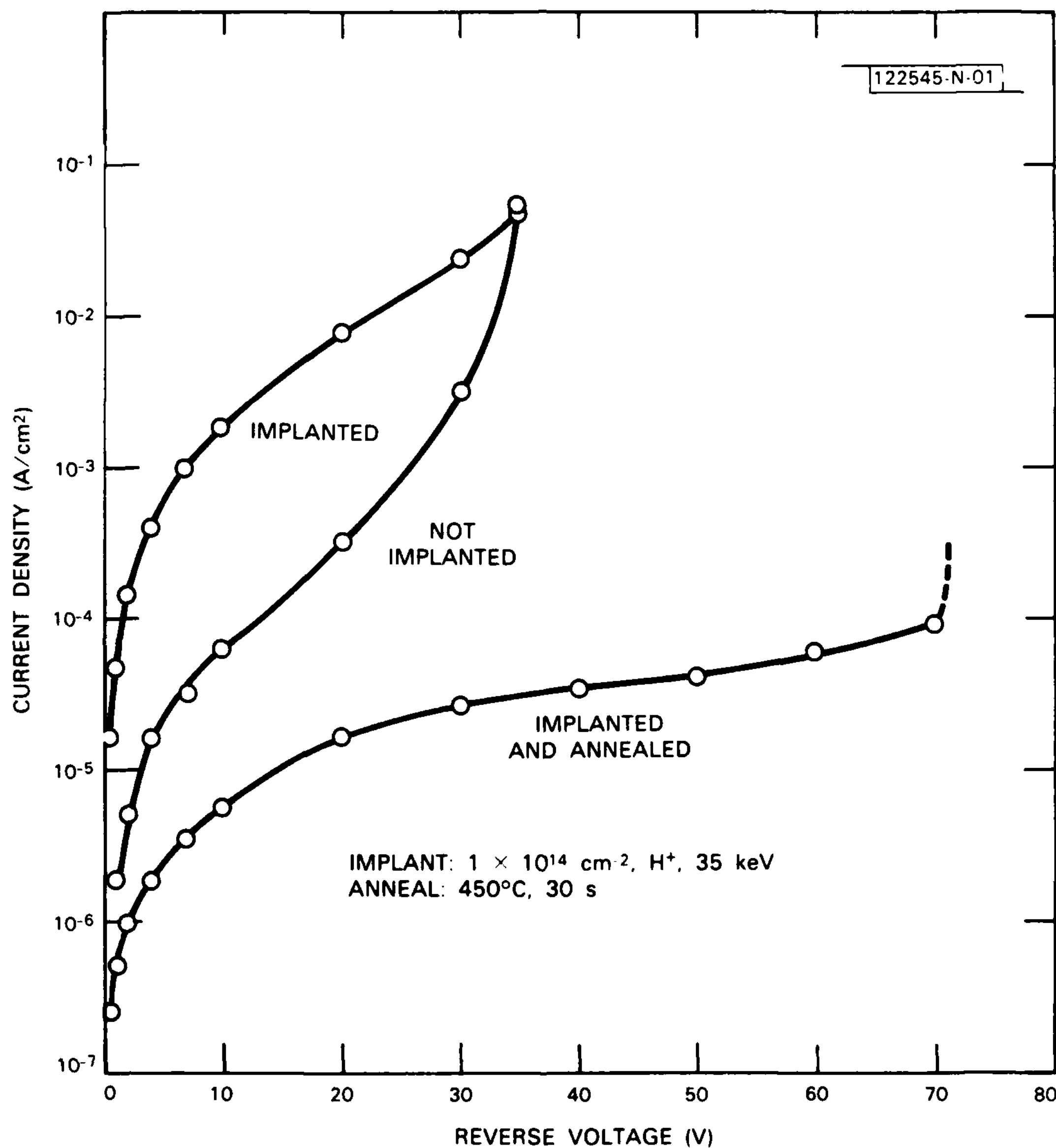

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Fig. 4-3. Reverse I-V characteristics of Schottky barriers having no shallow proton implant, an implant but no anneal, and an implant together with a 450°C anneal for 30 s.

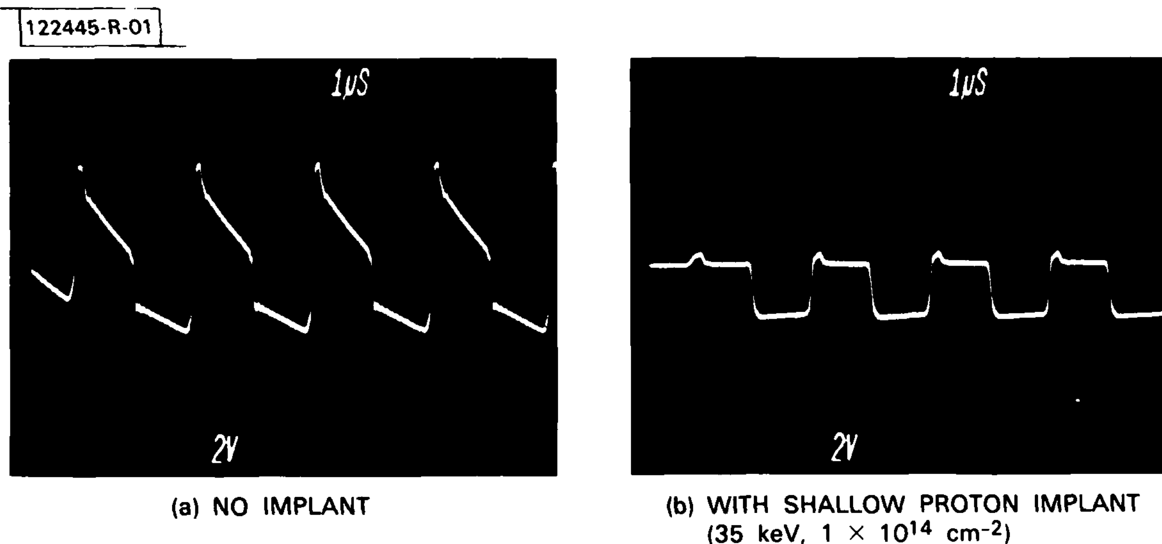
found that thin Ti is a satisfactory choice. A 100-Å Ti film has a sheet resistance after device processing of about 500 Ω/□ , and films of this thickness on glass substrates have an optical transmission of about 0.4 at a wavelength of 0.90 μm. Calculations of modulation vs channel pinch-off voltage V_p show a monotonic increase in modulation with V_p, with fairly high values of V_p needed for useful modulation.[1] For example, a transmission increase of 25 percent through the cell is predicted for 0.89-μm radiation, as a CCD well with $V_p = 25$ is filled with charge. CCD operation with pinch-off voltages of this magnitude is somewhat difficult because of breakdown problems. In addition, we have observed that devices operated at the required elevated voltages suffer from excess surface and bulk leakage currents which not only increase CCD dark current but also are detrimental to the FET output circuit performance. The most serious cases of this leakage have been associated with the deposition of the Si_3N_4.

We have found that a solution to the leakage problem consists of creating a shallow, SI region, formed by low-energy proton bombardment at the surface of both the CCD and FET channels. This technique has been described previously[2,3] for use in reducing gate leakage of GaAs FETs. This SI region effectively passivates the surface and reduces the leakage to the output circuit. On devices made to date, this implant is performed at energies of either 35 or 70 keV with a dose of 1×10^{14} cm^{-2}. We have also found that the wafer must be annealed after the implant, and we have found it convenient to use the ohmic contact anneal step for this purpose.

The improvement in reverse leakage and breakdown voltage after passivation can be seen in the Schottky-barrier I-V characteristics shown in Fig. 4-3. A device with no passivating implant exhibits a soft breakdown at about 35 V, while a device with a 35-keV implant performed after the ohmic contact anneal is likewise soft, but has higher leakage. A device receiving the implant before this anneal exhibits low leakage and a breakdown voltage of more than 70 V. Furthermore, the measured leakage for this diode includes a substantial component of current flow from the Schottky-barrier contact to the channel ohmic contact via the SI regions; the true Schottky-barrier

reverse leakage for the annealed device is therefore much lower than the measured values in Fig. 4-3.

The effects of this leakage reduction on output circuit performance can be seen in Fig. 4-4(a-b), which shows the FET output waveforms from devices on the same wafer (a) without and (b) with a 35-keV proton implant and anneal. In these measurements, charge packets are transferred to the output ohmic contact, each packet causing a 2-V drop in the output level. A short reset pulse ϕ_R is applied to the gate of the reset FET to restore the ohmic contact potential to V_R. With ϕ_R off, the ohmic contact is floating and, in the absence of surface leakage and dark current, would remain at the potential V_R until the next charge packet arrives. The marked negative slope of the upper waveform is evidence of a steady current flowing from the ohmic contact node. This current I can be calculated from the output slew rate dV/dt as $I = (C/G)dV/dt$, where $C \simeq 0.7$ fF is the output node capacitance and $G \simeq 0.7$ is the source follower gain. The slew rate of about 2 V/μs for the



(a) NO IMPLANT

(b) WITH SHALLOW PROTON IMPLANT (35 keV, 1 × 10^{14} cm^{-2})

Fig. 4-4. Oscilloscope photos showing CCD output waveforms from a device (a) without and (b) with proton passivation implant.

unpassivated device implies a current of 71 nA, while measurements on the passivated device gave a rate of only 6 mV/μs for a current of 0.2 nA. This latter current could be totally accounted for by dark current, implying that the surface leakage component is less than 0.2 nA. In these devices, the potential difference between the output ohmic contact and the reset and output gates is about 30 V.

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4.2 THE MICROWAVE SILICON PERMEABLE BASE TRANSISTOR

Silicon permeable base transistors (SiPBTs) have been fabricated which exhibit a maximum available gain at 2 GHz of 11 dB and a 6-dB/octave decrement, resulting in a maximum frequency of oscillation (f_{max}) of 10 GHz. Although the ultimate f_{max} of the Si device is anticipated to be lower than the corresponding device in GaAs (see Ref. 4), simulations by Alley et al.[5] and Snyder et al.[6] indicate that the Si device should be superior to present Si bipolar transistors. Coupled with the advanced state of Si processing and integrated circuit technology, this level of performance will make the SiPBT an attractive device for high-speed integrated circuits.

A three-dimensional breakaway drawing of the SiPBT is shown in Fig. 4-5. The device consists of four main regions: the n^+ substrate, a planar n-Si epitaxial pocket in a relatively thick SiO_2 isolation layer, an etched square-wave groove structure with 3200-Å period in the n-Si region, and a deposited W film which forms both the base grid as well as the collector contacts at the Si finger tops.

Although the SiPBT differs in structural detail from the GaAs version, in which the W base region is entirely encapsulated by the n-collector region, the principle of operation remains the same. Electrons from the emitter region are constrained by the SiO_2 field isolation to flow between the W fingers into the multichanneled collector region. The W fingers at the bottom of the etched-groove structure form a Schottky barrier that is used to modulate this current.

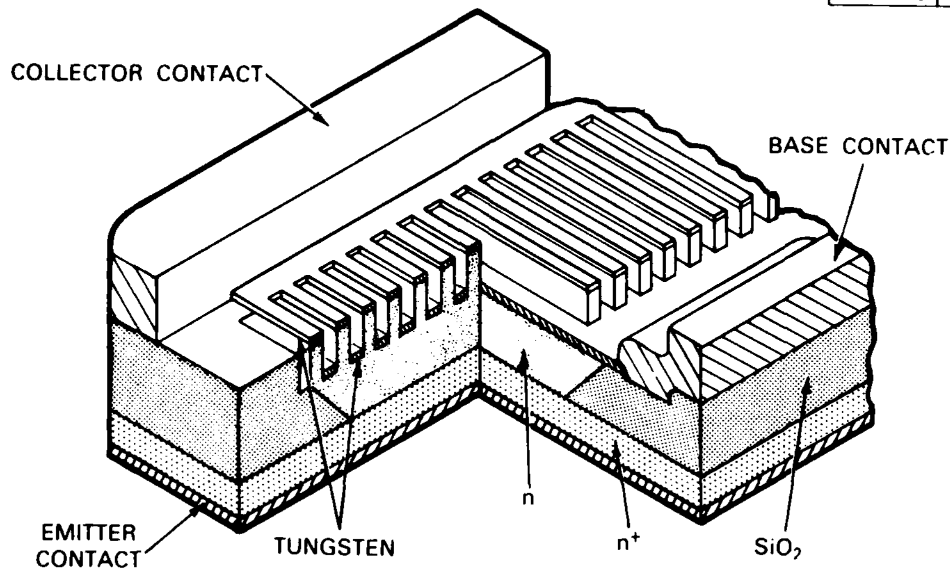

Fig. 4-5. Silicon permeable base transistor (SiPBT). The 3200-Å-period groove structure is formed by x-ray lithography and RIE. A thin film of W at groove bottoms forms base, while the etched Si region is collector.

The fabrication details are described elsewhere.[7] Figure 4-6(a-c) outlines the major processing steps which consist of (a) a selective area epitaxial growth process for dielectric isolation, (b) x-ray lithography combined with reactive ion etching to produce the 3200-Å-period etched-groove structure in Si, and (c) base Schottky metallization and base, emitter, and collector contact metallizations. A completed SiPBT is shown in Fig. 4-7.

The common emitter characteristics from one of the devices is shown in Fig. 4-8. About 50 percent of the 6000 devices on this 2-in. wafer exhibited DC transistor characteristics; about 5 percent had characteristics similar to those shown in Fig. 4-8. Both positive and negative biases were applied to the base for these curves; the $V_{BE} = 0$ is the third from the bottom.

Three typical devices were tested from microwave performance. The maximum available gain calculated from measured S parameters of the devices is shown in Fig. 4-9. The f_{max} was measured to be 10 GHz and the maximum

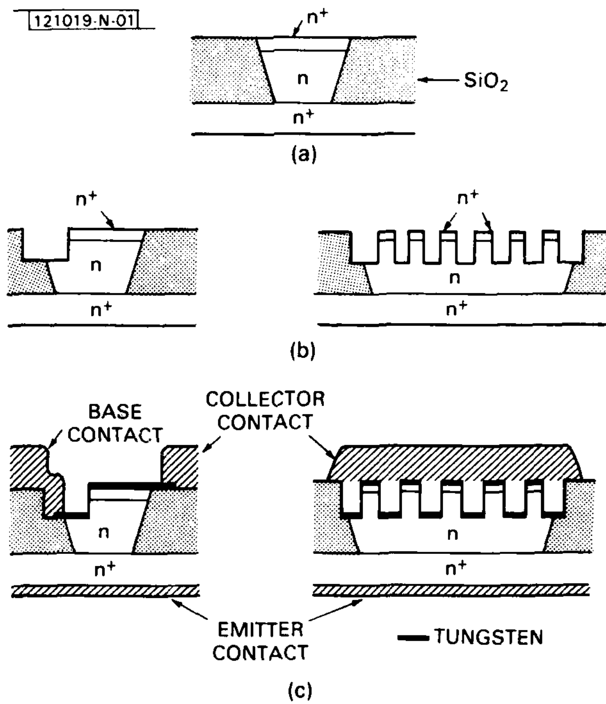

Fig. 4-6. Fabrication sequence of SiPBT. (b) and (c) are cross-sectional views both parallel and perpendicular to etched grooves.

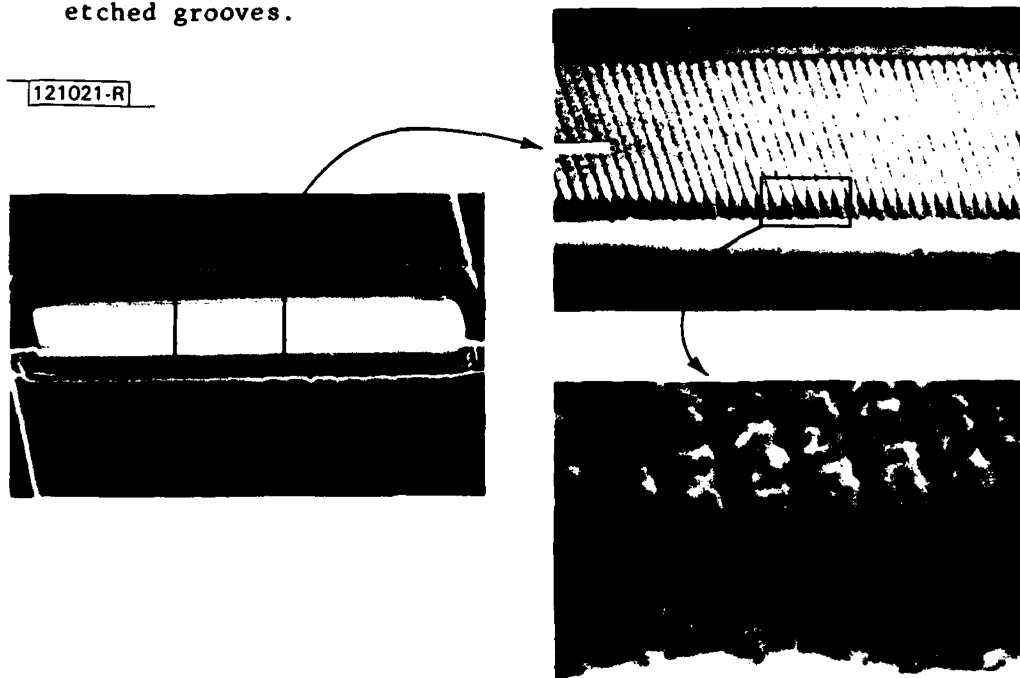

Fig. 4-7. An SEM micrograph of a completed SiPBT. Insert shows a closeup of 3200-Å-period grooves as viewed from base contact.

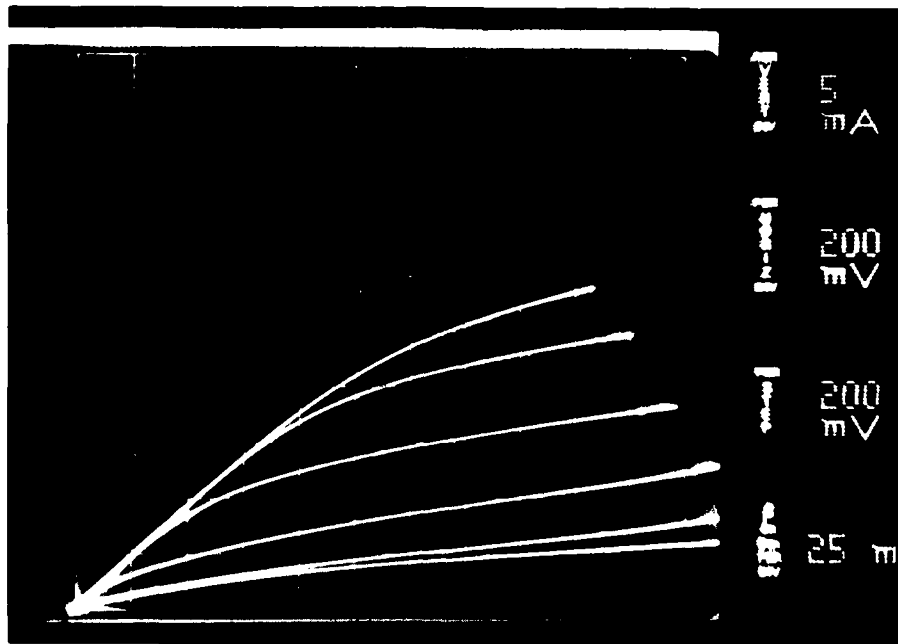

Fig. 4-8. Three-terminal I-V characteristics of one of the better SiPBTs. Transconductance is on order of 35 mS. More typical values are between 10 and 25 mS.

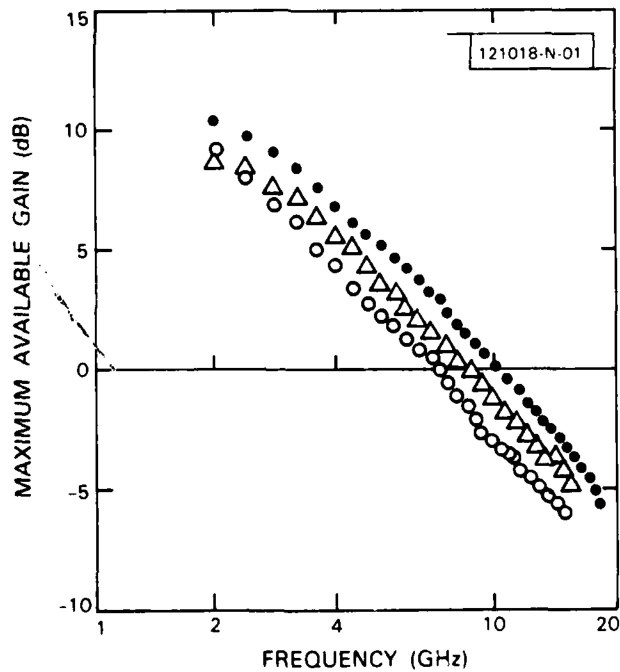

Fig. 4-9. Maximum available gain f_{max} vs frequency for three devices on same wafer.

gain at 2 GHz was 11 dB. The transconductances of these devices, measured with V_{CE} = 5 V, are greater than 20 mS with the base-to-emitter voltage forward-biased in the range 0.0 to 0.6 V. Collector currents are in the 30-mA range. Gain measurements in the 2- to 15-GHz region indicated a decrement of 6 dB/octave, as expected from the hybrid pi model. Preliminary results of device modeling currently in progress indicate that the measured transconductances are typically a factor-of-four times lower than predicted. We believe that, with fabrication improvements and process optimization, f_{max} can be improved substantially, resulting in an extremely fast Si device for integrated circuits.

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4.3 REDUCTION OF PHOTOVOLTAIC-CELL REVERSE BREAKDOWN BY A PERIPHERAL BYPASS DIODE

Photovoltaic (PV) modules consist of series strings of individual cells wired in a parallel array. When cracking or shadowing of an individual cell occurs, its short-circuit current decreases below that of other cells in the series string. The affected cell will tend to dissipate power, causing it to heat. The power dissipated by a PV cell operating in this "hot-spot" failure[8] mode is determined by the current forced through the cell and the cell's reverse breakdown voltage V_{br}. Cell heating can be reduced by decreasing V_{br}, but the method must be easy to implement and be cost effective.[9,10] Ideally, the V_{br} reduction technique should be distributed throughout the cell so that the protection is not lost when the cell cracks. A direct approach based on altering the doping to produce a low V_{br} is inappropriate because this will reduce cell efficiency. No alternative method for accomplishing these objectives has been proposed previously.[11]

The approach discussed in this work achieves low V_{br} by fabricating an isolated, narrow diode around the periphery of the PV cell and connecting this diode across the solar-converting portion of the cell. This method is

tolerant of cell cracks, and implementation of the peripheral protection diode requires only the addition of a few additional processing steps. Rather than diffusing two separate diode areas, the PV cell is produced in the conventional manner, with a single diffusion covering the entire top surface of the wafer. The peripheral diode, as indicated in Fig. 4-10, can be isolated from the remainder of the cell using a microscopic groove etching technique to cut through the diffusion on the top of the cell.

Two techniques for implementing bypass protection with a peripheral diode were investigated. In one implementation, the forward conduction of a conventional diode that is connected antiparallel across the PV cell provides the protection. In the other, the low reverse breakdown of a backward diode[12] connected in parallel with the PV cell is the protective device. The conventional diode approach requires only a simple addition (silicon-etch step) to the processing sequence, but additional interconnections between cells are needed. The backward diode uses standard interconnects but

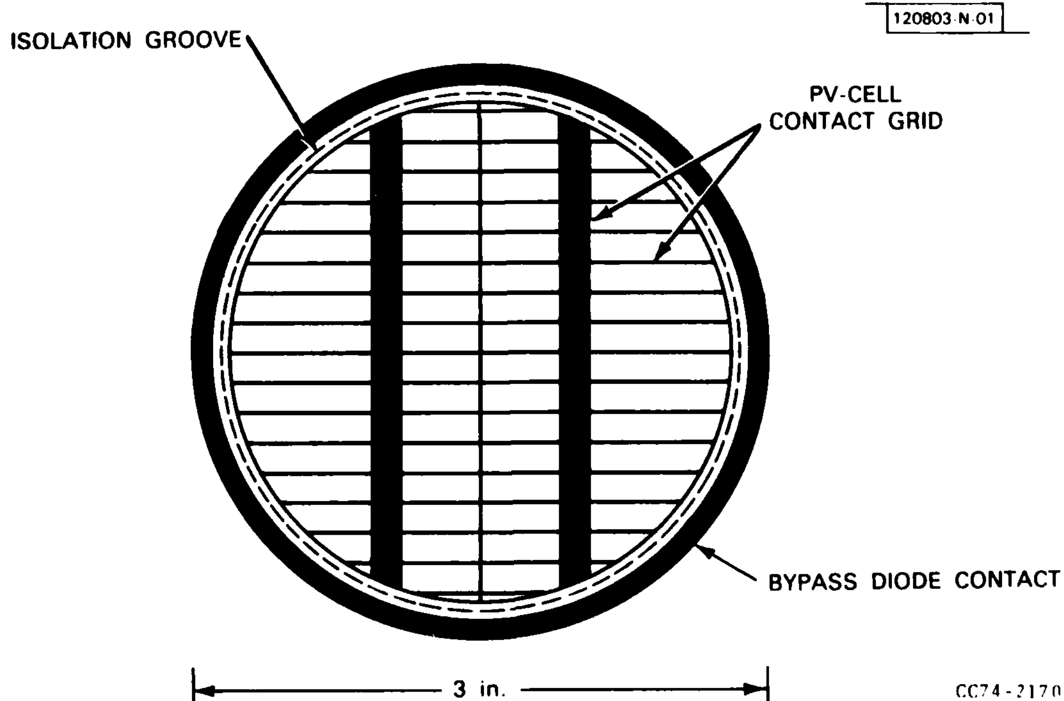


Fig. 4-10. Layout of wafer including peripheral-diode region isolated from central PV-cell region.

requires an additional doping step in the peripheral-diode region as well as an isolation etch.

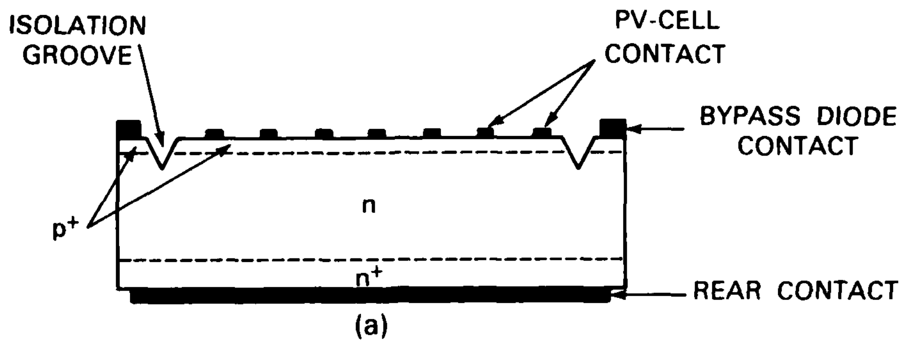
An edge view of a PV cell augmented by a standard diode to provide the bypass protection is shown in Fig. 4-11(a). For specificity, a p-on-n cell is shown, but all the following holds equally well for the reverse polarity. Isolation of the peripheral diode is accomplished, after metal plating of front and back, by a deep (>1 μm) CP4 isotropic wet Si etch, or a CF_4/O_2 plasma etch. The central PV portion of the wafer is protected with photoresist.

Schematically, the wafer can be represented as shown in Fig. 4-11(b). Since the bypass diode was produced by the same process that produced the PV cell, both diodes have the same reverse breakdown. Because the cathode of both the solar diode and the peripheral diode are common, the peripheral diode located on one cell is used to provide protection for the next cell in the series string, as indicated in Fig. 4-12. Thus, the simplicity of the processing has forced an additional complexity of interconnection.

In order to avoid this interconnection complexity, a means was sought for providing the desired protection through the reverse conduction of a parallel-connected diode. An edge view of the resulting structure is shown in Fig. 4-13(a). For processing reasons, this cell is shown as an n-on-p design, the opposite of the layout used for the conventional cell. The layer of the PV portion labeled n^+ and the layer of the peripheral backward diode labeled n^{++} are actually the same and are formed in the same step.

The schematic representation of the wafer is shown in Fig. 4-13(b). The bypass protection is achieved by tying the cathode of the low-reverse-breakdown backward diode directly to the cathode of the PV cell. The series interconnection of a PV cell with backward-diode protection is therefore identical to the interconnection of regular, unprotected PV cells, as shown in Fig. 4-14.

I-V curves for a PV cell, with and without the backward diode connected, are shown in Fig. 4-15(a-b). Operation of the PV cell in the first quadrant is virtually unaffected by the addition of the backward diode. In fact, an I-V curve of the backward diode itself indicated no forward tunneling



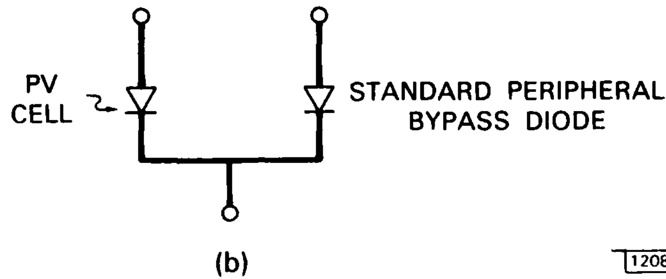


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Fig. 4-11. (a) Edge view of PV cell, and (b) schematic of cell with a standard diode in peripheral location for bypass protection.

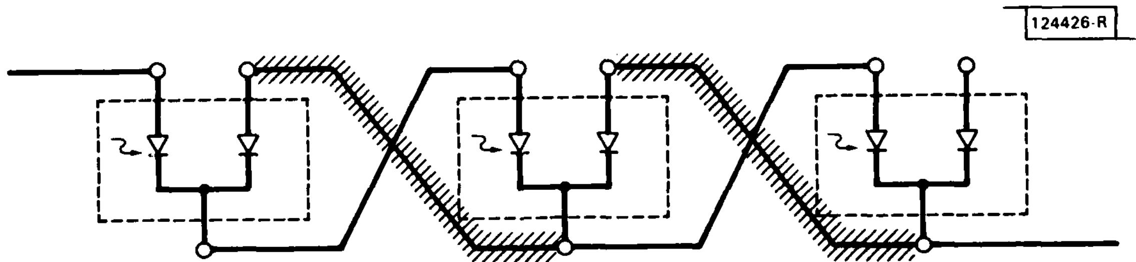
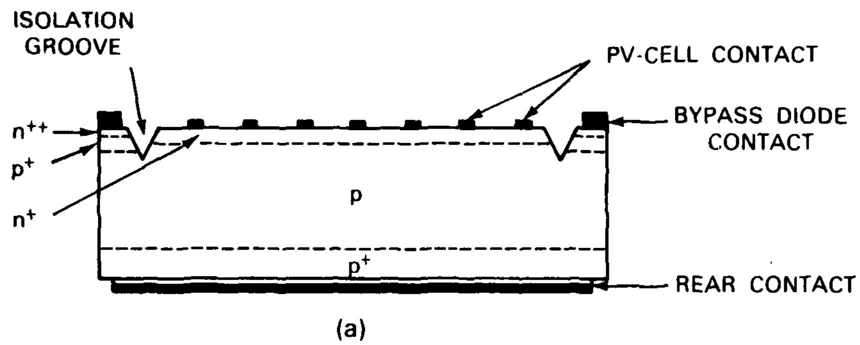


Fig. 4-12. Series interconnection of PV cells using standard peripheral diode. For a particular wafer, PV diode is protected by standard diode on wafer on left. Leftmost PV diode is unprotected. Additional interconnect required for this scheme is indicated in cross-hatching.



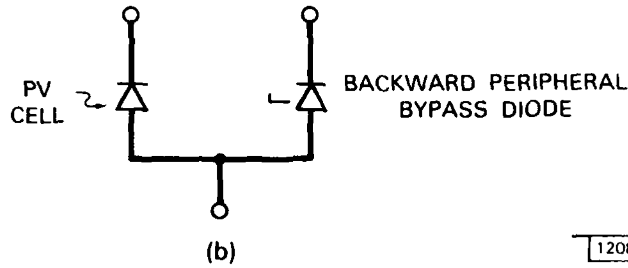


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Fig. 4-13. (a) Edge view of PV cell, and (b) schematic of cell with a backward diode in peripheral location for bypass protection.

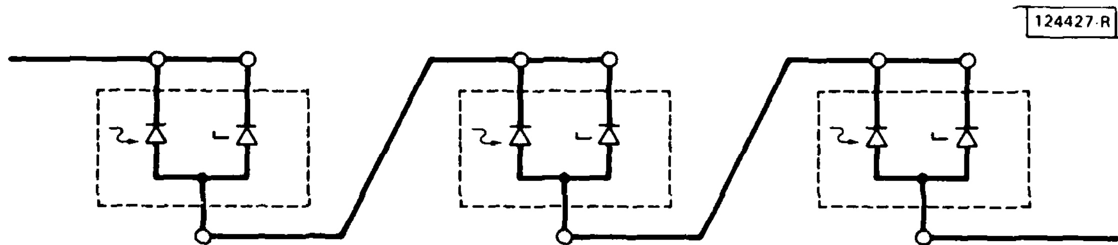

Fig. 4-14. Series interconnection of PV cells with backward-diode bypass protection.

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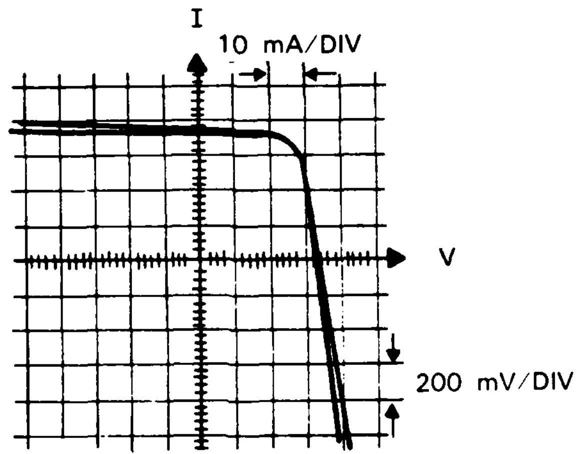
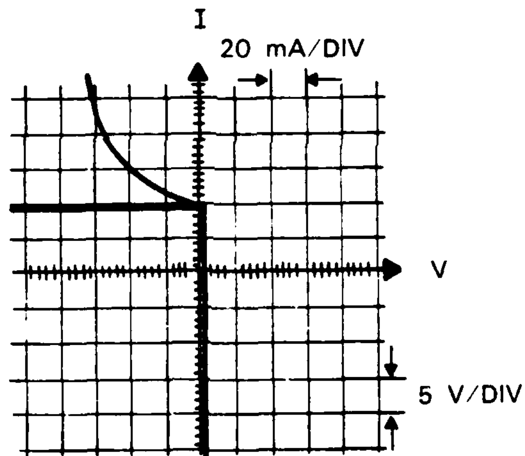


(a)



(b)

Fig. 4-15. I-V curve of PV cell with backward-diode bypass protection: (a) expanded scale indicating first-quadrant operation with and without backward diode connected in parallel, and (b) normal scale indicating reduced breakdown voltage of PV cell with backward diode.

current. Reverse breakdown of the PV cell alone was measured to be more than 150 V; the addition of the backward diode reduces V_{br} to approximately 15 V. The predicted V_{br} for an abrupt junction with the doping level used is about 2 V, and although the 15-V breakdown of the experimental diode as fabricated was higher than the predicted value, it is still an order-of-magnitude below the V_{br} of the PV cell.

Work is in progress to characterize the doping profile that was obtained with the first-generation process. This information will permit the establishment of process modifications necessary to fabricate a backward diode with a breakdown in the 2- to 3-V range. The present results indicate that a significantly lower reverse breakdown can be achieved with a simple additional implant. The complexities normally associated with fabrication of a "true" backward diode (in the RF sense) do not carry over to the present case because of the relatively loose requirement on reverse-breakdown voltage.

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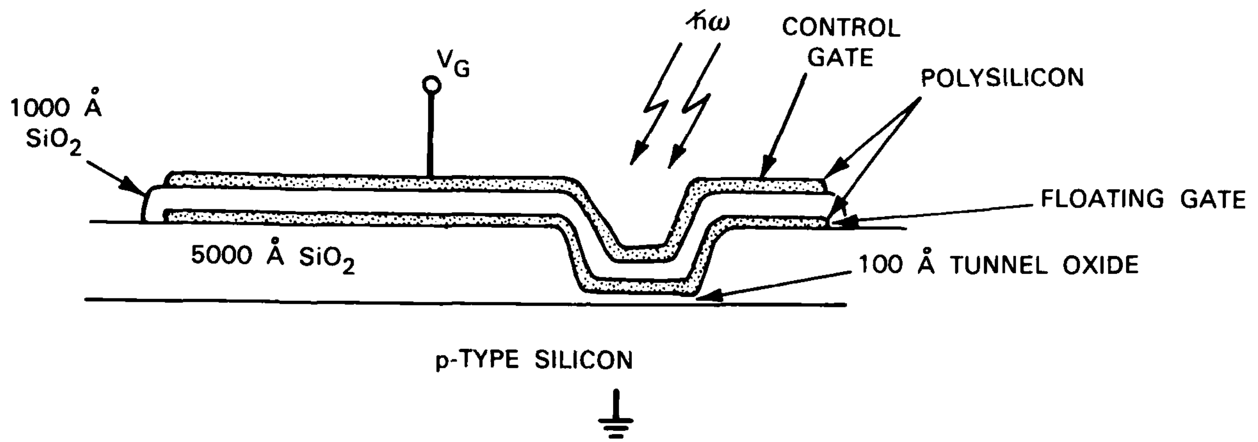
5. ANALOG DEVICE TECHNOLOGY

5.1 NONVOLATILE ANALOG MEMORY: FLOATING-GATE DEVICES

Extremely long retention (>10 years) of binary data is realized in floating-gate memories in which the signal charge is stored on an insulated polysilicon island.[1] We have tested the suitability of structures of this type for nonvolatile analog memory using Fowler-Nordheim[2] rather than avalanche injection. Discrete floating-gate capacitors were constructed, and nonvolatile storage of analog levels was demonstrated. The device structure is shown in Fig. 5-1(a). A 5000-Å-thick field oxide is thermally grown on 30- to 50-Ω-cm p-type silicon. A window is etched through this oxide; the thin (≈100 Å) tunnel oxide is thermally grown in this area. A layer of polysilicon is deposited and defined to form the floating gate and subsequently oxidized thermally to a thickness of 1000 Å. A second polysilicon layer is deposited, defined, and doped to form the control gate. The ratio of control gate to memory window (tunnel oxide) area is 10:1, permitting the establishment of much stronger electric fields in the tunnel oxide than in the control oxide.

The linearity of the charge storage process was tested using the optical technique described in Ref. 3. Minority carriers generated in the depletion layer by the controlled photon injection migrate to and along the silicon surface to the deeply depleted region below the tunnel oxide. With a sufficient concentration of these minority carriers at the Si/SiO_2 interface, the electric field in the tunnel oxide is large enough that Fowler-Nordheim tunneling of these carriers to the floating gate occurs and writing is accomplished. Erasure is performed by similar tunneling between the floating gate and an accumulated substrate.

Results of a sequence of erase/write (E/W) operations are shown in Fig. 5-1(b) in the form of a family of C(V) curves measured from the control gate to the substrate. These curves have a peculiar two-level shape because the equivalent circuit contains two parallel capacitors with different oxide thicknesses between the floating gate and the substrate. During these ramped



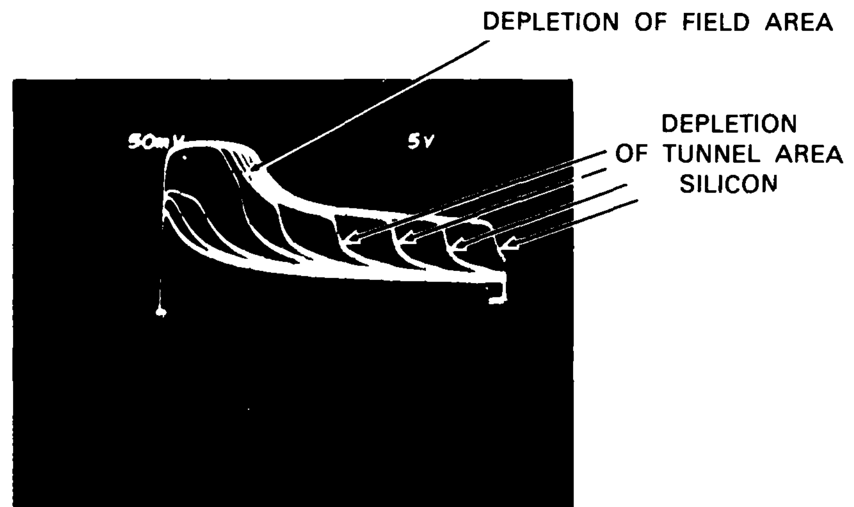


Fig. 5-1. Floating-gate nonvolatile analog memory: (a) structure, and (b) capacitance-voltage curves obtained after storage of linearly increasing signals in this device.

C(V) measurements, the gate voltage is swept from accumulation to deep depletion [-20 to +20 V in this case] in 100 μs. The dielectric relaxation time of the polysilicon gate which, for ease of fabrication, was not doped is on the order of a few seconds; thus, the distribution of charge along the gate does not change during the measurement. The leftmost curve corresponds to the erase operation, while each curve to its right was taken after a write operation, linearly increasing amounts of signal charge being used with each successive write. Erasure (V_G = -30 V) was done between each write (+30 V). The linear spacing of the flatband voltages of the tunnel area clearly demonstrates a linear transfer function from input to storage. Charge retention was found to be better than MNOS devices; E/W endurance was not tested.

Before the conclusion can be drawn that this type of floating-gate device can be integrated with a device which uses a surface-charge-addressed technique (as in the MNOS/CCD),[4] it must be ascertained that hot-carrier injection is not occurring. Hayashi et al.[5] constructed an analog optical memory which relied on the acceleration of photo-generated electrons in the depletion field between the point of carrier-pair generation and the silicon surface. These hot electrons then entered the SiO_2 conduction band and drifted to a floating gate. Because of collisions in the depletion layer, only a small fraction of the electrons arrive at the silicon surface with sufficient energy to surmount the barrier; in fact, for lightly doped substrates such as used in the structure of Fig. 5-1(a), injection efficiencies of less than 10^{-6} were measured by Hayashi et al.[5] In these experiments, a nearby drain diffusion collected the electrons which had insufficient energy to enter the floating gate, thereby maintaining the depletion layer.

In the capacitor structure of Fig. 5-1(a), no such drain is present. If an injection efficiency of 10^{-6} is assumed, the depletion layer would collapse before the flatband voltage had been shifted more than a few tens of microvolts. It can thus be concluded that Fowler-Nordheim tunneling, which is compatible with charge-addressed techniques, is the dominant means of injection.

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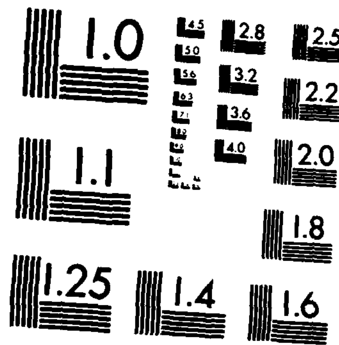

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5.2 ADAPTIVE CW FILTERING BY CHIRP TRANSFORMATION USING OVERLAP SUMMATION

When SAW chirp-transform adaptive filtering[6] was first described several years ago, it was found that CW filtering posed a particularly troublesome problem. Continuous inputs had to be segmented and each segment processed individually, which produced segmentation artifacts at the system output. At that time it was determined that the width of these artifacts had to be minimized by using chirp filters with the largest reasonable time-bandwidth products. In this report a process called overlap-summation is described that does more than minimize the width of these segmentation artifacts, it actually suppresses them at only a modest expense in device time-bandwidth product. A closer investigation of the underlying problem will be made first, then the technique will be described.

Figure 5-2 shows a chirp-transform adaptive filter (CTAF) configured as a notch filter. The continuous input to the system is shown segmented, and

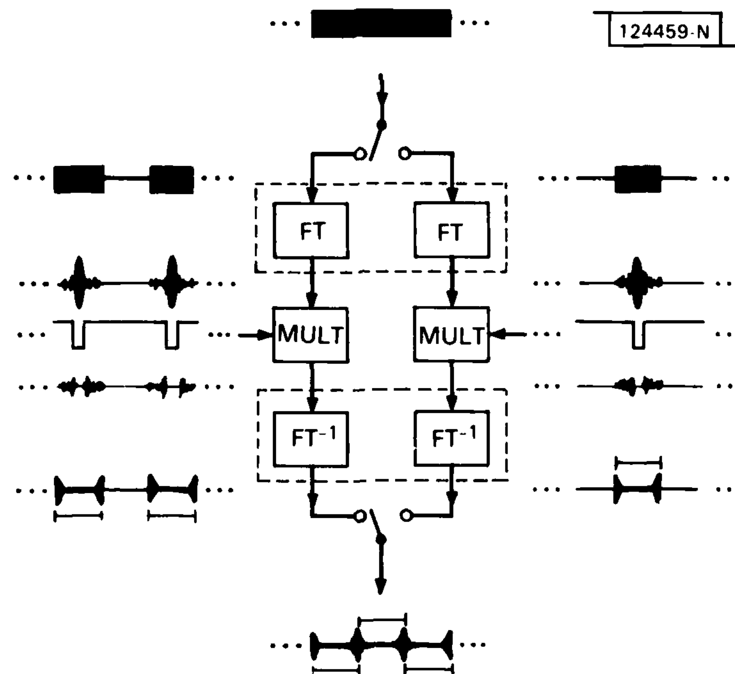

Fig. 5-2. Conventional chirp-transform system operating as a CW notch filter.

each segment is processed by alternating between two identical channels. Each channel consists of a Fourier-transforming subsystem at the front end, an inverse-Fourier-transforming subsystem at the back end, and a multiplication stage in-between. A signal is Fourier transformed and, while in the Fourier domain, is modified to produce the desired filter output following inverse Fourier transformation. Each segment of the continuous input is individually Fourier transformed. The Fourier transform of each segment of the continuous tone shown here, however, has side lobes not found in the CW spectrum. After each Fourier transform is notched, the side lobes remain. Since a major portion of the desired spectrum must be kept, overly wide notching or excision cannot be permitted. The remaining side lobes result in artifacts at the output. In Fig. 5-2 it can be seen that, when the full output is reconstructed in the conventional manner by alternating between the two channel outputs, the segmentation artifacts are retained. If the tone can be suppressed at the center of each segment by 40 dB and the artifacts represent 10 percent of the overall energy, the tone has actually been suppressed by only 10 dB. Suppression of these artifacts using overlap summation can be understood by investigating the way that a continuous signal is processed by an ideal notch filter.

Figure 5-3(a-b) shows the notch filtering of a continuous input accomplished using two distinct conceptual approaches. In Fig. 5-3(a) the signal is being processed continuously. Since this single-frequency tone falls at the center frequency of the filter, it is suppressed at the filter output by 12 dB and, as expected, is completely free of any kind of segmentation artifact. In Fig. 5-3(b) the tone has been segmented into two signals whose sum produces exactly the continuous input. Both of these are individually processed by the same filter used to process the continuous tone. As before, however, segmentation artifacts are produced with the filtered output segments. But, from the principles of linearity and superposition it is known that the overlapping sum of these two outputs must be identical to the output for the continuous case. The artifacts, therefore, must disappear after summation. Suppose that the two filters in Fig. 5-3 represent the two channels in a CTAF and the segmented inputs represent the inputs to these channels. It is appropriate to determine the

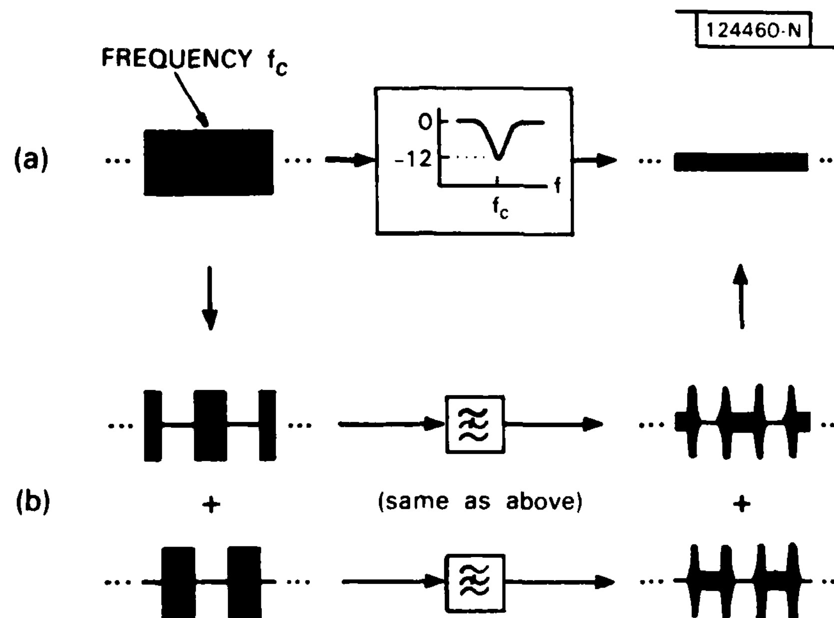

Fig. 5-3. Conceptual ideal notch filter operating on (a) CW tone and (b) segmented tone. In latter case, coherent summation of output channels removes segmentation artifacts.

conditions that must be met in order to obtain artifact suppression from the CTAF. First of all, valid outputs from the two channels must be permitted to overlap during summation. Although an infinite overlap is theoretically required for a band-limited filter response, realistically the overlap can be fixed to a fraction of a segment and still provide adequate performance when reasonably smooth spectral editing is used. The second condition is that the two channels in the CTAF be identical and coherent. To closely approximate this condition, a bilateral[7] structure should be used for the two subsystems. This structure is best described by comparison with the conventional approach.

Figure 5-4 shows the structure of the two chirp-transformation subsystems configured both with the conventional and bilateral structures. In the figure, E represents chirp-filter expanders, C is the chirp-filter compressors, and μ is their chirp slopes. Note that the conventional

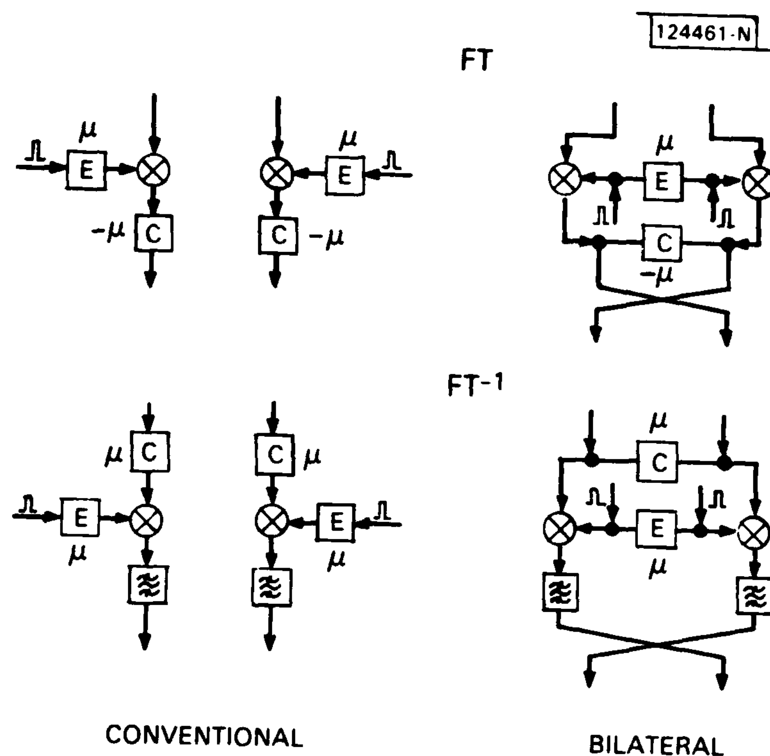

Fig. 5-4. Conventional and bilateral-type chirp-transform subsystems.

structure uses two distinct channels. In the bilateral structure, however, the chirp filters are shared by the two channels. (Each of the two ports on all devices in this structure function alternately as input and output. Couplers are used to separate inputs and outputs, and noncoincidence is necessary to prevent contamination between the two due to finite coupler feedthrough.) Because the devices are shared and the system performance is dominated by their characteristics, coherence is maintained between the two channels in the bilateral structure. This would be difficult to obtain using the conventional approach.

Realization of the output overlap is dependent upon timing and device characteristics. No overlap between the outputs of the two channels is obtained when the duration of each system output segment equals the duration of the input segmentation window. This will be considered as zero fractional overlap. To prevent contamination between consecutive outputs in each channel, the output duration cannot exceed twice the duration of the input window. This maximum value will be considered a fractional overlap of one. As this maximum value is approached, however, the time-bandwidth products of

the chirp filters required to realize the overlap go to infinity. This statement can be shown graphically. In Fig. 5-5 a curve is shown that represents the time-bandwidth product of the largest device in the CTAF plotted as a function of fractional overlap. This curve has been normalized to the time-bandwidth product of the system given by the product of the duration of the input and the Fourier-transform bandwidth. As a basis for the determination of a reasonable overlap, another curve has been plotted in Fig. 5-5. For a given overlap, this curve specifies the minimum width of a notch in the Fourier domain for which the segmentation artifacts at the output will be canceled. This has been normalized in frequency to the width of a resolution cell given by the reciprocal of the input duration. A reasonable operating point has been indicated in this figure which requires a one-quarter fractional overlap for full artifact cancellation, and the resultant device TB product increases by only a third. The main lobe and first side lobes of the (sin x)/x spectrum of a segment of a CW tone could be deleted using this four-resolution-cell-wide notch. This is depicted by the inset in Fig. 5-5.

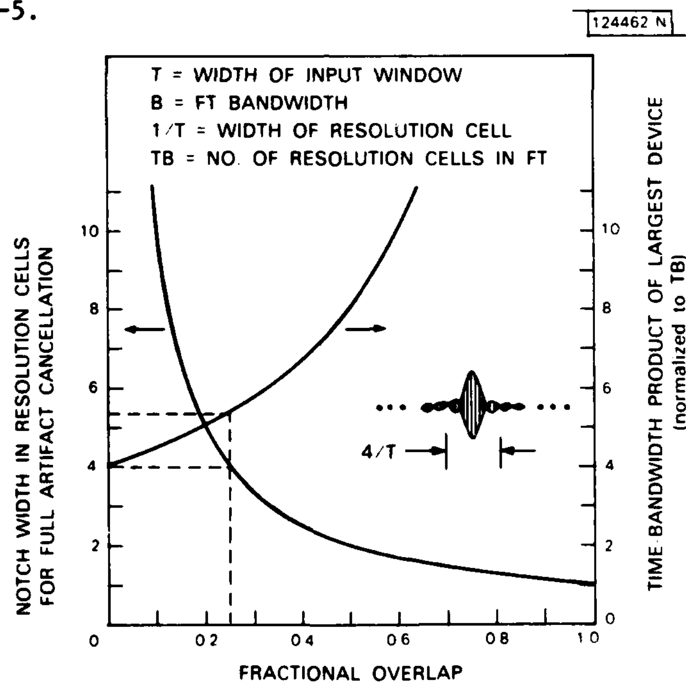

Fig. 5-5. Trade-off characteristics of device time-bandwidth product and notch width for improved chirp-transform system as function of fractional overlap of output segments.

This situation was demonstrated using an 8-MHz-bandwidth CTAF and SAW reflective-array chirp filters. The demonstration system was assembled using long lengths of flexible coaxial cable; unfortunately, because of poor isolation, large output spurious signals were produced. This made quantitative measurement of artifact cancellation capability impossible, but, nevertheless, adequately demonstrated the concept. Figure 5-6(a-c) shows channel-to-channel performance of the system. The two segmented versions of a continuous input tone are shown in Fig. 5-6(a). An undesirable dip in each segment is due to feedthrough of the impulse used in chirp generation as a result of inappropriate expander group delay. The Fourier transforms for each segment are shown in the two traces of Fig. 5-6(b). Following the example outlined in Fig. 5-5, the main lobes and first side lobes of these (sin x)/x spectra have been deleted. The two traces in Fig. 5-6(c) show the outputs with the expected segmentation artifacts. As required, about one-quarter fractional overlap is provided between the two outputs.

Figure 5-7(a-b) shows the full output after reconstruction. The output shown in Fig. 5-7(a) was obtained without overlap and the artifacts are evident. In Fig. 5-7(b), the artifacts have been suppressed to below the noise using overlap summation. (The residual spikes in this trace are not due to any ineffectiveness of the overlap summation process, but are the result of finite input-segmentation switch rise and fall times.) From past experience with chirp-transform systems and the bilateral structure, at least 40 dB of artifact cancellation is expected from this process. To verify this, a high-performance 100-MHz-bandwidth CTAF has been planned using rigid interconnections and appropriately designed and selected components.

In conclusion, the technique of overlap summation in chirp-transform systems will greatly increase the utility of such systems for adaptive excision of narrowband interference.

D.R. Arsenault

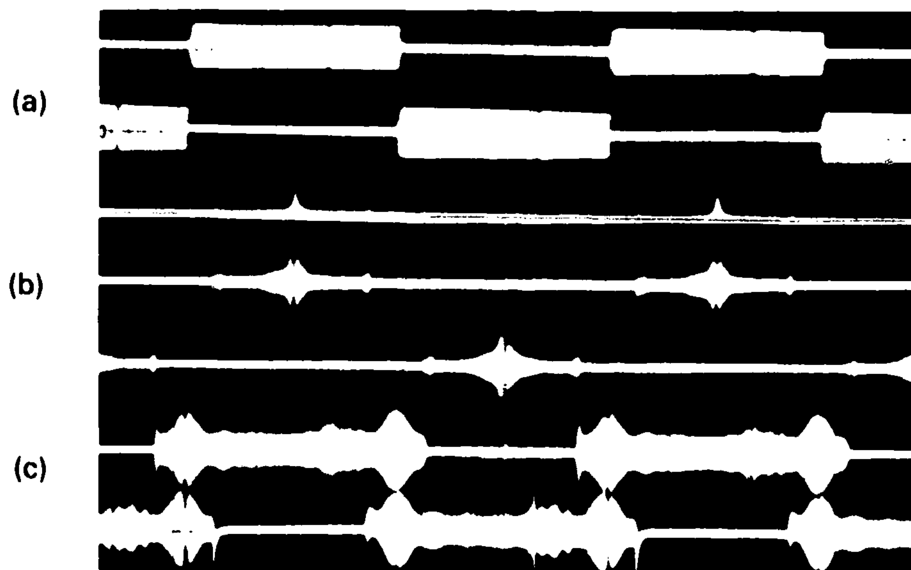

Fig. 5-6. Waveforms in improved chirp-transform system showing (a) segmented inputs, (b) notched Fourier transforms, and (c) separate inverse-transform outputs for each channel; time: 10 μs/div.

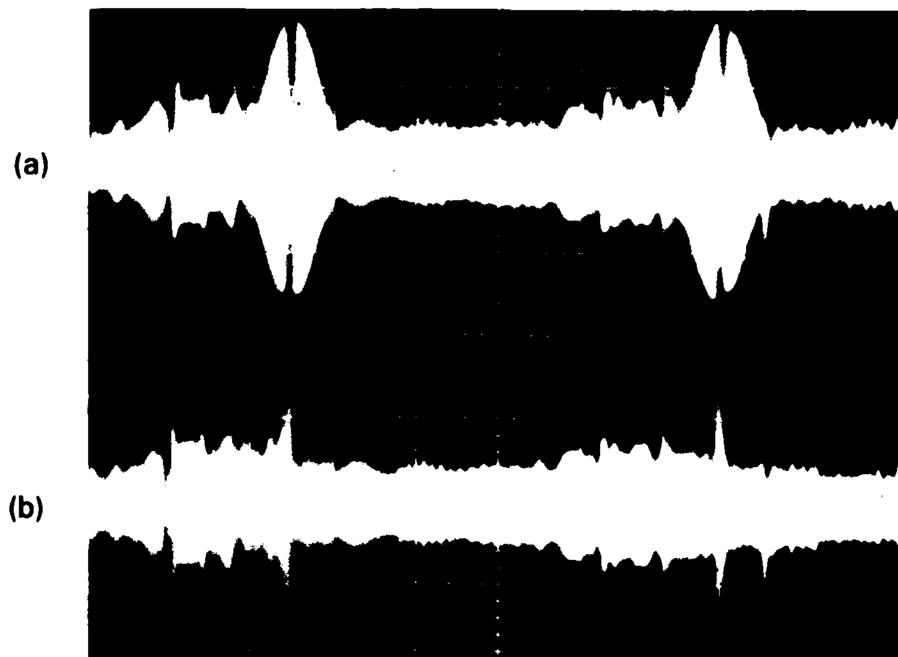

Fig. 5-7. Reconstructed chirp-transform output using (a) conventional method with persistent artifacts and with (b) overlap summation with artifact cancellation; time: 5 μs/div.

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER ESD-TR-82-105	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (*and Subtitle*) Solid State Research		5. TYPE OF REPORT & PERIOD COVERED Quarterly Technical Summary 1 August — 31 October 1982
		6. PERFORMING ORG. REPORT NUMBER 1982:4
7. AUTHOR(s) Alan L. McWhorter		8. CONTRACT OR GRANT NUMBER(s) F19628-80-C-0002
9. PERFORMING ORGANIZATION NAME AND ADDRESS Lincoln Laboratory, M.I.T. P.O. Box 73 Lexington, MA 02173-0073		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Program Element No. 63250F Project No. 649L
11. CONTROLLING OFFICE NAME AND ADDRESS Air Force Systems Command, USAF Andrews AFB Washington, DC 20331		12. REPORT DATE 15 November 1982
		13. NUMBER OF PAGES 106
14. MONITORING AGENCY NAME & ADDRESS (*if different from Controlling Office*) Electronic Systems Division Hanscom AFB, MA 01731		15. SECURITY CLASS. (*of this report*) Unclassified
		15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (*of this Report*)

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18. SUPPLEMENTARY NOTES

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19. KEY WORDS (*Continue on reverse side if necessary and identify by block number*)

solid state devices	photodiode devices	infrared imaging
quantum electronics	lasers	surface-wave transducers
materials research	laser spectroscopy	charge-coupled devices
microelectronics	imaging arrays	acoustoelectric devices
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20. ABSTRACT (*Continue on reverse side if necessary and identify by block number*)

This report covers in detail the solid state research work of the Solid State Division at Lincoln Laboratory for the period 1 August through 31 October 1982. The topics covered are Solid State Device Research, Quantum Electronics, Materials Research, Microelectronics, and Analog Device Technology. Funding is primarily provided by the Air Force, with additional support provided by the Army, DARPA, Navy, NASA, and DOE.

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