MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

DEVELOPMENT OF INDIUM-ANTIMONIDE
TWO-DIMENSIONAL CHARGE-INJECTION DEVICE ARRAY
WITH COMPLETE CHARGE TRANSFER

Final Report

Contract No. N00173-80-C-0281

Prepared for

Naval Research Laboratory
Washington, D.C. 20375

by

C.-Y. Wei and H.H. Woodbury

General Electric Company
Corporate Research and Development
Schenectady, N.Y. 12301

April 1983

83SRD025

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO. AD A127 716	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Development of Indium-Antimonide Two-Dimensional Charge-Injection Device Array with Complete Charge Transfer		5. TYPE OF REPORT & PERIOD COVERED Final Report
		6. PERFORMING ORG. REPORT NUMBER 83SRD025
7. AUTHOR(s) C.-Y. Wei and H.H. Woodbury		8. CONTRACT OR GRANT NUMBER(s) N00173-80-C-0281
9. PERFORMING ORGANIZATION NAME AND ADDRESS General Electric Company Corporate Research and Development P.O. Box 8 Schenectady, NY 12301		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Research Laboratory Washington, DC 20375		12. REPORT DATE April 1982
		13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

infrared imaging array, charge injection device (CID),

indium-antimonide (InSb), MOS capacitor

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A "non-etch-back" fabrication technique has been developed for an InSb two-dimensional infrared sensitive charge injection device. This report summarizes the first phase of a two phase program and describes the fabrication technique and test results on a set of experimental configurations.

The performance objectives relating to lag, well capacity, and charge transfer have been met. The second phase of this program has been initiated which is to fabricate the 16 x 64 2-D CID arrays.

DD FORM 1473 (1 JAN 73)   EDITION OF 1 NOV 65 IS OBSOLETE

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

TABLE OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

ABSTRACT

A "non-etch-back" fabrication technique has been developed for an InSb two-dimensional infrared sensitive charge injection device. This report summarizes the first phase of a two phase program and describes the fabrication technique and test results on a set of experimental configurations.

The performance objectives relating to lag, well capacity, and charge transfer have been met. The second phase of this program has been initiated which is to fabricate the 16 x 64 2-D CID arrays.

1. INTRODUCTION

The objective of this program is to demonstrate charge transfer in an InSb two-dimensional (2-D) charge injection device (CID) using a proposed "non-etch-back" array fabrication technique. In this technique the thickness of the oxide layers employed in the CID fabrication are those "as-deposited" by chemical vapor deposition (CVD). Degradation of oxide quality and thickness uniformity due to oxide etching is avoided. CID arrays of improved charge transfer, low lag, reduced crosstalk, and improved uniformity in responsivity and storage well capacity are expected. A high array yield can also be realized because of the planar processing used in the "non-etch-back" technique.

This program was divided into two phases. Phase I was to design and fabricate test arrays and study the charge transfer characteristics. This phase also included the design of a Navy IRST 16x64 2-D CID array if the test arrays showed good charge transfer characteristics.

In Phase II the Navy IRST 16x64 2-D array will actually be fabricated and forty selected chips will be delivered to NRL for testing.

This final report describes the results obtained during Phase I of this program. The gate oxide fabrication is first described in Section 2. The design and fabrication of the test arrays are then given in Section 3. The array testing facilities are described in Section 4. Finally, the results obtained on the test arrays are presented in Section 5.

2. GATE OXIDE FABRICATION

In contrast to the "etch-back" technique in which the gate oxide is formed by selectively thinning from a thick oxide (see Figure 1a), the proposed "non-etch-back" technique consists of a 1500 A thick layer of as-deposited CVD SiO_2 for the gate oxide and a layer of 75 A thick Cr film for the sensing area metallurization (see Figure 1b).

The deterioration of oxide films in the "etch-back" process is best illustrated in Figures 2 and 3. Figure 2 shows two Nomarski micrographs of surface morphology for the as-deposited (see Figure 2a) and the etched oxide films of ~ 1200 A thick (see Figure 2b). The initial thickness of the etched oxide film was ~ 6000 A. Note that the thin ~ 1200 A as-deposited oxide film is featureless whereas the oxide after an extended etch in 3% HF appears to be rough. The roughness of the etched surface can only be guessed but is of the order of a few hundreds of Angstroms.

Figures 3a and 3b show the oxide breakdown voltages for oxide films which have been thinned by 100 and 500 A in 3% HF, respectively. The initial oxide thickness was 1500 A. It is clear that there is a significant degradation in dielectric strength after chemical etch in 3% HF. The degradation of these oxide films becomes worse if a layer of 4500 A thick oxide is removed from an oxide film of 6000 A initial thickness (see Figure 3c). Note that breakdown is observed down to 0V and shows a broad peak at 20V. The oxide breakdown voltage is defined as the voltage necessary to cause a 10 μ A oxide leakage current for Si-MOS capacitor of 1.14×10^{-3} cm^2 area.

1

3. TEST ARRAY STRUCTURE AND FABRICATIONS

Two test array structures were designed and fabricated during Phase I of this program. Figure 4 shows cross-sectional views of the two test structures. In the first test structure the row sensor and the field shield are first patterned over a layer of ~ 1500 A thick oxide. A second layer of oxide film (~ 1000A) is then deposited and the column sensor is finally defined. Note that the column sensor overlaps the row sensor to avoid any possible charge transfer barrier. The conducting films employed in Figure 4a are Cr of ~ 75 A thickness. The transmission of such films is ~ 70% at $\lambda = 4\mu m$ when an anti-reflective coat is used.

The cross-sectional view of the second 2-D test structure is shown in Figure 4b. In this test structure the row sensor, the column sensor, and the field shield are separated by narrow gaps of $\leq$ 5000 A patterned over the same oxide layer of ~ 1500 A thickness. The gap width between the row and column sensors was achieved by a controlled undercut during the row gate patterning as illustrated in Figures 5a-5d employing a standard lift-off technique. Figure 6 shows an optical micrograph of a test pattern exhibiting a gap width of ~ 5000 A, which has been chosen for convenience. Note that the edge definition of the gap looks sharp and the gap width appears to be very uniform. The typical gap width employed in the array processing was ~ 3000A. The advantage of this second test structure over the first is that all the electrodes have the same oxide thickness which simplifies the array operation.

In addition to the two test structures described above, the test mask design included arrays of two different transfer lengths, i.e., the average distance the charge has to move to get from row to column or vice versa. Figure 7 shows the top-views of the two CID cells. Note that unlike the conventional side-by-side design, the row sensor is completely surrounded by the column sensor, reducing the transfer length for a fixed area of sensing site. The transfer length in Figure 7 is ~ 20μm whereas in Figure 7b it is ~ 10μm. It should be noted that the cell geometries shown in Figure 7 are designed at the expense of increasing the periphery-to-area ratio. The increased periphery will slightly increase the edge trapping and hence may reduce the charge transfer efficiency. However, the benefit of the large increase in transfer speed will offset the small, if any, decrease in the transfer efficiency.

4. ARRAY TESTING SETUP

All the measurements described hereafter have been made on individual gates or on gates connected in parallel. Thus, any interaction or cross-talk between adjacent gates that might occur in an actual device with sequential readout schemes will not show up in these tests. The chips are given a preliminary screening for shorts and opens with conductance and C-V measurements. The latter also give an idea of the threshold voltages and any perculiarities in behavior which mostly arise from charges in the oxide or at interfaces.

The principal parameters studied are well capacity, lag, and the transfer characteristics between the row and column gates. The first two parameters have been measured with one of the set-ups shown in Figures 8 and 9. Figure 8 shows, for a linear array, the injection and bias arrangements for reading the injected charge either off the substrate or off the MOS gate. Additional bias

2

supplies and injection pulses are required for 2-D arrays as noted below. Figure 9b schematically illustrates a charge sensitive pre-amp that was built on a small copper plate attached to the sample holder in the dewar vacuum. The 2N4416A input J-FET isolates the unacceptably high input bias current of the HA-2605 operational amplifier from the input. The 2N4416A is mounted directly on the copper plate and is thus cooled with the sample. This reduces its already low input bias current to a completely negligible amount. The HA-2605 is thermally isolated from the copper plate and is "heat" sunk to the warm (outside) wall of the dewar through copper strip fingers since it will not satisfactorily operate at low temperatures.

The absolute value of the charge signal is determined by the product of the output voltage and C_{FT}, the total feed back capacitance. The latter is determined by making a measurement (test pulses at room temperature are sufficient since the temperature dependence of the small mica capacitors that are used is small), and then adding a calibrated capacitor in parallel to C_F and remeasuring the same signal. A comparison of the amplitudes of the two signals will give C_{FT}. Alternatively, a small current, e.g., 1 μ amp, is fed into the input and the time rate change of the output voltage is determined from the digital scope. It was found that the circuitry adds ~ 3 pf to C_F.

Figure 9a shows a capacitor load, voltage sensitive pre-amp circuit. The load capacitor, C_L, must be much greater than the capacitance of the gate(s) measured, otherwise charge sharing occurs between the gate and load capacitances giving an "electronic lag". The 2N4416A source follower serves the same function as in the circuit shown in Figure 9b. Since there is no feedback around this source follower, a constant current source supply is provided so that the gain is very close to unity.

The total load capacitance, C_{LT} is calibrated the same as C_{FT} in the circuit shown in Figure 9b. Because C_{LT} must be large (typically 1000 pf), the signals are small and a pre-amp must be used between the source follower and the Nicolet digital scope. A 10 nsec rise time pre-amp with a nominal gain of 50 was put together utilizing a SN72733 chip for this purpose. Because of the large value of C_{LT}, wiring capacitances are of minimal effect and have no effect on circuit stability. This permits all the electronics to be external to the dewar. This in turn provides greater flexibility in testing a sample, once it is mounted and the dewar evacuated, since all pertinent sample leads are directly brought out.

Both of the arrangements and circuits shown in Figures 8 and 9 have been used. After concluding that these different arrangements did indeed give identical results, the combination shown in Figure 8a and 9a was adopted because of the flexibility noted above and the fact that the dewar did not have to be specially fitted with a pre-amp. Most measurements have been carried out with a dewar having two separate connectors with only the signal lead coming out one connector. This minimizes electronic cross-talk.

In utilizing the arrangement as shown in Figure 8a, the injection pulse must be applied simultaneously and equally to the field plate (or the columns if they are used as field plates in testing the row gates) and the substrate. Since the read out circuit resets the signal gate(s) to ground potential, the substrate-signal gate potential must be applied to the substrate. However,

3

the behavior of the device is determined by any field plate and/or column gate potentials with respect to the substrate. The circuitry shown in Figure 10 provides this arrangement with considerable flexibility for testing linear or 2-D arrays. Channel 1 is usually connected to the substrate. The dc input potential and any injection pulse supplied through input 1 can be added to any additional (positive and negative) biases and/or pulses in channel 2 or channel 3. Channel 2, e. g., is usually connected to the column gates and channel 3 to the field plate.

To measure the charge transfer behavior in 2-D devices, one more electronic box was built. This is a counter and an electronic analog switch which, with the circuitry of Figure 10, permits the turning on or off of a column inject pulse after a pre-set number of row inject pulses, or vice versa.

The injection pulses and overall timing of the signals are generated by four signal generators, specifically, Wavetek models 113 and 164 and/or Ailtech model 511. This provides complete flexibility in the timing, amplitudes, and widths of the pulses required and is especially useful in carrying out the charge transfer tests between row and column gates.

The handling of the chips was found to influence the threshold voltages, especially in structures with thin oxide layers and/or non-overlapping gate/field plate structures. This is presumably related to moisture and/or photo effects charging the surface or inducing charges on interface states or between oxide layers. A vacuum annealing at 100°C for a few hours stabilizes the thresholds as long as the detectors are kept in the dewar vacuum.

5. RESULTS

As noted above, the arrays have a concentric ring structure, i. e., each column gate completely surrounds a row gate. (The terminology of column and row is arbitrary. In this report, however, the above designation will always be used, namely, column gates will be those gates each of which surrounds a row gate.) This permits the column gates to act as a field plate to the row gates since one has a local geometry similar to that of a linear array with a field plate. Figure 11 shows an example of a completed test array with all pertinent pads labeled.

A 2-D array with the second test structure (see Figure 4b) was wire-bonded and tested. This array shows normal C-V curves for both row and column gates. Good charge transfer between row and column gates was also observed when the array was operated in the charge-sharing mode and the sequential row injection mode (see below). This array, however, showed some irreproducibility in the bias conditions from day-to-day even when the array was kept in vacuum. This was thought due to oxide charge-up over the unshielded gap between the row and column gates although very stable unshielded structures have since been made. It was, therefore, concluded at that time to focus on the array development of the first test structure.

5.1 Characterization of Signal (Row) Gates in a Field Plate Geometry

4

In the typical signal gate-field plate configuration, the field plate is biased to threshold. This permits the maximum injection voltage to be applied which is typically at least twice the maximum injection voltage in the case where the field plate is connected to the substrate.

Most of the data has been taken on one device which has 1500 A oxide under the signal (row) gates and 2000-2200 A oxide under the column gates. The actual field plate developed partial shorts to the substrate and in all experiments it was connected directly to the substrate. All the data reported below was with an H pattern geometry, i.e., the signal (row) gate was H-shaped with the column gate completely surrounding and overlapping it in geometrically complementary pattern (See Figure 7b).

Figure 12 gives the C-V characteristics of the row and column gates and the approximate threshold voltages derived from these measurements. These threshold voltages are typical following a two-hour anneal as described above.

Figure 13 shows typical data. The well (depleted volume) under the signal gate is permitted to fill (invert) from dark current by waiting 0.5 to 5 seconds. Usually, the cold infrared filter in the optical window is replaced by a copper plate so that the sample sees only the cold dewar temperature. In Figure 13a, a series of readout sequences is shown starting at the left followed by the 2nd through 6th readouts following the dark current integrating period. Looking at the 6th readout, the reset transient is first seen, then the injection pulse of 0.5 μsec width (not resolved on the recording) followed by the actual signal and ending with the reset clamp. There is no significant difference between the 6th signal and succeeding ones and this 6th signal is taken as the reference signal. The reference signal is sometimes referred to, in total, as the dark current signal but it is made up of at least three parts: (1) The true dark current integrated between injection pulses of about 35 μsec in this case. This dark current appears to be volume generated but with a "volume-perimeter" component. (2) A reversible "breakdown" current that increases very non-linearly with injection voltage. This is the limiting factor on the injection level and hence the well capacity. This breakdown is dependent on the field plate bias and involves the edge field enhancement effects modeled by Tantraporn and Wei[1]. The injection voltage level applied to the sample for the data shown in Figure 13a is just before the "breakdown point" as observed visually on the scope, i. e., there is less than a few milivolts contribution to the reference signal over the normal dark current. If the injection voltage is much too high, the signal clearly deviates from the straight line characteristic of a constant dark current (see Figure 13 b). Under such conditions, the breakdown current, presumably band-to-band tunneling current, quickly flows into the deeply depleted well until the electric fields are reduced below the breakdown levels. (3) Lag or the failure to inject all the charge in the previous injection pulse. Under typical conditions, this component is negligible for the 6th readout (since the well is nearly "empty") but is clearly seen in the 2nd readout following the large signal in the 1st readout. Cross talk, or the recapture of injected charge by

---

1. W. Tantraporn and C.-Y. Wei, "Computer Simulation of the Electric Field in Indium-Antimonide Semiconductor under an MOS's Gate and Field Plate", General Electric Corporate Research and Development, Report No. 81CRD256, October 1 81.

an adjacent gate is minimal in these measurements because all the gates are read (injected) simultaneously.

Quantitatively, the signal on the 6th readout is taken as a reference or the zero signal and the amplitudes of the preceeding signals are measured with respect to it. Lag is defined as the ratio of the 2nd to the 1st signals and the well capacity is calculated from the magnitude of the 1st signal. The actual total charge collected in the well is closer to the sum of all the signals since this tends to correct for any lag effects. However, the performance of a device is related to the magnitude of the 1st signal since that would be interpreted as the image signal.

As noted above, the data in Figure 13a is for the maximum injection voltage before non-linear "breakdown" effects are obvious with the column potential set as negative as possible. The maximum injection voltage without breakdown is quite dependent on the column (field plate) potential whereas the results are insensitive to the row potential between -8 and down to at least -16 volts. The lag is seen to be 6.4% and the well capacity calculates out to be

$$\frac{0.349 \text{ volts}}{G} \times \frac{C_L}{q} = 4.81 \times 10^7 \text{carriers}$$

where C_L = 1080 pf, G = 49 (preamp gain), and q is the electron charge. The measurements were carried out on a row of 8 gates that were tied together on the chip. Since each gate had an area of 6.76mils^2,

$$\text{well capacity} = 8.9 \times 10^5 \text{ carriers mils}^{-2}.$$

With the dark current integration time reduced to 2 msec, the well is only half filled. Under these conditions, the lag was measured to be 9.0%. Reducing the injection voltage to 0.82 volts (i.e., one-half) reduces the signal to 137 mv and the lag was measured to be 9.3%. The increase in the lag noted under these latter conditions is easily seen when running through a series of measurements although the absolute accuracy of repeating lag measurements is no better than ± 1% from day to day.

If the column potential is made more negative, it was found that the injection voltage, and hence well capacity, could be significantly increased. Figure 14 shows data on the same sample shown in Figure 13 illustrating the increased well capacity without breakdown. The wells are permitted to fill with a 5sec integration period and an equal and simultaneous injection voltage is applied to the column and row gates but only the row gates are read. Note that with the thicker oxide under the column gates, the actual change in the surface potential under the column gates is less than that under the row gates. Table I summarizes these results.

5.2 Charge Transfer Characteristics

6

Many readout schemes for 2-D arrays require transferring the signal charge and all or part of any background charge from row to column gates or vice versa. The efficiency and speed of transfer are important points in considering certain schemes. Several of these schemes have been considered and basic tests have been carrried out on the transfer modes involved. The relative merits of these various schemes in potential 2-D systems are not considered here since the object is to demonstrate the dynamic responses of the basic modes in a simple 2-element (one row, one column) hook-up. Figure 15 illustrates a comparison of the potential wells during the elemental read cycle for four common readout schemes, i. e., the normal charge sharing mode (CSM), the sequential row injection mode, the ideal mode readout, and the quasi ideal mode. Note that for the sequential row inject, all rows are read simultaneously (there is no row select) which requires a pre-amp for each row. It is also noted that for the first two modes it is only important that there be a significant common background charge under a row/column pair. Figure 15 illustrates only this common charge and does not imply the necessity or even usual occurrence of an equal surface potential.

a) Normal Charge Sharing Mode

In the normal charge sharing mode (CSM), both the column and row gates are in deep inversion and tightly coupled together. The biases on the row and column gates are not critical since it is not necessary to empty either well. The charge is shared between the row and column and the output corresponds to 1/2 the injected charge or signal.

This mode is demonstrated in Figure 16. In the two sequences shown, "injection/transfer" pulses are applied only to the row gates for the first 6 readouts whereas beginning with the 7th, injection pulses are applied to both the row and column gates. In the lower sequence, a long (0.5 sec) integration time occurs before the 1st readout and the wells are completely filled. Thus, charge is injected in the first readout (pulse on the row gates only). Following this injection, the signal wells are half filled, as illustrated in Fig. 15, and immediate repeated injection on the row gates only transfers charge to the column gates and is not injected.

Figure 16a is a case where the wells are only partially filled by limiting the integration time to 0.5 msec. Here, no charge is injected in the first readout, but charge is transferred to the partially empty column and then returned, hence, no signal is seen. The presence of the transferred charge is indicated on the 7th readout where, as in Figure 16b, an injection pulse is applied to both the row and column gates, charge injection takes place, and a signal is seen. The integration time was set to give the maximum signal without injecting on the first readout, hence the signal applitude on the 7th readout is similar for the two tracings. An important point is that the signal is "sharp", i.e., in this tightly coupled, highly inverted case, the charge moves quickly as well as efficiently.

b) Sequential Row Inject Modes

The sequential row inject mode differs from the charge sharing mode in that the wells are permitted to fill completely with signal and only the first inject (i.e., select row or select column) voltage pulse is applied. This

mode is illustrated in the first read out in Figure 16b. With only the one injection, however, the injection voltage can be doubled without emptying the well to breakdown. This has been observed.

c) Ideal Mode

Ideal modes are where a limited bias voltage is applied to both the row and column gates and all the well charge is transferred between them. This is similar to a normal CCD operation and while this makes the simplest configuration conceptually, the bias and injection voltages are critical. Figure 17 illustrates the device behavior in an approximate ideal mode which is useful for observing charge transfer behavior. The slow response indicates a "slow-moving" charge in getting the column well emptied into the row well following the row injection pulse. The charge, however, is not lost as evidenced by an unchanged signal following 1 or 10 such initial pulse readouts. Following the injection pulses on both row and column gates (5th readout in this case), the opposite is seen, namely, a slow decay of minority carriers under the row gates. It is believed that charge transfer indeed occurs in the ideal mode but the charge appears to move slowly and less efficiently. In addition, the requirement of critical biasing conditions for both row and column will likely make this mode of operation impractical.

d) Quasi Ideal Mode

When the row bias is increased beyond the injection voltage, bias charge will always be present under the row gate sensors (see Figure 15d). Signal charge is then integrated under the row sensor until it starts to spill over under the column sensor. The signal charge is first read out from the row and again transferred to column. In the quasi-ideal mode no charge is shared between row and column during readout or reference and hence all the signal charge is read out. However, charge is shared between row and column during row select which gives high charge transfer efficiency. These features plus the fact that the row bias is no longer critical, makes this a very attractive mode of operation.

6. Summary

In summary, the feasibility of fabricating InSb CID 2-D array with improved charge transfer characteristics has been successfully demonstrated on test arrays fabricated by the proposed "non-etch-back" technique. Good charge transfer has been obtained for devices operated in the normal charge sharing mode, the sequential row injection mode, and the quasi-ideal mode. Charge transfer was also observed in the ideal mode but the charge appeared to move slowly and less efficiently. These encouraging results on these test arrays have given us confidence in designing a Navy IRST 16x64 2-D array for time-delay-and-integration application. This array is presently being fabricated and tested.
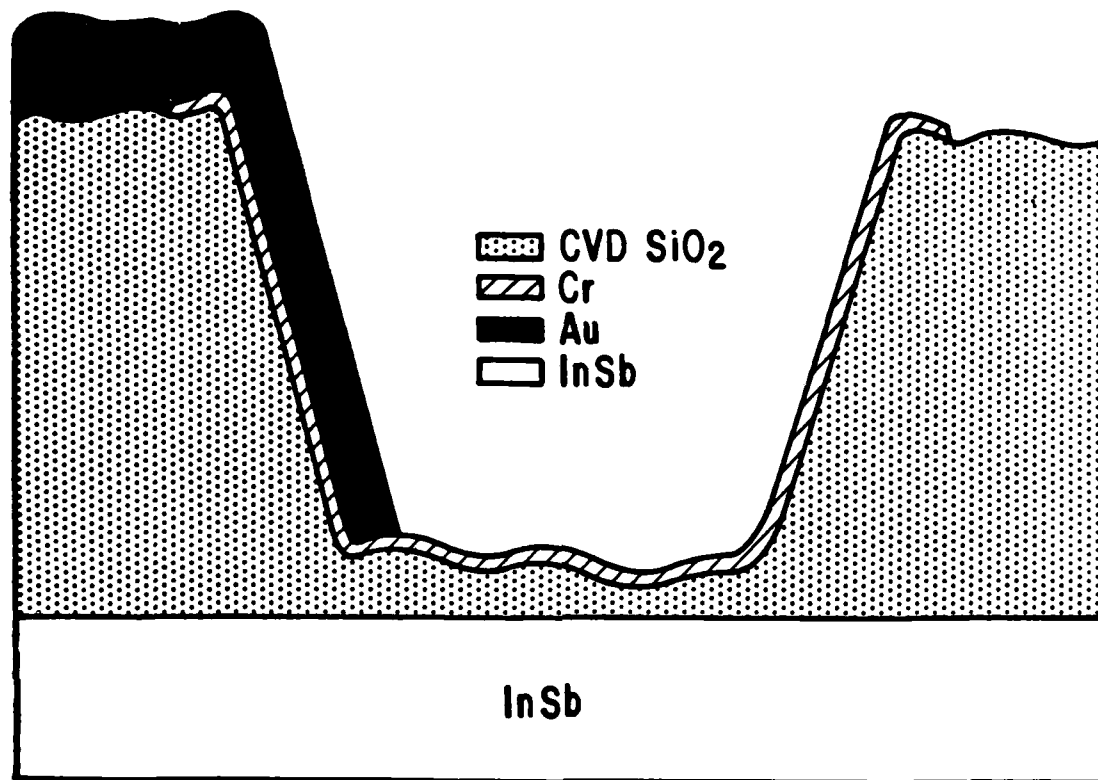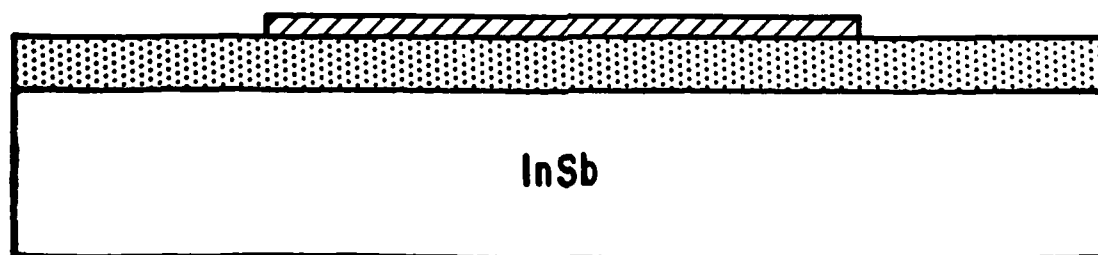
TABLE I

Summary of Lag and Well Capacity Measurements. Gate Bias = −12.0 V.
Field Bias (Column Gates) = −5.3 V. In the Last Entry the Column
Gate Bias = −7.0 V.

INJECTION VOLTAGE VOLTS	INJECTION PULSE WIDTH (sec)	LAG (%)	WELL CAPACITY $(10^{6}/mil^{2})$
1.67	0.50	6.4	0.89
1.67	0.50	9.3	(half filled)
0.82	0.50	8.4	0.35
1.67	1.0	3.9	0.93
3.56	0.50	7.5	2.17

Figure 1. Etch-back (a) vrs non-etch-back (b) fabrication. See text.

10
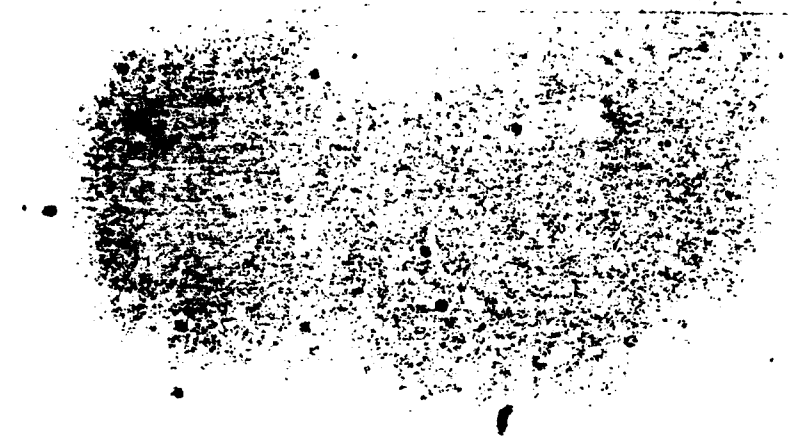
(a)

(b)

Figure 2.   Nomarski micrographs of an as-deposited CVD SiO_2 film about 1200 Å thick (a) and of a film originally about 6000 Å and then etched to about 1200 Å (b).

11
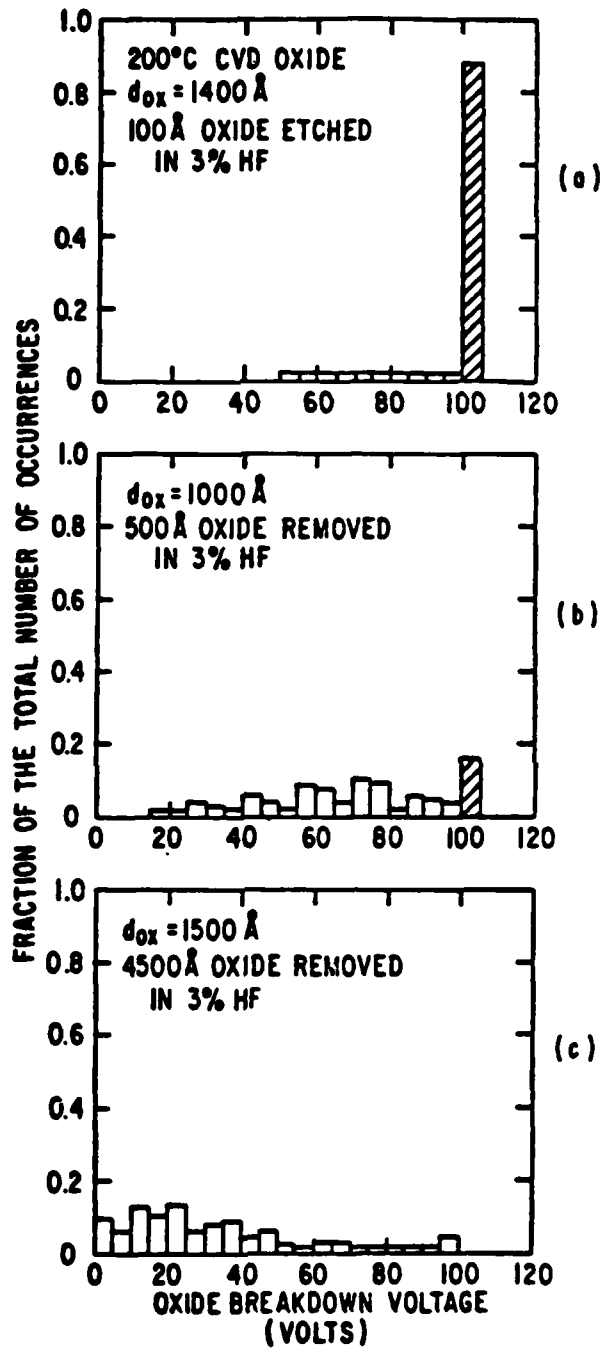
Figure 3. Distribution of breakdown voltages of MOS capacitors for three etching condition. See text.

12
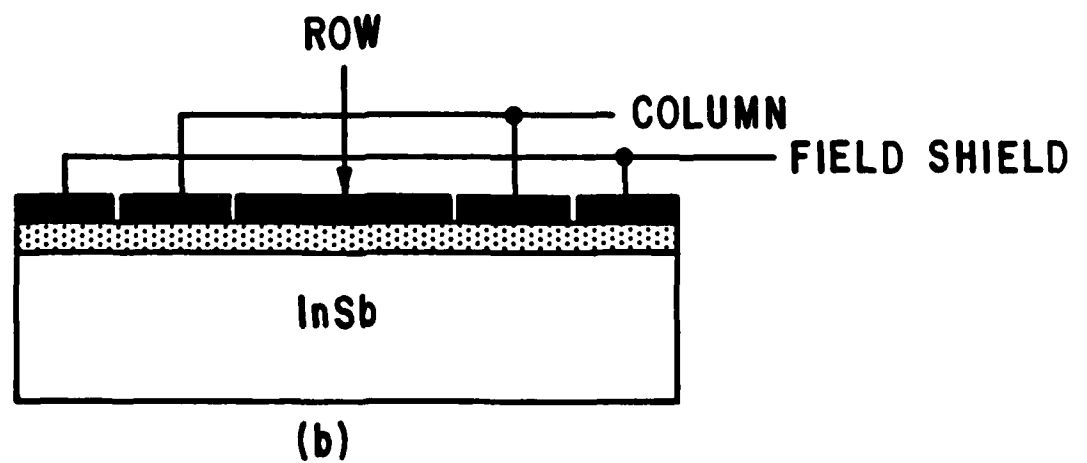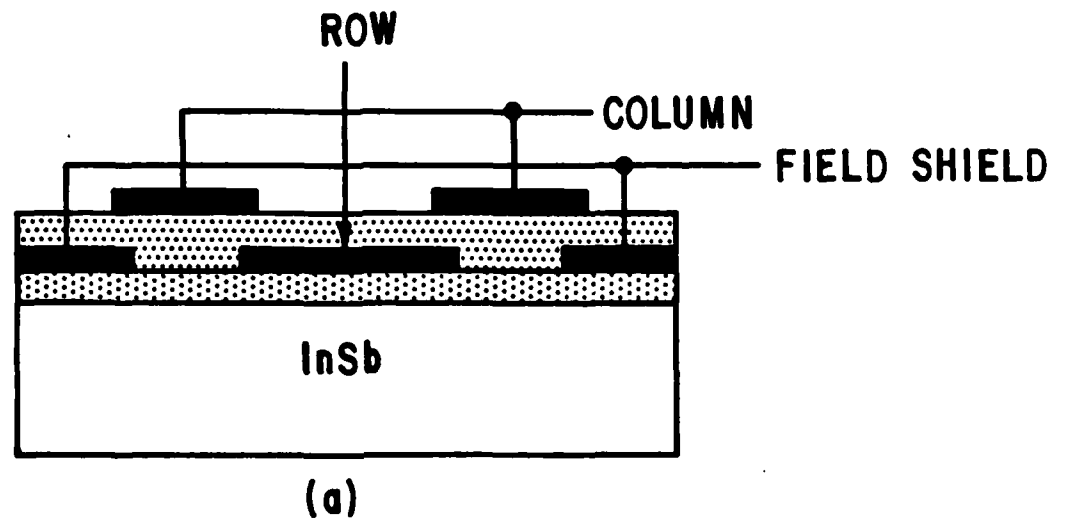
Figure 4. Cross sectional schematics of the two test structures fabricated. See text for details.
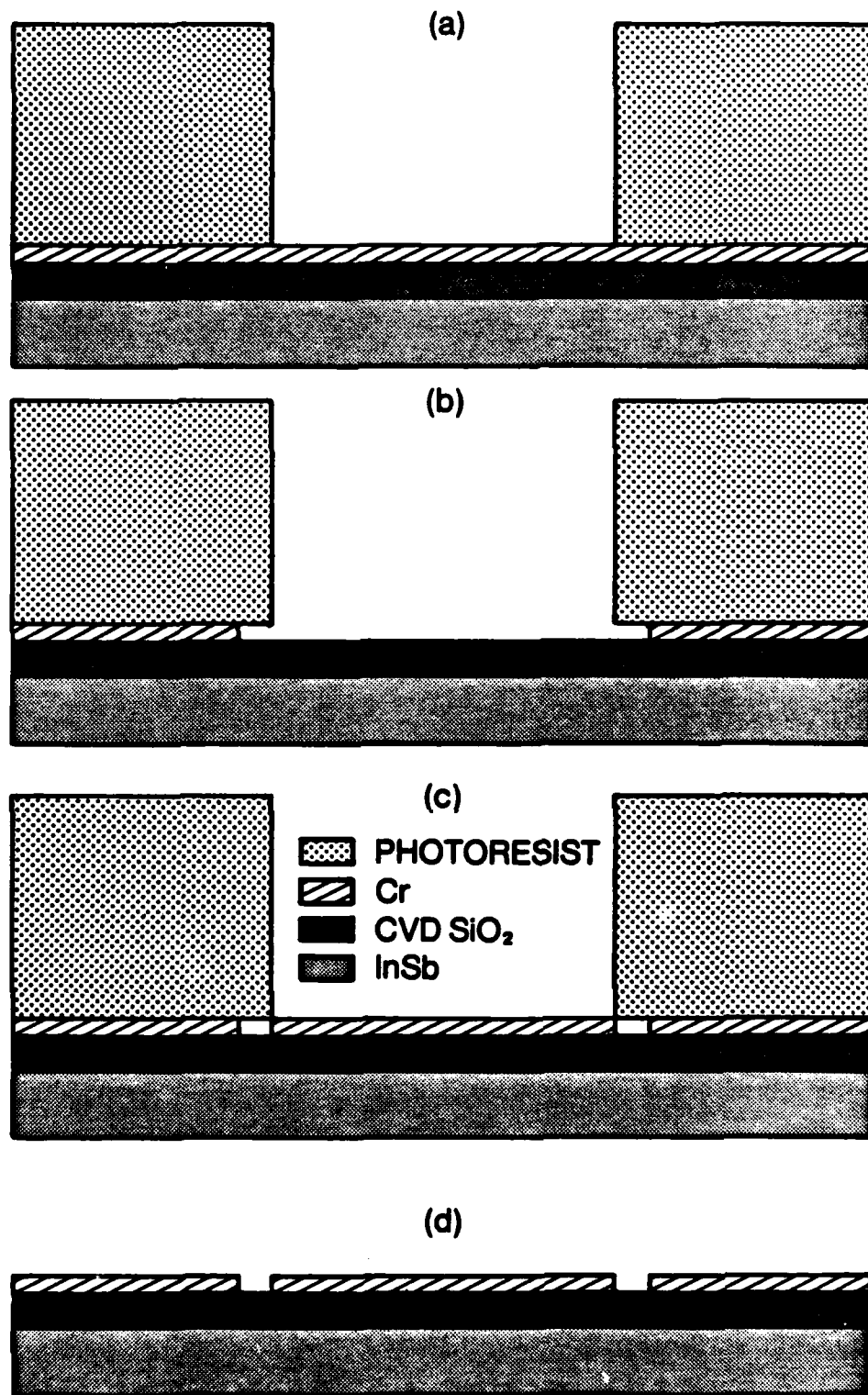
Figure 5. Schematic of the sequence used to achieve the gaps in the co-planar structure shown in Fig. 4 (b).

14

5000 Å
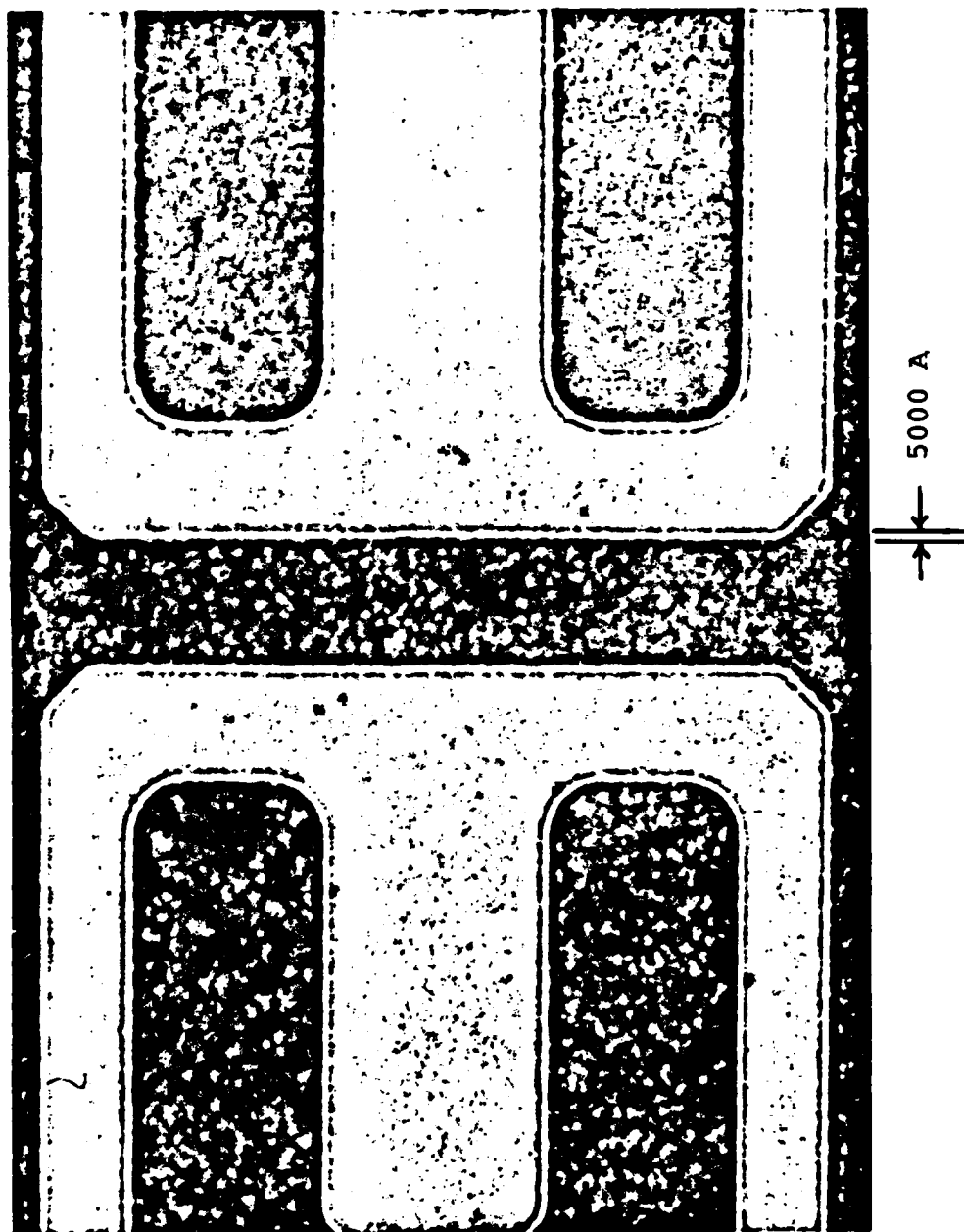
Figure 6. Optical micrograph illustrating the uniform gap width achieved by the process illustrated in Fig. 5.

15
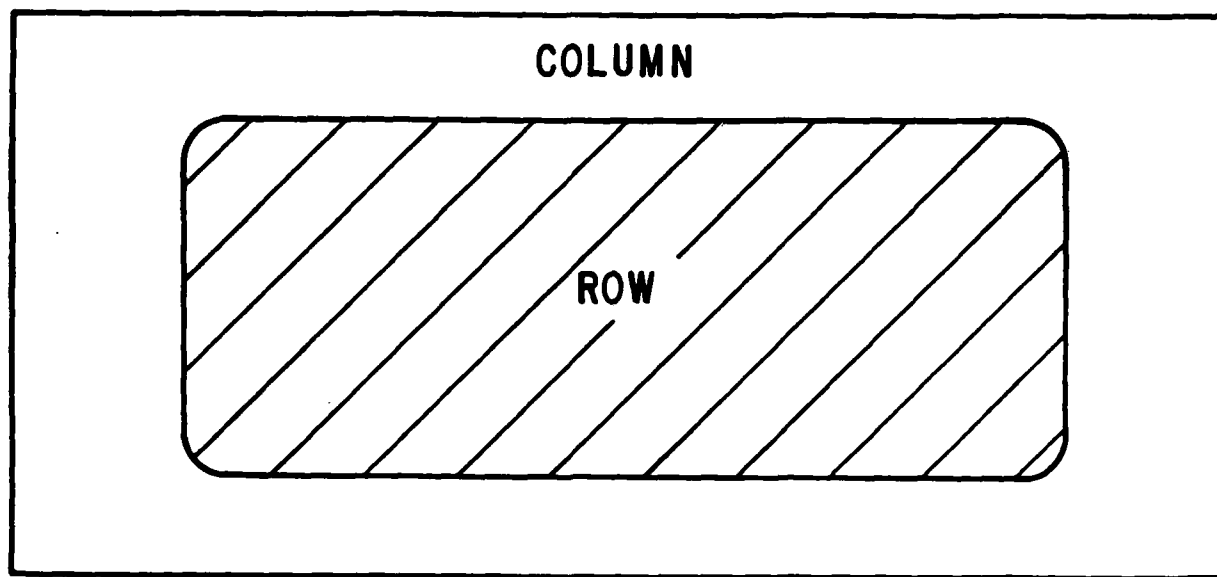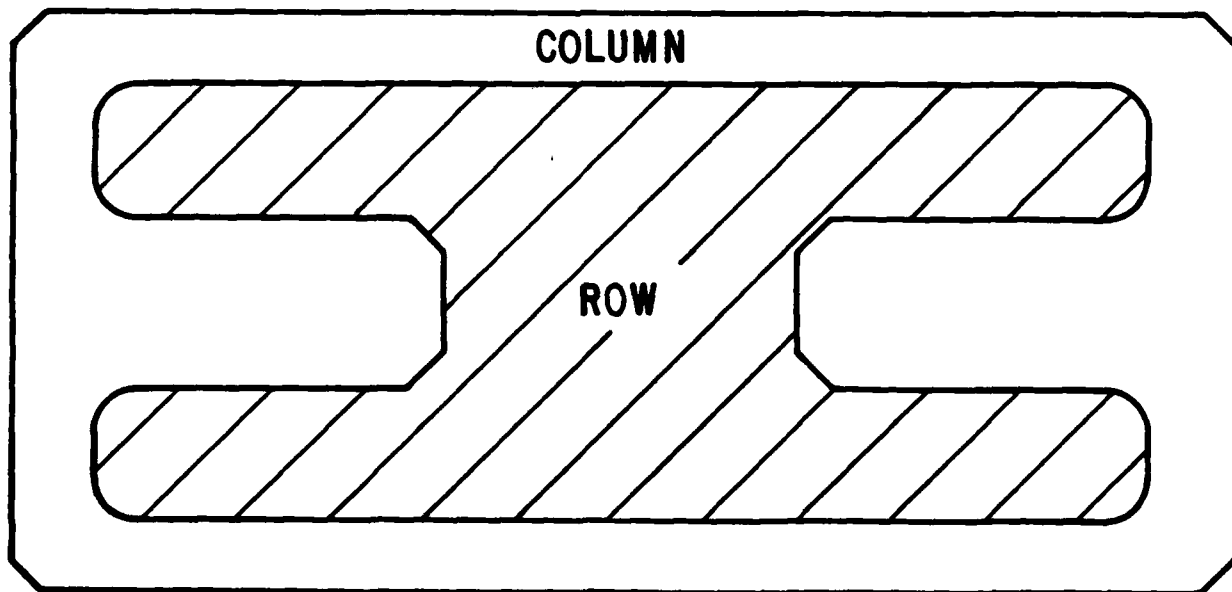
Figure 7. Two test patterns giving different transfer lengths between the row and column gates or sensors. Note that in both cases, the row sensor is completely surrounded by the column sensor.
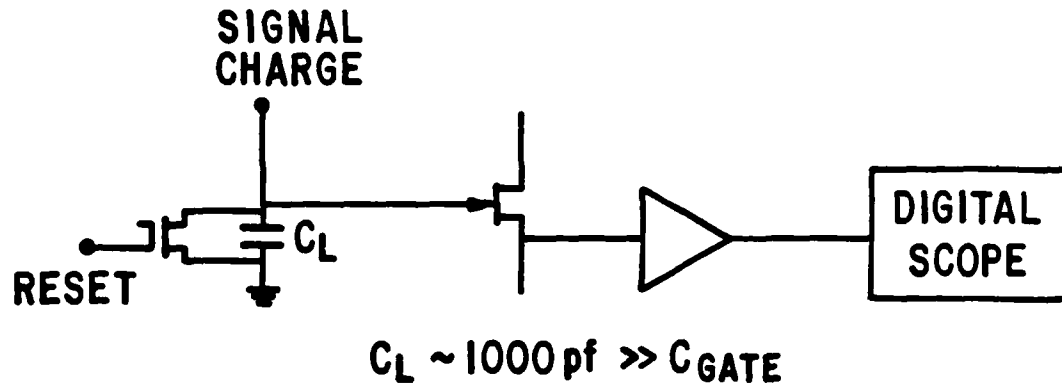
16

SIGNAL OFF GATE (a)

FIELD
BIAS

PRE-AMP

GATE
BIAS
INJECT

SIGNAL OFF SUBSTRATE (b)

GATE
BIAS
INJECT

FIELD
BIAS
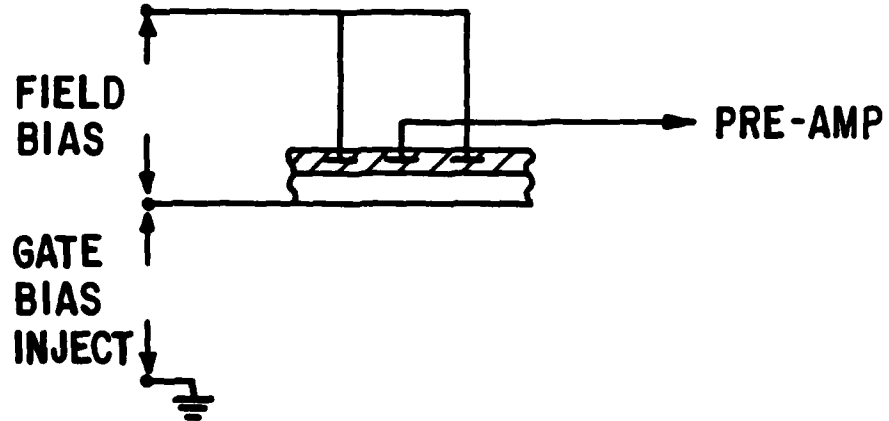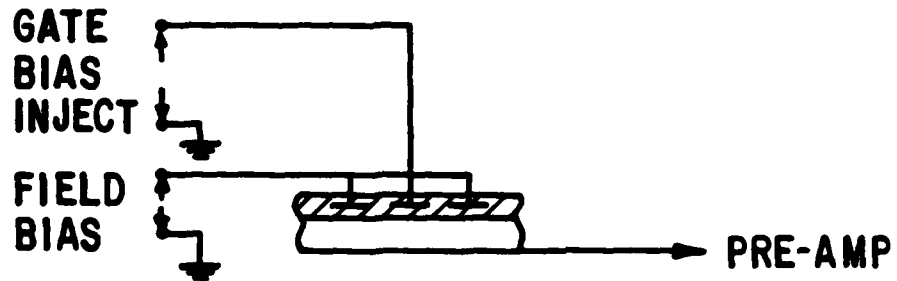
PRE-AMP

Figure 8. Bias and voltage injection connections for reading signal off either substrate or gate pixel.
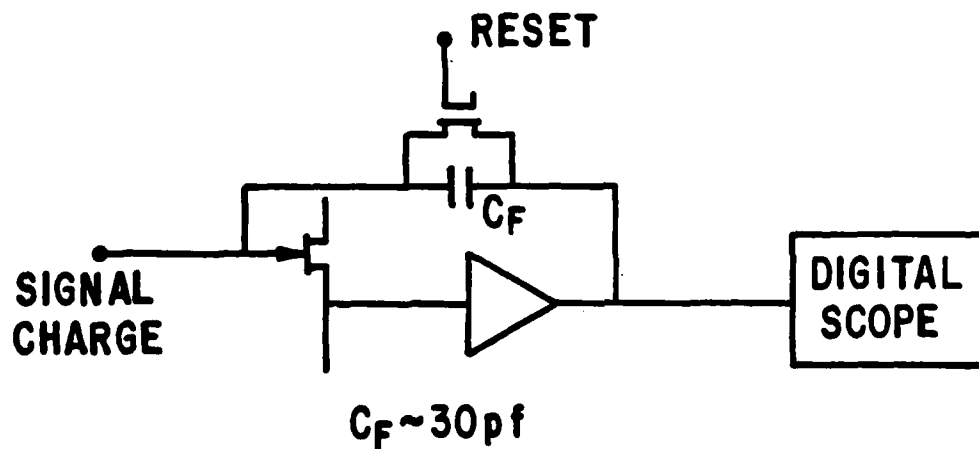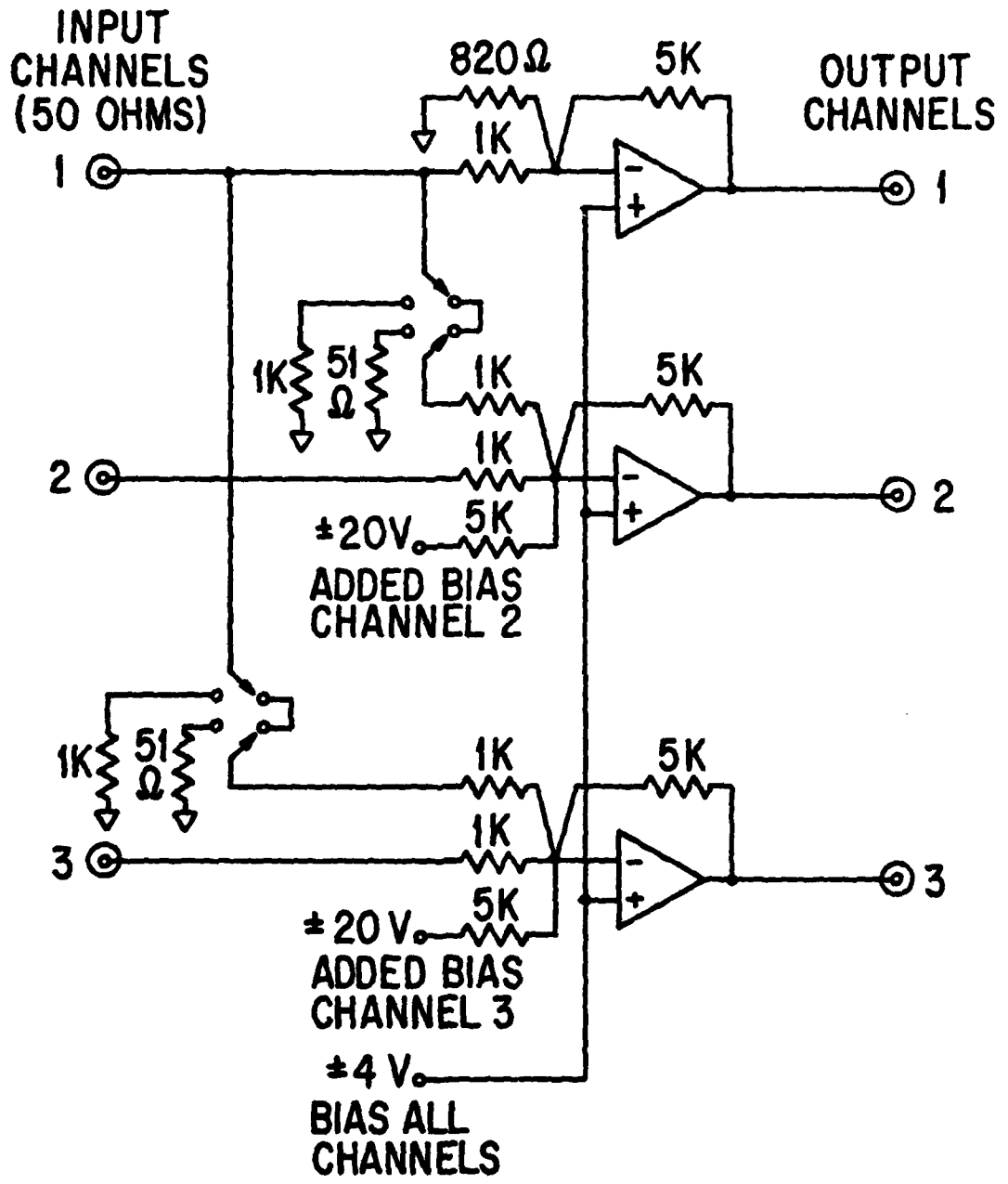
CAPACITOR LOAD / VOLTAGE AMPLIFIER (a)

$C_L \sim 1000\,pf \gg C_{GATE}$

CHARGE SENSITIVE AMPLIFIER (b)

$C_F \sim 30\,pf$

Figure 9. Charge sensitive pre-amp and alternative capacitor load, voltage pre-amp circuitry used to measure the signals off the CID chips.

18

INPUT
CHANNELS
(50 OHMS)

OUTPUT
CHANNELS

820 Ω   5K

1K

1   −   1

1K   51
Ω

1K   5K

1K   −   2

±20V   5K

ADDED BIAS
CHANNEL 2

1K   51
Ω

1K   5K

1K   −   3

± 20 V   5K

ADDED BIAS
CHANNEL 3

± 4 V

BIAS ALL
CHANNELS

ALL RESISTORS ARE 1%
ALL OP-AMPS ARE HA-2525
   OPERATED FROM ±20V SUPPLY

Figure 10.   Bias supplies and inject/transfer voltage drive circuitry for CID
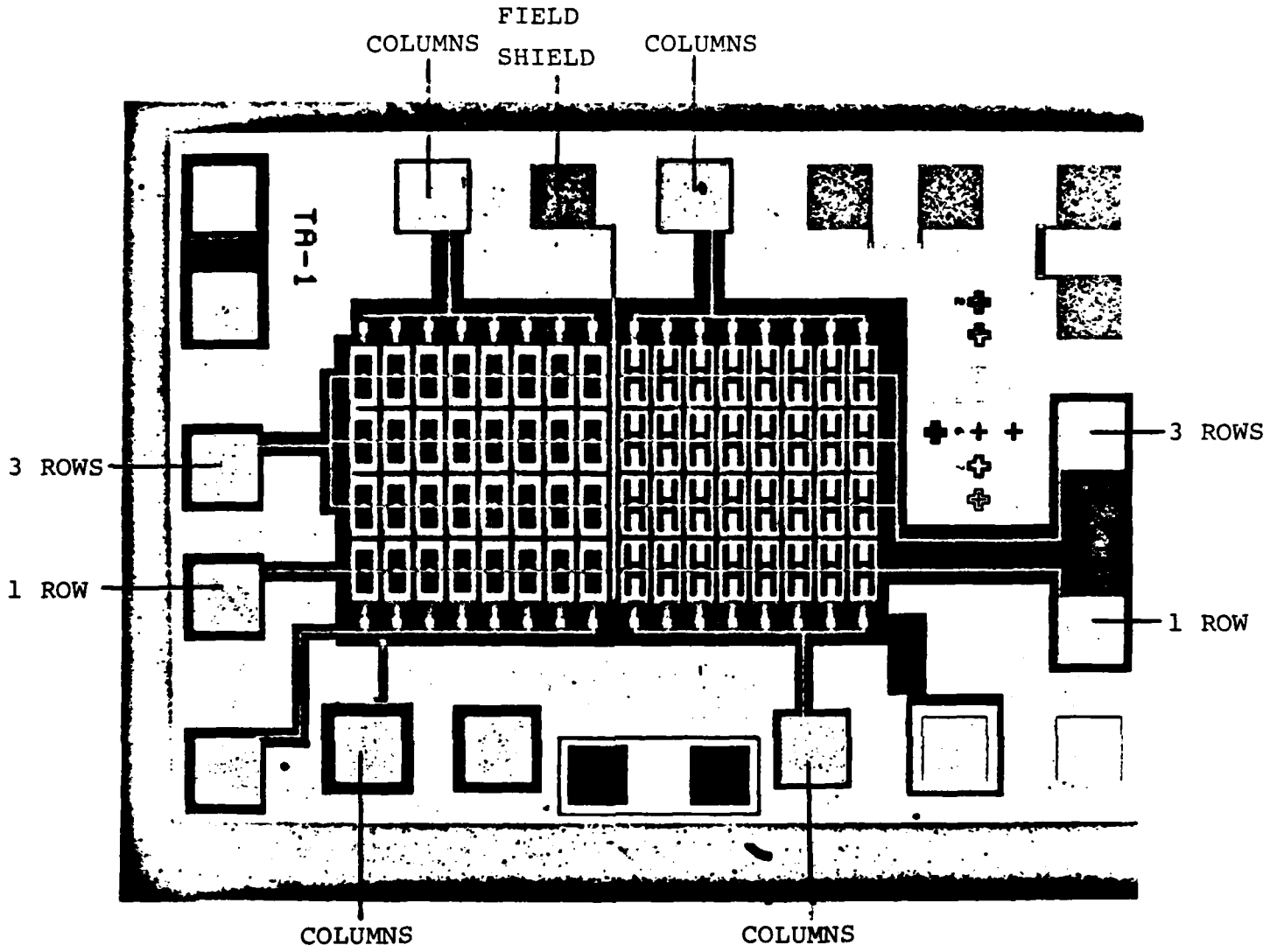   devices.

19

Figure 11. Pattern of the actual test array. The right half uses the H pat-
tern shown in Fig. 7 (b) while the left half uses the rectangular
pattern shown in Fig. 7 (a). Only the field shield is common to
both. The unmarked pads are various capacitance or conductivity
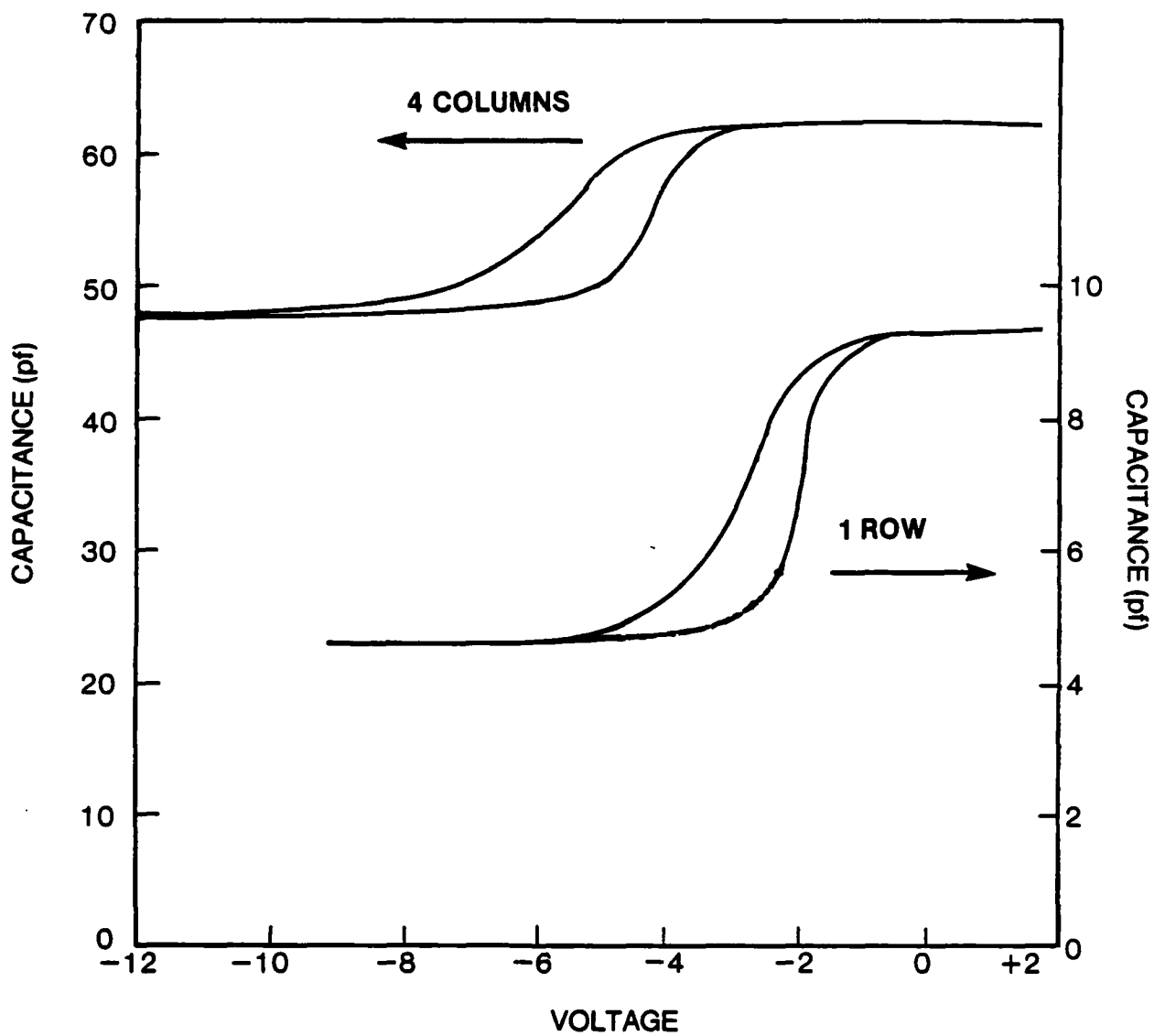probes for checking the different processing steps.

Figure 12. C-V characteristics of the row and column gates for the principal
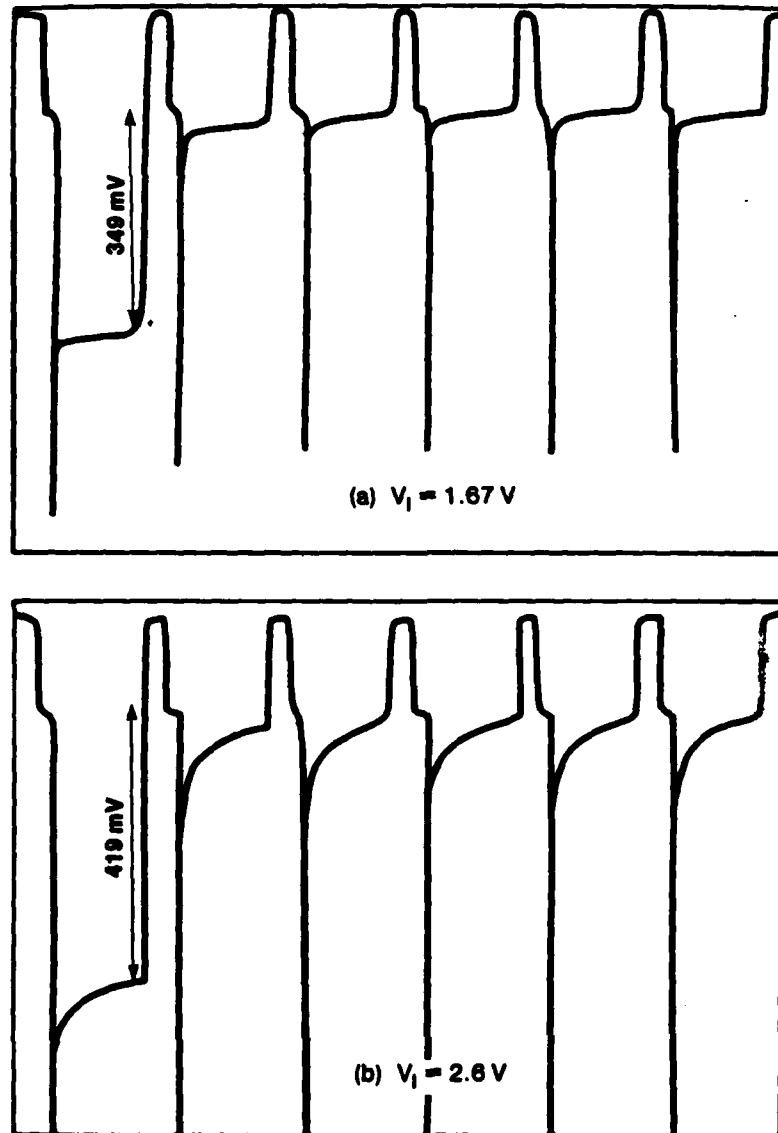device under test. Temperature is 77°K.

Figure 13. Typical results for a signal gate/field plate geometry (linear array configuration). From data such as this, the lag and well capacity can be calculated. The row bias is -12.0 V. The column bias (acting as a field shield) is -5.3 V. The injection width is 0.5 μsec. The sample is at 77K and the row well is permitted to fill for 5 sec with dark current before the first injection pulse illustrated. Typical maximum injection voltage, V_I, is shown in

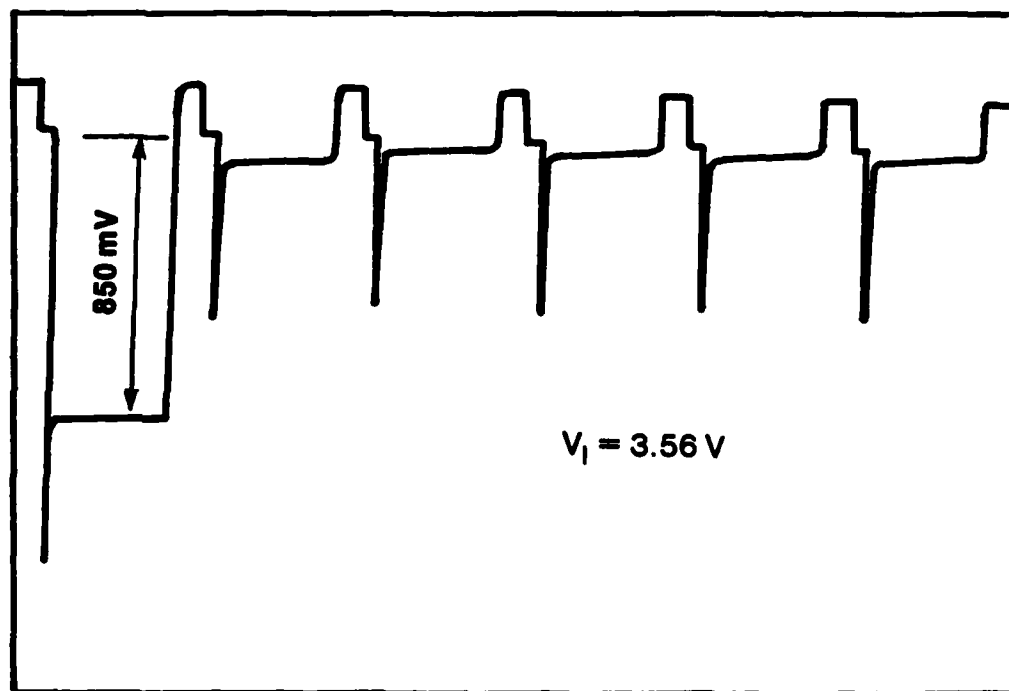(a) while (b) illustrates signal when overdriven.

22

Figure 14. As Fig. 13 but column bias increased to -7.0 V. Note lack of breakdown with high injection voltage. Compare with Fig. 13b.
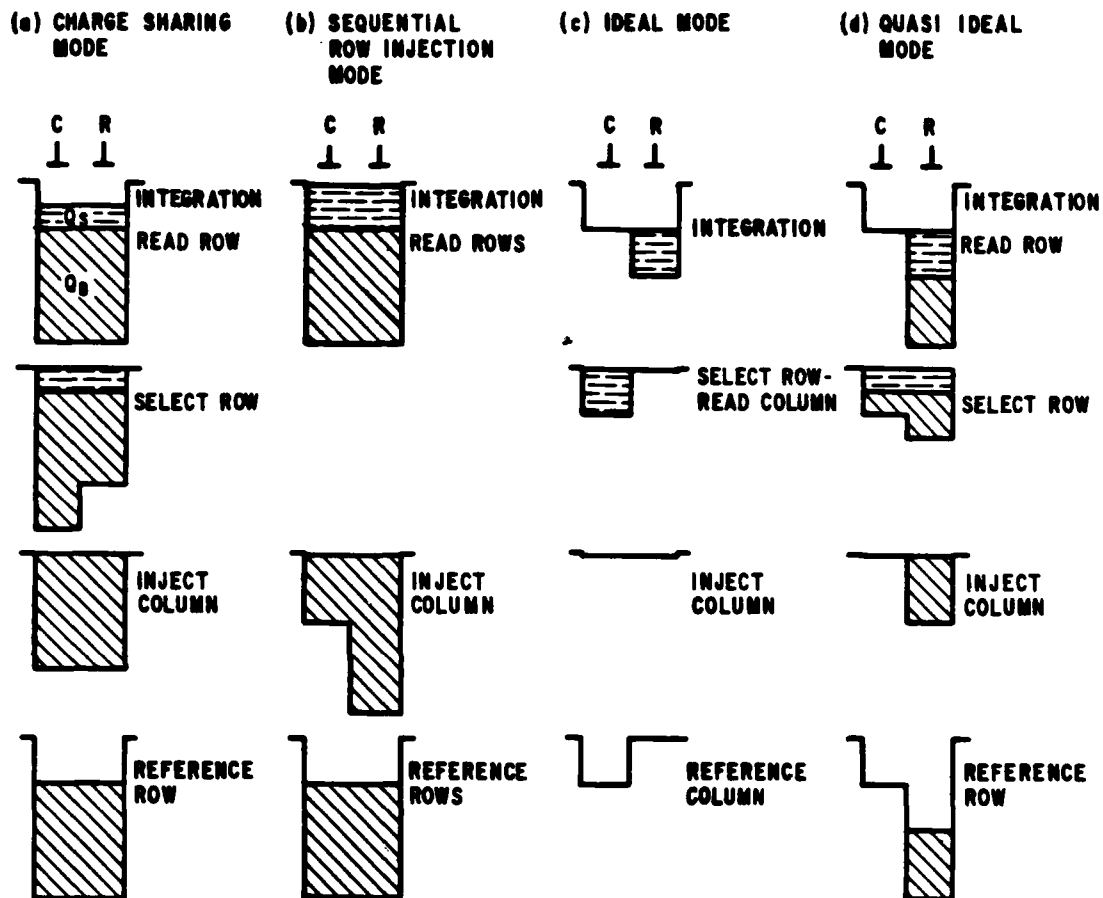
23

Figure 15. Schematic of the potential wells and charge distributions for four possible 2-D readout schemes. See text for a description of each. The dashes represent the maximum possible injected charge and hence the maximum signal charge or well capacities. The slant lines represent excess inversion charge. R and C represent row and column gates, respectively. For simplicity, the column gates and wells are drawn adjacent to the rows whereas in the device under test, each row gate has a concentric column structure surround it. The READ and REFERENCE functions, of course, are interchangeable since it is the injected charge or the difference in the gate charge before and after injection that is measured. Threshold voltage is represented by the ''tops'' of the wells.
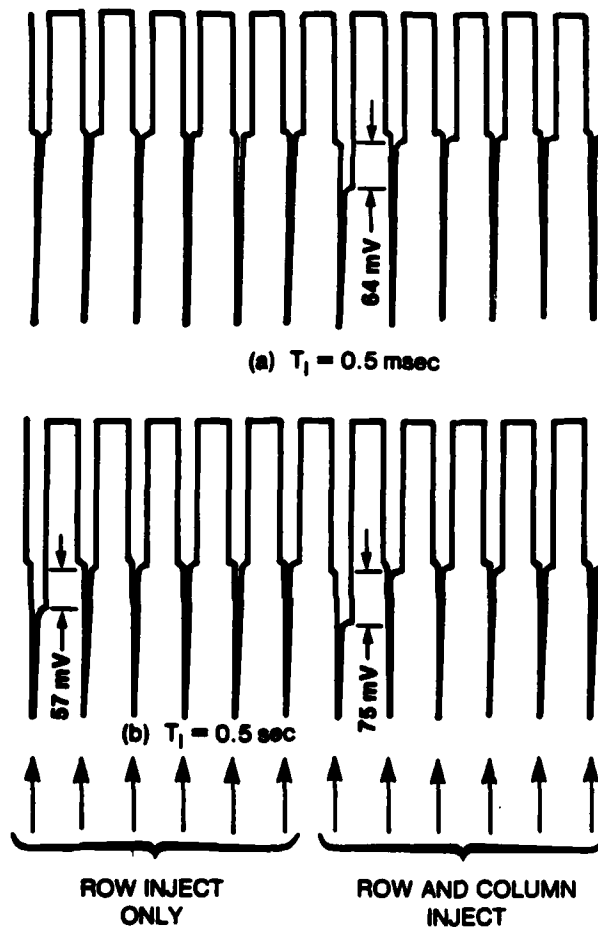
Figure 16. Demonstration of the Charge Sharing Mode. The sample is at 77K. Row bias = -12.0 V; row inject = 0.65 V. Column bias = -15.0 V; column inject = 0.85 V width of injection pulses is 1.0 μsec. See text for a description of the pulse sequences.
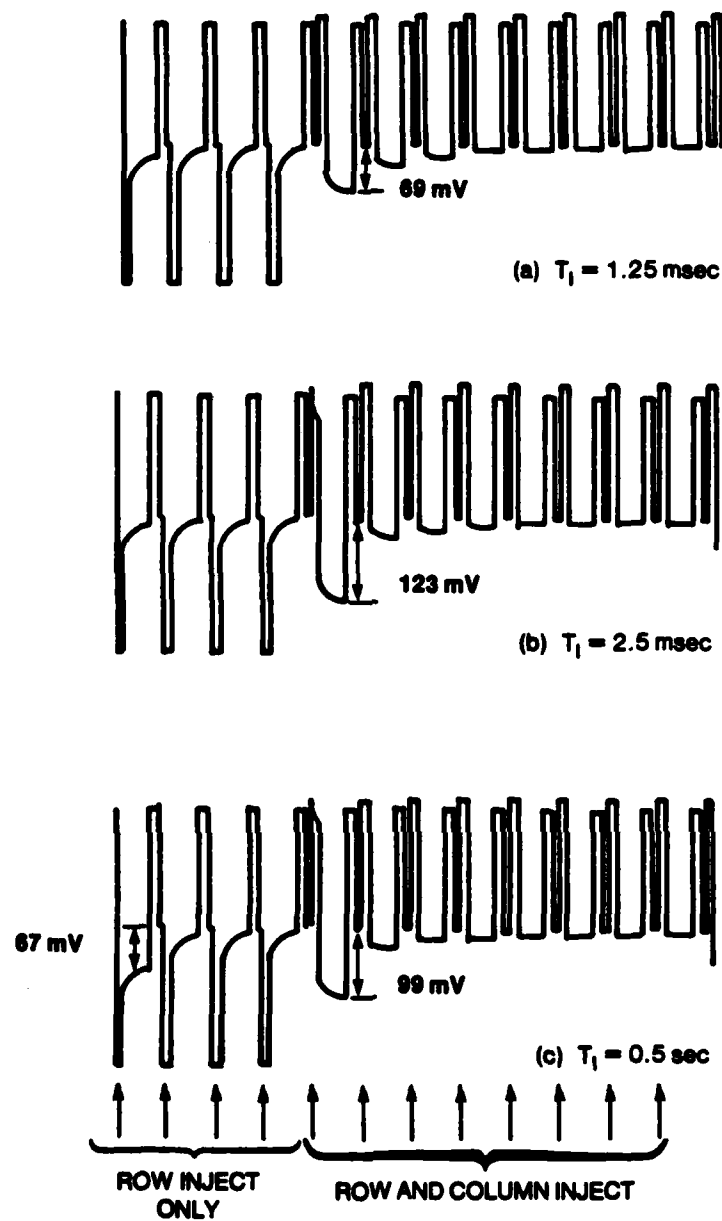
Figure 17. Ideal Mode behavior under different dark current integration times
at 77K. Row bias = 6.73 V: row inject = 0.54 V. Column bias =
-9.24 V; column inject = 1.77 V. Width of injection pulses is
5.4 μsec. The first four sequences are with a row inject voltage
only. For the fifth sequence and on, the inject voltages are
applied simultaneously to both row and column gates. For T_I =

1.25 msec, the row well is 1/2 filled (as measured to the bottom
of the column well). For T_I = 0.5 sec, both wells are filled and
the excess charge (for ideal mode operation) is injected in the
first (row) injection pulse.

26

END

FILMED

6-83

DTIC