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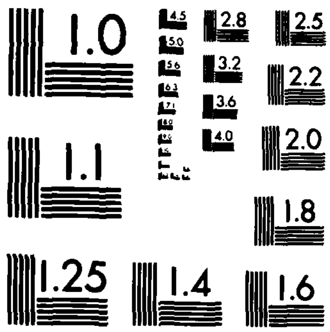

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FABRICATE INDIUM-ANTIMONIDE TWO-DIMENSIONAL CHARGE INJECTION DEVICE ARRAY

Final Report

Contract N00173-80-C-0572

Prepared for

Naval Research Laboratory
Washington, D.C. 20375

by

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The objective of this program was to fabricate 16x64 two-dimensional InSb CID arrays using the process sequence developed by GE CR&D under contract N00173-80-C-0281. This process sequence does not involve a thick-thin cut back of the pixel gate oxide and therefore produces an essentially planar structure.

InSb CID focal plane arrays with 16x64 elements have been fabricated and various 2-D CID modes demonstrated on test structures incorporated on the chips. Low threshold voltages, low density of states in the interfaces and in the gate oxides

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ABSTRACT

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InSb CID focal plane arrays with 16 x 64 elements have been fabricated and various 2-D CID modes demonstrated on test structures incorporated on the chips. Low threshold voltages, low density of states in the interfaces and in the gate oxides, and dual-gate coupling between row and column gates of less than one volt have led to the demonstration of practical ideal mode behavior.

I. INTRODUCTION

The objective of the program described in this report is to fabricate 16 x 64 InSb charge injection device (CID) arrays using the "non-etch-back", or planar, fabrication technique developed in a prior program, Contract N00173-80-C-0281. In this technique the thickness of the oxide layers employed in the CID fabrication are those "as-deposited" by chemical vapor deposition (CVD). Degradation of the oxide quality and of the thickness uniformity due to oxide etching is thus avoided and CID arrays of improved charge transfer, low lag, reduced cross talk, and improved uniformity in responsivity and storage well capacity have been demonstrated. A high yield is expected because of the planar processing.

Section II describes the design and fabrication of the 16 x 64 InSb CID arrays. The testing facilities and results obtained from test devices on these arrays are given in Sections III and IV. The program results are summarized in Section V.

II. ARRAY DESIGN AND FABRICATION

The design concepts of the present 16 x 64 2-D array are similar to those described in the final contract report of the above Contract N00173-80-C-0281. Figure 1 shows the cross-sectional and top views of the unit CID cell geometry that was developed. Note that unlike the conventional side-by-side design, the row gate is completely surrounded by the column gate reducing the transfer length for a fixed area of sensing site. The transfer length for the design shown in Fig. 1 is 10 μm. It should be noted that this cell geometry incurs the expense of an increased periphery-to-area ratio. The increased periphery will slightly increase the edge trapping and hence may reduce the charge transfer efficiency. However, the benefit of the large increase in transfer speed offsets the small, if any decrease in the transfer efficiency.

As shown in Fig. 1, the row gate and the field plate are first patterned over a layer of oxide. A second layer of oxide is then deposited and the column gate is defined. Note that the column gate overlaps the row gate to avoid any possible charge transfer barrier. The column gate and field plate are overlapped in a 32 element test column (as well as in the main portion of the array) and non-overlapped in a 16 element test column. (See Fig. 4 and Section IV.) The inside dimensions of the field plate given in Fig. 1 are the actual outside column gate dimensions for the non-overlap case. For the non-overlap case, the field plate is dimensioned so that there is a 5 μm gap (projected) between it and the column gates. The corners of the row gates are rounded, as noted, to minimize the electric fields in their vicinity. The charge storage area of an individual row gate is 2.52×10^{-5} cm^2 while that of the column gate is 1.73×10^{-5} cm^2.

The conducting films employed are Cr of ~ 75 A thickness. The transmission of such films is ~70% at $\lambda = 4$ µm when an anti-reflective coating is used.

III. ARRAY TESTING SETUP

With the exception of cross talk measurements between adjacent columns in the actual 16 x 64 array, all the measurements described hereafter have been made on test columns where all the row and column gates are separately interconnected in parallel on the chip. (The singular "gate" will refer to these parallel connected gates unless specifically noted.) Thus, any interaction or cross-talk between adjacent gates that might occur in an actual device with sequential readout schemes will not influence the results of these tests.

The chips are given a preliminary screening for shorts and opens with conductance and capacitance-voltage (C-V) measurements. The latter also give an idea of the threshold voltages and any peculiarities in C-V behavior which mostly arise from charges in the oxide or at interfaces.

The principal parameters studied with the set-up shown in Fig. 2 are well capacity, lag, crosstalk, and the transfer characteristics between the row and column gates. As noted in Fig. 2b, a capacitor load, voltage sensitive preamplifier is used to measure the signal charge. The load capacitor, C_L, must be much greater than the capacitance of the gate being measured, otherwise charge sharing occurs between the gate and load capacitance giving an "electronic lag". The source follower is a 2N4416A with 5 volts on the drain.

This isolates the unacceptable loading of the following circuitry. Since there is no feedback around this source follower, a constant current source supply is provided so that the gain is very close to unity.

The total load capacitance, C_L^T, is calibrated by measuring a given signal with and without a calibrated capacitance added in parallel to C_L. From the ratio ot the output signals, C_L^T can be calculated. Because C_L^T must be large (typically 1000 pf), the signals are small and additional amplification must be used between the source follower and the Nicolet digital scope. A two stage pre-amp using HA-5195 operational amplifiers was built for this purpose. This gives nominal gains of 15 from the first stage and 150 from the second with a d.c. to 10 MHz response.

Because of the large value of C_L^T, wiring capacitance is of minimal effect and has no effect on circuit stability. This permits all the electronics to be external to the dewar. This in turn provides flexibility in testing an array, once it is mounted and the dewar evacuated, since all pertinent leads are brought out directly.

With the arrangement shown in Fig. 2, the signal (row) injection pulse must be applied simultaneously and equally to the field plate, the column gate, and the substrate. Since the read out circuit resets the signal gate to ground potential, its bias potential must be applied to the substrate. However, the behavior of the device is also determined by the column gate and field plate potentials with respect to the substrate. The circuitry shown in Fig. 3 conveniently provides for this. Channel 1 is usually connected to the substrate. The d.c. bias potential and any injection pulse supplied to channel 1 can be added to any additional (positive or negative) potentials and/or pulses in channel 2 or channel 3 which can be, e.g., connected to the column gate and the field plate, respectively.

To measure the charge transfer characteristics, one more electronic box was built. This is a counter which, with the circuitry of Fig. 3, permits the turning on or off of a column inject pulse after a pre-set number of row inject pulses, or vice versa.

The inject pulses and overall timing of the signals are generated by four signal generators, specifically, Wavetek models 113 and 164 and/or Ailtech model 511. This provides complete flexibility in the timing, amplitudes, and widths of the pulses required and is especially useful in carrying out the charge transfer tests in the cross talk measurements.

The handling of some CID chips was found to influence the threshold voltages, especially in structures with thin oxide layers and/or non-overlapping gate/field plate structures. This is presumably related to moisture and/or photo effects charging the surface or inducing charges on interface states or between oxide layers. The chips processed in this program were quite stable, showing only a slow uniform shift toward zero volts (less than one volt measured over several months) in the threshold voltage. Nevertheless, an anneal for a few hours was often carried out prior to measurements to "standardize" the immediate prior history of the chip.

IV. RESULTS

Figure 4 shows a photo-micrograph of a completed 2-D array. As noted above, the arrays have a concentric ring structure, i.e., each column gate completely surrounds a row gate. (The terminology of column and row is arbitrary. In this report, however, the above designation will always be used, namely, column gates will be those gates each of which surrounds a row gate.) This permits the column gates to act as a field plate to the row gates since one has a local geometry similar to that of a linear array with a field plate. The inverse is also true since the row gate and field plate connected together act like a field plate to the column gate. Thus, the individual characteristics of either the row or column gates can be determined which is useful to check design parameters and processing integrity.

IV.1. Individual Gate Characteristics

Figure 5 gives the C-V characteristics of the 32 element test device. Both the row and column gates have flatband voltages near zero volts, small hysteresis, as well as a sharp accumulation-to-inversion transition indicative of a low density of traps in the oxide and also a low density of interface states. The sharp transition is also indicative of a high degree of uniformity among the 32 elements connected in parallel. Low densities of interface states and oxide traps are crucial for the "ideal mode" of operation although less critical for the "charge sharing" modes of operation as discussed below.

There is approximately 4 pf of wiring and row-column overlap capacitance in these measurements. Thus, the capacitances of individual column and row gates, per cell, are 0.24 pf and 0.66 pf, respectively, giving a ratio or cell split of 2.7:1. This is somewhat less than the designed value of 3:1 but is well within the uncertainties of the oxide thicknesses.

IV.2. Dark Current

Dark current was measured as a function of column injection voltage with both the row and column gates biased into heavy inversion, i.e., the row and column wells are tightly coupled in the charge sharing type situation (see Fig. 8). Figure 6 compares the dark current results obtained from the two test columns. During the measurements, the cold infrared filter in the dewar is replaced by a copper plate so that the sample sees only the cold dewar temperature (0° field of view). As seen in Fig. 6, the dark current increases sharply as the injection voltage is increased beyond a certain value which is defined as the maximum injection voltage or breakdown voltage. For the overlap structure, this is seen to be about 4.2 V whereas for the non-overlap structure it is about 5.2 V.

Because of the common well under the row and column gates giving an equipotential surface, the equivalent injection voltage for the row gate is C(col)/[C(col) + C(row)] times the column injection voltage. With this factor, the normalized dark current is 11 $\mu A/(V\ cm^2)$. This is comparable to what is observed in InSb linear arrays with similar processing and gate oxide thickness. (See Final Report of Contract N00014-81-C-2578.) The pixel size in these linear arrays, however, is about 4 times larger than the row-column cell size in the present array. This is suggestive that no excess dark current exists in the present 2-D array of smaller geometry as would be expected if the dark current is generated primarily in the depletion region underneath the gates.

IV.3. Charge Transfer Characteristics

The operation of 2-D CID arrays requires transferring the signal charge and all or part of any backgrou:d charge from row to column gates or vice versa. The efficiency and speed of charge transfer are important points in considering certain 2-D array readout schemes. We will first discuss the C-V data which demonstrates charge coupling and then some read-out schemes and related charge transfer data.

Charge coupling between row and column gates is demonstrated in Fig. 7. When only the row electrode is biased (i.e., V_{col} = 0 V), the C-V curve of the row electrode shows a shape typical of standard high frequency (1 MHz) C-V data. This is a repeat of the lower curve of Fig. 5 without the retrace. When the column gate is biased into inversion (i.e., V_{col} = -6V), the C-V curve of the row gate shows a response typical of low frequency C-V data for an individual gate but, in fact, is a direct measure of the added column capacitance as the row and column gates are coupled. This is equivalent to the closing of the switch of the equivalent circuit shown in the upper left of Fig. 7. The transition from the first curve to the strongly inverted value of the second curve in this figure is a measure of the charge coupling. Theoretically, the transition should start at the moment the row gate is weakly inverted and be completed when it is strongly inverted; this is less than 0.5 V for InSb. The transition shown in Fig. 7 is indeed less than 0.5 V indicative of "tight" charge coupling. This is to be compared to typical values of ~2 V for most devices processed by the "etch-back" technique.

Several read-out schemes have been considered and basic tests have been carried out on the transfer modes involved. The relative merits of these various schemes in potential 2-D systems are not considered here since the object is to demonstrate the dynamic response of the basic modes in a simple 2-element (one row, one column) hook-up. Figure 8 illustrates a comparison of the potential wells during the elemental read cycle for four common read-out schemes, i.e., the normal charge sharing mode (CSM), the sequential row injection (SRI) mode, the ideal mode, and the quasi-ideal mode (QIM). Note that for the sequential row inject, all rows are read simultaneously (there is not a row select) which requires a pre-amp for each row. It is also noted that for the first two modes it is only important that there be a significant common background charge under a row/column gate pair and that the well depths need not be "equal".

In the normal charge sharing mode (CSM), both the column and row gates are in deep inversion and tightly coupled together. The biases on the row and column gates are not critical since it is not necessary to empty either well. The charge is shared between the row and column gates and the output is correspondingly reduced giving rise to a charge sharing efficiency factor. Including the usual depletion loading capacitance, the net read out efficiency factor (η) is given by

$$\eta = C_{ox}(row) \;/\; [C_{ox}(row) + C_{ox}(col) + C_{dep}]$$

where C_{dep} is the common depletion capacitance under both the row and column gates and is, of course, dependent on the injection voltage and InSb doping level. Taking

$$C_{dep} = [C_{ox}(row) + C_{ox}(col)]/5$$

as a typical value and using the cell split ratio as given above, then

$$\eta = 0.61.$$

The SRI mode differs from the CSM in that the injection voltage is applied to the row gate only (column gate in our tests—see caption of Fig. 8). Figure 9 shows the results when the device is operated in this mode. In the presence of the large bias charge resulting from the bias potentials indicated, the transferred charge moves quickly as well as efficiently as discussed in the previous study as described in the final report of Contract N00173-80-C-0281. The total well capacity per row-column cell is given by

$$\text{well capacity} = (\text{1st} + \text{2nd} + \ldots\ \text{readout})/\eta$$

$$= (3.7 + .26) \times 10^6 /(0.61)$$

$$= 6.5 \times 10^6 \text{ carriers/cell.}$$

The lag is 7% as calculated by the ratio of the second read out to the first

These test devices can also be operated with a high bias charge only underneath the row gate (quasi-ideal mode, QIM) or in the complete absence of bias charge underneath both the row and column gates (ideal mode). The QIM was originally conceived to minimize any charge transfer problems which may occur in the ideal mode. This mode presents no real advantage over the ideal mode if such problems do not exist. Since satisfactory ideal mode behavior has been seen, no results of the QIM will be given here.

Figure 10 shows the signal read out when the device is operated in the ideal mode. (For proper ideal mode operation, the signal should be read off the column gates during row injection instead of the read-inject scheme used here. This eliminates "photo-current" effects. However, demonstration of charge transfer is well illustrated in Fig. 10.) The row well is permitted to nearly fill with dark current for 0.5 msec to the point illustrated in the upper right of the figure. The first six read out signals are with only a row injection which would correspond to a "row half-select". The 1 μsec "injection pulses" are actually transfer pulses moving the charge to the column gate. The time between injection pulses is 33 μsec. The fast recovery of the signal following the row half-select pulse is indicative of a fast transfer of charge. The "signal" that is seen in the first read out (about 6 mV) represents a charge that does not return to the row and would be referenced as a "zero" charge. This is a one time only charge trapping that occurs following the signal read out. Signal read out occurs when the column is "injected" simultaneously with the row injection. This begins with the seventh read out in Fig. 10. The signal charge is now actually injected since the column well is collapsed and there is no other place for the charge to go. A lag signal (13%) is seen on the second column injection or eighth read out.

For this "ideal" mode, the maximum signal is determined by the well capacity of a column gate which, as noted above, is small as a result of the cell split design. The maximum signal is seen with a dark integration time of about 0.8 msec and corresponds to a signal of 82 mV. With the preamp gain of 16 and the load capacitance of 1100 pf, this corresponds to a well capacity (the direct read out signal) of 1.1×10^6 carriers/cell. The "zero" charge that is retained by the column gate is about 8% of this. An optimized array design would have an equal row-column cell split and an improved column gate/field plate structure to increase the breakdown voltage. With such a design, a well capacity of about 5×10^6 carriers/cell should be achievable.

In going from the ideal mode or QIM described above to a charge sharing mode (both row and column gates biased into deep inversion), the response to a constant infrared signal should decrease by about 0.73 in accordance with the ratio $[C_{ox}(row)/[C_{ox}(row) + C_{ox}(col)]$. This is demonstrated in Fig. 11 where only the column bias is changed between the two curves. The ratio of the infrared response between the SRI mode and the ideal mode is about 0.71 in good agreement with the expected value. This presents direct evidence that this array can indeed operate in the ideal mode. Also, in going from the ideal mode to a charge sharing mode, the charge trapping that is seen in the former disappears as the presence of the bias charge keeps the traps filled.

IV.4. Cross Talk Measurements

The cross talk between adjacent 64 cell columns in the main array is measured as follows: All 16 row lines are tied together and shorted to the substrate. The field plate is also tied to the substrate. Three adjacent column lines are brought out with the center column of the three being read out as the signal gate. Bias is applied to all three columns, the associated wells are permitted to fill with dark current, an inject pulse is applied first only to empty the well of center column, and the resulting signal charge is read as the well charge of the center column. An injection pulse is then applied to the two adjacent columns. Some of the injected charge from the adjacent columns is captured by the center column and can be read out. The cross talk is determined as the ratio of the captured charge to the well charge. The setup and read out is identical to the cross talk measurements described in the previously mentioned report on the linear array work.

The results of the above measurements give a cross talk of 33% for the two adjacent columns to the column being measured or 16-17% cross talk per column. This high value is not surprising considering that there is only about 12 μm distance between adjacent column elements. A wider gap at the expense of the fill factor or some kind of recombination streets between column gates will be required to reduce this cross talk.

V. SUMMARY

We have successfully fabricated 16 x 64 two-dimensional InSb CID arrays using a processing sequence developed at the General Electric Corporate Research and Development which does not involve a thick-thin cut back or etch-back processing.

A number of lots have been processed with some variations in the row-column area split as well as some process variations. The most successful lots have been with a design with a cell split of 2.7:1 for use in the so called SRI mode of operation. (This success is because of the processing variations and not because of the particular cell split.)

Tests have been carried out on two "test columns" fabricated on the array chips comprising of 16 and 32 row-column cells, respectively, connected in parallel. Low dark current values of 11 $\mu AV^{-1}cm^{-2}$ have been observed indicating a successful processing technique. Efficient and rapid charge transfer between the row and column gates has been observed with no obvious barriers or charge loss indicating successful structure design. In fact, ideal mode operation (no excess bias charge) has been seen with a one-time charge trapping of 8% of the well capacity of 1.1×10^6 carriers.

For the SRI mode, a well capacity of 6.5×10^6 carriers with no trapping is observed. The lag is 7%. Further work on the design of the column gate/field plate structure should increase the breakdown voltage at this point and hence increase the well capacity. This would be similar to the improvements made in linear arrays in our laboratory.

Three wafers with approximately 30 chips per wafer of the SRI mode configuration have been sent to the E-Lab, General Electric Co., Syracuse, N.Y. for further testing.

ACKNOWLEDGEMENTS

L.J. Keifer, H.M. Lees, and R.S. Lewandowski assisted in the fabrication and testing of these devices.

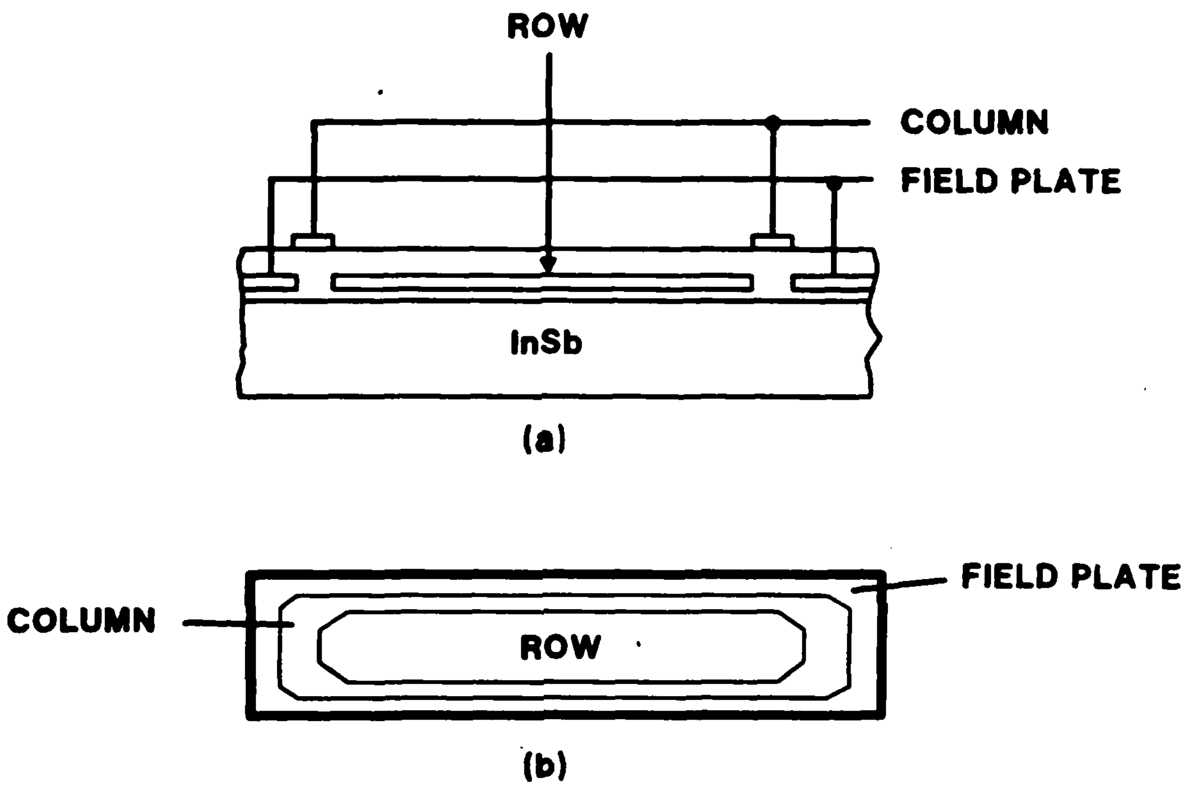
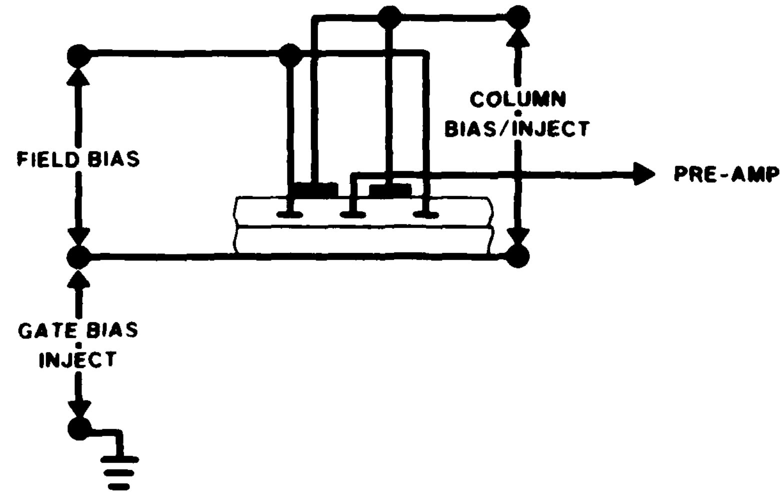


Figure 1 Cross-sectional and top views of an "overlapped" 2-D cell. The overall dimensions of the row gate are 18μm x 142μm while the inside dimensions of the field plate are 28μm x 152μm. The latter defines the effective outside dimensions of the column gate. See text for description of non-overlapped design.

SIGNAL OFF ROW GATE (a)



CAPACITOR LOAD/VOLTAGE AMPLIFIER (b)

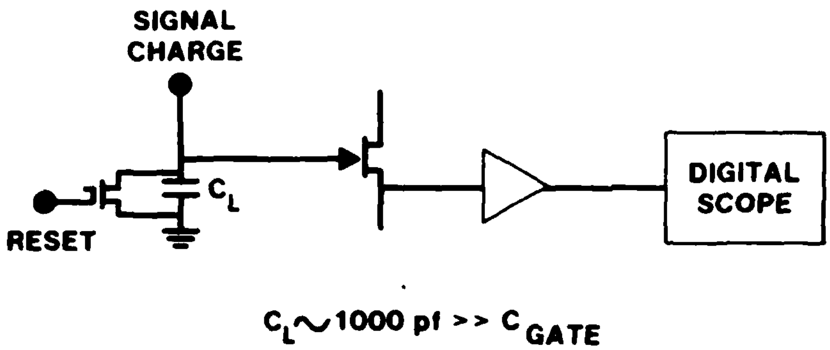


Figure 2 Typical test setup for measuring the characteristics of an individual CID row-column cell. (a) Bias and injection voltage connections for reading signal off one of the gates (usually the row or center gate as indicated). (b) Capacitor load, voltage pre-amp circuitry used to measure the signal charge from the CID arrays.

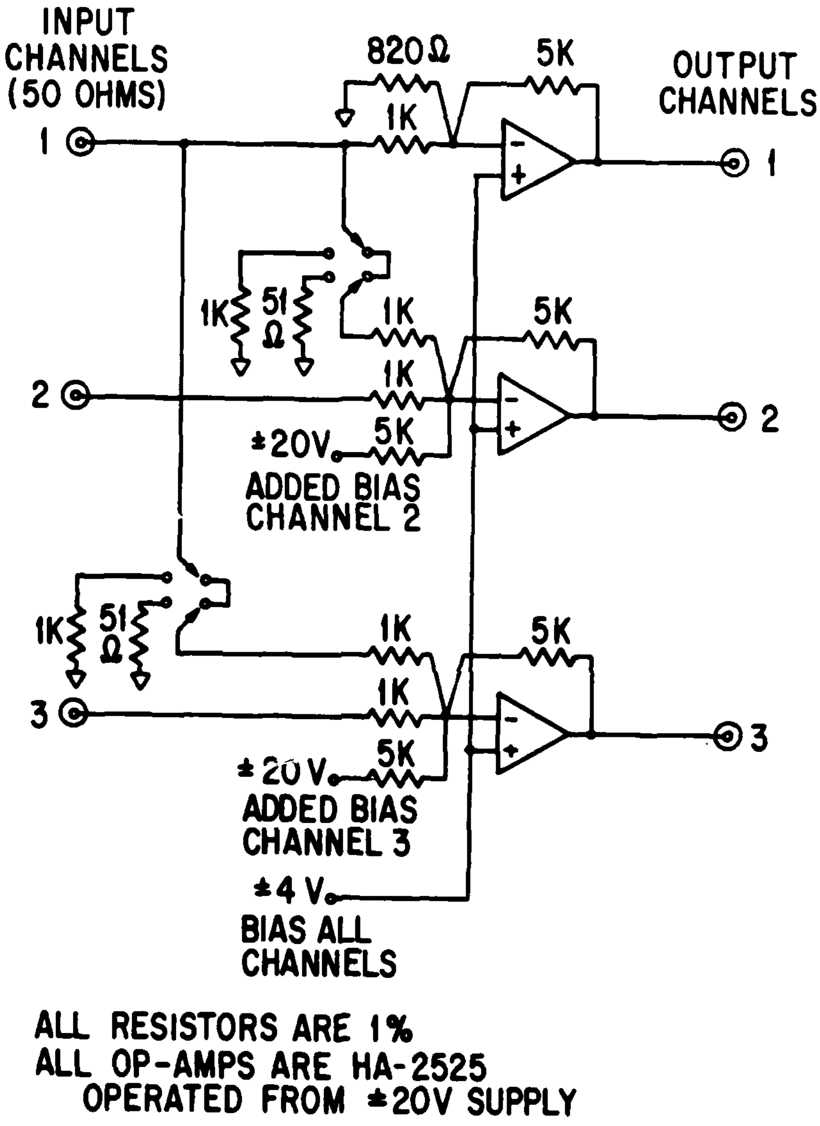


Figure 3 Bias supply and injection voltage drive circuitry for measuring CID gate characteristics.

Figure 4 Photo-micrograph of a completed 16x64 array. Except for the cross talk measurements, all the tests were carried out on either the 17th "test" column (32 cells connected in parallel) or the 16 cell test column.

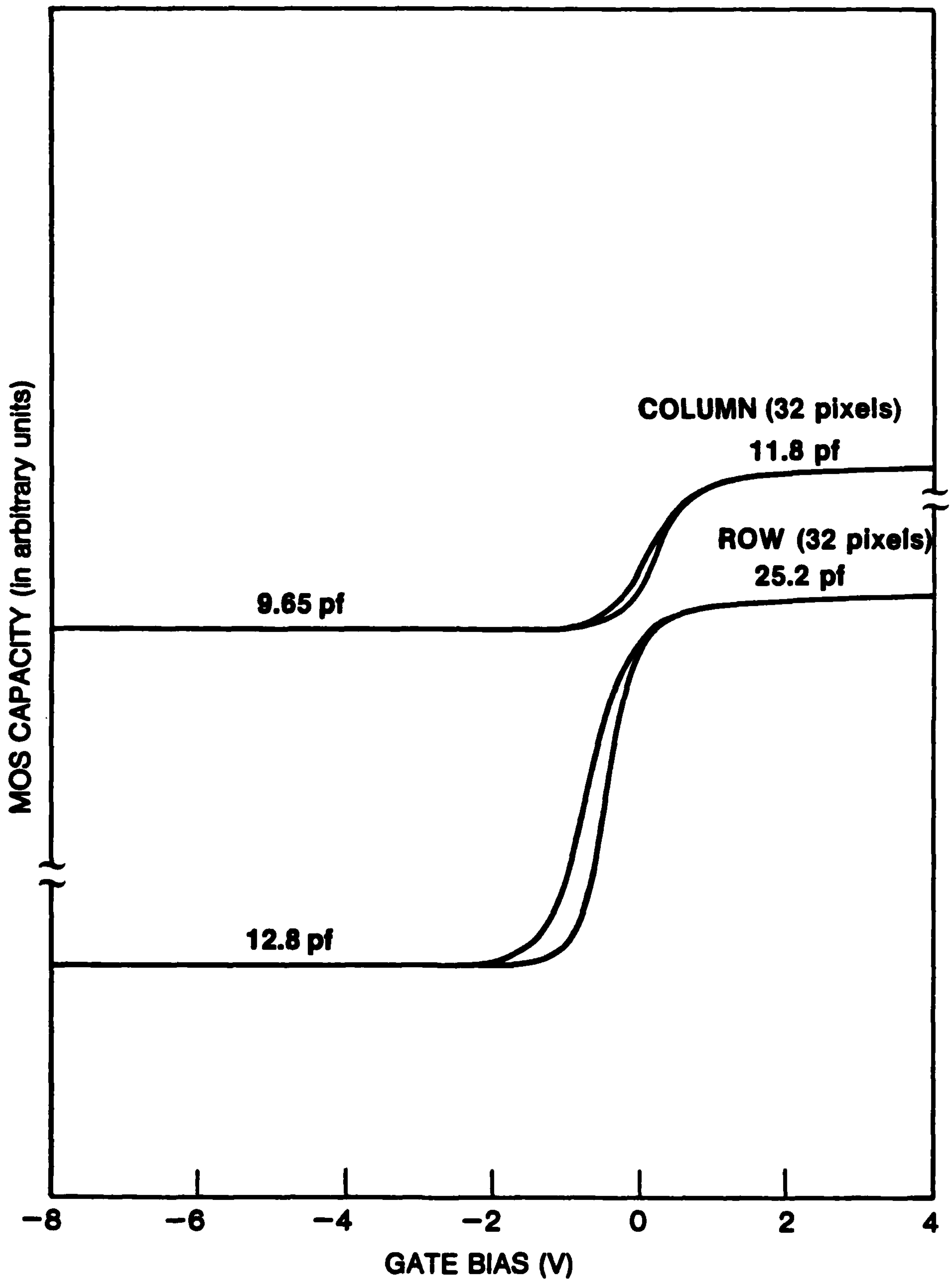


Figure 5 Capacitance-voltage (C-V) data on the 32 element test column. When the column gates are measured, the row gates are grounded and vice versa.

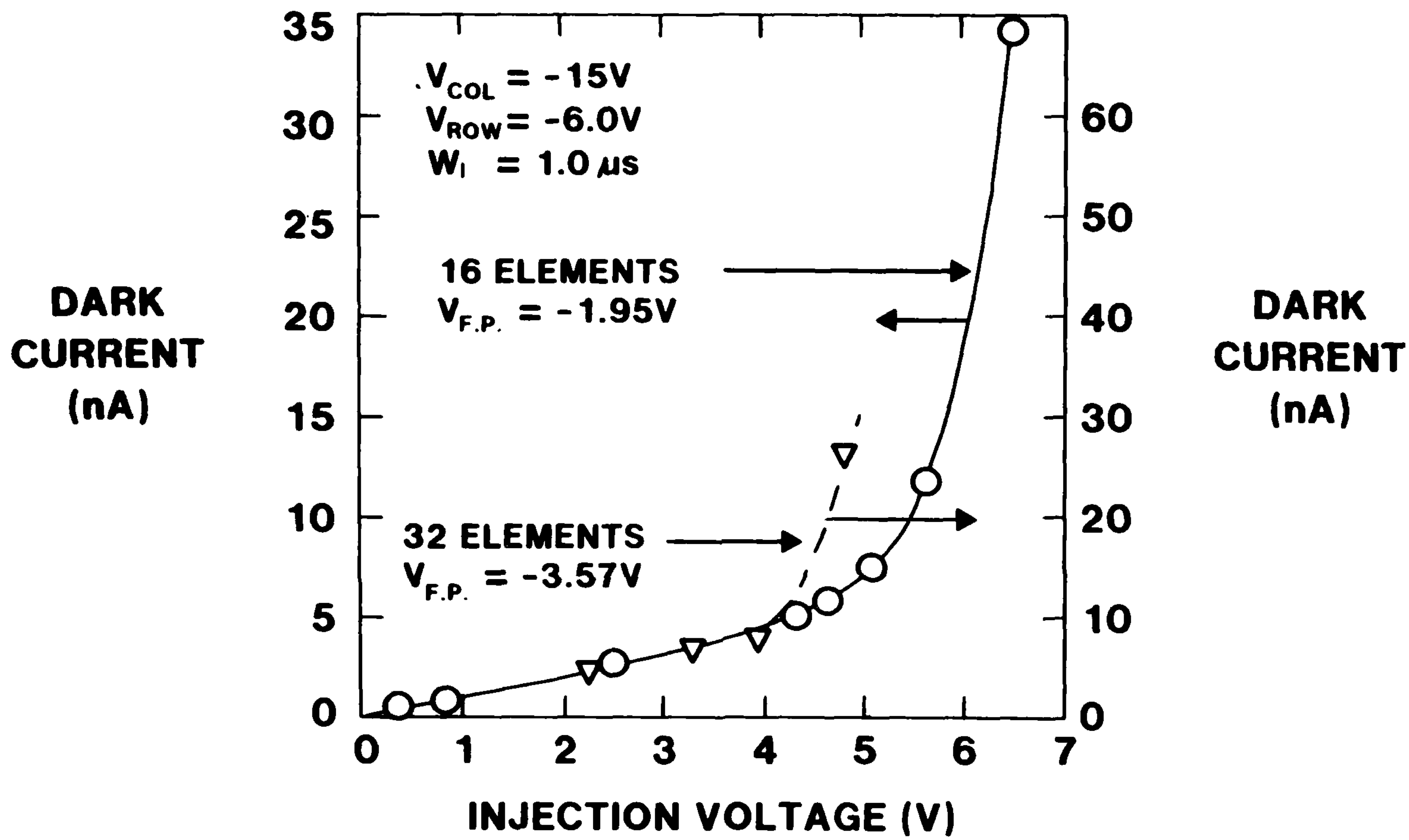


Figure 6 Dark current as a function of column injection voltage for the two test structures shown in Fig. 4. Both row and column gates are in heavy inversion and hence tightly coupled. Note that the scale for the 16 element test structure (left) is 1/2 that for the 32 element test structure (right). The field plate potential was set in each case for a minimum dark current.

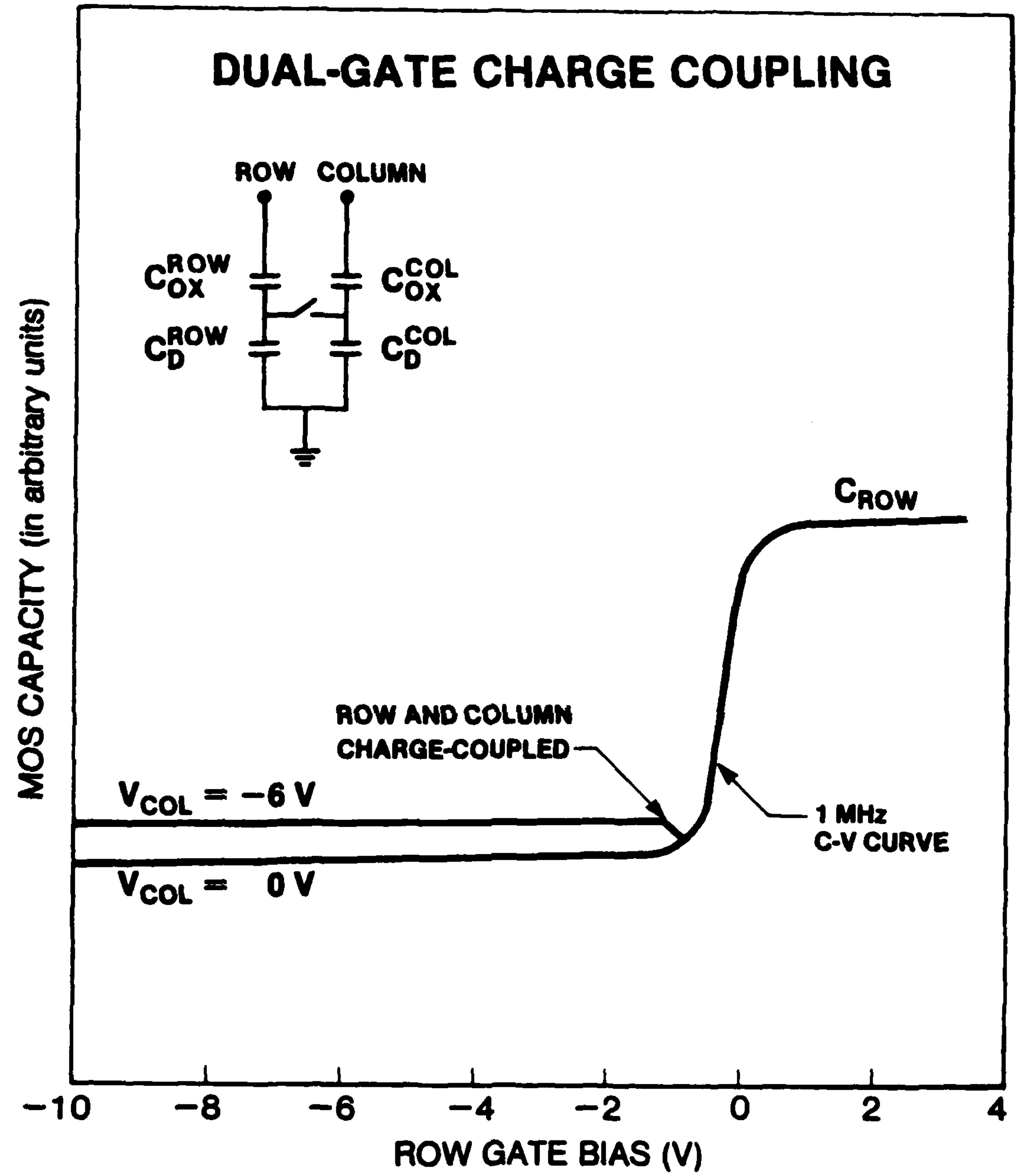


Figure 7 C-V curves of the row gate for two bias settings of the column gate. The voltage sweep is only from right to left without the retrace as in Fig. 5. See text.

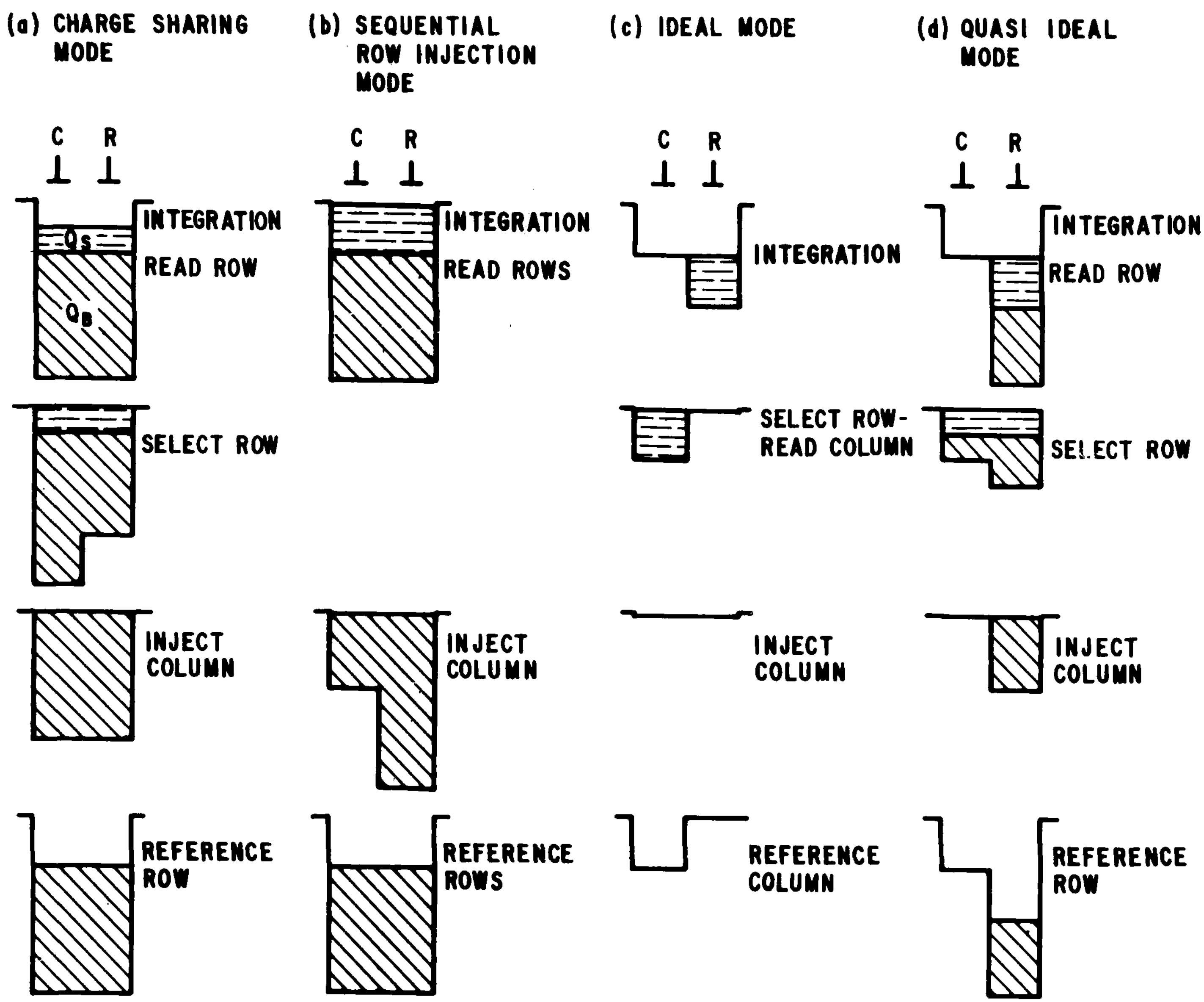


Figure 8 A comparison of four common read-out schemes for 2-D CID devices. See text. In our tests and as indicated in the figure, the "Sequential Row Injection" (SRI) mode is actually a "Sequential Column Injection" mode because of our designation of the "row" and "column" gates. (The injection is done on the smaller area gate in this mode.) The "SRI" name is retained here and in the text as the common name for this type of mode.

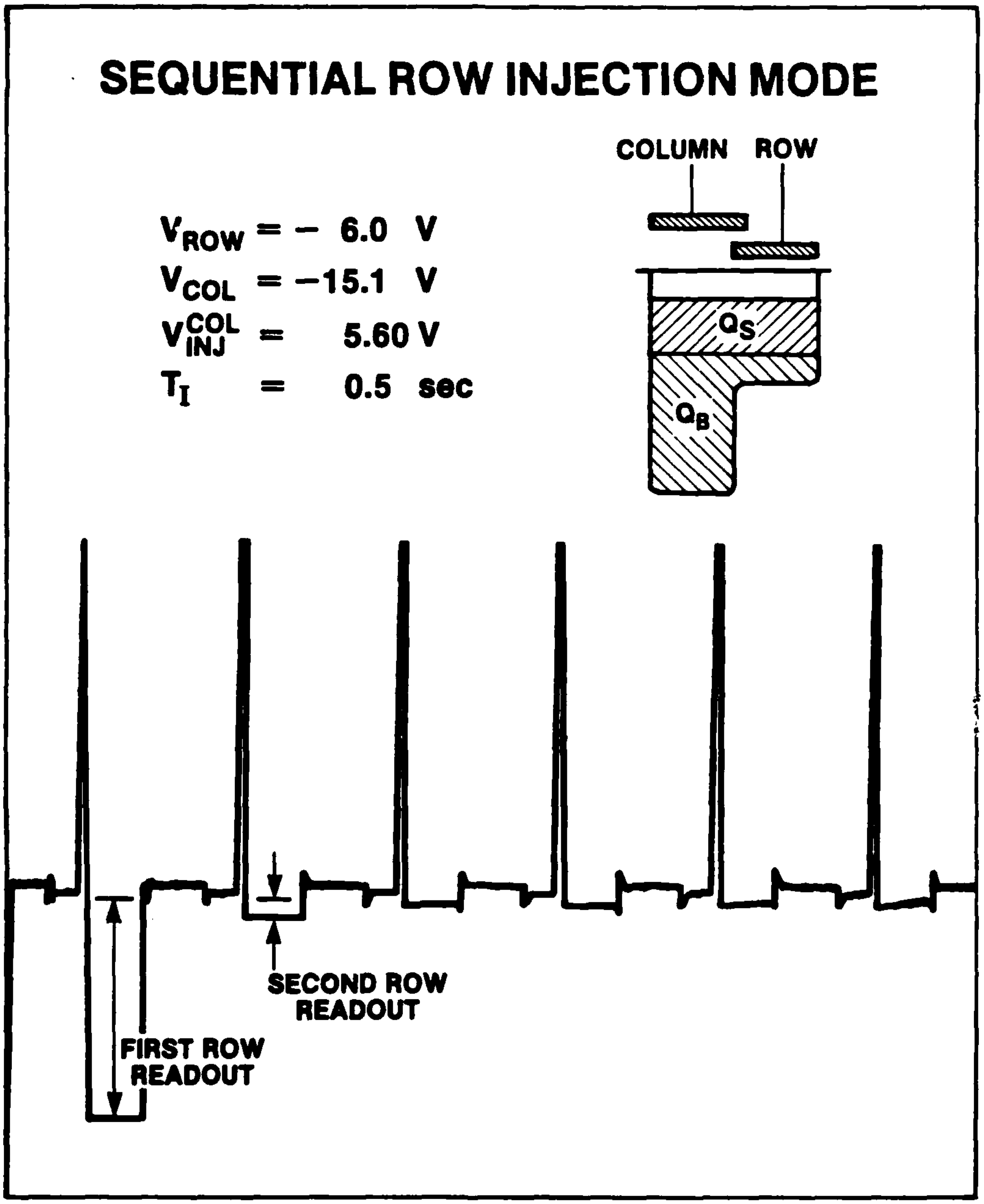


Figure 9 Read out of the 16 element 2-D test column biased in the SRI mode. See Fig. 8. This is a single sweep output of the digital scope (see Fig. 2) showing the first six row read out signals following the first six column injection pulses following the 0.5 sec dark current integration time. The bias voltages are with respect to the substrate.

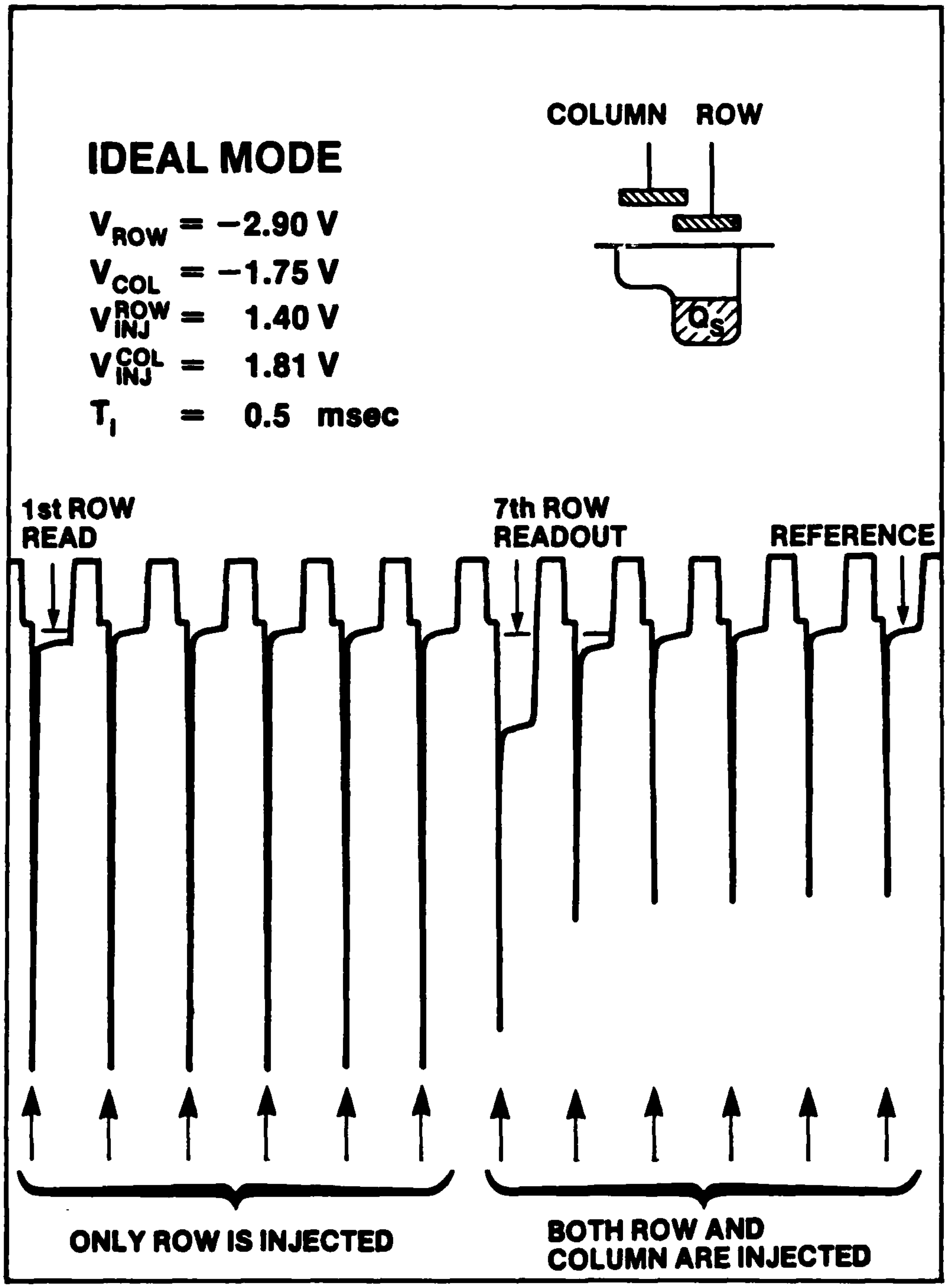


Figure 10 Read out of the 32 element 2-D test column biased in the ideal mode. As in Fig. 9, this is a single sweep output showing the row read out signals following the indicated dark current integration time. See text.

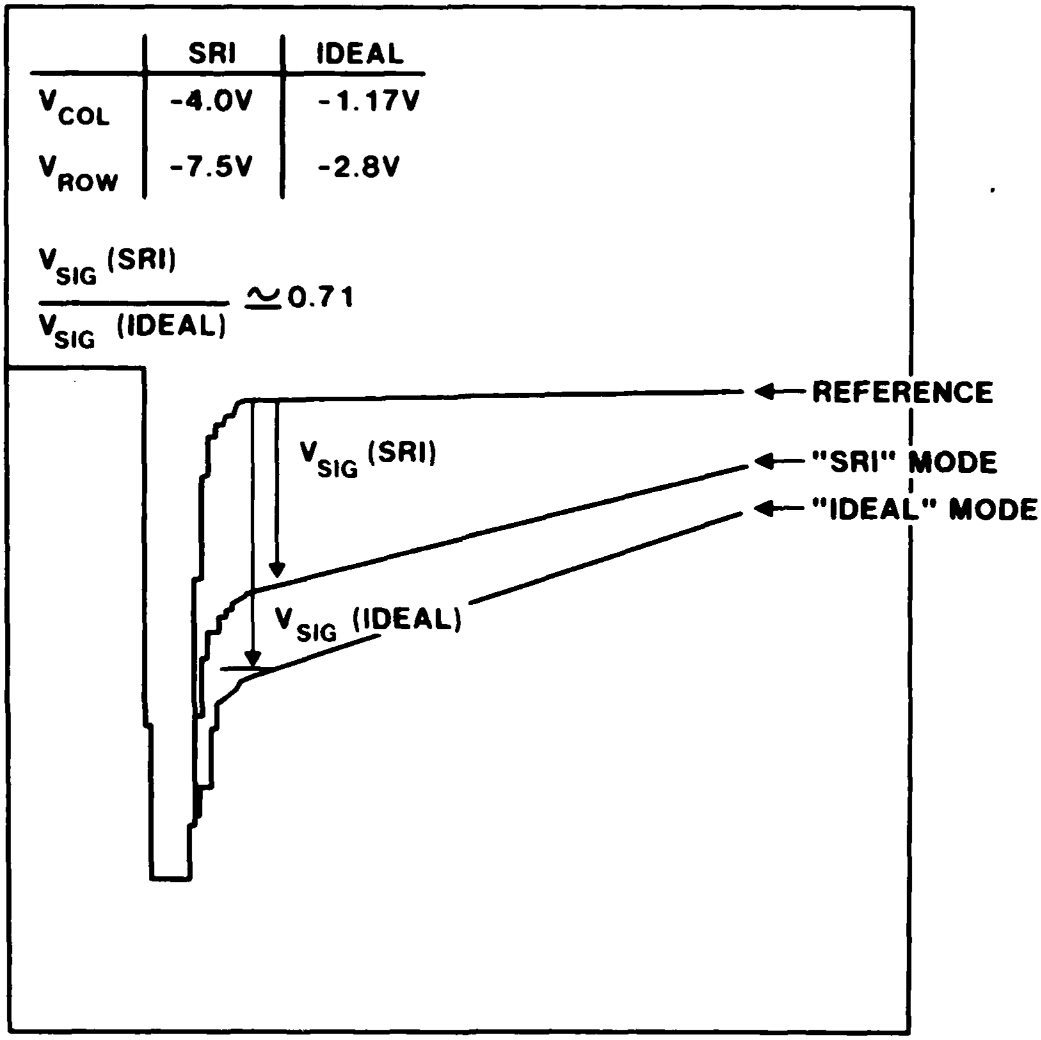


Figure 11 The row read out signal under a constant infrared flux for the SRI mode and the ideal mode of operation. Following the injection pulse, the infrared signal is seen to be integrating for 16 μsec before the reset clamp. The total well integration time between the 1 μsec injection pulses is 33 μsec.

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