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# LSI/VLSI ION IMPLANTED GaAs IC PROCESSING

Quarterly Technical Report No. 7

For Period 02/01/82 through 04/30/82

Contract No. F49620-80-C-0101

Project No. 3384-4

ROCKWELL INTERNATIONAL
Microelectronics Research and Development Center
Thousand Oaks, CA 91360

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This report covers the seventh quarter of a program aimed at fully realizing the potential of GaAs for digital integrated circuits employing depletion mode MESFETs. During this reporting period, growth of low dislocation GaAs crystals by the horizontal Bridgman method is reported. LEC semi-insulating substrate material from a commercial supplier of 3 inch diameter wafers was evaluated finding that three out of four ingots passed the qualification tests. The major process activities centered on the testing of processing equipment before the start of the 3 inch process line. Excellent results in terms of

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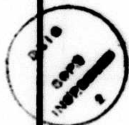
resolution and alignment accuracy of the CENSOR direct-step-on-wafer projection aligner are reported. Resolution better than 1 μm; alignment accuracy, mean + 3 σ, better than 0.25 μm were measured. Studies have been done in reactive ion etching (using 3 inch process equipment) to optimize differential etch rates. Work on MESFET modeling has continued.



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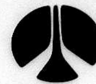

**Rockwell International**



# FOREWORD

The research covered in this report is carried out in a team effort having the Rockwell International Microelectronics Research and Development Center as the prime contractor, with two universities and a crystal manufacturer as subcontractors. The effort is sponsored by the Defense Sciences Office of the Defense Advanced Research Projects Agency. The contract is monitored by the Air Force Office of Scientific Research. The Rockwell program manager is Fred H. Eisen. The principal investigators for each organization are:

| | |
|---|---|
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| California Institute of Technology | M-A. Nicolet |
| North Carolina State University | N.A. Masnari |
| Crystal Specialties | W.P. Allred |

Numerous other researchers were involved in the work reported herein. The principal contributors were:

| | |
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## 1.0 INTRODUCTION

This report covers the seventh quarter of a program on LSI/VLSI Ion Implanted Planar GaAs IC Processing. The main objective of this program is to realize the full potential of GaAs digital integrated circuits by expanding and improving fabrication techniques as well as material growth, preparation and selection. The principal goal is to improve material and processing capabilities so that large wafers (3 inch diameter) can be processed in order to satisfy anticipated needs for high-speed low-power GaAs digital VLSI integrated circuits. In parallel with increasing circuit complexity and wafer size, the program is also directed toward the investigation of circuit reliability, and the development of processing techniques and circuit designs capable of attaining the highest reliability. Circuit design advancements are also explored. Three subcontractors, the California Institute of Technology, North Carolina State University, and Crystal Specialties, Inc. are contributing to the program with their expertise in ion beam techniques, device modeling, and crystal growth, respectively.

The principal activities in this quarter were centered on preparations for the start of the 3 inch process line, the main item being the successful testing of the Censor wafer stepper for 10X projection lithography. Work continued in several other process development activities.

Progress has been made at Crystal Specialties in the reduction of dislocations in GaAs crystals grown by the horizontal Bridgman technique. Etch pit densities varying from $10^3$ $cm^{-2}$ at one end of an ingot down to 200 $cm^{-2}$ at the other end were obtained. This work is discussed in Section 2.0.

Three inch LEC sample wafers provided by Cominco have been evaluated. Sample material from three ingots out of four passed the qualification test for ion implantation. Polishing of the wafers was also evaluated. The polishing done at Cominco still needs improvement before polished wafers could be acceptable for processing at Rockwell. This work is discussed in Section 3.0.

The Censor direct-step-on wafer (DSW) 10X projection aligner recently received and installed underwent preliminary tests. The tests on 13 wafers (416

fields) showed better than 1 μm resolution on all fields. The overall distribution of finest patterns resolved was 20% < 1 μm; 51% < 0.875 μm; and 29% < 0.75 μm. The alignment accuracy test on 10 wafers indicated that the mean + 3σ is better than 0.25 μm. These results are discussed in Section 4.0.

A new recently installed reactive ion etcher capable of handling 3 inch wafers was evaluated. Experiments have been carried out on the new equipment to optimize etch rates for maximum selectivity between dielectrics and photoresist. This work is described in Section 5.0.

The work at North Carolina State University during this period has been concentrated on scaled MESFET devices. A transistor with a gate length of 0.2 μm and gate to source/drain spacings of 0.2 μm has been analyzed both by two-dimensional modeling and Monte Carlo analysis. This subject is discussed in Section 6.0.

## 2.0 DISLOCATION DENSITY REDUCTION IN HORIZONTAL BRIDGMAN GaAs

Considerable progress has been made at Crystal Specialties in the reduction of dislocations generated during crystal growth by the horizontal Bridgman method. Single crystals with dislocation densities as low as 200 etch pits/$cm^2$ have been grown.

The crystals were grown in the (111) and (110) directions. The low dislocations were obtained by close control of the thermal gradients and arsenic pressure. Previously, the dislocation density of an ingot progressively increased toward the tail of the ingot. Using these new techniques of growth, the dislocations are considerably lower at the tail of the ingot. Typically, ingots have dislocations which vary from about $5 \times 10^3$ pits/$cm^2$ at the front of the ingot to about $1 \times 10^4$ pits/$cm^3$ at the tail. The new ingots start at about $1 \times 10^3$ pits/$cm^2$ on the front of the ingot, and improve to a value of about 200 pits/$cm^2$ at the back end of the ingot.

It is evident from this work that very low dislocation density material can now be grown on a routine basis. Since twins and lineage arise from dislocations, it appears that lowering dislocation densities may allow for longer boats to be used without incurring in twinning and lineage problems. This may lead to improvements in yield and lower cost of production.

## 3.0 QUALIFICATION OF SUBSTRATES FROM COMMERCIAL SUPPLIERS

Qualification studies on commercial large diameter (3 inch) LEC GaAs materials resulted in the selection of thee Cominco ingots as suitable for integrated circuit processing. Another Cominco ingot did not pass the qualification tests. Satisfactory resistivity after cap and anneal, and acceptable depletion voltages were observed in the three qualified crystals. This is a very promising result.

Wafer preparation was also evaluated. The supplier was cooperative in realigning their flat system to provide for automatic crystallographic orientation of the large wafers coinciding with the flat orientation system developed in the Rockwell LEC growth program. Edge beveling was not yet available. Difficulties in polishing from the supplier still preclude the purchase of polished wafers. Therefore, all the materials are being bought as-cut for polishing at our facility.

Figure 1 indicates the degree of flatness typical of purchased materials. The numerous fringes indicate a high center with several microns drop-off toward the edge. The Rockwell polishing capability results in as few as 3 - 5 fringes on the same size substrate. Upgrades in polishing equipment are under way at several commercial GaAs suppliers to improve their polishing results.

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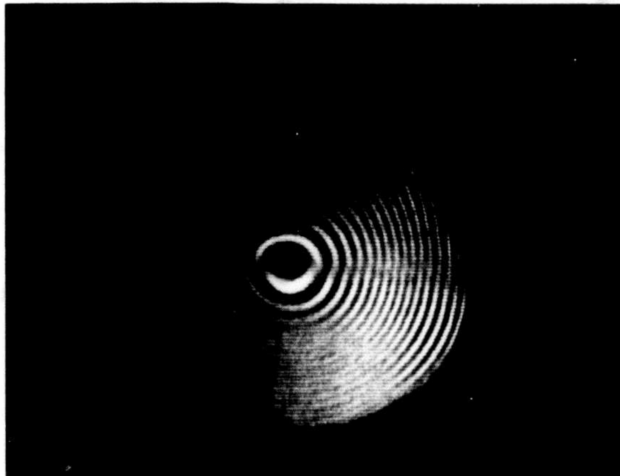

Fig. 1 Flatness photo of 3-inch polished GaAs wafer as received from the supplier. The wafer exhibits a high center.

## 4.0 DIRECT-STEP-ON-WAFER PHOTOLITHOGRAPHY

It is indispensable for the attainment of GaAs LSI/VLSI capability to fabricate integrated circuits on large diameter wafers. Based on this consideration, a decision was made to make a transition from the present processing 1 inch square GaAs wafer to the processing of 3 inch diameter circular wafers. It would have been extremely impractical and probably impossible to make this change with the limitations imposed by the Canon 4X projection aligner which has been used in all the GaAs digital IC projects at our facility. Consequently, a state of the art, direct step on wafer (DSW) system was selected and acquired. A Censor SRA-100 10X projection aligner has been procured and is now fully operational. Figure 2 is a photograph of a Censor SRA-100 DSW system. This system is equipped to handle both 1 inch square wafers and 3 inch diameter circular wafers, thereby allowing an easy photolithography processing transition to take place.

The Censor DSW was selected because it clearly had the best specifications and it contained certain features not available on any other equipment. The specifications of this system are: better than 1 μm resolution; automatic X, Y and θ field by field alignment with ±0.1 μm (1σ) overlay precision; automatic focusing; and field by field automatic leveling. This last feature, field by field leveling, is unique to this system and is particularly important since the Censor high resolution Zeiss lens has a small depth of focus (±1.5 μm) by virtue of its high (0.35 na) numerical aperture. In practice, this local field-by-field leveling feature eases the flatness specification of the GaAs wafers, and allows the submicron resolution capability of the lens system to be utilized effectively.

This Censor DSW equipment will provide more repeatable and precisely controlled photolighographic processing. For example, Fig. 3 shows the histograms of alignment vernier readings ($X_{Top}$, $X_{Bottom}$, Y) from 10 wafers randomly selected for an alignment test. These statistical results confirm that this equipment is capable of an overlay accuracy of mean +3σ of < 0.25 μm.

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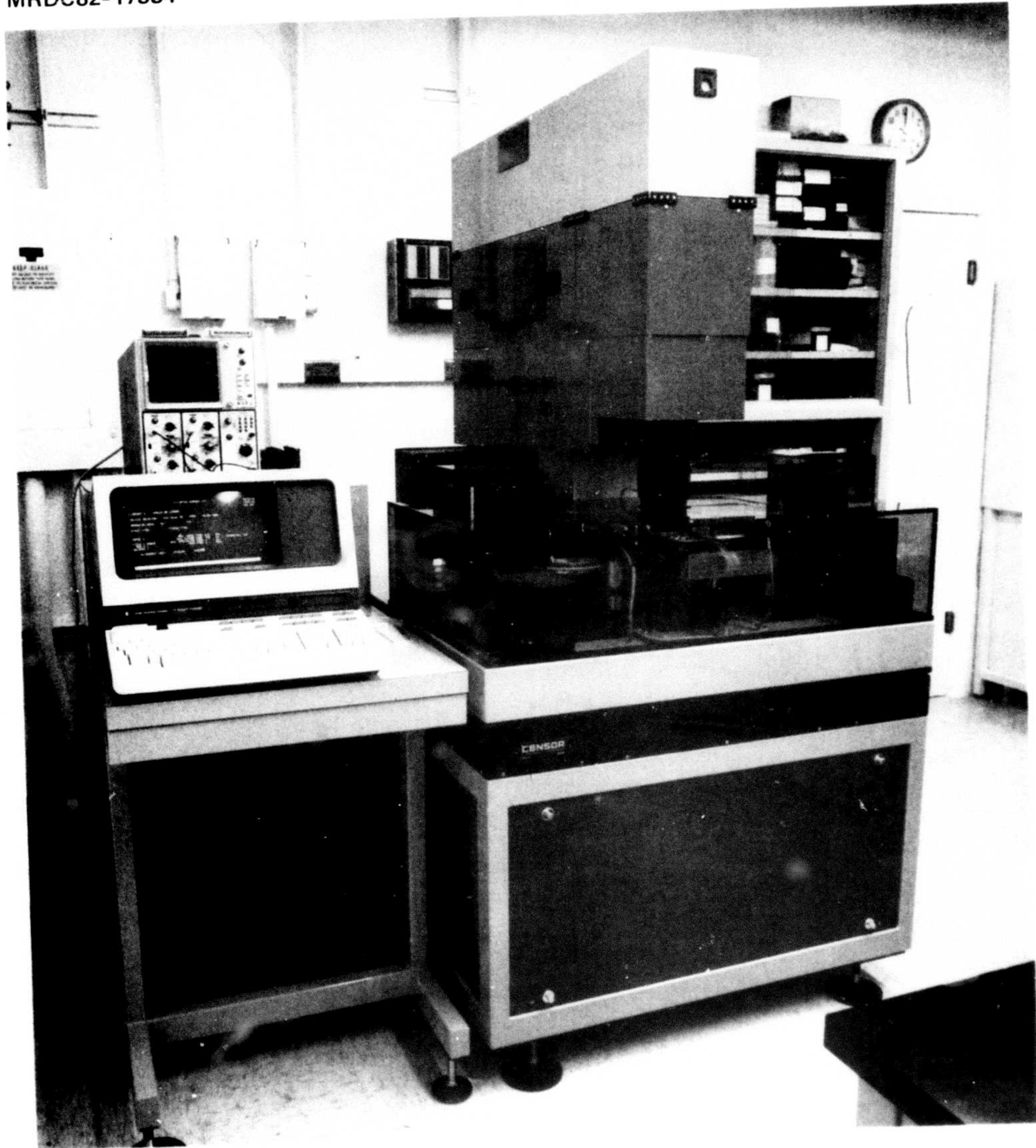


Fig. 2 Photograph of a Censor SRA-100 DSW system.

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Fig. 3 Characterization of the alignment accuracy of the Censor projection aligner.

Besides the excellent overlay results, resolution patterns surveyed during the same tests showed resolution consistently lower than or equal to 1 µm. The majority (>50%) of the patterns exhibited ~0.875 µm resolution on all the wafers surveyed. Figure 4 illustrates the distribution of patterns resolved as measured from 13 three-inch wafers (416 fields).

While these early tests have clearly demonstrated the 1 micron resolution and better than 0.25 µm overlay capability of this equipment, it must be pointed out that these tests were conducted on unprocessed (flat topology) wafers with optimal resist patterns for the overlay tests. Photolithography process optimization on GaAs IC wafers at various process steps will require further work due to the constraints and sensitivity of DSW automatic focusing, leveling and alignment techniques. At this time, several areas have been identified for further investigation and development. For instance, every GaAs process level will require the determination of a precise resist thickness which will yield optimal ≤1 µm resolution while still maintaining process compatability for the subsequent process step (e.g., implant, lift-off, plasma etch, etc.). Alignment marks must be optimized for edge acuity and maximum contrast in order to obtain the best possible overlay precision. A metal alignment mark embedded between the $Si_3N_4$ and $SiO_2$ layers will be used for the majority of the GaAs process levels. Identification of a refractory metal alignment mark that can be both precisely replicated with high yield and survive the 850°C post implantation anneal is another task to be undertaken.

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13 WAFERS
416 FIELDS

NUMBER

1400
1200
1000
800
600
400
200

0.625 0.75 0.875 1.0 1.125

SMALLEST PATTERN RESOLVED (μm)

Fig. 4 Censor SRA-100 resolution test results.

## 5.0 DRY LITHOGRAPHY REPLICATION TECHNIQUES - REACTIVE ION ETCHING

Dry replication processing techniques such as reactive ion etching (RIE), plasma etching (PE) and ion milling (IM) are used extensively in the developed planar GaAs LSI fabrication technology. Several new dry etch process systems capable of handling 3 inch wafers were installed and were evaluated. One of the critical processes is reactive ion etching, which is used to open windows in the dielectrics for the deposition (and indirect lifting) of metallizations. Efforts were made in this quarter to characterize the new equipment and, at the same time, optimize differential etch rates.

In the present process, the etch rates for $Si_3N_4$ and photoresist are twice the rate of $SiO_2$. These unfavorable etch ratios make it difficult to etch through $SiO_2$ films completely without the risk of etching too far through the underlying $Si_3N_4$ layer or eroding the photoresist pattern beyond its usefulness for lift-off. Minimum acceptable etch ratios established for a practical LSI/VLSI process are a $Si_3N_4/SiO_2$ etch rate ratio of 1, and a $SiO_2$/photoresist etch rate ratio of >2.

Developments toward achieving these conditions are in progress. The etch rate of $SiO_2$ has been shown to be higher than $Si_3N_4$ and photoresist when using $CHF_3$. It is theorized that in a $CHF_3$ plasma, the addition of hydrogen to the freon-based chemistry scavenges fluorine radicals through the formation of HF; HF increases the probability of carbon deposition, thereby reducing the etch rate, and providing a protective film of carbon which minimizes the removal of the photoresist mask. However, in practice the etch rate of $SiO_2$ is maintained since oxygen is released during the $SiO_2$ etching. It is believed that the oxygen reacts locally with carbon on the $SiO_2$ surface forming volatile CO or $CO_2$ compounds, so that the etching of $SiO_2$ is not supressed as in the case of photoresist.

Another factor which can effect the etch ratios is the gas residence time $\tau$, $\tau(s) = P(Torr) \times V\ (liter)/Q\ (Torr\ liter/s)$, where P is the operating pressure, V is the volume of chamber, which is constant, and Q is the flow

rate. The residence time is therefore a function of the flow rate when the operating pressure is kept constant. The etch rate of $SiO_2$, $Si_3N_4$ and photoresist as a function of flow rate (residence time) in a $CHF_3$ plasma is shown in Fig. 5. These data indicate that etching in $CHF_3$ at a flow rate greater than 40 SCCM (at 70 mTorr) can provide the etch rate requirements previously established for this process. However, heavy polymer formation in the $SiO_2$ windows and on the surface of the photoresists has restricted the usefulness of this particular plasma etching approach at present. Further work is required in order to understand the plasma chemistry interactions and evaluate alternative chemistry. Presently, experiments have been initiated using $H_2$ and $CF_4$ gas mixtures. Early results look very encouraging for achieving both the desired etch ratios and controlling the polymer redeposition.

An optical emission spectroscopic system has been set up on the new RIE equipment. This system can be used as an optical end-point detector as well as a diagnostic tool. Figure 6 shows the different emission spectra obtained during $SiO_2$ and $Si_3N_4$ etching in a $CF_4$ plasma. Note these spectra are almost identical except at 3870 . In our particular application, an increase in the intensity of the $Si_3N_4$ 3870Å line can be used to tell when the $SiO_2$ has been etched through to the underlying $Si_3N_4$. In practice, these differences in the emission spectrum can only be used as an end-point detection method if the sensitivity of the electronics can be improved or the difference signals increased. Improvements in these methods or alternative end point techniques will be investigated further during this program.

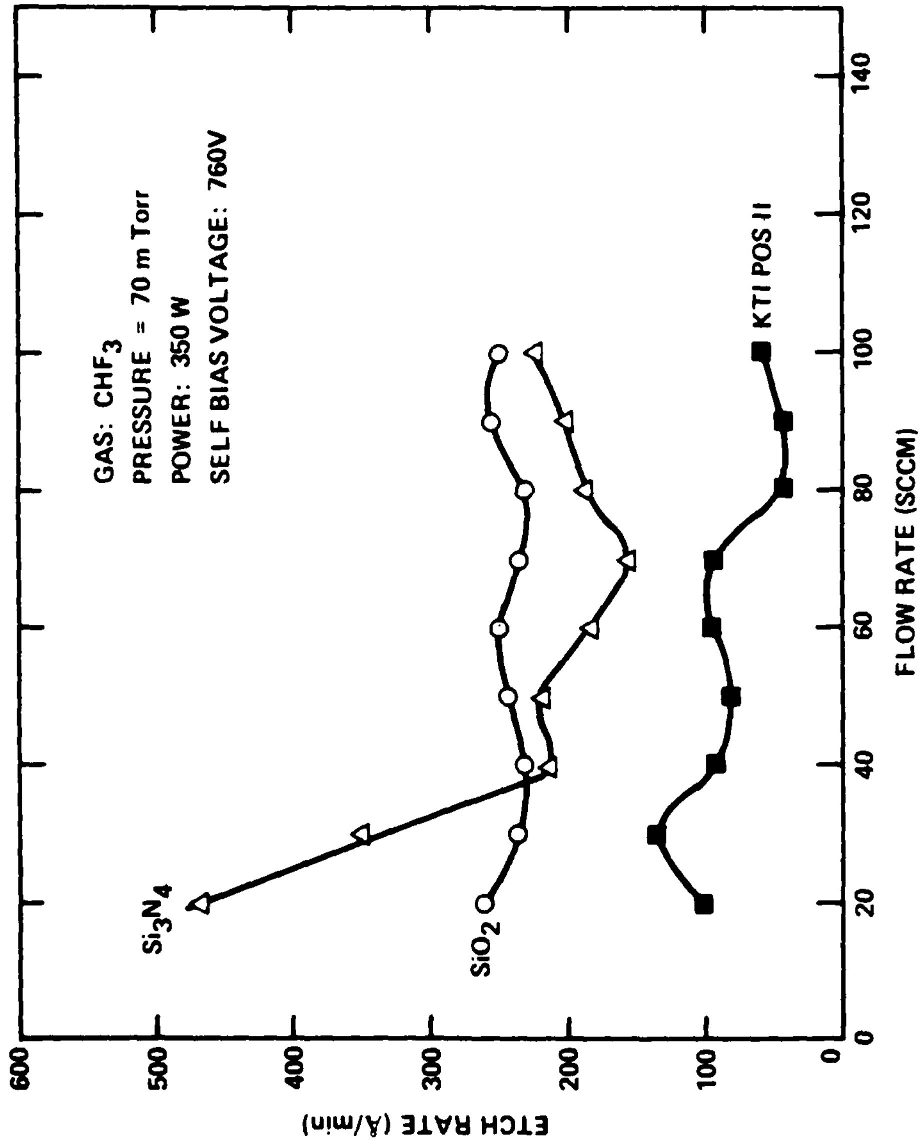


Fig. 5 RIE etch rates for $Si_3N_4$, $SiO_2$ and photoresist as a function of the flow rate in a $CHF_3$ plasma at a constant pressure.

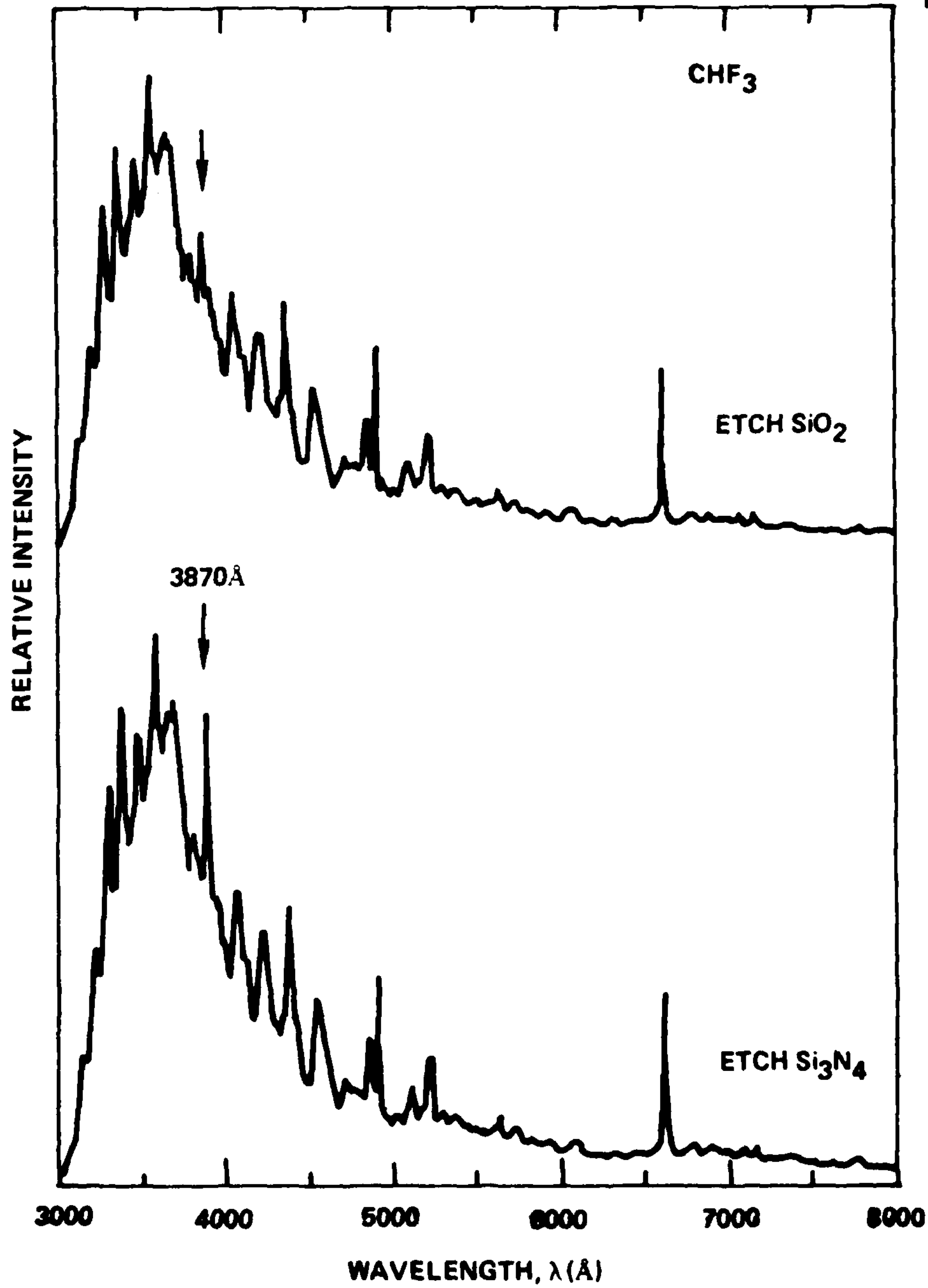


Fig. 6 Plasma emission spectra obtained during $SiO_2$ and $Si_3N_4$ etching in a $CHF_3$ plasma.

# 6.0 MESFET MODELING

The modeling activities at North Carolina State University have continued the three general areas.

## 1. Two-Dimensional FET Modeling

The work during this period was concentrated on a scaled FET device. The lateral dimensions of the FET were reduced by a factor of 5 to yield a device with a gate length of 0.2 µm and source-to-gate and gate-to-drain spacings of 0.2 µm. The doping density in turn was increased by a factor of 25. Ideally this will cause the depletion layer widths to scale by a factor of 5 and keep the relative widths of the channel and depletion layers the same as the unscaled device. Finally the depth scale on the implanted channel was reduced by a factor of 5. The resulting channel impurity profile is shown in Fig. 7.

The calculated I-V characteristics for this scaled device are shown in Fig. 8. The characteristics are similar to those of previously modeled larger devices except for the increased current scale. Other calculated device parameters are seen in Table 1. The calculated capacitance values are similar to those of a 1 µm gate device, as expected from an ideal scaling of the device dimension and the doping density. The calculated $f_T$ of 61 GHz is considerably larger than that of the 1 µm device. This improvement occurs mainly from the improved $g_m$, since the capacitance values have not changed significantly. These results are now being compared with the two-dimensional Monte Carlo results.

## 2. Analytic FET Model Development

Programming of the one-dimensional MESFET model for arbitrary doping profiles is essentially complete. The program accepts material and geometric input data including donor density as a function of depth and computes values for a thirteen element equivalent circuit. The circuit is then analyzed and device figures of merit along with two-port S-parameters are calculated within the program.

Fig. 7 Doping profile used to analyze a scaled down MESFET with 0.2 µm gate length.

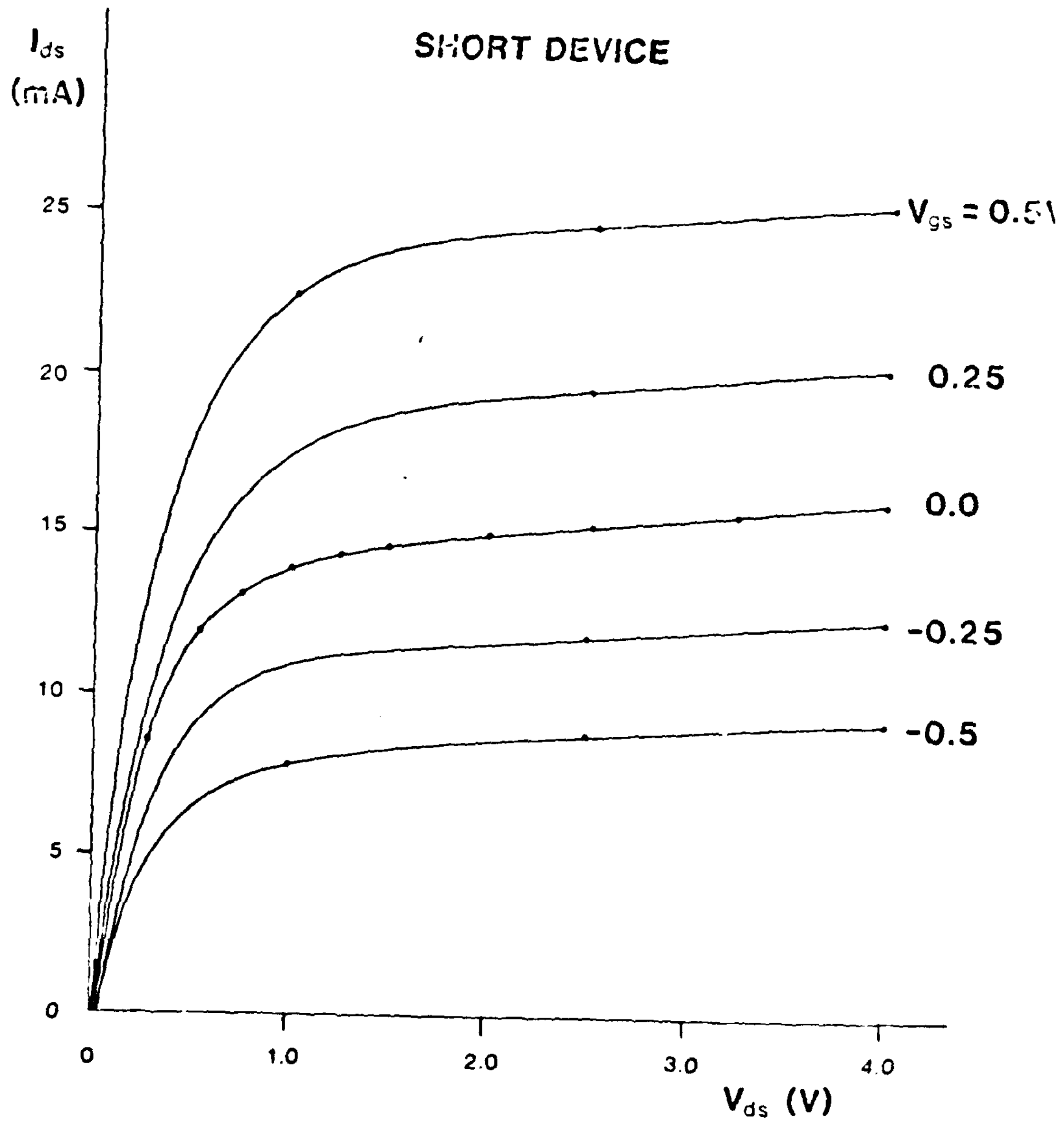


Fig. 8 Calculated I-V characteristic of a scaled MESFET with 0.2 µm gate length.

Table 1

Calculated Device Parameters for Scaled Device

$C_{gs}$ = 0.04114 pF  $C_{gd}$ = 0.004507 pf

$g_m$ = 15.76 mA/V  $g_d$ = 0.5826 mA/V

$f_T$ = 60.98 GHz  $V_{gs}$ = 0

| $V_{DS}$ (V) | 0.25 | 0.5 | 0.75 | 1.0 | 1.25 | 1.5 | 2.0 | 2.5 | 3.25 | 4.0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{DS}$ (mA) | 8.664 | 12.05 | 13.39 | 14.02 | 14.42 | 14.72 | 15.17 | 15.50 | 15.89 | 16.199 |

$I_{DS}$ (mA)

| $V_{gs}$ (V) | $V_{DS}$ = 1.0 V | $V_{DS}$ = 2.5 V | $V_{DS}$ = 4 |
|---|---|---|---|
| .5 | 22.75 | 24.62 | 25.39 |
| .25 | | 19.62 | 20.36 |
| 0 | | 15.50 | 16.20 |
| -.25 | | 11.84 | 12.43 |
| -.5 | 7.884 | 8.856 | 9.38 |

The model simulation, which requires less than 30 seconds of CPU time to run, is relatively inexpensive to use. This allows for extensive studies of device performance as a function of fabrication controllable parameters to be made. Guidelines for the desired depth, width, and peak of dopant implants, as well as for the desired geometric dimensions can be determined.

Efforts are currently being made to confirm that the predicted I-V characteristics of the model match those of measured devices. This requires that the ionized donor concentration of the measured devices be known as a function of depth into the active layer. The donor profile for ion-implanted devices, however, will differ from the free-carrier profile as determined from C-V measurements. Preliminary calculations indicate that this difference may affect device performance significantly. A method for more precisely determining the donor profile from C-V data is therefore being developed.

3. Monte Carlo Analysis

Generation of the two-dimensional Monte Carlo I-V characteristics of the 0.2 μm gate device, described in the previous report, has been completed. The results are presented in Fig. 9 for a channel width of 50 μm. The most noticeable feature of the I-V characteristics is the static negative differential resistance region seen for a gate bias of 0 V. This region has been observed by others using analytical device-modeling programs. It is thought to be an artifact, and it has been attributed to insufficient spatial resolution.

Figure 10 shows the I-V characteristics of the same device obtained using a 2D analytical device analysis program. No negative resistance region is observed, thus indicating that spatial resolution is not the cause of that phenomena as observed in the results of the 2D Monte Carlo simulation. However, the currents obtained from the 2D Monte Carlo simulation are about twice as large as those from the device analysis program. This difference may be due to the fact that the Monte Carlo analysis does not assume static velocity-field characteristics, thus permitting carriers to experience velocity overshoot. The higher carrier velocities resulting from velocity overshoot will give rise to larger currents. This is being investigated further and will be reported in future reports.

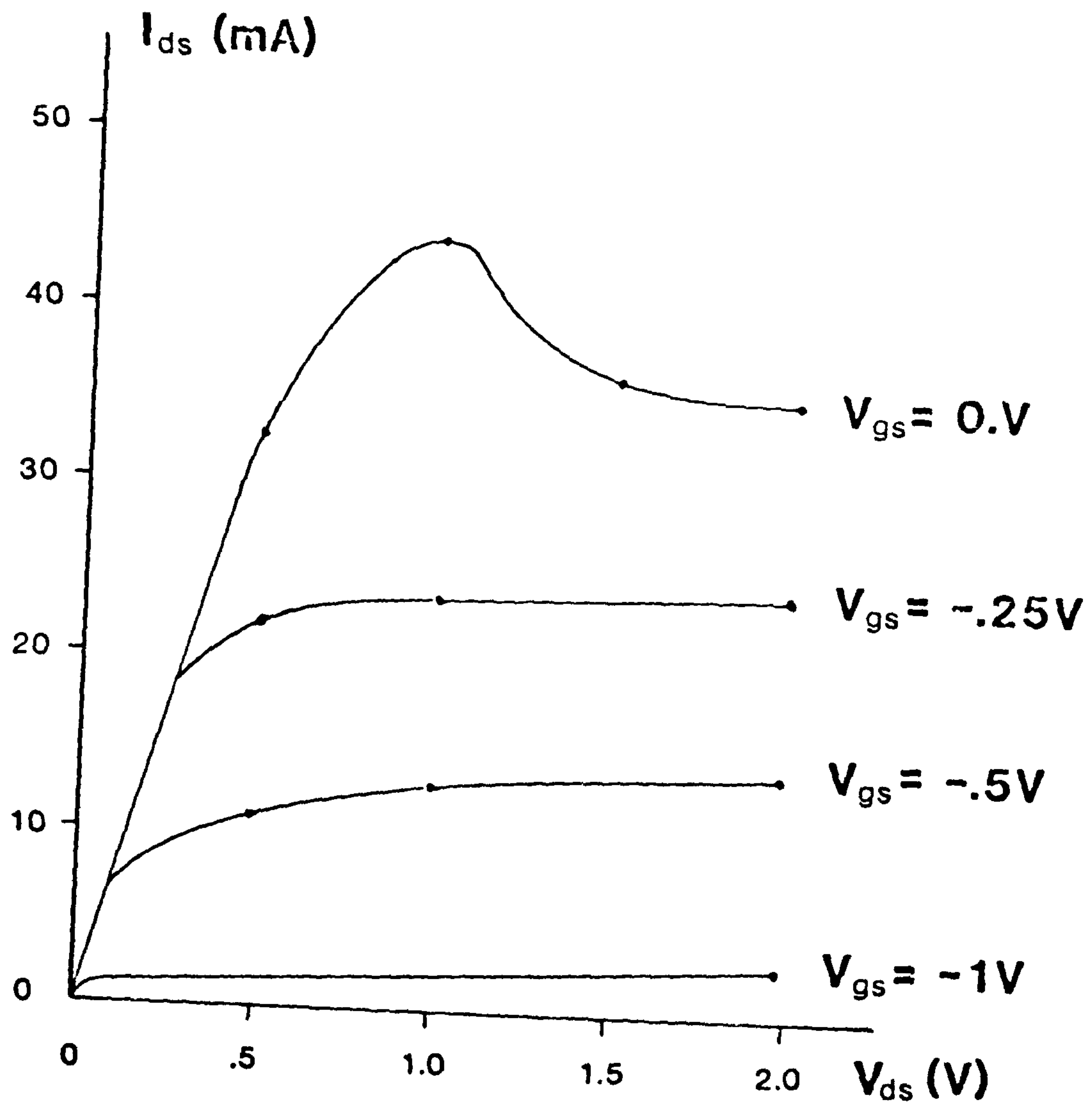


Fig. 9 I-V characteristics of 0.2 μm gate MESFET from the two-dimensional Monte Carlo program.

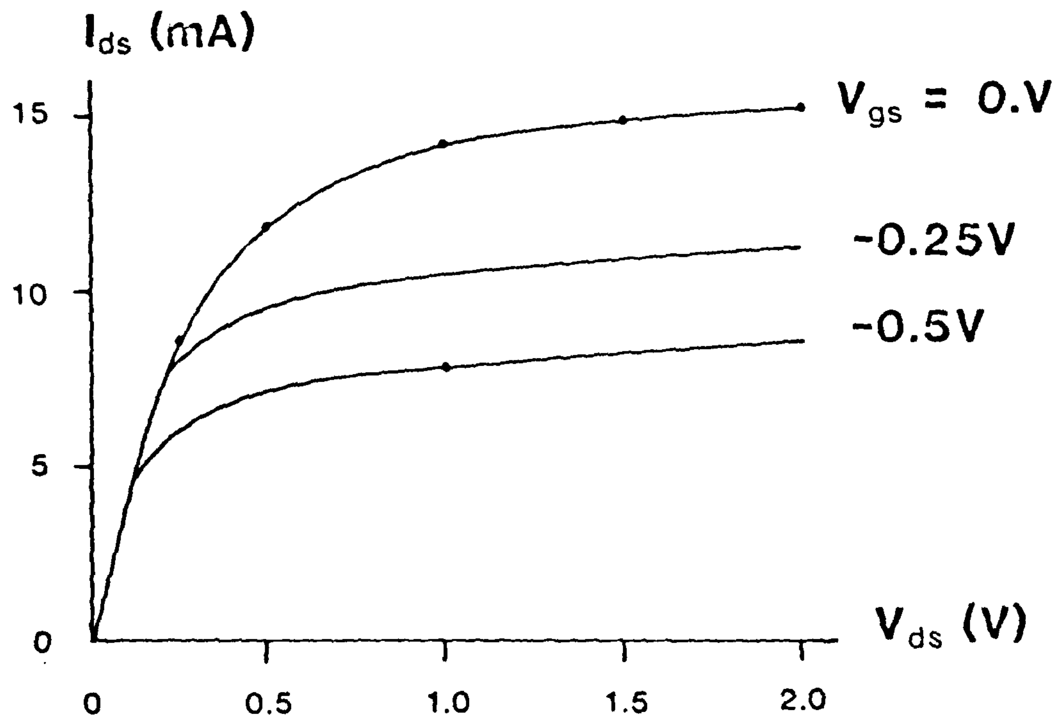


Fig. 10 I-V characteristics of 0.2 μm gate MESFET obtained from the 2D device analysis program.