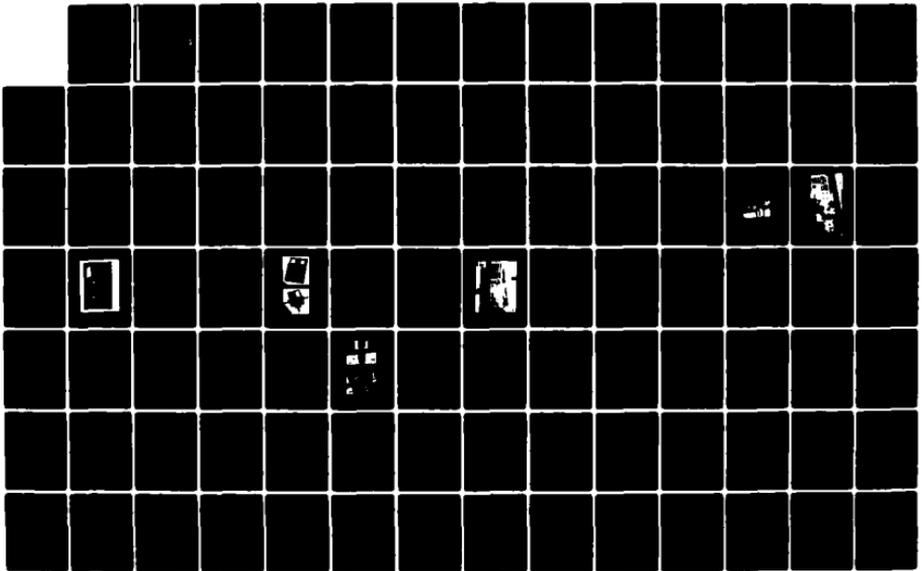


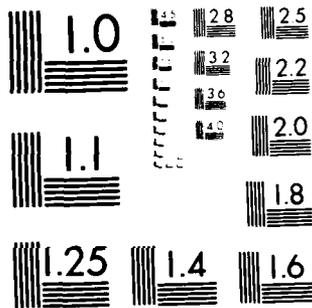
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# FET Noise Studies

## Final Technical Report

Contract No. F49620-81-C-0052

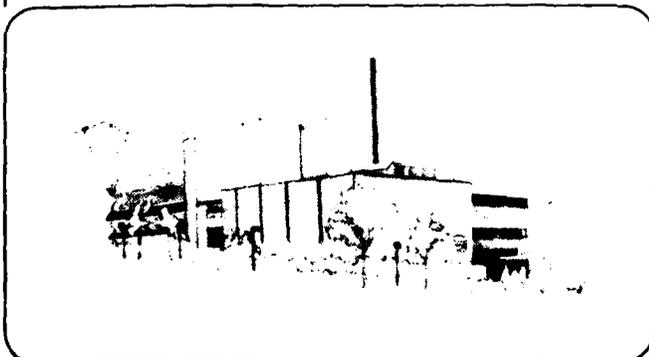
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Prepared for  
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progress made during the report period in understanding the relationship between fabrication technology and near-carrier oscillator noise of FETs.

The IV characteristics, baseband noise, and near-carrier FM noise of GaAs FETs were measured for a variety of fabrication technologies. These included FETs with Al, CrAu, and TiPtAu gates, with  $SiO_x$ ,  $Si_3N_4$ , and polyimide passivations, with epitaxial and implanted channels, and with mesa and oxygen implant isolation.

It was shown that bulk and surface traps were primarily responsible for the hysteresis of the IV characteristics, and the baseband and near-carrier 1/f noise. The hysteresis vanished at high temperatures or under illumination of the FET surface with a GaAlAs laser. The baseband noise increased with laser illumination.

The near-carrier oscillator FM noise was unaffected by gate technology, but increased for  $SiO_x$  passivation. Neither  $Si_3N_4$  or polyimide passivation, or oxygen implant isolation had any effect on this noise. The highest level of oscillator noise was measured for an FET with an implanted channel.

The best FM oscillator noise performance measured on epitaxial channel FETs was over 20 dB better than any results reported in the literature.

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## 1.0 INTRODUCTION

The performance of the voltage-controlled oscillator (VCO) is critical to the success of many radar systems, especially electronic countermeasure systems until recently, the only viable solid-state sources were the bipolar transistor at the lower microwave frequencies (L- to S-bands) and the Gunn and IMPATT diodes at higher frequencies.

In recent years, however, the gallium arsenide field-effect transistor (GaAs FET) has demonstrated its superiority as a low-noise amplifying element at C-band and above. The intrinsic noise mechanisms responsible for its extremely good noise performance are well understood, and have been discussed by workers at this laboratory and elsewhere.<sup>1</sup>

There is thus a growing interest in the use of FETs as wide-band voltage-controlled oscillators. Starting from the early work reported by this laboratory,<sup>2</sup> numerous papers have been published on experimental results obtained with FET oscillators.<sup>3</sup> It is now evident that octave-tuned GaAs FET oscillators, operating up to 20 GHz, with usable power output, are realizable.

The GaAs FET has one major drawback which makes it unacceptable for many radar systems applications, namely, its rather high level of near-carrier 1/f noise, especially in the FM spectrum. In all cases where oscillator noise spectra have been reported, unless extreme measures are invoked (such as the use of temperature-compensated high-K dielectric cavities for frequency stabilization) the near-carrier noise level of GaAs FETs has been higher than that for comparable Gunn and avalanche diode oscillators.<sup>2,3,4</sup> Reduction of the noise level of the FET oscillator is highly desirable, because this device has many attractive features: its inherent wide-band performance; the variety of its possible operating modes, such as grounded source and grounded gate; and its ease of design.

The need for reduction of the 1/f noise is becoming evident in another important application of FETs, namely microwave monolithic circuits. Here,

ultra-broadband monolithic amplifiers ( = dc-to-microwave) are exhibiting very poor noise figures at the lower end of the band, principally because of  $1/f$  noise.<sup>5</sup>

If the origin of this excess noise can be identified and either eliminated or reduced, it is believed that FETs can become important candidates for low-noise VCOs and mixers and low-frequency monolithic amplifiers. The availability of low-noise devices would open the possibility of construction of low-noise front ends in monolithic form with FETs used as preamplifiers, oscillators, and mixers.

The purpose of the research summarized in this report was to obtain a better understanding of excess noise in a GaAs FET, an understanding from which one might develop the means to reduce this noise to an acceptable level.

#### 1.1 Review of Preceding Contractual Research

During a preceding contractual effort performed at this laboratory, also funded by AFOSR\*, considerable headway was made towards development of a better understanding of  $1/f$ -like noise in GaAs FETs. For example, the following conclusions were drawn from that research:

(1) There exists a strong correlation between the  $1/f$  baseband drain current noise, and the near-carrier FM oscillator noise.

(2) The principal mechanism by which baseband noise manifests itself as near-carrier FM oscillator noise is by depletion layer modulation of the source-gate capacitance.

---

\*"FET NOISE STUDIES", Final Technical Report, Contract No. F49620-79-C-0024, March, 1981.

(3) The primary source of baseband noise (hence near-carrier oscillator noise) is either deep bulk traps within the depletion layer under the gate, or surface states at the interface between the gate and semiconductor, or on the exposed semiconductor surface adjacent to the gate. Surface states are considered the most probable source.

(4) Little or no correlation exists between the microwave noise figure (white noise) of an FET and the near-carrier FM noise. Within a megahertz from the carrier, the baseband noise dominates the white noise even when the noise figure is as high as 6 dB.

(5) The near-carrier FM noise level is reduced by about 10 dB when a buffer layer separates the active layer from the substrate.

In the present contractual study, this research has been extended. Specifically, the effects of process technology, especially that related to surface treatment and gate metallurgy, on  $1/f$  noise were studied.

## 1.2 Scope of Present Contractual Research

### 1.2.1 Introduction

It has been mentioned that the most consistent feature of the near-carrier noise is an inverse dependence on frequency offset from the oscillator carrier, which noise appears to emanate, in large part, from surface states. Part of the present research effort was devoted to evaluation of methods for conditioning the surface by processing techniques such as dielectric passivation and by proper selection of the gate metal. Thus the research to be described includes new device and material fabrication techniques encompassing a variety of passivation technologies, gate metallurgies, and mesa isolation processes.

Gallium arsenide FETs are currently fabricated in a process sequence similar to that shown in Fig. 1-1. As the figure shows, the process can use either epitaxial material or ion-implanted regions; in either case the salient

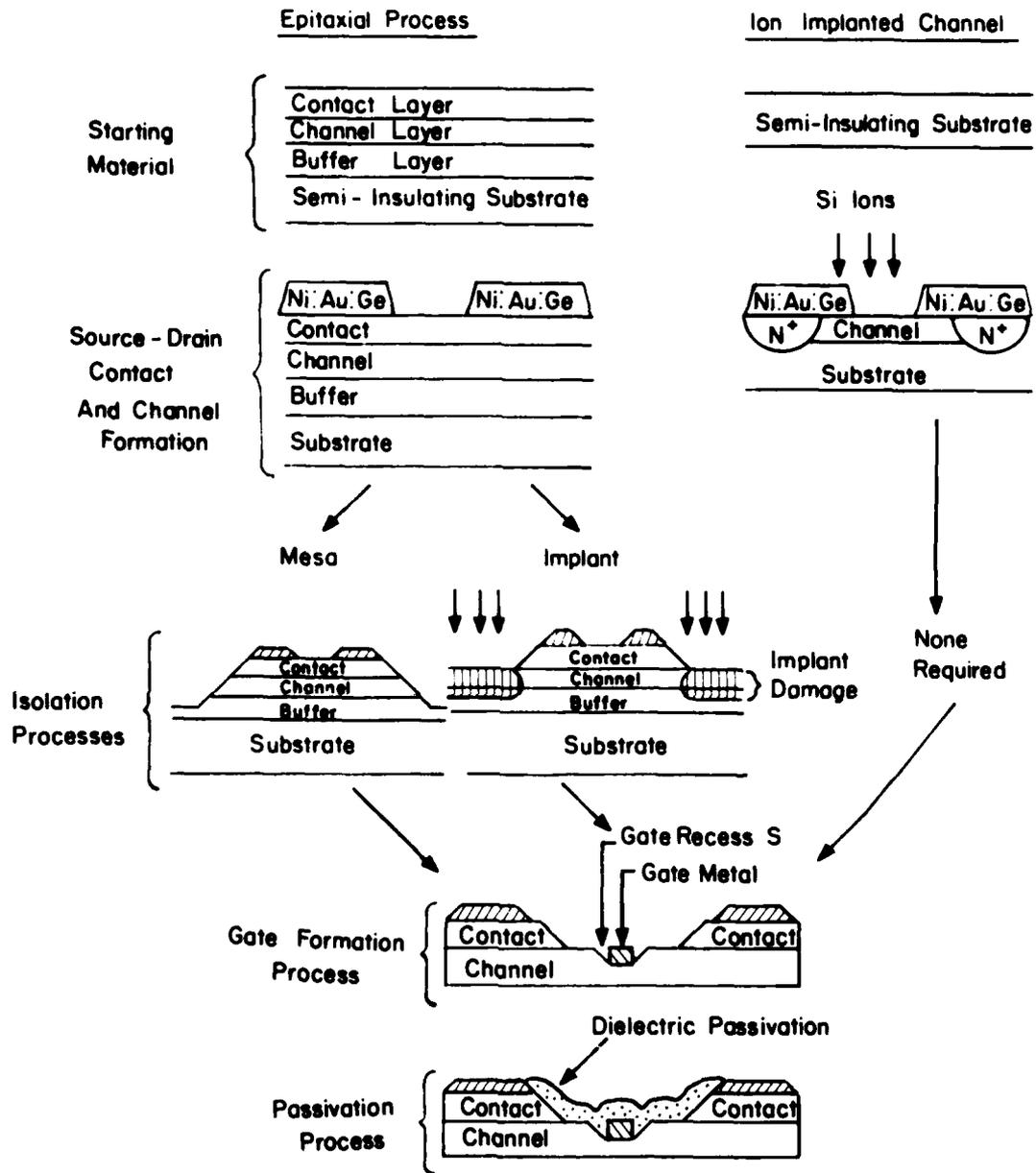


Figure 1-1. Typical FET fabrication sequence(s).

features that contribute to device noise performance are similar. Because GaAs has a high density of surface states, the channel is formed in a gate recess to place the Schottky barrier below the natural depletion layer caused by surface states. The gate recess (labelled S near the bottom of Fig. 1-1) is usually formed by an anisotropic wet chemical etch. This etch provides a characteristic level of surface states in the gate recess that act as traps. The traps cause modulation of the channel current as they are randomly populated and emptied.

To make device noise performance stable and immune to ambient conditions, it is necessary to provide some form of passivation over the surface of the channel. The current favorites among passivating layers are some form of  $\text{SiO}_2$  or  $\text{Si}_3\text{N}_4$  deposited by vacuum deposition processes. The quality of the passivation varies with deposition process and, depending on process variables and surface preparation, can give rise to varying amounts of noise. We have performed noise measurements of FETs with a variety of passivation layers.

Additional noise mechanisms can arise from the gate metal used to form the Schottky barrier. Any stress caused at the GaAs-metal surface can be expected to introduce trap states into the band structure of the GaAs. We have made a comparative evaluation of the relative noise performance of FETs whose gates are formed from various metals. All gate metals were deposited by E-beam evaporation.

The final experiments for this contract period pertain to evaluation of low-noise FETs formed with ion-implant isolation. As developmental technology brings monolithic microwave circuits closer to practice, the need for planar fabrication processes increases. One of the more popular approaches to planar FET and monolithic circuit construction employs high-energy implantation of either  $^{16}\text{O}^+$  or  $^1\text{H}^+$  ions into the inactive area of the GaAs wafer to cause lattice damage and convert the GaAs to high-resistivity material. The ion-implant-damaged region surrounds the active portions of the device. The damage introduces trap states that strongly inhibit electrical conduction through the ion-implanted region. The trap states may, however, influence the "noisiness" of the channel current by trapping channel current carriers or by releasing trapped electrons into the channel. We have studied two types of FETs: those made by the

conventional deep mesa isolation as well as by the more planar implant-isolation as shown in Fig. 1-1.

1.2.2 Specific objectives of research effort

The specific objectives of the contractual effort were to investigate the following process technologies and their effect on near-carrier noise.

A. PASSIVATION TECHNOLOGY

Dielectric

Deposition Process

- |   |                                  |
|---|----------------------------------|
| (1) Silicon Dioxide (Oxide)- $\text{SiO}_2(\text{O}_x)$ | E-beam evaporation or sputtering |
| (2) Silicon Nitride ( $\text{Si}_3\text{N}_4$ )         | Sputtered, plasma deposited      |
| (3) Polyimide   | Coated and post-baked            |

B. GATE TECHNOLOGY

Metals

Deposition Process

- |                                     |                    |
|-------------------------------------|--------------------|
| (1) Titanium-Platinum-Gold (TiPtAu) | E-beam evaporation |
| (2) Chromium-Gold (CrAu)            | E-beam evaporation |

C. ISOLATION TECHNOLOGY

- (1) Mesa Isolation
- (2) Implant Isolation ( $1\text{H}^+$ ,  $160^+$ )

#### D. CHANNEL TECHNOLOGY

- (1) Epitaxial Deposition
- (2) Implantation (silicon)

Our goal was to evaluate the relative merits of these technologies as they pertain to the baseband and near-carrier FM noise generation. In each set of experiments, half of each wafer was left unpassivated, as a control, and the remaining half passivated. Each of these half wafers, in turn, were fabricated equally with devices lacking gate electrodes, and with devices including gate electrodes.

It is obvious that many combinations could be fabricated in this manner. However, time was not available to allow study of all possible permutations. Experiments early in the program allowed us to "weed" out some combinations which would not provide us with any new information.

##### 1.2.3 Scope of experimental measurements

A variety of measurements were performed on the FETs fabricated by the technologies described above. These can be broken down into three basic categories:

- (1) DC I-V Characteristics.
- (2) Low-frequency (baseband) Noise Measurements.
- (3) Near-carrier Microwave Noise Measurements.

The first two categories, in turn, were expanded two-fold by use of temperature and optical excitation as parameters.

Based on this comprehensive set of measurements, a series of conclusions could be drawn concerning the nature of traps in GaAs FETs, their effect on

baseband noise, and their relation to the technology used in fabrication of the FETs. These conclusions constitute the major results of this contractual effort and are listed below.

### 1.3 Major Conclusions of Present Research

Our research has led to the following conclusions:

- (a) Surface electron traps contribute to hysteresis in the I-V characteristic.
- (b) Laser illumination of FETs empties traps and removes hysteresis.
- (c) Surface traps contribute to baseband noise. Under laser illumination, this noise increases because of stimulated electron transitions from traps and their return.
- (d) Baseband noise generally increases with increasing temperature because of trap emptying, but may exhibit peaks at certain temperatures. Some compensation of this increase occurs, however because of the decrease in channel current with increasing temperature.
- (e) Hysteresis in I-V characteristics vanishes at high drain bias voltages. This suggests ionization (emptying) of electron traps (surface or bulk) by hot electrons or high fields in the channel.
- (f) The basic mechanism for near-carrier FM oscillator noise is upconversion of baseband noise by depletion layer modulation of the gate capacitance (previous contract).
- (g) Not all of baseband noise manifests itself as depletion layer modulation and FM noise.
- (h) Baseband and near-carrier FM noise do not appear to be a function of gate technology.

(i) FM noise may be degraded by the type of surface passivation used.  $\text{Si}_3\text{N}_4$  and polyimide do not degrade FM noise performance. However,  $\text{SiO}_x$  increases noise by about 10 dB.

(j) Oxygen implant isolation does not degrade FM noise performance.

(k) The FM noise level for a device with an implanted channel was between 10 and 20 dB higher than for epitaxial channel devices. This indicates a high level of bulk traps in implanted channel devices.

(l) The best FM oscillator carrier-to-noise ratio obtained with epitaxial channel FETs during this contract exceeded any heretofore reported results by over 20 dB.

The findings in items (h)-(l) are considered major results of this research. These results have important implications in regard to the choice of a preferred device technology.

Before a detailed discussion of the experimental results, a brief review will be given of noise theory of oscillators as it pertains to the present work.

## 2.0 REVIEW OF OSCILLATOR NOISE THEORY

### 2.1 Introduction

#### 2.1.1 Nonlinear model of FET oscillator

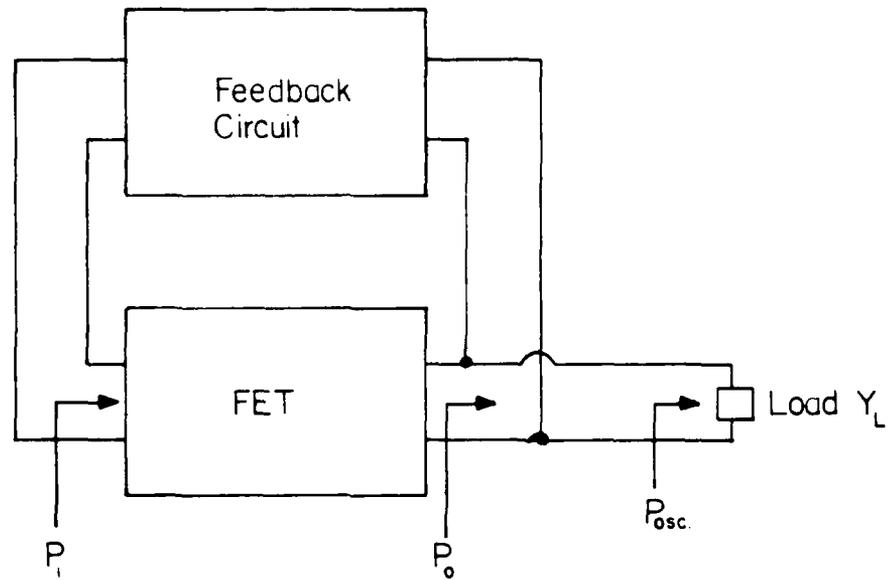
All existing theories of electronic oscillators, whether they be one-port such as avalanche diodes, or two-port devices with feedback, such as transistors or tube oscillators, reduce the problem of analysis to that of a one-port admittance (or impedance) with a negative real part.<sup>6-8</sup> The general treatment of a two-port oscillator as a nonlinear transducer is a difficult one, and has not been solved.<sup>9</sup>

The FET, with its associated feedback network, can be treated as a "black box" which presents a signal-dependent admittance with a negative real part to the load. This representation is shown in Fig. 2-1(a). The reduced, one-port equivalent circuit, looking from the load terminals, is illustrated in Fig. 2-1(b). Shown is a nonlinear device admittance  $Y$ , a function of signal amplitude  $A$  and frequency  $\omega$  with a negative real part in shunt with the frequency-dependent load  $Y_L$  and a conductance  $G_c$  representing circuit and feedback losses.

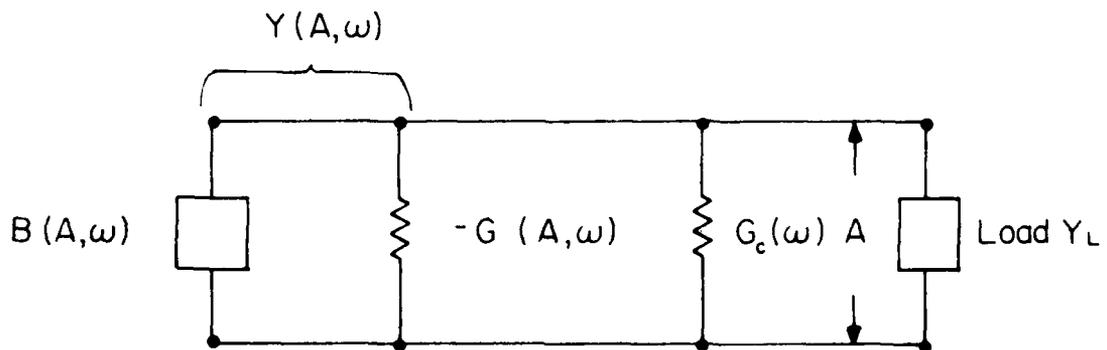
For stable oscillations, the negative real part of the device admittance must be a decreasing function of the signal amplitude  $A$ , where  $A$  may represent some current or voltage signal. (In the representation of Fig. 2-1,  $A$  represents the node voltage.) A necessary condition for oscillation is that

$$G_c(\omega) + Y(A_0, \omega_0) + Y_L(\omega_0) = 0 \quad (1)$$

at some frequency  $\omega = \omega_0$ , where  $A = A_0$  is the resulting oscillation amplitude. This condition establishes the frequency and amplitude of oscillation for any prescribed load. The power delivered to the load will be maximum for some "optimum" load.



(a) Two-Port FET Oscillator with feedback



(b) One-Port Representation of FET Oscillator with losses  $G_c$

Figure 2-1. Large-Signal model of FET oscillator.

For single-state oscillators (one oscillation amplitude and frequency for any prescribed load), it is usually possible to approximate the nonlinear dependence of the device admittance as a power series of the oscillation amplitude. The simplest representation which leads to stable oscillations is the so-called van der Pol approximation,<sup>6</sup>

$$-G(A, \omega) = \alpha A - \beta A^3 \quad (2)$$

where  $G$  is considered frequency-independent over a narrow band and  $\alpha$  and  $\beta$  are properties of the device. Most existing oscillator noise theories are based on this approximation. This cubic approximation also can be applied to the FET oscillator because the oscillator can be considered as a power amplifier in which a portion of the output is fed back to the input to produce a negative input conductance which cancels the input circuit losses and loading, and, hence, leads to sustained oscillations.

The cubic approximation, though convenient analytically, is oversimplified and also ignores any nonlinear reactive elements in the active device. Neither of these approximations is satisfied for a microwave FET. We have developed in the previous contract a nonlinear model of the FET which overcomes these restrictions and which represents the nonlinear properties of the FET not only at microwave frequencies but also in the dc condition. This model agrees well with dc and rf measurements.

The predominant sources of nonlinearity in the FET, relevant to oscillator analysis, are the transconductance  $g_m$  and the source-gate capacitance  $C_{sg}$ . Thus, in the representation of Fig. 2-1  $g_m$  contributes to  $-G(A, \omega)$  and  $C_{sg}$  contributes to  $B(A, \omega)$ .

## 2.1.2 Noise model

### 2.1.2.1 Background noise

There are two general categories of noise mechanisms in an FET: intrinsic sources, i.e., noise associated with the FET operation itself, and extrinsic noise, i.e., noise generated by sources not essential to FET operation.

The intrinsic sources are thermal noise in the channel and diffusion noise generated at high channel fields in the velocity saturated zone. These noise sources produce a flat (white) spectrum. Avalanche noise, possibly generated at very high drain voltages, also produces white noise. Noise associated with a parasitic resistance, one of the extrinsic noise sources, is also flat.

These white noise sources, because they produce spectra which overlap the carrier frequency, are called background sources. This noise interacts directly with the carrier to produce AM and FM noise sidebands. No frequency conversion of the noise spectra takes place. That is to say, the background noise sources, collectively considered as a "small signal", can be represented as a voltage or current source (in the case of Fig. 2-1, a current source) driving the already established large-signal equivalent circuit. This is the customary way of treating background noise in oscillators.<sup>10-12</sup> Figure 2-2 represents the equivalent circuit for the background noise. The noise is represented by the current generator  $i_b$ .

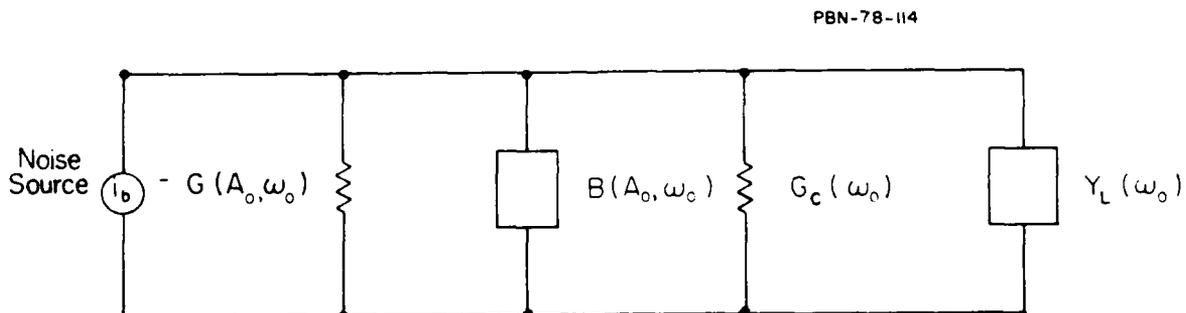


Figure 2-2. Noise equivalent circuit for FET oscillator.

The major task in handling background noise in an FET oscillator is to obtain a suitable representation for the noise source amplitude  $i_b$  in terms of the physical white noise sources. As a starting point, one may use the background noise model for the FET amplifier, such as developed at this laboratory.<sup>1</sup> Then by taking into account feedback in the oscillator, and averaging the noise sources over an oscillator cycle, if necessary, the background noise contribution can be computed in the traditional way. Knowing the background noise contribution, one can determine its contribution to the measured oscillator noise or vice versa.

For example, if the spectral density of the available noise power associated with the background current noise source is denoted by  $N_b$ , then the rms frequency deviation  $\Delta f_{\text{rms}}$ , arising from a band B of this white noise, is given by<sup>10-12</sup>

$$\Delta f_{\text{rms}} = \frac{f_o}{Q_L} \sqrt{\frac{N_b B}{P_o}} \quad (3a)$$

where  $f_o$  is the oscillation frequency,  $Q_L$  is the loaded Q of the oscillator circuit, and  $P_o$  the carrier or oscillator power. The corresponding (double-sideband) noise/carrier ratio at the frequency offset  $f_m$  is<sup>11-13</sup>

$$\left(\frac{N}{C}\right)_{\text{FM}} = \frac{N_b B}{P_o} \frac{1}{(f_m Q_L / f_o)^2} \quad (f_m > 0) \quad (3b)$$

This relationship ties in the measured  $\Delta f_{\text{rms}}$  (associated with white noise) to the equivalent noise source power  $N_b$ , which in turn is linked with the physical sources of noise.

Likewise the AM noise spectra arising from background sources can be related to the double sideband noise-to-carrier ratio by<sup>11-13</sup>

$$\left(\frac{N}{C}\right)_{\text{AM}} = \frac{N_b B}{P_o} \frac{1}{1+(f_m Q_L / f_o)^2} \quad (4)$$

Background noise in an FET oscillator is only observable far from the carrier, around 10 MHz removed. It is low compared with other oscillators, such as avalanche and Gunn diodes. It is dominated, near the carrier, by  $1/f$ -like noise, which is to be discussed next.

#### 2.1.2.2 Baseband noise

We turn now to the portion of extrinsic noise which we called "excess noise," and with which we are concerned in this research. We include in this category all sources of noise associated with material defects or introduced by other factors in the device technology. These noise contributions usually can be correlated with traps (electron and/or hole) which are either within the semiconductor, at the interface between the active layer and the substrate, or at the exposed surface (between electrodes or at the electrode-semiconductor interfaces). This trap-related noise originates at baseband and is usually of the form

$$N_e = \frac{AI^\alpha}{f^\beta} \quad (5)$$

over a finite frequency range,<sup>14-17</sup> where  $I$  is the bias current,  $\alpha \sim 2$ , and  $\beta \sim 1-2$ , depending on the distribution and nature of the traps. For example, for a single-level trap distributed uniformly throughout the bulk, one finds  $\alpha = 2$ ,  $\beta = 2$ , i.e., a baseband contribution falling off with frequency as  $1/\omega^2$  and quadratically dependent on bias current. On the other hand, for a set of traps with a uniform distribution of trapping times, Van der Ziel<sup>16</sup> shows that  $\beta = 1$  leads to a  $1/f$  spectrum over a finite frequency band. A  $1/f$  spectrum can also be produced by a continuum of states with a uniform distribution of energy levels. The situation often can be approximated by surface states.

Baseband noise can manifest itself as an rf spectrum only by a modulation or frequency up-conversion or "mixing" process involving the nonlinearity of the device. Therefore, oscillator noise contributed by upconverted baseband

noise is often called "modulation noise." Since the frequencies of the noise components are at base band (and hence much lower than the large-signal carrier frequency), baseband noise manifests itself as a slow, random variation of the nonlinear elements of the oscillator--in the case of Fig. 2-1(b), the real and imaginary parts of the device admittance.

This phenomenological treatment of the baseband  $1/f$  noise, as it pertains to the near-carrier noise spectra of oscillators, is quite successful, and amenable to analytic treatment.<sup>12-13</sup> Thus if  $\langle (\Delta Y)^2 \rangle$  is the mean square fluctuation of the device admittance produced by modulation noise,\* an "equivalent" modulation noise current source  $i_m$  of mean square value  $|A_o|^2 \langle (\Delta Y)^2 \rangle$  can be added in shunt with the background noise generator  $i_b$ , where  $A_o$  is the amplitude of the carrier.<sup>12</sup>

In the special case where the fluctuations in  $-G$  and  $B$  are uncorrelated, the modulation noise contribution can be added very simply to the background noise contribution in Eqs. (3) and (4). In this case the fluctuation in  $G$  leads to AM noise and the fluctuation in  $B$  leads to FM noise. For example, Eq. (3a) becomes

$$\Delta f_{\text{rms}} = \frac{f_o}{Q_L} \sqrt{\frac{(N_b + N_{mb})B}{P_o}} \quad (6)$$

and Eq. (4) becomes

$$\left(\frac{N}{C}\right)_{\text{AM}} = \frac{(N_b + N_{mg})B}{P_o} \frac{1}{1 + (f_m Q_L / f_o)^2} \quad (7)$$

where  $N_{mg}$  is the available noise power associated with the noise modulation of  $-G$  and  $N_{mb}$  is the available noise power associated with the modulation of  $B$ . Both  $N_{mg}$  and  $N_{mb}$  will exhibit a spectrum corresponding to the form given by Eq. (5).

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\*The symbol  $\langle \rangle$  represents a statistical average.

Equations (6) and (7) are mathematical representations of the background noise and baseband noise mechanisms as power spectral densities,  $N_b$ ,  $N_{mb}$ ,  $N_{mg}$ . As such they are useful in that they allow one to compare these noise contributions to some reference, such as thermal source noise,  $kT$ . On the other hand, to relate the noise contributions to some specific physical source, one must identify the mechanism by which the noise is generated, and explain how it modulates the carrier.

For example, take the case of  $1/f$  noise. To show how this manifests itself as upconverted AM and FM noise, we follow a simple model of Scherer.<sup>18</sup> Let  $P$  be some low-frequency device parameter whose fluctuation is suspected of producing near-carrier noise. For example,  $P$  may represent drain bias current, gate bias, gate source capacitance, etc. Suppose, in general, that both the oscillator power output and carrier frequency are affected. If  $\langle (\Delta P)^2 \rangle$  represents the mean-square value of the statistical fluctuation of the parameter measured at baseband, in a bandwidth  $B$  at some baseband frequency  $f_m$  (by the low-frequency noise analyzer), then the corresponding AM and FM noise contributions to the near-carrier spectrum displaced by a frequency  $f_m$  from the carrier are, respectively,

$$\left(\frac{N}{C}\right)_{AM} = \frac{|S_{ap}|^2}{4P_c^2} \langle (\Delta P)^2 \rangle, \quad (8)$$

$$\Delta f_{rms}^2 = |S_{fp}|^2 \langle (\Delta P)^2 \rangle \quad (9)$$

where  $S_{ap}$  and  $S_{fp}$  are amplitude and frequency-sensitivity factors for the parameter  $P$  given by

$$S_{ap} = \frac{\partial P_c}{\partial P} \quad , \quad (10a)$$

$$S_{fp} = \frac{\partial f_o}{\partial P} \quad , \quad (10b)$$

As an example of this modulation process, consider the case of surface states or bulk states under the gate electrode. A fluctuation in the occupancy of these states will result in a fluctuation of the depletion layer depth, i.e., the gate capacitance. A fluctuation in the gate capacitance causes a fluctuation in the imaginary part of the device susceptance, hence in frequency, as per Eq. (9). The experimental results obtained in the previous contract suggest that a fluctuation process, similar to this, can indeed lead to the FM noise measured in our experiments. We shall invoke this mechanism of noise modulation to explain our present results. We must add, however, that not all baseband noise manifests itself as depletion layer modulation. Noise generated outside of the gate-channel region, is an example. More will be said of this later.

### 3.0 EXPERIMENTAL APPROACH

#### 3.1 Introduction

Baseband and near-carrier noise measurements were made on a 500 micron periphery FET, of a design normally used for low-noise purposes. The noise was measured on devices processed in a variety of passivation, isolation, and metallization techniques.

Baseband noise was measured as a function of temperature, with and without illumination by a laser source. Baseband noise for non-oscillating devices was measured in the frequency range of 100 Hz to 200 kHz.

Near-carrier noise performance was obtained for devices operating in a microstrip oscillator configuration near 9 to 10 GHz. RF noise spectra were obtained in the frequency band 10 kHz to 10 MHz from the carrier at room temperature.

In addition to noise measurements, I-V plots of drain current as a function of drain bias and gate bias were taken on an X-Y recorder in the conventional manner.\* These measurements were taken for different temperatures, with and without laser illumination of the device.

#### 3.2 Description of Experimental Test Set-Ups

##### 3.2.1 Baseband noise measurements

It was mentioned earlier that baseband noise measurements were made as a function of baseband frequency and temperature, under conditions when the source-drain region was either exposed to controlled optical excitation or kept dark.

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\*Hewlett-Packard X-Y Recorder Model 7034A.

The temperature and optical excitation experiments were facilitated by measurement of the baseband noise in a vacuum chamber which included a sapphire optical window. The chamber was evacuated; the device and its stage were elevated to 100°C for a 3-hour bake-out. (Previous experiments had shown that this bakeout schedule was sufficient to guarantee repeatable results during temperature measurements.) Measurements of the baseband noise in the source-drain current were then obtained, with and without laser illumination, as a function of temperature while the device was under a vacuum.

Temperature cycling of the devices, for the most part, was limited to the range  $\pm 100^\circ\text{C}$ , though some of the measurements taken early during the reporting period were over a larger range, as will be noted later. The high limit was established to not exceed the processing temperatures used in some of the device variations investigated. The low limit resulted from observed stress fractures in some of the device structures at  $-150^\circ\text{C}$  and below. Either continuous temperature variations were employed, where temperature was the independent variable, or temperature steps of  $25^\circ\text{C}$  were used when temperature was a parameter.

The laser diode utilized for illumination studies was an infrared solid state device (GaAlAs) made by Laser Diode Laboratories.\* It was biased with a constant-current source to produce 0.5 mW of radiation at 8080 Å. Mounted on an X-Y-Z platform external to the vacuum chamber, it could easily be adjusted to place its narrow beam on the gate area of the FET structure being studied.

The baseband noise was measured with a baseband analyzer\*\* as a noise voltage drop across a resistor in the drain circuit of a non-oscillating FET. This is shown in Fig. 3-1. The noise voltage was converted to a drain current fluctuation. Initially, the sensing resistor  $R_L$  was immersed in liquid nitrogen to reduce its own thermal noise contribution when measurements far from the carrier were made. However, this precaution was unnecessary in the near-carrier

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\*Laser Diode Laboratories Model LCW-30.

\*\*Hewlett-Packard Spectrum Noise Analyzer Series 8500.

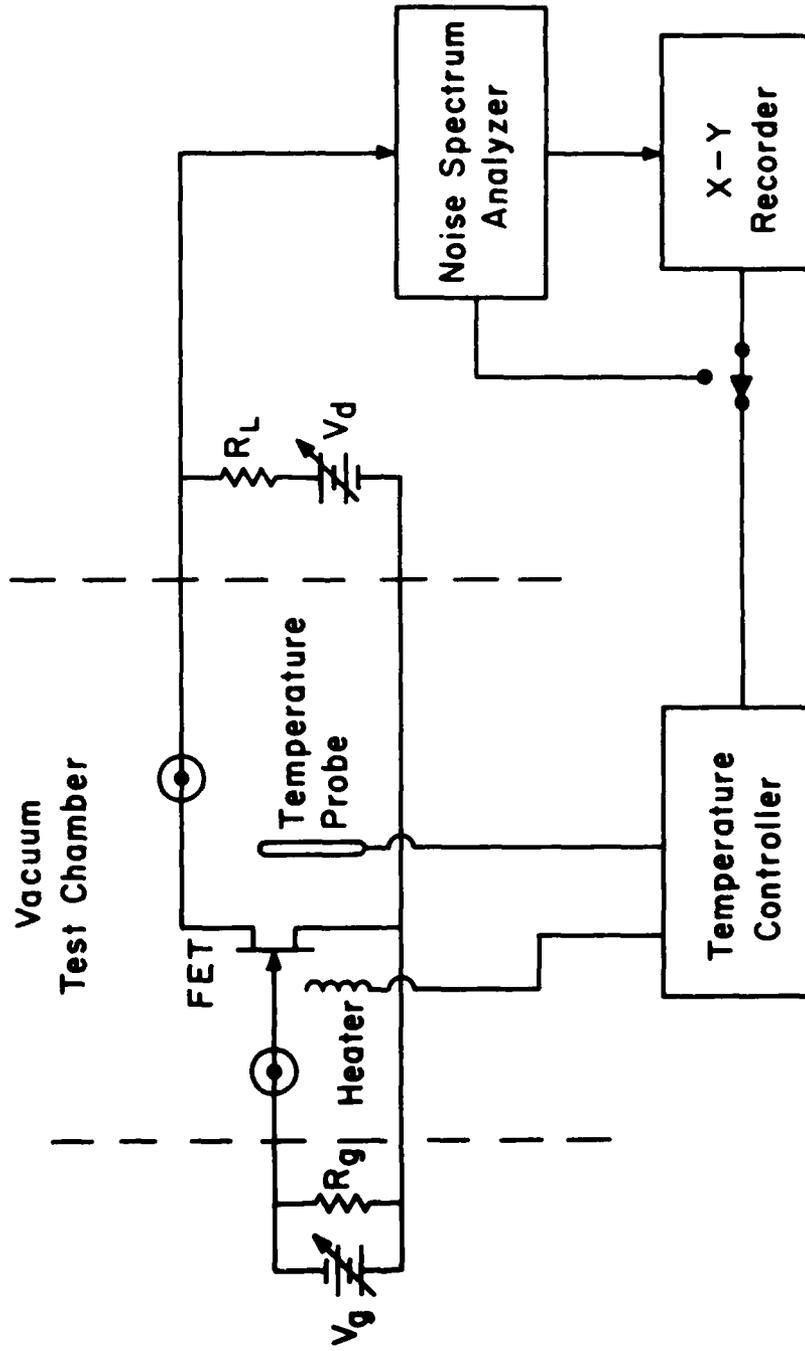


Figure 3-1. Test set-up for measurement of baseband noise as a function of frequency and temperature.

1/f range, where the device noise was high. Both battery operation and well-filtered AC power supply operation were compared, with no noticeable difference in noise spectra. Of course, extreme care was taken to shield the device from outside noise pickup.

The noise analyzer "window" bandwidths used varied from 10 Hz through 3 kHz. At all times the minimum useable bandwidth was used to preserve accuracy of measurement. However, in the reduction of the data for graphs, all of the data were mathematically normalized to a 1 Hz bandwidth to provide a common basis for comparing noise levels. This normalization procedure also was followed for the near-carrier oscillator FM noise measurements.

A detailed block diagram for obtaining of the baseband noise measurements as a function of frequency, with temperature held constant, or conversely, as a function of temperature with frequency held constant is shown in Fig. 3-2. This diagram illustrates specifically the method by which the noise at a single frequency is measured as the temperature is varied. The arrangement for obtaining swept frequency data at a constant temperature is very similar. The device under test (DUT) in its fixture was thermally bonded to a cold finger, which also incorporated an integral heater; electrical connections were made through vacuum feed-throughs to the fixture. The assembly was then evacuated. Liquid nitrogen in the dewar was used as the coolant.

The power available to the heater was adjusted to provide a nearly constant rate of rise of the temperature of the assembly - approximately one-two degrees per minute; the temperature controller, acting only in the read-out mode, provided a temperature analog voltage to the X-Y recorder. The spectrum analyzer operated as a fixed-frequency noise receiver and also provided a noise-power analog voltage to the X-Y recorder.

Swept frequency data at a constant temperature was obtained by allowing the temperature controller to hold the temperature while the spectrum analyzer swept the frequency range of interest. The analyzer provided both noise-power and frequency analog voltages to the recorder. The system allowed temperature

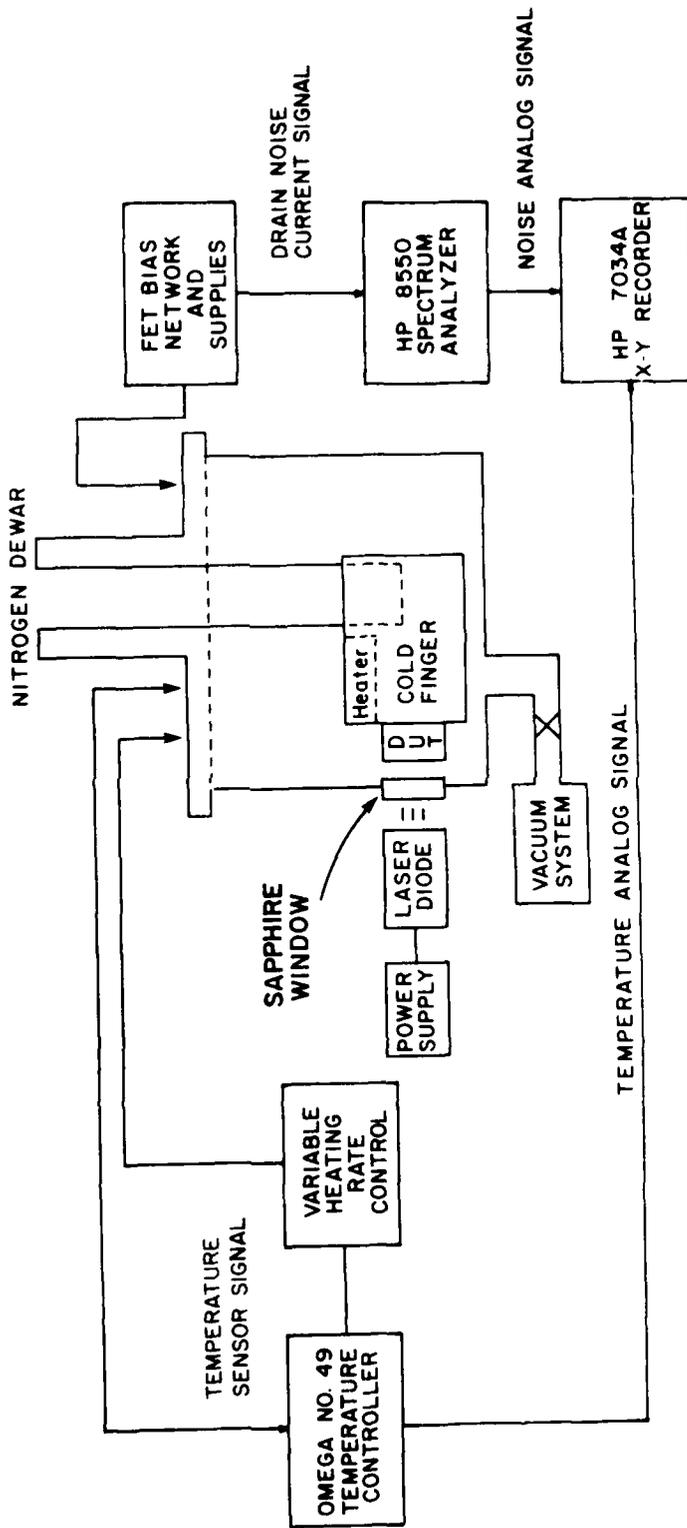


Figure 3-2. Complete baseband noise measurement block diagram.

measurements from  $T = -100^{\circ}\text{C}$  to well above room temperature. The test data was normalized to a 1-Hz bandwidth and replotted against linear temperature, inverse temperature, or baseband frequency, as appropriate.

The diagram also shows how the device under test was measured under conditions of laser illumination through a sapphire window in the sidewall of the evacuated dewar. Figure 3-3 is a photograph of a portion of the noise set-up illustrating the temperature controller and evacuated dewar. The complete optical setup is shown in Fig. 3-4.

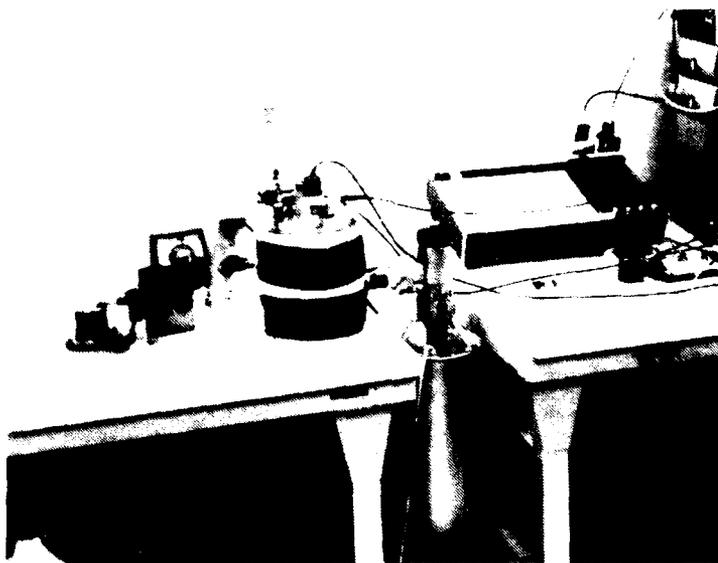


Figure 3-3. Portion of test set-up showing vacuum test chamber.

### 3.2.2 Microwave noise measurements

#### 3.2.2.1 The measurement system

Microwave noise measurements consisted of near-carrier FM noise measurements taken on an oscillating FET. For these measurements the direct detection scheme was used to eliminate any problems associated with L.O.

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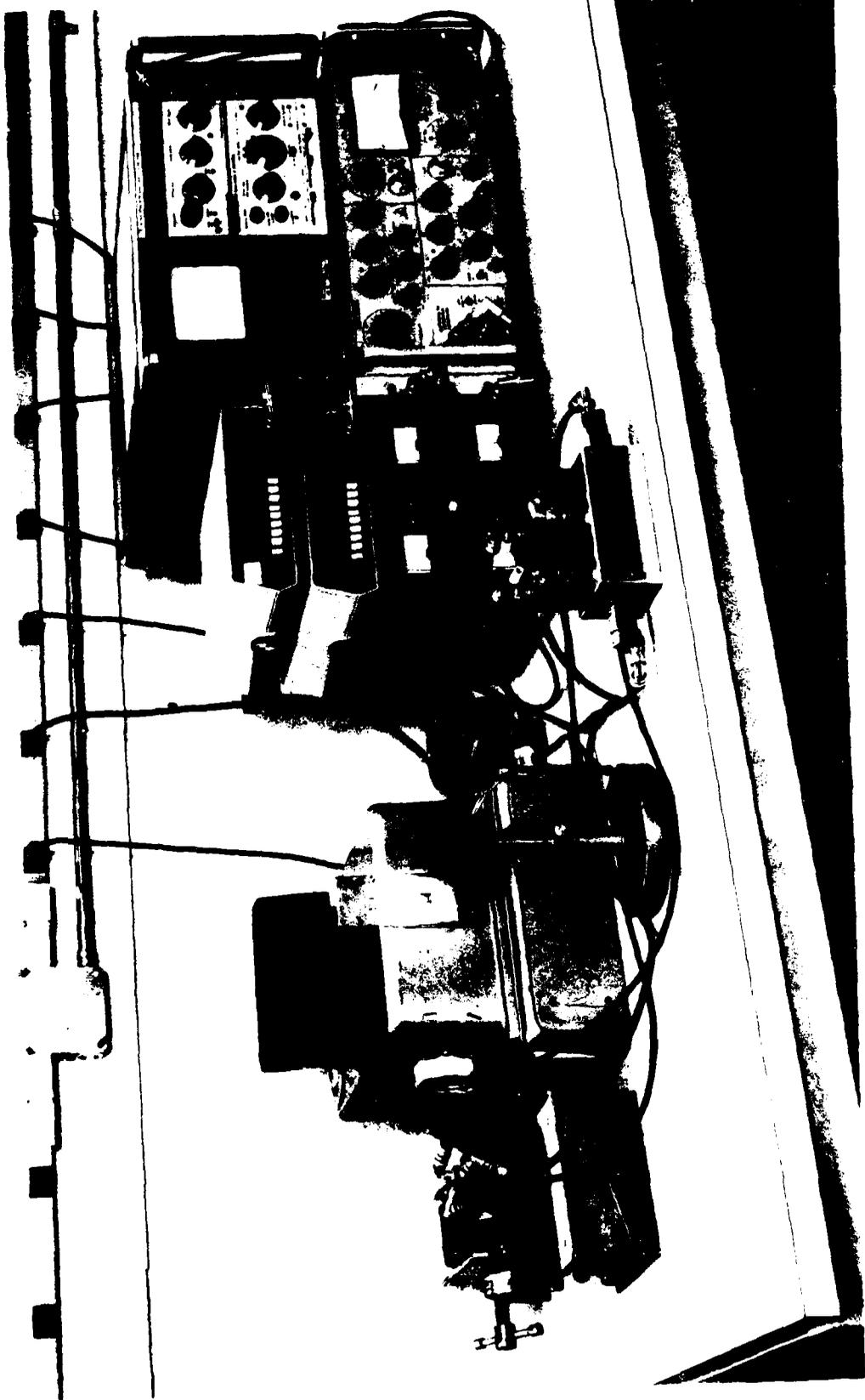


Figure 3-4. Optical set-up.

frequency jitter and AM noise. This is a serious problem with heterodyne techniques, since the near-carrier noise in the L.O. sets the limiting sensitivity of the system for measurement of noise near the carrier frequency.

Satisfactory microwave noise analyzers (as contrasted to spectrum analyzers) were not commercially available, therefore, a versatile, ultrasensitive direct detection system was designed and built for our laboratory by the Electronic Equipment Group of Raytheon's Microwave and Power Tube Division. This system incorporates features which were designed with near-carrier FET oscillator noise measurements in mind. The system is capable of measuring noise from 50 cycles from the carrier to as far as 10 MHz from the carrier in two, switchable bands. A simplified block diagram is shown in Fig. 3-5. This system is tunable from 8.5 to 10.5 GHz. Figure 3-6 is a photograph of the noise analyzer.

The FM demodulator (discriminator) is a frequency-sensitive microwave bridge. Unlike other noise measurement techniques employing carrier suppression, this system retains the carrier power. This not only results in lower rf input requirements, but makes the analyzer simpler to operate. Only two adjustments, the rf short and the microwave cavity, are used to balance the discriminator. The analyzer may be battery-operated to eliminate power-supply noise modulation.

The detected output is passed to a baseband analyzer (not shown)\*. All noise spectra can be traced on an X-Y recorder for a permanent record. Although the system is also capable of making AM noise measurements, none were taken during the reporting period as they were deemed unnecessary.

A detailed block diagram of the microwave noise measurements system is illustrated in Fig. 3-7.

#### 3.2.2.2 FET oscillator circuit configuration

A common-gate oscillator was designed for X-band noise studies. The circuit utilizes an inductance in the gate-ground arm for feedback (see

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\*Same analyzer as used in baseband measurements. See footnote, p. 20.

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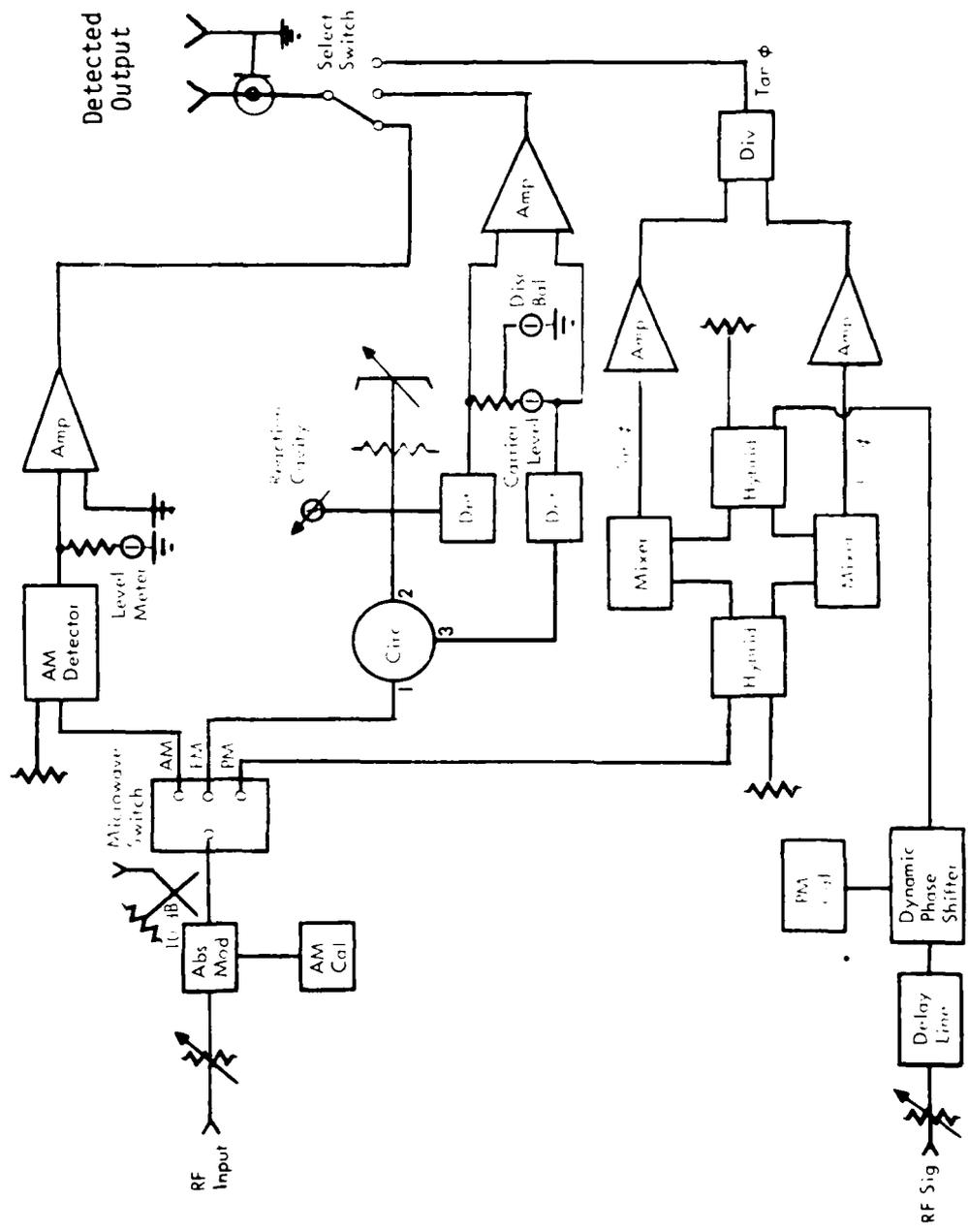


Figure 3-5. Block diagram of noise analyzer.

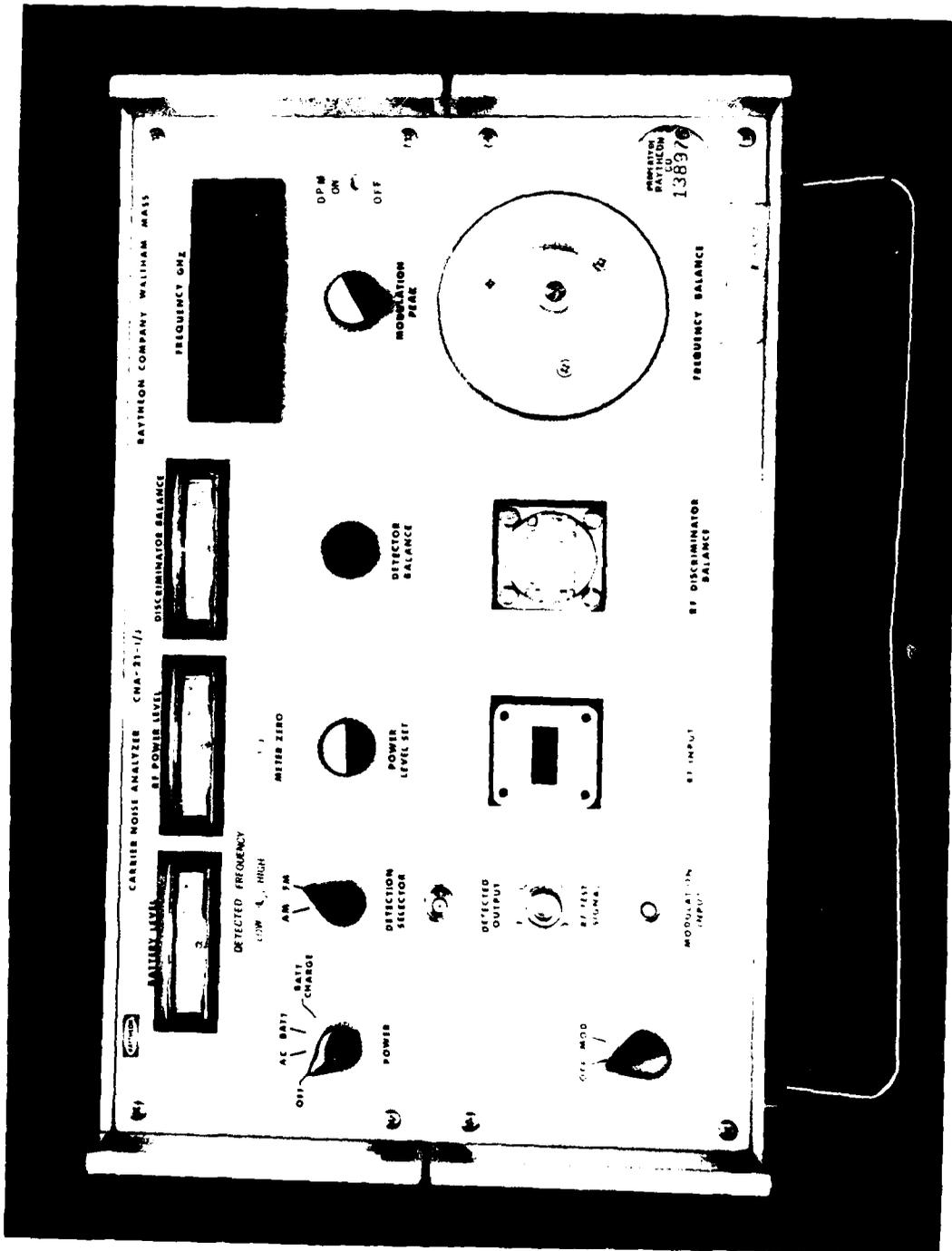


Figure 3-6. Noise analyzer.

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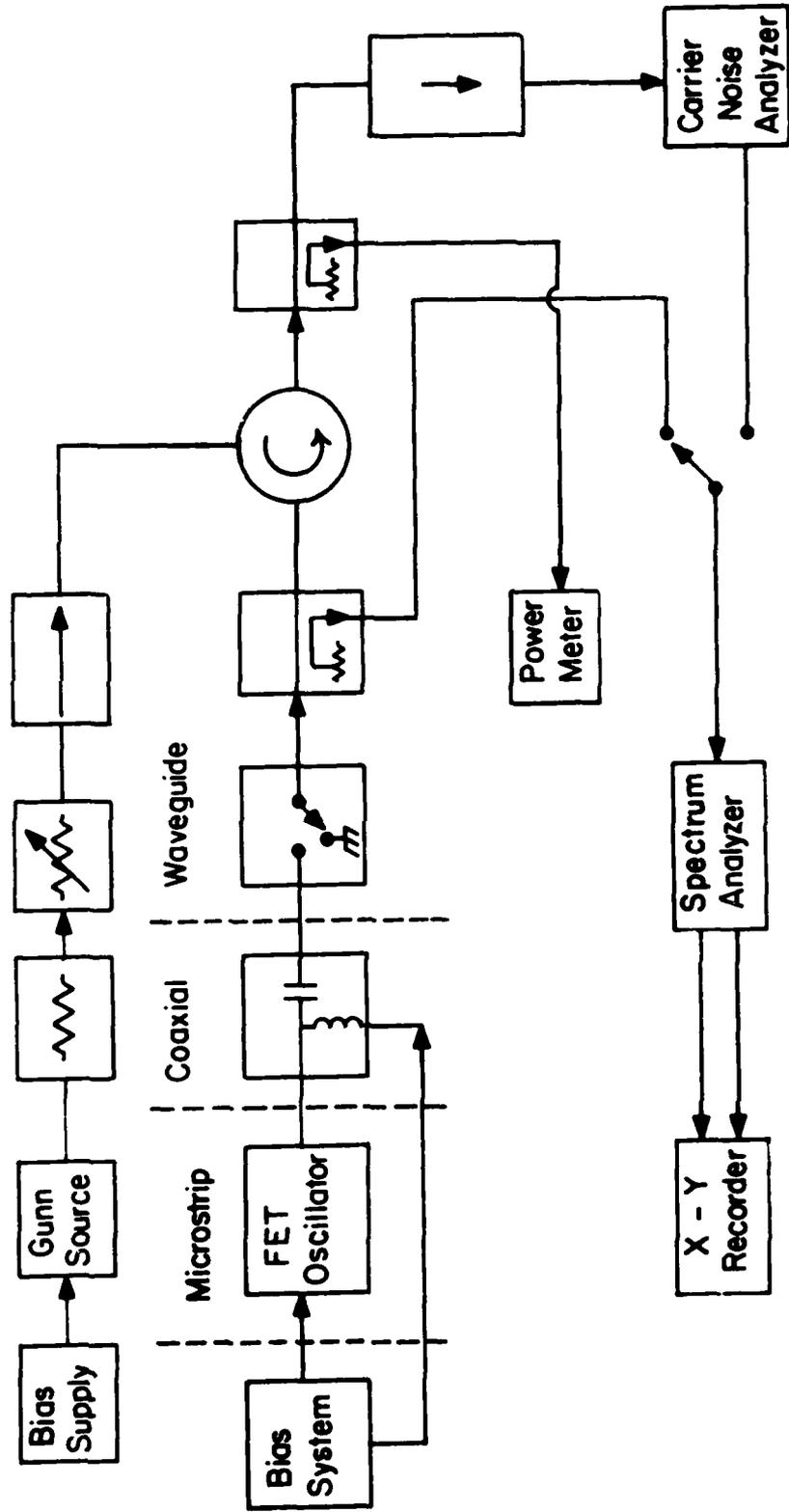


Figure 3-7. Complete RF noise measurement block diagram.

Fig. 3-8). The circuit was designed to operate with a load approximating that for maximum power output. The inductance was in the form of a 1-mil diameter wire which could be "tweaked" for fine tuning.

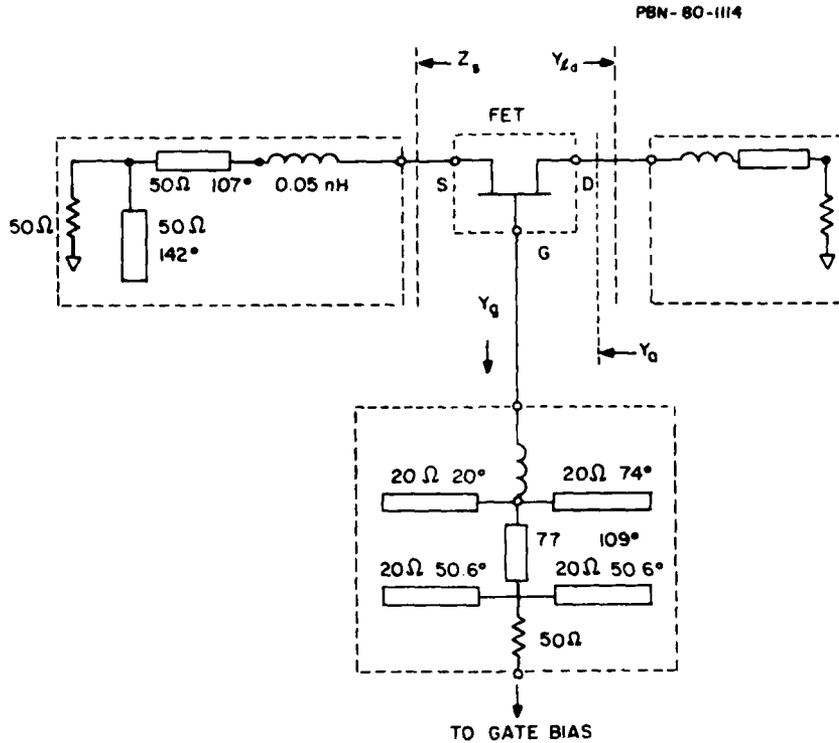


Figure 3-8. Schematic of oscillator circuit.

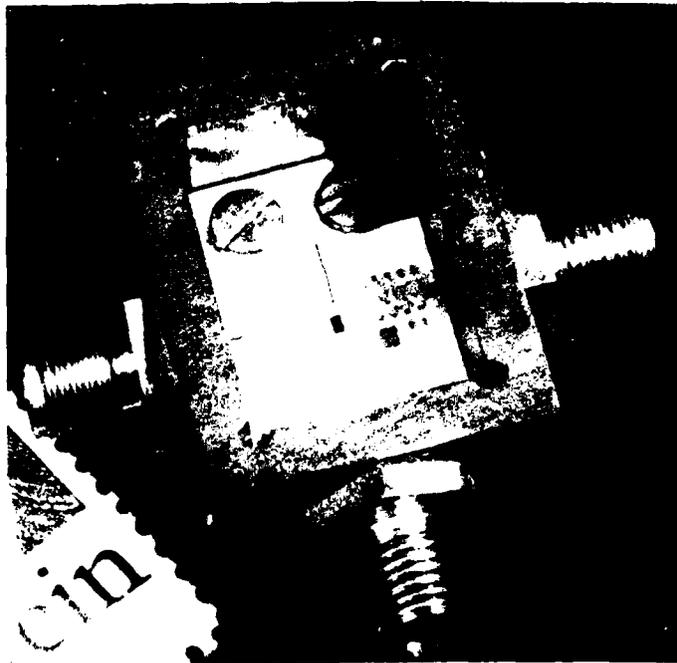
The oscillator circuit was printed on an alumina substrate. In addition to the rf output port connected to the drain, a coaxial input port also was used to connect to the source to allow injection of a synchronizing signal and for external cavity tuning and/or stabilization, when desired. With the help of silver paste, the oscillator frequency and power were fine-tuned by appropriate connection of source stubs and drain capacitive tabs on the substrate. A photograph of the circuit is shown in Fig. 3-9(a). The circuit mounted in its holder appears in Fig. 3-9(b).

CN-24-624



(a) Oscillator circuit on alumina substrate.

CN-24-625



(b) Oscillator circuit mounted in test jig.

Figure 3-9. Oscillator circuit.

The bias scheme that evolved permitted the supplies, digital multimeters, oscilloscope, and spectrum analyzer to be interchanged. Bias tees readily pass signals in the baseband frequency range. All rf ports may be used for modulation signal injection at baseband frequencies or for monitoring noise in this frequency range. Figure 3-10 illustrates the connection of the bias supplies to the oscillator through bias tees. Figure 3-11 is a photograph of the oscillator test set-up.

### 3.3 Cases Studied

#### 3.3.1 Technology categories

We mentioned earlier that a variety of process variations were made in the fabrication of the FETs to allow one to examine the relation between excess noise and processing technology.

We have tried, in most cases, to maintain a "control", that is, a portion of the wafer which did not pass through the processing step being examined. In this way, a meaningful comparison could be made. For example, in the study of the effect of gate technology one-half of the wafer contained gateless devices. This half experienced all processing steps of the remaining half, except gate deposition. Similarly, in the study of passivation, one half of the wafer remained unpassivated.

When isolation technology was being examined, however, we chose to use an entire wafer either for mesa isolation, or for oxygen or proton implant isolation. The same was done when implanted channels were compared with epitaxial channels. Despite this reduction in possible categories, there were more cases to examine than time allowed.

If we divide our cases into the two categories pertaining to channel formation, i.e., epitaxial and implanted channel, then Fig. 3-12 illustrates these categories and their subdivisions. Thus, for example, in the case of epitaxial

FET OSCILLATOR

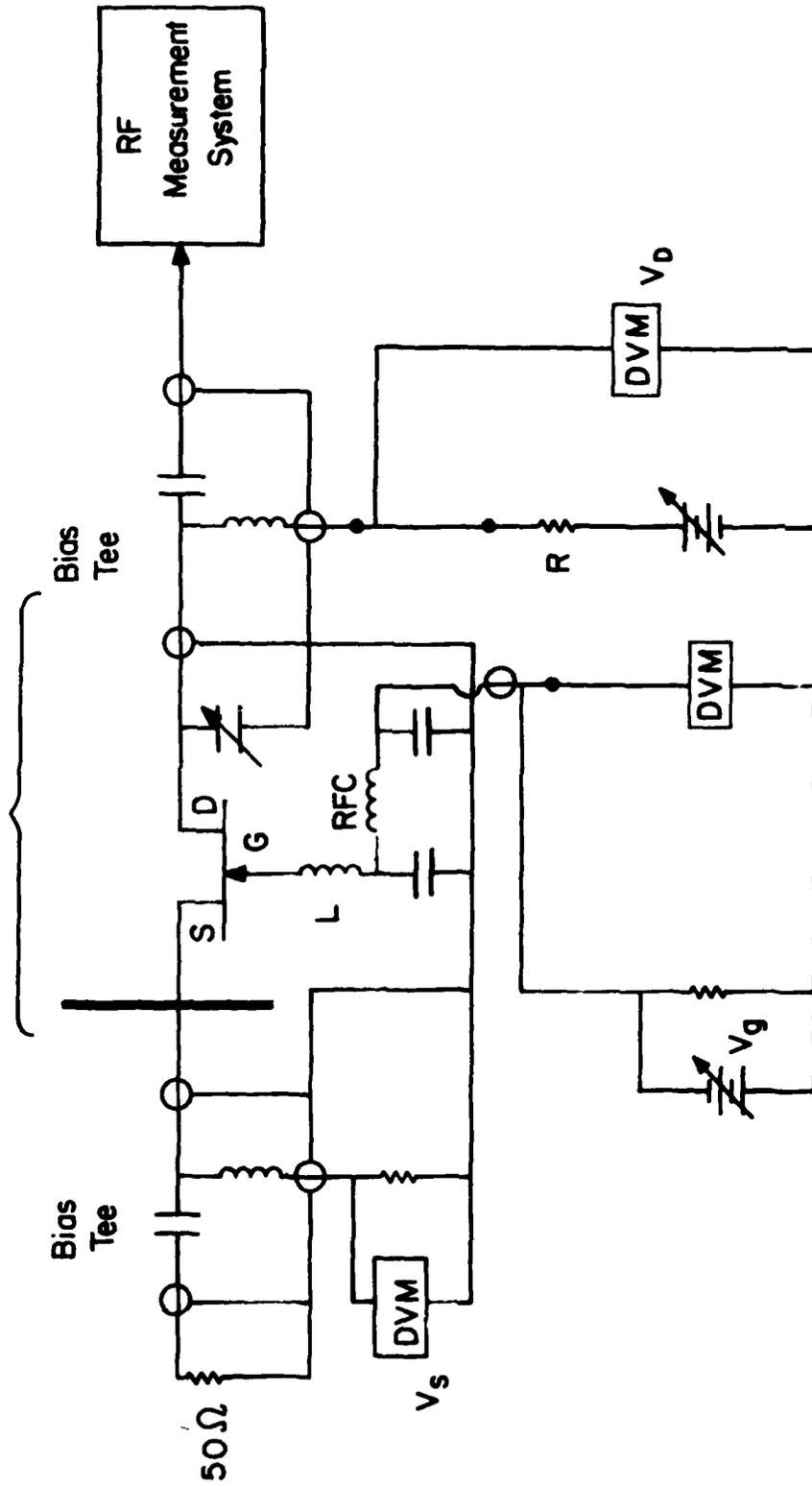


Figure 3-10. Schematic diagram of oscillator noise measurement set-up showing method of biasing the FET.

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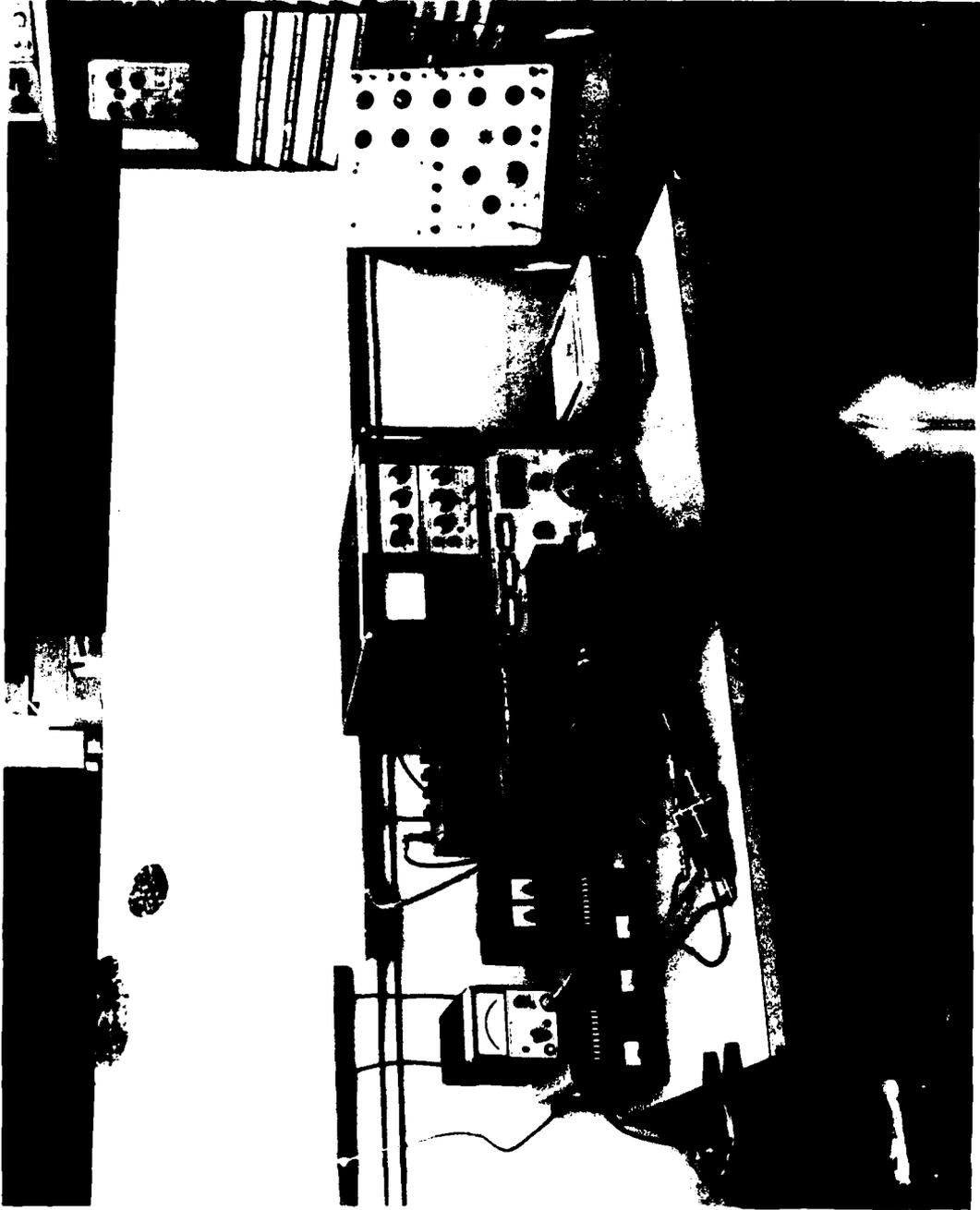


Figure 3-11. Photograph of oscillator test system.

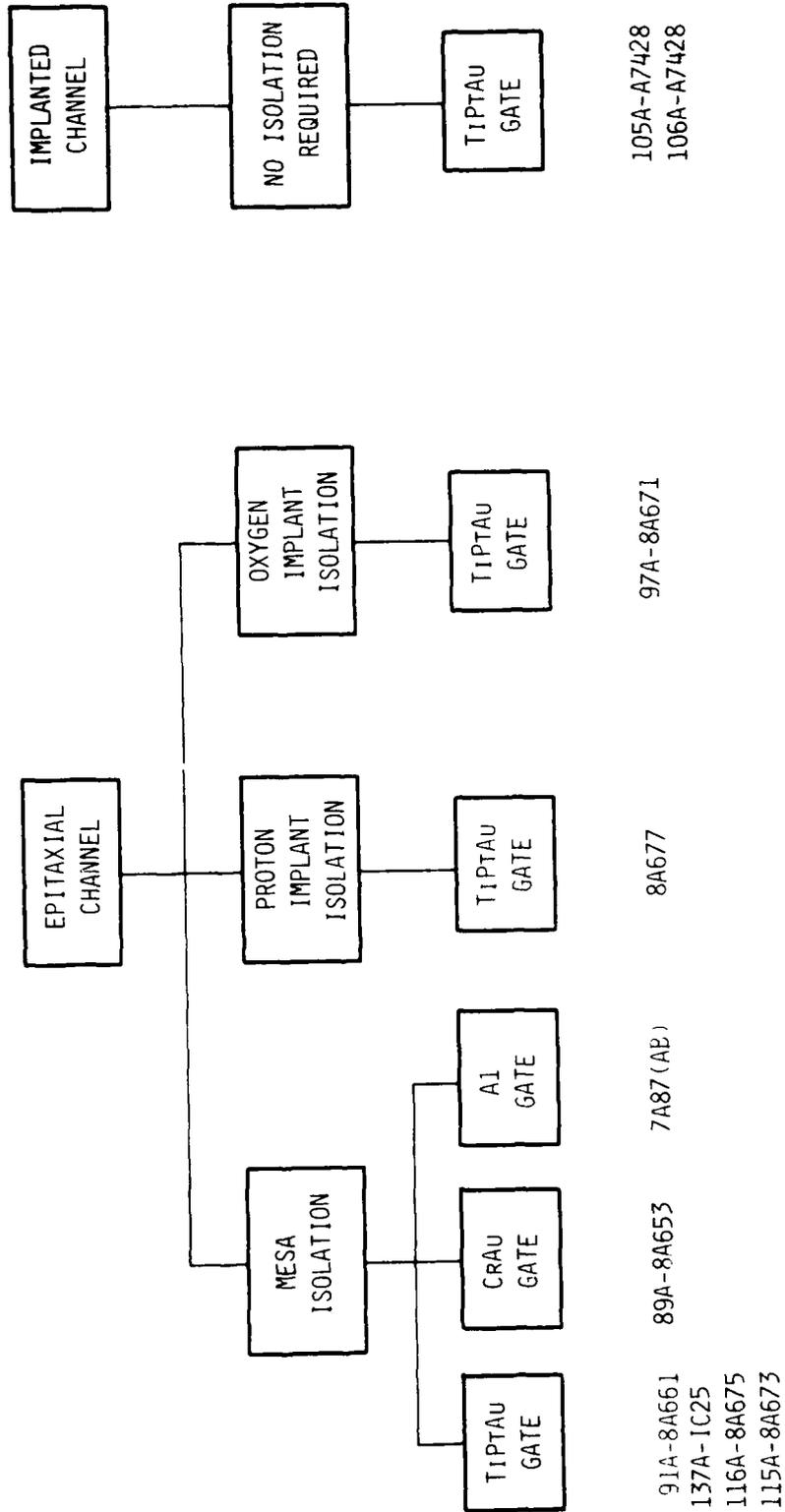


Figure 3-12. Main categories of processed devices that were studied.

channels, the three subcategories, mesa-, proton implant-, and oxygen implant isolation, denote the different schemes of device isolation used (see Fig. 1-1). In the case of implanted channel devices, of course, no isolation scheme was necessary because of the semi-insulating nature of the substrate into which the channel (and contacts) were implanted.

Figure 3-12 also shows that for the mesa isolated devices, three gate technologies were studied, namely, TiPtAu, CrAu, and Al. These were chosen because they are the most commonly used technologies. Actually the series of measurements pertaining to the Al gates were performed on devices fabricated during the previous contract. Only TiPtAu gates were used with the isolation implanted devices to keep the number of subcategories to a manageable level.

Below each subcategory are numbers referring to the wafer designation. These will be used throughout the report for identification. These numbers refer only to the successful wafer "runs". A number of cases were "aborted" prior to wafer processing and are not listed.

Figure 3-13 is a more detailed breakdown of the mesa isolation subcategories to demonstrate the passivation options studied. Note that in the case of mesa devices fabricated with TiPtAu gates, three passivation dielectrics were examined, namely,  $\text{SiO}_x$ ,  $\text{Si}_3\text{N}_4$ , and polyimide. Half of each wafer remained unpassivated. Again, to reduce the number of permutations, only  $\text{SiO}_x$  passivation was studied for devices with CrAu and Al gates.

Nearly all of the subcategories also included gateless devices, that is, FET structures without gates.

Figure 3-14 is a companion to Fig. 3-13 for the isolation implanted devices.

### 3.3.2 Measurement categories

Table 3-1 is a complete summary of the devices studied, listed by wafer number, substrate type, channel type, and isolation and passivation technologies

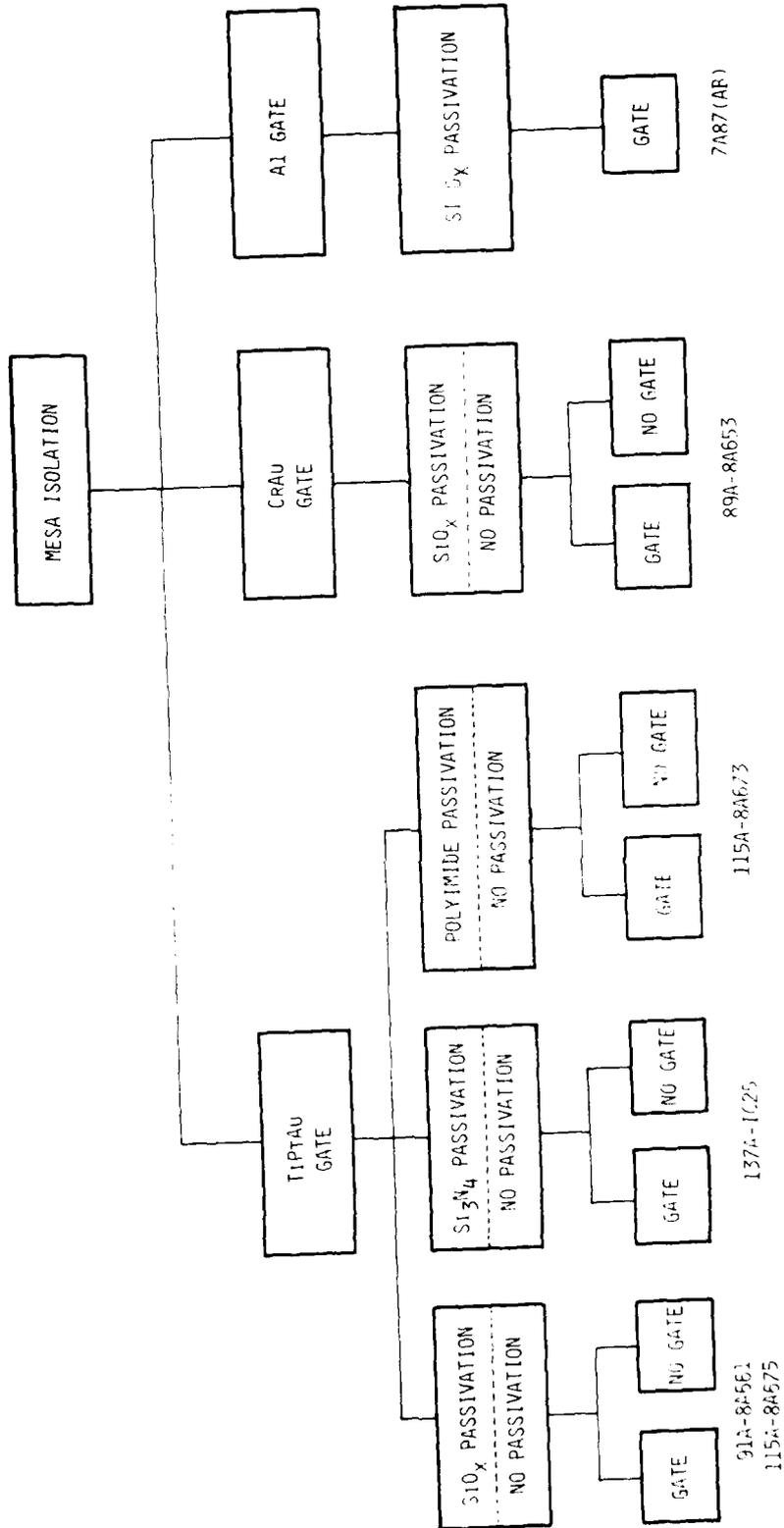


Figure 3-13. Diagram illustrating subcategories of mesa isolated devices.

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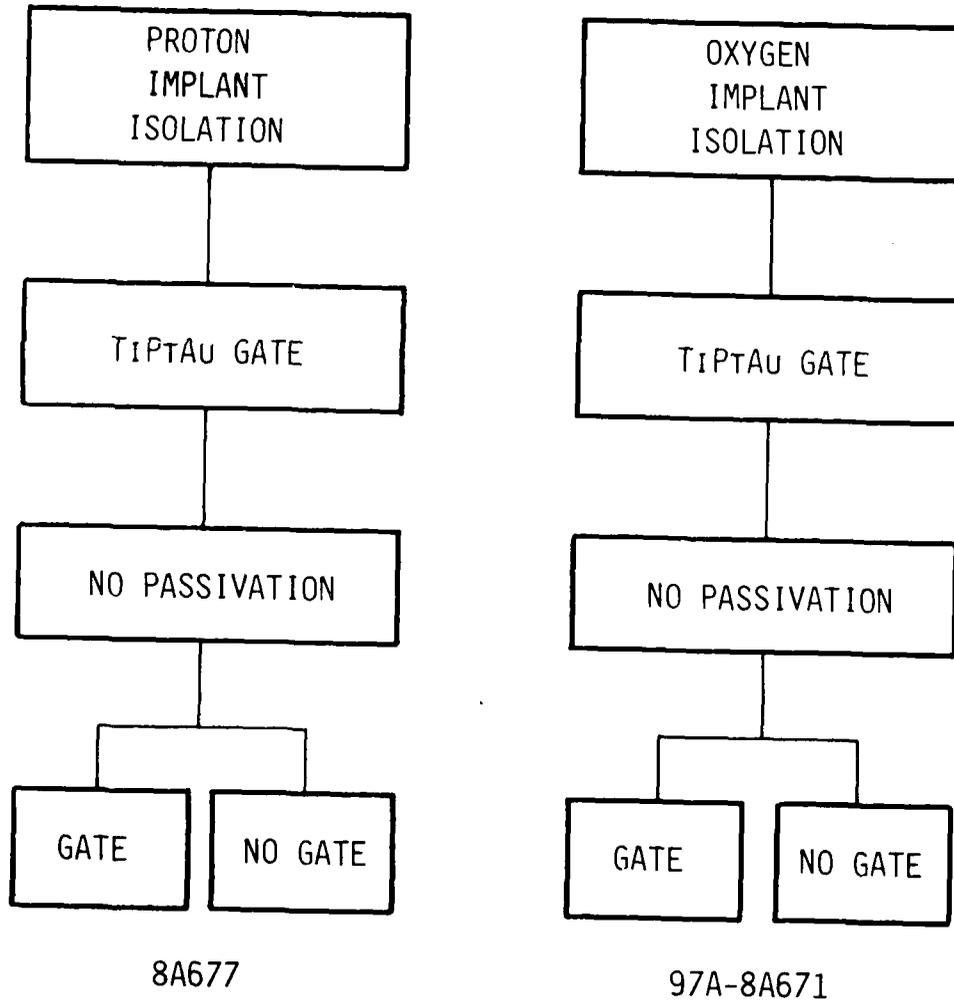


Figure 3-14. Subcategories of implant isolated devices.

used. Note that all substrates were chromium doped, except the one used for channel implant, which was a Czochralski pulled crystal purchased from Metals Research Industries.

The last four columns in each category list the types of electrical measurements performed. This table will be convenient for later reference when the experimental results are discussed.

### 3.4 Description of Device Technology

#### 3.4.1 Introduction

All devices were processed on two types of wafers, namely, (1) CVD epitaxially grown thin films on Cr-doped semi-insulating substrates and (2) silicon implanted channel layers in undoped semi-insulating substrates.

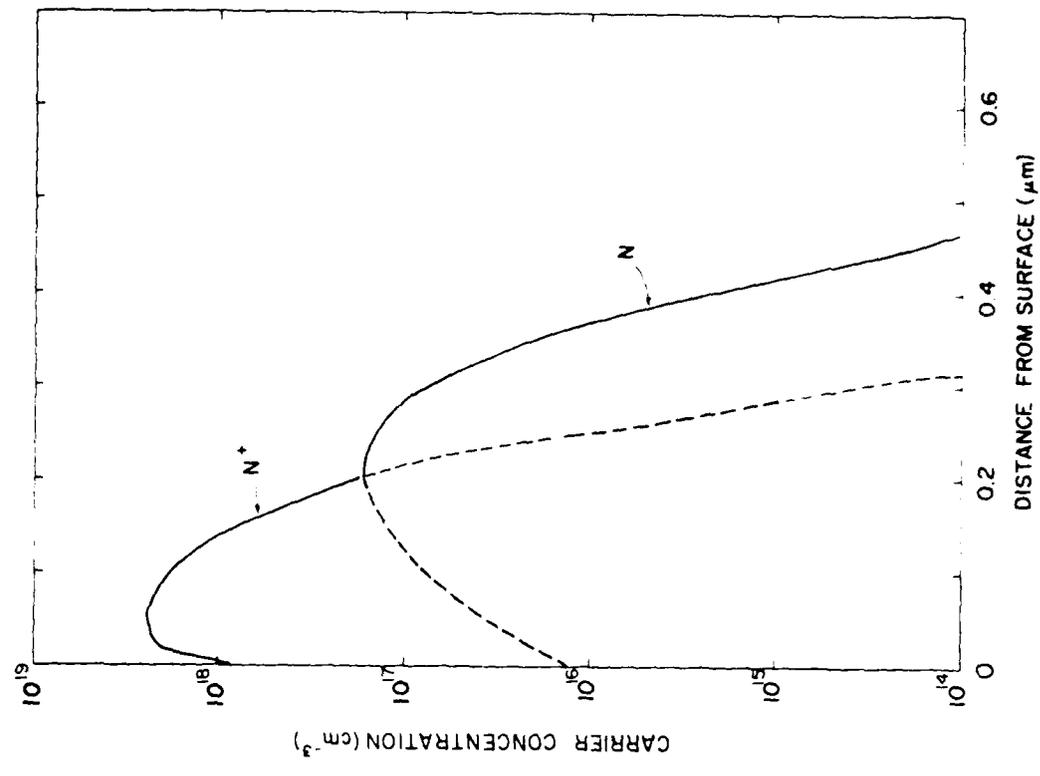
The epitaxial wafers consisted of a 0.2  $\mu\text{m}$  thick  $\text{N}^+$  layer for ohmic contacts ( $n > 2 \times 10^{18} \text{ cm}^{-3}$ ) deposited over a 0.25  $\mu\text{m}$  thick N-layer for the channel ( $n \approx 2 \times 10^{17} \text{ cm}^{-3}$ ). The channel layer, in turn, was grown over a buffer layer approximately 2  $\mu\text{m}$  thick ( $n \approx 5 \times 10^{13} \text{ cm}^{-3}$ ). The starting thickness of the semi-insulating substrate was 0.43 mm (17 mils). All of the substrates were Cr-doped but from different suppliers. The silicon implanted wafers were undoped LEC substrates from Metals Research Industries. See Table 3-1. Doping profiles typical of those used are shown in Fig. 3-15.

The general process steps were identical for all wafers with the exception of the mesa isolation. This will be discussed later. The source and drain contacts were composites of Ni/AuGe alloyed at 460°C. The alloying temperature cycle is shown in Fig. 3-16. TiPtAu gates were used on all wafers except wafer 8A653 which had CrAu gates. The gates were recessed. The recessed trough was obtained by chemical etching (see Fig. 1-1). Some of the wafers were passivated after the gate process, as will be discussed later. All gate metals were deposited by E-beam evaporation. The source, drain, and gate pads, and gate, source, and drain beam leads were plated up to a thickness of 2.5  $\mu\text{m}$  to form

TABLE 3-1  
LIST OF PROCESS CATEGORIES STUDIED AND TYPES OF MEASUREMENTS TAKEN

WAFER DESIGNATION	SUBSTRATE DOPING AND MANUFACTURER	TYPE OF CHANNEL	TYPE OF ISOLATION	TYPE OF GATE	TYPE OF PASSIVATION	I V CHARACTERISTIC	BASEBAND NOISE VS. FREQUENCY	BASEBAND NOISE VS. TEMPERATURE	OSCILLATOR FM NOISE
89A-8A653	Cr-DOPED SUMITOMO	EPITAXIAL	MESA	{ CrAu NO GATE }	{ SiO <sub>x</sub> NONE SiO <sub>x</sub> NONE }	X X X X	X X X X	X X X	X X
91A-8A66	Cr-DOPED SUMITOMO	EPITAXIAL	MESA	TiPAu	{ SiO <sub>x</sub> NONE }	X X	X X	X X	X X
137A-1C25	UNDOPED MICROWAVE ASSOCIATES	EPITAXIAL	MESA	TiPAu	{ Si <sub>3</sub> N <sub>4</sub> NONE }	X X	X X	X	X X
115A-8A673	Cr-DOPED SUMITOMO	EPITAXIAL	MESA	TiPAu	{ POLYIMIDE NONE }	X X	X X	X	X X
97A-8A671	Cr-DOPED SUMITOMO	EPITAXIAL	OXYGEN IMPLANT	TiPAu	NONE		X		
105A A7428 106A A7428	UNDOPED METALS RESEARCH	IMPLANTED	MESA	TiPAu	{ SiO <sub>x</sub> NONE }	X	X		X X
7A87	Cr-DOPED SUMITOMO	EPITAXIAL	MESA	Al	SiO <sub>x</sub>	X	X	X	

PBN-82-1102



PBN-82-1170

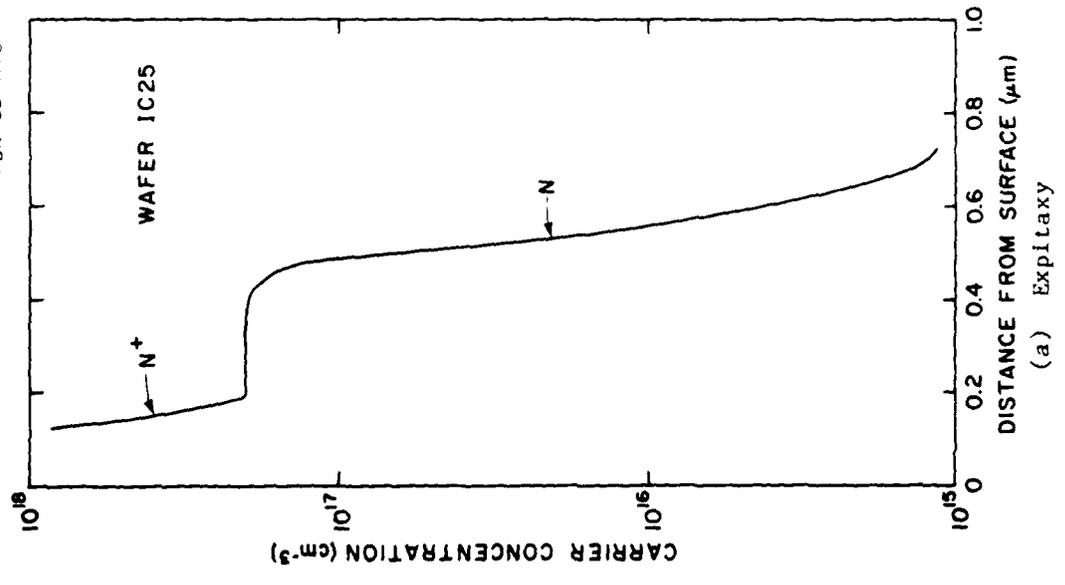


Figure 3-15. Profiles of carrier concentration for epitaxial and implanted devices.

PBN-80-657

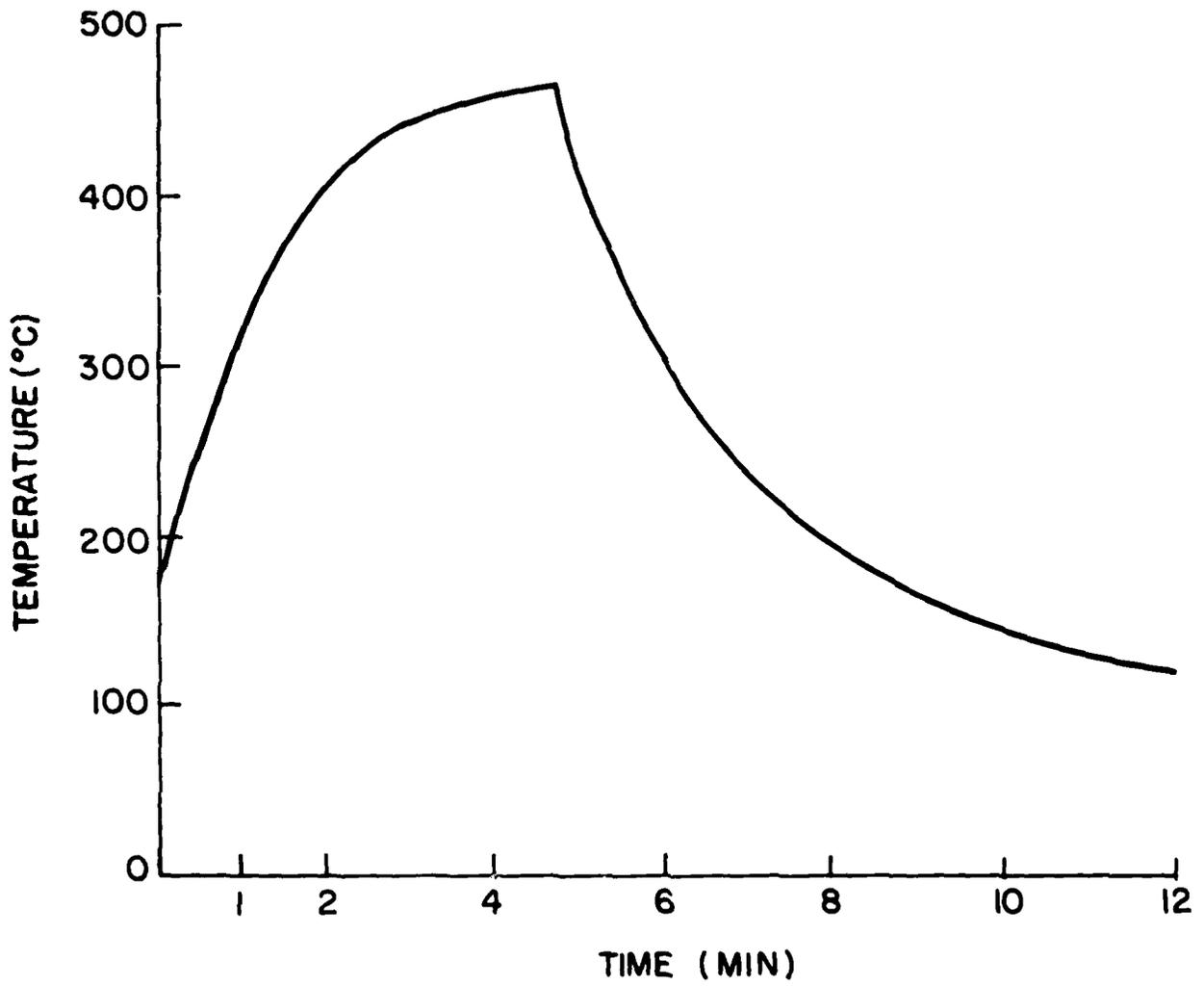


Figure 3-16. Heating cycle for alloying contacts.

sturdy, easily bondable contacts. The substrates were then lapped down from the backside to 0.1 mm and gold plated, after which the chips were diced by chemical etching.

#### 3.4.2 Mesa formation and implant isolation

Two types of mesa isolation were used, etching and implantation with  $^{16}\text{O}^+$  or  $^1\text{H}^+$  ions, as mentioned earlier.

Mesa etching was achieved by chemical removal of the  $\text{N}^+$  and N layers outside of the mesa area. The etch depth exceeded the sum thickness of the two layers.

Implant isolation with either  $^{16}\text{O}^+$  ions or  $^1\text{H}^+$  ions was investigated because of its importance in monolithic circuit technology. In this method of isolation, carrier compensation occurs by radiation damage yielding a semi-insulating layer. A nearly planar surface is maintained since little or no surface etching is required.

In our implantation the  $\text{N}^+$  layer was removed by chemical etching outside of the "mesa" area. See Fig. 1-1. Following this step, in the case of  $^{16}\text{O}^+$  implantation, four ion energy levels were employed. This was done in order that the implanted ion and associated radiation damage would be distributed uniformly from the surface down to about  $0.75 \mu\text{M}$  below the surface. The dosage used was based on the carrier concentration of the N-layer. For each carrier, one  $^{16}\text{O}^+$  ion was implanted. The dose energy schedules followed was:  $5 \times 10^{12} - 50$ ;  $4 \times 10^{12} - 100$ ;  $7 \times 10^{12} - 215$ ;  $5 \times 10^{10} - 400$  ( $\text{O}^+$  ions/ $\text{cm}^2$ -keV).

Implant isolation with  $^1\text{H}^+$  ions was carried out in a similar fashion but only at two beam energy levels. The dose schedule was:  $2 \times 10^{13} - 40$ ;  $2 \times 10^{13} - 80$  (ions/ $\text{cm}^2$  - keV).

The oxygen ion implant was completed before the source-drain alloying cycle, whereas the proton implant followed this cycle. Our experience indicates that some undesired annealing of the proton damaged area would occur at the 460° alloying temperature which would result in some loss of compensation. This loss does not occur for oxygen implants at the dose levels used even at temperatures much higher than 460°C.

#### 3.4.3 Channel implantation

Silicon was used as the dopant for the channel implanted wafers in areas delineated by a shallow etch. The  $N^+$  doping was implanted only in the source-drain contact regions. The implanted doping profile is shown in Fig. 3-15. This profile corresponds to an LSS calculation with third moment correction included for the implants used, namely:  $3.3 \times 10^{12} \text{ Si}^+/\text{cm}^2$  at 220 keV for the channel,  $2 \times 10^{13}$ - and  $1.3 \times 10^{13} \text{ Si}^+/\text{cm}^2$  at 60 and 120 keV, respectively, for the  $N^+$  contacts. Actual activations measured on monitor slices were about 45 percent for the channel doping. We have obtained over 75 percent activation on other LEC material indicating that this material may not be the best available for devices.

The implanted substrate, after capping with  $\text{Si}_3\text{N}_4$  was annealed at 850°C for 20 min in a nitrogen atmosphere. The capping cycle occurred in a cold wall reactor and consisted of a 5-min period at 200°C followed by a rise to 710°C and a 500 to 700A  $\text{Si}_3\text{N}_4$  deposition, all in about 20 sec. This step was followed by a rapid cooling to 200°C in less than 1 min. An additional coating of about 2500A of  $\text{SiO}_2$  deposited at 400°C in 7 min was then added to both sides of the wafer.

#### 3.4.4 Dielectric passivation

It was mentioned previously that three types of passivation were used, namely,  $\text{SiO}_x$ ,  $\text{Si}_3\text{N}_4$ , and polyimide. In the case of  $\text{SiO}_x$ , 4000A thick films were deposited by E-gun evaporation of  $\text{SiO}_x$  with  $\text{O}_2$  bled into the evaporator. The pattern was obtained by a lift-off process.

$\text{Si}_3\text{N}_4$  films, 5000 Å thick were deposited in a Technics plasma enhanced CVD system. The substrate was heated to 150°C and then to 200°C for about 1/2 hr each. The deposition was carried out at 300°C for approximately 1/2 hr. The pattern was delineated by Freon plasma etching.

Polyimide films were produced by spinning on Dupont Pyralin polyimide coating PI-2555 followed by a curing step at 250°C for 1 hr\*. The film thickness was approximately 0.75 μm. The film patterns were produced by  $\text{O}_2$  plasma etching.

#### 3.4.5 Device design

All devices tested were of a low-noise design with a channel doping of  $2 \times 10^{17} \text{ cm}^{-3}$ , and a contact doping exceeding  $2 \times 10^{18} \text{ cm}^{-3}$ . The gate was centered with a total periphery of 500 μm, and a length of 1 μm. To permit valid comparison between devices, the target specification for  $I_{\text{DSS}}$  was set for the range 60 to 100 mA at room temperature. Most devices tested met this requirement, though in some cases, because of yield, out-of-range devices were also accepted.

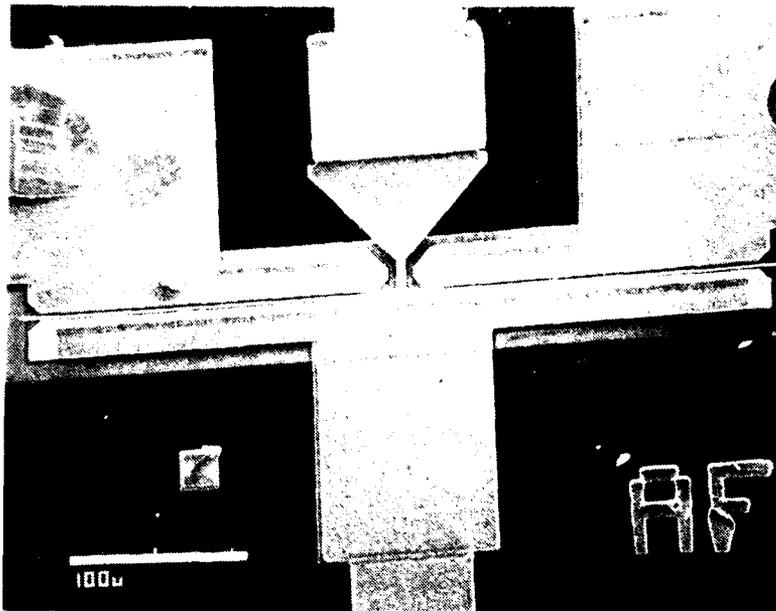
Except for wafer run 7A87, all devices had "plated-up" beam lead source-, gate-, and drain contacts. We chose the beam lead approach so that no stresses would be applied to the chip during bonding of the source, gate, and drain contacts. We have determined in the previous contractual study that stresses can increase the 1/f noise substantially. Fig. 3-17 (a), (b) are SEM photographs of a typical device (in this case, a channel implanted device).

Wafer run 7A87 did use gate and drain contact pads. A description of this device is reported in the final report of the previous contract.

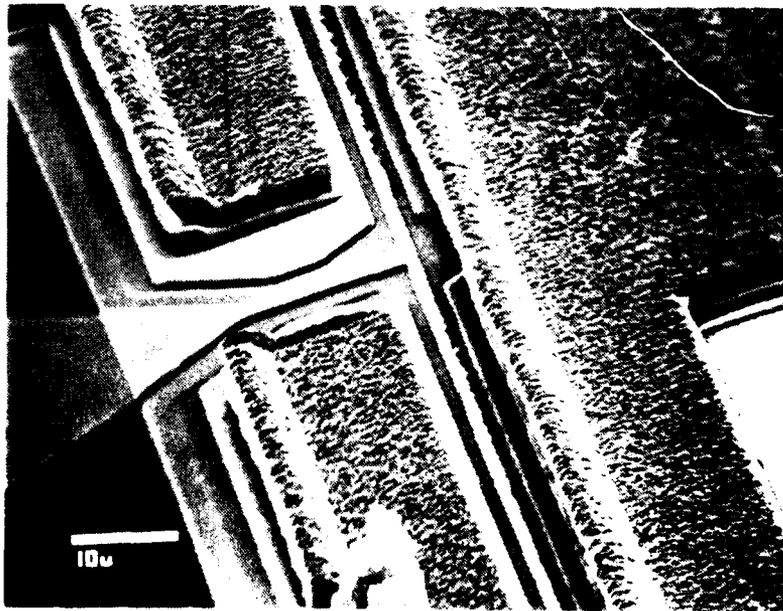
The chip thickness was 0.1 mm and the remaining chip dimensions are 0.8 x 0.6 mm. All wafers were gold plated bottom side to facilitate die bonding.

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\*Wafer 8A673, an exception, was cured for 2 hr, because of reworking of the wafer.



(a) Entire device.



(b) Close-up of gate region.

Figure 3-17. SEM photograph of low-noise device.

## 4.0 EXPERIMENTAL RESULTS

### 4.1 Introduction

There does not appear to be an optimum way to present the voluminous and variety of data measured on the devices listed in Table 3-1. Therefore, results will be presented in the way which, it is believed, emphasizes the similarities and differences in the data obtained with the various technologies. Thus, rather than present all of the data for one device consecutively from D.C. I-V characteristics to FM oscillator noise, the following order of presentation has been adopted. First the I-V characteristics as a function of temperature and optical excitation will be described, sequentially, for all devices. Next, the baseband noise vs. frequency, temperature, and optical excitation will be presented. Finally, FM oscillator noise for each device will be presented, again sequentially.

Simply put, in reference to Table 3-1, the data corresponding to column 7 will be described first, then column 8 and 9, followed by column 10.

### 4.2 I-V Characteristics as a Function of Temperature and Optical Excitation

#### 4.2.1 Introduction

In these experiments, the I-V characteristics were taken with a conventional X-Y recorder as a function of gate and drain bias. Temperature was varied from +100°C to -100°C in steps. At each temperature, the surface of the device between the source-drain region was illuminated by a GaAlAs laser at a wavelength of 8080 Å. (For convenience, we have approximated this by 8000 Å on the graphs.) At this wavelength, the absorption coefficient is approximately  $10^4 \text{ cm}^{-1}$ . See Fig. 4-1. The penetration depth corresponding to this wavelength

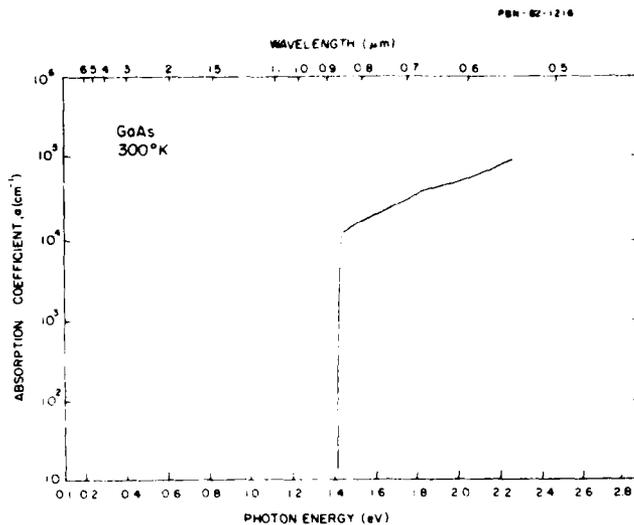


Figure 4-1. Absorption coefficient in GaAs as a function of photon energy.

is about 1 μm, which means that the entire channel region and some is penetrated. Despite this fact, it shall be argued, based on the results obtained during the previous contract and the data to be presented, that the changes observed in the I-V characteristics and baseband noise with laser illumination can be explained by surface states.

We chose a laser power output of 0.5 mW for all of our tests. This level was determined to be sufficient to "saturate" whatever change was being observed. For example, in the case of the I-V characteristics, the drain current increases with laser illumination as Fig 4-2 shows, but the change diminishes about 0.5 mW. A similar saturation was observed in the level of baseband noise with illumination as Fig. 4-2(b) illustrates.

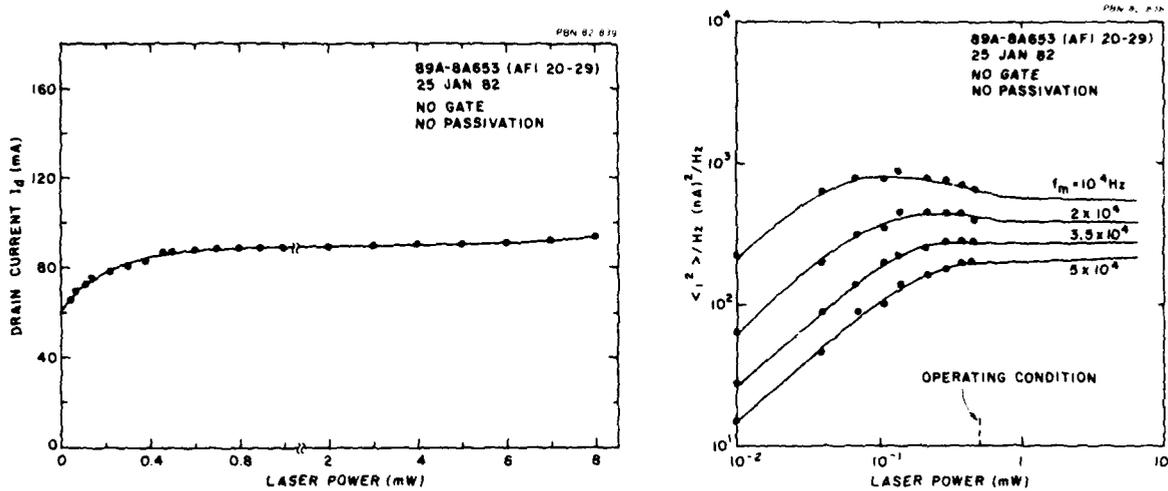
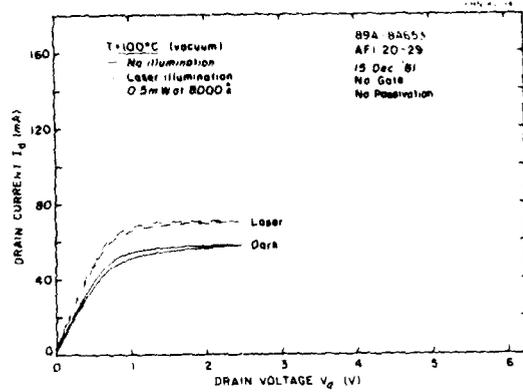


Figure 4-2. Relation between laser power and change in drain current and baseband noise.

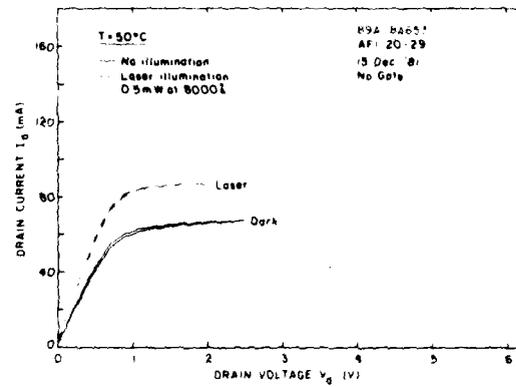
#### 4.2.2 Ungated devices with and without SiO<sub>x</sub> passivation (wafer 89A 8A653)

Figures 4-3 and 4-4 are I-V characteristics of ungated devices with and without SiO<sub>x</sub> passivation. Two sets of curves are shown in each graph, the solid lines (no illumination) and dashed lines (laser illumination). Five temperatures are illustrated, for 50° intervals (though finer steps were measured) between +100°C to -100°C.

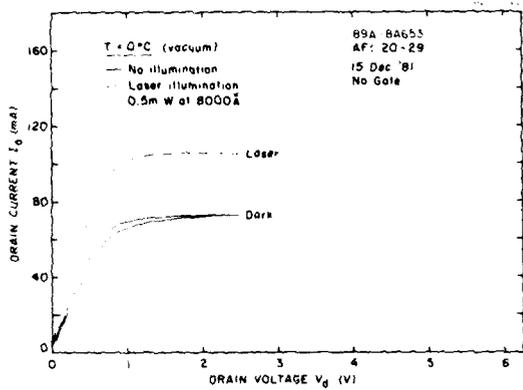
Four outstanding features of both sets of graphs are evident, namely, (1) the drain current increases with decreasing temperature, (2) laser illumination increases the current, (3) hysteresis increases with decreasing temperature, and (4) laser illumination eliminates or reduces the hysteresis, especially at the lower temperatures.



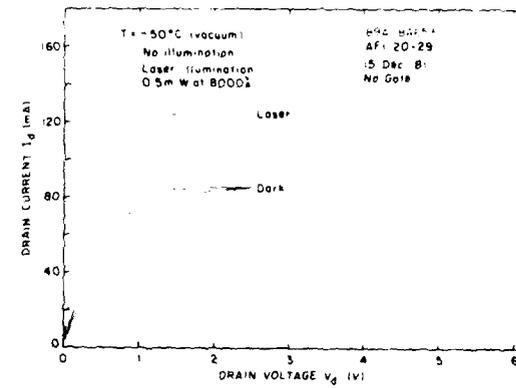
(a)  $T = 100^{\circ}\text{C}$ .



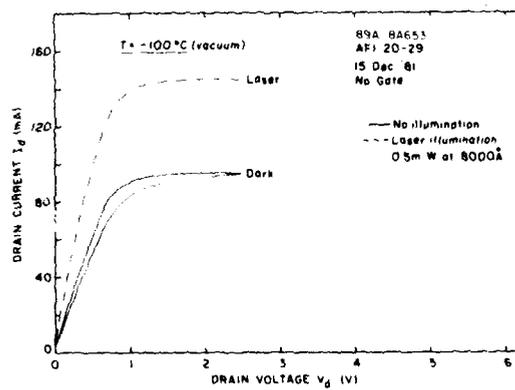
(b)  $T = 50^{\circ}\text{C}$ .



(c)  $T = 0^{\circ}\text{C}$ .

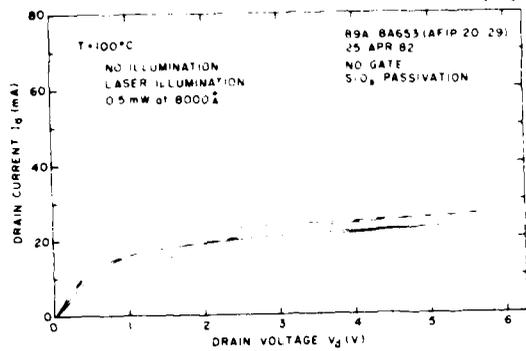


(d)  $T = -50^{\circ}\text{C}$ .

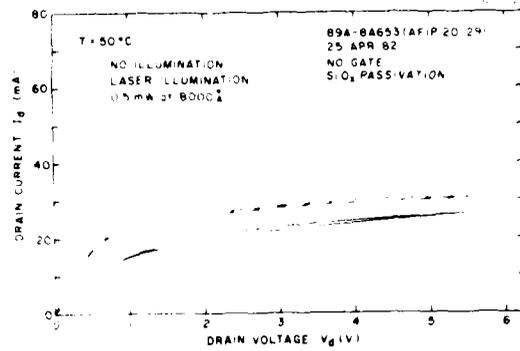


(e)  $T = -100^{\circ}\text{C}$ .

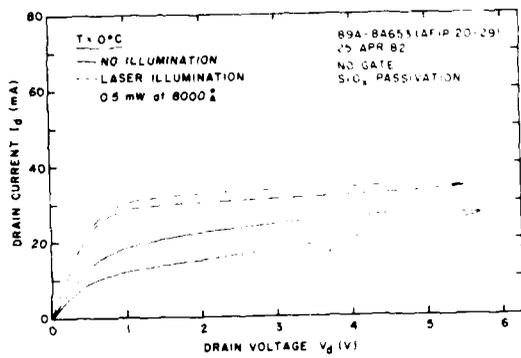
Figure 4-3. Effect of temperature and laser illumination on I-V characteristics of an ungated FET with no passivation (wafer 89A-8A653).



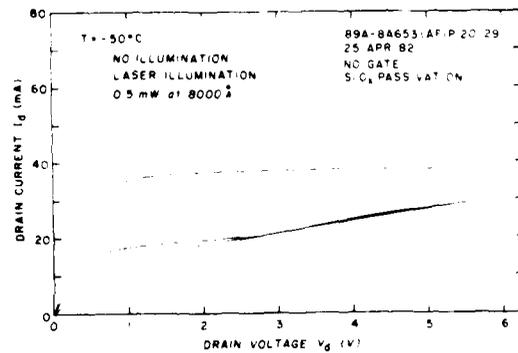
(a)  $T = 100^{\circ}\text{C}$ .



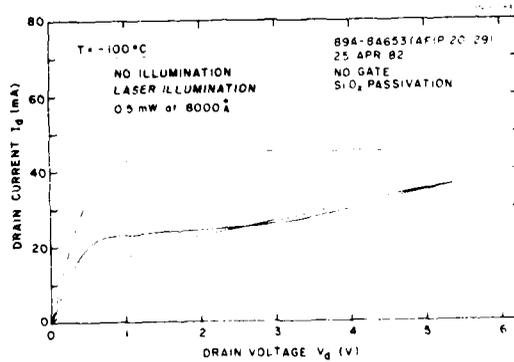
(b)  $T = 50^{\circ}\text{C}$ .



(c)  $T = 0^{\circ}\text{C}$ .



(d)  $T = -50^{\circ}\text{C}$ .



(e)  $T = -100^{\circ}\text{C}$ .

Figure 4-4. Effect of temperature and laser illumination on I-V characteristic of an ungated FET with  $\text{SiO}_x$  passivation (wafer 89A-8A653).

The first observation can be explained readily by the increase in the electron saturated velocity with decreasing temperature.<sup>20</sup> However, the increase in current is somewhat greater than the velocity data predicts. This is understandable since the velocity data corresponds to a constant field, which is hardly the case in an FET structure. It is to be noted that the percentage increase in current is higher for the laser-illuminated case than for the non-illuminated case. This, we believe, can be explained by a trap model to be discussed shortly.

That traps are playing a role is quite evident from the second, third and fourth observations. It is reasonable to assume that the elimination of hysteresis with laser illumination, and the associated increase in current is caused by emptying of electron traps by the optical excitation. This hypothesis is buttressed by the fact that in the non-illuminated case, the hysteresis is also reduced when the temperature is increased -- in this case, due to trap emptying by thermal excitation. The final argument supporting this hypothesis is the fact that optical excitation has a diminishing effect on increasing the current as the temperature is increased, simply because the traps have already been emptied to a great extent by thermal energy imparted to the trapped electrons.

Where are these traps? Based on our present data, and the fact that the laser excitation penetrated through the active channel layer, it could be argued that either bulk or surface traps (or both) are involved. We favor surface traps based on our studies in the previous contract. A surface trap model can easily explain the types of changes caused by thermal and optical excitation that we have just discussed.

Figure 4-5 is a simplified diagram representing an electron surface state trap model. In actuality, there is undoubtedly a thin oxide layer on the surface of the GaAs which alters the details of the trap model, as was described in a previous report.<sup>21</sup> Nevertheless, the trap states on the semiconductor, itself, are still the means by which coupling to the semiconductor bulk takes place.

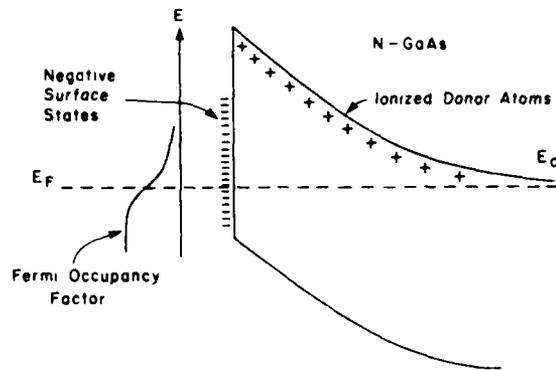


Figure 4-5. Simplified surface-state model of semiconductor.

We assume, therefore, the existence of electron surface states, distributed more or less uniformly over a range of energies within the band gap. This is a realistic assumption. Those states above the Fermi level will be essentially empty, and hence each will have lost a negative charge.

The depletion layer in the underlying semiconductor will extend to a depth such that the ionized donor atoms will just balance the net negative surface charges. As a consequence, the energy bands bend upward at the surface as shown in Fig. 4-5 and a barrier is established. This barrier, for a "normal" surface, that is, a surface not purposely contaminated, is approximately  $0.6 \text{ eV}^{22}$ .

When the surface is illuminated by a laser, some electrons are given sufficient energy by photo-excitation to escape from the traps and surmount the potential barrier as shown in Fig. 4-6. Thermal excitation produces the same effect.

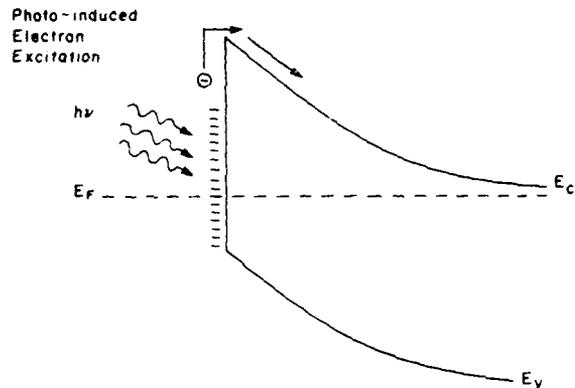


Figure 4-6. Photo-excitation of electron and its release from a surface trap.

We apply this model to the gateless structure. See Fig. 4-7(a). The depletion layer of depth "d" defines the channel height "h," which, in turn, determines the saturated current level I in the device above the knee of the I-V characteristic.

Consider what happens when the surface between the source and drain contacts is illuminated with a laser. If sufficient laser power is used, the surface traps can be emptied of electrons which surmount the barrier. These electrons are swept out of the depletion layer into the channel. In addition, the depletion layer contracts, and the channel opens up to its maximum height. See Fig. 4-7(b). As long as the surface is illuminated, the traps remain empty, and the hysteresis vanishes.

The same effect is achieved at elevated temperatures, except that electrons are emptied by thermal excitation over the barrier. However, unless the temperature is high enough, not all traps are emptied, and the current does not quite reach the illuminated level, and may exhibit some hysteresis. See Fig. 4-3(a) and 4-4(a).

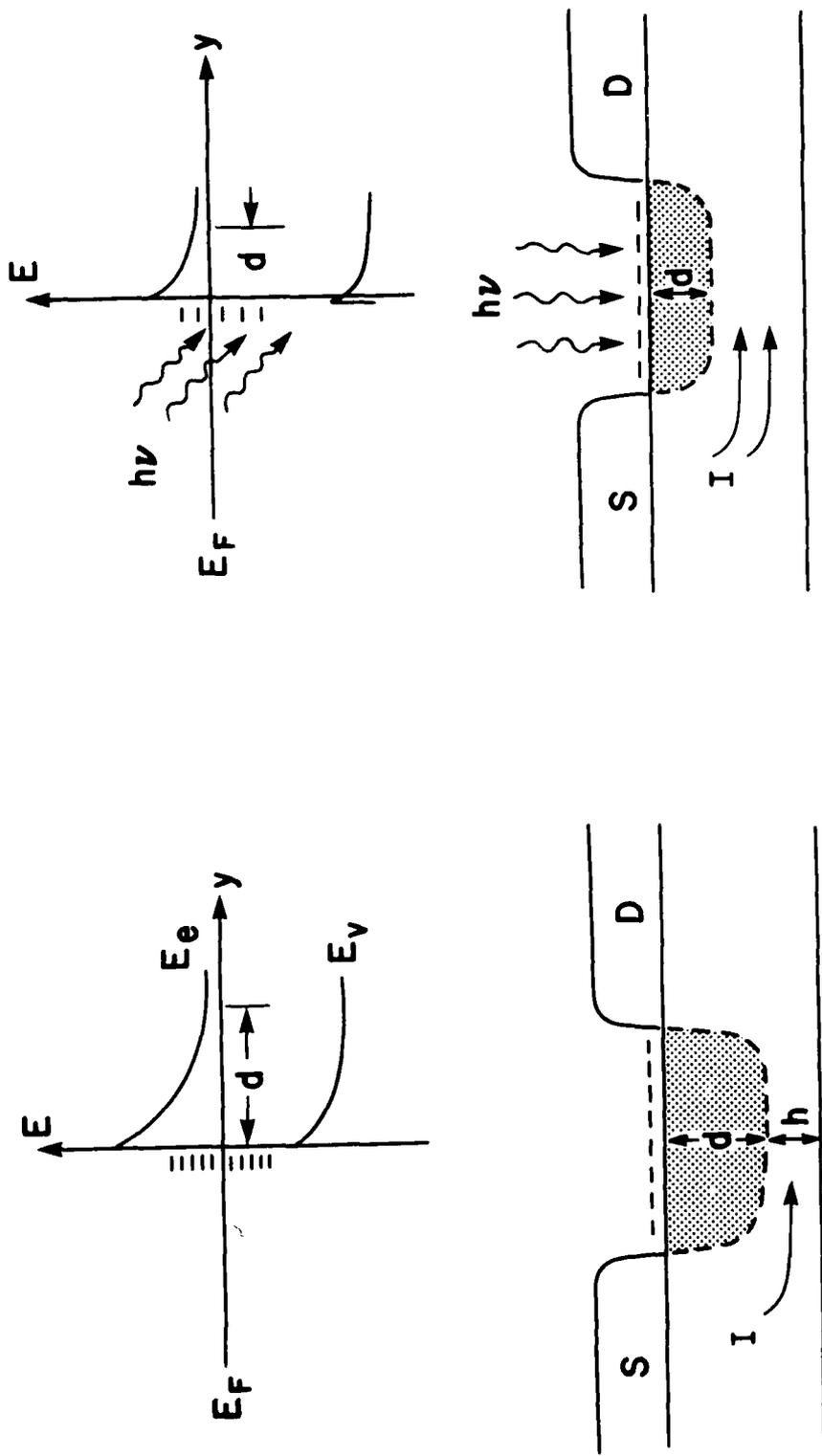


Figure 4-7. Model for depletion layer formation by surface states in an ungated FET.

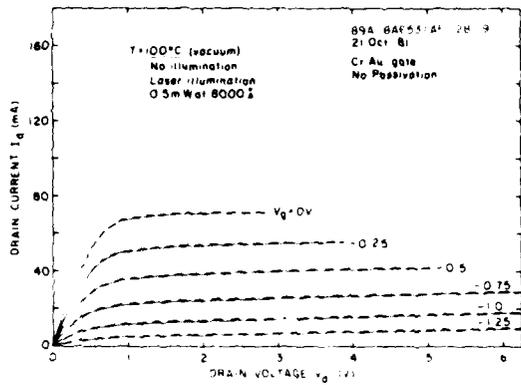
The above model explains the general features of the I-V characteristics for both the unpassivated and passivated structure. However, a closer look at the graphs in Fig. 4-3 and 4-4 shows that the hysteresis is much more pronounced for the passivated device. We conclude that the  $S_iO_x$  is responsible for additional surface states which are probably slower than those on the unpassivated structure. The additional surface states may also cause some reduction in saturated current. However, most of the reduction in saturated current for the passivated structure can be attributed to the fact that the channel was etched down excessively.

No ungated devices from other wafers were tested because of lack of time. However, based on our measurements of FETs, we did not expect results which could differ significantly from those discussed.

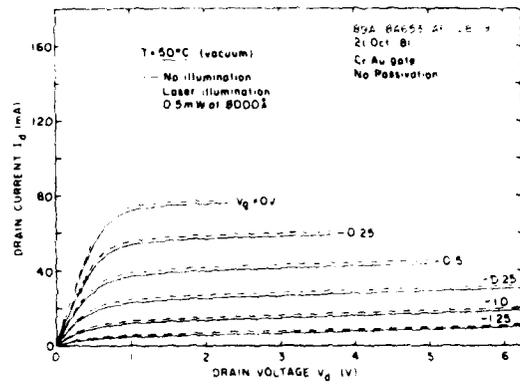
#### 4.2.3 FET with a CrAu gate and with and without $S_iO_x$ passivation (wafer 89A-8A653)

Figures 4-8 and 4-9 are I-V characteristics of FETs from the same wafer as the gateless devices just discussed. Note that the I-V characteristics go through the same transformation with temperature and laser excitation as did the gateless devices. Thus, both optical excitation and elevated temperatures remove the hysteresis. The explanation is the same, namely, emptying of surface states. However, there is a subtle difference because of the presence of the gate. See Fig. 4-10.

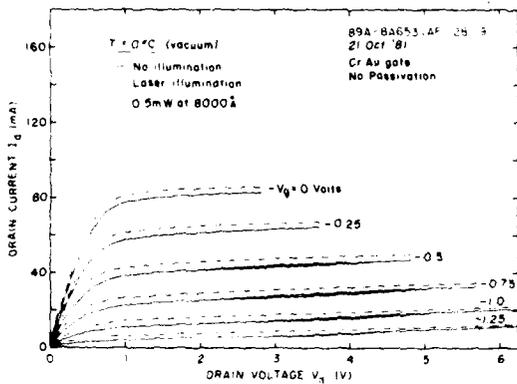
Let us assume for the moment surface states only in the exposed region between the gate electrode and the source and drain, corresponding to Fig. 4-10(a). If the associated depletion region extends further into the channel than under the gate, then it follows that the gate will lose control of the current and severe crowding of the I-V characteristic would result. Emptying of these traps would open up the channel as shown in Fig. 4-10(b) and restore control to the gate with a concomitant increase in channel current. Such current crowding is



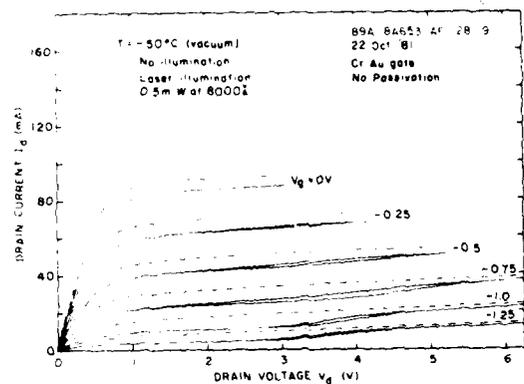
(a)  $T = 100^{\circ}\text{C}$ .



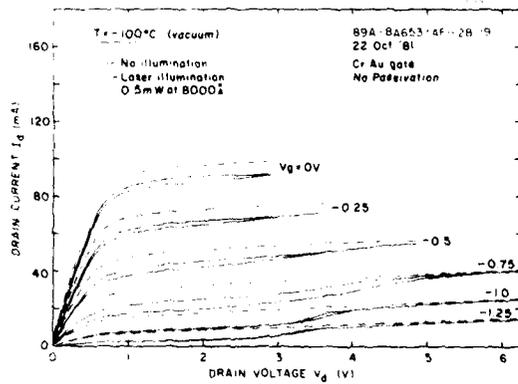
(b)  $T = 50^{\circ}\text{C}$ .



(c)  $T = 0^{\circ}\text{C}$ .

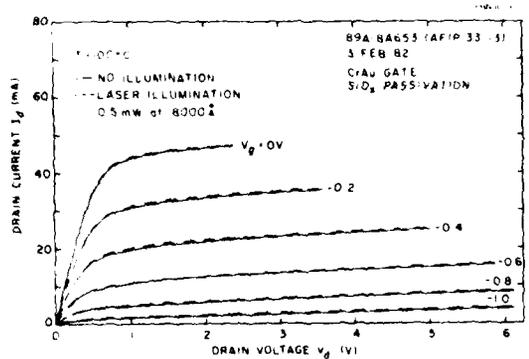


(d)  $T = -50^{\circ}\text{C}$ .

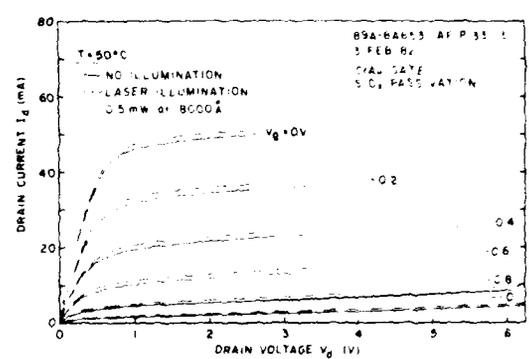


(e)  $T = -100^{\circ}\text{C}$ .

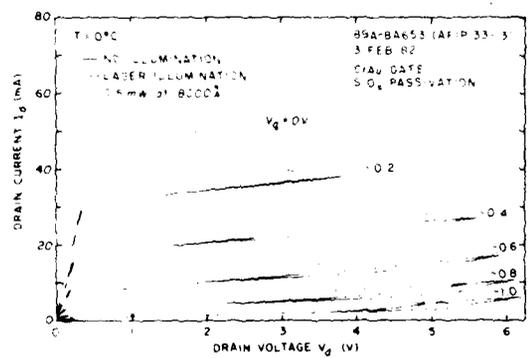
Figure 4-8. Effect of temperature and laser illumination on I-V characteristics of an FET with a CrAu gate and no passivation (wafer 89A-8A653).



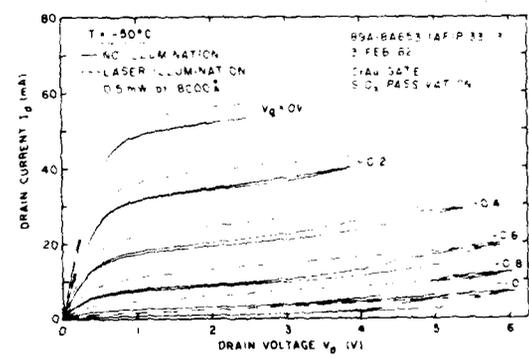
(a)  $T = 100^{\circ}\text{C}$ .



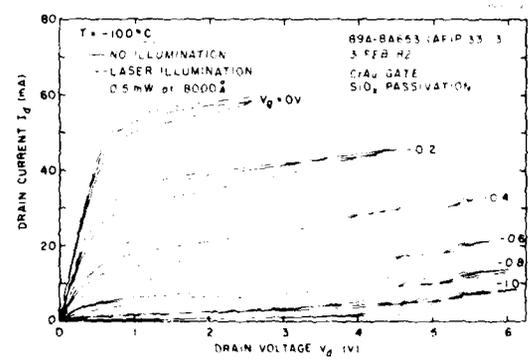
(b)  $T = 50^{\circ}\text{C}$ .



(c)  $T = 0^{\circ}\text{C}$ .



(d)  $T = -50^{\circ}\text{C}$ .



(e)  $T = -100^{\circ}\text{C}$ .

Figure 4-9. Effect of temperature and laser illumination on I-V characteristics of an FET with a CrAu gate and  $\text{SiO}_2$  passivation (wafer 89A-8A653).

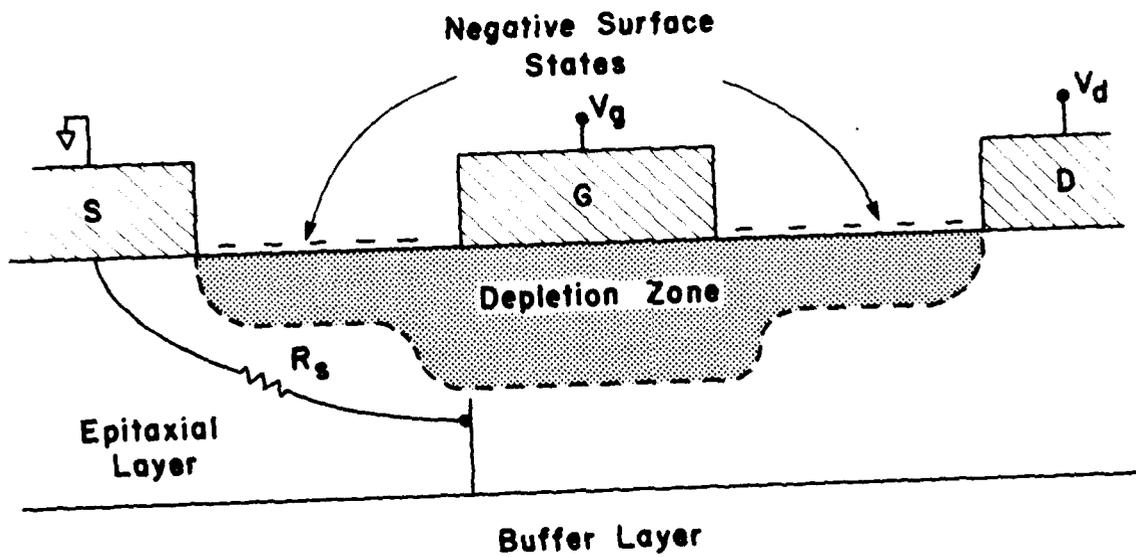
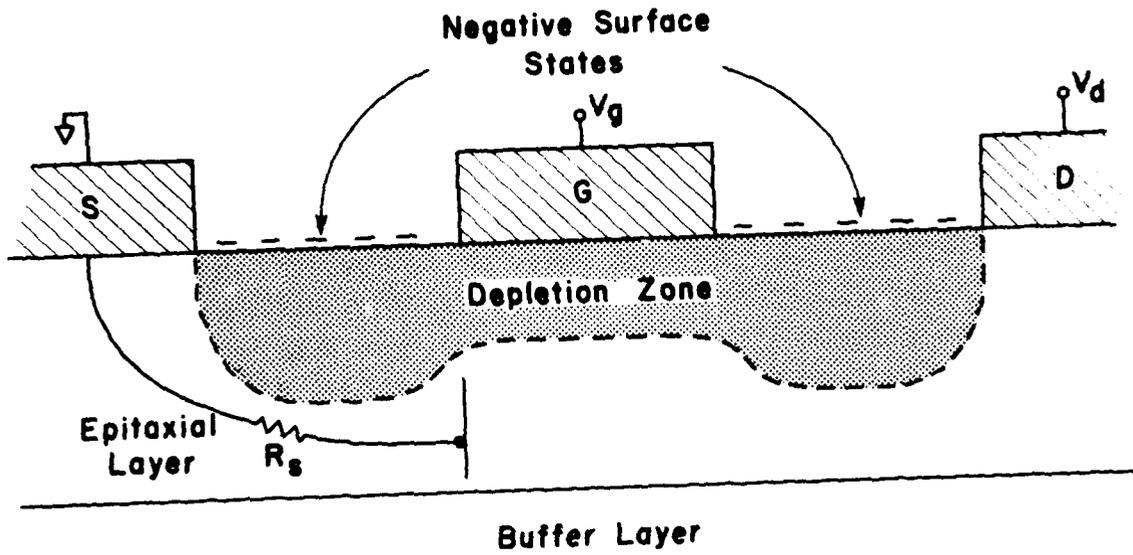


Figure 4-10. Simplified model for modulation of drain current by negative surface states.

not observed, therefore it must be concluded that this situation does not exist. That is to say the depletion layer produced by surface states between the electrodes does not define the channel height, that is, extend deeper than the depth of the layer under the gate.

How then is the current changed? There are two possible ways. First, modulation of the depletion layer depth by optical/thermal excitation in the region between source and gate can change the current because of the change produced in  $R_s$ , the source parasitic resistance. Thus opening up the channel in the region will reduce  $R_s$  and increase the current. Note that in this case one does not have to invoke any modulation of the depletion layer under the gate - hence no modulation of the source-gate capacitance. The implications of this will become evident, later, when FM noise is discussed. Second, there is no reason to assume that the region under the gate is devoid of surface states. Therefore, one must allow for the possibility that some of these, at least near the edges of the gate, can be excited optically. All of the states here can be excited thermally, of course. Therefore, modulation of the channel height under the gate will occur just as for the gateless structure. This modulation also will produce changes in channel current.

It must be concluded, therefore, that surface states on the exposed FET surface as well as those under the gate can affect the channel current, the first by modulation of  $R_s$ , the second by modulation of the source-gate capacitance. Both effects will also produce low-frequency drain current noise, but only the second source will lead to FM oscillator noise. Later, experimental evidence supporting this model will be presented.

There is still one remaining feature in the I-V characteristics shown in Figs. 4-8 through 4-10 which has not been explained. This is the sharp jump in current at large drain bias voltages. Note that these increases occur at low temperatures and only for the non-illuminated cases.

The following explanation is proposed. Since the current jump does not exceed the current level produced by optical excitation, it follows that the current increase is related to emptying of traps rather than to some other cause, such as avalanching. Since the jumps are most pronounced at high gate bias voltages, corresponding to maximum longitudinal electric field in the channel, it is suggested that ionization of traps is occurring, either by transfer of energy to trapped electrons by hot electrons, or by lowering of the barrier in the vicinity of a trap by the high fields.<sup>23</sup> Both of these mechanisms would more likely apply to bulk traps (traps within the channel) than to surface traps. If this is the case, then it follows that not all of the current increases produced by optical/thermal excitation can be attributed to surface traps alone. Our results do not allow us to separate the two sources.

It is to be noted that the unpassivated and passivated results do not differ markedly. The higher degree of hysteresis for the passivated devices is probably due to additional surface states introduced by the oxide layer as was proposed earlier.

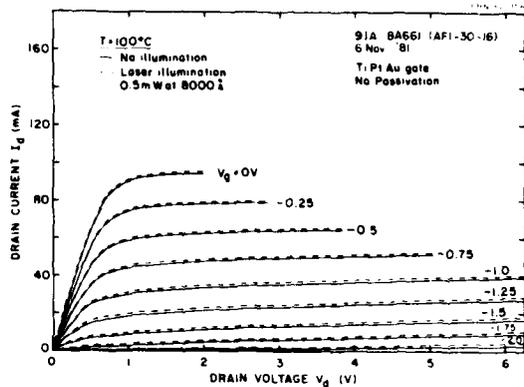
The results that we have just presented were repeated with our remaining devices fabricated with different passivations and gate metals. That is, though the degree of change may be different, qualitatively, the changes are identical. These additional results shall be described.

#### 4.2.4 FET with a TiPtAu gate and with and without SiO<sub>x</sub> passivation (wafer 91A-8A6b1).

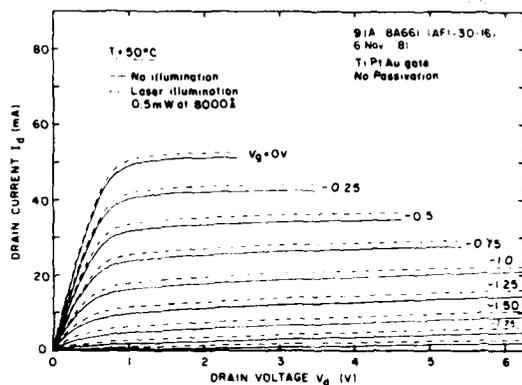
Figures 4-11 and 4-12 are I-V characteristics of FETs fabricated with TiPtAu gates, but in all other respects are identical to the devices discussed above\*. No new effects have been introduced by the change in gate metals, indicating that gate metallization is not important.

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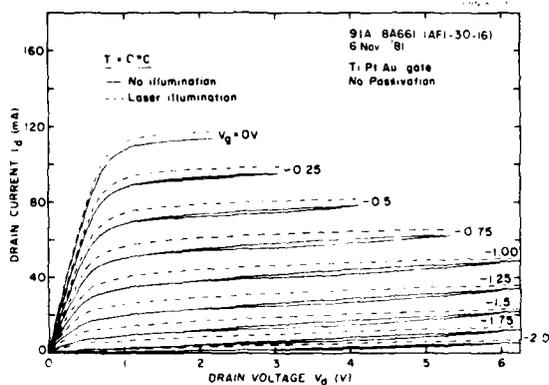
\*Note that the data for T = -100°C is missing in Fig. 4-12. This data was not taken.



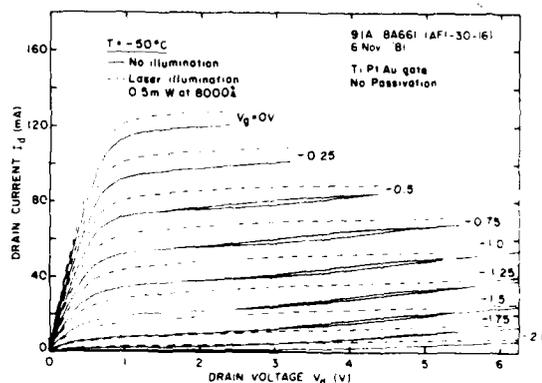
(a)  $T = 100^{\circ}\text{C}$ .



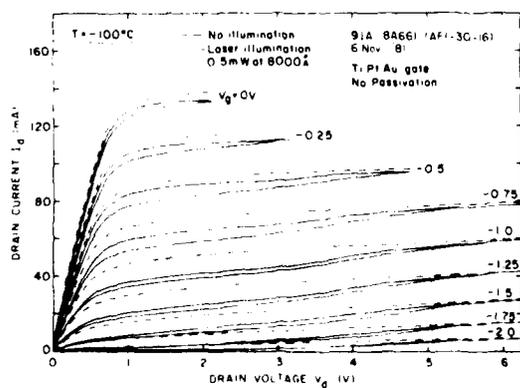
(b)  $T = 50^{\circ}\text{C}$ .



(c)  $T = 0^{\circ}\text{C}$ .

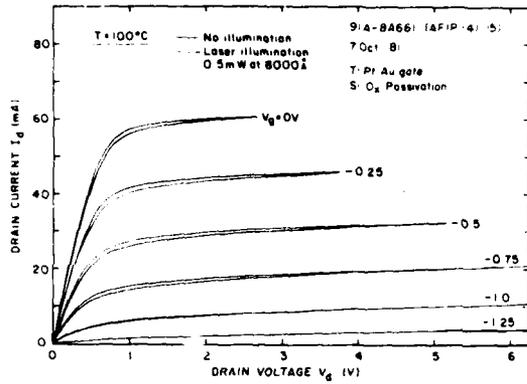


(d)  $T = -50^{\circ}\text{C}$ .

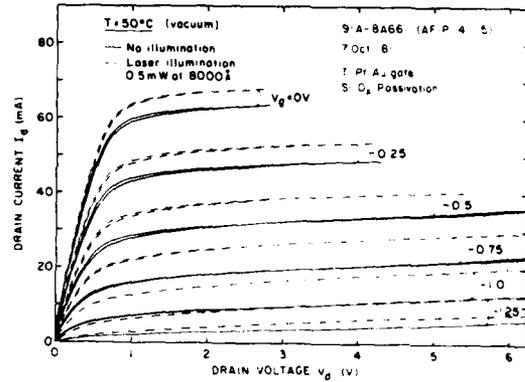


(e)  $T = -100^{\circ}\text{C}$ .

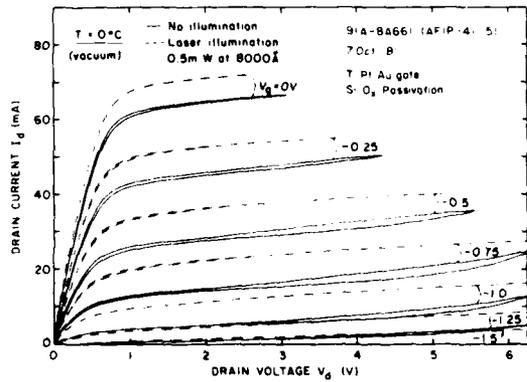
Figure 4-11. Effect of temperature and laser illumination on I-V characteristics of an FET with a TiPtAu gate and no passivation (wafer 91A-8A661).



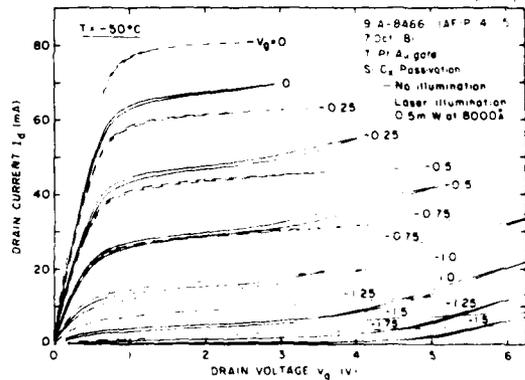
(a)  $T = 100^{\circ}\text{C}$ .



(b)  $T = 50^{\circ}\text{C}$ .



(c)  $T = 0^{\circ}\text{C}$ .



(d)  $T = -50^{\circ}\text{C}$ .

Figure 4-12. Effect of temperature and laser illumination on I-V characteristics of an FET with a TiPtAu gate and  $\text{Si}_3\text{O}_x$  passivation (wafer 91A-8A661).

4.2.5 FET with a TiPtAu gate and with and without Si<sub>3</sub>N<sub>4</sub> passivation (wafer 137A-IC25).

Figures 4-13 and 4-14 apply to the device category in which Si<sub>3</sub>N<sub>4</sub> passivation was being examined. (Note that for this set of curves, the non-illuminated and illuminated results were plotted as separate graphs which are presented side-by-side.)

The only difference between these results and those shown in Fig. 4-11 and 4-12 is a somewhat reduced hysteresis in the case of the Si<sub>3</sub>N<sub>4</sub> passivation. This would indicate that Si<sub>3</sub>N<sub>4</sub> introduces fewer traps than SiO<sub>x</sub>. The microwave noise measurements to be described later support this contention.

4.2.6 FET with a TiPtAu gate and with and without polyimide passivation (wafer 115A-8A673).

Figures 4-15 and 4-16 are results obtained with devices passivated with polyimide. The gate metals is TiPtAu. Here again all the familiar features are displayed. Note that the degree of hysteresis for the devices with passivation is only slightly greater, if at all, than that displayed by the unpassivated devices. This indicates that polyimide also does not introduce significant traps of its own. The microwave noise measurements bear this out, too, as will be demonstrated later.

4.2.7 FET with a TiPtAu gate, no passivation, and an implanted channel (wafer 105A-A7428).

Only a limited amount of I-V data was obtained for implanted channel devices because of lack of time. Fig. 4-17 illustrates the I-V characteristics for T = 100°C. Comparison of this curve with corresponding curves shown earlier indicates no qualitative difference.

#### 4.2.8 FET with an Al gate and no passivation (wafer 7A87(AB))

Some measurements were taken on devices fabricated during the previous contract. These were epitaxial channel devices with Al gates. The data presented in Fig. 4-18 represent these devices. Note again that the non-illuminated and illuminated curves are plotted on separate graphs and presented side-by-side. These measurements were taken early in this contract, before the temperature steps were standardized.

These results are rather unique in that the increase in current levels with laser illumination is much smaller than with all previous devices. Furthermore, the hysteresis is much reduced. This would indicate a much smaller level of surface (or bulk) states than implied by the previous results. The reason for this is not known. It is tempting to attribute this improvement in hysteresis to the Al gates. However, some devices from this wafer which were measured during the previous contract exhibited a pronounced hysteresis\*.

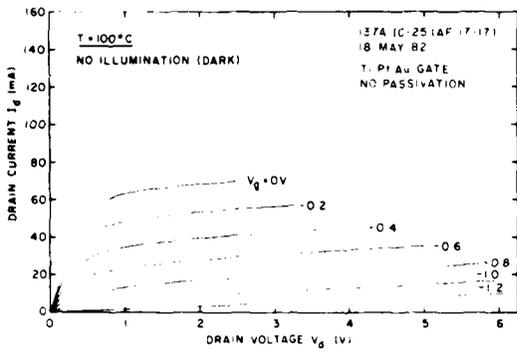
#### 4.3 Baseband Noise as a Function of Temperature and Optical Excitation

##### 4.3.1 Introduction

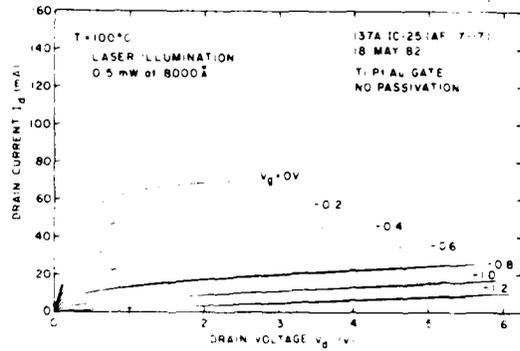
This section deals with measurements of the drain current fluctuations (noise) at baseband in the frequency range from 100 Hz to 200 kHz. Most measurements were taken for a drain bias voltage just above the knee of the I-V characteristic. The devices tested are listed in columns 8 and 9, Table 3-1. The order of device presentation adopted above will be retained for ease of reference to the I-V characteristics.

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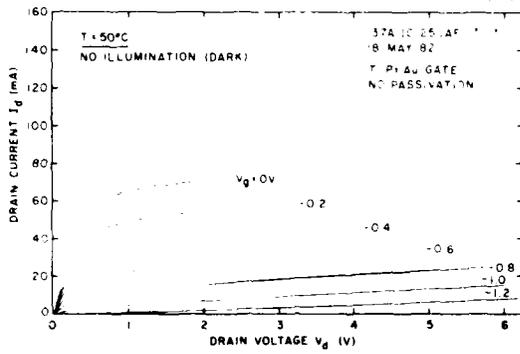
\*See Fig. 41 of the final report for this contract. (ref. 21).



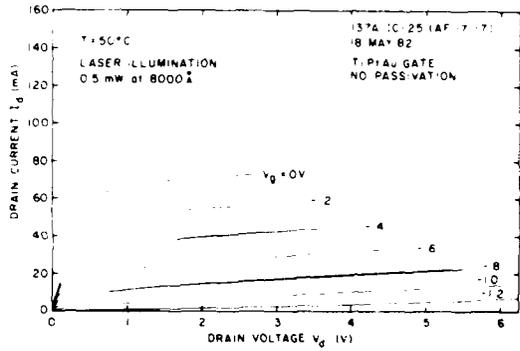
(a)  $T = 100^{\circ}\text{C}$ .



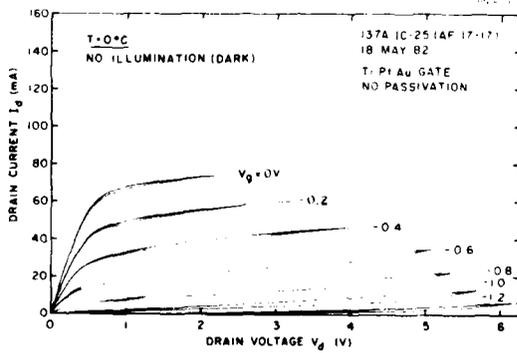
(b)  $T = 100^{\circ}\text{C}$ .



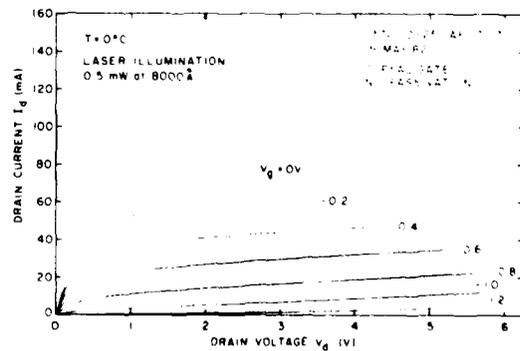
(c)  $T = 50^{\circ}\text{C}$ .



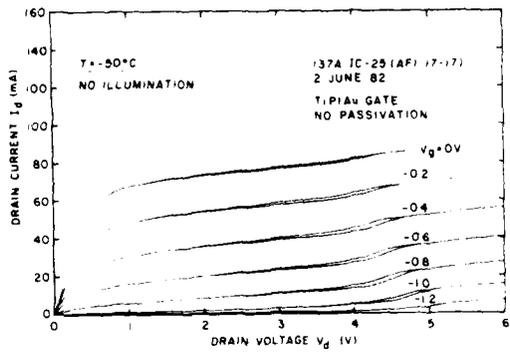
(d)  $T = 50^{\circ}\text{C}$ .



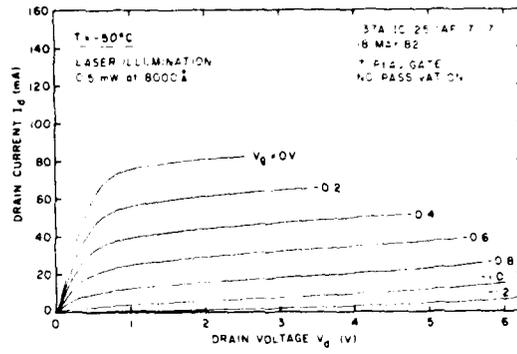
(e)  $T = 0^{\circ}\text{C}$ .



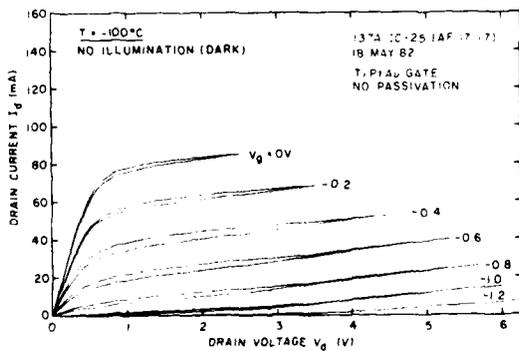
(f)  $T = 0^{\circ}\text{C}$ .



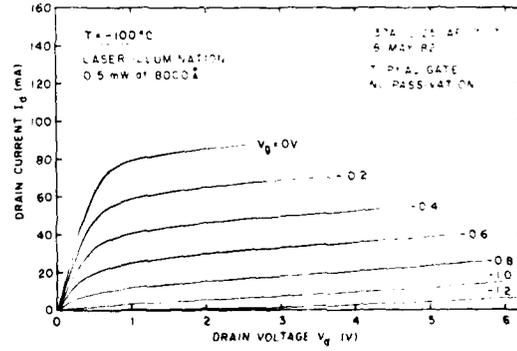
(g)  $T = -50^{\circ}\text{C}$ .



(h)  $T = -50^{\circ}\text{C}$ .

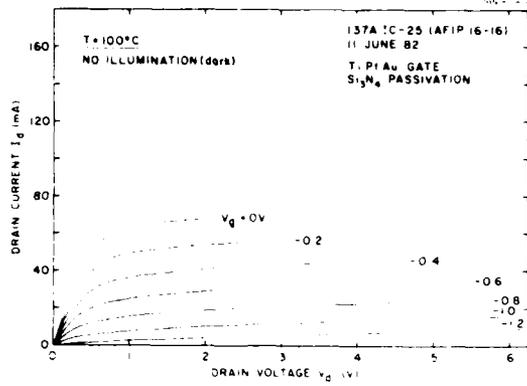


(i)  $T = -100^{\circ}\text{C}$ .

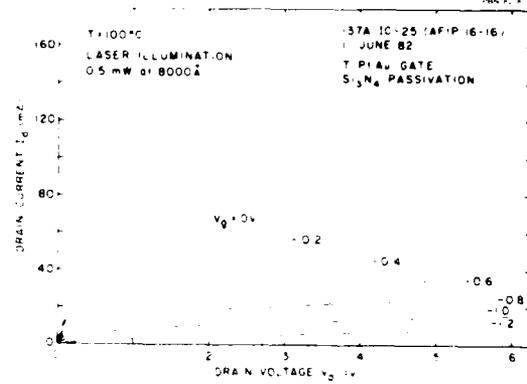


(j)  $T = -100^{\circ}\text{C}$ .

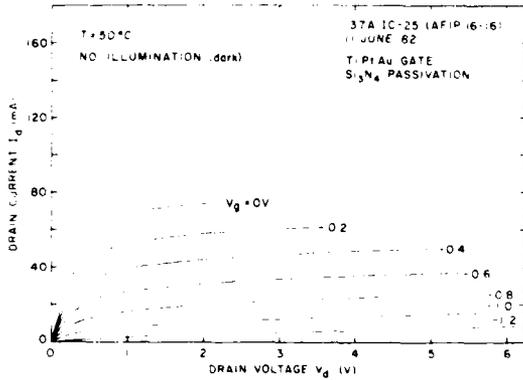
Figure 4-13. Effect of temperature and laser illumination on I-V characteristics of an FET with a TiPtAu gate and no passivation (wafer 137A-IC525).



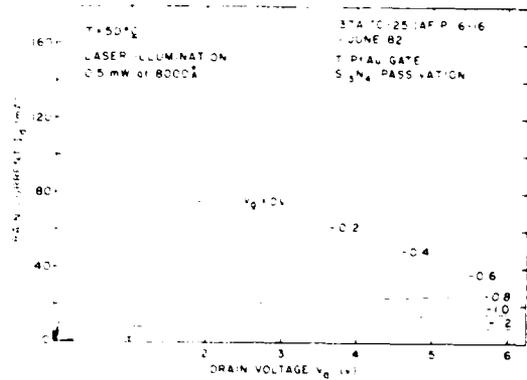
(a)  $T = 100^{\circ}\text{C}$ .



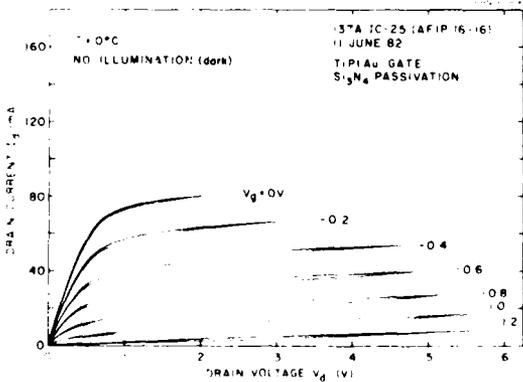
(b)  $T = 100^{\circ}\text{C}$ .



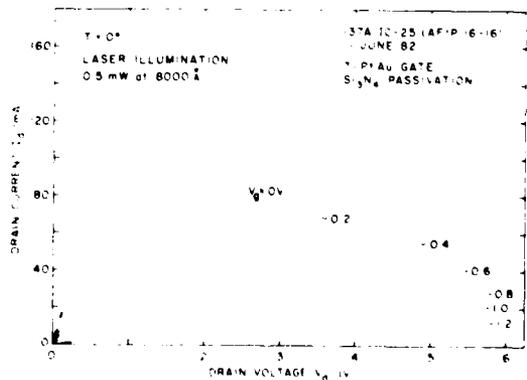
(c)  $T = -50^{\circ}\text{C}$ .



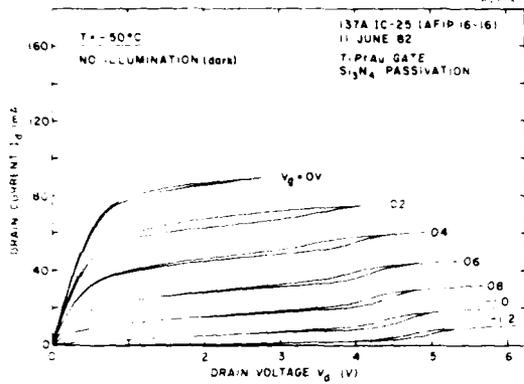
(d)  $T = -50^{\circ}\text{C}$ .



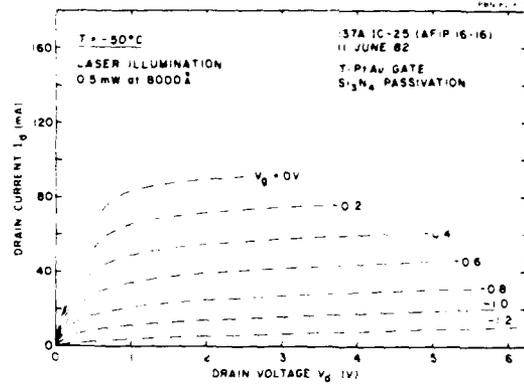
(e)  $T = 0^{\circ}\text{C}$ .



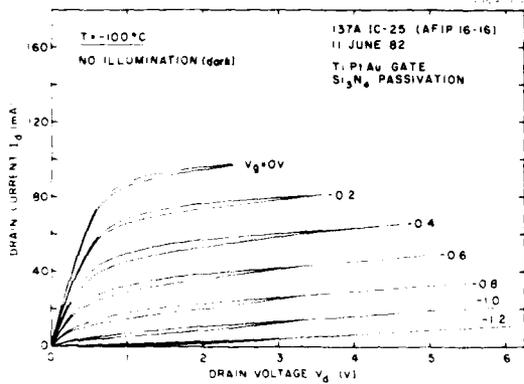
(f)  $T = 0^{\circ}\text{C}$ .



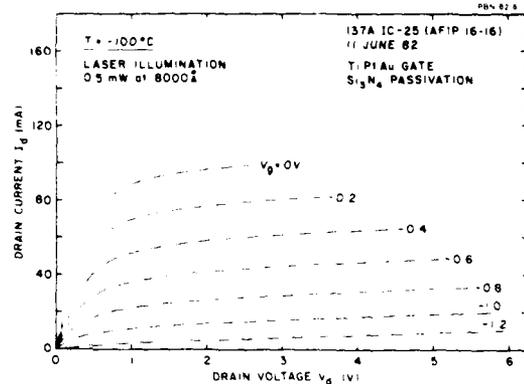
(g) T = -50°C.



(h) T = -50°C.

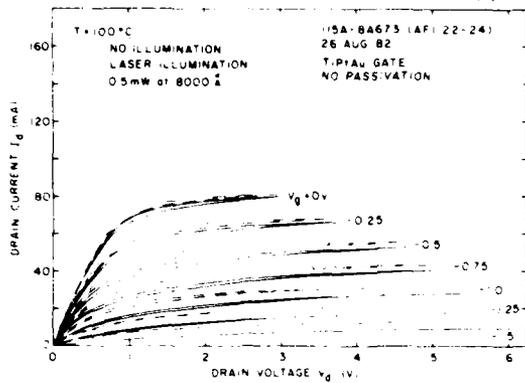


(i) T = -100°C.

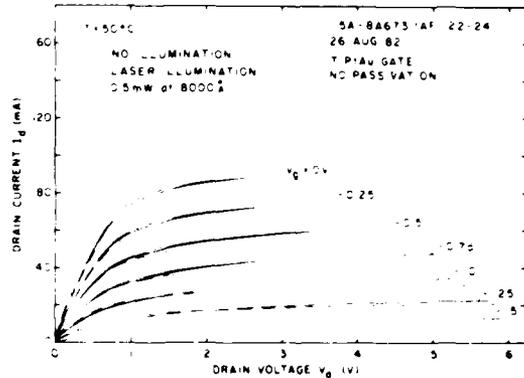


(j) T = -100°C.

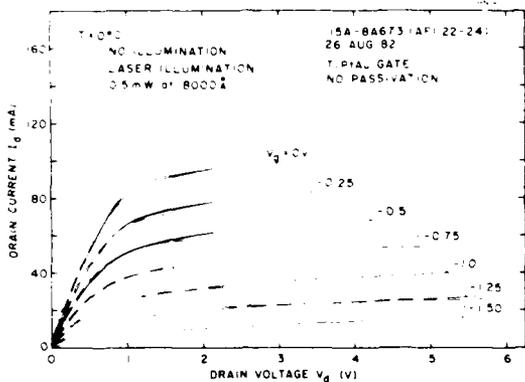
Figure 4-14. Effect of temperature and laser illumination on I-V characteristics of an FET with a TiPtAu gate and Si<sub>3</sub>N<sub>4</sub> passivation (wafer 137A-IC525).



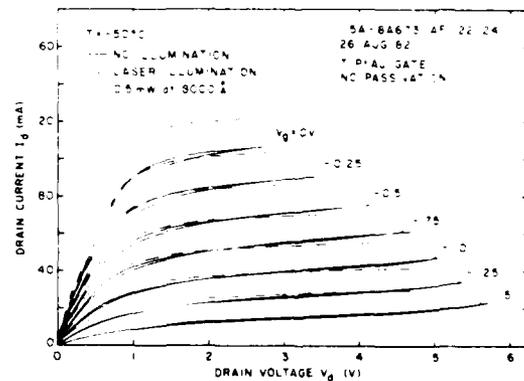
(a)  $T = 100^{\circ}\text{C}$ .



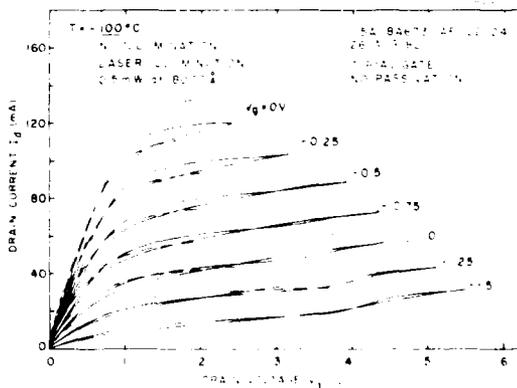
(b)  $T = 50^{\circ}\text{C}$ .



(c)  $T = 0^{\circ}\text{C}$ .

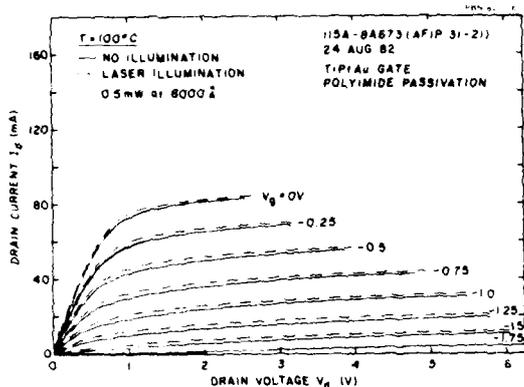


(d)  $T = -50^{\circ}\text{C}$ .

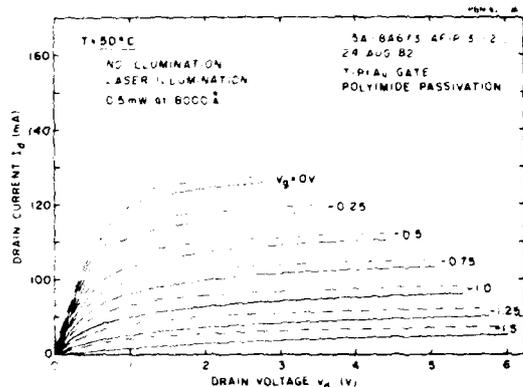


(e)  $T = -100^{\circ}\text{C}$ .

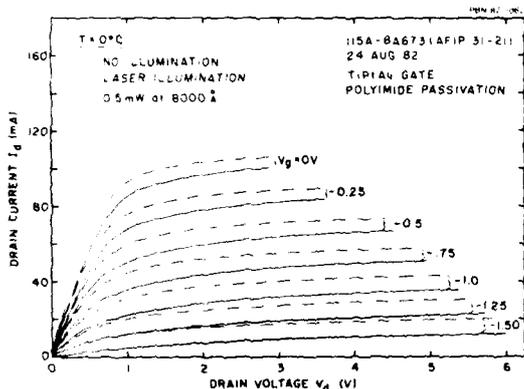
Figure 4-15. Effect of temperature and laser illumination on I-V characteristics of an FET with a TiPtAu gate and no passivation (wafer 115A-8A673).



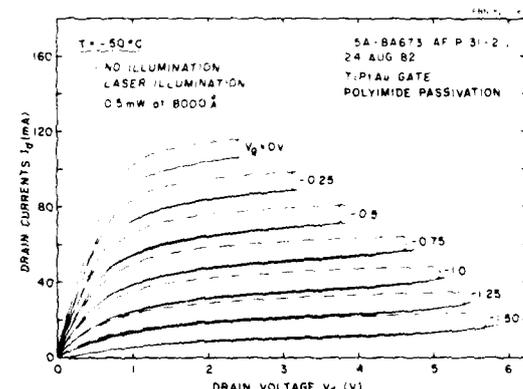
(a)  $T = 100^{\circ}\text{C}.$



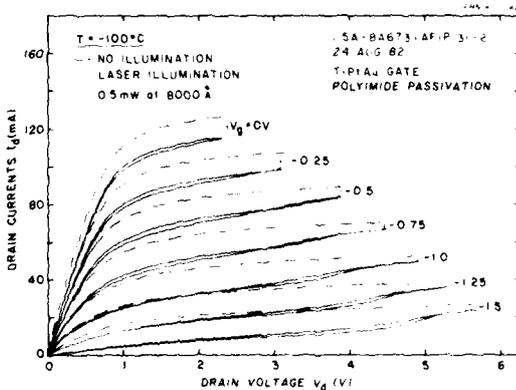
(b)  $T = 50^{\circ}\text{C}.$



(c)  $T = 0^{\circ}\text{C}.$



(d)  $T = -50^{\circ}\text{C}.$



(e)  $T = -100^{\circ}\text{C}.$

Figure 4-16. Effect of temperature and laser illumination on I-V characteristics of an FET with a TiPtAu gate and polyimide passivation (115A-8A673).

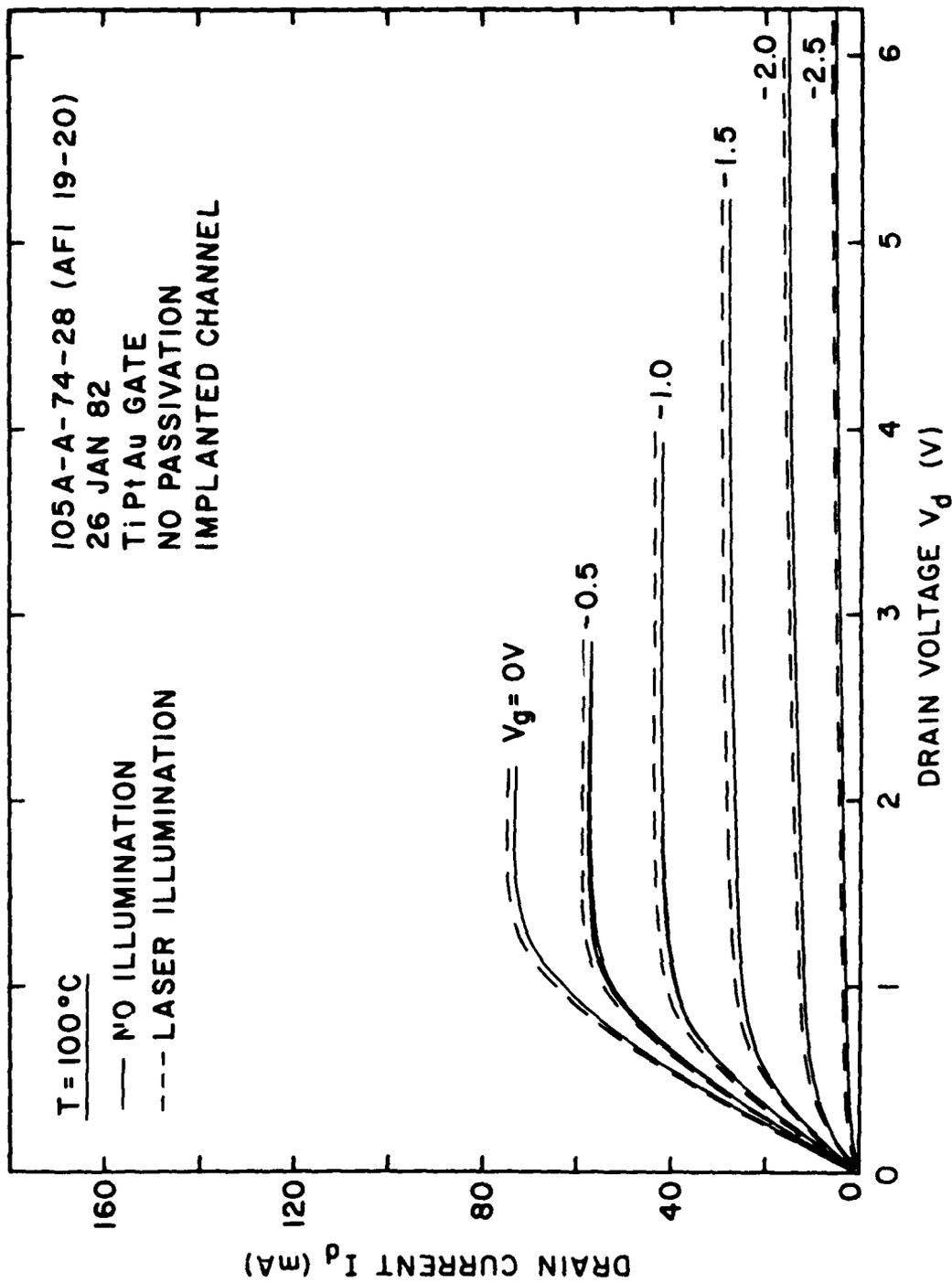


Figure 4-17. Effect of laser illumination on I-V characteristics of an FET with a TiPtAu gate, no passivation, and an implanted channel (wafer 105A-A-74-28).

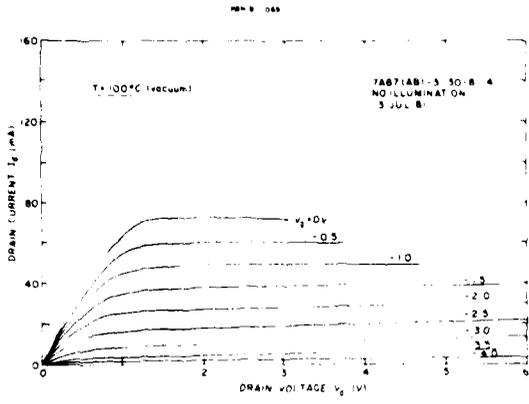
#### 4.3.2 Ungated devices with and without $\text{SiO}_x$ passivation (wafer 89A-8A653)

The baseband noise data corresponding to this case is displayed in Fig. 4-19 and 4-20. At first glance, the feature that is most evident in both sets of graphs is the decreasing effect of laser illumination on the noise as the temperature is increased. This behavior is consistent with the changes observed in the drain current. That is to say, as more traps are being emptied, a random process, more fluctuations are expected in the drain current. When all possible traps are emptied, such as at high temperature, or with laser illumination, carrier density fluctuation noise will be a maximum, as the graphs show.

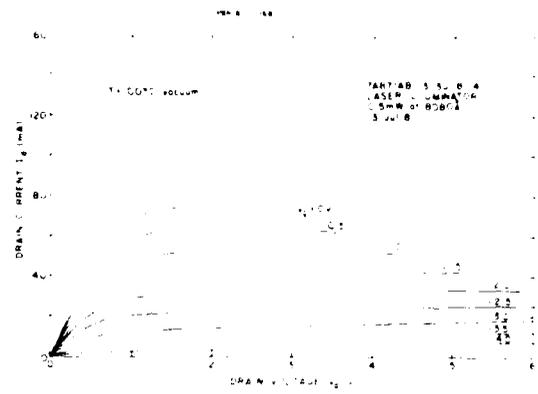
A second obvious feature is the non- $1/f$  dependence of the noise, especially under laser illumination. It is well known that a variety of conditions will lead to a  $1/f$  dependence (or an approximation thereof). One such condition is that the trap levels be densely and uniformly distributed in energy<sup>24</sup>. This condition is most likely approximated with surface states than with bulk states. Other conditions, more difficult to justify, apply to bulk states.<sup>25</sup> We conclude, therefore, that some of the noise is probably contributed by electrons making transitions from traps residing in the bulk. These, of course, can be excited thermally, and in our case, optically, also, because of the penetration depth of the laser beam. Evidence to be shown later, when FM noise is discussed, will suggest that the component of baseband noise not following a  $1/f$  law is probably not affecting the depletion layer under the gate.

When a comparison is made between the results for the passivated and unpassivated case, a remarkable difference emerges. Note that the noise level for the passivated case is about an order of magnitude higher than for the unpassivated case, despite the fact that the drain current is about a factor of four lower. This strongly suggests that the oxide trap levels are contributing heavily to the noise. Again, microwave noise measurements will support this hypothesis.

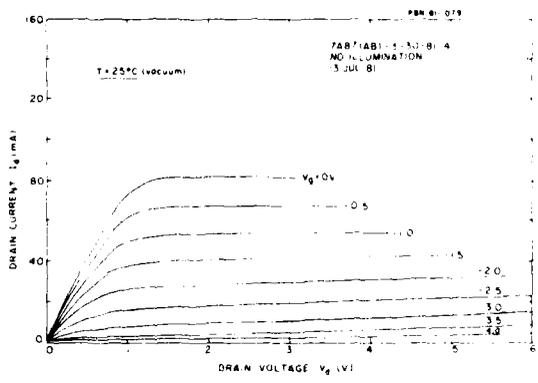
Notice that at some temperatures the curves cross. We do not have an explanation for this peculiar behavior. This cross-over phenomenon also occurs for some, but not all, gated devices.



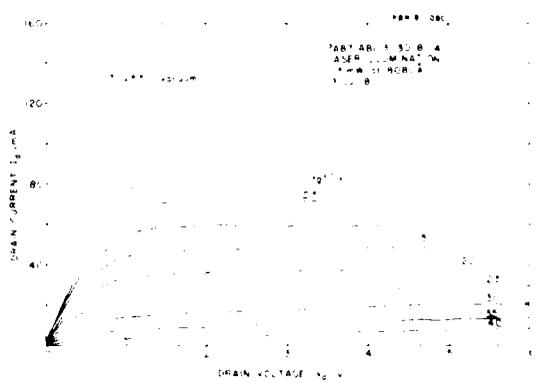
(a)  $T = 100^\circ\text{C}$ .



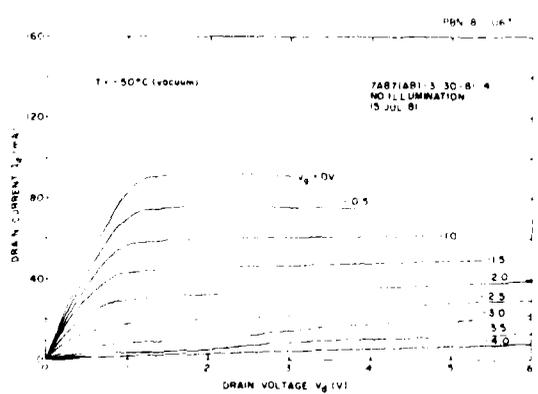
(b)  $T = 100^\circ\text{C}$ .



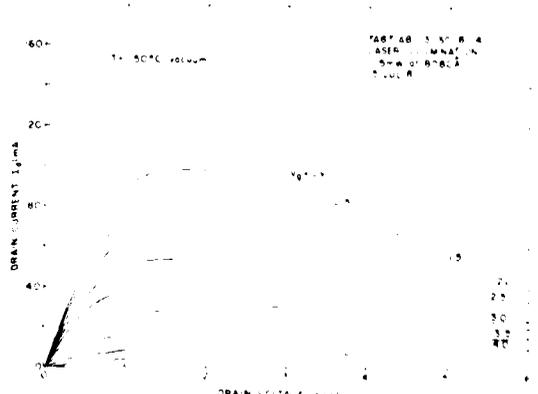
(c)  $T = 25^\circ\text{C}$ .



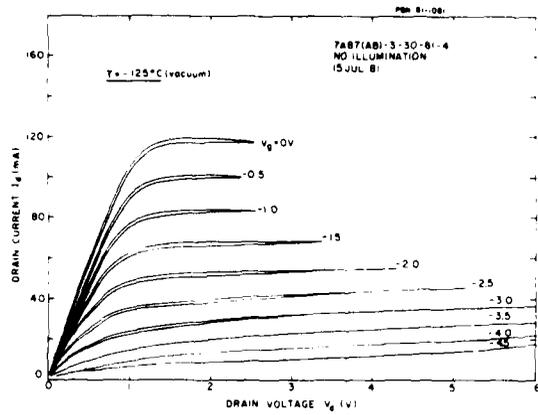
(d)  $T = 25^\circ\text{C}$ .



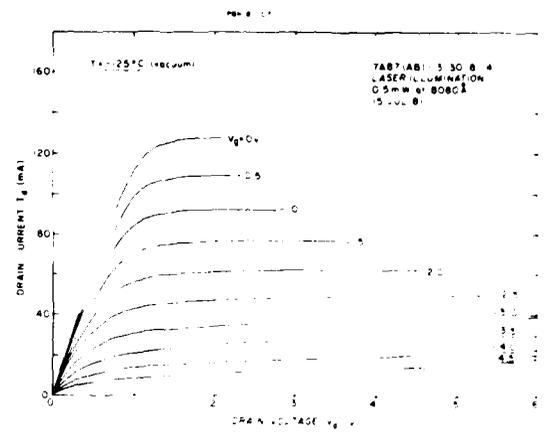
(e)  $T = -50^\circ\text{C}$ .



(f)  $T = 50^\circ\text{C}$ .

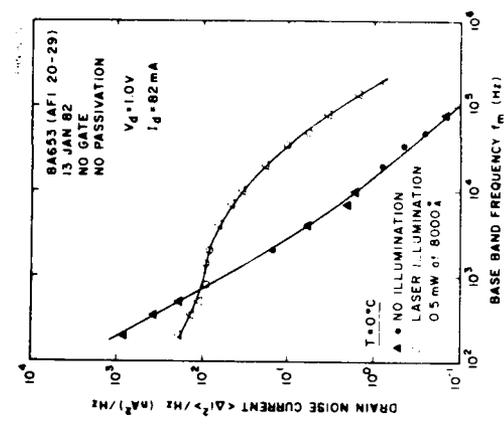


(g)  $T = -125^{\circ}\text{C}$ .

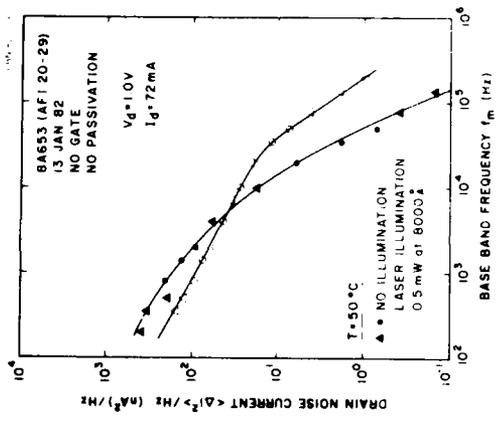


(h)  $T = -125^{\circ}\text{C}$ .

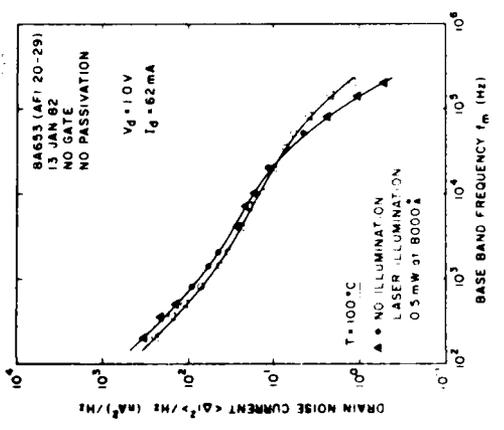
Figure 4-18. Effect of temperature and laser illumination on I-V characteristics of an FET with Al gate and no passivation (wafer 7A87(AB))



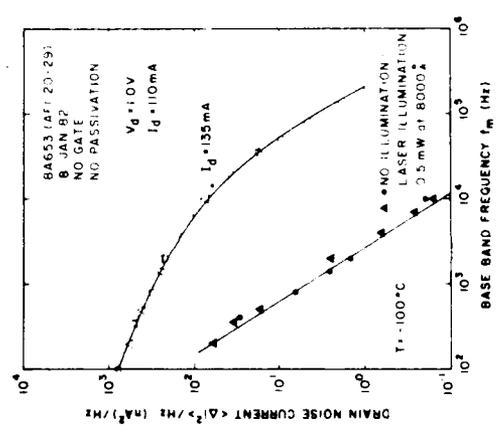
(a)  $T = 0^\circ\text{C}$ .



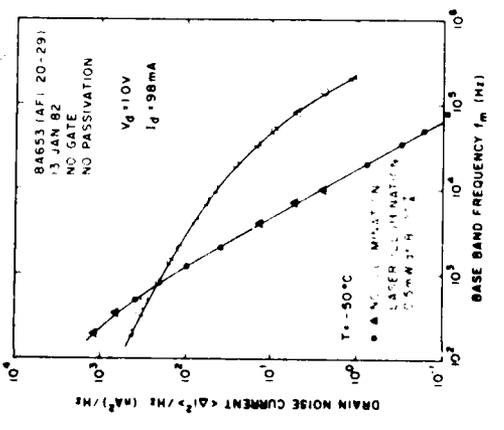
(b)  $T = 50^\circ\text{C}$ .



(c)  $T = 100^\circ\text{C}$ .

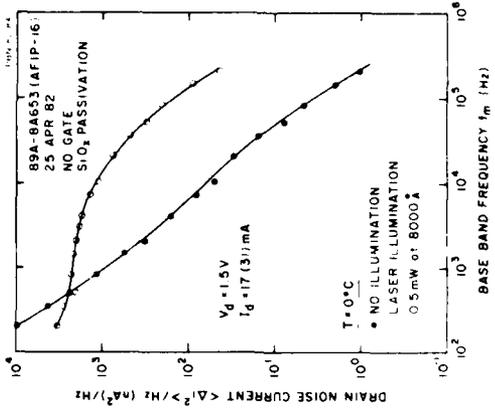


(d)  $T = -50^\circ\text{C}$ .

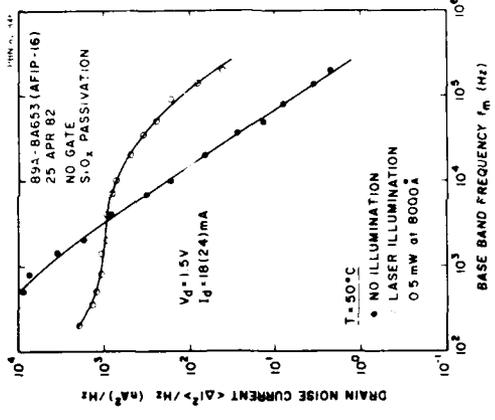


(e)  $T = -100^\circ\text{C}$ .

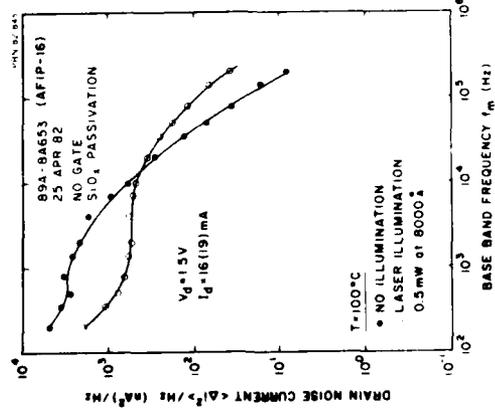
Figure 4-19. Effect of temperature and laser illumination on baseband noise of a gateless FET with no passivation (wafer 89A-8A653).



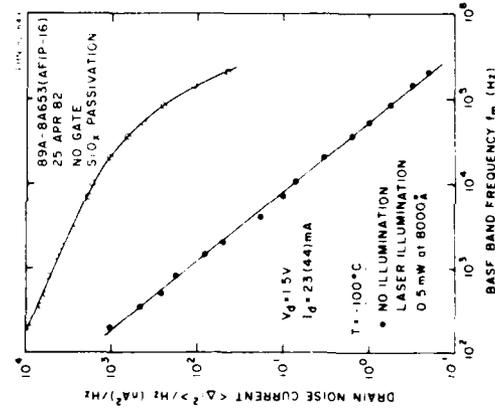
(a)  $T = 100^\circ\text{C}$ .



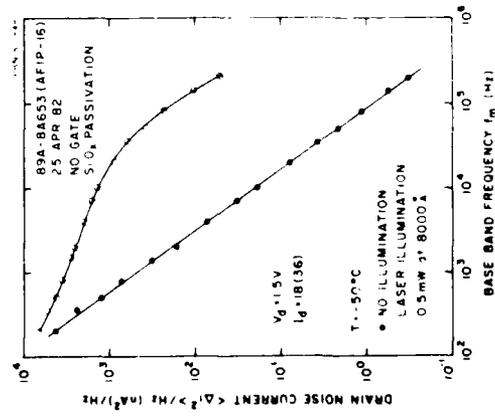
(b)  $T = 50^\circ\text{C}$ .



(c)  $T = 0^\circ\text{C}$ .



(d)  $T = -50^\circ\text{C}$ .



(e)  $T = -100^\circ\text{C}$ .

Figure 4-20. Effect of temperature and laser illumination on baseband noise of gateless FET with SiO<sub>2</sub> passivation (wafer 89A-8A653).

#### 4.3.3 FET with a CrAu gate and with and without $\text{SiO}_x$ passivation (wafer 89A-8A653)

These results, shown in Fig. 4-21 and 4-22, resemble those for the ungated structures. However, the increase in noise when passivation is added is not as pronounced. This is probably due to the fact that a smaller fraction of the source-drain region is covered with  $\text{SiO}_x$ , and in particular, the critical region under the gate is not covered. We do not have an explanation for the dip or "kink" in the curves for  $T = 0^\circ \text{C}$  in Fig. 4-21(c) and 4-21(d).

#### 4.3.4 FET with TiPtAu gate and with and without $\text{SiO}_x$ passivation (wafer 91A-8A661)

These results, shown in Fig. 4-23 and 4-24, resemble the preceding curves, thus, a change of gate metallization from CrAu to TiPtAu has no noticeable effect on the noise, just as for the case of the I-V characteristics.

#### 4.3.5 FET with a TiPtAu gate and with and without $\text{Si}_3\text{N}_4$ passivation (wafer 137A-1C25)

Again the general features of the baseband noise curves, shown in Fig. 4-25 and 4-26, resemble the preceding curves qualitatively. However, one important difference exists. The noise is significantly lower with passivation than without. This implies two things; namely,  $\text{Si}_3\text{N}_4$  does not introduce negligible trap levels of its own, and  $\text{Si}_3\text{N}_4$  inhibits surface trap formation by the processing steps following passivation, or by the ambient, itself.

#### 4.3.6 FET with a TiPtAu gate and with and without polyimide passivation (wafer 115A-8A673)

Here again, as with  $\text{Si}_3\text{N}_4$  passivation, polyimide passivation either lowers the noise level, or at least does not increase it. See Fig. 4-27 and 4-28. The improvement is not as uniform over temperature as it was for  $\text{Si}_3\text{N}_4$  passivation.

#### 4.3.7 FET with a TiPtAu gate, no passivation, and an implanted channel (wafer 105A-A7428)

As was the case with I-V characteristics, Fig. 4-17, baseband noise data was only taken at  $T = 100^{\circ}\text{C}$ . See Fig. 4-29. Nothing unusual emerges from these experimental results.

#### 4.3.8 FET with an Al gate and no passivation (wafer 7A87(AB))

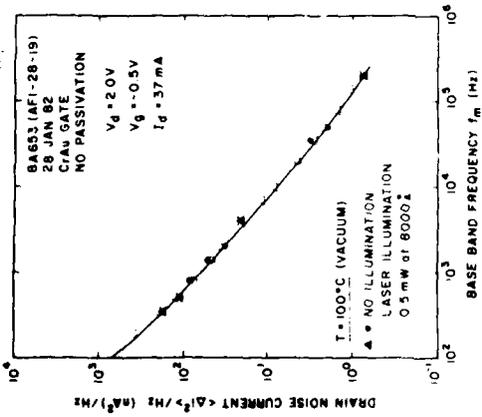
We have made some baseband noise measurements on devices with Al gates. These FETs, as stated earlier, were fabricated during the previous contract. The noise data is shown in Fig. 4-30. Generally speaking, the frequency dependence resembles that obtained for CrAu and TiPtAu gates. Two notable differences are evident, however. The first is that the noise level under non-illuminated conditions is lower (by as much as a factor of 10 at low temperatures) for these devices. This result is consistent with the observation that the I-V characteristics for this condition display less hysteresis. See Fig. 4-18. The second difference is that the increase in noise under illumination at low temperatures is greater than for the previous devices. In fact, under illumination, the noise level is not much different than the CrAu and TiPtAu cases. From these facts, it would appear that the trap levels for these older devices might be somewhat lower in the band gap than for the devices fabricated during the present contract.

This completes the presentation of the DC and low-frequency data. In the next section, the near-carrier FM noise measurements will be presented for a selected set of devices as listed in Table 3-1, last column.

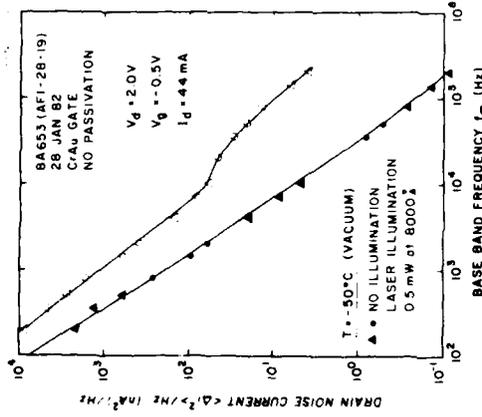
### 4.4 Near-Carrier FM Noise Measurements

#### 4.4.1 Introduction

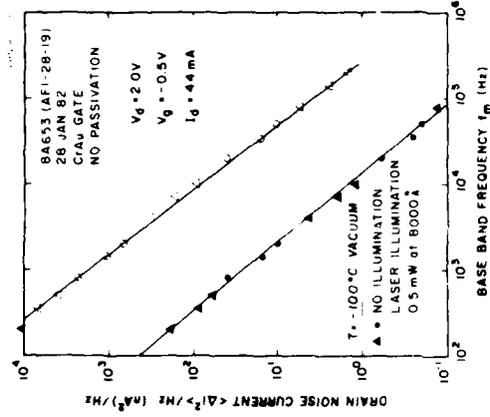
Noise measurements were made near the carrier of an oscillating FET as described in Sec. 3.2.2. Only FM noise was measured. Amplitude modulation noise in FETs, generally speaking, is negligible.



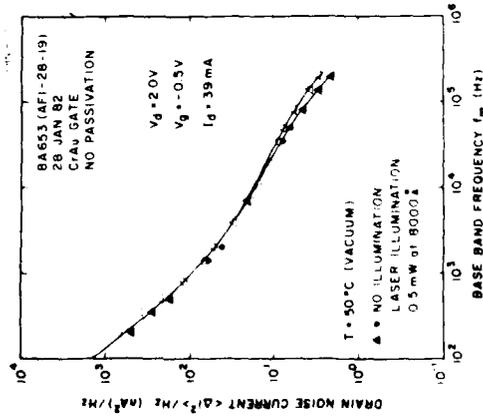
(a)  $T = 100^\circ\text{C}$ .



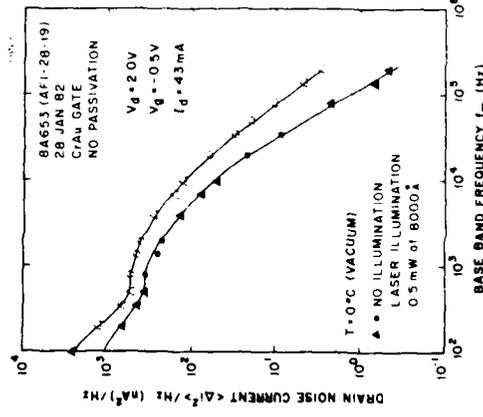
(b)  $T = 50^\circ\text{C}$ .



(c)  $T = 0^\circ\text{C}$ .

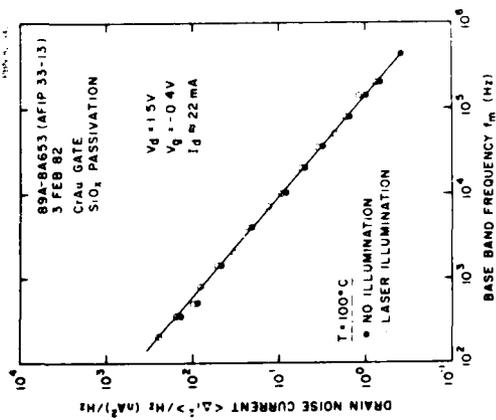


(d)  $T = -50^\circ\text{C}$ .

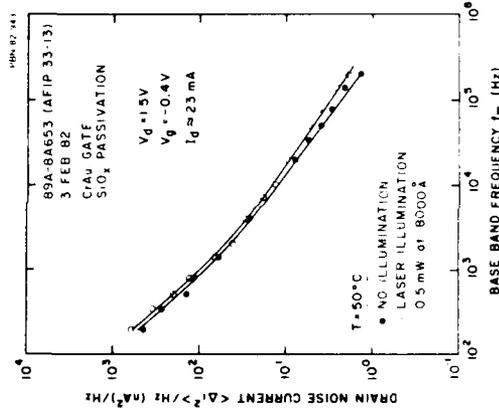


(e)  $T = -100^\circ\text{C}$ .

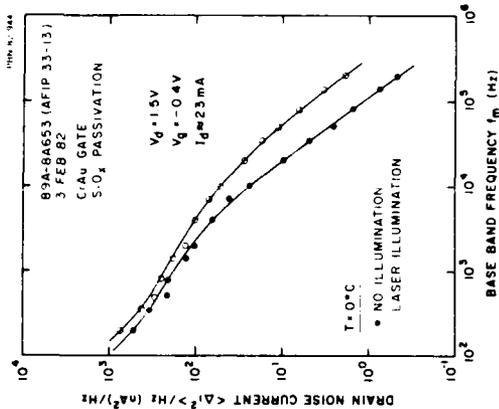
Figure 4-21. Effect of temperature and laser illumination on base-band noise of an FET with a CrAu gate and no passivation (wafer 89A-8A653).



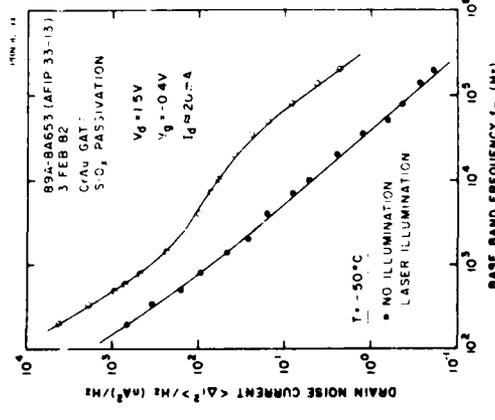
(a)  $T = 100^\circ C$ .



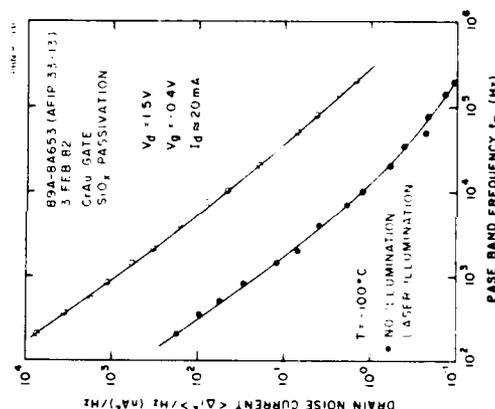
(b)  $T = 50^\circ C$ .



(c)  $T = 0^\circ C$ .

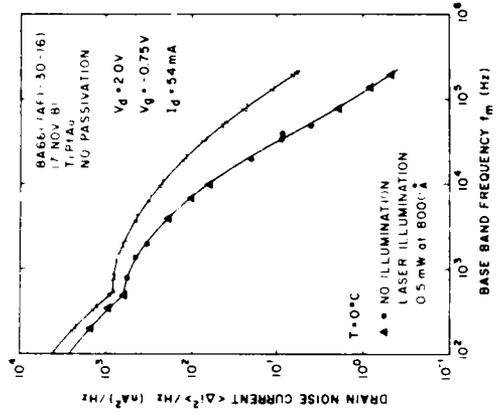


(d)  $T = -50^\circ C$ .

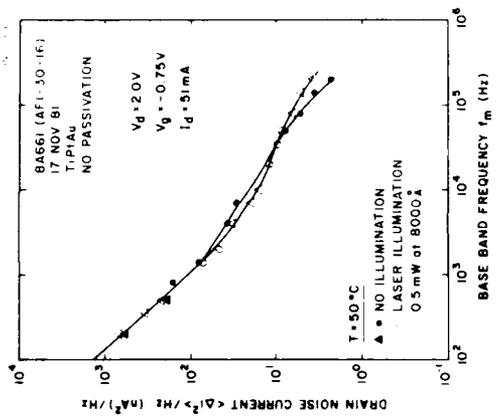


(e)  $T = -100^\circ C$ .

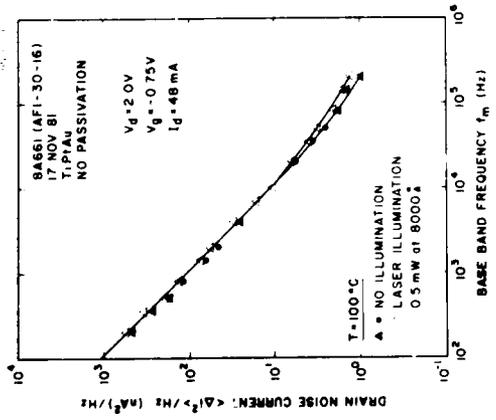
Figure 4-22. Effect of temperature and laser illumination on base-band noise of an FET with a CrAu gate and SiO<sub>2</sub> passivation (wafer 89A-8A653).



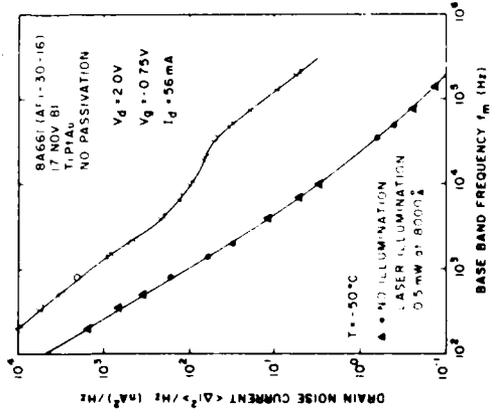
(a)  $T = 100^\circ\text{C}$ .



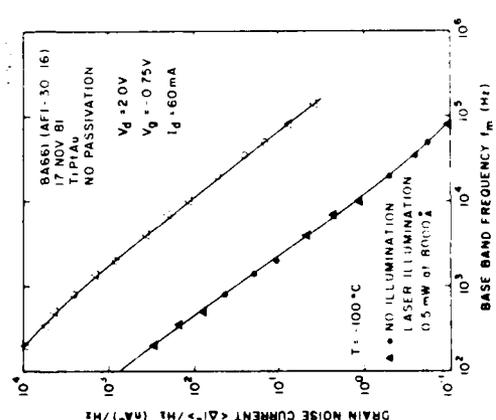
(b)  $T = 50^\circ\text{C}$ .



(c)  $T = 0^\circ\text{C}$ .



(d)  $T = -50^\circ\text{C}$ .



(e)  $T = -100^\circ\text{C}$ .

Figure 4-23. Effect of temperature on base-band noise of an FET with a TiPtAu gate and no passivation (wafer 91A-8A661).

AD-A126 792

FET (FIELD-EFFECT TRANSISTOR) NOISE STUDIES(U) RAYTHEON  
CO LEXINGTON MA R A PUCEL OCT 82 S-3147  
AFOSR-TR-83-0222 F49620-81-C-0052

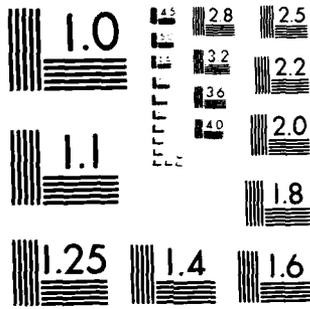
27

UNCLASSIFIED

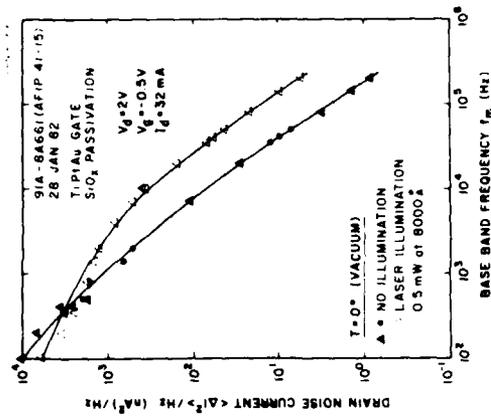
F/G 9/5

NL

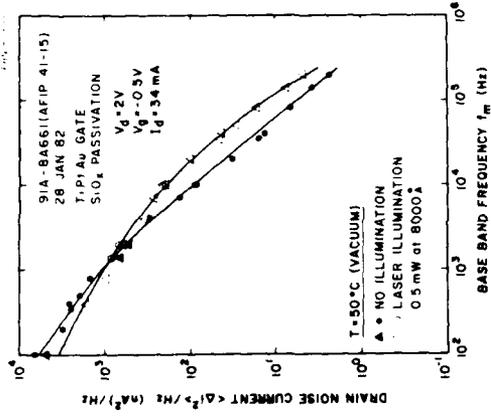

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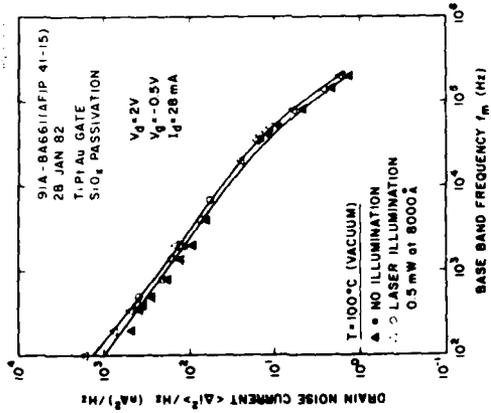
MICROCOPY RESOLUTION TEST CHART  
NATIONAL BUREAU OF STANDARDS 1963-A



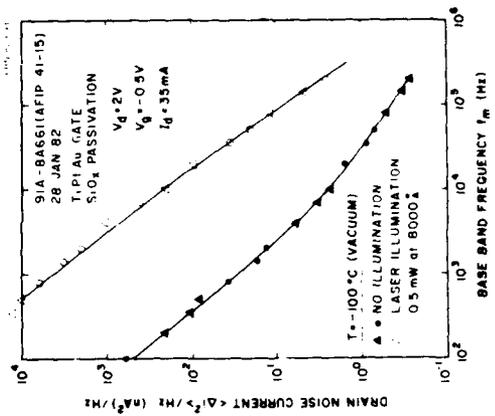
(c)  $T = 0^\circ\text{C}$ .



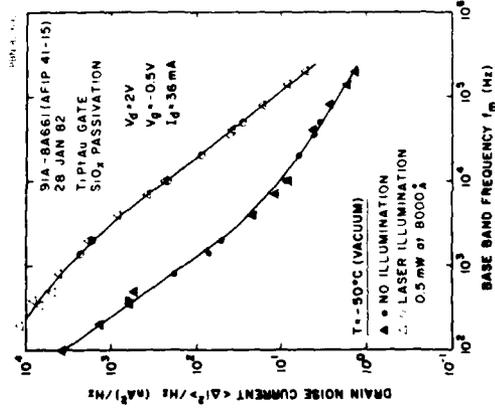
(b)  $T = 50^\circ\text{C}$ .



(a)  $T = 100^\circ\text{C}$ .

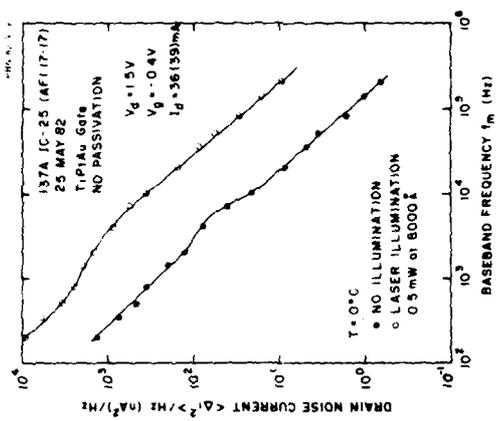


(e)  $T = -100^\circ\text{C}$ .

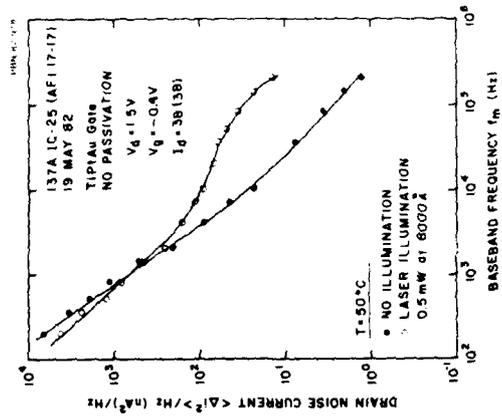


(d)  $T = -50^\circ\text{C}$ .

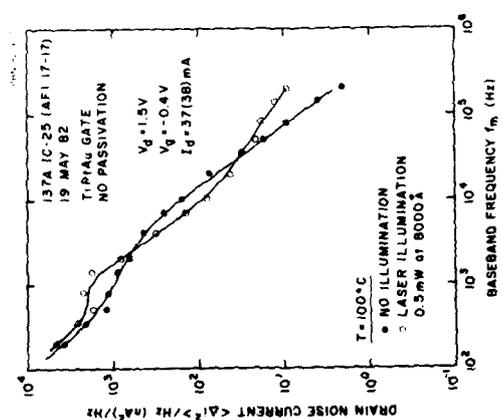
Figure 4-24. Effect of temperature and laser illumination on base-band noise of an FET with TiPtAu gate and SiO<sub>2</sub> passivation (wafer 91A-8A661).



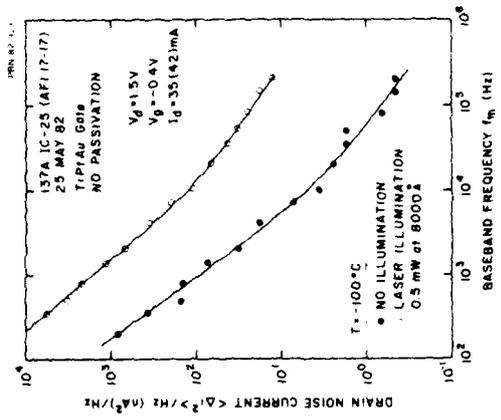
(a)  $T = 100^\circ\text{C}$ .



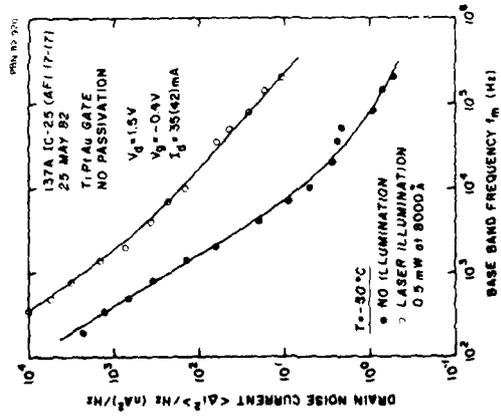
(b)  $T = 50^\circ\text{C}$ .



(c)  $T = 0^\circ\text{C}$ .

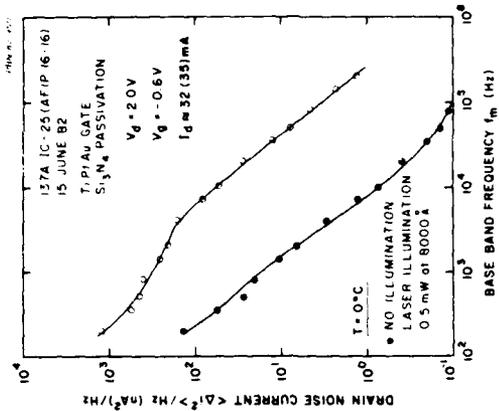


(d)  $T = -50^\circ\text{C}$ .

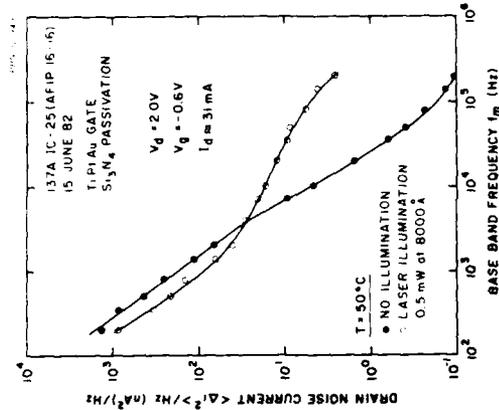


(e)  $T = -100^\circ\text{C}$ .

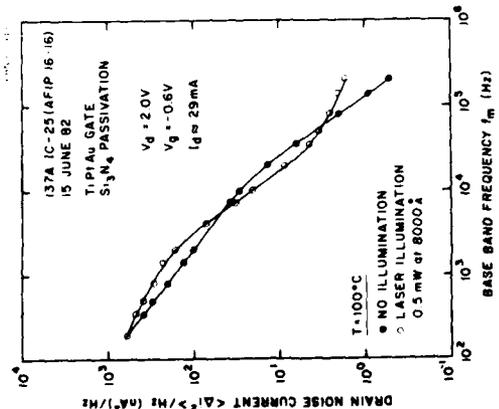
Figure 4-25. Effect of temperature and laser illumination on baseband noise of an FET with a TIPSu gate and no passivation (wafer 137A-IC25).



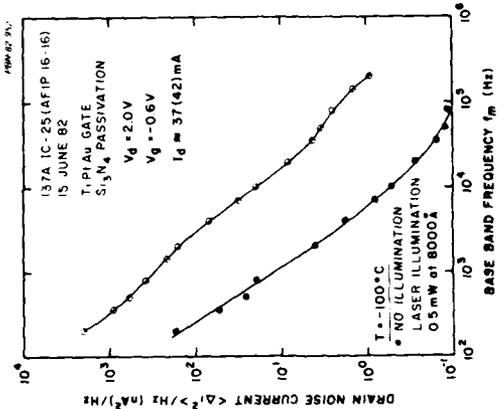
(c)  $T = 0^\circ\text{C}$ .



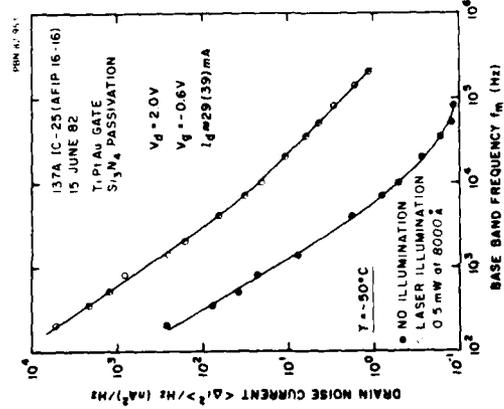
(b)  $T = 50^\circ\text{C}$ .



(a)  $T = 100^\circ\text{C}$ .

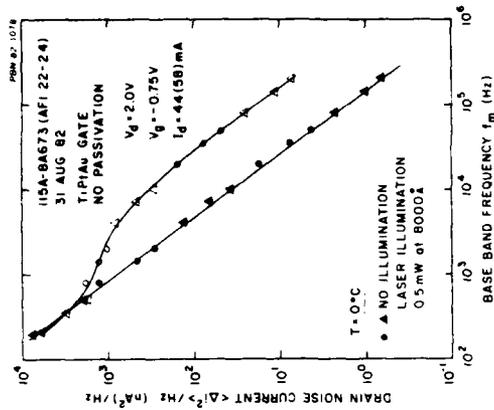


(e)  $T = -100^\circ\text{C}$ .

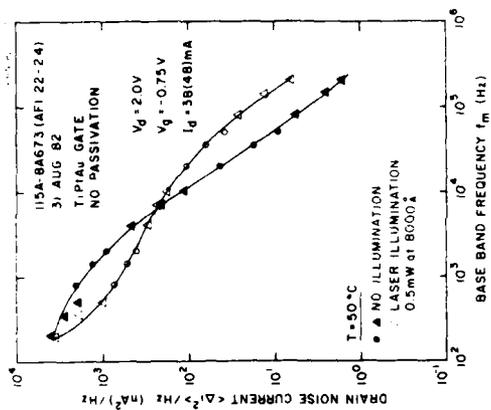


(d)  $T = -50^\circ\text{C}$ .

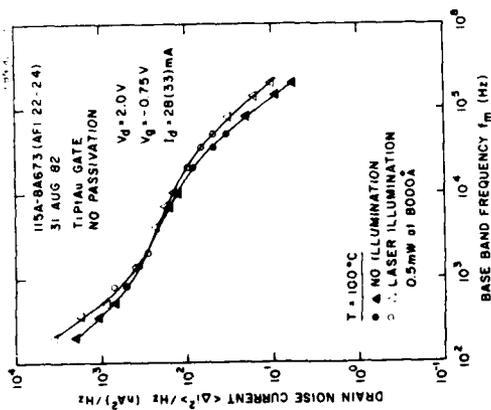
Figure 4-26. Effect of temperature and laser illumination on base-band noise of an FET with a TiPtAu gate and  $\text{Si}_3\text{N}_4$  passivation (wafer 137A-IC15).



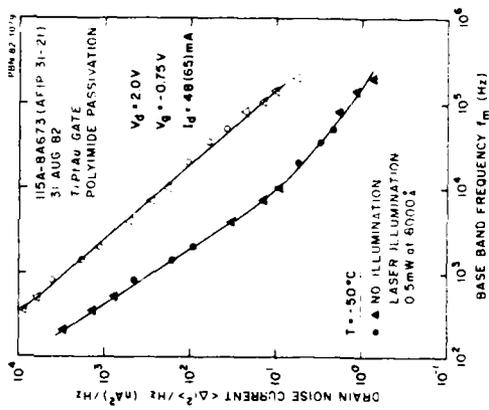
(c)  $T = 0^\circ\text{C}$ .



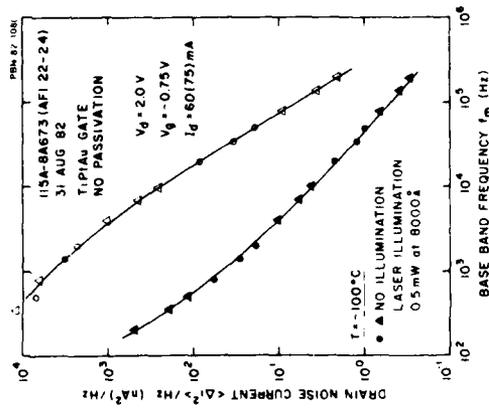
(b)  $T = 50^\circ\text{C}$ .



(a)  $T = 100^\circ\text{C}$ .

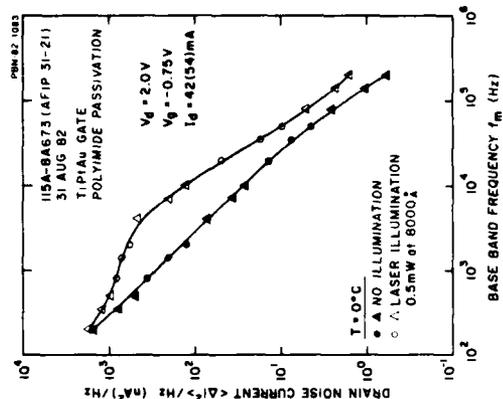


(e)  $T = -100^\circ\text{C}$ .

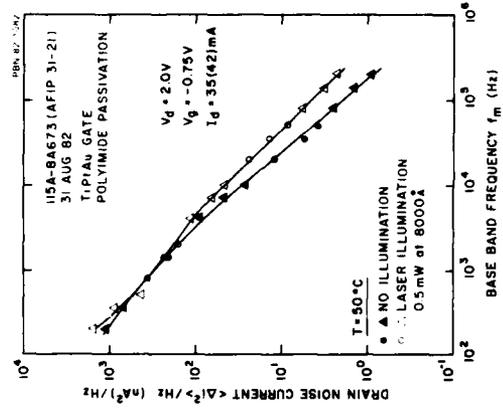


(d)  $T = -50^\circ\text{C}$ .

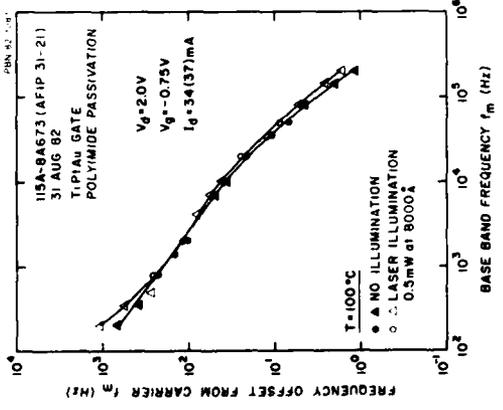
Figure 4-27. Effect of temperature and laser illumination on base-band noise of an FET with a TiPtAu gate and no passivation (wafer 115A-8A673).



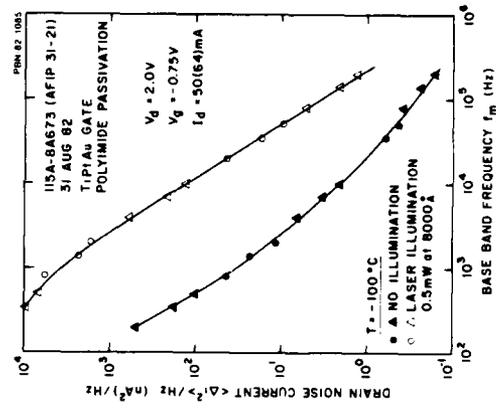
(c)  $T = 0^\circ\text{C}$ .



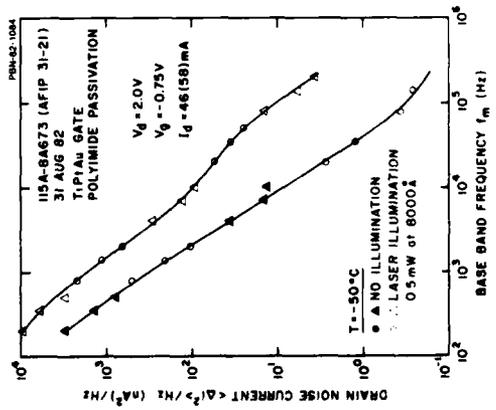
(b)  $T = 50^\circ\text{C}$ .



(a)  $T = 100^\circ\text{C}$ .



(e)  $T = -100^\circ\text{C}$ .



(d)  $T = -50^\circ\text{C}$ .

Figure 4-28. Effect of temperature and laser illumination on base-band noise of an FET with a TiPtAu gate and polyimide passivation.

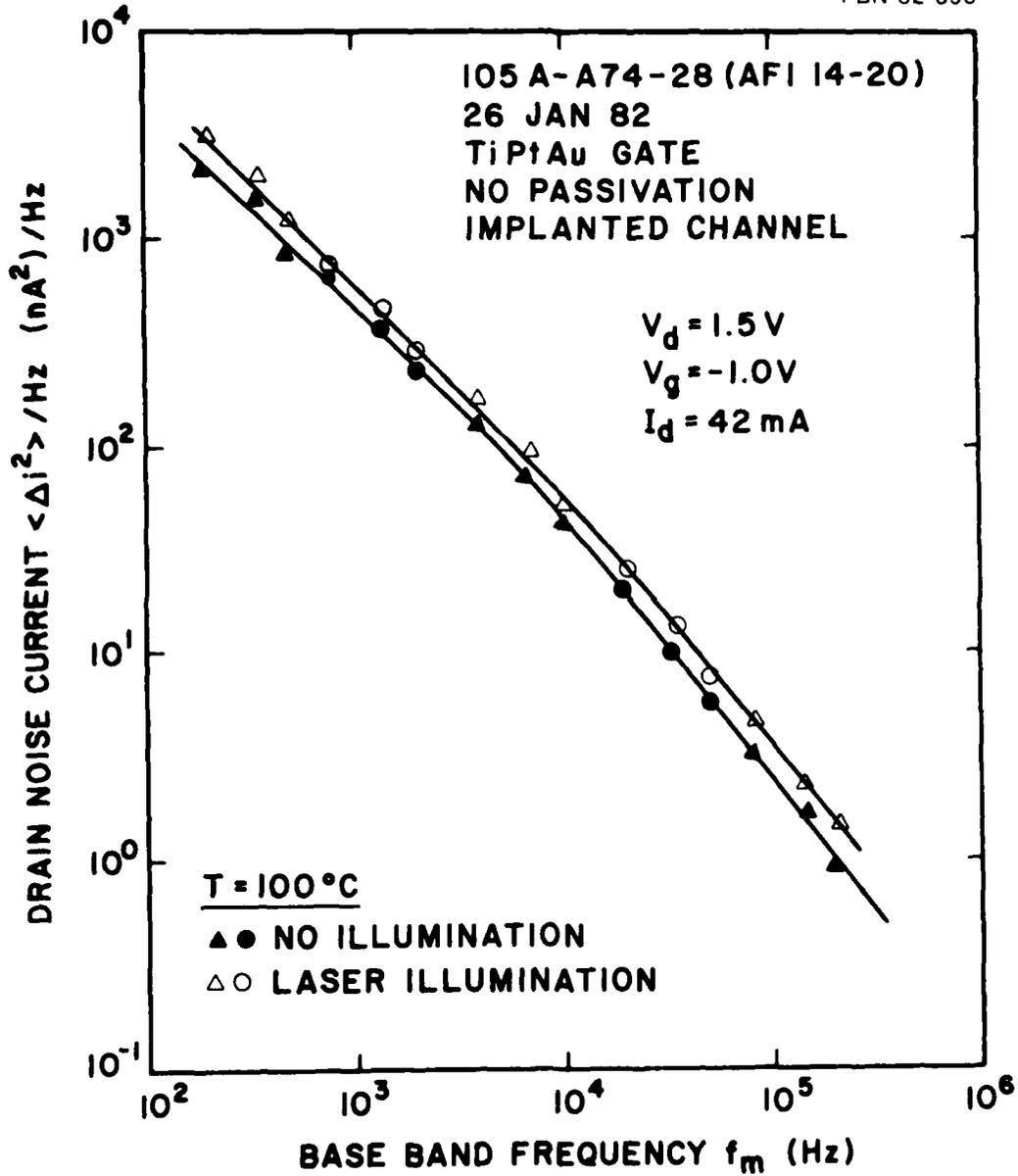
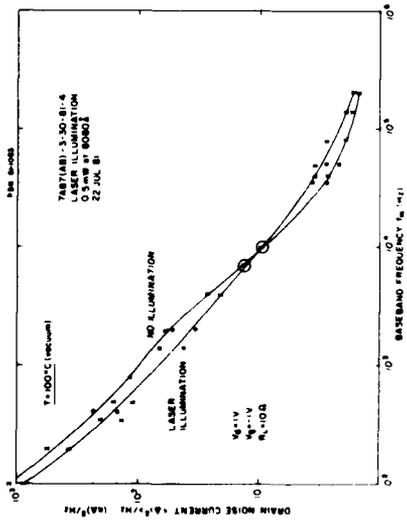
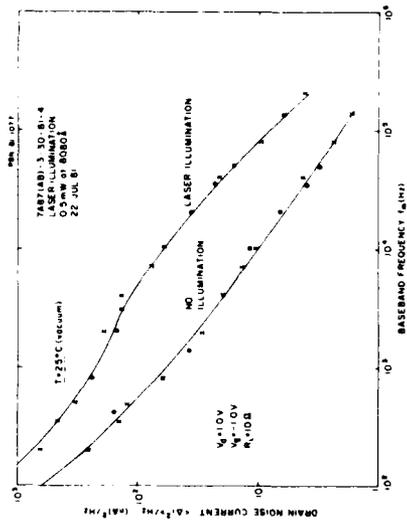


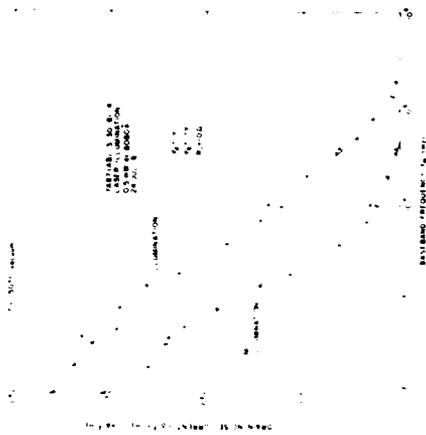
Figure 4-29. Effect of laser illumination on baseband noise of an FET with a TiPtAu gate, no passivation, and an implanted channel (wafer 105A-A7428).



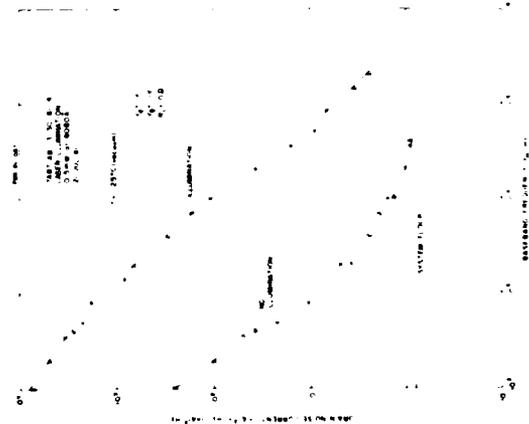
(a) T = 100°C.



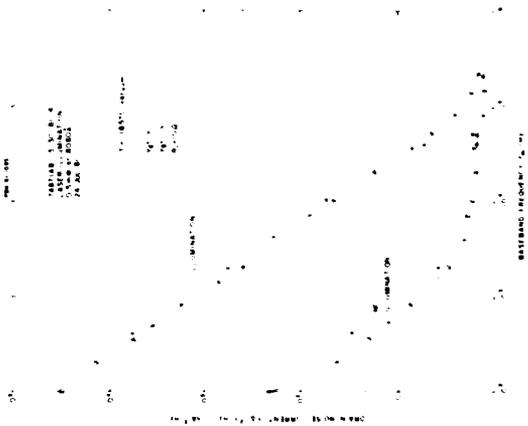
(b) T = 25°C.



(c) T = -50°C.



(d) T = -125°C.



(e) T = -185°C.

Figure 4-30. Effect of temperature and laser illumination on baseband noise of an FET with an Al gate (wafer 7A87(AB)).

According to theory, the FM noise-to-carrier ratio follows the law described by Eq. 3(b), repeated here for convenience, namely,

$$\left(\frac{N}{C}\right)_{\text{FM}} = \left(\frac{N_b(f_m)B}{P_o}\right) \left(\frac{f_o}{Q_L}\right)^2 \frac{1}{f_m^2} \quad (3b)$$

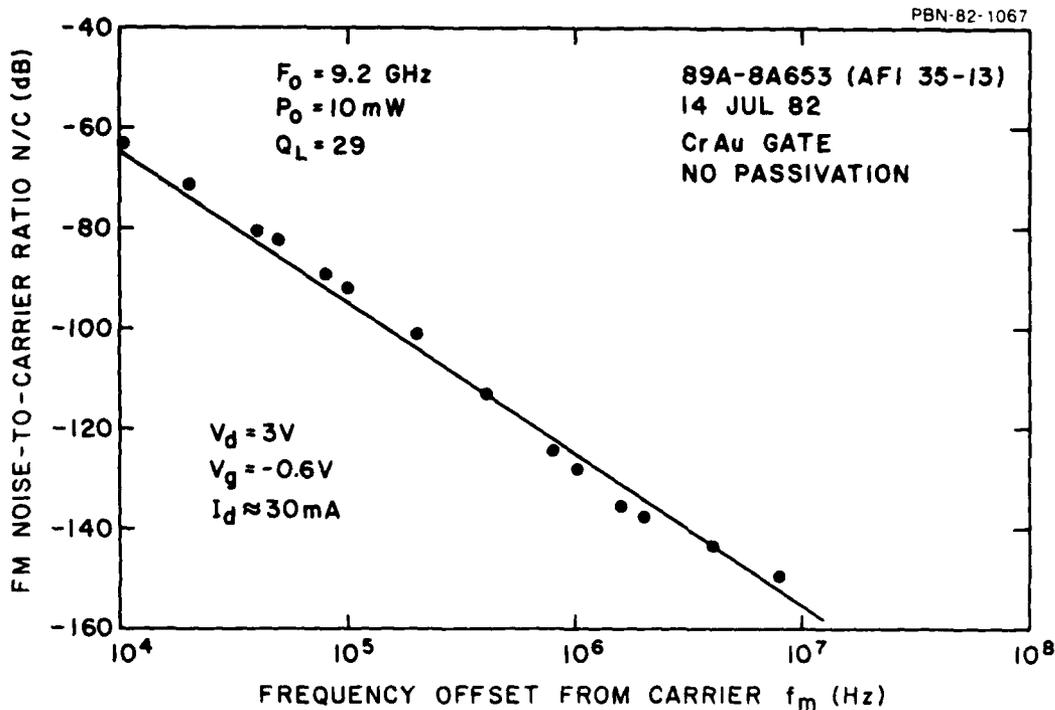
where  $B$  is the noise measurement bandwidth in Hertz,  $P_o$  is the oscillator power,  $f_o$  the carrier frequency,  $Q_L$  the loaded Q-factor of the oscillator circuit, and  $f_m$  the frequency offset from the carrier.

The noise parameter  $N_b(f_m)$  depends on the type of noise present. For thermal or "white" noise,  $N_b = \text{constant}$ , and  $N/C$  varies as  $1/f_m^2$ . On the other hand, for upconverted  $1/f$  noise,  $N_b \sim 1/f_m$ , and  $N/C$  varies as  $1/f_m^3$ . For a more general frequency dependence of baseband noise,  $N_b$  corresponds only to that component of this noise which is up-converted to the oscillator band.

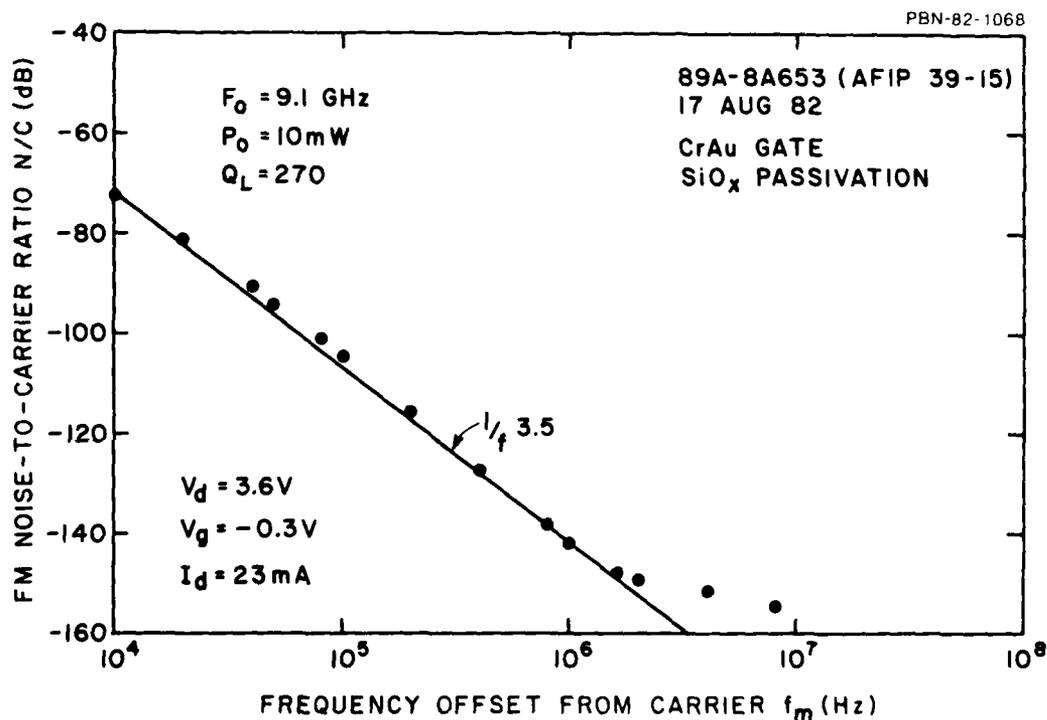
#### 4.4.2 FET with CrAu gate and with and without $\text{SiO}_x$ passivation

Figure 4-31 is a graph of the noise-to-carrier ratio. For this case, the device was biased at a higher drain voltage than was the case for baseband noise. This was necessary so that sufficient oscillator signal would be available for analysis. All noise measurements were taken at room temperature and without laser illumination.

Although a direct comparison of the noise levels for the passivated and unpassivated cases is not meaningful because of the large difference in loaded Q-factor, nevertheless, the data is significant in that it illustrates the frequency dependence of the near-carrier noise. (This, and the data to follow, will be presented again, later, in normalized form which will allow us to make a direct comparison of the noise levels.)



(a) No passivation.



(b)  $\text{SiO}_x$  passivation.

Figure 4-31. FM N/C ratio vs. frequency offset from carrier for oscillating FET with CrAu gate and with and without  $\text{SiO}_x$  passivation.

What is important to note in Fig. 4-31 is that in both cases the noise data follow a simple law, unlike the baseband noise. See Fig. 4-21 and 4-22. The unpassivated noise data varies at  $1/f_m^3$ . A stronger dependence is displayed by the passivated device.

It is evident that not all of the baseband noise is being upconverted to the oscillator band, otherwise the simple power law dependence of the near-carrier noise would not be obtained\*. Since the upconversion takes place via depletion layer modulation under the gate, it follows that the more complex frequency dependence observed in the baseband noise is most likely contributed by traps outside of the gate depletion region. For example, in the region defining  $R_S$ . See Fig. 4-10.

#### 4.4.3 FET with TiPtAu gate with and without $SiO_x$ passivation

A near true  $1/f$  dependence is obtained for both the unpassivated and passivated cases as is evident from Fig. 4-32.

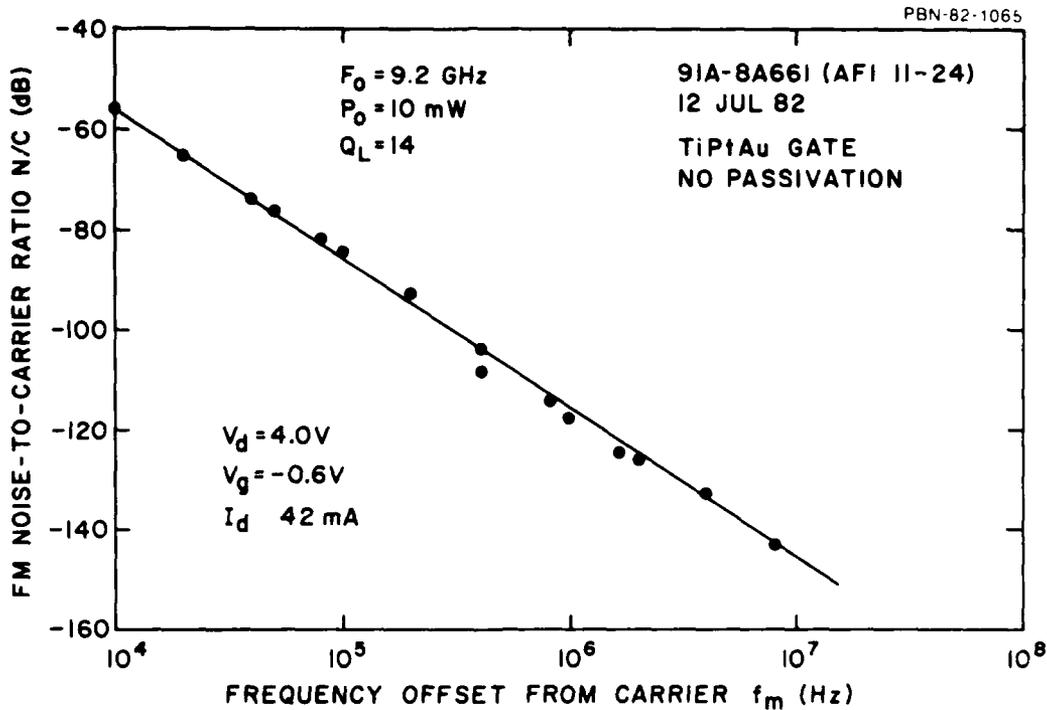
#### 4.4.4 FET with TiPtAu gate with and without $Si_3N_4$ passivation

Silicon nitride passivation does not affect the  $1/f$  dependence of the near-carrier noise, either. See Fig. 4-33. In fact, the passivated device data clusters around the  $1/f^3$  line more closely than the unpassivated device data. Note the extremely low level of noise. The results depicted here represent an improvement in FM noise performance in excess of 20 dB over any corresponding result reported in the literature to date for FET oscillators with this loaded Q-factor.

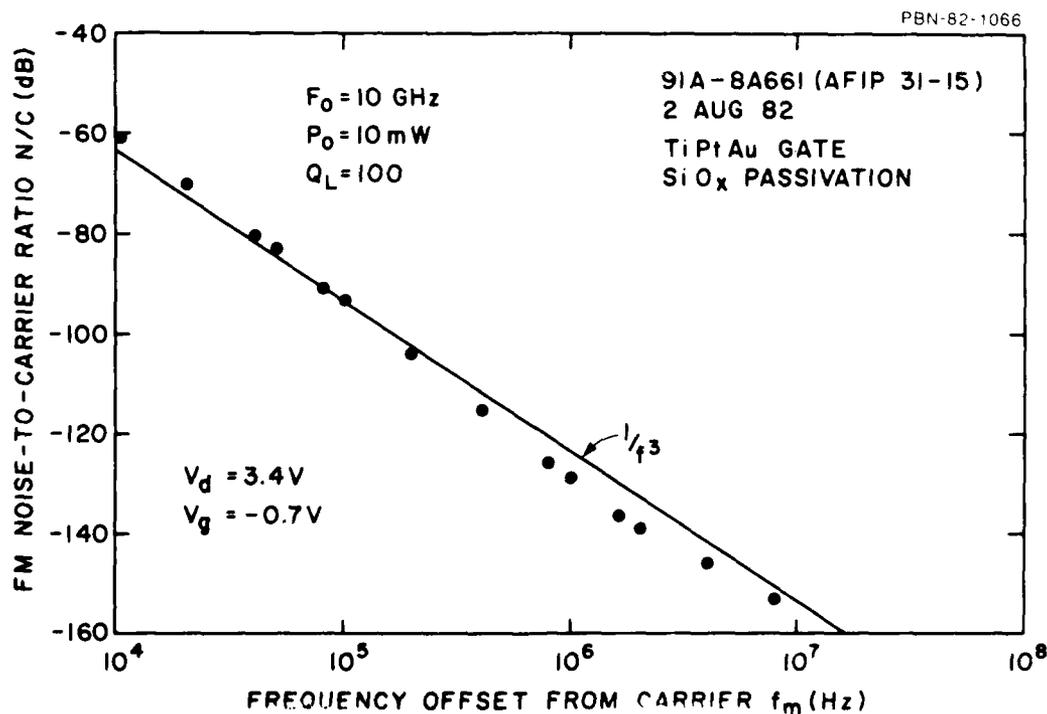
#### 4.4.5 FET with a TiPtAu gate and with and without polyimide passivation

Near-carrier noise measured on a polyimide device is shown in Fig. 4-34. Some deviation from a  $1/f_m^3$  law is exhibited at the higher frequency end.

\*Note, however, that the FM noise is measured for the higher end of the frequency band of the baseband noise. At this end of the band, the baseband noise does tend towards a simple law of variation with frequency.

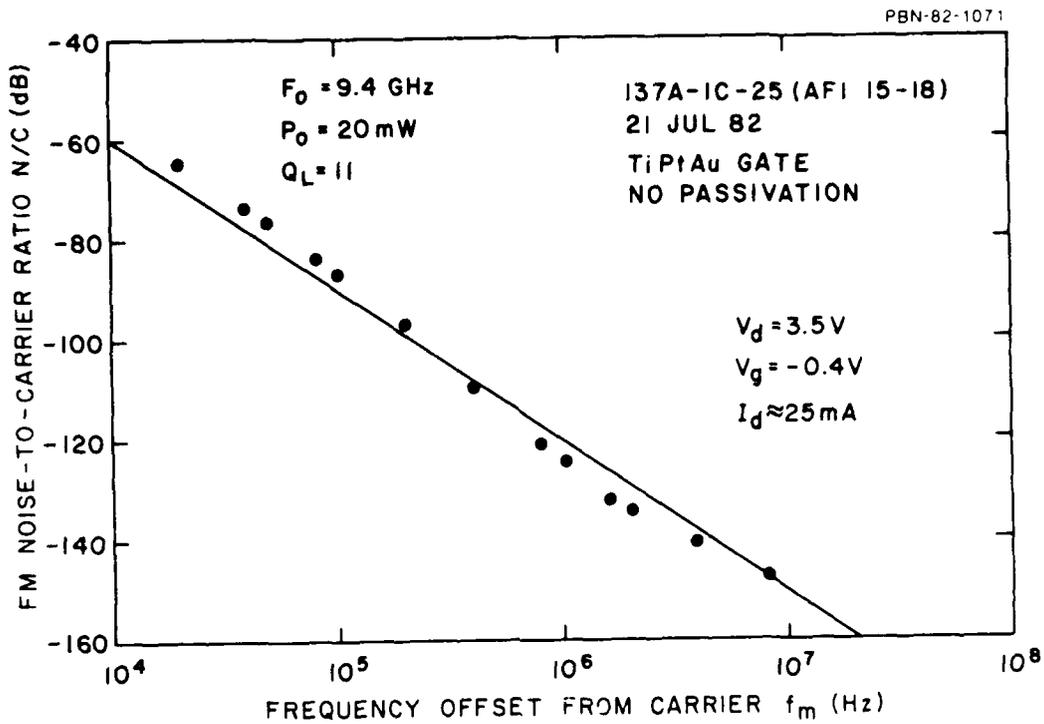


(a) No passivation.

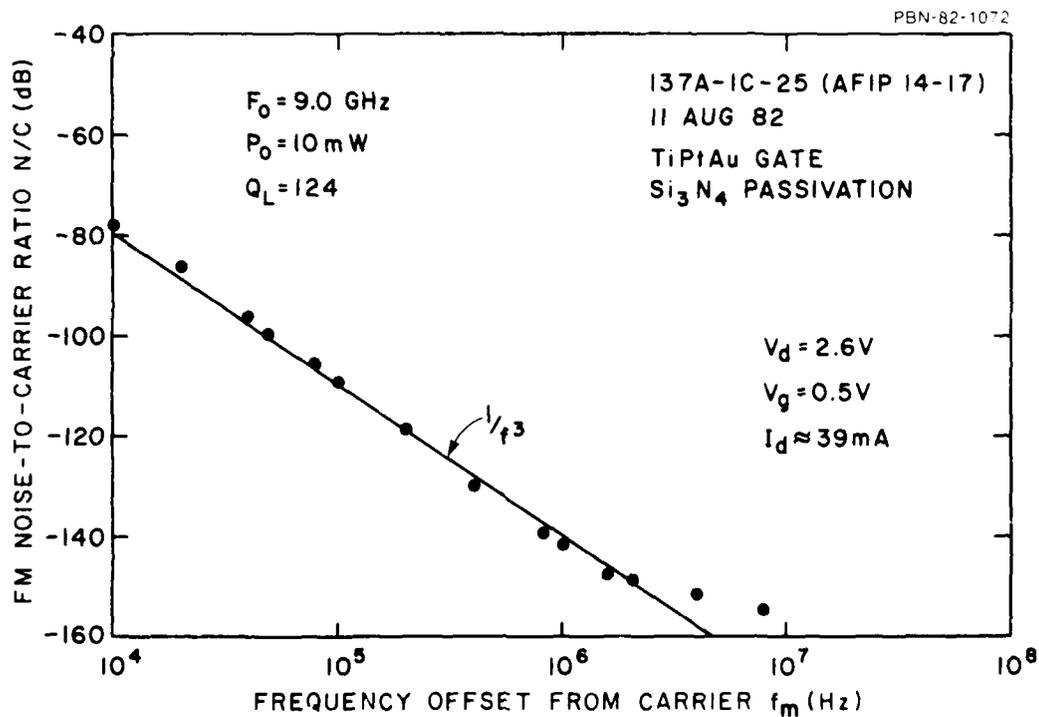


(b)  $\text{SiO}_x$  passivation.

Figure 4-32. FM N/C ratio vs. frequency offset from carrier for oscillating FET with TiPtAu gate and with and without  $\text{SiO}_x$  passivation.

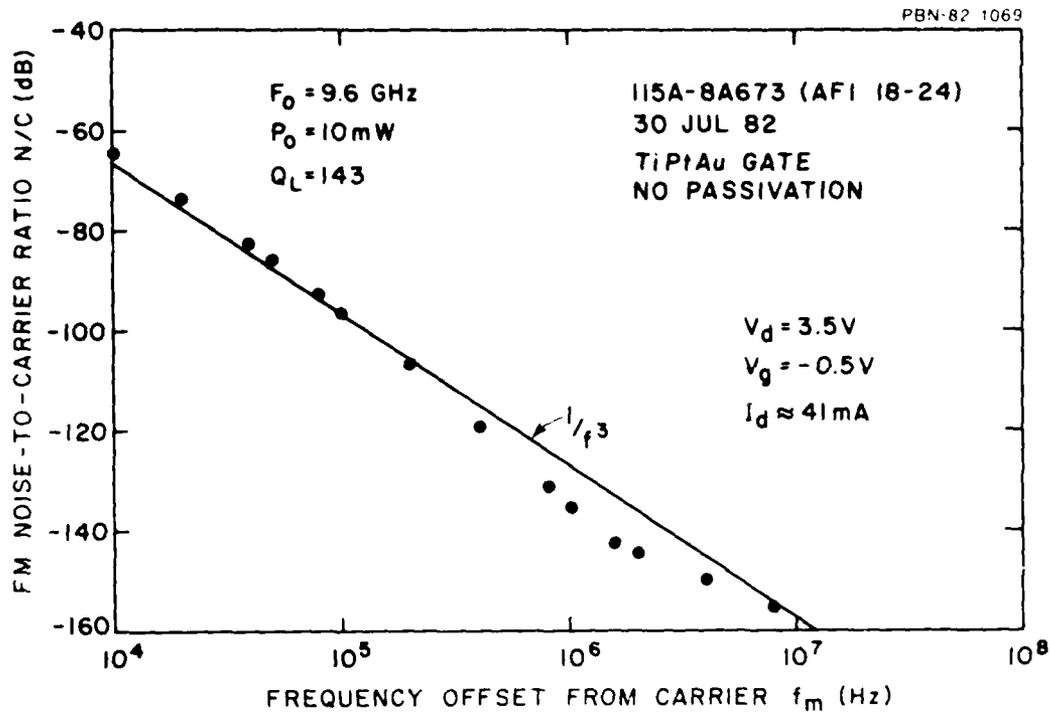


(a) No passivation.

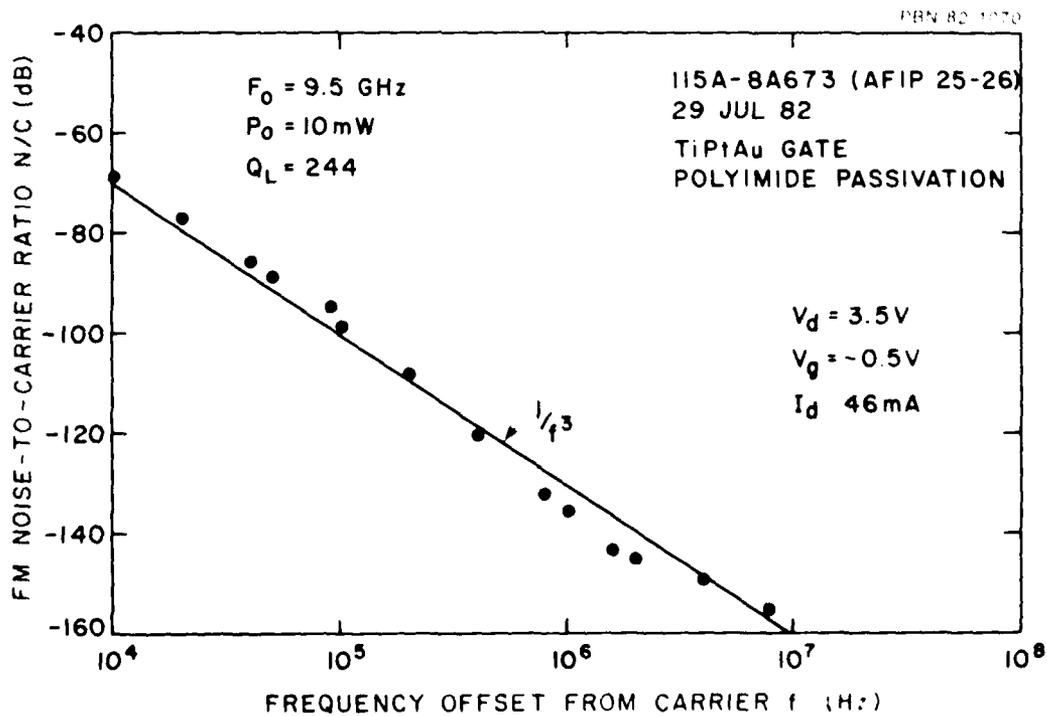


(b)  $\text{Si}_3\text{N}_4$  passivation.

Figure 4-33. FM N/C ratio vs. frequency offset from carrier for oscillating FET with TiPtAu gate and with and without  $\text{Si}_3\text{N}_4$  passivation.



(a) No passivation.



(b) Polyimide passivation.

Figure 4-34. FM N/C ratio vs. frequency offset from carrier for oscillating FET with TiPtAu gate and with and without polyimide passivation.

#### 4.4.6 FET with a TiPtAu gate and with oxygen implant isolation

For this case, no devices were passivated. However, the data obtained compares favorably with passivated mesa isolated devices. Indeed, as Fig. 4-35 shows, a very strong adherence to a  $1/f_m^3$  dependence is exhibited. Again, as for the case of  $\text{Si}_3\text{N}_4$  passivation, the noise performance shown here represents at least a 20 dB improvement over any corresponding result reported to date.

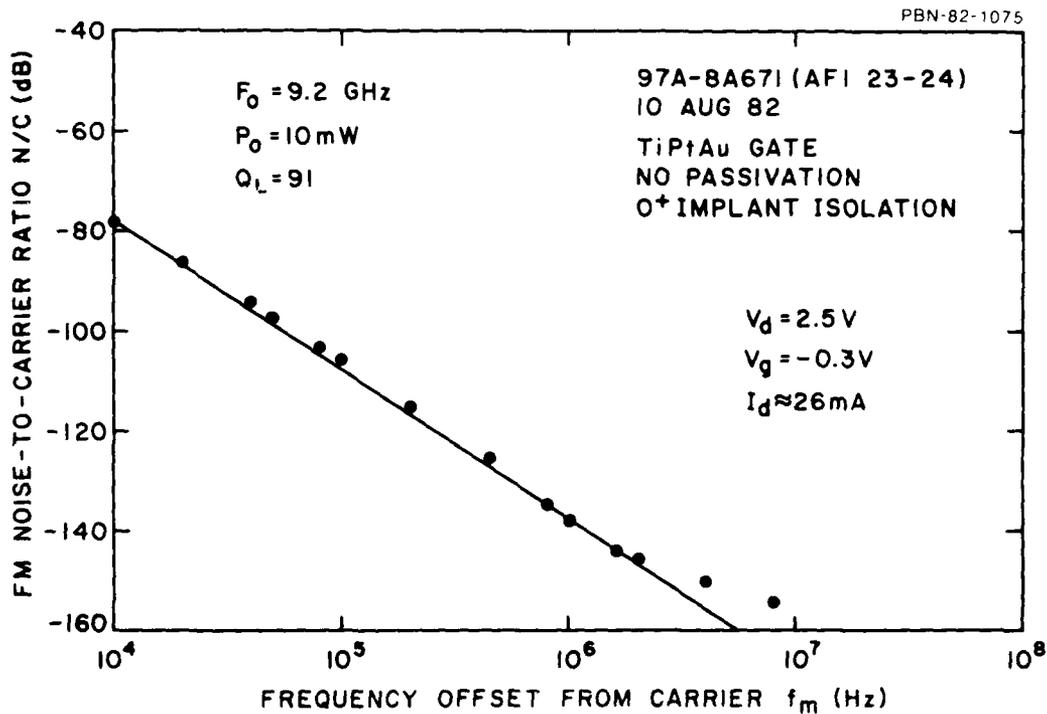


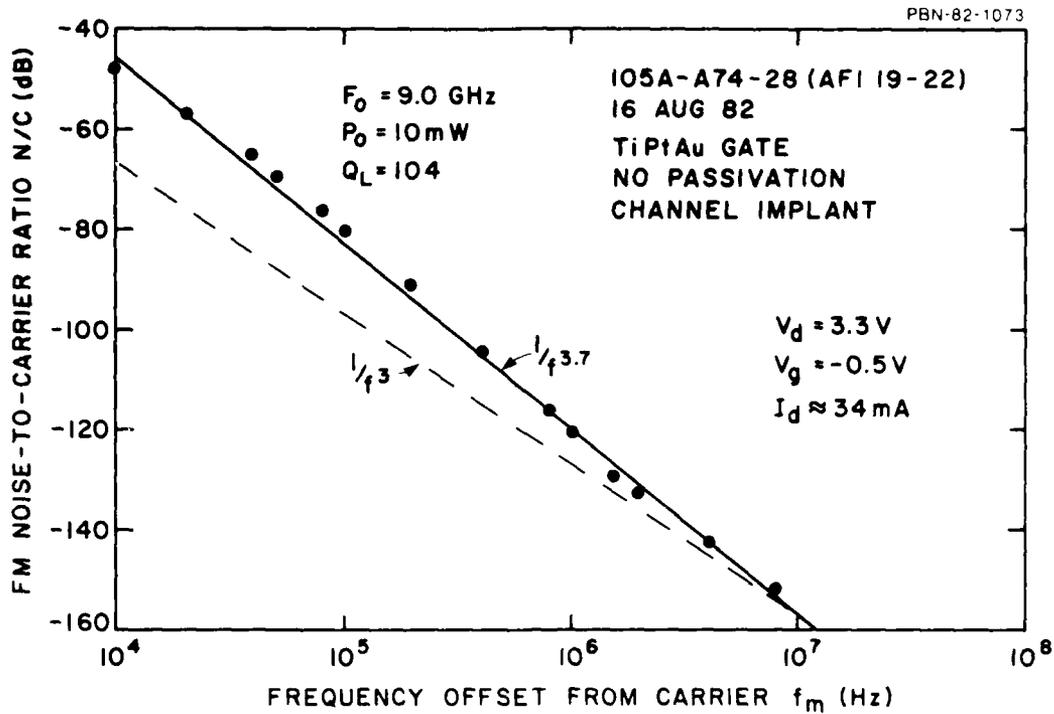
Figure 4-35. FM N/C ratio vs. frequency offset from carrier for oscillating FET with TiPtAu gate, oxygen implant isolation and no passivation.

#### 4.4.7 FET with a TiPtAu gate with and without $\text{SiO}_x$ passivation and an implanted channel

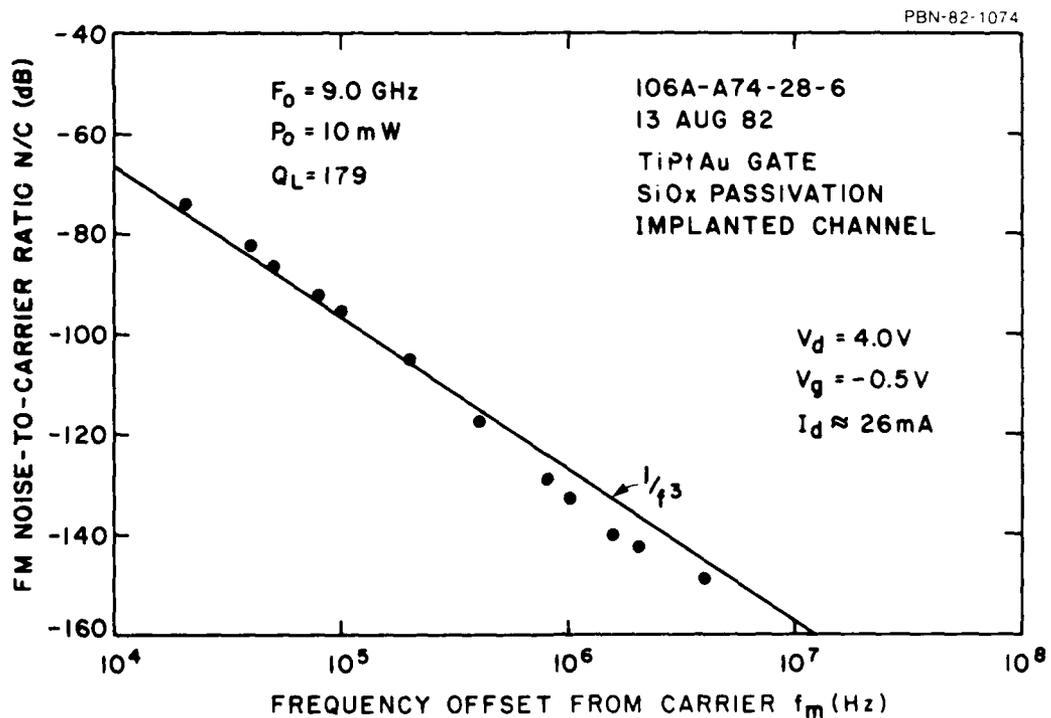
All of the previous oscillator data applied to devices with epitaxial channels. The following data were taken on a device with an implanted channel. See Fig. 4-36. It is a curious fact that the unpassivated data exhibits a  $1/f^{3.7}$  dependence, whereas the device with  $\text{SiO}_x$  does. We do not have an explanation for this. Note, however, that the abscissa crossing of the straight line is the same for both the unpassivated and passivated cases. What is contributing to the faster frequency dependence is the fact that the low-frequency noise very near the carrier is much higher. We shall show later, when we compare all of the results after normalization to a common Q-factor and carrier frequency, that the implanted channel noise levels are substantially higher than the epitaxial channel results.

One remaining case, obtained by "accident" bears discussion since it demonstrates what can happen to the oscillator noise when the surface is inadvertently contaminated during the processing. These results are depicted in Fig. 4-37.

This device happened to be one for which there remained on the surface a photoresist residue. Not only was the frequency dependence altered radically, but, as we shall show later, the noise level was increased substantially.



(a) No passivation.



(b)  $\text{SiO}_x$  passivation.

Figure 4-36. FM N/C ratio vs. frequency offset from carrier for oscillating FET with implanted channel, TiPtAu gate and  $\text{SiO}_x$  passivation.

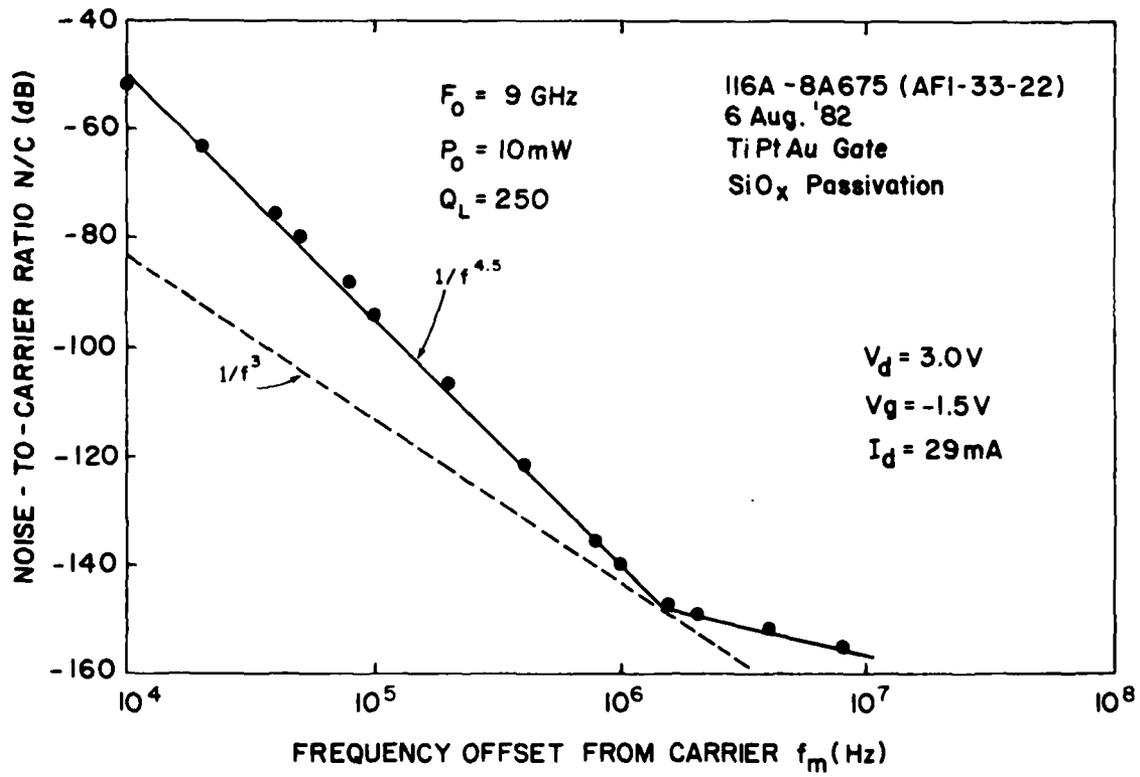


Figure 4-37. FM N/C ratio vs. frequency offset from carrier for oscillating FET with contaminated surface.

#### 4.5 Comparison of FM Oscillator Noise Performance for Various Fabrication Technologies

##### 4.5.1 Introduction

One of the objectives of this contract was to draw some conclusions as to which technologies lead to the best noise performance of the FET oscillator.

In order to do this, one must reduce all of the data shown so far to some common denominator, that is, one must be sure that variations in oscillator noise level attributable to circuit parameter variations are eliminated. For example, since the FM noise-to-carrier ratio depends on  $Q_L$ ,  $f_o$ , and  $P_o$  (see Eq. 3(b)), it is important to normalize the FM noise data in Fig. 4-31 through 4-37 to a common  $Q_L$  and  $f_o$ , and  $P_o$ .

Therefore, all data to be presented in this section has been normalized to a unity Q-factor, a carrier power of 10 mW, and a carrier frequency of 9.0 GHz. This is equivalent to plotting the quantity:

$$\left(\frac{f_n}{f_o}\right)^2 \left(\frac{P_o}{P_n}\right) Q_L^2 \left(\frac{N}{C}\right)_{FM} = \frac{N_b B}{P_n} \left(\frac{f_n}{f_m}\right)^2 \quad (11)$$

where  $f_n$  and  $P_n$  are the normalizing carrier frequency and power. Note, then, that the quantity on the right is a direct measure of the noise source  $N_b(f_m)$  associated with the device.

The data will be presented in the following way: For each technology, that is, CrAu gate, TiPtAu gate, etc., two curves will be plotted on each graph, one curve for the unpassivated case, the other, if available, for the passivated case. These data are based on Figs. 4-31 through 4-37. A plot of the data in this manner will make it evident what effect passivation has on the near-carrier

FM noise. Then by comparison of the graphs for the various gate technologies and the same passivation, in this case  $\text{SiO}_x$ , conclusions can be drawn regarding the effect of gate technology on noise. Finally, by comparison of all cases with one another, quantitative conclusions will be made regarding the preferred technologies for minimizing near-carrier FM noise.

#### 4.5.2 Normalized FM noise results

The data will be presented in the same order as in the previous section. For clarity, only the straight line "fit" to the data points is plotted, rather than the actual data\*.

The first plot, shown in Fig. 4-38, refers to the CrAu gate (wafer 89A-8A653) corresponding to Fig. 4-31. It is obvious that  $\text{SiO}_x$  passivation has degraded the FM noise performance by as much as 10 dB at the low frequency end. It is also evident that the drop-off with frequency is faster for the passivated device.

Lest one think that this may be a chance result, Fig. 4-39, which applies to the TiPtAu gate technology, but the same  $\text{SiO}_x$  passivation, also displays a 10 dB degradation, but here, uniformly over the frequency band.

The next set of results, Fig. 4-40, apply to a device with  $\text{Si}_3\text{N}_4$  passivation. Note that the passivation does not degrade the noise performance.

Virtually, the same conclusion applies to devices passivated with polyimide, Fig. 4-41. Thus, from these results, it can be concluded that of the three surface passivations studied, only  $\text{SiO}_x$  degrades the near-carrier FM noise performance.

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\*Note the  $Q_L$ -factor in parentheses is the value as measured, i.e., before normalization. It is stated for reference purposes, only.

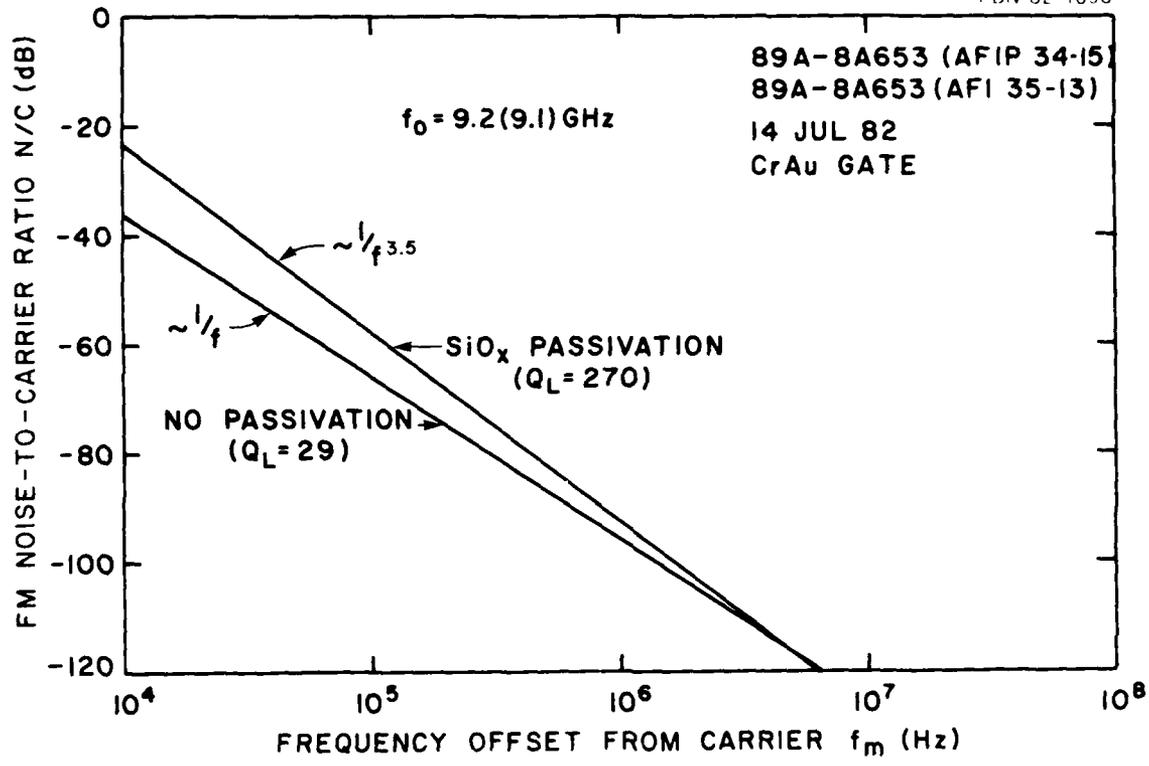


Figure 4-38. Normalized FM N/C ratio vs. frequency offset from carrier for an oscillating FET with a CrAu gate and with and without  $\text{SiO}_x$  passivation.

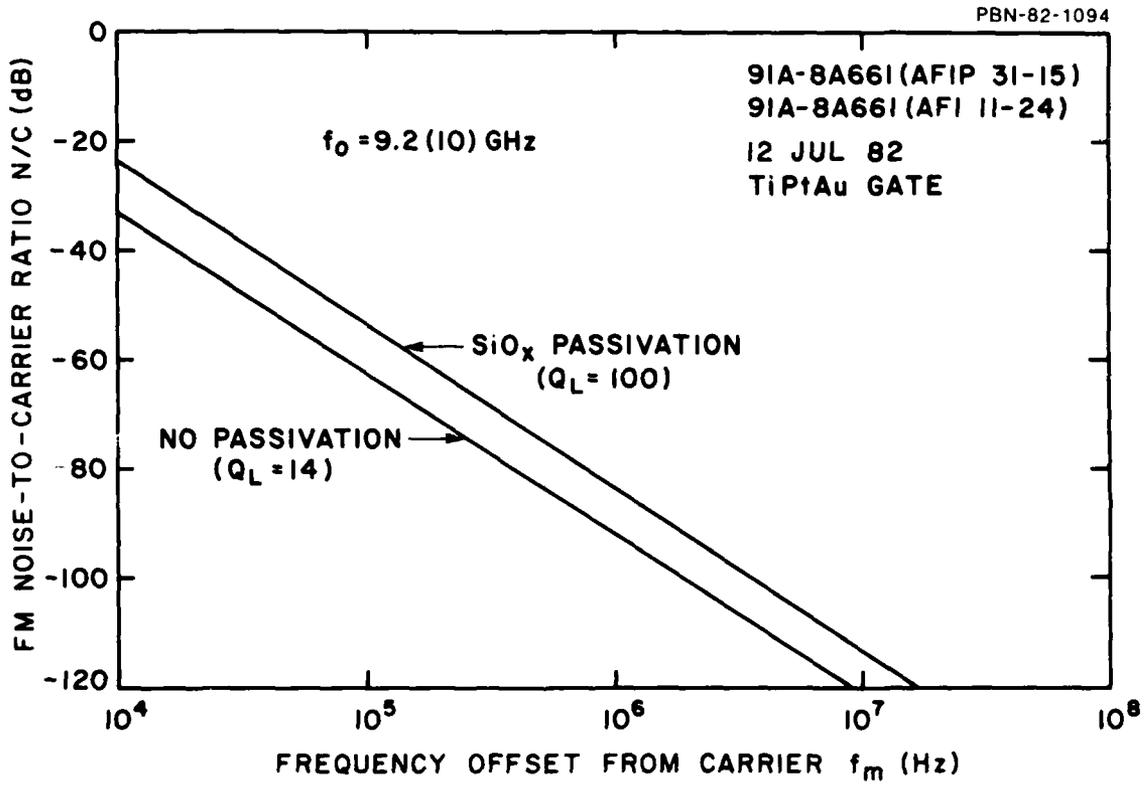


Figure 4-39. Normalized FM N/C ratio vs. frequency offset from carrier for an FET with a TiPtAu gate and with and without SiO<sub>x</sub> passivation.

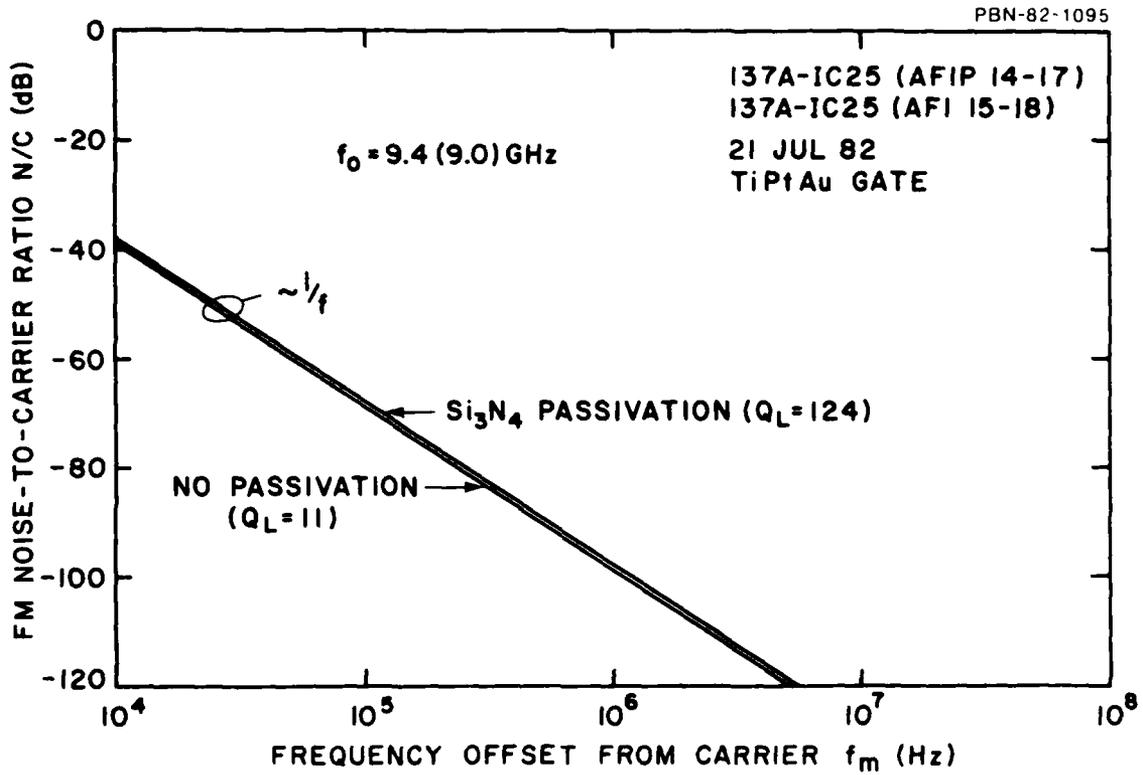


Figure 4-40. Normalized FM N/C ratio vs. frequency offset from carrier for an oscillating FET with a TiPtAu gate and with and without Si<sub>3</sub>N<sub>4</sub> passivation.

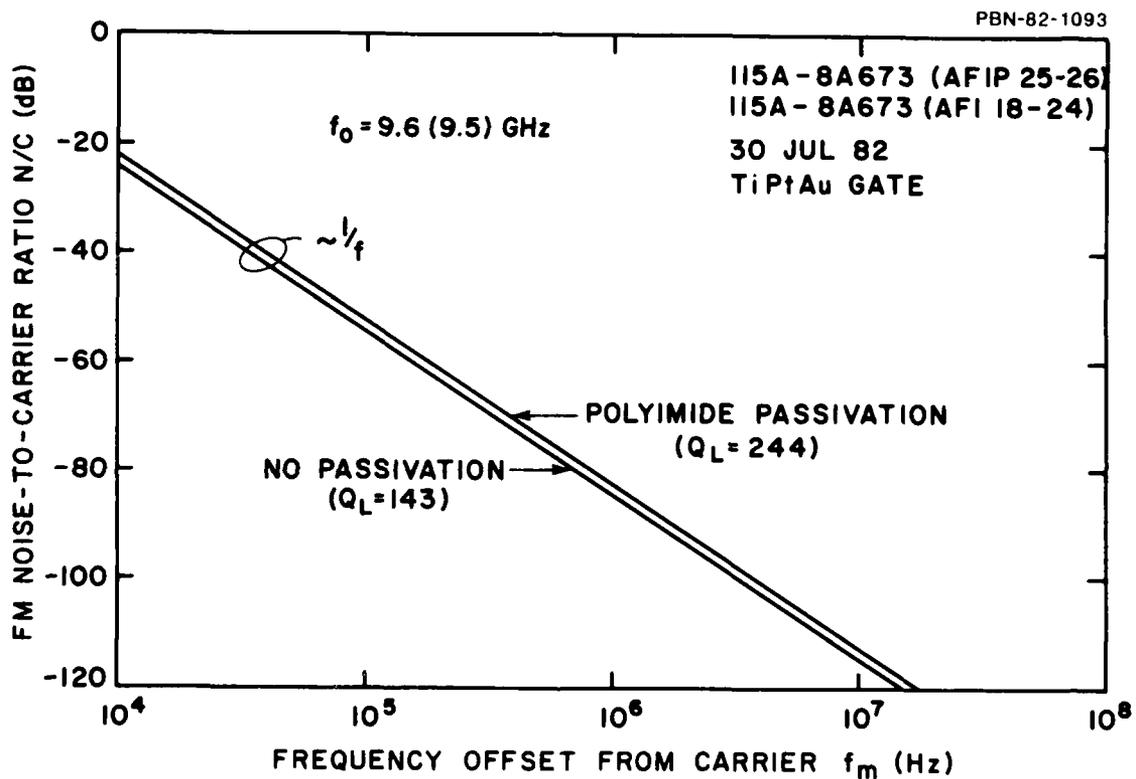


Figure 4-41. Normalized FM N/C ratio vs. frequency offset from carrier for an oscillating FET with a TiPtAu gate and with and without polyimide passivation.

The  $\text{Si}_3\text{N}_4$  and polyimide passivated devices differ in one important respect, however. The polyimide passivated device exhibited a noise level some 20 dB higher than the  $\text{Si}_3\text{N}_4$  passivated device, and indeed all previous devices without passivation, including the oxygen implant isolated device data illustrated in Fig. 4-42.

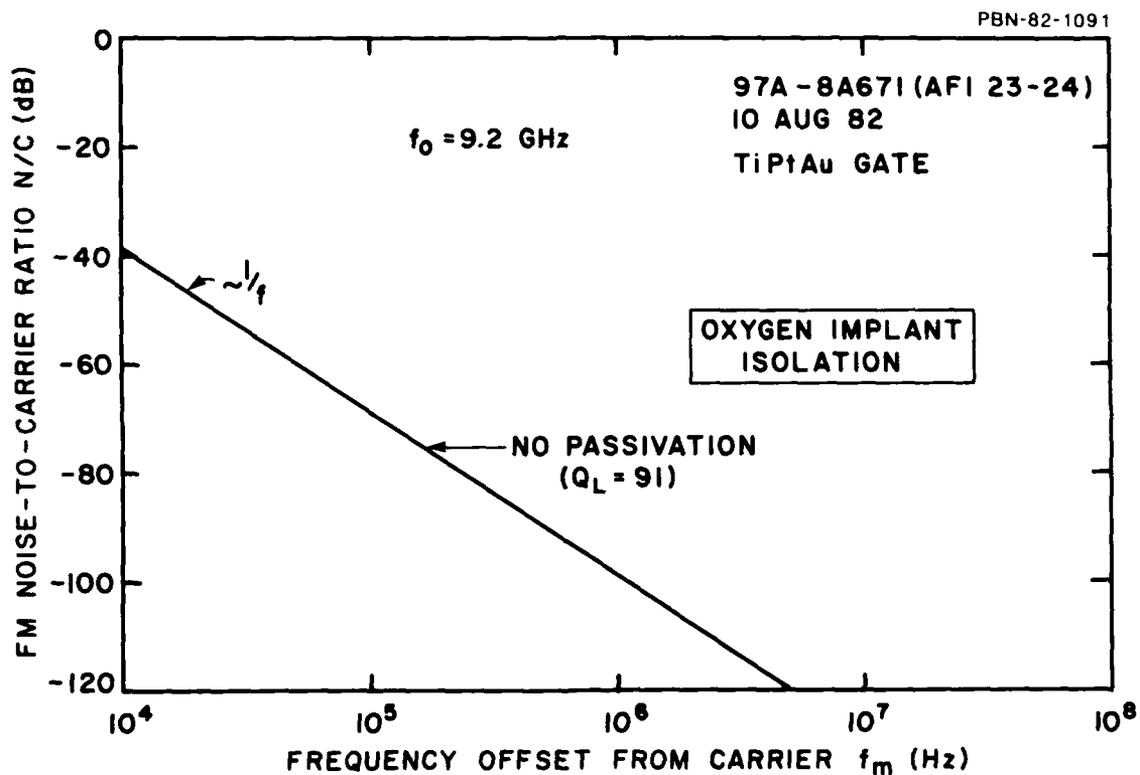


Figure 4-42. Normalized FM N/C ratio vs. frequency offset from carrier for an oscillating FET with a TiPtAu gate, no passivation, and an oxygen implant isolation.

We do not have any obvious explanation for this observation, but we shall propose some hypotheses later.

It is gratifying to note that isolation by implantation techniques does not degrade noise performance, because this is an attractive technology for monolithic microwave circuits. It is a technology being used extensively at this laboratory for this purpose.

Figure 4-43 is a clear demonstration of the degradation caused by disorders introduced by implantation of the channel region. Although there may be no intrinsic reason why implanted channels should be noisier than epitaxial channels, it is well known that incomplete "annealing out" of the lattice disorders, which introduce traps, can be responsible. An explanation for why, in this case, passivation lowers the noise, is not obvious. However, it should be pointed out that the two devices were not from the same wafer, though the wafers were from the same boule. Thus, one may be observing a normal variation associated with different wafer runs. Note the high noise level at the low frequency end.

The next graph, Fig. 4-44, refers to the device with the Al gate fabricated during the previous contract. Observe that the normalized noise level falls in the range between the lowest and highest level devices described for CrAu and TiPtAu gates.

The final graph, Fig. 4-45, is the normalized noise level for the device which contained a residue of photoresist on its surface. Note the extremely high noise level throughout most of the frequency range.

This completes the presentation of the experimental results. In the next section, an attempt will be made to draw some general conclusions from these results.

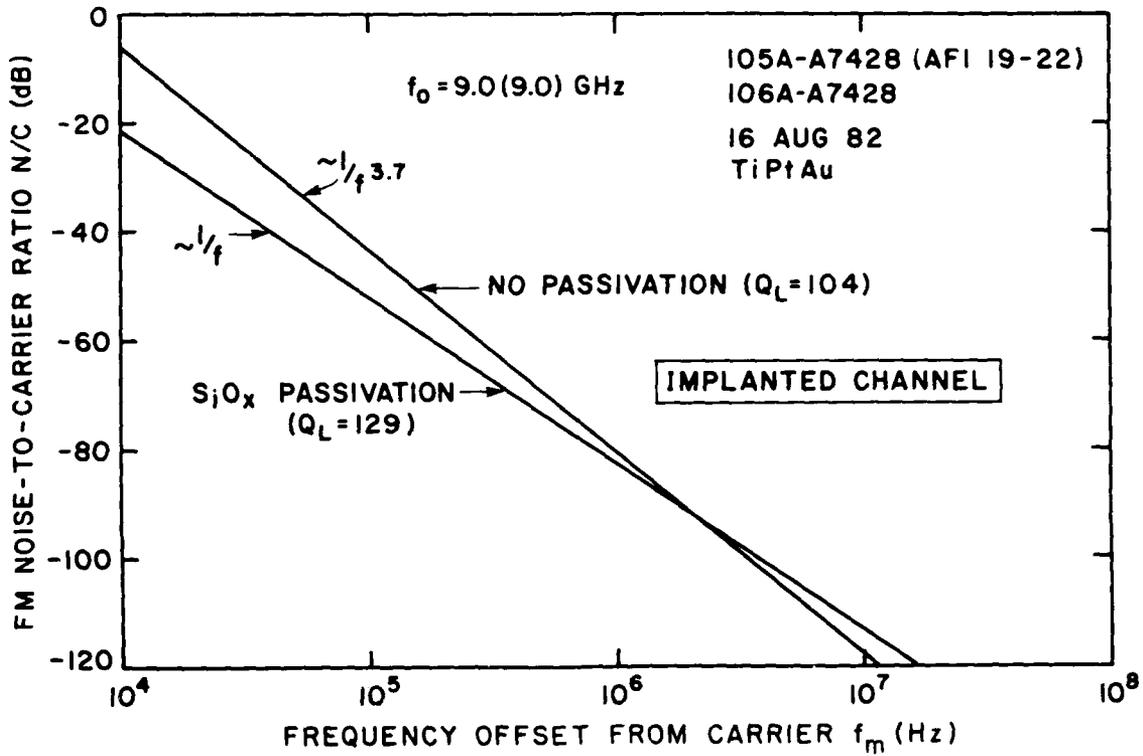


Figure 4-43. Normalized FM N/C ratio vs. frequency offset from carrier for an oscillating FET with a TiPtAu gate, with and without  $S_iO_x$  passivation, and an implanted channel.

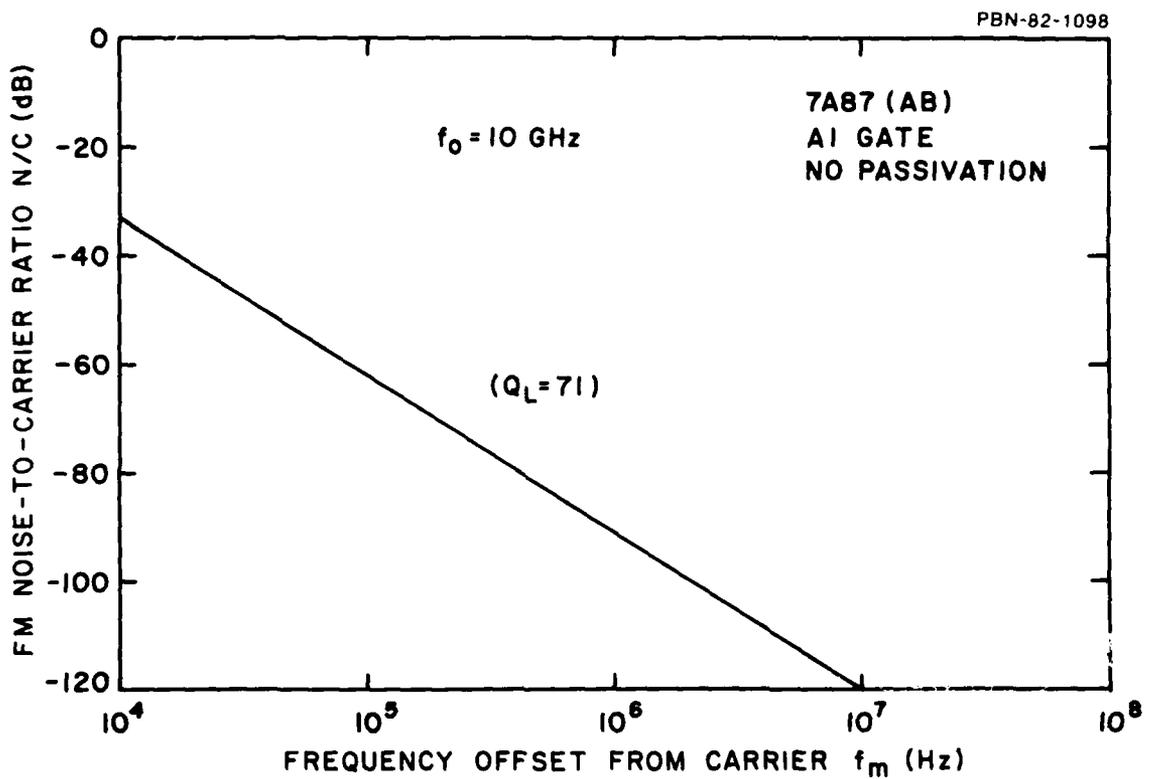


Figure 4-44. Normalized FM N/C ratio vs. frequency offset from carrier for an oscillating FET with an Al gate and no passivation.

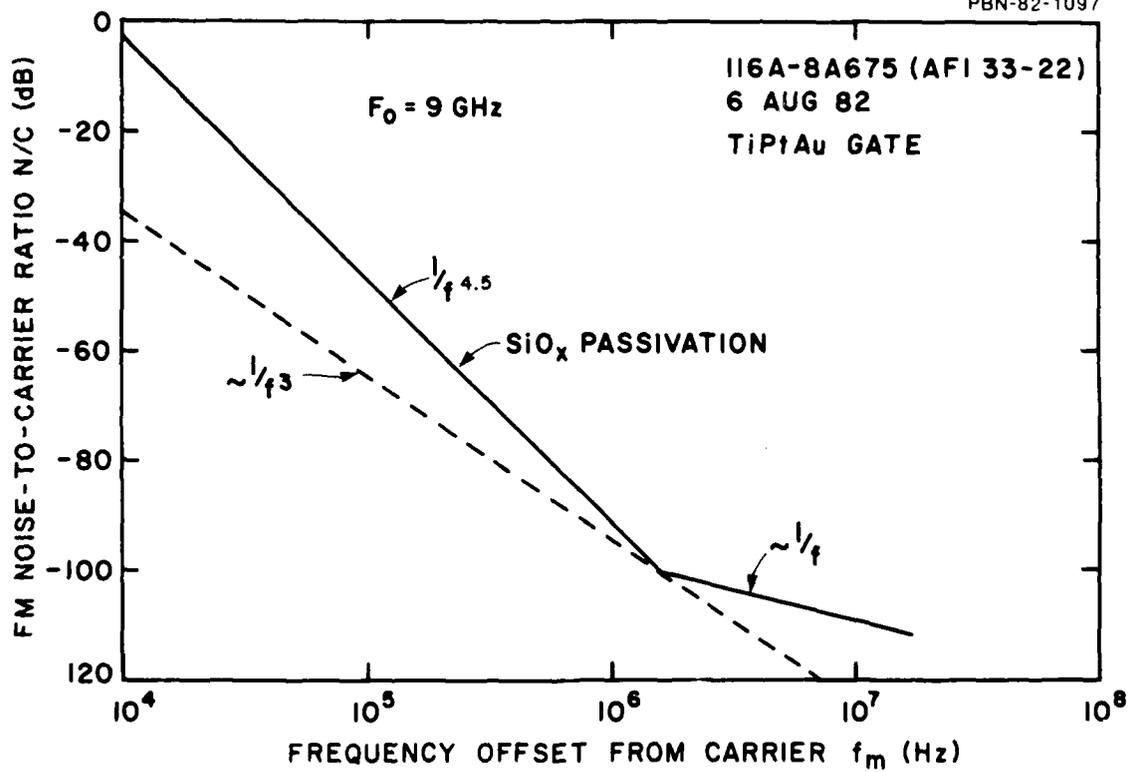


Figure 4-45. Normalized FM N/C ratio vs. frequency offset from carrier of an oscillating FET with a contaminated surface.

#### 4.6 Summary and Conclusions

There should be little doubt in the reader's mind that the baseband and near-carrier noise arise from the same source, namely, traps. This is evident from the fact that the baseband noise is strongly temperature dependent - much more so than, say, thermal noise. Furthermore, the strong influence of optical excitation on both the baseband noise, and on the hysteresis in the I-V characteristics, is another indication of traps.

The dependence of the hysteresis and noise on temperature and optical stimulation does not offer, however, a clue as to where the traps reside, since both bulk and surface traps are vulnerable to this stimulation. Indeed, even traps at the channel-buffer layer interface could be affected.

The role of interface traps can be eliminated, based on the findings of the previous contract. It has also been argued, based on this earlier work, that although bulk traps could not be ruled out completely, the implied density of these traps inferred from the noise level was rather high. On the other hand, the required surface trap densities were reasonable.

The present work also does not rule out bulk traps. Nevertheless, if bulk traps do play a role (and they probably do) their effect is remarkably uniform from wafer to wafer. If one compares the normalized noise data for all wafers with epitaxial channels (Table 3-1), with the exception of 8A673, one finds only about a 4-dB variation. Some of this spread, undoubtedly, is experimental. Although wafers 8A653, 8A661, and 8A671 are from the same Sumitomo boule (No. 0789), wafer 7A87 is from an earlier boule. Furthermore, wafer IC25 is from a boule from a different manufacturer, namely, Microwave Associates.

Why the normalized noise level from wafer 8A673, also from boule 0789, is over 20 dB higher, is a mystery. Wafer-to-wafer variation within the same boule is ruled out, since this latter wafer was adjacent to wafer 8A671.

That surface traps are at least partially responsible for near-carrier noise is not in doubt. The fact that different passivations affect the noise level differently points clearly to the role of surface traps. What is also evident is that not all baseband noise, whether caused by surface or bulk traps, is upconverted to near-carrier FM noise. The more well-behaved power-law frequency dependence of near-carrier noise vs. baseband noise seems to imply that the upconverted noise component is caused by those traps which are more densely, and uniformly distributed in energy. This would seem to favor surface traps. To this writer's knowledge, there is no convincing model for generation of  $1/f$  noise in GaAs FETs by bulk traps, or other bulk sources, which agrees quantitatively with experiment.

The evidence presented also demonstrates that  $\text{Si}_3\text{N}_4$  and polyimide passivation had no detrimental effect on near-carrier noise, whereas  $\text{SiO}_x$  did. That the latter degraded the noise performance is not too surprising since previous experience with oxide passivations on silicon bipolars and GaAs FETs showed that surface states were introduced. It is gratifying to know that  $\text{Si}_3\text{N}_4$ , in particular does not degrade noise performance since this passivation technology is being favored by workers in the field, both for discrete devices and for microwave monolithic circuits.

The concern that gate technology might play a dominant role in  $1/f$  noise generation seems to be dispelled by experiment, since no discernable difference was found between devices fabricated with CrAu, TiPtAu, and Al gates, the three most favored technologies.

It is felt that the above conclusions based on the experimental evidence gathered during this period of research, have answered the major questions which were to be answered. These were, namely, (1) what effect do gate technology, surface passivation, and implantation have on the oscillator noise performance, and (2) what are the preferred technologies for low-noise FET oscillators.

A model based on surface state traps was proposed. Although no attempt was made to obtain quantitative agreement with experiment, as was done in the previous contractual effort, the model was shown to be qualitatively plausible. It is suggested that further study, more narrowly confined to one or two technologies, could, perhaps, lead to a quantitative model. Also, more definitive experiments with laser illumination confined to a thin surface layer, could help quantify the surface model, and, separate the effects of bulk and surface traps.

It is to be emphasized that the experiments described do not, per se, exclude bulk traps as a component source of noise. Indeed, the narrow spread in residual noise level obtained for unpassivated devices after normalization, for the many wafers tested, suggests that bulk traps are involved. It is likely that the sources responsible for this residual level of noise are probably quite common among manufacturers of boules, and from boule to boule. If bulk traps are involved, as they seem to be, then a model based on them which could explain the residual noise level still remains elusive to workers in the field. It is hoped that the results of this research will renew research effort to solve this problem and help explain why devices based on GaAs material, compared to, say silicon, exhibit high residual  $1/f$  noise.

Nevertheless, it is worth reporting that this residual noise level measured on our epitaxial channel devices is substantially lower than anything reported heretofore in the literature. This conclusion has been corroborated by other workers.<sup>25</sup>

5.0 PROFESSIONAL PERSONNEL ASSOCIATED WITH THE RESEARCH EFFORT

1. Mr. Robert W. Bierig
2. Mr. Jack Curtis, Sr.
3. Dr. Raymond Ellis
4. Ms. Aphrodite Gracie
5. Dr. Bruce Lauterwasser
6. Dr. Robert Mozzi
7. Dr. Herman Statz
8. Ms. Elsa Tong

6.0 WRITTEN PUBLICATIONS IN TECHNICAL JOURNALS

No publications were published in connection with this effort.

7.0 INTERACTIONS

There were no talks or consultations connected with this effort.

8.0 NEW DISCOVERIES, INVENTIONS, OR PATENT DISCLOSURES AND SPECIFIC APPLICATIONS STEMMING FROM THIS RESEARCH EFFORT

There were none.

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