39

14

October, 1982 MRDC41070.15QR

LSI/VLSI ION IMPLANTED GaAs PROCESSING

Quarterly Technical Report No. 5

For Period 08/01/81 through 10/31/81

Contract No. F49620-80-C-0101

Project No. 3384-4

ROCKWELL INTERNATIONAL
Microelectronics Research and Development Center
Thousand Oaks, CA 91360

Sponsored by:

Advanced Research Projects Agency (DOD)

ARPA Order No. 3384-4

Monitored by AFOSR under Contract No. F49620-80-C-0101

Prepared by:

Ricardo Zucca

R. Zucca
Principal Investigator

A. Firstenberg
Principal Investigator

Rockwell International

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: AFOSR-TR- 83-0136 / 2. GOVT ACCESSION NO.: AD-A12	3. RECIPIENT'S CATALOG NUMBER: 6394
4. TITLE (and Subtitle): LSI/VLSI ION IMPLANTED GaAs IC PROCESSING	5. TYPE OF REPORT & PERIOD COVERED: Quarterly Technical Report 8/1/81 through 10/31/81
	6. PERFORMING ORG. REPORT NUMBER: MRDC41070.15QR
7. AUTHOR(s): R. Zucca, C. P. Lee, Y. D. Shen, P. Asbeck, C. G. Kirkpatrick, A. Firstenberg	8. CONTRACT OR GRANT NUMBER(s): F49620-80-C-0101
9. PERFORMING ORGANIZATION NAME AND ADDRESS: ROCKWELL INTERNATIONAL/Microelectronics Research and Development Center, 1049 Camino Dos Rios, Thousand Oaks, CA 91360	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: ARPA Order No. 3384-4, 61102F
11. CONTROLLING OFFICE NAME AND ADDRESS: Advanced Research Projects Agency (DOD), 1400 Wilson Boulevard, Arlington, VA 22209	12. REPORT DATE: October 1982
	13. NUMBER OF PAGES: 37
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office): Air Force Office of Scientific Research, Bolling Air Force Base, Washington, DC 20332	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

This research was sponsored by the Advanced Research Projects Agency (DOD) ARPA Order No. 3384-4

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Semi-Insulating	High Speed Logic
Ion Implantation	GaAs
IC	FET
Integrated Circuits	MESFET

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report covers the fifth quarter of a program aimed at fully realizing the potential of GaAs for digital integrated circuits employing depletion mode MESFETs. During this reporting period the processing of wafers with mask set AR6 containing the SD^2FL 8 x 8 parallel multiplier has continued. DC parametric testing has shown good FET and diode characteristics and yield, as well as good results in terms of other process related parameters. Studies of the effects of impurity contamination on implanted layers characteristics have shown that wafer contamination by Si, Au, or Cr during

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

the post-implant anneal can lead to detrimental implant compensation. Reliability studies on ring oscillators have confirmed the progress made with the adoption of an Au-Ge/Ni ohmic contact metalization scheme. Modeling efforts of MESFETs have continued.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (continued)

LIST OF TABLES

FOREWORD

The research covered in this report is carried out in a team effort having the Rockwell International Microelectronics Research and Development Center as the prime contractor, with two universities and a crystal manufacturer as subcontractors. The effort is sponsored by the Defense Sciences Office of the Defense Advanced Research Projects Agency. The contract is monitored by the Air Force Office of Scientific Research. The Rockwell program manager is Fred H. Eisen. The principal investigators for each organization are:

Microelectronics Research and Development Center	R. Zucca, A. Firstenberg
California Institute of Technology	M-A. Nicolet
North Carolina State University	N.A. Masnari
Crystal Specialties	W.P. Allred

Numerous other researchers were involved in the work reported herein. The principal contributors are:

Microelectronics Research and Development Center	P.M. Asbeck, D. Hou, A. Firstenberg, W.P. Fleming, G.R. Kaelin, C.G. Kirkpatrick, C.P. Lee, F.S. Lee, M.J. Sheets, E.K. Shen, Y.D. Shen, J.O. Thompson, E.R. Walton, B.M. Welch, R. Zucca
California Institute of Technology	T. Banwelo, M. Martimaenpaa,
North Carolina State University	J.R. Hauser, T.H. Glisson, R.J. Trew
Crystal Specialties	J. Burns

1.0 INTRODUCTION

This report covers the fifth quarter of a program on LSI/VLSI Ion Implanted Planar GaAs IC Processing. The main objective of this program is to realize the full potential of GaAs digital integrated circuits by expanding and improving fabrication techniques as well as material growth, preparation and selection. The principal goal is to improve material and processing capabilities so that large wafers (3 inch diameter) can be processed in order to satisfy anticipated needs for high-speed low-power GaAs digital VLSI integrated circuits. In parallel with increasing circuits complexity and wafer size, the program is also directed toward the investigation of circuit reliability, and the development of processing techniques and circuit designs capable of attaining the highest reliability. Circuit design advancements are also explored with the introduction and implementation of multilevel logic circuits. Three subcontractors, the California Institute of Technology, North Carolina State University, and Crystal Specialties, Inc. are contributing to the program with their expertise in ion beam techniques, device modeling, and crystal growth, respectively.

During this reporting period, processing on mask set AR6 containing the SD^2FL 8 x 8 multipliers has been completed on 5 lots (20 wafers), with two additional lots still in progress at the end of the quarter. Low frequency parametric testing has shown acceptable FET and diode characteristics, high yields of these devices, as well as acceptable results in terms of other process related characteristics such as ohmic contact resistance, carrier concentration profiles, metallization specific resistance, interconnect resistance, etc. Results from circuit tests will be presented in the next report.

In materials and ion implantation, an effort was made during this quarter to investigate the effects of impurity contamination which are known to contribute to variations in implanted layer characteristics. It was found that wafer contamination by Au or Cr curing the post-implant anneal leads to

detrimental implant compensation, while Ni or Ti contamination does not. Silicon contamination of the cap-GaAs interface was also shown to be detrimental.

Reliability tests were made on GaAs integrated circuits using accelerated life tests. Ring oscillators were thermally aged at 200° and 250° under bias, and the propagation delays were measured. From these measurements degradation activating energies were calculated, and mean time to failure times were estimated.

Finally, work has continued at North Caroline State University in MESFET modeling. Three activities, two-dimensional numerical modeling, development of an analytical FET model, and Monte Carlo analysis are being pursued. The program for Monte Carlo analysis underwent a major change so that better convergence is obtained. Rather than starting on electron on either the source or drain contact, an ensemble of carriers is followed starting from positions determined by the charge density obtained form a two-dimensional model.

The investigation on impurity contamination is discussed in Section 2. In Section 3, parametric data on the AR6 wafers processed are presented. The reliability study on ring oscillators is discussed in Section 4, and MESFET modeling is covered in Section 5.

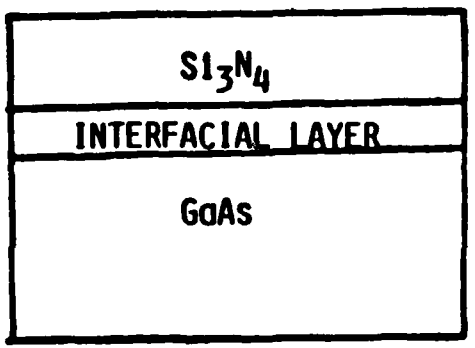
2.0 IMPACT OF IMPURITY CONTAMINATION ON IMPLANTED CHANNEL REGIONS

Reproducibility of the electrical characteristics of implanted FET channel regions is one of the important concerns of this program. Work reported in the last quarter indicated that impurity contamination introduced during the implant process was an important source of nonreproducibility. During this quarter, the effects of contamination by several potential impurities was investigated in detail. As described below, it was detemined that Au or Cu contamination of the wafer during the post-implant anneal leads to detrimental implant compensation, while Ni or Ti contamination does not. Silicon contamination of the cap-GaAs interface was also shown to be detrimental, although it causes an acceptor-like contribution to the doping, rather than a donor-like component as would be naively expected.

To study the effects of Au, Cu, Ni, Ti contamination, evaporated layers of these metals were deposited on the back sides of test wafers of semi-insulating GaAs. The wafers had been previously encapsulated with sputtered Si_3N_4, and implanted with Se (at a fluence of 2.5×10^{12} cm^2, typical of FET channel layers). The wafers were subsequently annealed at 850°C for 30 min, as used in the IC process. Sealed quarz ampoules were utilized to avoid furnace contamination. After stripping the dielectric encapsulant and carrying out C-V measurements, it was found that the Ni and Ti contaminated samples were comparable to concurrently processed uncontaminated control wafers (having a threshold voltage of -2.0 ± 0.1 V), while there was no discernable implant activation in the Au or Cu contaminated samples. It was of interest to determine if the effects of Au and Cu could be eliminated by protecting the back sides of the wafers with sputtered silicon nitride. Accordingly, samples were processed with evaporated metal layers on the back of wafers encapsulated both front and back. Again, no implant activation was obtained. Apparently these metals can readily diffuse through the cap.

Investigation of silicon contamination of the cap-GaAs interface was undertaken because of the concern that free Si-rich silicon nitride could

potentially be formed in the early phases of the cap sputter deposition under some circumstances. To investigate its effects, a silicon layer of the order of 15Å thick was intentionally deposited on test GaAs wafers, and followed by immediate deposition of the standard Si_3N_4 cap without exposing the wafers to air. The silicon deposition was accomplished by sputtering, using a silicon target and argon plasma; a nitrogen plasma was subsequently used to produce the Si_3N_4. The contaminated wafers were implanted with Se, annealed and evaluated in the standard fashion. It was anticipated that an extra donor component would appear due to silicon indiffusion. Unexpectedly, the profiles showed that in addition to the normal Se donor concentration, there was an acceptor-like doping component localized near the GaAs surface, as determined from a reduction in the absolute value of the threshold voltage of about 0.7 V, and an increase in the zero-bias depletion depth of about 600Å as shown in Fig. 1. The nature of the acceptors is not known. They may result from an alteration of the GaAs stoichiometry near the surface, if Ga or As preferentially interacts with the silicon-rich interfacial layer.



INTERFACIAL LAYER:
SPUTTERED Si (ARGON PLASMA)

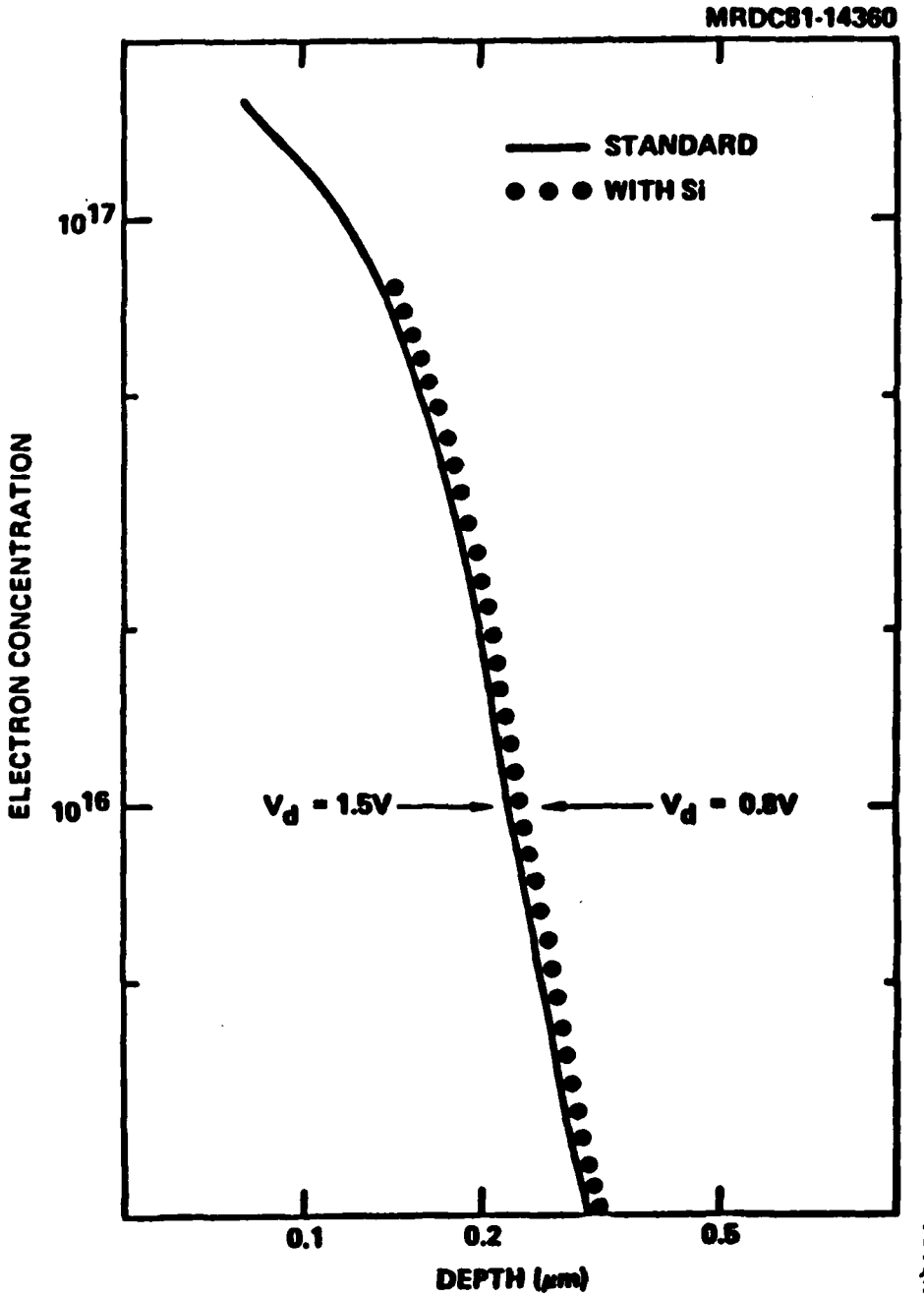


Fig. 1 Change in the carrier concentration profile caused by a Si layer deposited on the surface of the substrate prior to encapsulation to simulate the effects of Si contamination.

3.0 PARAMETRIC DATA FROM AR6 WAFERS

At the end of this quarter, processing of 5 lots (20 wafers) using mask set AR6 had been completed, and two more were well advanced in process. All the wafers were characterized by our standard parametric test procedure based on the automatic test of arrays of test structures placed on all wafers.

A sample of such parametric data is shown in Figs. 2 and 3. The data in Fig. 2 represent a histogram of threshold voltages for the 48 test FETs (50 μm channel width, 1 μm gate length) distributed across the 1 inch square wafer. A wafer map is shown on the left. The average threshold voltage, V_p = -1.02 V is within the desired range of 0.9-1.3 V, and the wafer standard deviation of 72 mV is quite typical (best values are ~30 mV). A complete summary of parametric data from the same array of FETs is shown in Fig. 3. Here the averages and standard deviations of all the parameters needed to characterize the devices are printed. Most important among these parameters are the threshold voltage, V_p, the saturation current, I_{dss}, the "on" resistance R_{ON}, and constant K in the equation used to model the saturation region of the characteristics,

$$I_{ds} = K(V_{gs} - R_s I_{ds} - V_p)^2 \quad . \tag{9}$$

The average values and standard deviations in Fig. 3 are quite typical for 50 μm wide FETs, and they scale with the width with the exception of V_p. These data contribute to the data base from which SPICE circuit simulation parameters are extracted and updated.

Figures 4 to 6, display the average value of some key parameters as a function of time for all the AR6 wafers. In these three figures, the horizontal scale represents the date on which the data were taken, which are very close to the dates on which fabrication was completed. Each point corresponds to the average value over one wafer of the parameter displayed in the plot. Figure 4 corresponds to threshold voltages, which fall in the -0.9

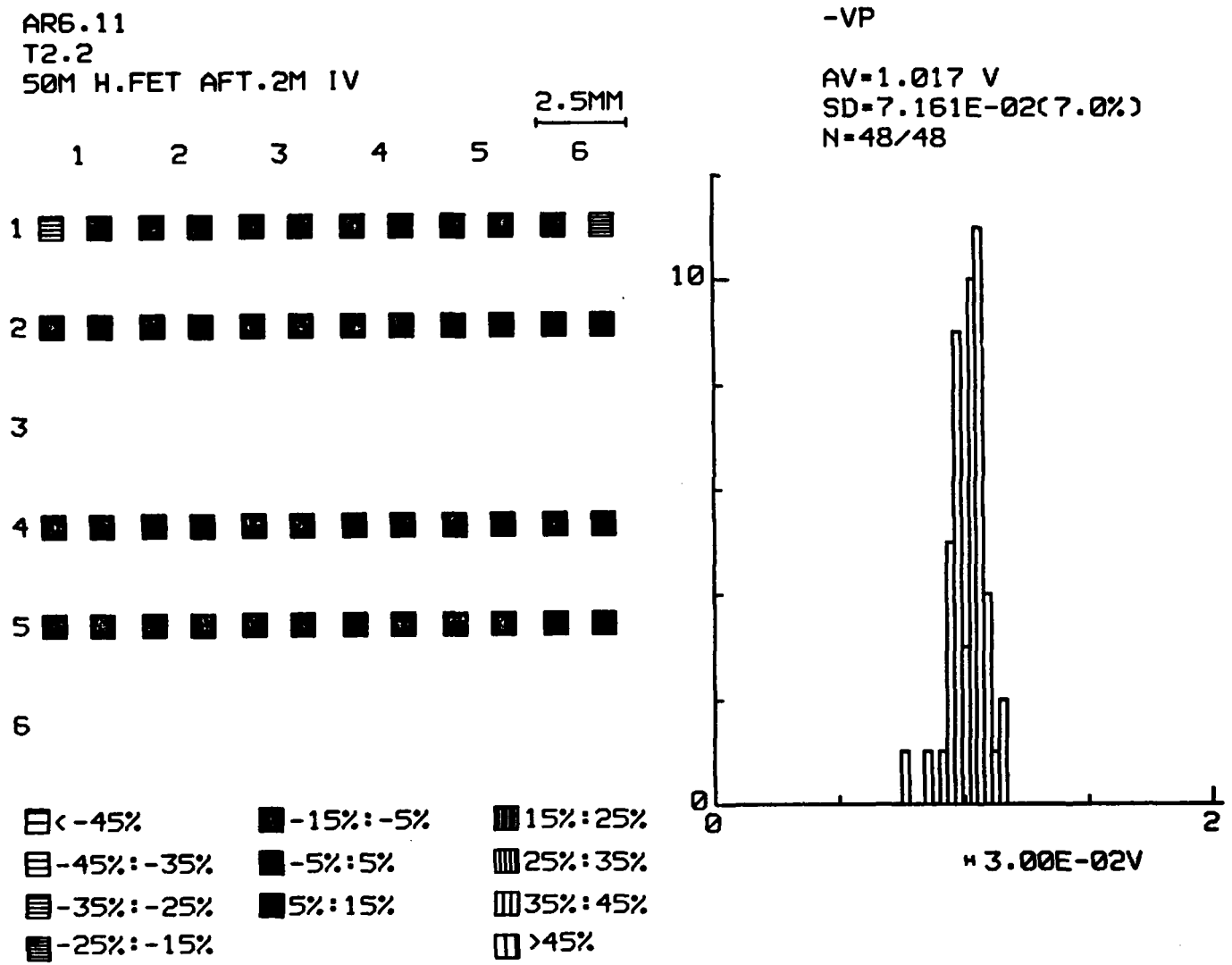


Fig. 2 Wafer map and histogram of test FET threshold voltages ($-V_p$) from a typical AR6 wafer.

AR6.11
T2.2
50M H.FET AFT.2M IV

PARAMETER	UNIT	AVERAGE	SD	%
-VP	V	1.017	7.1613E-02	7.0
RS	OHMS	47.40	13.58	28.6
K	MMHO/V	4.047	.9966	24.6
-VPE	V	.5811	4.8636E-02	8.4
IDSS	MA	3.055	.3676	12.0
GD	MMHO	.1128	2.9177E-02	25.9
RON	OHMS	184.3	22.15	12.0
VSAT	V	1.009	.1039	10.3
IG	NA	9.500	7.366	77.5

TOTAL: 48
WORK : 48 (100.0%)

Fig. 3 Summary of test FET data from a typical AR6 wafer.

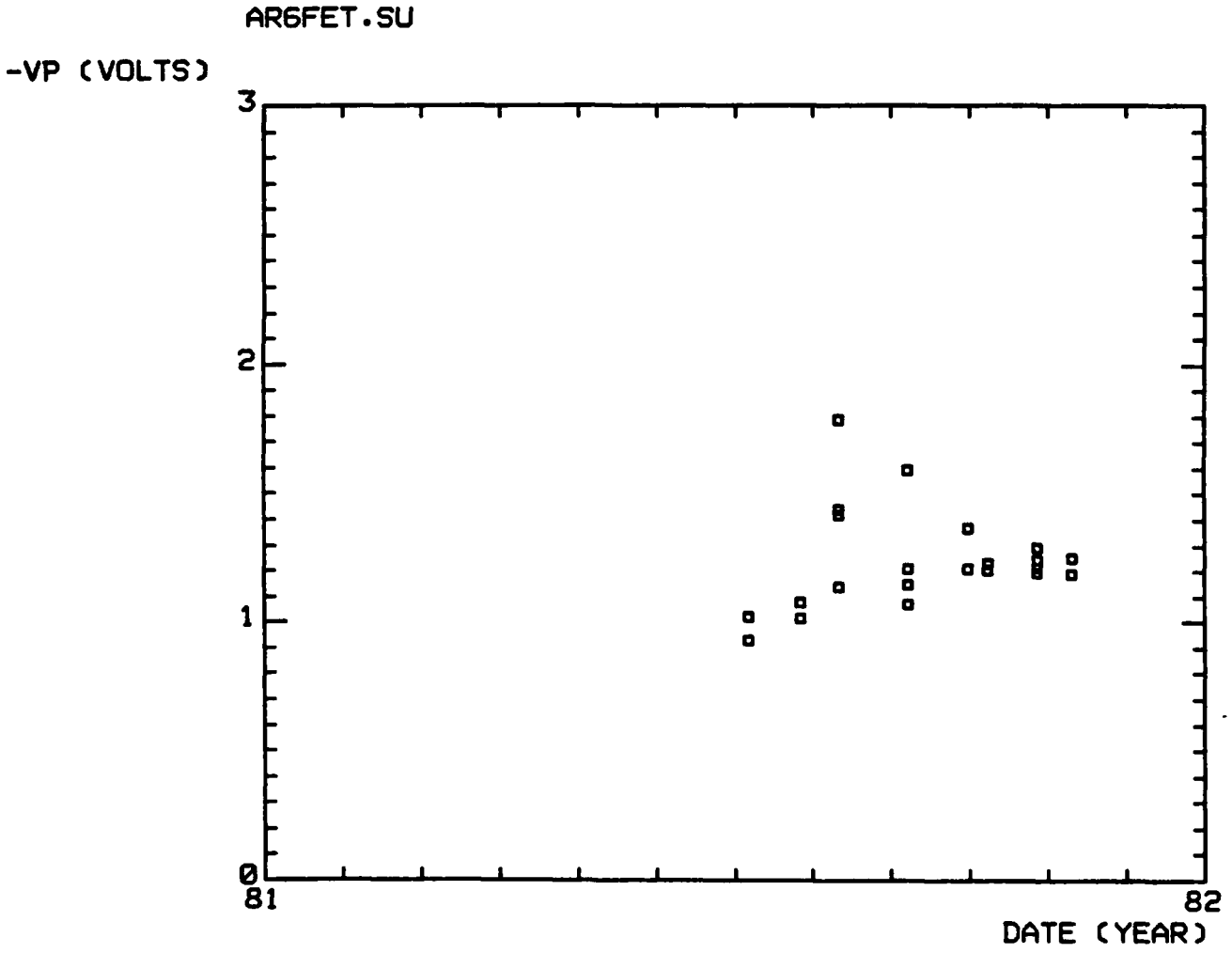


Fig. 4 History of average of threshold voltages, V_p, for the AR6 wafers. Each data point represents the average over one wafer.

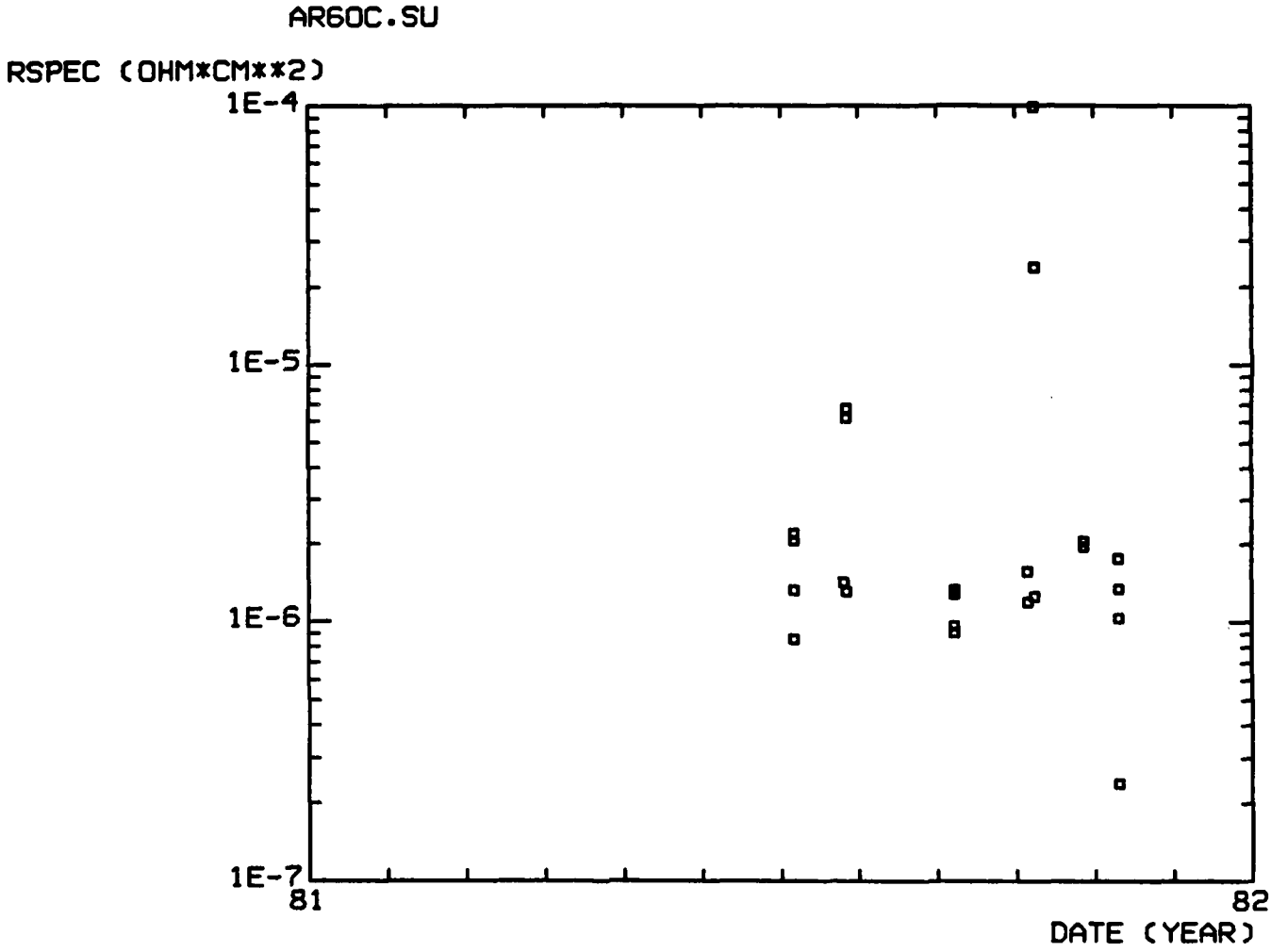


Fig. 5 History of ohmic contact specific resistance for the AR6 wafes. Each data point represents the average over one wafer.

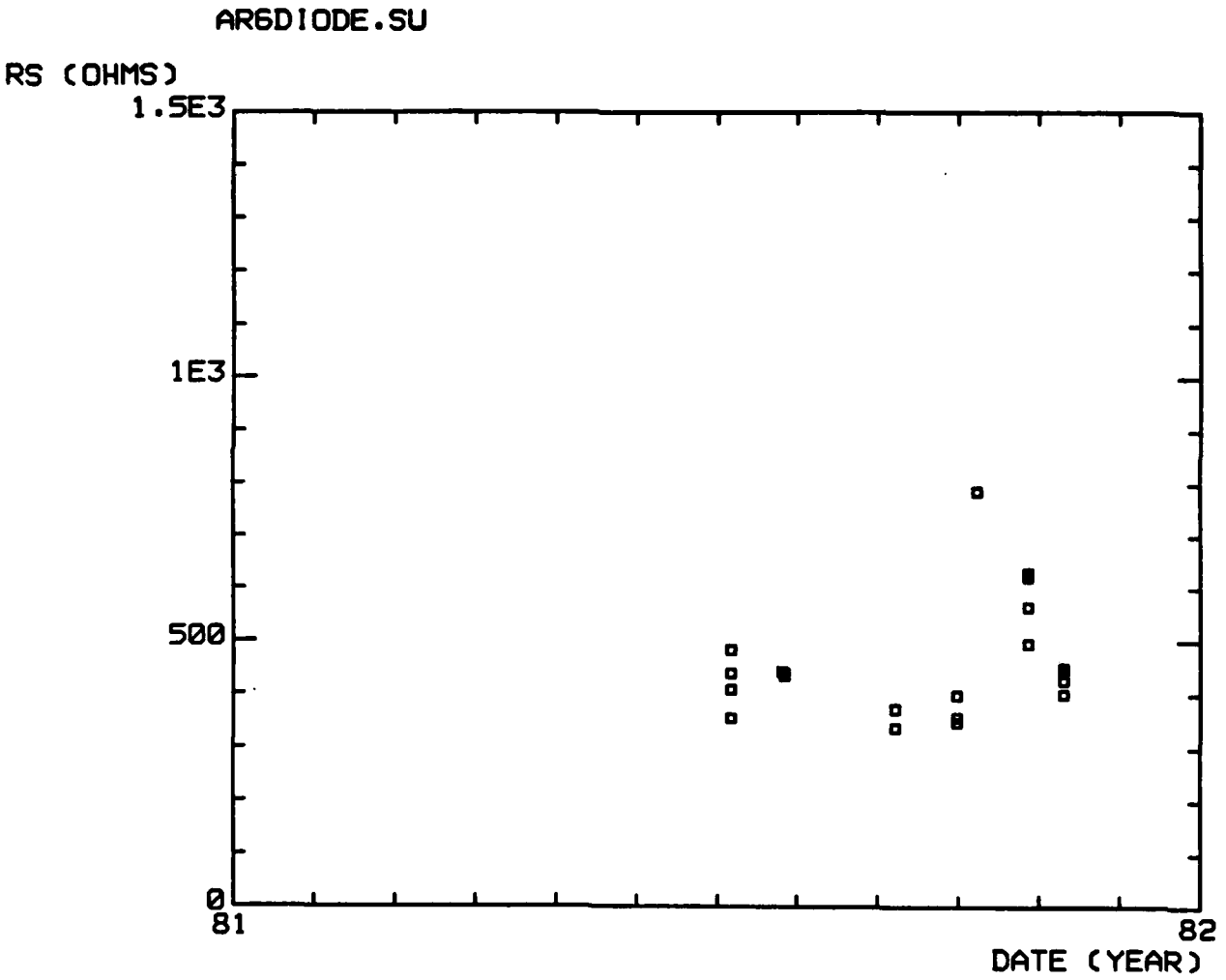


Fig.6 History of logic diode series resistance, R_S, for the AR6 wafers. Each data point represents the average over one wafer.

to 1.3 V range, with few exceptions. Figure 5 corresponds to the specific resistance of the ohmic contacts, which is lower than 10^{-5} Ω-cm^2 for all but two wafers, and near 10^{-6} Ω-cm^2 for the majority of the wafers. Finally, Fig. 6 corresponds to the series resistance of the logic diodes, which all fall in the desired R_S<800Ω range, with most wafers below 500Ω. Other characterization measurements not discussed here include verification of carrier concentration profiles (automatic) and verifications of metallization and interconnect resistance and crossover capacitances.

The above results are quite satisfactory. Table 1 contains a summary of the parametric test results. Of 25 wafers on which fabrication was completed (89% of the starts), 20 (80%, or 75% of the total) exhibited a threshold voltage within the acceptable range, were considered acceptable for circuit testing.

Table 1

Summary of Fabrication Results from AR6 Wafers

Number started	7 × 4 = 28
Number completed	25 (89%)
Number with required diode Rs range (<800Ω)	25 (89%)
Number with required V_p range (0.9V < V_p < 1.2 V)	20 (71%)
Number acceptable for circuit testing	20 (71%)

4.0 CIRCUIT RELIABILITY

The investigation of the reliability of GaAs integrated circuits is more complex than that of discrete MESFETs. The complexity is due to the use of more complex metallization systems, the need to maintain isolation between devices, the large number of transistors and diodes on a chip, the complexity of the dielectric systems, the length of interconnections, and the existence of large numbers of crossovers. In the last report, the result of high temperature storage tests of 9-stage ring oscillators was presented. The data showed an activation energy of 1.41 eV for degradation, and a lifetime of more than 10^{13} hours at room temperature was predicted. These figures are comparable to those that have been reported for discrete GaAs MESFETs.

During the last reporting period, reliability studies have been carried out on circuits under bias. Ring oscillators with 9 inverter stages were chosen for this study. Each stage in the circuits contained a 10μm wide switching FET, an 8μm wide pull-up active load, and a 2μm wide pull-down transistor, all with a gate length of 1μm. The circuits were packaged into 24-pin flat-packs, which could accommodate six devices in each package, and were suitable for high-frequency operation. The packages were mounted in a test fixture in which the flat-pack leads were pressed using O-ring material onto two ceramic substrates. The substrates were separated by the width of the flat-pack. The substrates had a gold line patternd designed to match the package leads, and such that the lines had 50-ohm characteristic impedance. The substrates were placed in a copper outer shell on which the SMA connectors and dc feedthroughs were mounted to connect the metal lines on the substrates to the outside wiring. The coaxial cables and the wires used were chosen to have Teflon coating so that they could be used at high temperatures. A bench-top forced-air convection oven was used to provide the high temperature environment.

The power supply biases were applied to the circuits through a switch box in which each line was connected in series with a low power fuse so that

the shorting of one device would not affect other devices. The readings of the supply current values and the frequency of oscillation of each device could be selected by the switch box. The oscillation frequency was measured with a spectrum analyzer.

Two temperatures, 200°C and 250°C, were selected for high temperature testing; the tests were carried out in flowing N_2 ambient. From room temperature to high temperatures, the current values, I_{dd} and I_{ss}, of the devices increased, and the oscillation frequency decreased. The increase of the currents is explained by built-in potential changes at the Schottky gate and the channel-substrate interface of the FETs, and the decrease of the frequency is presumably due to the lower electron mobility at high temperatures. When the devices reached the testing temperature, the operations of the devices stablized, and the degradation with time was very slow. At 200°C, five devices were tested for a period of more than 400 hours. The normalized values of the oscillation frequencies of the circuits as functions of aging time are shown in Fig. 7. Four devices were started at 250°C, but one ceased operation after 70 hours due to instrumentation problems, not device failure. The other three were tested for about 400 hours. The oscillation frequencies are plotted against aging time in Fig. 8. The devices degraded at a faster rate than those aged at 200°C, but most of the degradation occurred during the first 150 hours of operation. After that time the devices stabilized and degraded at very slow rate.

For estimating the lifetime of the devices, the failure of a ring oscillator was arbitrarily defined as the point when the frequency of oscillation at the given temperature reaches a 20% degradation. At 200°C, a median life of 3700 hours was estimated from Fig. 7. At 250°C, because of the nonlinear relation between the oscillation frequency and the aging time, a worst case median life was estimated by using the data from the first 150 hours of operation. In this way a median life of 35 hours was obtained. By plotting the median life against the inverse of temperature in a semi-log form, and joining the two data points with a straight line, as shown in

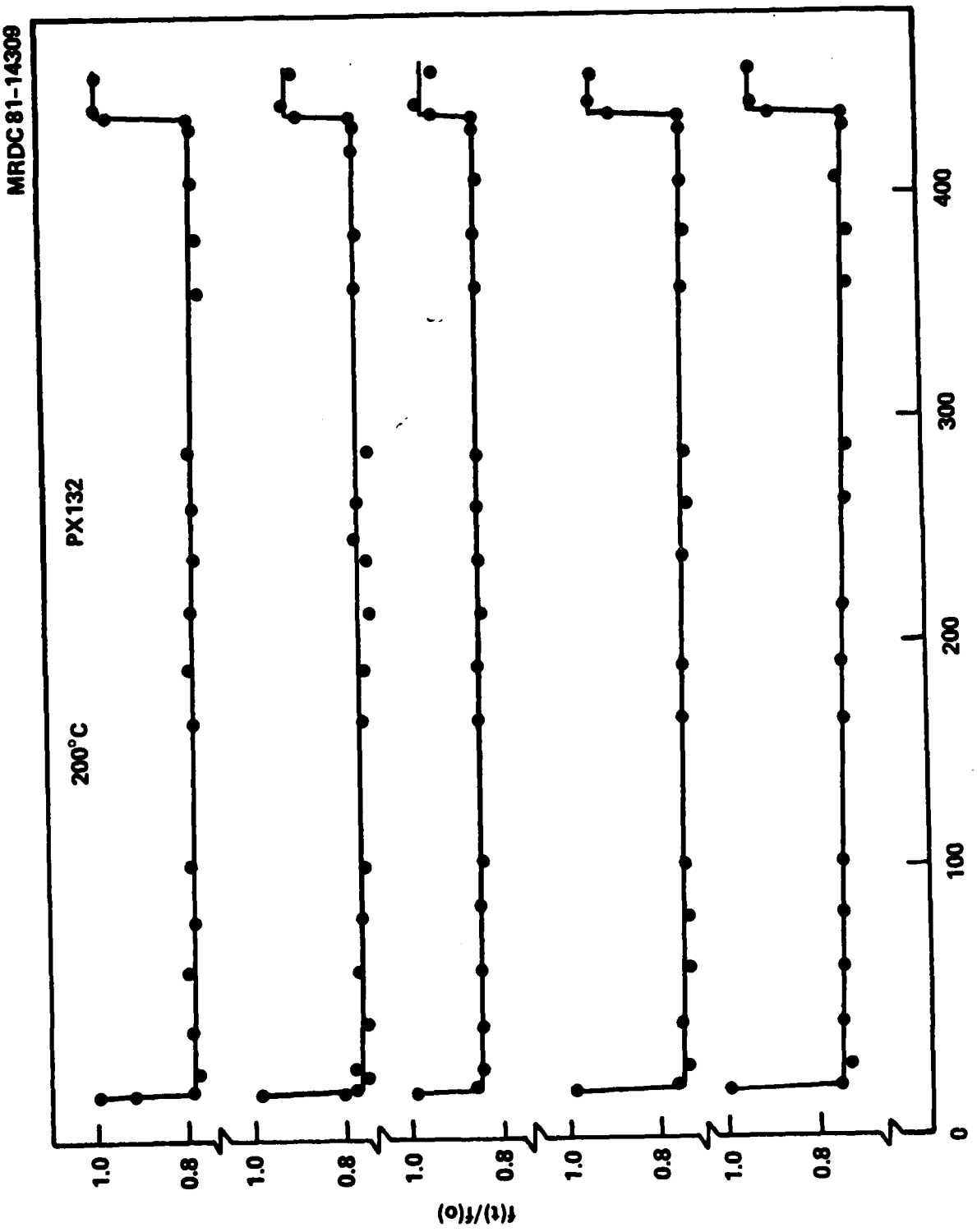


Fig. 7 Oscillation frequency vs time for five 9-stage ring oscillators operating at 200°C. The frequencies are normalized to the room temperature frequency at t = 0.

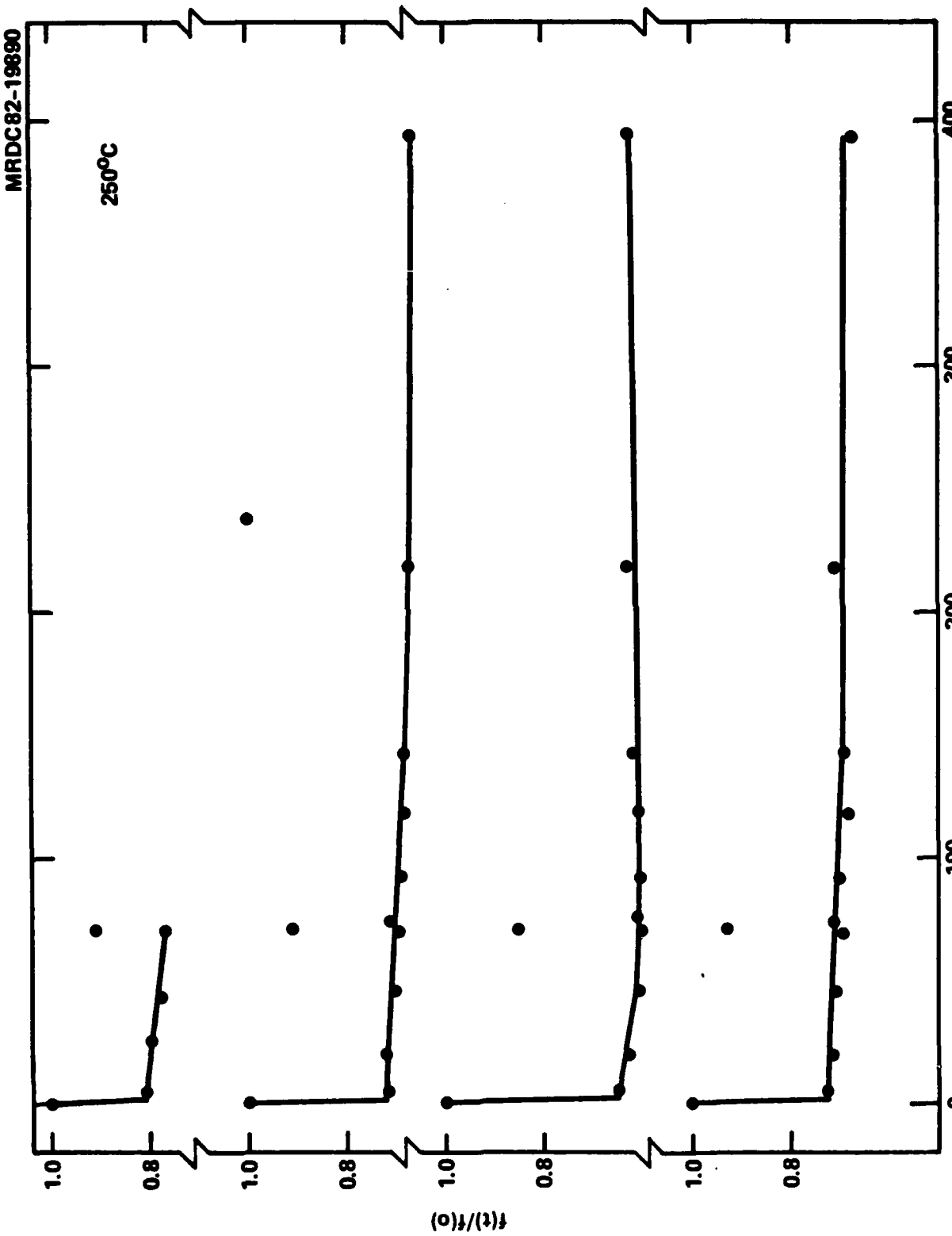


Fig. 8 Oscillation frequency vs time for four 9-stage ring oscillators at 250°C. The frequencies are normalized to the room temperature frequency at t = 0. The failure of one device was due to an

Fig. 9, an activation energy of 0.98 eV was obtained. If the straight line is extrapolated to room temperature an estimated lifetime of more than 10^9 hours is obtained.

It should be noted that the extrapolation technique used above is valid only for gradual (or slow) degradation; catastrophic failures are not included. No such failure was observed in 400 hours of aging at 200°C and 250°C for the small population tested. Although these results are very promising, a much larger sample population needs to be tested, and more temperature data points need to be obtained.

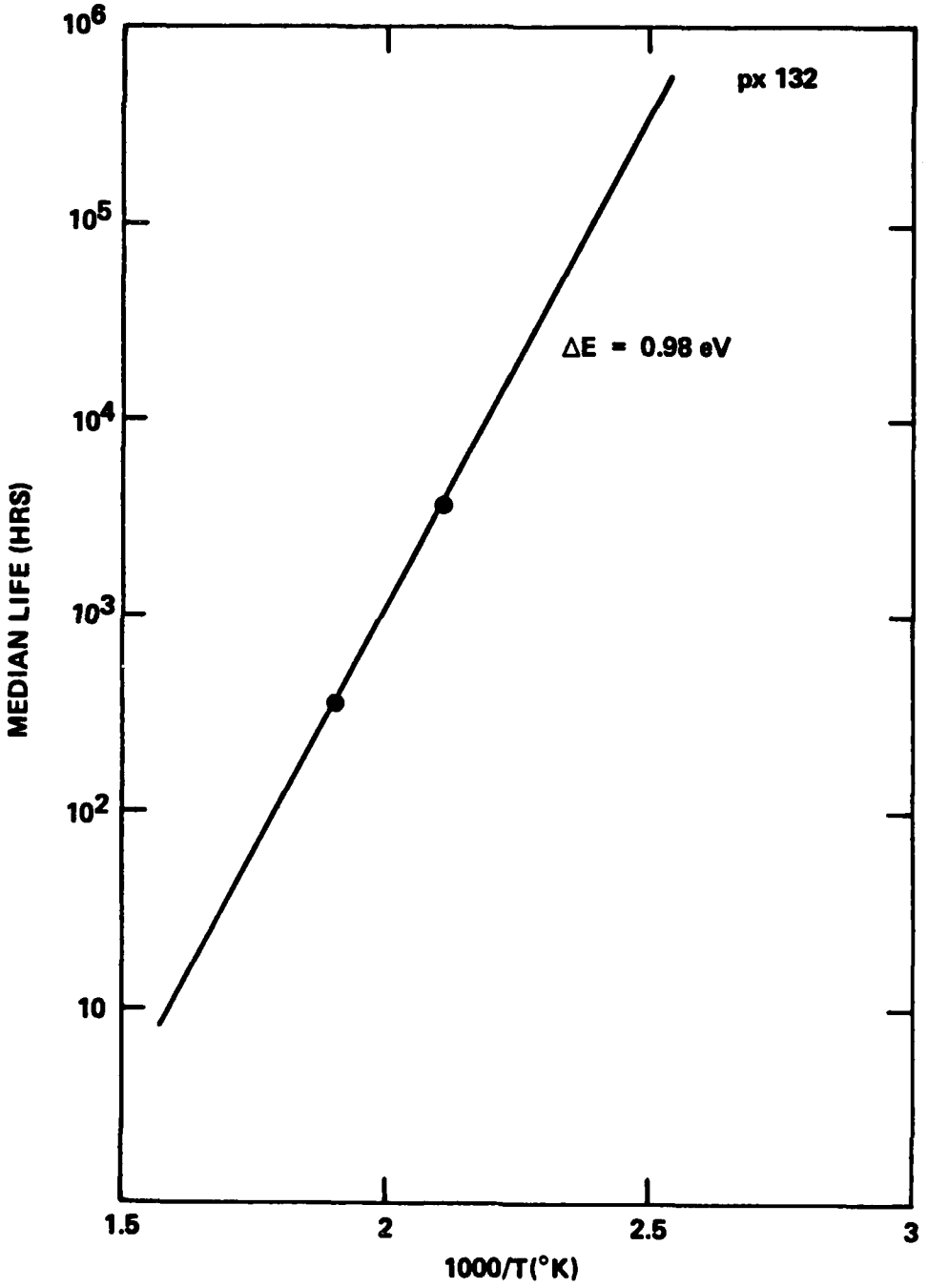


Fig. 9 Arrhenius plot for the medium lifetime of 9-stage ring oscillators. Failure was defined as the point when the oscillation frequency at the given temperature degrades by 20%.

5.0 MESFET MODELING

The modeling activities at North Carolina State University have been focused on three topics.

1. Two-Dimensional Numerical Analysis

The device structure to which the numerical modeling is being applied is shown in Fig. 10. As previously reported, the basic structure is an ion implanted FET with a gate length of 1μm and 0.5μm spacings on the gate and drain sides of the gate between the edges of the gate and the heavily doped source and drain regions. A typical impurity profile under the gate is shown in Fig. 11. Although the profile is only shown to about 0.3μm, a profile to 0.5μm has been used in many of the calculations.

The two-dimensional grid used in the calculations is illustrated in Fig. 12. A typical grid size has 60 × 15 points in the y and x directions respectively, so that the spatial resolution is about 0.033μm along both the channel direction and perpendicular to the channel. The calculated results have been found to be relatively insensitive to the size of the grid, at least for the grid sizes used in this work.

In addition to doping gradients perpendicular to the channel, doping gradients are included at the contacts to model the second ion implantation used to form the source and drain regions.

The computer calculations give detailed results on the internal operation of the FET device. Figure 13 shows a typical plot of electron concentration as a function of x and y when the drain potential is 2.5 V and the gate potential is zero. The peaked shape of the profile near the source and drain regions follows closely the implanted profile, as expected.

The ion implanted FET shows many of the same features which have been observed in calculations for uniformly doped channel FETs. If one considers an electron concentration profile deep within the device such as curve A of

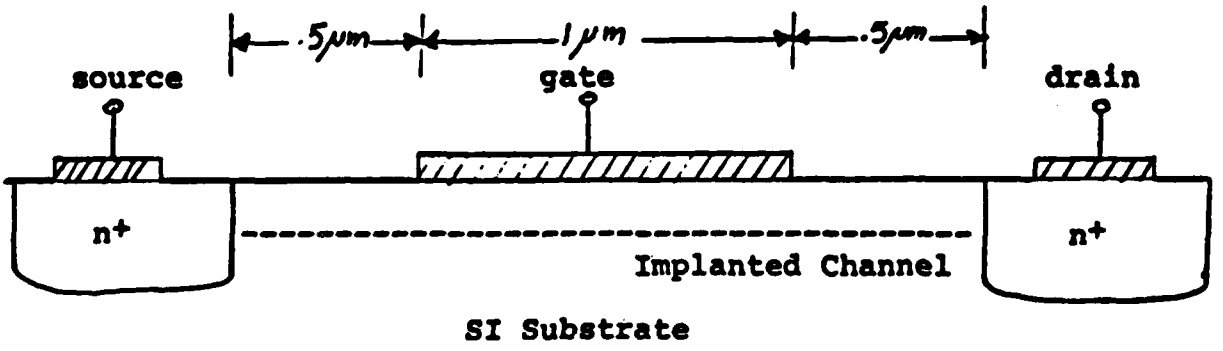


Fig. 10 FET structure used for two-dimensional analysis.

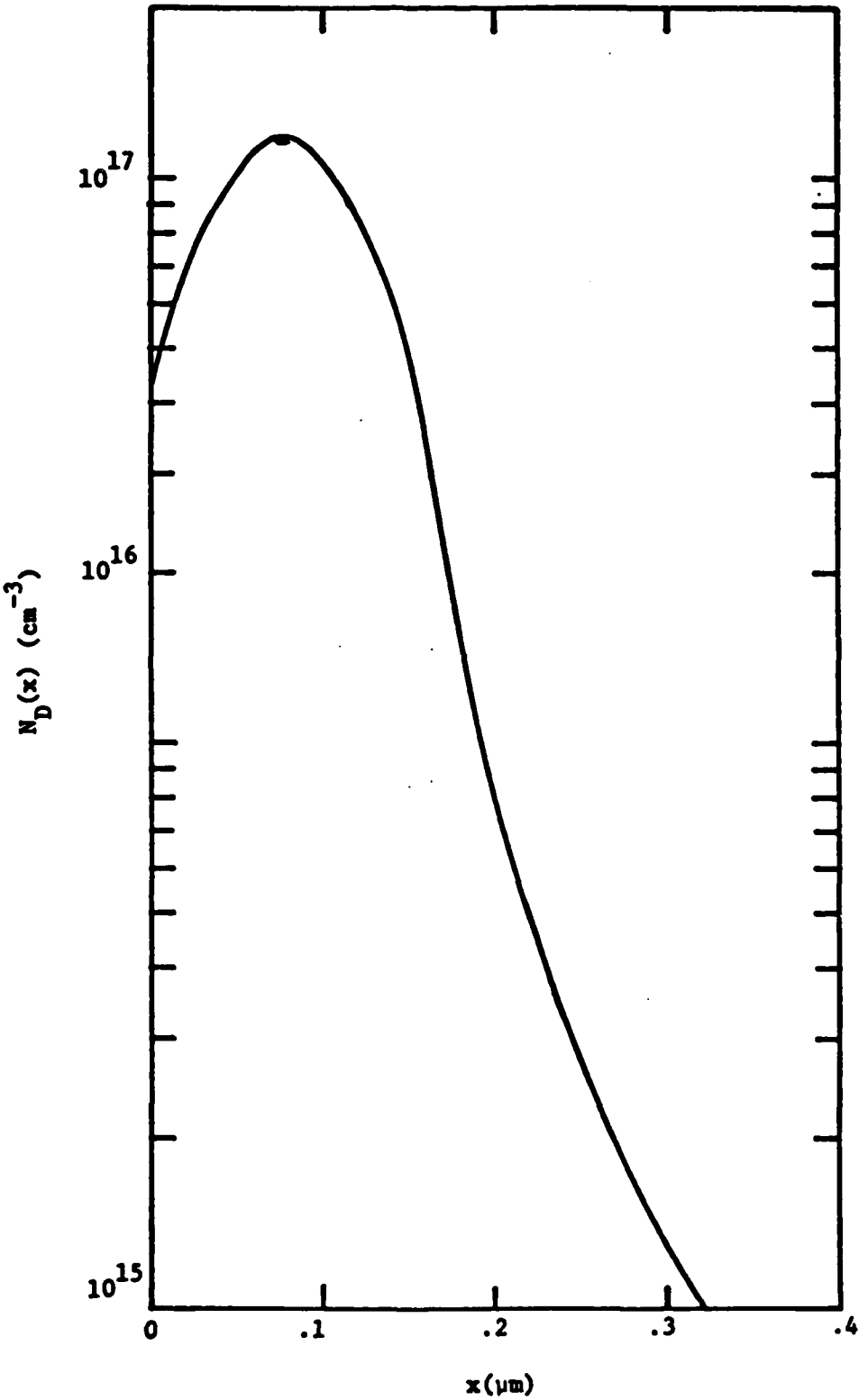


Fig. 11 Ion-implanted doping profile used in 2D modeling.

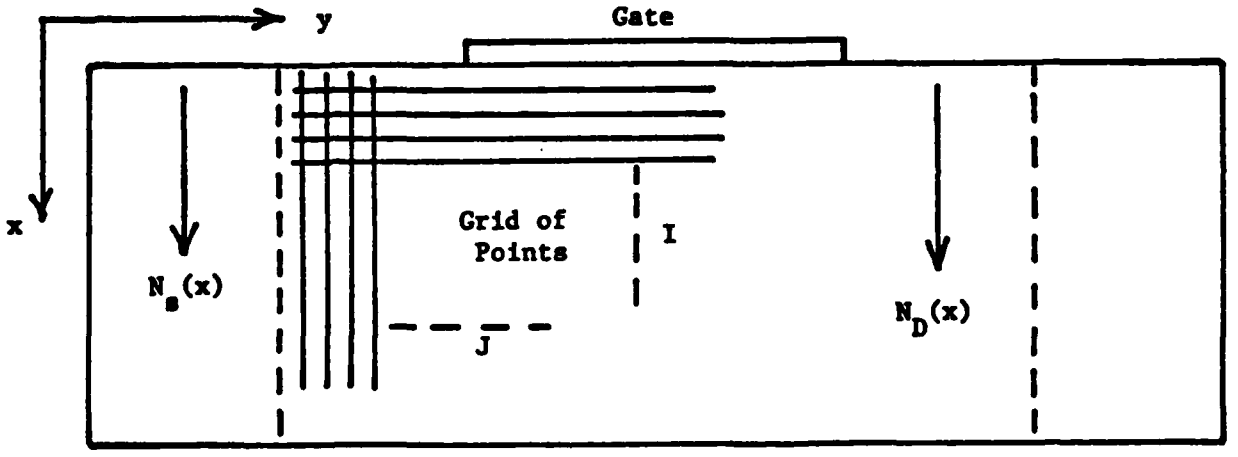


Fig. 12 Two-dimensional grid structure used in 2D modeling.

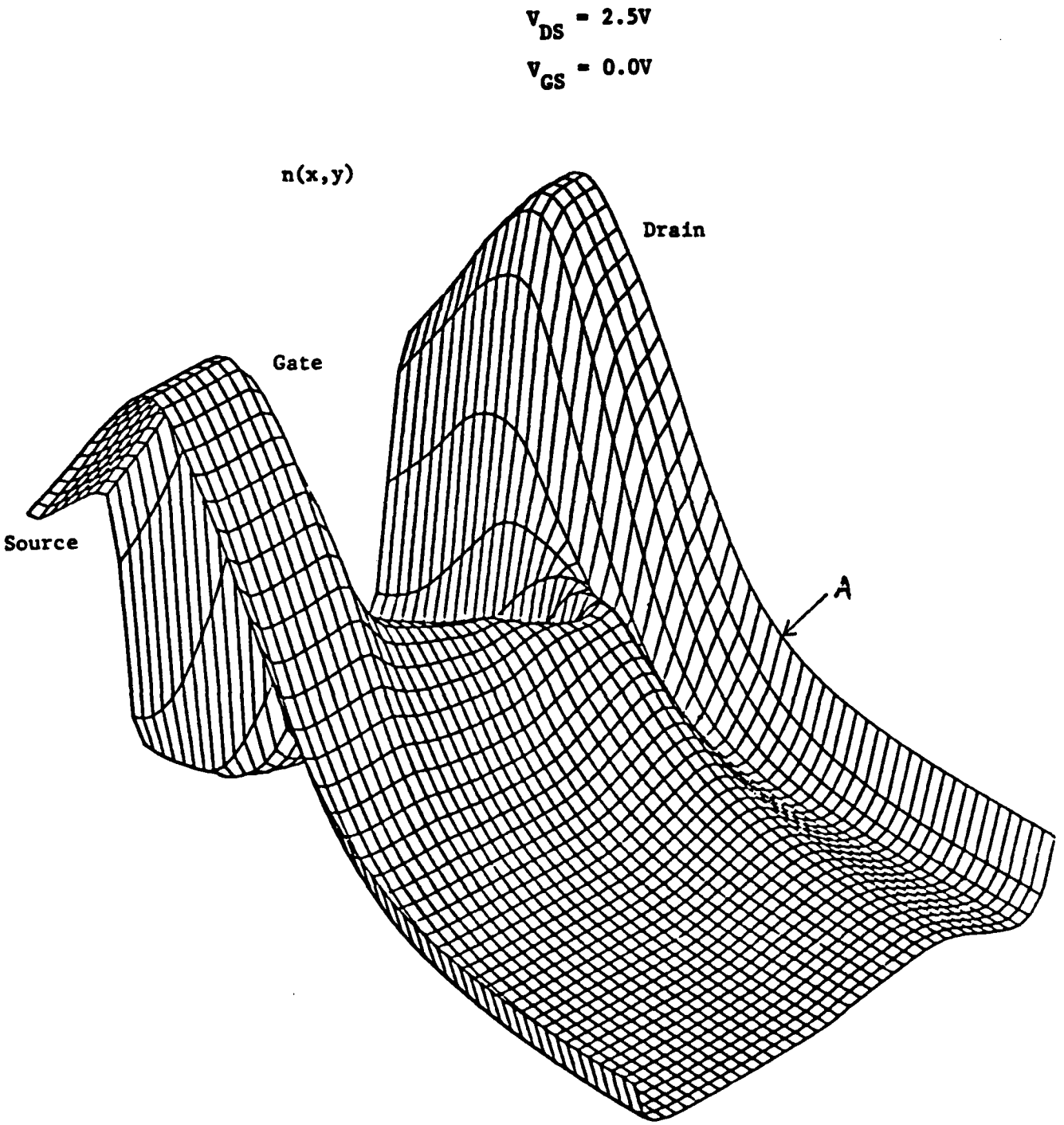


Fig. 13 Electron concentration in the channel region.

Fig. 13, it is seen that a hump exists in the electron concentration toward the drain end of the gate. This is an electron accumulation region which has also been seen in uniformly doped FETs. More difficult to see in Fig. 13 is a slight depletion of carriers beyond the accumulation region and closer to the drain.

Figure 14 shows current density in the x-direction as a function of position in the FET. The current is seen to flow close to the surface near the source and drain contacts, but is forced to flow deeper into the device under the gate because of the depletion region. It is also seen that the largest current densities occur near the source end of the gate, as opposed to a uniformly doped FET where the largest current densities would occur near the drain end of the FET. This is related to the accumulation layer of electrons discussed in connection with Fig. 13. Such accumulation causes a large electron concentration to exist fairly deep within the device. The bearing of these effects on switching times and small signal parameters remains to be explored.

Device characteristics and small signal parameters have been partially computed for a device with the impurity profile of Fig. 11. The results are summarized in the following figures:

Figure 15: I_{ds} vs V_{ds} for constant V_{gs}
Figure 16: g_m vs V_{ds} for constant V_{gs}
Figure 17: g_d vs V_{ds} for constant V_{gs}
Figure 18: C_{gs} vs V_{ds} for constant V_{gs}
Figure 19: C_{gd} vs V_{ds} for constant V_{gs}

The calculations need to be extended to lower voltages to complete the analysis. The general magnitudes and shapes of the curves appear to be reasonable when compared with experimental data, although no detailed comparison has been made so far. One point is worthy of note. The ratio of gate-to-drain capacitance to gate-to-source capacitance is approximately 0.1, which agrees with the experimental ratio of these capacitance.

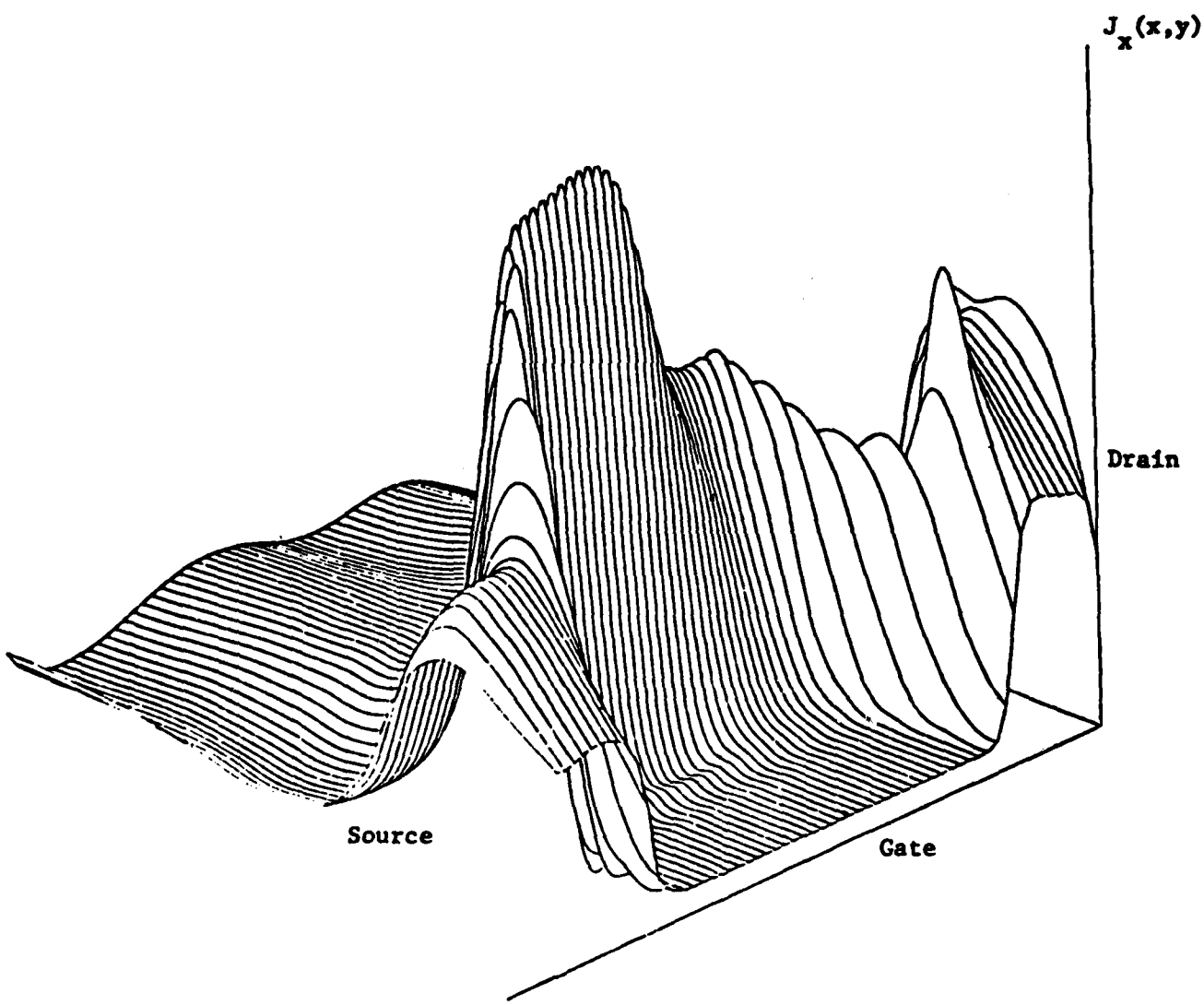


Fig. 14 Current density distribution.

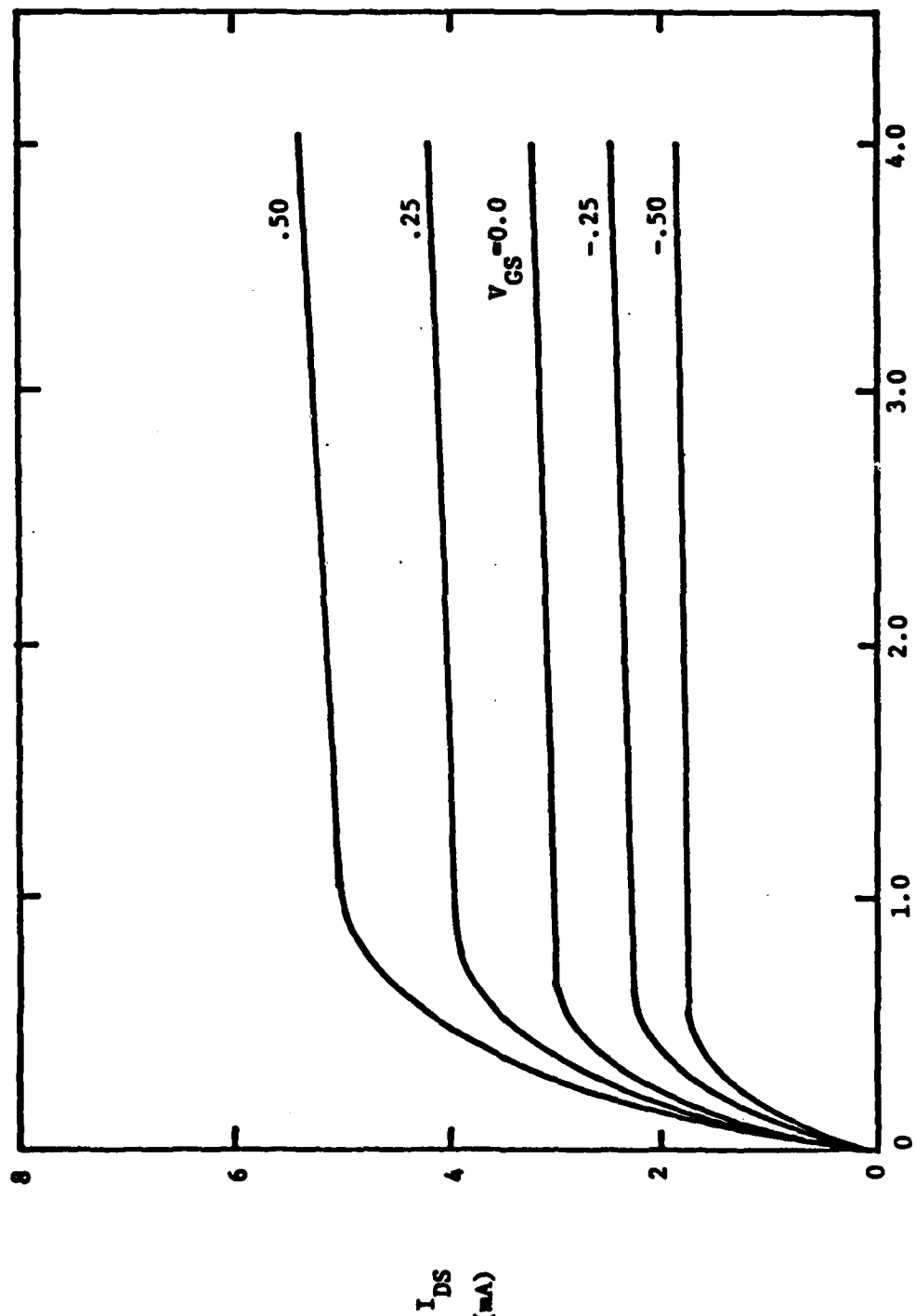


Fig. 15 I_{ds}-V_{ds} characteristics for ion-implanted FET.

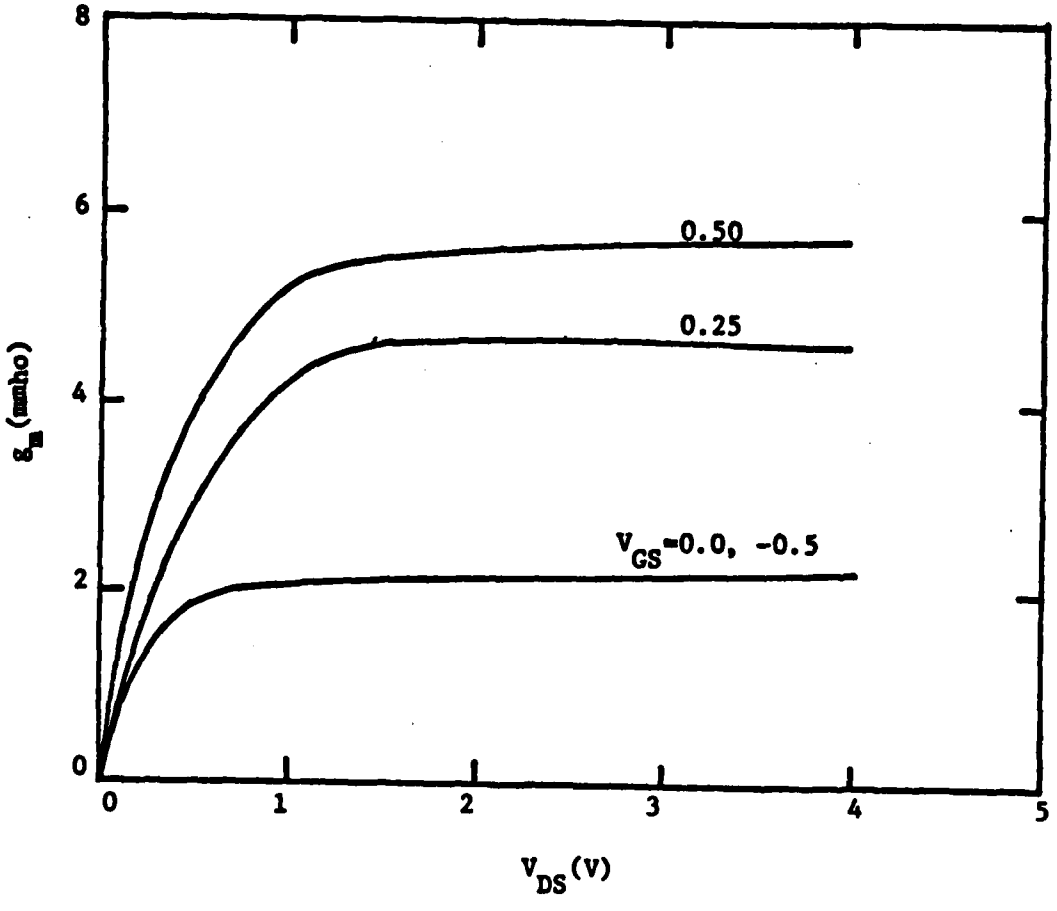


Fig. 16 g_m for ion-implanted FET.

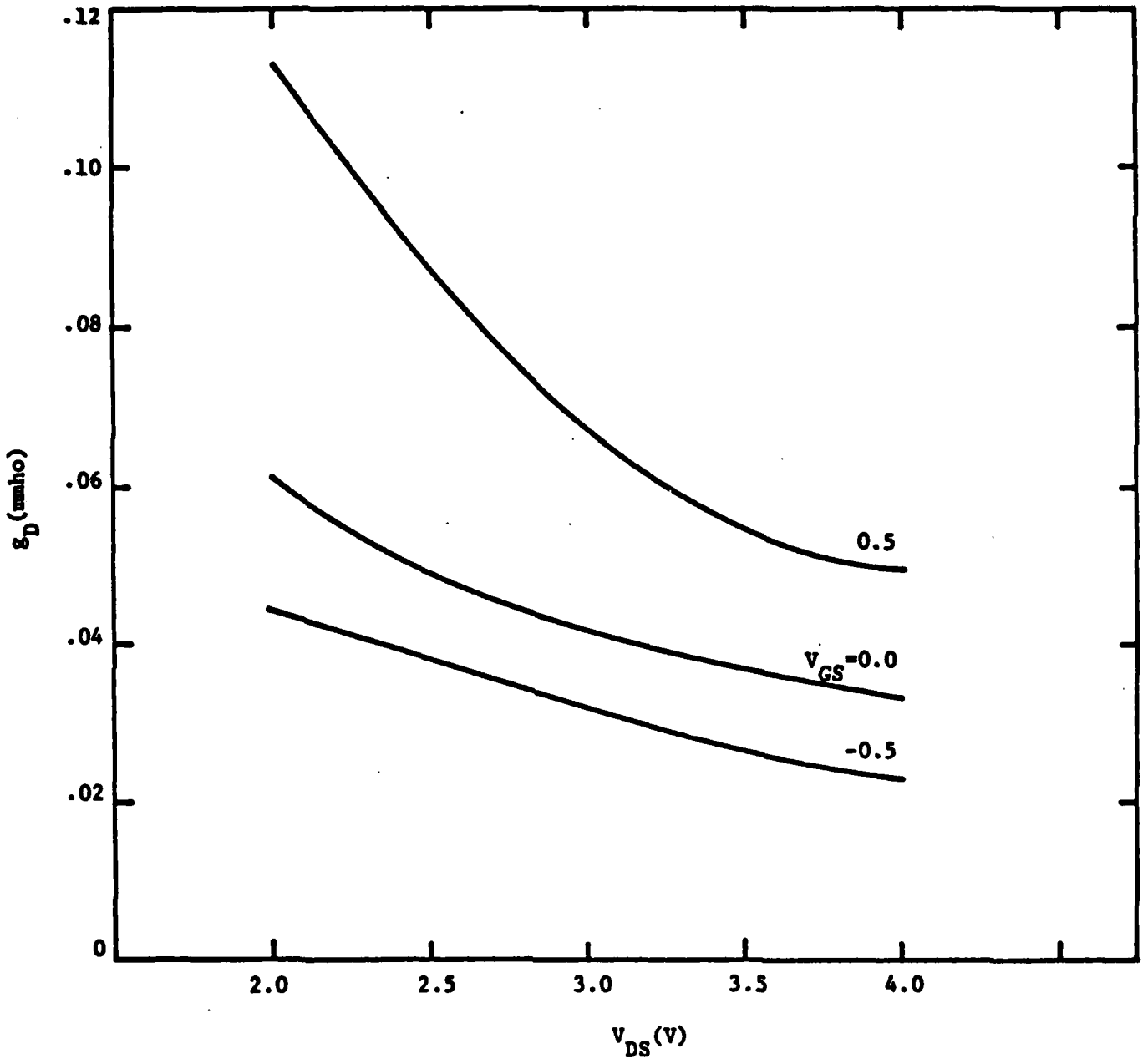


Fig. 17 g_d for ion-implanted FET.

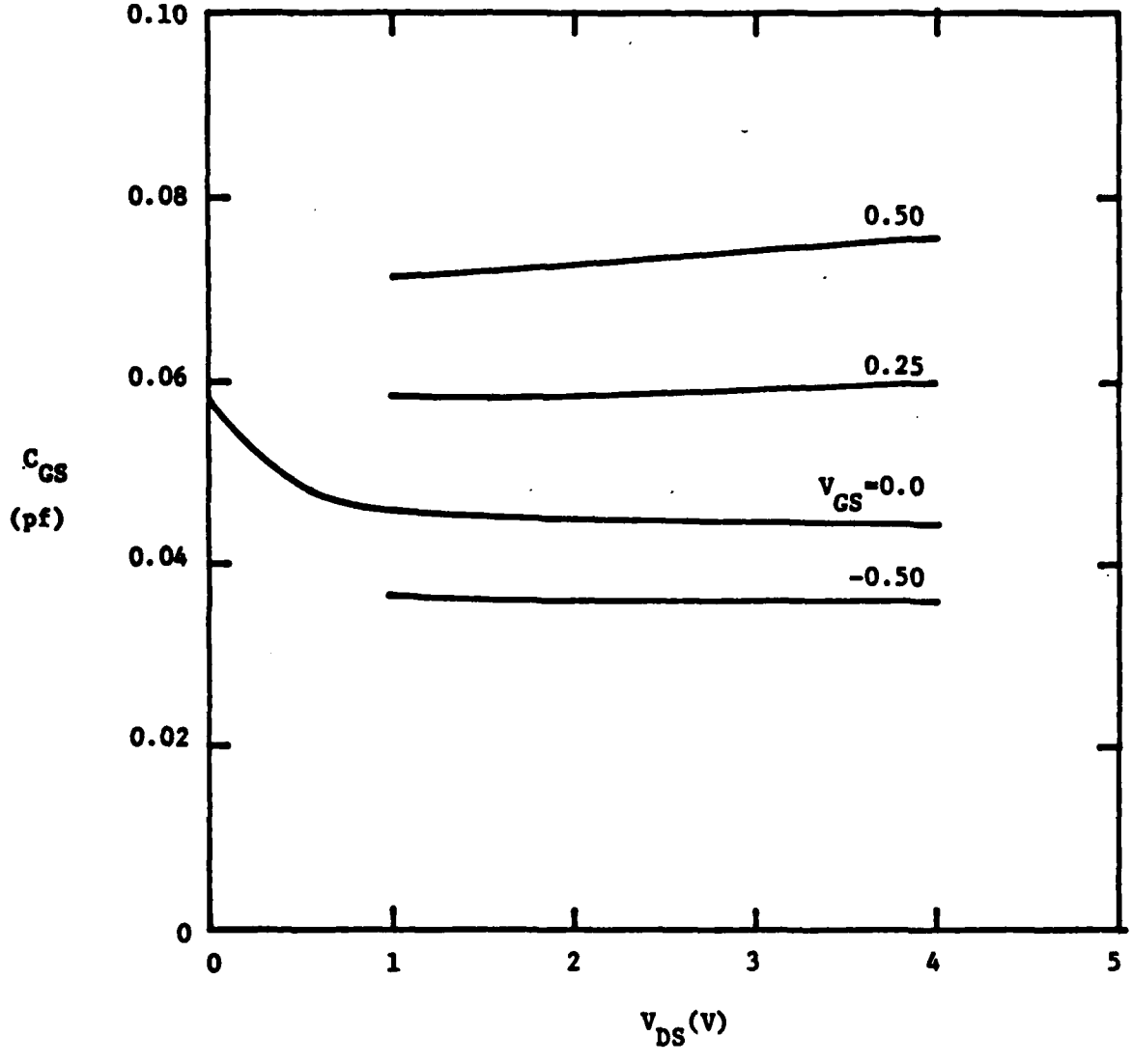


Fig. 18 C_{gs} for ion-implanted FET.

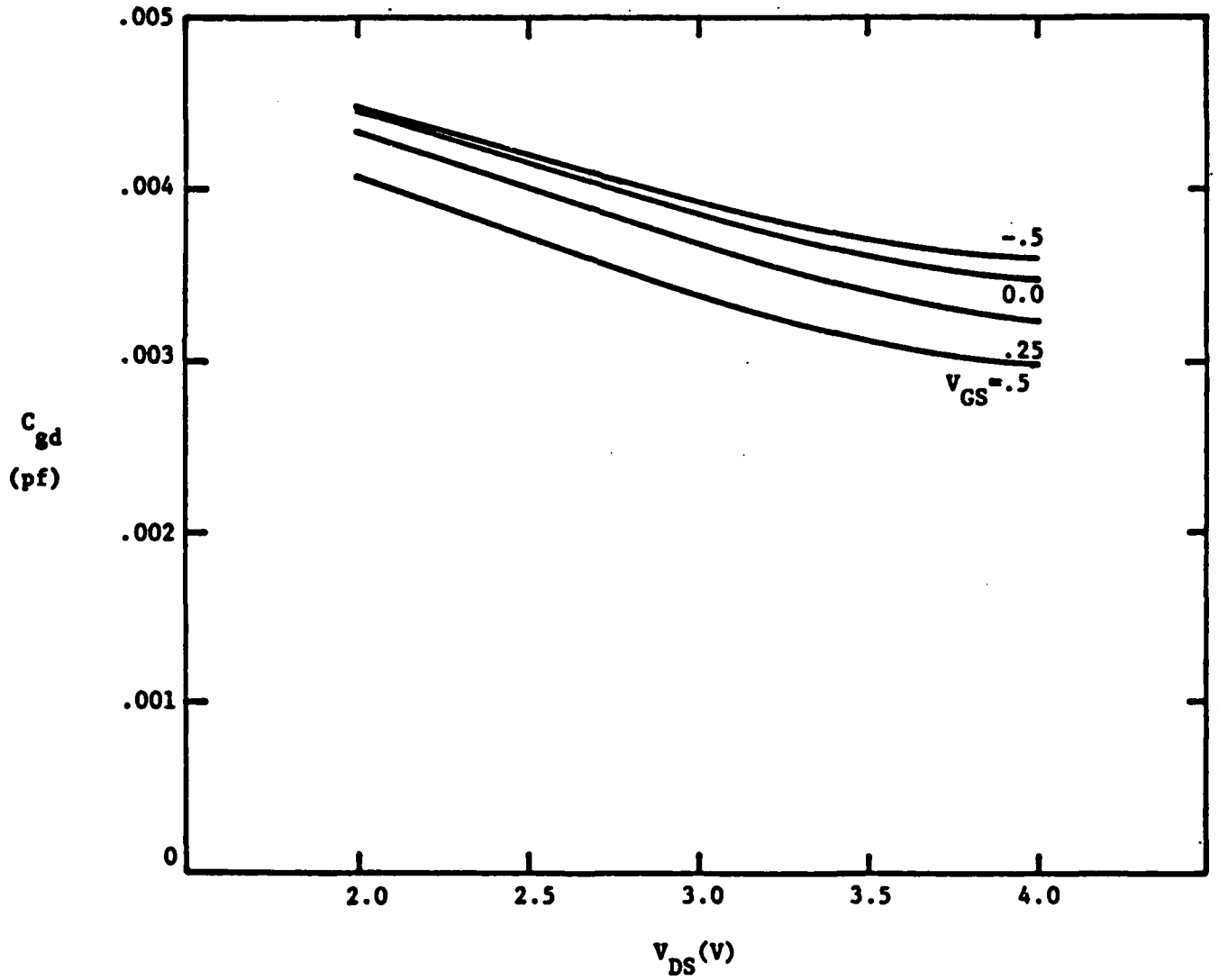


Fig. 19 C_{gd} for ion-implanted FET.

2. Analytical FET Model

The development of the one-dimensional analytic model is continuing. A general formulation for the source-to-drain current for a FET with an arbitrary channel impurity concentration profile has been completed. This current expression has been tested against the simpler expression for the flat profile device and excellent agreement is obtained. The general current expression has been used to obtain an expression for the device transconductance. Various experiments are being conducted for the ion-implanted device to investigate the effects of channel impurity profile on device transconductance. Work is progressing on the development of the general capacitance expressions. Also, since the model requires the use of a two-piece, linear velocity-field characteristic, an improved method for obtaining an accurate saturated velocity is being developed. This method is based upon the gate region transit-time concept.

3. Monte Carlo Analysis

The two-dimensional Monte Carlo program has undergone a major change since the last reporting period. Originally, the procedure used was:

(1) Start an electron on either source or drain contact.

(2) Simulate that electron's movement through the device until it reaches one of the ohmic contacts.

(3) Go back to step 1 until either a specified number of interactions occur, or a specified number of carriers are simulated.

As previously reported, after one iteration through the Monte Carlo program and Poisson solver the results looked promising. However, when the iterative process was continued, erroneous domains developed and a valid solution could not be achieved. This problem arose due to the procedure of starting each electron on one of the ohmic contacts.

To avoid the problem just described, a two-dimensional "ensemble" Monte Carlo program was developed. In this program a large number of carriers (representing the distribution in the device) is simulated. The initial placement of the carriers is determined from the charge density p(x,y) obtained from a two-dimensional device analysis program. After all the carriers have been simulated for a short time, ΔT, the simulation is interrupted and the charge density and the electric fields are updated. The simulation then resumes for another ΔT. This iterative process is continued until a self-consistent solution is obtained.

The program just described was tested on a simplified FET. It was simplified only in that the doping density in the channel was assumed to be constant, at 5×10^{16} cm^{-3}. The structure of the device was otherwise the same as the one last reported. The operating voltages for the device were $V_{gs} = 0$ and $V_{ds} = 2.5$ V. Figures 20 and 21 show the initial new charge density and the initial potential obtained from the two-dimensional device analysis program. Figures 22 and 23 show the net charge density and the potential obtained from the two-dimensional "ensemble" Monte Carlo program after a self-consistent solution is reached. The most noticeable effect on the new charge density is that the accumulation-depletion region near the drain is narrower and is nearer to the drain in the Monte Carlo results than in the result of the 2D device analysis. This difference may be due to the fact that the Monte Carlo analysis does not assume static velocity-field characteristics; i.e., in the 2D analysis a carrier is assumed to respond instantaneously to the electric field, whereas the Monte Carlo simulation accounts correctly for transient response.

The two-dimensional "ensemble" Monte Carlo is currently being modified to allow simulation of the FET with non-uniform doping.

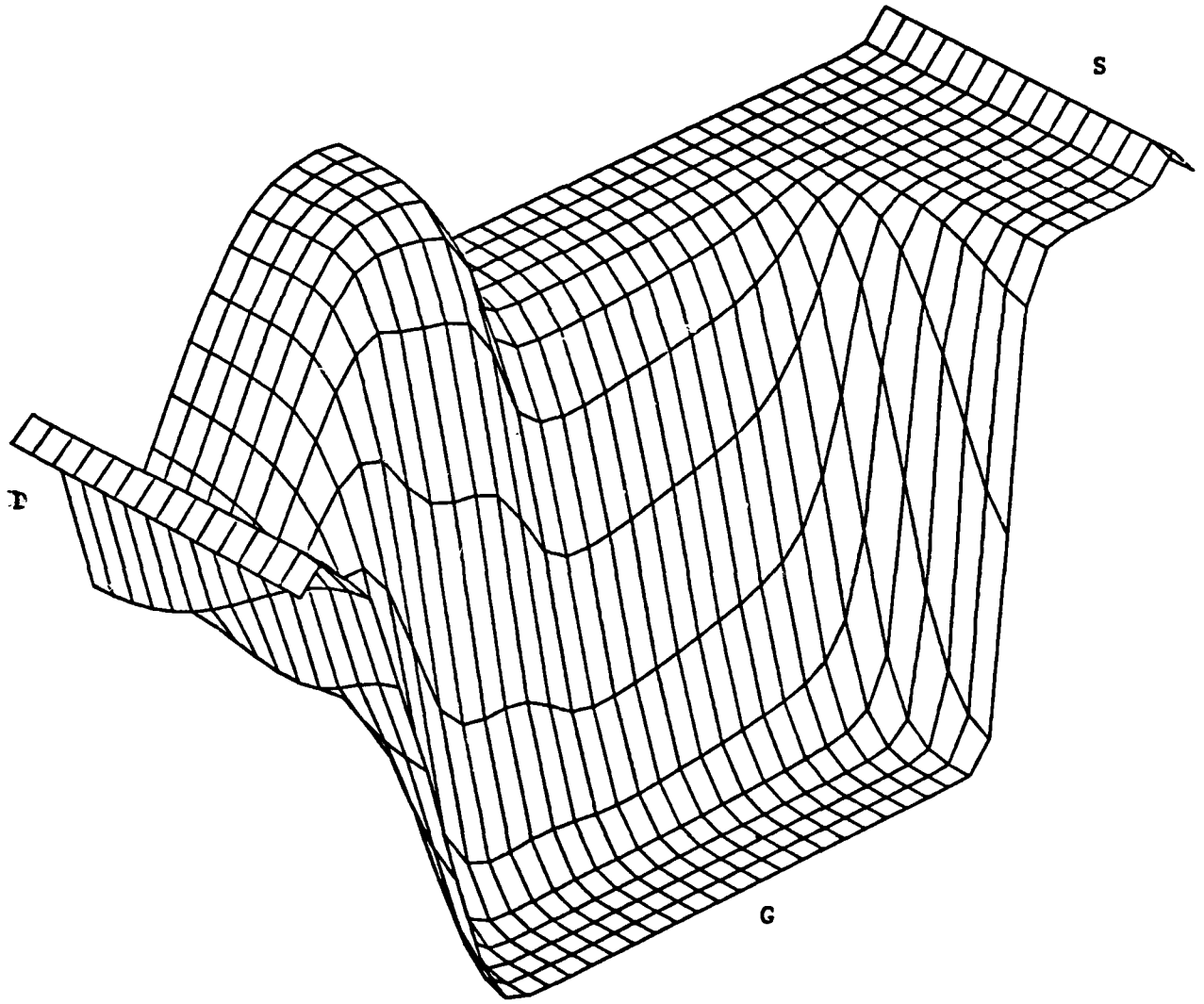


Fig. 20 Initial net charge density for a uniformly doped device.

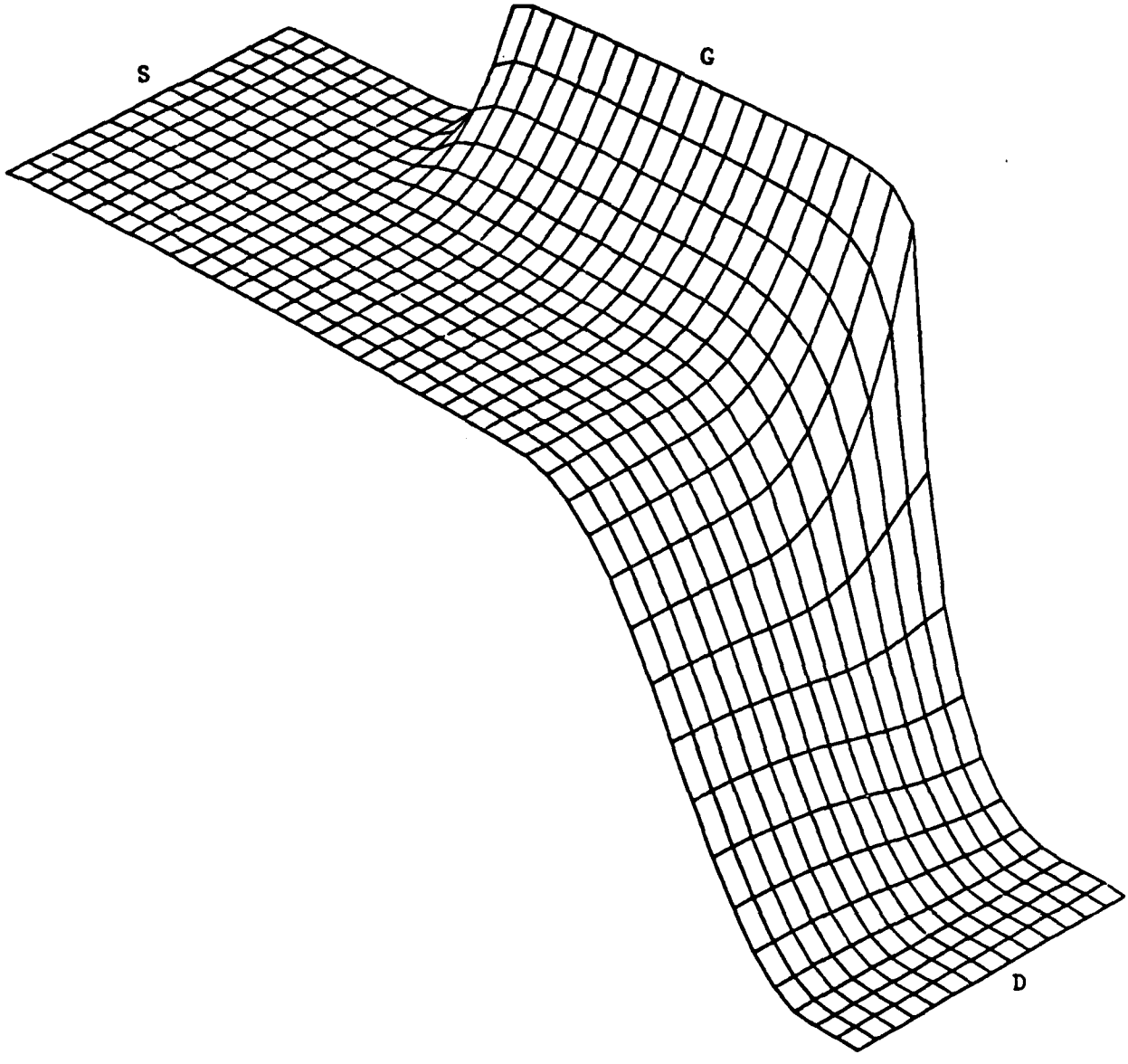


Fig. 21 Initial potential obtained from the device analysis program.

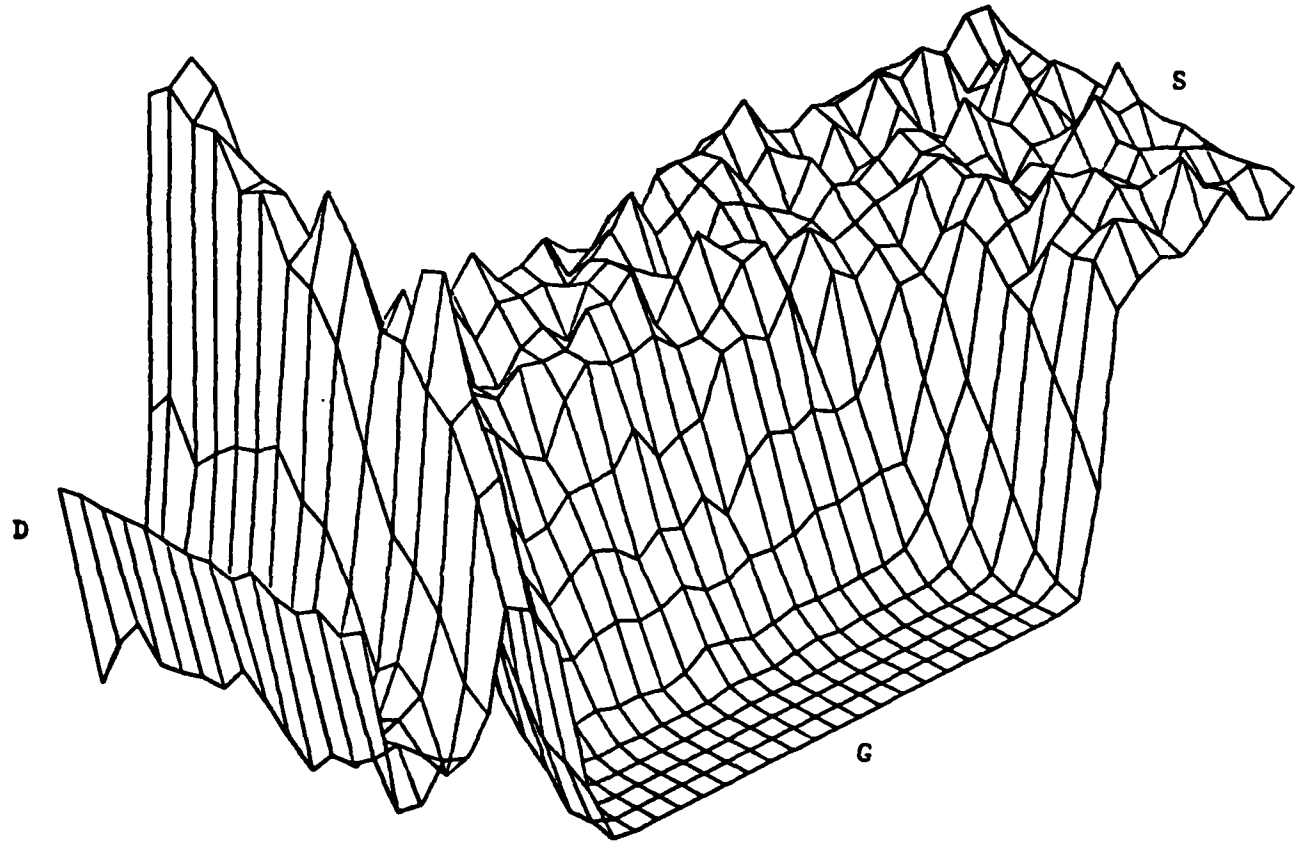


Fig. 22 Net charge density obtained a self consistent solution is reached.

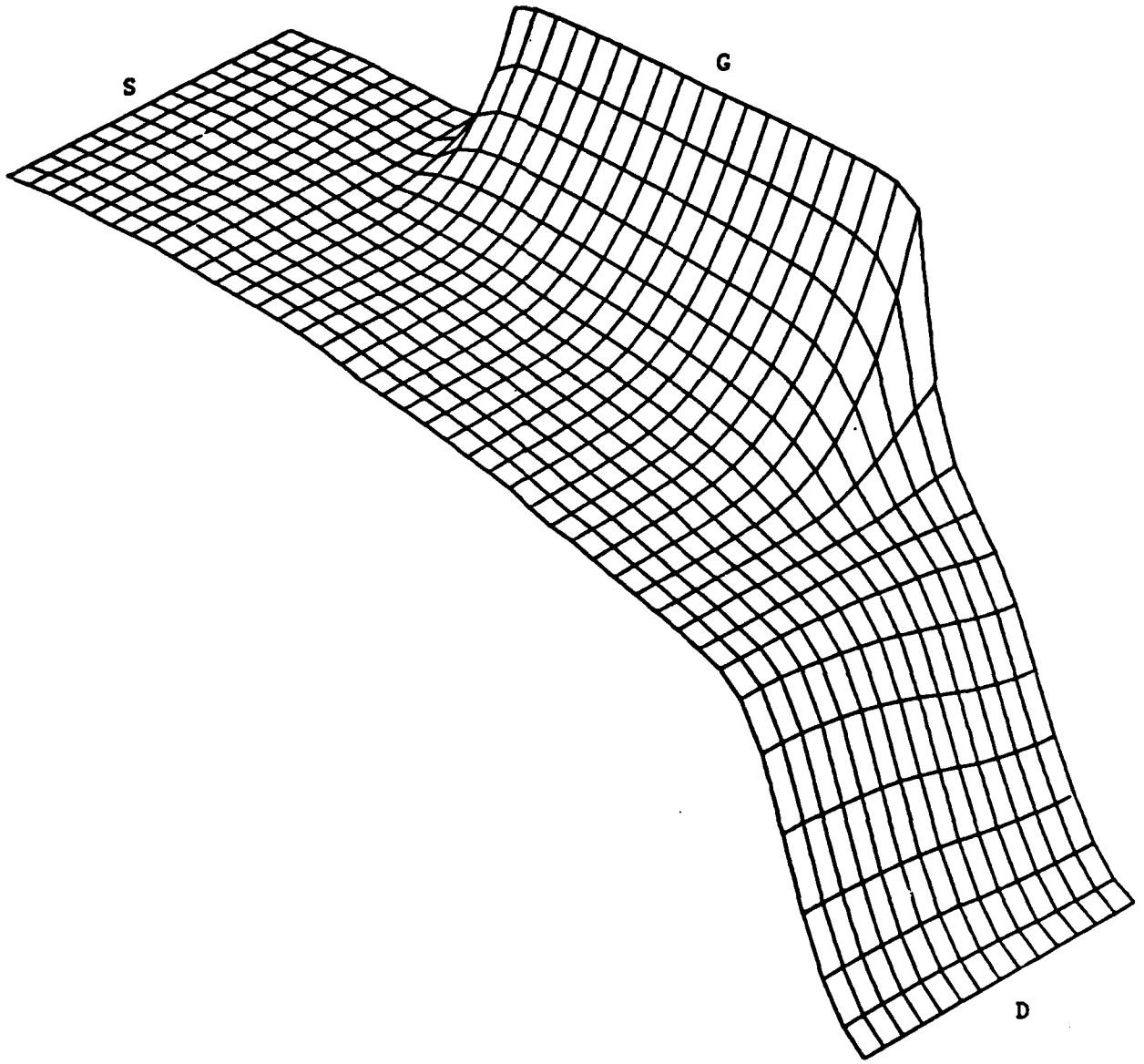


Fig. 23 Potential obtained from Monte Carlo analysis.