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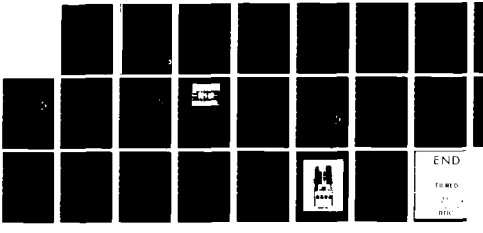

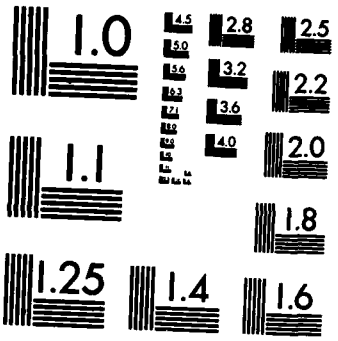

FET POWER AMPLIFIER FOR QUIET RADAR TRANSMITTER

J. B. Klatskin
R. L. Camisa
A. Mikelsons
W. J. Cvecich, Jr.

RCA Laboratories
Princeton, New Jersey 08540

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The report describes the design and performance of FET power amplifier modules for quiet radar requirements. In the initial part of this program suitable device types capable of operation at the 9.5- to 10.5-GHz frequency band were studied. FET combiner circuits were developed to increase power performance of FET chips. Power modules were designed and tested for inclusion into a prototype

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power amplifier. Module requirements were 4-dB gain with >1.2-W output power. Results obtained from a typical combined FET module were a power output of 1.3 W with 4.5-dB gain.

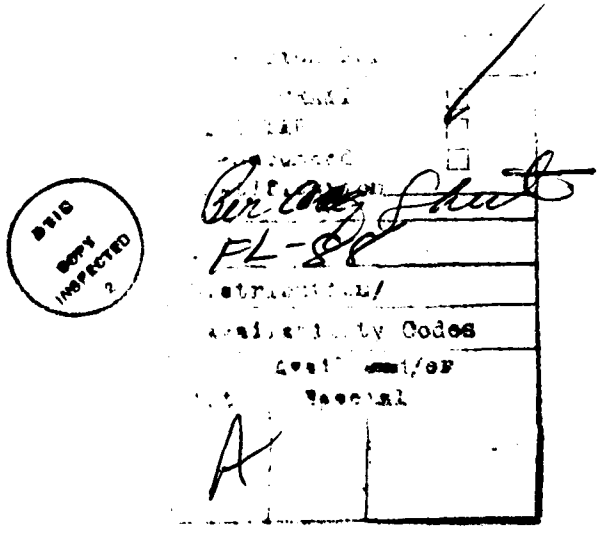
The final part of the program emphasized the construction of power modules for a conjoint power amplifier with 5-W output power. In all, seven 1.2-W and two 0.5-W modules were built and incorporated into the final amplifier. The following results were obtained from the completed unit: 5-W power output with a gain of 29±1 dB from 9.5 to 10.5 GHz.

PREFACE

This final report was prepared by RCA Laboratories, Princeton, NJ, under Contract No. DAAK40-77-C-0099 for The U.S. Army Missile R&D Command (MICOM), Redstone Arsenal, AL.

The project was carried out in the Microwave Technology Center, F. Sterzer, Director. The Project Supervisor is S. Y. Narayan, and the Project Engineers are J. B. Klatskin and R. L. Camisa. Other personnel who participated in the program were A. Mikelsons and W. J. Cvecich, Jr.

The MICOM Program Manager was G. T. O'Reilly.



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SECTION I

INTRODUCTION

The objective of this program was to develop an FET power amplifier for the 9.5- to 10.5-GHz frequency band. The original goals were 4 W with a gain of 26 dB. Technical Requirement No. 6187 was changed to read 10 W with a gain of 30 dB. In addition, techniques were to be developed to increase the power level available from a solid-state FET amplifier through the use of device combining. The program management stressed a reduction of the number of devices needed to fulfill the requirements listed in Table 1.

TABLE 1. PROGRAM SPECIFICATIONS

Power-Out	10 W
Bandwidth	9.5-10.5 GHz (1 dB) (operational bandwidth without tuning)
Linear Gain	30±1 dB across the band
Efficiency	10%
Maximum Number of Transistors on Output Stage	10
Input VSWR	1.5:1
Noise Figure	≤10 dB

These specifications were predicated on the commercial availability of GaAs FETs rated at 2.5-W output in this band. During the program, it was found that these devices would not operate satisfactorily. When devices with a lower-rated output power were used, an amplifier with the performance shown in Table 2 was realized.

TABLE 2. FINAL RESULTS

Power-Out	4.5±0.5 W across the band
Bandwidth	9.5-10.5 GHz (1 dB)
Linear Gain	31±1 dB across
Efficiency	10%
Number of Transistors on Output Stage	4
Input VSWR	1.6:1
Noise Figure	12.0-13.4

This report describes the design and performance of FET power amplifier modules and a 5-W FET power amplifier assembly. We also describe the evaluation and characterization of various available GaAs FETs. Sections II to V cover the following subjects:

Section II describes device investigations of the MSC* 88110, Raytheon** RPX-4310, and MSC* 88104.

Section III indicates the overall circuit design approach of the selected device type and individual module performance.

Section IV outlines the computer (CAD) circuit model and predicted circuit performance.

Section V describes the conjoint power amplifier performance.

*Microwave Semiconductor Corp., Somerset, NJ.
**Raytheon Co., Waltham, MA.

SECTION II

DEVICE INVESTIGATIONS

A. 2-W FET DEVICE

This program began with an investigation into the MSC 88110 FET device. The specifications of this device type are as follows:

Power at 1-dB compression: 2.0 W

Gain at 1-dB compression: 5.0 dB

Highest operating frequency: 12 GHz

The Chip-Pac* packaged device was received for this task.

TABLE 3. S-PARAMETERS OF 88110 DEVICE. (A) AS RECEIVED. (B) AFTER PARTIAL MATCHING

TITLE: 88110
DATA FILE: 88110

FREQ	S11		S21		S12		S22		STAB	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	K	GMAX
8000.0	.935	163.3	.429	-.800	.025	-8.90	.739	157.6	2.065	6.467
8500.0	.924	162.4	.403	-5.70	.025	-7.10	.746	153.6	2.634	5.023
9000.0	.925	161.7	.384	-8.10	.025	-3.70	.772	151.4	2.459	5.139
9500.0	.924	159.9	.370	-12.5	.026	-.600	.790	152.3	2.262	5.208
10000.	.922	157.6	.354	-16.8	.026	.801	.802	149.0	2.323	4.886
10500.	.897	155.6	.340	-22.6	.027	1.700	.826	146.8	2.792	3.678
11000.	.869	152.6	.311	-28.2	.027	.500	.836	144.4	3.801	1.882
11500.	.852	148.9	.294	-33.8	.027	1.400	.829	141.6	4.840	.558
12000.	.804	146.8	.273	-38.0	.027	1.601	.819	138.0	7.387	-1.63

(A)

TITLE: 88110 PARTIAL MATCH
DATA FILE: 88110 PARTIAL MATCH

FREQ	S11		S21		S12		S22		STAB	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	K	GMAX
9000.0	.619	-33.4	1.357	160.2	.124	106.1	.181	58.30	1.911	4.903
9500.0	.364	-94.3	1.446	116.8	.147	65.00	.096	-60.6	2.096	3.976
10000.	.267	153.7	1.352	73.00	.148	23.10	.279	-123.	2.209	3.396
10500.	.474	77.80	1.113	30.60	.126	-15.5	.426	-149.	2.319	3.015
11000.	.634	30.60	.795	-7.30	.095	-48.4	.525	-164.	2.834	1.835

(B)

The devices were measured in an RCA-developed coaxial test fixture that allows quick mounting without heating or soldering of the package. Table 3(A) and Fig. 1(A) show the measured S-parameters of a typical 88110 device. We

*Microwave Semiconductor Corp., Somerset, NJ.

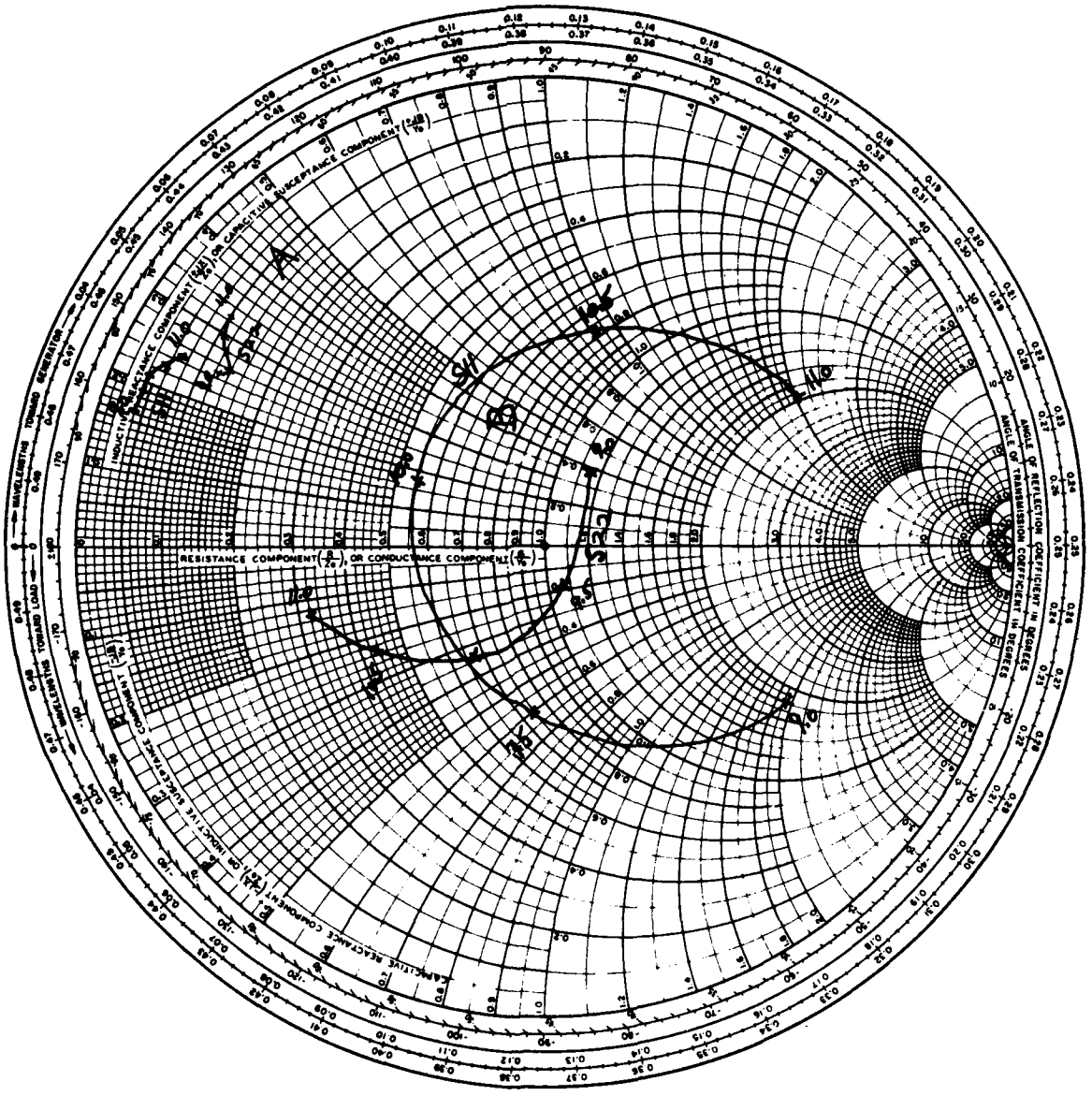

Figure 1. Plot of S-parameters of 88110 device. (A) As received. (B) After partial matching.

thought that use of the Chip-Pac series package, which has an exposed GaAs chip, would enable us to improve rf performance above 9 GHz. The Chip-Pac consists of an RCA-developed flip-chip mounting system in which the GaAs FET is flipped onto a heat sink. Since the device is mounted down with the source pads bonded onto the heat sink, the thermal resistance is reduced by one half. A second feature is a reduction of parasitic inductance between source and ground.

The predicted device performance, G_{max}, is an indication of device capability. For maximum power transfer and gain, matching networks at the terminals of the device must be used to provide conjugate matches to the frequency-dependent input and output impedances. Figures 1(B) and Table 3(B), respectively, show and list measured small-signal performance after the addition of partial-matching circuits at the device terminals. G_{max}, after partial matching, did in fact decrease, and thus predicted poor performance for this device series above 9 GHz. If this device type were capable of operating above 9 GHz, G_{max} would have increased after the reduction in the S_{11} and S_{22} terms.

High-power performance of FETs can be determined by an RCA-developed load-pull test system. This system permits measurements of power-out, gain, and efficiency of an FET under large-signal conditions. Figure 2 shows the conjugate S_{22} required for best power-out for the 88110 series chip.

Figure 3 depicts the gain response at best match with a power-in of 400 mW. The insert in Fig. 3 shows device performance with only the on-carrier matching network. It is clear that the Microwave Semiconductor MSC 88110 device series cannot be utilized for this program, since the minimum acceptable gain must be greater than 4 dB at the desired frequency band.

B. 1.2-W "VIA-HOLE"* FET DEVICE

An investigation into the Raytheon RPX-4310 device series was initiated. This FET is specified to provide 1-W output power with a gain of 6-8 dB at 10 GHz. A "Via-hole" technology is used to reduce source inductance. In our evaluation two such devices were employed. Table 4(A) lists the initial S-parameter measurement data on the received devices. This information was used to design a matching circuit for the 9.5- to 10.5-GHz frequency band. Figure 4(A) shows the plot of the S_{11} and S_{22} terms prior to matching. Table 4(B) depicts the S_{11} and S_{22} terms with a matching circuit. In Table 4(B) note the drop in predicted gain (G_{max}) after inclusion of the matching circuit. This comes about due to a more accurate measurement when reflections are reduced on the input and output ports.

The forward transmission term, S_{21}, also increased, as it should, with the matching circuit. Figure 5 is the completed circuit, fixture, and RPX-4310 FET.

*Raytheon Co., Waltham, MA.

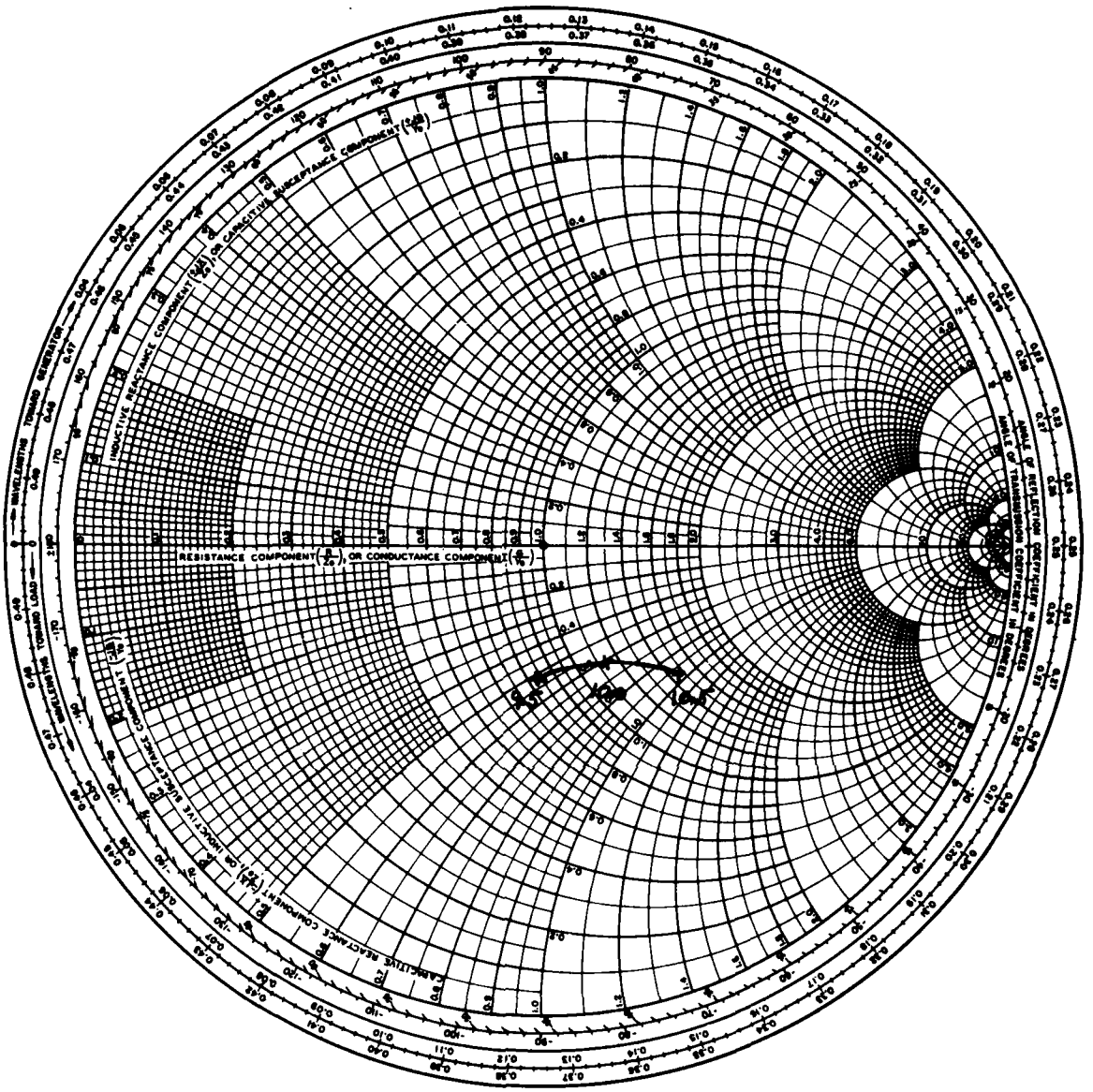

Figure 2. S-parameters of 88110 device under large-signal conditions.

Figure 6 depicts small-signal gain response, S_{21} (dB), for the RPX-4310 in the circuit. Power performance measurements in this circuit yielded 1.2-W out with only a 2-dB gain at 9.75 GHz; however, the power curve followed the small-signal gain curve shown in Fig. 6.

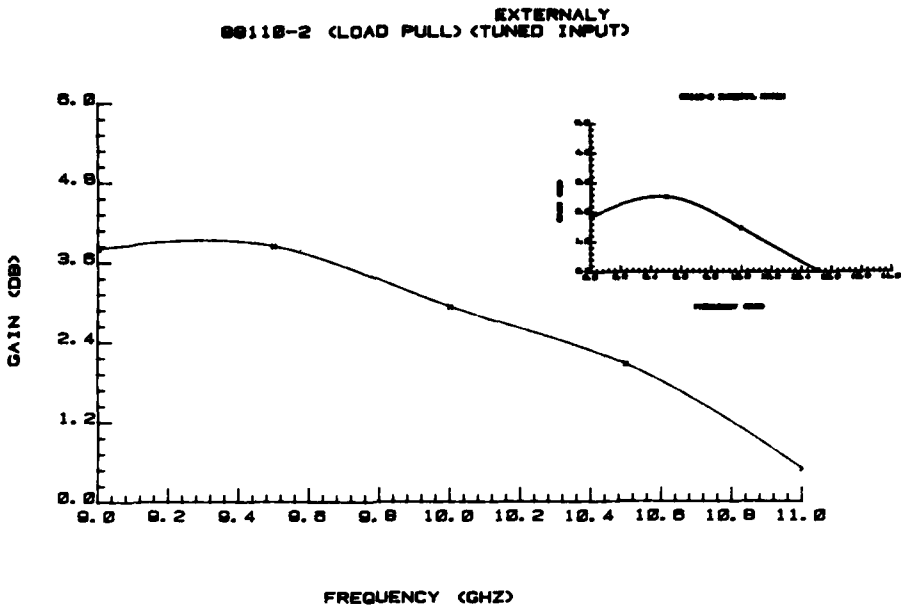

Figure 3. Gain response with matching network.

TABLE 4. S-PARAMETERS OF RPX-4310 DEVICE. (A) AS RECEIVED. (B) AFTER PARTIAL MATCHING

TITLE: RPX-4310

FREQ	S11		S21		S12		S22		STAB	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	K	GMAX
9000.0	.792	78.30	.650	-109.	.033	-56.6	.854	122.8	1.691	8.095
9500.0	.731	63.80	.718	-119.	.036	-72.0	.861	120.2	1.736	8.009
10000.	.674	39.30	.769	-135.	.040	-89.1	.870	117.3	1.624	8.209
10500.	.666	6.200	.916	-154.	.049	-109.	.817	115.6	1.590	8.204
11000.	.590	-31.6	.970	174.6	.059	-139.	.718	95.30	2.413	5.523

(A)

TITLE: RPX-4310 IN CIRCUIT

FREQ	S1		S21		S12		S22		STAB	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	K	GMAX
9000.0	.616	-105.	.852	146.1	.053	147.2	.555	171.7	5.013	2.095
9500.0	.319	158.6	1.296	43.50	.082	59.70	.455	91.10	3.525	3.596
10000.	.132	-121.	1.295	-59.8	.089	-27.5	.295	-3.90	3.919	2.760
10500.	.511	138.2	1.055	-160.	.094	-110.	.340	-128.	3.313	2.391
11000.	.679	43.00	.669	108.5	.109	172.1	.553	149.4	2.590	.908

(B)

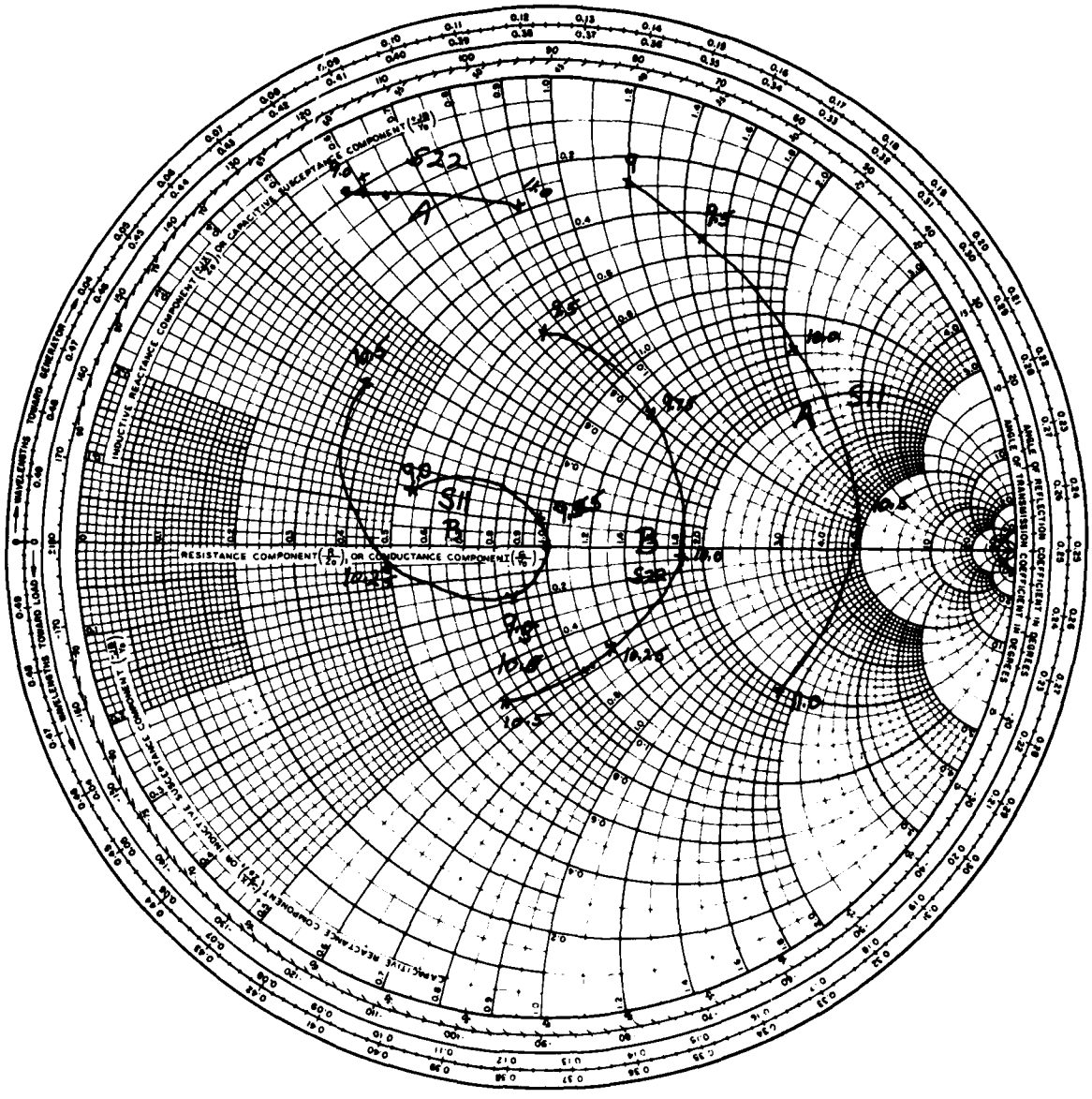

Figure 4. Plot of S-parameters of RPX-4310 device.

C. 1-W FET DEVICE

Due to the difficulty of obtaining wide bandwidth, and the time frame for this task, an alternate approach was investigated. This approach was based on the use of combining techniques and the MSC 88104 FET.

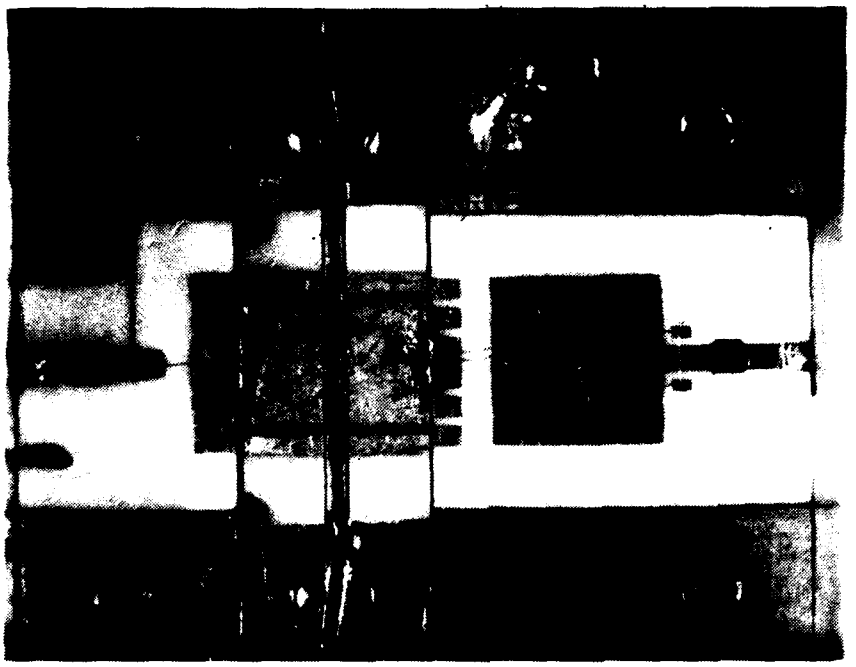

Figure 5. RPX-4310 circuit.

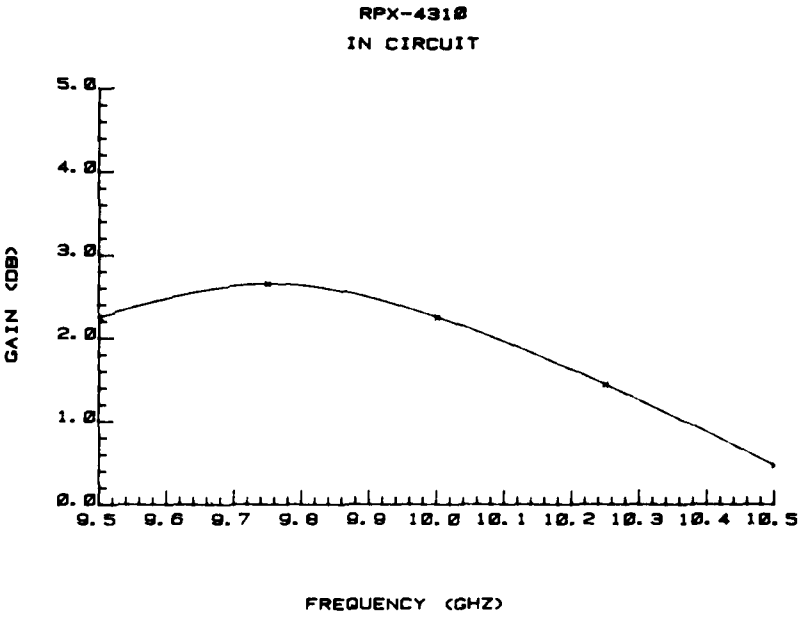

Figure 6. Gain response of RPX-4310 with circuit.

Combining techniques make it possible to obtain the desired bandwidth and power with a smaller FET device and then, by use of a combining circuit,

to increase the power to 1.2 W or greater with a gain of 4 dB or more. Listed below are the manufacturer's specifications of the MSC 88104 device.

Power at 1-dB compression:	1 W
Gain at 1-dB compression:	5 dB
Highest operating frequency specified:	12 dB

The Chip-Pac package device was received for this task.

Table 5 lists S-parameters both before (A) and after partial matching (B). Attention should be directed to the G_{max} and S_{21} terms prior to and after the

TABLE 5. S-PARAMETERS OF 88104 DEVICE. (A) AS RECEIVED. (B) AFTER PARTIAL MATCHING

TITLE: 88104

FREQ	S11		S21		S12		S22		STAB	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	K	GMAX
9000.0	.880	162.1	.836	21.10	.040	3.200	.638	-177.	1.251	9.393
9500.0	.832	159.0	.759	18.00	.046	5.300	.671	-176.	2.014	6.420
10000.	.803	157.0	.718	14.40	.047	6.200	.690	-175.	2.343	5.345
10500.	.759	158.4	.657	12.50	.045	7.600	.694	-173.	3.299	3.553
11000.	.766	157.2	.617	11.90	.043	11.20	.746	-172.	3.014	3.891

(A)

TITLE: 88104-C4 PARTIAL MATCH

FREQ	S11		S21		S12		S22		STAB	
MHZ	MAG	DEG	MAG	DEG	MAG	DEG	MAG	DEG	K	GMAX
9000.0	.588	120.1	1.775	-72.4	.099	-124.	.392	128.9	1.644	7.839
9500.0	.418	81.60	1.993	-97.8	.125	-148.	.338	101.7	1.542	7.686
10000.	.306	7.100	1.958	-131.	.144	-178.	.261	54.80	1.560	6.928
10500.	.427	-58.7	1.661	-161.	.138	156.1	.257	.200	1.715	5.881
11000.	.623	-95.4	1.317	169.4	.125	136.1	.342	-39.6	1.688	5.386

(B)

incorporation of matching networks. The increase in these terms is as it should be when device performance potential is excellent. These initial measurements show that the MSC 88104 series chip has the capability of operating in the desired frequency band. By use of the equation

$$S_{21}\ (dB) = 20\ \log_{10}\ S_{21}$$

the S_{21} term translates to the following values for a small-signal test fixture gain at varying frequencies:

Frequency	Gain (dB)
9.0	4.98
9.5	5.99
10.0	5.84
10.5	4.41
11.0	2.39

Figure 7 is a plot of S_{11} and S_{22} before and after partial matching.

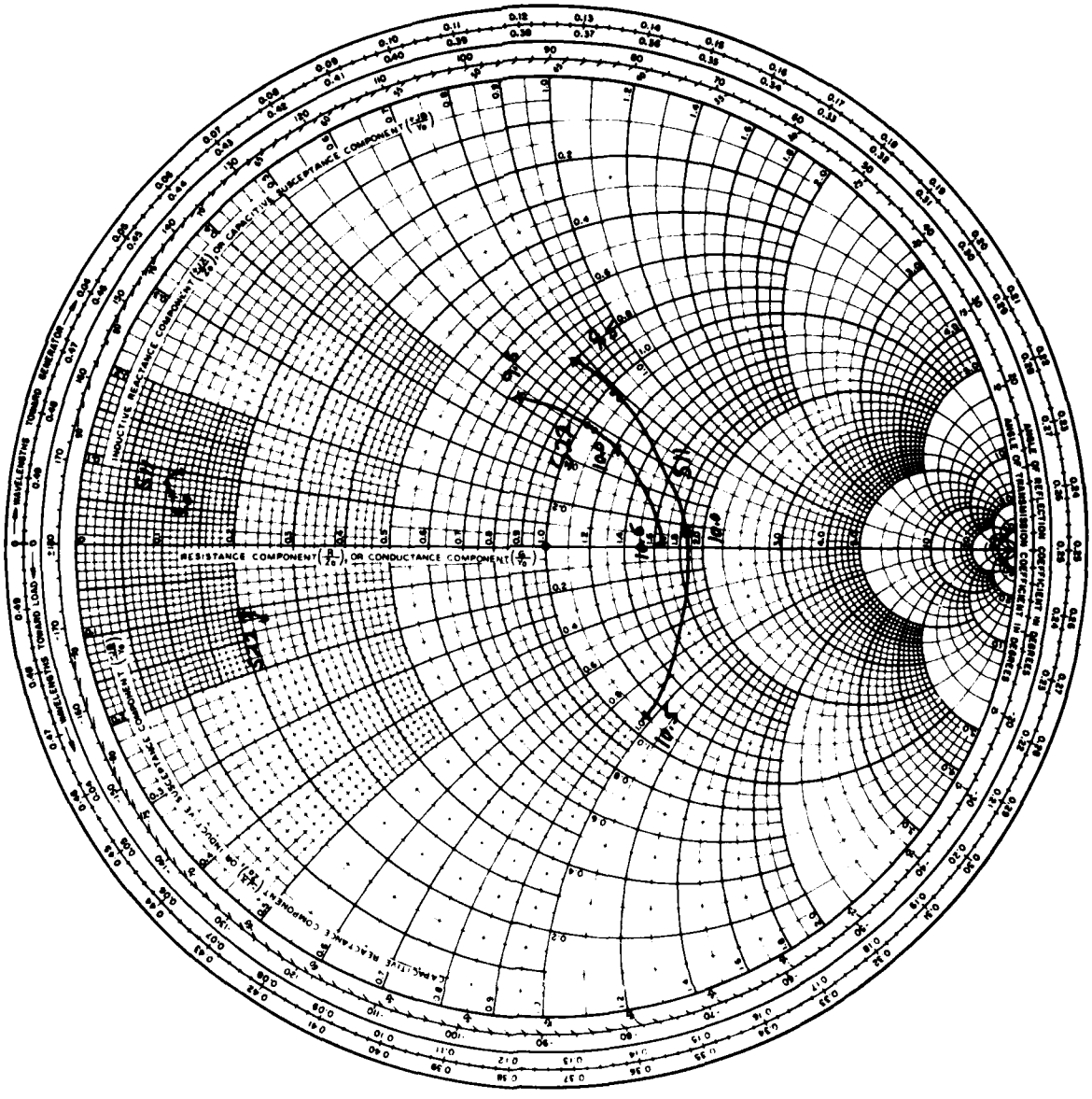

Figure 7. Plot of S-parameters of 88104 device.

SECTION III

CIRCUIT DESIGN

A. INTENT

Following the incoming initial measurement of S-parameters on every FET device, a partial-matching network is constructed and tested. This progression serves two intents: (1) to evaluate the device near operating conditions, and (2) to establish the input and output impedances for the future combining circuit. Figures 8 and 9 depict gain response for the two selected FETs used in module no. 3 under small-signal conditions. The FET selection procedure from this point on is based on drain current (I_{ds}) values, within a predetermined range, with devices of near-I_{ds} values paired.

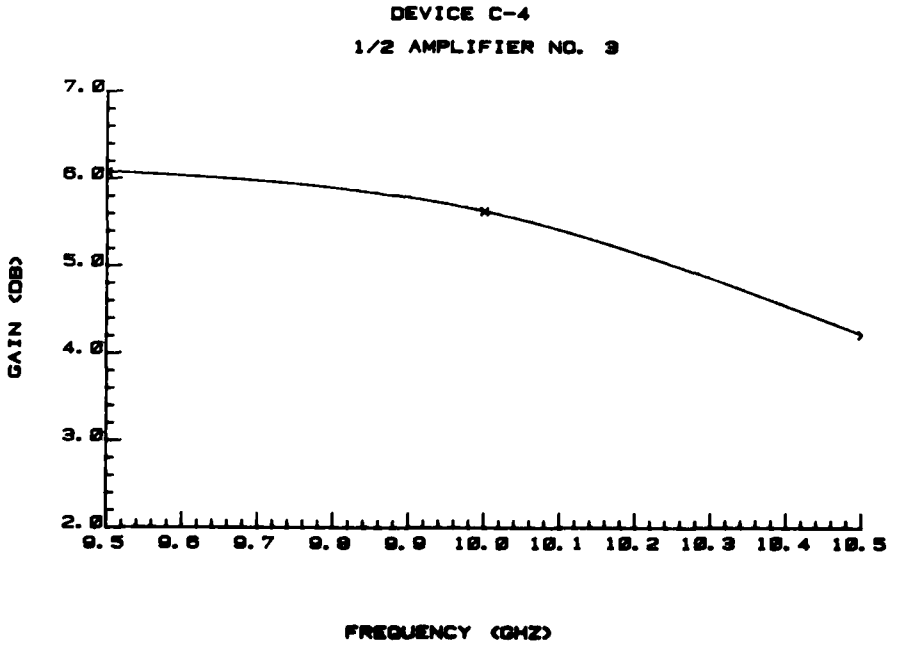

Figure 8. Gain response of selected device (C-4) used in module.

Gold wires, used as inductors, with attendant chip capacitors are the tuning elements. Every component fits on the FET carrier. This integrated matching scheme accounts for the small size of each amplifier module.

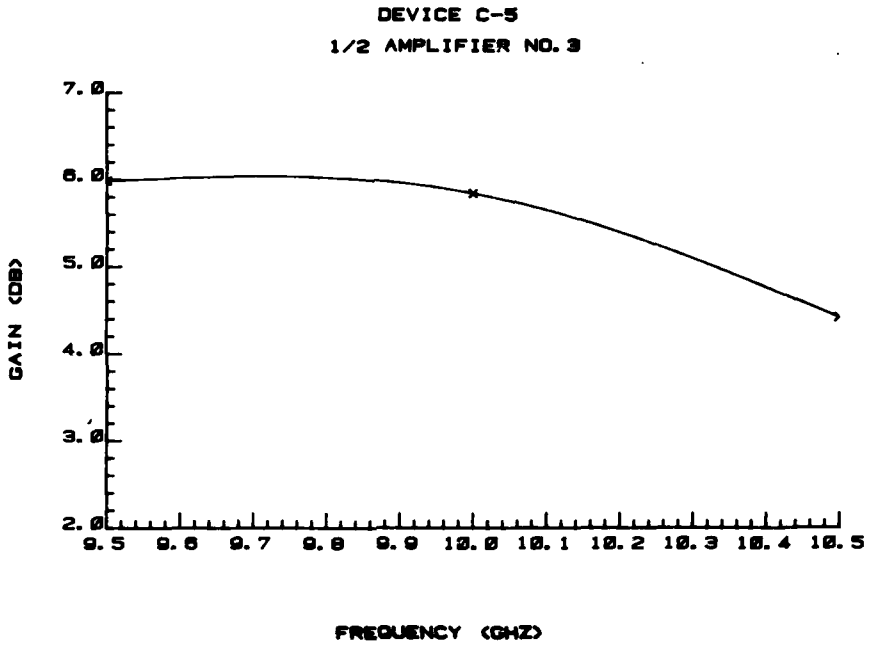

Figure 9. Gain response of selected device (C-5) used in module.

B. CIRCUITS

Optimization of the matching circuit is accomplished by changing the length of the bond wires. Figure 10 schematically shows the circuit that was used.

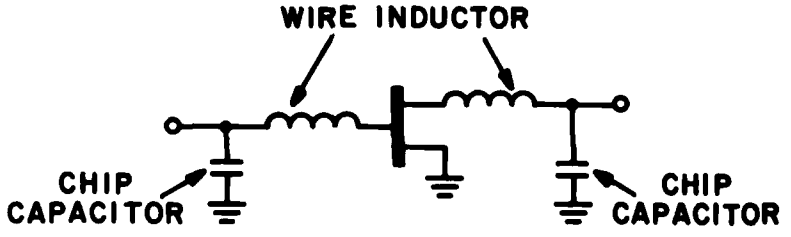

Figure 10. Partial-matching circuit.

Combining circuits are designed and optimized by computer-aided design (CAD) (see Section IV). The basic format of the circuit is shown in Fig. 11.

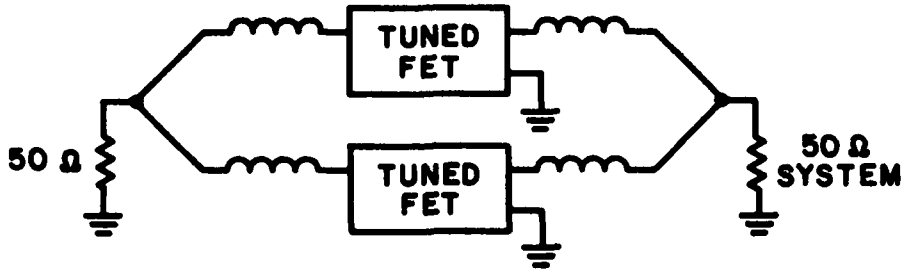

Figure 11. Combining circuit.

C. EXPERIMENTAL RESULTS

1. Power Stages

Figure 12 shows the gain-response curves of a combined FET module. It can be seen that the ideal CAD model and small-signal response, after subtraction of combining loss, follow each other. The 400-mW power-in curve is the module performance under power conditions. Figure 13 gives module performance, at 10 GHz, with increasing power input. Each module is characterized in a similar manner.

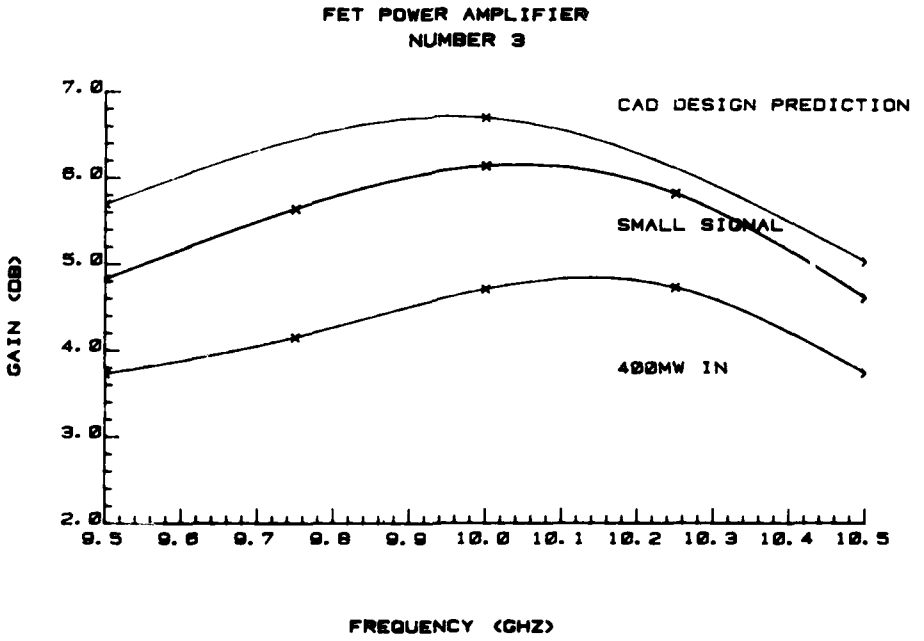

Figure 12. Gain response of combined FET module.

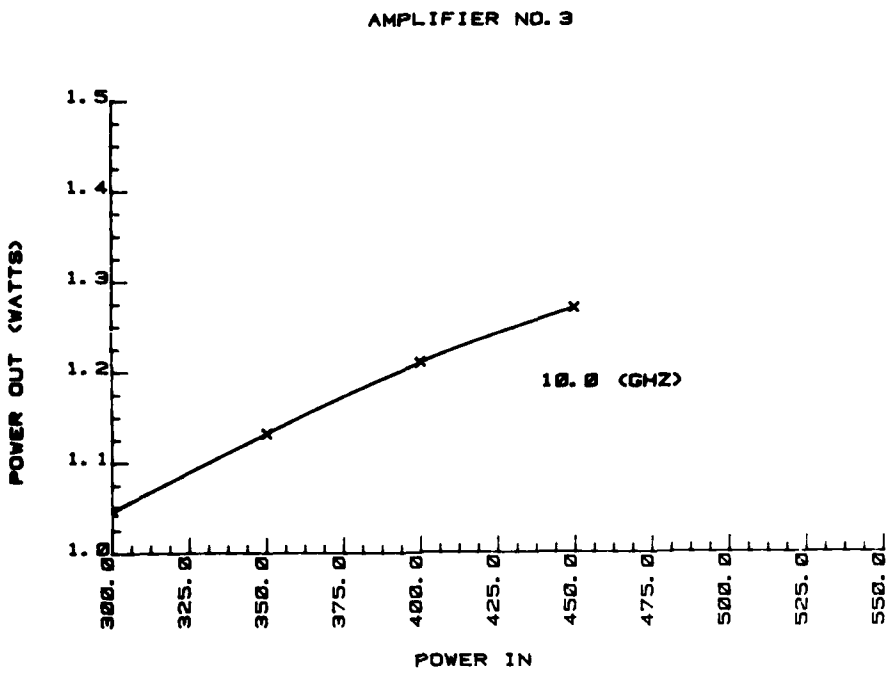

Figure 13. Performance curve of module no. 3.

2. Driver Stages

The MSC 88102 FET, a 0.4-W device, was selected for the two front-end drivers. The manufacturer's specifications are listed below.

Power-out:	0.4 W
Typical gain	6.5 dB
Highest frequency:	12 GHz

Figure 14 shows the gain response of the 88102 device with matching networks. The same fixturing used on the high-power devices is utilized for the device stage(s) except that only one FET is installed.

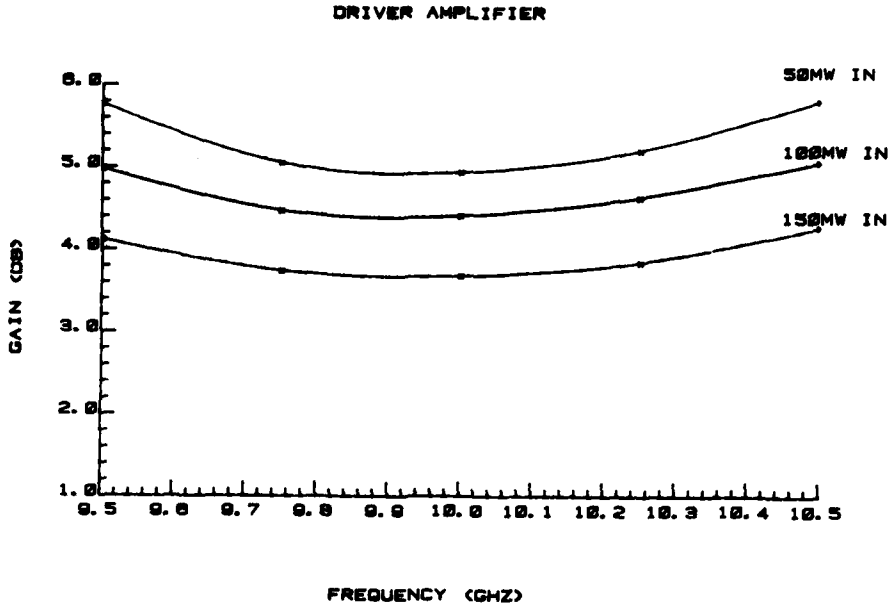

Figure 14. Typical driver-amplifier gain response.

SECTION IV

COMPUTER DESIGN AND OPTIMIZATION

Computer-aided design (CAD) techniques [1] are common tools used to analyze and optimize design problems. CAD simplifies complex networks and explores performance when presented with accurate measurements. The computer system also has the capabilities of optimization and plotting.

To ensure module performance, each module is characterized by CAD before assembly. Figure 15 shows the result of optimization on module no. 3.

A special computer program was written for this project to calculate ribbon and wire length for a desired inductance and wire size.

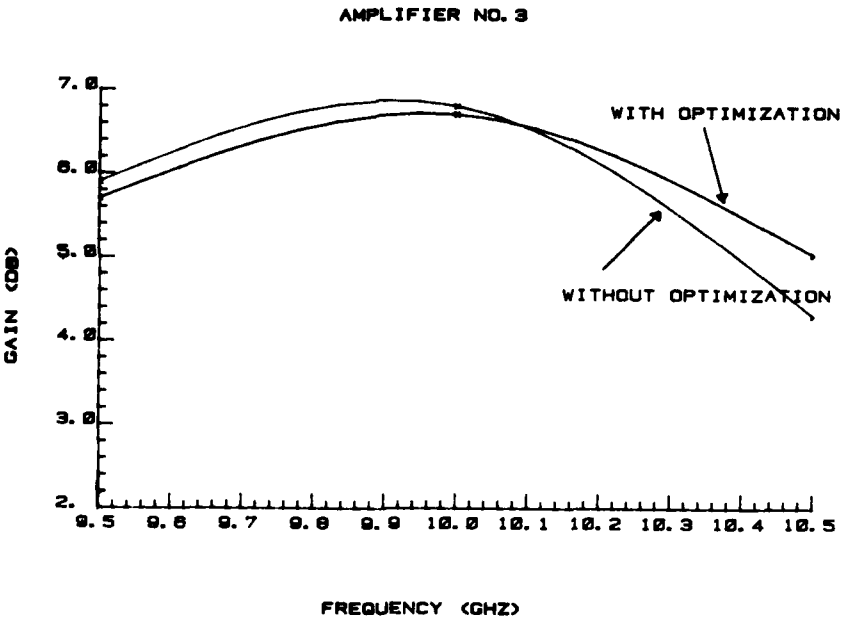

Figure 15. CAD optimization of module no. 3.

1. B. S. Perlman, "Computerized Optimization and Simulation of Microwave Circuits," Technical Report PRRL-75-TR-028, 24 January 1975.

SECTION V

AMPLIFIER LAYOUT AND PERFORMANCE

All nine amplifier modules were fabricated and tested with emphasis on common voltages, for each gate and drain, respectively. Wilkinson-type combiners were constructed with a one-eighth offset giving a quadrature effect. This reduces interstage mismatches when amplifiers are combined, thereby minimizing interaction between stages. Figure 16 shows the full coupler insertion loss vs frequency. Capacitive coupling is used between amplifier modules to reduce low-frequency effects where gain is highest. Bias lines are decoupled throughout, reducing the chance of feedback. Each module carrier is fabricated with sidewalls spaced at waveguide below cutoff, increasing isolation between units.

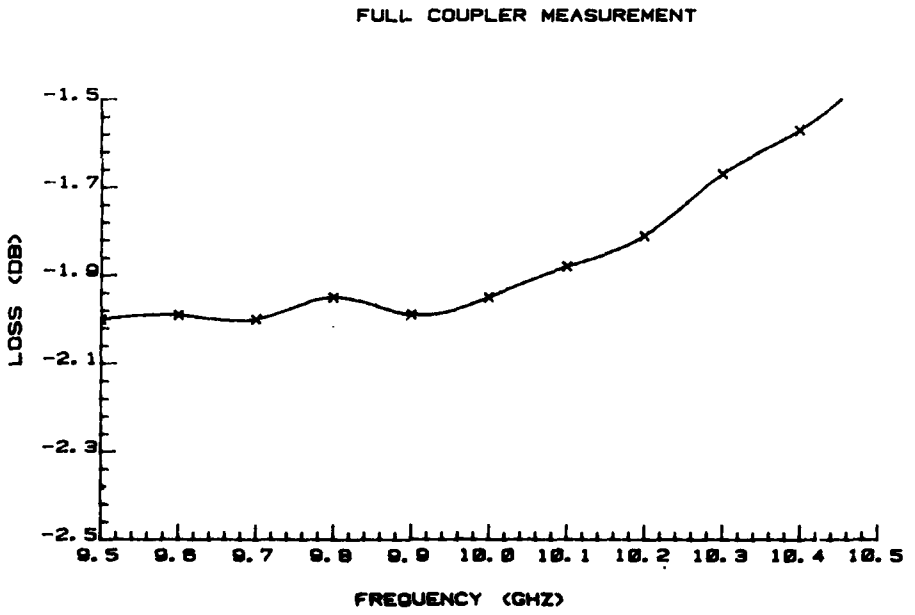

Figure 16. Coupler loss.

In Fig. 17 we show the rf schematic diagram of the assembled power amplifier. Aside from the first two stages, each amplifier module is identical. Coupler loss listed is an approximation since individual couplers were not measured. Figure 18 depicts the mechanical layout and dimensions of the assembled amplifier.

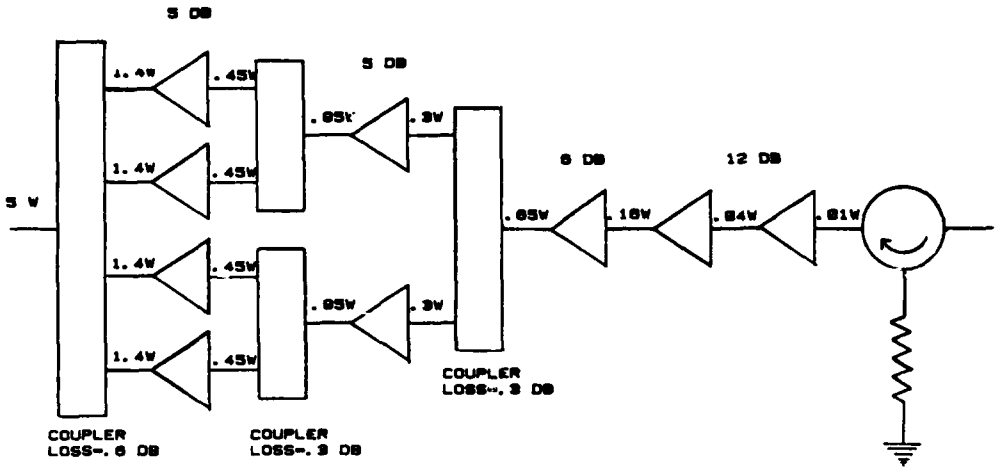

Figure 17. Amplifier rf schematic diagram.

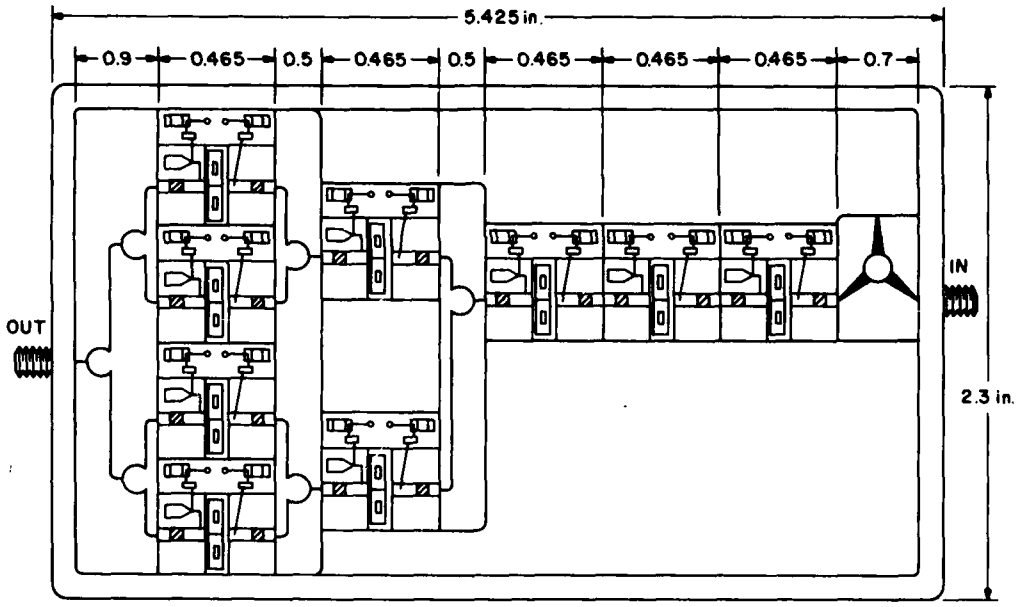

Figure 18. Mechanical layout of assembled amplifier.

A. MEASURED PERFORMANCE

Figure 19 shows the frequency response of the assembled FET power amplifier at the 8-mW power-in level. In Figure 20 we indicate measured efficiency at two input power levels. All measurements were performed at constant-bias voltages. As mentioned above, this was a design goal. The test voltages are

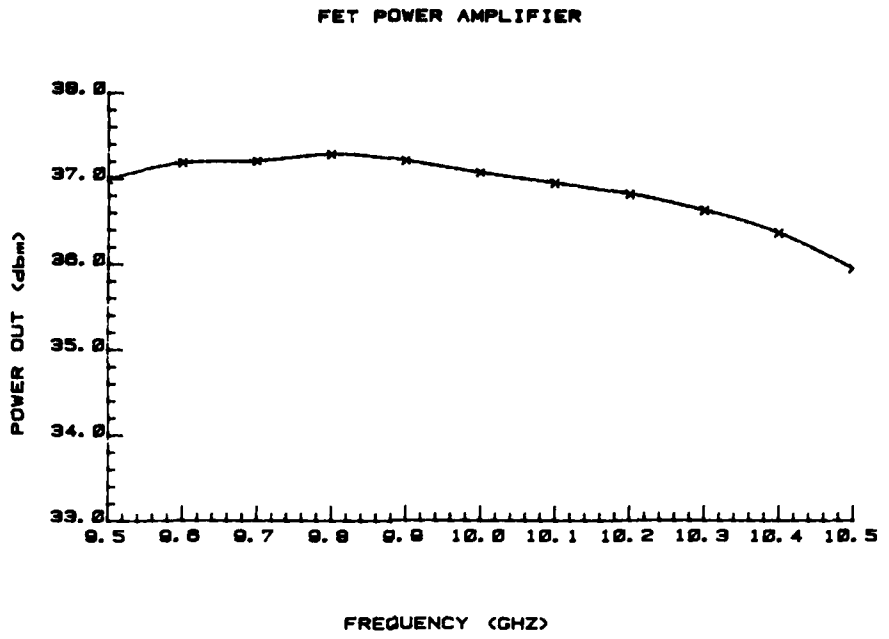

Figure 19. Frequency response of assembled amplifier.

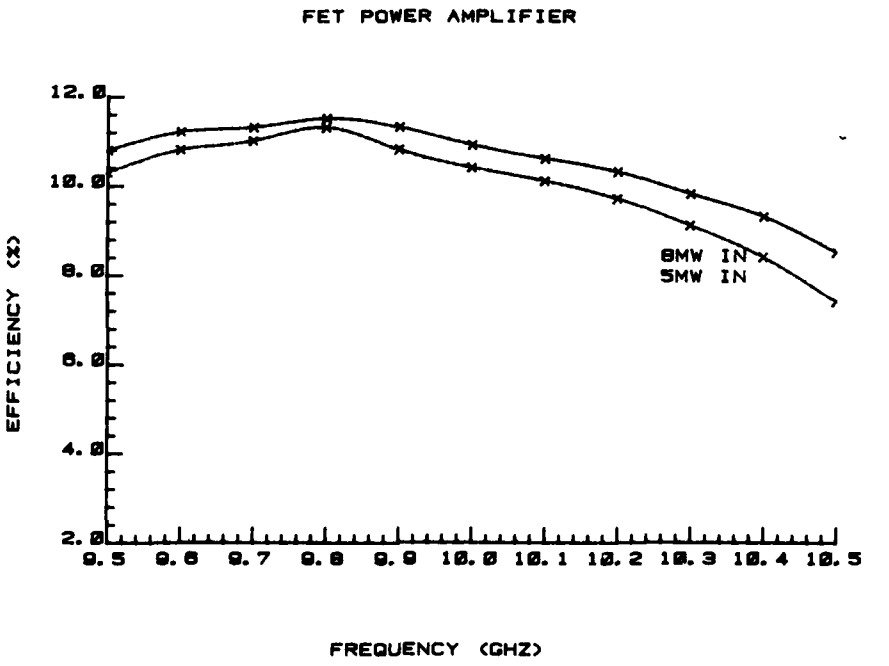

Figure 20. Measured efficiency of assembled amplifier.

-2 V_{gs} and +8 V_{ds}. Drain current hovered around 5.7 A. Figure 21 shows the gain-frequency response with various power-in levels. Figure 22 depicts

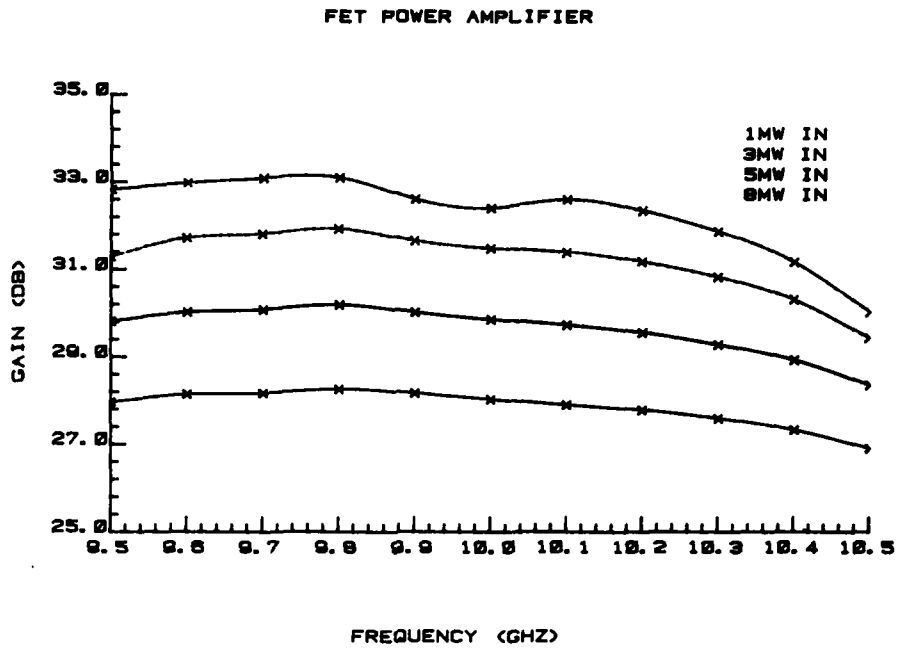

Figure 21. Gain-frequency response of assembled amplifier.

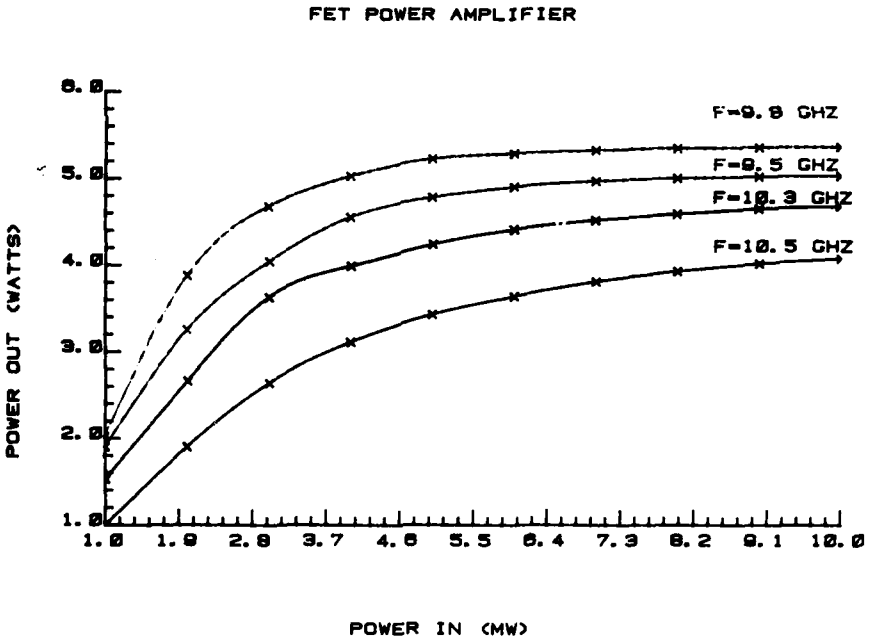

Figure 22. Measured power-out at different frequencies.

measured power performance at different frequencies. Table 6 is a summary of measured data of the assembled FET power amplifier. Noise figure measurements

TABLE 6. SUMMARY OF DATA FOR ASSEMBLED AMPLIFIER

FREQUENCY GHZ	PWR IN (MW)	PWR OUT WATTS	GAIN DB	PWR ADDED EFFICIENCY %	INPUT VSWR
9.5	1.00	1.90	32.82	4.10	1.47
9.5	2.00	3.25	32.11	7.00	1.47
9.5	3.00	4.04	31.29	8.70	1.47
9.5	4.00	4.55	30.57	9.80	1.47
9.5	5.00	4.78	29.81	10.30	1.47
9.5	6.00	4.90	29.12	10.50	1.47
9.5	7.00	4.97	28.51	10.70	1.47
9.5	8.00	5.00	27.96	10.80	1.47
9.5	9.00	5.02	27.47	10.80	1.47
9.5	10.00	5.03	27.01	10.80	1.47
9.6	1.00	1.98	32.97	4.30	1.53
9.6	2.00	3.47	32.72	4.30	1.53
9.6	3.00	4.46	31.72	8.10	1.53
9.6	4.00	4.81	30.80	10.40	1.53
9.6	5.00	5.03	30.02	10.80	1.53
9.6	6.00	5.13	29.33	11.00	1.53
9.6	7.00	5.19	28.70	11.10	1.53
9.6	8.00	5.22	28.14	11.20	1.53
9.6	9.00	5.23	27.64	11.30	1.53
9.6	10.00	5.23	27.19	11.30	1.53
9.7	1.00	2.03	33.08	4.40	1.59
9.7	2.00	3.82	32.82	8.20	1.59
9.7	3.00	4.56	31.81	9.80	1.59
9.7	4.00	4.89	30.87	10.50	1.59
9.7	5.00	5.09	30.08	11.00	1.59
9.7	6.00	5.19	29.37	11.10	1.59
9.7	7.00	5.22	28.73	11.20	1.59
9.7	8.00	5.25	28.17	11.30	1.59
9.7	9.00	5.26	27.67	11.30	1.59
9.7	10.00	5.27	27.22	11.30	1.59
9.8	1.00	2.03	33.09	4.40	1.60
9.8	2.00	3.88	32.88	8.40	1.60
9.8	3.00	4.68	31.93	10.10	1.60
9.8	4.00	5.03	30.99	10.80	1.60
9.8	5.00	5.23	30.19	11.30	1.60
9.8	6.00	5.29	29.45	11.40	1.60
9.8	7.00	5.33	28.82	11.50	1.60
9.8	8.00	5.35	28.26	11.50	1.60
9.8	9.00	5.36	27.75	11.50	1.60
9.8	10.00	5.37	27.30	11.50	1.60
9.9	1.00	1.82	32.60	3.90	1.60
9.9	2.00	3.54	32.48	7.60	1.60
9.9	3.00	4.40	31.66	9.50	1.60
9.9	4.00	4.78	30.77	10.30	1.60
9.9	5.00	5.03	30.02	10.80	1.60
9.9	6.00	5.15	29.34	11.00	1.60
9.9	7.00	5.22	28.72	11.20	1.60
9.9	8.00	5.25	28.17	11.30	1.60
9.9	9.00	5.26	27.67	11.30	1.60
9.9	10.00	5.27	27.22	11.30	1.60

TABLE 6. (Continued)

10.0	1.00	1.73	32.40	3.73	1.60
10.0	2.00	3.35	32.25	7.20	1.60
10.0	3.00	4.22	31.49	9.10	1.60
10.0	4.00	4.59	30.60	9.90	1.60
10.0	5.00	4.84	29.86	10.40	1.60
10.0	6.00	4.99	29.20	10.70	1.60
10.0	7.00	5.05	28.58	10.80	1.60
10.0	8.00	5.08	28.03	10.90	1.60
10.0	9.00	5.10	27.54	11.00	1.60
10.0	10.00	5.12	27.10	11.00	1.60
10.1	1.00	1.81	32.59	3.90	1.60
10.1	2.00	3.42	32.34	7.40	1.60
10.1	3.00	4.13	31.39	8.90	1.60
10.1	4.00	4.48	30.49	9.60	1.60
10.1	5.00	4.70	29.73	10.10	1.60
10.1	6.00	4.84	29.07	10.40	1.60
10.1	7.00	4.90	28.45	10.50	1.60
10.1	8.00	4.94	27.90	10.60	1.60
10.1	9.00	4.59	27.41	10.70	1.60
10.1	10.00	4.98	26.97	10.70	1.60
10.2	1.00	1.70	32.33	3.70	1.60
10.2	2.00	3.19	32.03	6.90	1.60
10.2	3.00	3.93	31.17	8.50	1.60
10.2	4.00	4.27	30.28	9.20	1.60
10.2	5.00	4.50	2.55	9.70	1.60
10.2	6.00	4.66	28.91	10.00	1.60
10.2	7.00	4.76	0.00	10.20	1.60
10.2	8.00	4.80	27.78	10.30	1.60
10.2	9.00	4.84	27.30	10.40	1.60
10.2	10.00	4.86	26.86	10.50	1.60
10.3	1.00	1.53	31.86	3.30	1.56
10.3	2.00	2.66	31.22	5.70	1.56
10.3	3.00	3.63	30.83	7.80	1.56
10.3	4.00	3.99	30.00	8.60	1.56
10.3	5.00	4.24	29.28	9.10	1.56
10.3	6.00	4.41	28.66	9.50	1.56
10.3	7.00	4.52	28.10	9.70	1.56
10.3	0.00	0.00	0.00	0.00	0.00
10.3	9.00	4.65	27.13	10.00	1.56
10.3	9.00	4.65	27.13	10.00	1.56
10.3	10.00	4.68	26.71	10.10	1.56
10.4	1.00	1.30	31.16	2.80	1.50
10.4	2.00	2.44	30.86	5.30	1.50
10.4	3.00	3.22	30.31	6.90	1.50
10.4	4.00	3.64	29.59	7.80	1.50
10.4	5.00	3.91	28.93	8.40	1.50
10.4	6.00	4.09	28.34	8.80	1.50
10.4	7.00	4.24	27.82	9.10	1.50
10.4	8.00	4.33	27.33	9.30	1.50
10.4	9.00	4.40	26.89	9.50	1.50
10.4	10.00	4.44	26.48	9.60	1.50
10.5	1.00	1.00	30.02	2.20	1.40
10.5	2.00	1.90	29.79	4.10	1.40
10.5	3.00	2.64	29.44	5.70	1.40
10.5	4.00	3.11	28.91	6.70	1.40
10.5	5.00	3.43	28.36	7.40	1.40
10.5	6.00	3.64	27.83	7.80	1.40
10.5	7.00	3.81	27.36	8.20	1.40
10.5	8.00	3.93	26.91	8.50	1.40
10.5	9.00	4.02	26.50	8.60	1.40
10.5	10.00	4.08	26.11	8.80	1.40
0.0	0.00	0.00	0.00	0.00	0.00

were performed with an AIL* Automatic Noise Figure Indicator. Table 7 lists these measurements at selected frequencies.

TABLE 7. NOISE FIGURE (NF) MEASUREMENTS

Frequency (GHz)	NF
9.5	12.1
9.75	12.0
10.0	12.4
10.25	12.95
10.5	13.4

B. AMPLIFIER GEOMETRY

Figure 23 shows the amplifier as completed. All bias lines are dressed through the housing to the underside; there they are joined together. Power is applied through two feed-through filter connections. Provision for water cooling is included and is recommended to extend the life of the model.

*Airborne Instrument Laboratories, a division of Cutter-Hammer, Farmingdale, Long Island, NY.

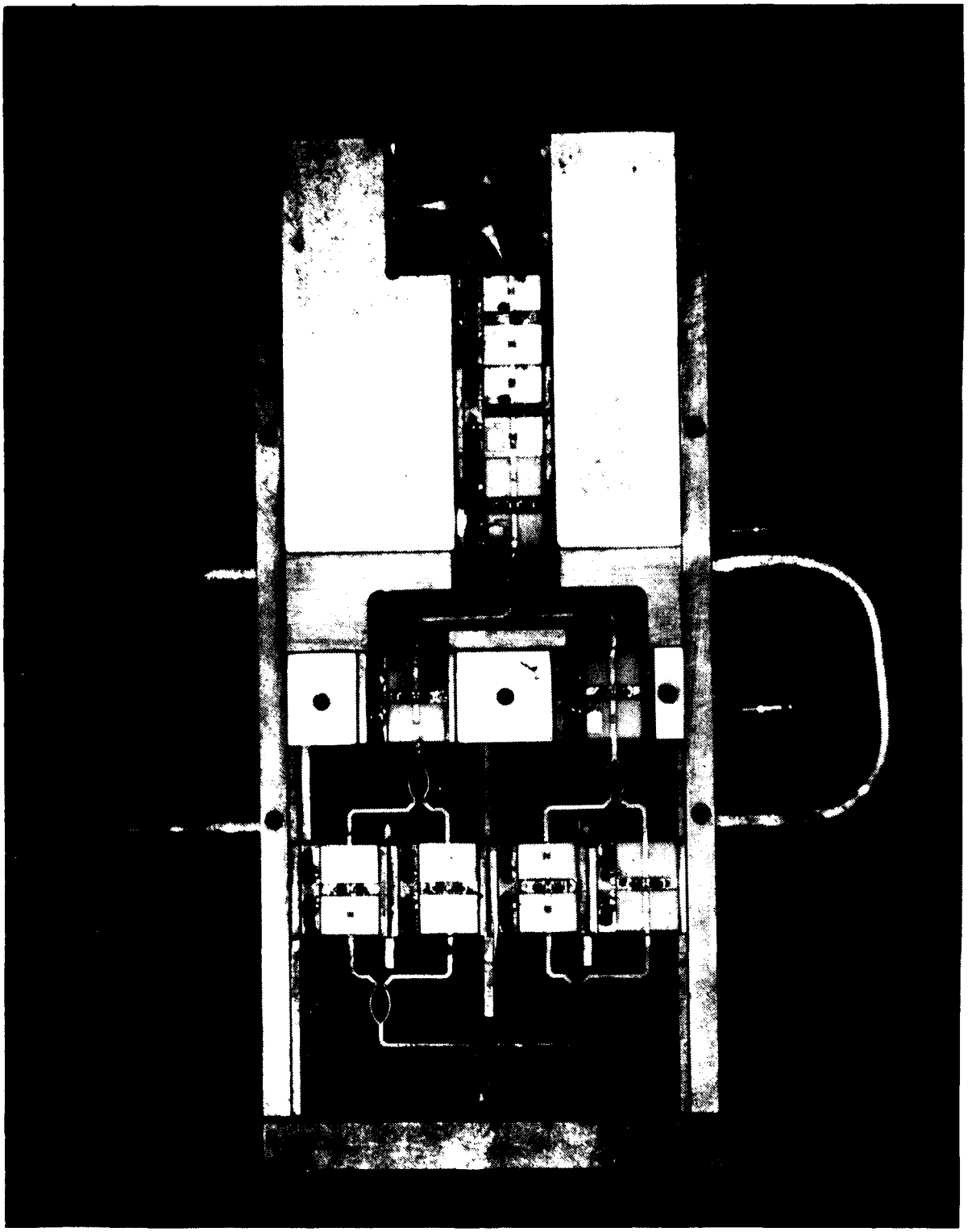

Figure 23. Assembled amplifier.

SECTION VI

CONCLUSIONS

This report summarizes the results achieved in a 12-month program to develop an FET power amplifier applicable to a quiet radar.

During the course of this program three power FET devices were investigated for possible inclusion in the final model.

Combining techniques were improved for pairing FET chips so that these would yield greater power and bandwidth. Seven FET power amplifier modules were developed and fabricated, each delivering 1.2 W or greater power-out. Two front-end 0.5-W power amplifier modules were also fabricated and used as drivers. The fact that all amplifiers operate at the same bias voltages simplifies subsequent cascading to form larger units.

An FET 5-W power amplifier, along with test data, has been delivered to MICOM.

During this program we have accomplished the following:

- o Improved FET combining techniques.
- o Improved module fabrication techniques.
- o Integrated power modules for high-power operation.

In conclusion, we have demonstrated the feasibility of using low-power devices in combination to yield high-power modular amplifier units. We have shown that power modules can be cascaded with relative ease to form high-power amplifier assemblies.