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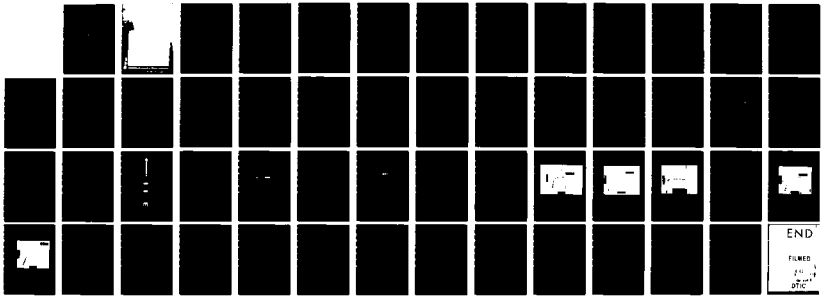

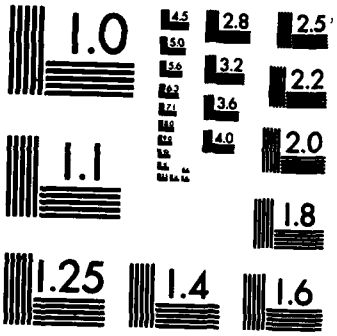

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An alternative field effect transistor (FET) structure to the junction FET (JFET) and the metal-semiconductor FET (MESFET), the camel gate FET (CAMFET), is described. This device uses the voltage-variable depletion width of a camel diode for modulating the channel current. By varying the structural parameters of the CAMFET, a wide variety of FET characteristics may be obtained. CAMFETs can be designed to yield relatively voltage independent transconductances, large forward turn-on voltages, and large gate-drain breakdown voltages, all of which are

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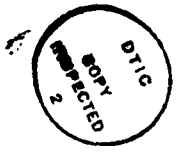
desirable in large signal applications. CAMFETs with large transconductances, desirable in logic applications, may also be obtained. Together with ease of fabrication and potentially improved reliabilities and yields, the many advantages of CAMFETs appear to point to a promising future in both discrete and large scale integrated circuit applications.

CAMEL GATE FIELD EFFECT TRANSISTORS

BY

ROBERT EDWARD THORNE



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CAMEL GATE FIELD EFFECT TRANSISTORS

BY

ROBERT EDWARD THORNE

B.Sc. E.E., University of Manitoba, 1981

THESIS

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I. INTRODUCTION

Gallium arsenide field effect transistors (GaAs FETs) have been the subject of an intense research effort over the past decade. Between 1973 and 1979, over 350 papers were published on these devices [1]. The reason for this interest is that they are well suited to a variety of high-frequency and high-speed logic applications. FETs have very high input impedances, making it easy to match them to standard microwave systems [2]. Since their characteristics obey a square law, intermodulation and cross-modulation products are smaller than, for example, bipolar transistors. FETs are majority carrier devices, and thus do not suffer from minority carrier storage effects which degrade high-frequency performance. GaAs FETs are outstanding low noise devices [3]. Further, GaAs FETs have been demonstrated which provide gain between 2 and 40 GHz [1], and with RF power outputs in excess of 20 W. All of these features make them excellent candidates for application in low noise amplifiers and receivers for communication and radar applications [4]. In addition, GaAs FET logic gates with switching times of 19.6 ps at 300 k have been reported [5], so these devices are clearly promising for logic applications as well.

The two principal types of GaAs FETs are the junction FET (JFET) [6] and the metal-semiconductor FET (MESFET) [7]. (GaAs MOSFETs are not feasible because the nature of the surface states on GaAs does not permit modulation of the channel current.) Figure 1 gives a schematic diagram of a JFET. The JFET consists of an n-type conducting channel with two ohmic metal contacts, known as the source and drain, at either end. When a positive voltage is applied to the drain, electrons flow from the source to drain. A p layer is formed on

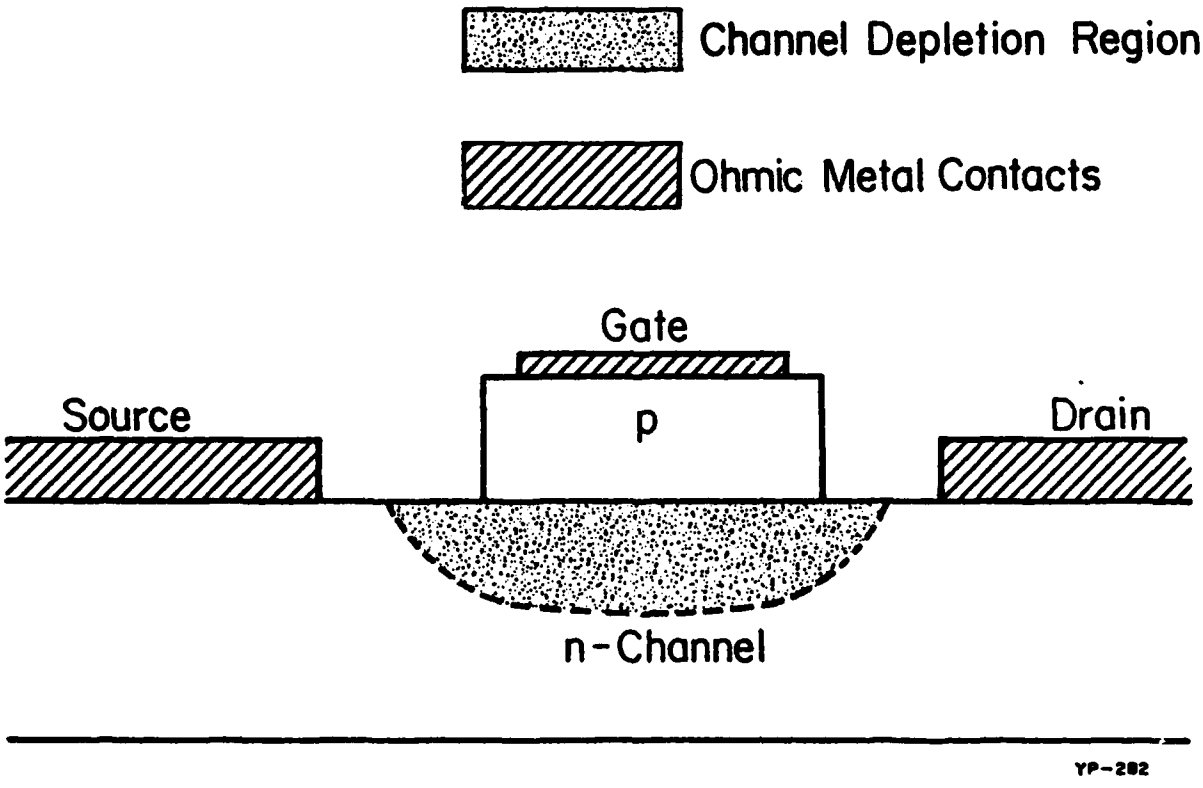

Figure 1: Schematic diagram of a junction field effect transistor (JFET).

top of the n channel, resulting in a rectifying p-n contact known as the gate. When a voltage is applied between the gate and source, the depletion depth of the p-n junction into the channel layer changes, thereby changing the conducting cross-section of the channel and thus the current. The MESFET is virtually identical in concept to the JFET, the principal difference being that a rectifying metal-semiconductor contact (Schottky barrier) is used in place of the p-n junction to provide channel modulation. In both devices, a voltage at the gate controls the current in the channel; the FET is basically a voltage controlled resistor.

Of these two types of GaAs FETs, the MESFET has attracted the greatest attention. The principal reason for this is that the MESFET is relatively easy to fabricate; in particular, the submicron dimensions required for high frequency operation are readily obtained. MESFETs, however, are beset with several problems. First, the metal-semiconductor contact presents significant metallurgical difficulties. This contact tends to be unstable, particularly when the operating temperature of the device is high due to either adverse environments or high power dissipation [8]. Second, the barrier height to current conduction through the gate is difficult to adjust, and is typically only about 0.7 V. In linear applications, this small barrier height constrains the input signal amplitude and thus the FET output power, while in logic applications it restricts the noise margin.

The JFET has several advantages relative to the MESFET. The p-n gate contact is much more temperature stable than the Schottky contact, allowing larger power handling capability and better reliability. Much larger built-in voltages may be obtained, allowing larger gate voltages to be applied without gate conduction, and thus larger input signals and noise margins. In addition, JFETs can have a variety of gate configurations such as heterojunction

or buffered layer gates which improve high frequency performance [2]. Unfortunately, JFETs are difficult to fabricate with submicron dimensions [9]. They also require a metal contact be made to p-type semiconductor, which results in large gate resistances and thus degraded microwave performance.

In this thesis, an alternative device structure to ' MESFET and JFET, the camel gate FET, or CAMFET [10]-[12], is describec The camel gate FET allows all the advantages of JFETs and MESFETs to be o d in a single device. In the following, the basic device concept, theory, and experimental performance of the CAMFET will be presented.

II. BASIC DEVICE CONCEPT

The fundamental difference between the camel gate FET and the MESFET or JFET is that, instead of a rectifying metal-semiconductor contact or a p-n junction, the gate is formed using very thin n^+ and p^+ layers. The n^+ and p^+ layers, together with the n-type channel layer, form a camel diode. Before proceeding to a discussion of the CAMFET, the important features of the camel diode will be reviewed.

A. The Camel Diode

The camel diode was first proposed by Shannon in 1979 [13]. A similar device, the planar doped barrier, was demonstrated independently in 1980 by Malik et al. [14]. The basic structure of the camel diode consists of n^+ and n layers, with a very thin (typically 100 Å) p^+ layer in between. The parameters of the structure are chosen so that the p^+ layer is fully depleted. Figure 2 gives the conduction band-edge energy diagram of a camel diode under equilibrium and reverse biased conditions. Charge transport in these devices is primarily via thermionic emission of electrons from the n layer, over the barrier or "hump" in the p^+ layer and into the n^+ layer. (The hump in the conduction band provided the inspiration for the name "camel" diode.) As the bias on the diode is varied, the depletion depths in the n and n^+ layers vary.

The most important feature of the camel diode is that, as with the Schottky diode, it is a majority carrier device. It differs from the Schottky diode, however, in that the active junction is located away from the surface, eliminating the importance of interface states. Further, the barrier height of the camel diode may be easily adjusted by varying the dopings and thicknesses of the structure.

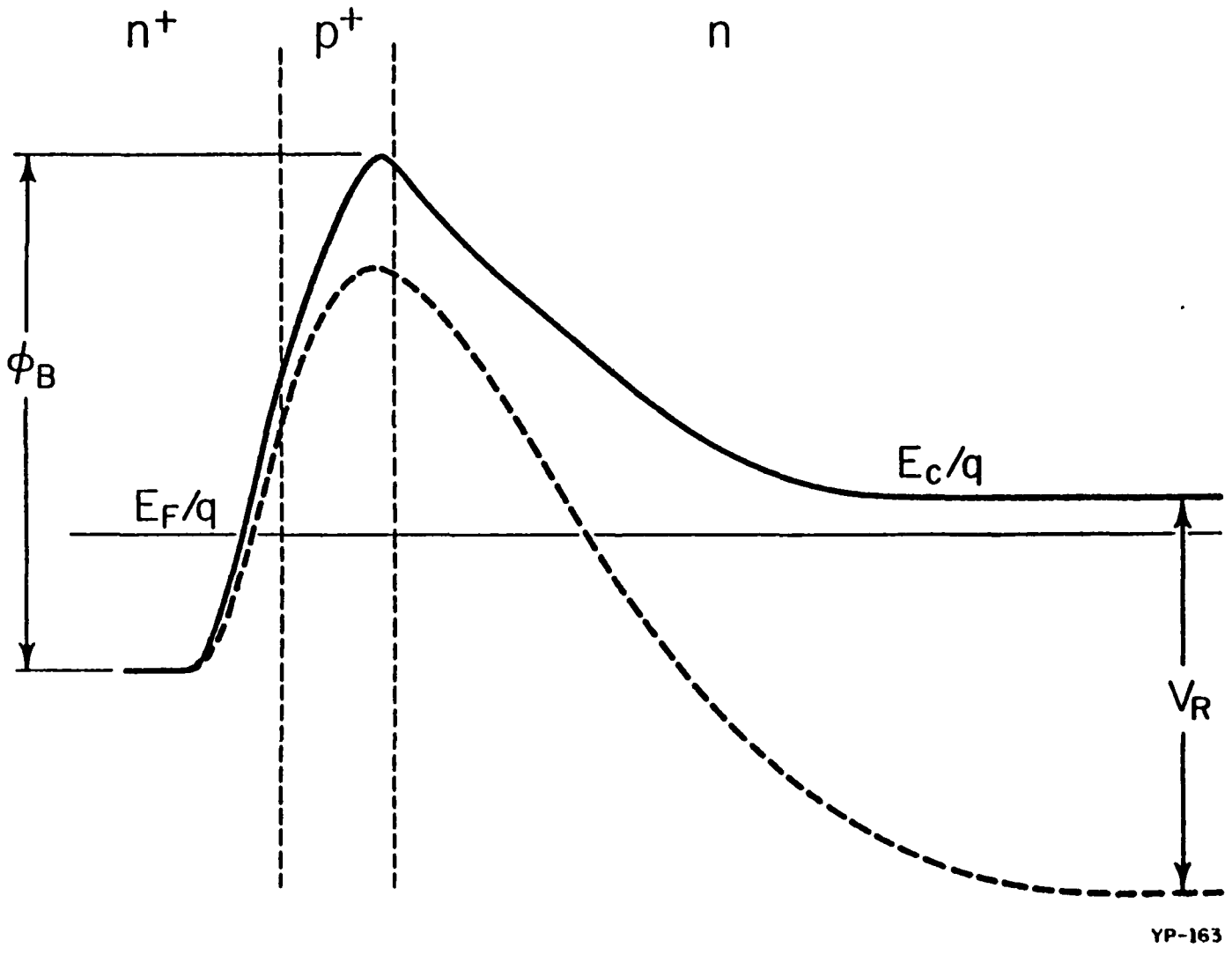

Figure 2: Conduction band-edge energy diagram of camel diode under equilibrium (solid line) and reverse bias (dashed line) conditions.

B. The Camel Gate FET

The purpose of the gate in the JFET and MESFET is to provide depletion of the FET channel which varies with the applied signal voltage. Because the depletion of the n layer of the camel diode is also a function of the applied voltage, this suggests the possibility of replacing the n layer of the diode with the channel layer of an FET. The resulting device structure, the camel gate FET, or CAMFET, is illustrated in Figure 3.

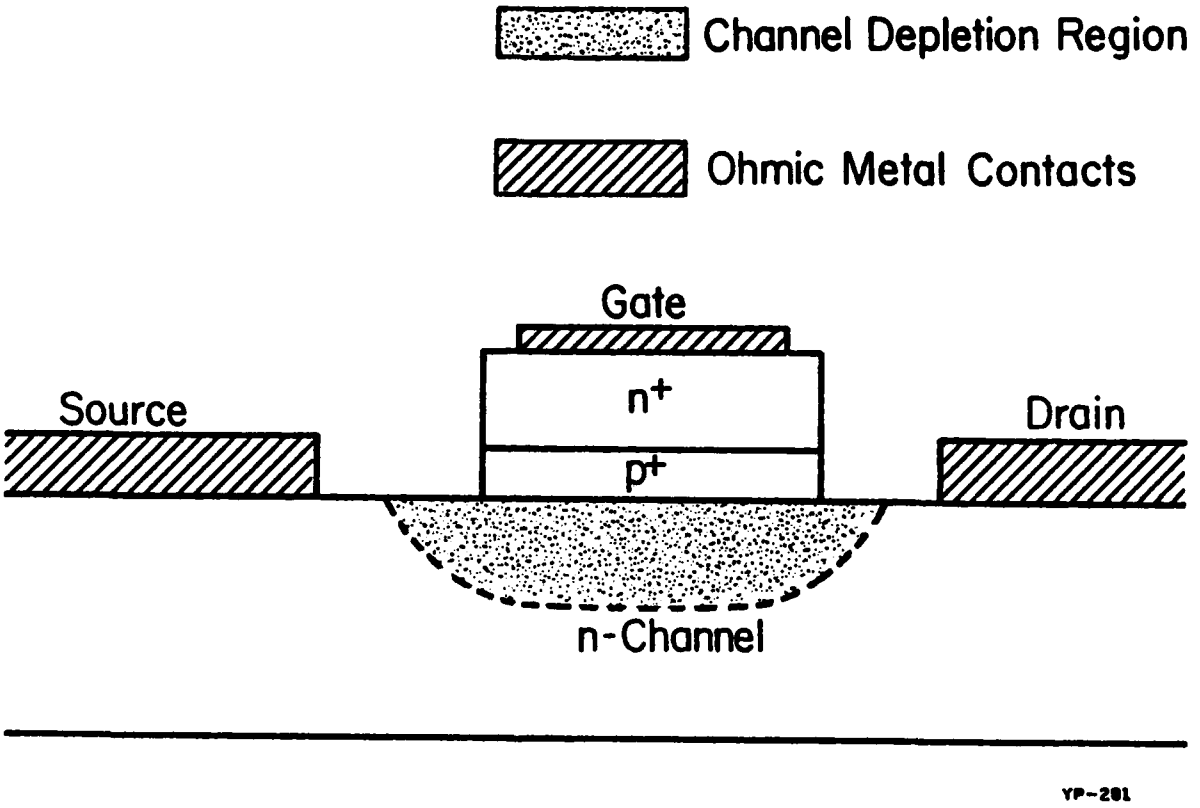

Figure 3: Schematic diagram of a camel gate field effect transistor (CAMFET).

III. THEORETICAL ANALYSIS

In order to better understand how a CAMFET works, a theoretical analysis is useful. Figure 4 shows the conduction band-edge energy diagram of a homojunction camel gate under equilibrium conditions.

Using the depletion approximation and Poisson's equation, the equations describing the CAMFET can be derived. The equations which follow describe the general case of a heterojunction CAMFET, i.e., where the p^+ layer semiconductor is different from that of the channel and n^+ layers. The meanings of the symbols used in these equations are given in Table 1.

The channel depletion depth W satisfies

$$\alpha W^2 + \beta W + \gamma = 0 \tag{1}$$

where

$$\alpha = \frac{q}{2\varepsilon_1} N_d \left(1 - \frac{N_d}{N_d^+} \right) \tag{2}$$

$$\beta = \frac{qN_d t}{\varepsilon_2} \left(1 + \frac{\varepsilon_2}{\varepsilon_1} \frac{N_d}{N_d^+} \right) \tag{3}$$

$$\gamma = V_{n2} + V_{n1} + V_a - \frac{qN_a t^2}{2\varepsilon_2} \left(1 + \frac{\varepsilon_2}{\varepsilon_1} \frac{N_a}{N_d^+} \right) \tag{4}$$

From conservation of charge, the n^+ depletion depth d is given by

$$d = t \frac{N_a}{N_d^+} - W \frac{N_d}{N_d^+} \tag{5}$$

The barrier height to current conduction Φ_B is

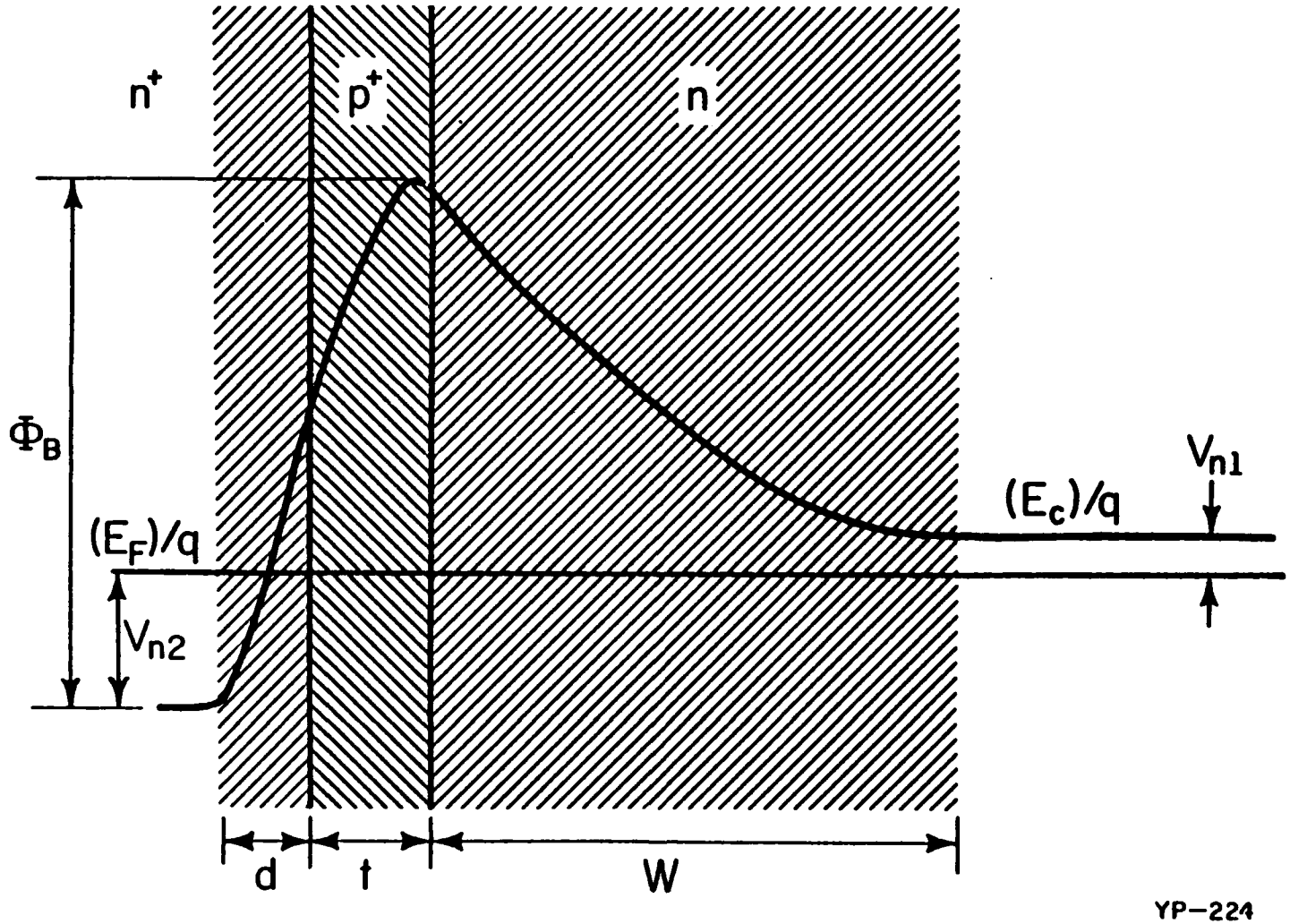

Figure 4: Conduction band-edge energy diagram of a homojunction camel gate in equilibrium. The shading denotes depleted regions

Table 1: LIST OF SYMBOLS

Symbol	Description
N_d	channel layer doping level
N_d^+	n^+ layer doping level
N_a	p^+ layer doping level
V_{n1}	Fermi potential in channel layer relative to the conduction band edge
V_{n2}	Fermi potential in the n^+ layer relative to the conduction band edge
V_a	applied bias (n^+ positive relative to the channel)
ΔE_c	conduction band-edge energy discontinuity at the n^+-p^+ and p^+- channel layer interfaces
ε_1	dielectric constant of the n^+ and channel layers
ε_2	dielectric constant of the p^+ layer
v_s	electron saturation velocity
t	thickness of the p^+ layer
W	channel layer depletion width
d	n^+ layer depletion width
A	effective gate area
Z	effective gate length
q	electronic charge

$$\Phi_B = \frac{qN_a}{2\varepsilon_2}\left(t - \frac{WN_d}{N_a}\right)^2 + \frac{qN_d^+}{2\varepsilon_1}\left[\frac{N_a}{N_d^+}\left(t - \frac{WN_d}{N_a}\right)\right]^2 + \frac{\Delta E_c}{q} \qquad (6)$$

From (1) and (6), an alternative expression for W, similar in form to that for the depletion of a Schottky barrier, is

$$W = \sqrt{\frac{2\varepsilon_1}{qN_d}\frac{\Phi_B - V_{n1} - V_{n2} - \Delta E_c/q - V_a}{1 + \frac{\varepsilon_1}{\varepsilon_2}\frac{N_d}{N_a}}} \qquad (7)$$

The gate depletion capacitance is given by

$$C_{gs} = \frac{A}{\frac{t}{\varepsilon_2}\left(1 + \frac{\varepsilon_2}{\varepsilon_1}\frac{N_a}{N_d^+}\right) + \frac{W}{\varepsilon_1}\left(1 - \frac{N_d}{N_d^+}\right)} \qquad (8)$$

Finally, for a short channel FET operating in the velocity saturation limit, the intrinsic transconductance is obtained from

$$g_m = \frac{v_s Z}{\frac{t}{\varepsilon_2}\left(1 + \frac{\varepsilon_2}{\varepsilon_1}\frac{N_a}{N_d^+}\right) + \frac{W}{\varepsilon_1}\left(1 - \frac{N_d}{N_d^+}\right)} \qquad (9)$$

To gain some insight as to what these equations mean, in the following a series of plots calculated using these equations is presented. The values of the FET parameters used in the calculations were $N_d^+ = 7 \times 10^{18}$ cm^{-3}, $N_d = 2 \times 10^{17}$ cm^{-3}, and $t = 100$ Å, which are typical of actual devices. Since the doping-thickness product of the p^+ layer is most important in determining the CAMFET's performance, the calculations were made using three different values of the p^+ layer doping : $N_a = 4 \times 10^{18}$, 7×10^{18}, and 1×10^{19} cm^{-3}.

The n^+, p^+ and channel layers were all assumed to be of GaAs.

Figure 5 shows the barrier height Φ_B as a function of gate reverse bias (i.e., gate potential negative with respect to the source). The barrier height is very sensitive to the p^+ layer doping level, varying from a zero bias value of 1.2 V for $N_a = 1 \times 10^{19}$ cm^{-3} down to 0.3 V for $N_a = 4 \times 10^{18}$ cm^{-3}. The barrier height may be increased by increasing the thickness and doping of the p^+ layer and decreasing the dopings of the n^+ and channel layers. In theory, the maximum barrier height possible is the semiconductor bandgap, the limit arising due to tunneling of electrons from the valence band in the p^+ layer to the conduction band of the n^+ layer. (This tunneling raises the electrostatic potential of the p^+ layer until $\Phi_B \approx E_g$.) A larger bandgap material such as (Al,Ga)As may be used to enhance the barrier height to current conduction. However, the potential depleting the channel depends only on the doping, thickness, and dielectric constant of the p^+ layer and not on its bandgap. Consequently, since the dielectric constants of GaAs and (Al,Ga)As are comparable, using an (Al,Ga)As p^+ layer has little effect on the channel depletion.

An important feature of the barrier height of the CAMFET is that it has a much stronger dependence on gate voltage than does that of a Schottky barrier. Indeed, if the p^+ layer is lightly doped, the barrier height may be reduced to near zero by the application of a relatively small reverse bias, leading to heavy gate conduction. By choosing the structural parameters properly, however, substantial barrier heights may be maintained for reverse gate biases in excess of 30 V. The variation in barrier height is a consequence of the fact that, unlike a p-n junction or Schottky barrier, the total charge in the depletion region is constant. Thus, application of a reverse bias can only rearrange this charge, and this rearrangement necessarily reduces

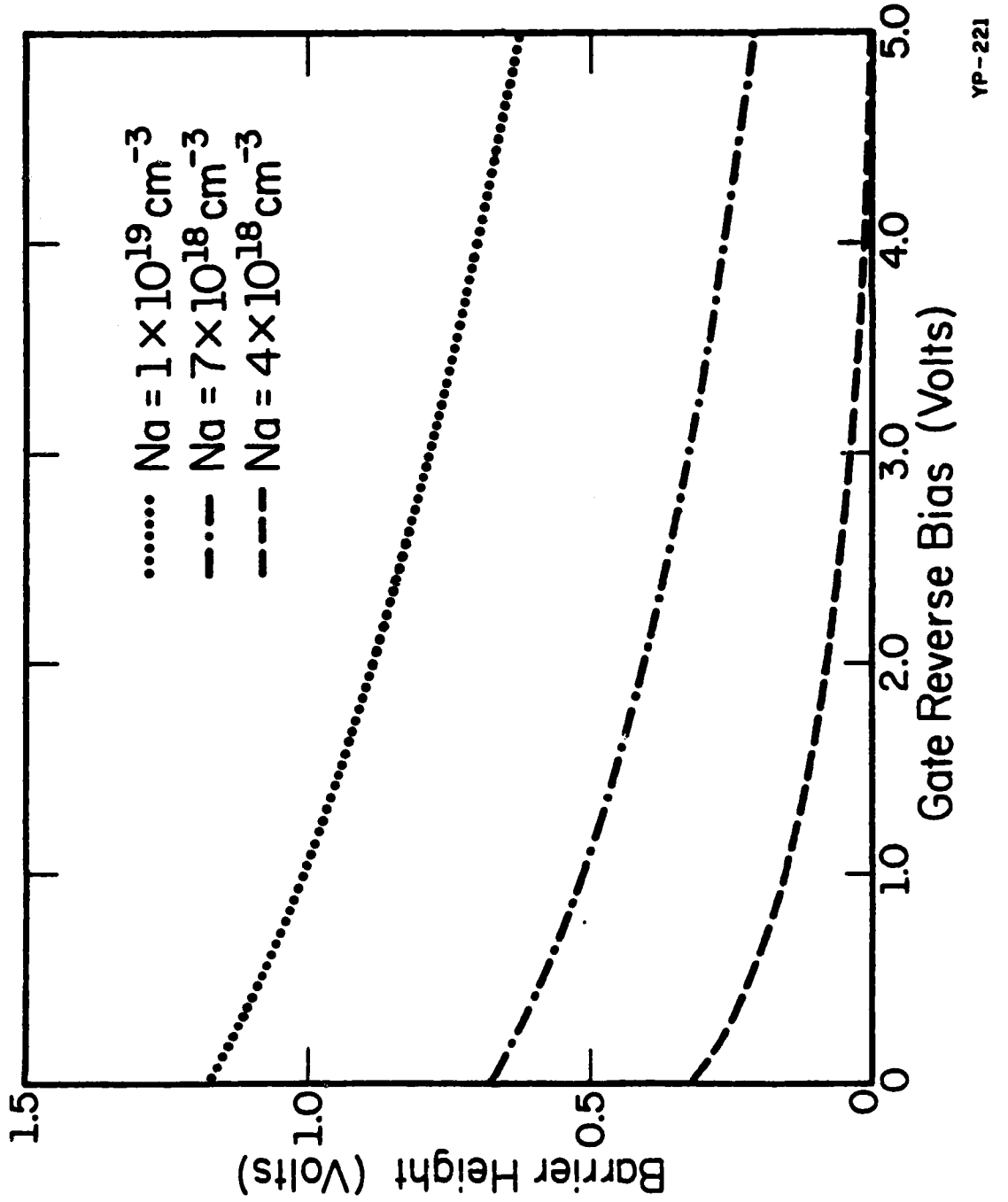

Figure 5: Barrier height to current conduction via thermionic emission ϕ_B vs. gate reverse bias.

the barrier height.

The dependence of the depletion depth W into the FET channel on gate reverse bias is illustrated in Figure 6. For comparison purposes, the depletion depth of a Schottky barrier with a 0.8 V built-in voltage is also illustrated. The depletion depth of a camel gate increases more slowly with applied bias than does that of a Schottky gate. One way of looking at this phenomenon is in terms of the reduction in barrier height with applied gate bias. From equation (7), W increases with the square root of $\Phi_B - \Phi' - V_a$, where Φ' is a constant, similar to a Schottky barrier. However, since Φ_B decreases with increasing reverse bias, the total effective potential depleting the channel is reduced, so that W increases more slowly than if Φ_B were constant.

Figure 7 gives the relation between d, the depletion depth into the n^+ layer, and the gate reverse bias. The decrease in depletion depth with increasing reverse bias is a consequence of charge conservation. The sum of the charges in the n^+ and channel depletion layers is equal to the charge in the p^+ layer. Consequently, under reverse bias, an increase in the charge in the channel depletion layer must be accompanied by a corresponding decrease in that of the n^+ depletion layer. The depletion depth for $N_a = 1 \times 10^{19}$ cm^{-3} is about 100 Å. For $N_d^+ = 7 \times 10^{18}$ cm^{-3}, surface states will deplete about another 120 Å. Thus, provided the n^+ layer is less than about 200 Å thick, it will be fully depleted. As discussed later, this fact can greatly simplify fabrication of the FET.

The intrinsic transconductance g_m of a CAMFET operating in the saturated velocity limit is illustrated in Figure 8. The saturation velocity is assumed to be 1.4×10^7 cm/s. Again, the corresponding g_m for a MESFET with a 0.8 V barrier height is also indicated. By choosing a small p^+ doping N_a,

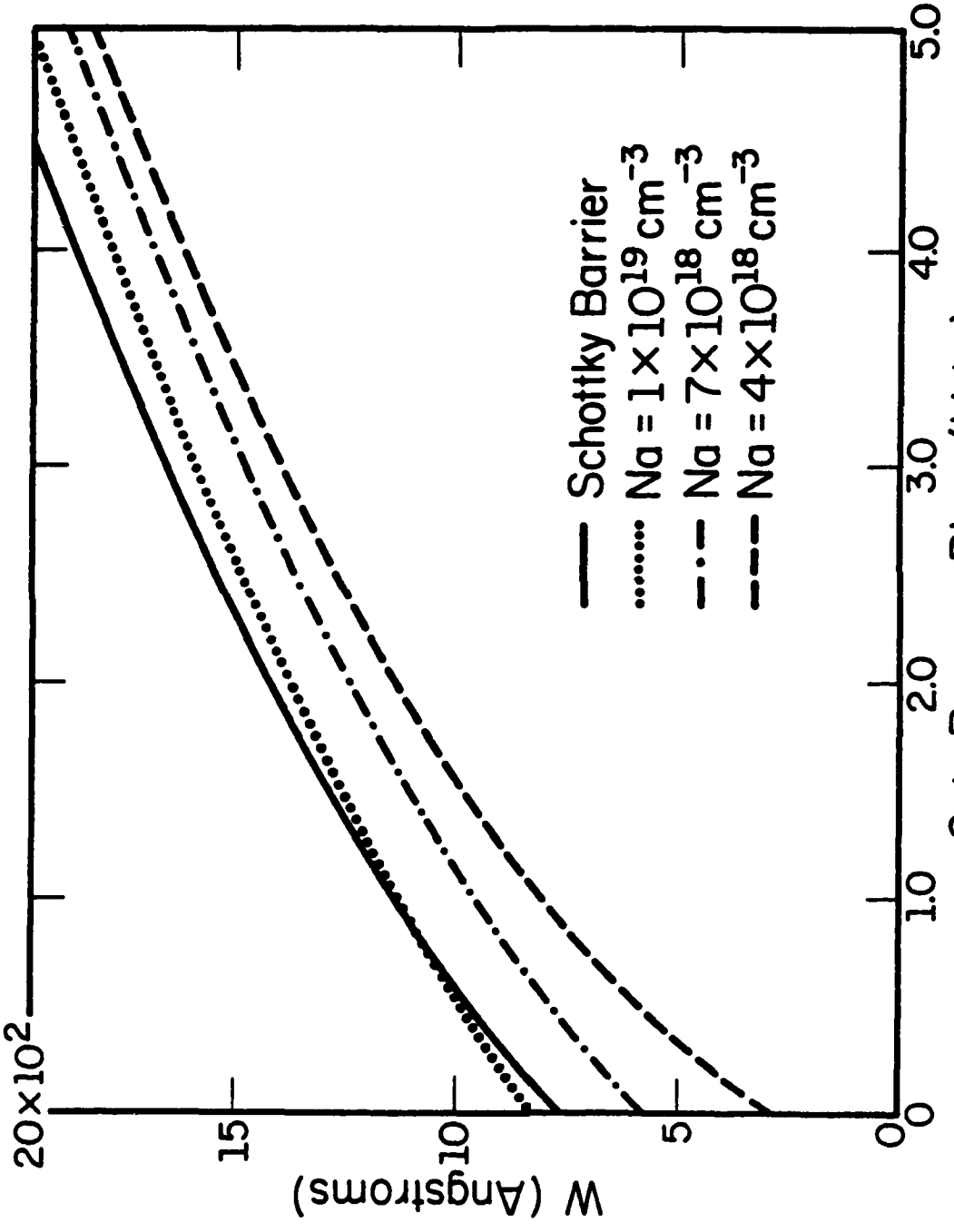

Figure 6: Depletion depth W into the CAMFET channel vs. gate reverse bias. The depletion depth for a 0.8 V Schottky barrier is also shown.

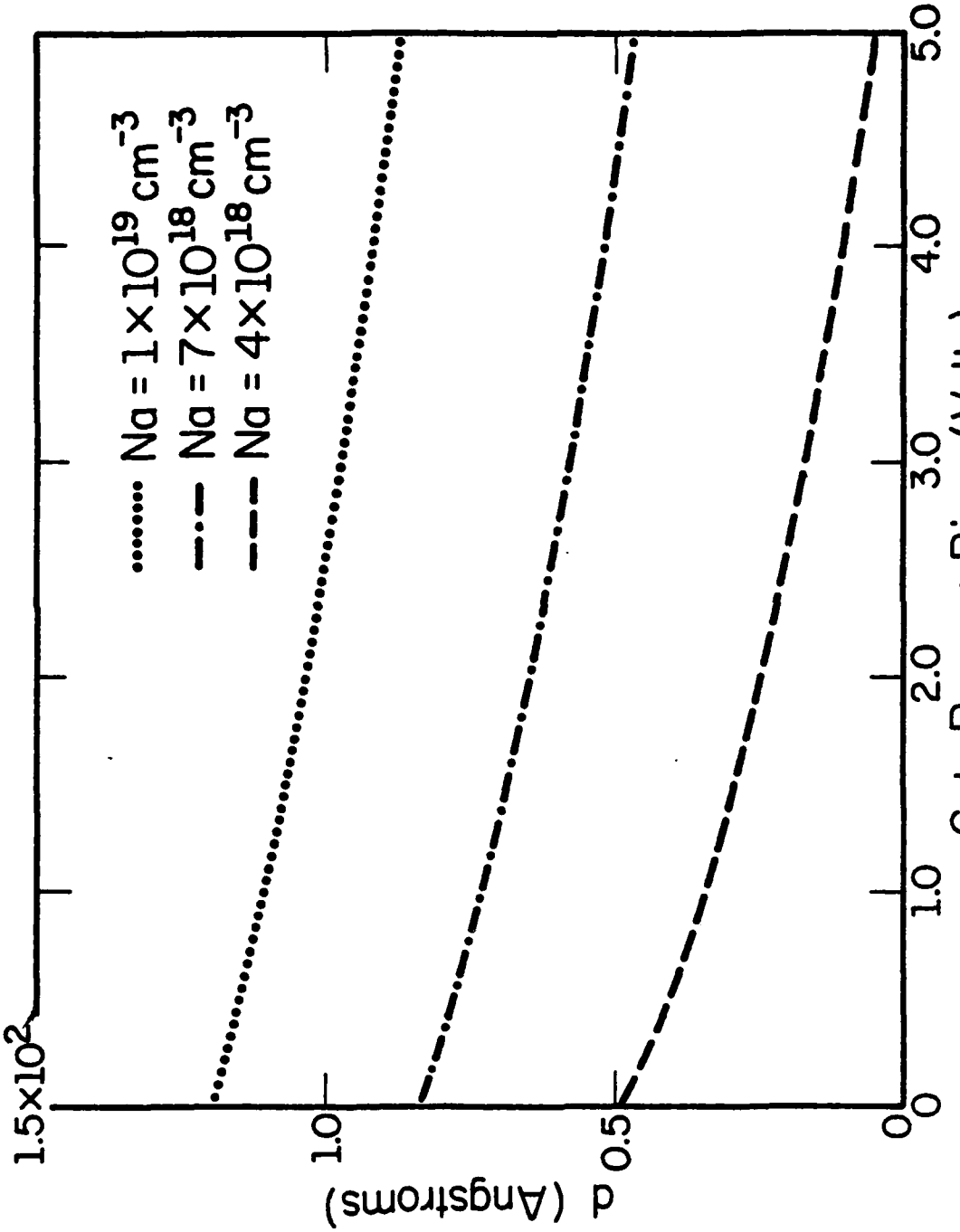

Figure 7: Depletion depth d into the n^+ layer vs. gate reverse bias.

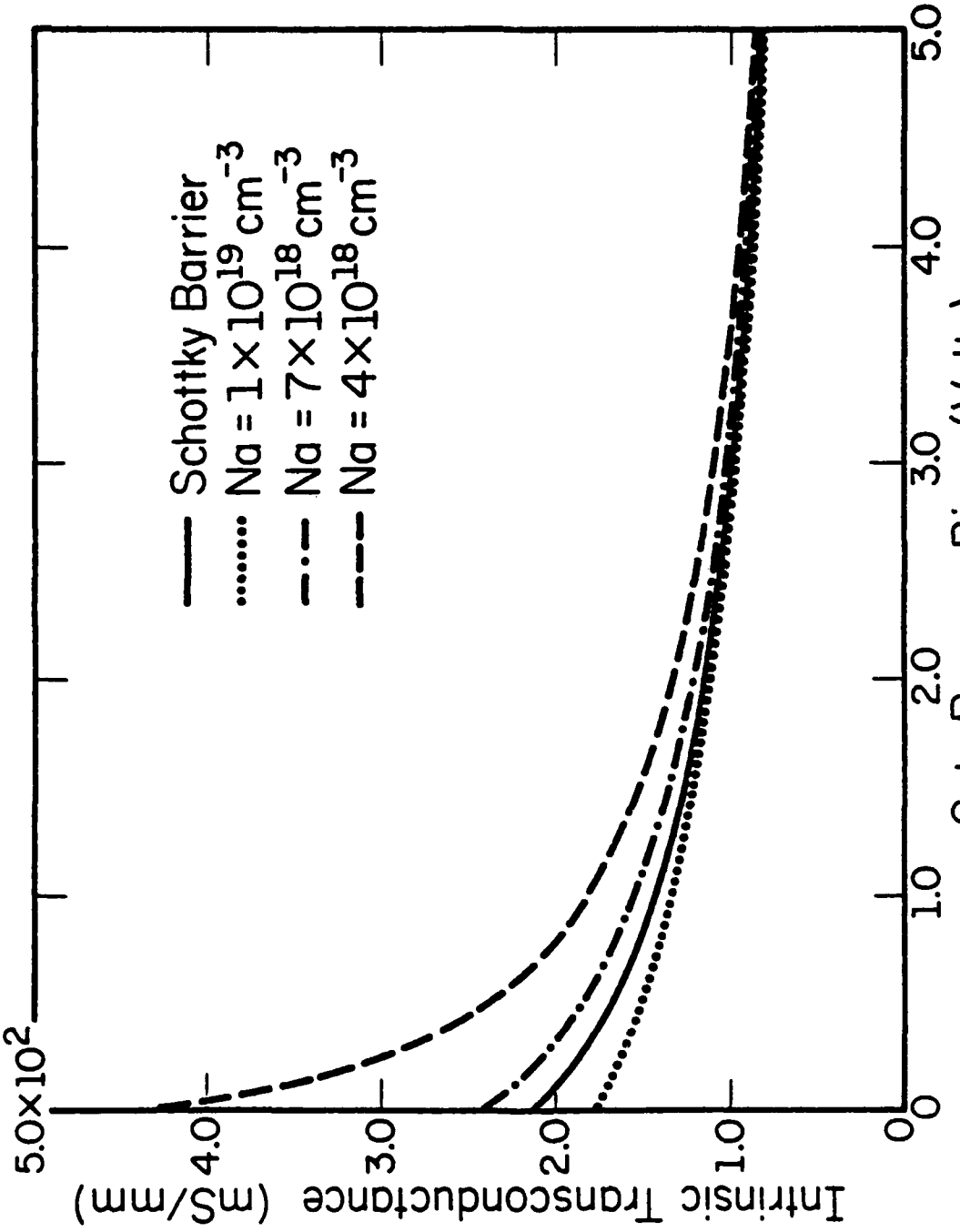

Figure 8: Intrinsic transconductance of a CAMFET in the saturated velocity limit vs. gate reverse bias, as well as that of a Schottky gate FET.

a large g_m can be obtained. Conversely, a large N_a yields a small g_m. Note also that for large N_a, the transconductance shows a relatively small variation with gate bias. Such a device should yield reduced third harmonic distorsion, and thus perform well as a linear amplifier.

The high frequency performance of an FET depends not only on the transconductance but on the gate capacitance, which is illustrated in Figure 9. In particular, an important figure of merit is $f_T = g_m/2\pi C_{gs}$. For short channel devices, f_T depends only on geometrical factors and material parameters, and not on the structure of the layers. Consequently, the high frequency performance of camel gate FETs should be similar to that of MESFETs.

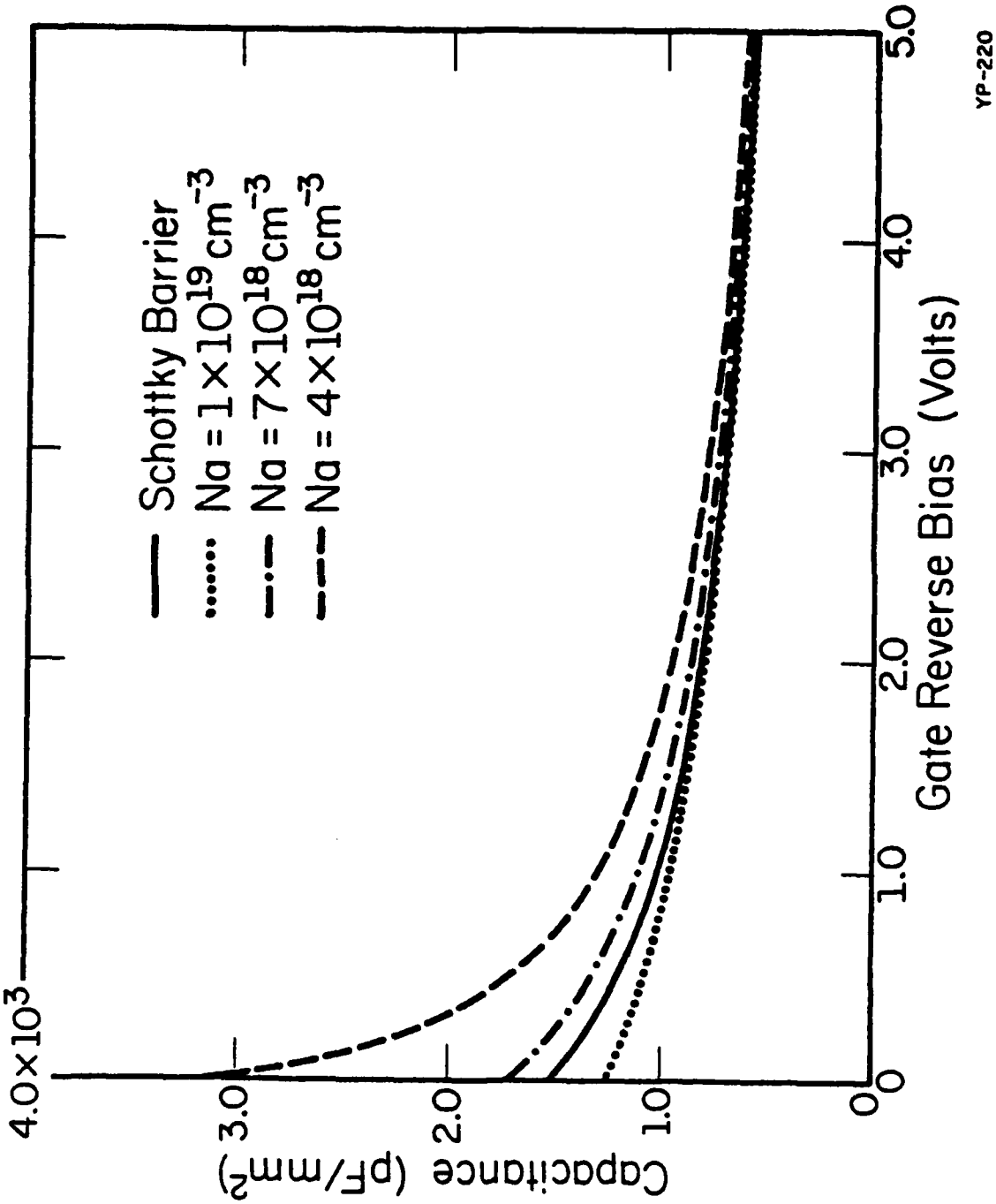

Figure 9: Gate depletion capacitance of a CAMFET vs. gate reverse bias, as well as that of a Schottky gate.

IV. EXPERIMENTAL PROCEDURE

A. Growth by Molecular Beam Epitaxy

In order to test the basic idea of the camel gate FET and to investigate its properties, a large number of devices with a wide range of structural parameters were fabricated. The layers from which these devices were fabricated were grown on (100) oriented chromium doped semi-insulating GaAs substrates using molecular beam epitaxy (MBE) [15][16]. MBE was chosen for two reasons. First, it was readily available. Second, and more importantly, MBE allows preparation of high quality semiconductor films with unsurpassed control of layer thickness (down to a few atomic layers) and doping profiles. These features were particularly useful in preparing the thin (100 Å), highl· doped p^+ layer of the camel gate.

The substrates were prepared for epitaxial growth by first degreasing and then etching them in a 5:1:1 H_2SO_4:H_2O_2:H_2O solution. The purpose of the etch was to remove any oxide and to provide a smooth surface for growth. The substrates were next etched briefly in HCl to remove any organic residues and to passivate the surface. Finally, the substrates were mounted on molybdenum blocks using indium and loaded into the MBE system.

The MBE system used was a Riber model MBE 1000. As illustrated in Figure 10, this system was equipped with a sample exchange chamber, a liquid nitrogen cooled cryoshroud, as well as several analytical instruments.

Before beginning growth of the layers, the substrate was heated to 630 C to desorb the surface oxide. The substrate temperature was then lowered to the growth temperature - typically 580 to 610 C - and the growth initiated.

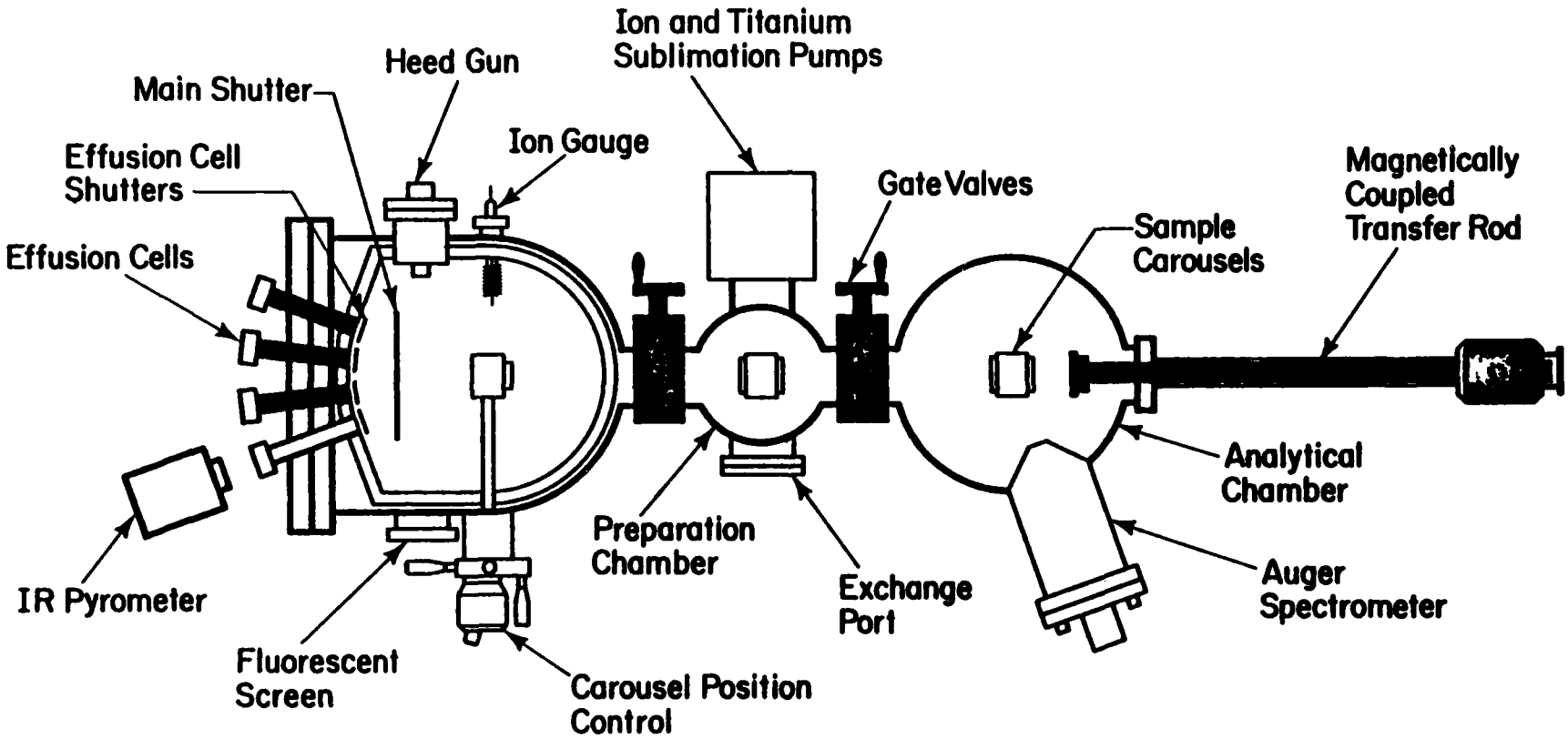

Figure 10: Schematic view of the molecular beam epitaxy used to grow the CAMFET structures.

The layers were grown under arsenic-stabilized conditions, with a group V/III ratio of approximately 3:1 to provide high quality layers with a minimum of Ga vacancies. The Ga flux was adjusted to give a GaAs growth rate of roughly 1 μm/hr. The dopants used for the channel, p^+ and n^+ layers were silicon, beryllium and tin, respectively.

For all of the FET structures grown, a 1 μm thick undoped GaAs or (Al,Ga)As layer was grown directly on top of the substrate. The purpose of this buffer layer was to reduce propagation of defects from the substrate and to provide an atomically smooth, clean surface on which to grow the FET channel [17].

B. Device Fabrication

Although a variety of FET configurations were fabricated, only long-channel normally-off and short-channel normally-on devices will be discussed here. A cross-sectional view of a long-channel normally-off camel gate FET is illustrated in Figure 11. The (Al,Ga)As p^+ layer was used to allow selective etching techniques to be employed in fabricating the devices.

Fabrication of normally-off CAMFETs began with etching isolation mesas. Source-drain windows were photolithographically defined and the n^+ and p^+ layers removed using $NH_4OH:H_2O_2:H_2O$ and HF selective etches, respectively. The etching of the p^+ layer resulted in slight undercutting of the n^+ layer. A AuGe/Ni/Au source-drain metallization was then evaporated, lifted off, and alloyed into the FET channel in an H_2 atmosphere at 500 C for 1 minute. The 1 μm gate metal pattern was then defined and Au gate metallization evaporated. No alloying of the gate metal was necessary to obtain ohmic contacts because of the heavy doping of the n^+ layer [18]. The completed devices had 400 Å n^+ layers, 100 Å p^+ layers, 500 Å channels, 3 μm channel lengths, gate lengths of just under 3 μm, and gate widths of 145 μm.

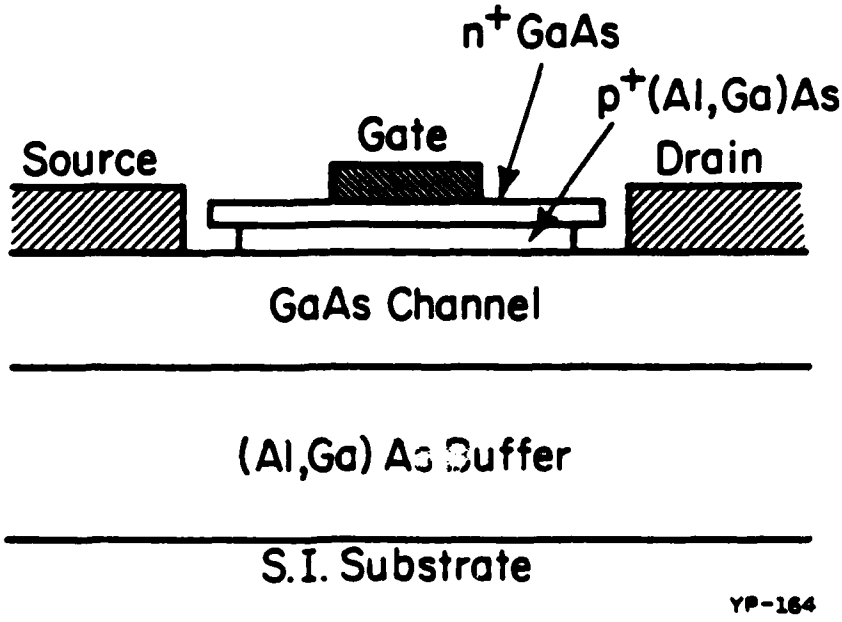

Figure 11: Cross-sectional view of a long-channel normally-off CAMFET with an (Al,Ga)As p^+ layer.

A slightly different procedure was used to fabricate the short-channel normally-on FETs. After the mesa etch, the source and drain patterns were photolithographically defined and then a AuGe/Ni/Au metallization evaporated directly on top of the n^+ layer. The metallization was then lifted off and alloyed through the n^+ and p^+ layers into the channel in an H_2 atmosphere at 500 C for 1 minute. (The n^+ layer thickness was reduced to 200 Å to facilitate this alloying.) This procedure yielded contacts with specific contact resistivities, as determined using the transmission line method, in the low 10^{-6} Ω-cm range. The gate pattern was then defined and a Au gate metallization evaporated.

The next step in the fabrication of the CAMFETs was to have been to etch the n^+ and p^+ layers between the gate and source and drain, using the gate, source and drain metallizations as a mask. However, experiments showed that, for sufficiently thin n^+ layers, the FET characteristics were unaffected if the n^+/p^+ gate layers were left unetched. The reason for this is clear. As explained previously, the parameters of the structure are chosen so that the p^+ layer is fully depleted. If the n^+ layer is sufficiently thin, it too will be fully depleted by Fermi pinning at the surface and charge transfer to the p^+ layer. Since both layers are fully depleted and thus nonconducting, leaving them unetched does not affect the FET characteristics.

Figure 12 shows a cross-sectional view of a short-channel normally-on CAMFET. The device had a 0.2 μm channel thickness, a 3 μm source-drain spacing, a 1 μm gate length, and a 145 μm gate width.

In summary, the important features of this fabrication procedure are as follows. First, unlike the JFET, no critical etching steps are involved, so that submicron dimensions required for high frequency operation should be as readily obtained as for the MESFET. Second, all metal contacts are ohmic and

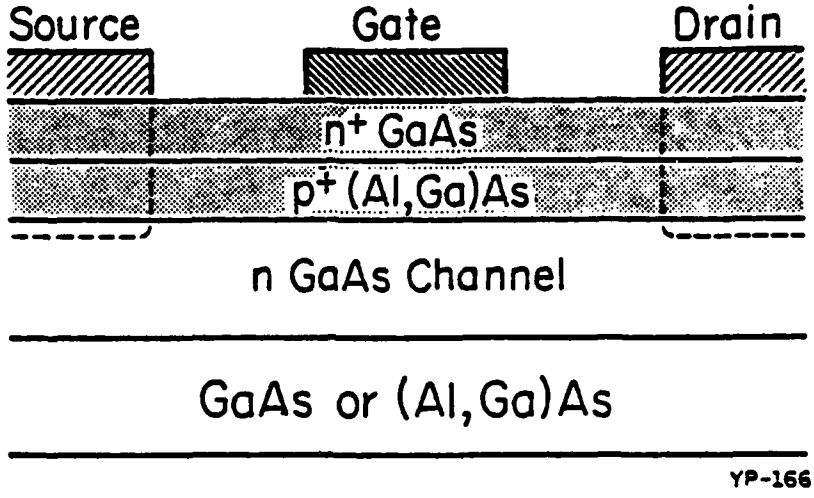

Figure 12: Cross-sectional view of a short-channel normally-on CAMFET with an (Al,Ga)As p^+ layer.

are made to n^+ GaAs. This should result in lower contact resistances than in the JFET, and better reliability than in the MESFET.

V. EXPERIMENTAL RESULTS

A. DC Characteristics

The three terminal characterstic of a long-channel normally-on CAMFET with the n^+ and p^+ layers removed from between the gate, source and drain is shown in Figure 13. The device saturates well and has a maximum normalized transconductance of 80 mS/mm of gate width. The reverse gate-drain breakdown voltage was roughly 30 V.

Figure 14 shows the three terminal characteristic of a short-channel normally-on CAMFET for which the n^+ and p^+ layers were left unetched. This device saturates and pinches off very well, and the maximum transconductance is 120 mS/mm. Good pinch-off and very low gate leakage, even at large drain voltages, were characteristic of virtually all the CAMFETs fabricated. In comparison, Schottky gate FETs with comparable characteristics were obtained far less consistently.

The gate-drain I-V characteristic of this short-channel device is shown in Figure 15. The breakdown voltage of 30 V is extremely high for a device with a gate-drain spacing of 1 μm and a channel doping of 2×10^{17} cm^{-3}. This compares with a value of 10 V for similar geometry MESFETs fabricated in our laboratory.

B. Influence of p^+ Layer Doping-Thickness Product

To further investigate the properties of CAMFETs and to test the theory, a large number of short-channel normally-on devices were fabricated. As described previously, the doping-thickness product of the p^+ layer is most important in determining the properties of the camel gate. Thus, several layers were grown with varying p^+ dopings and the rest of the parameters similar. The parameters chosen were nominally $N_d^+ = 6 \times 10^{18}$ cm^{-3}, Nd = 8×10^{16} to

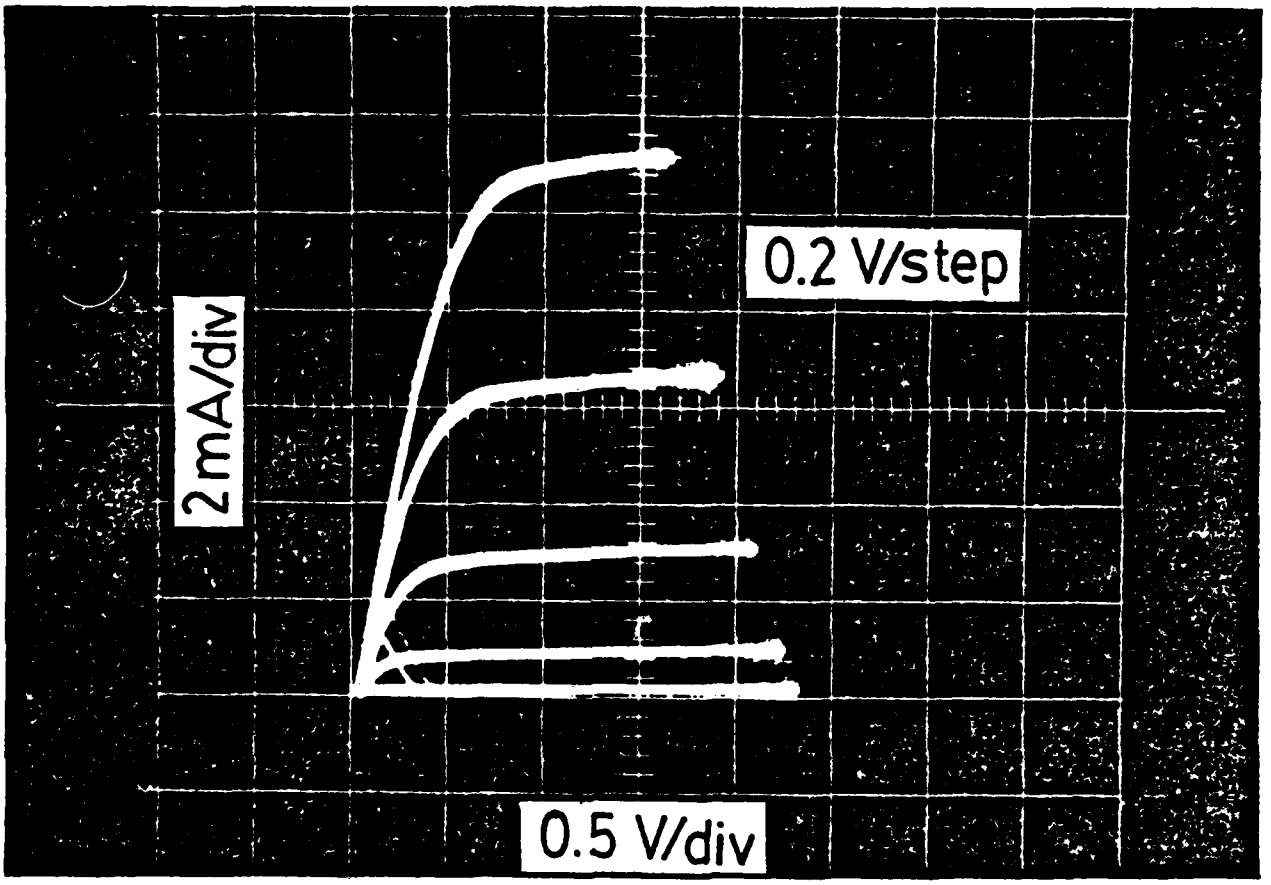

Figure 13: Three terminal characteristic of a 3 μm gate long-channel normally-off CAMFET.

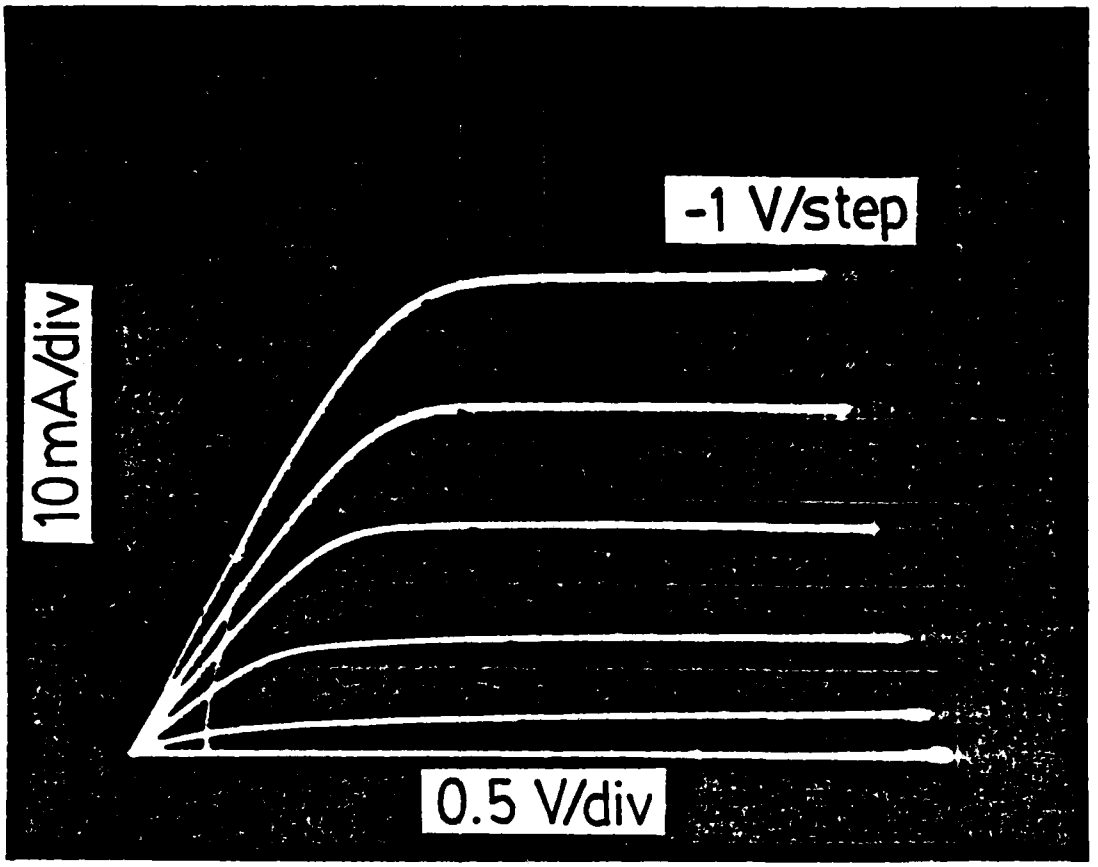

Figure 14: Three terminal characteristic of a 1 μm gate short-channel normally-on CAMFET.

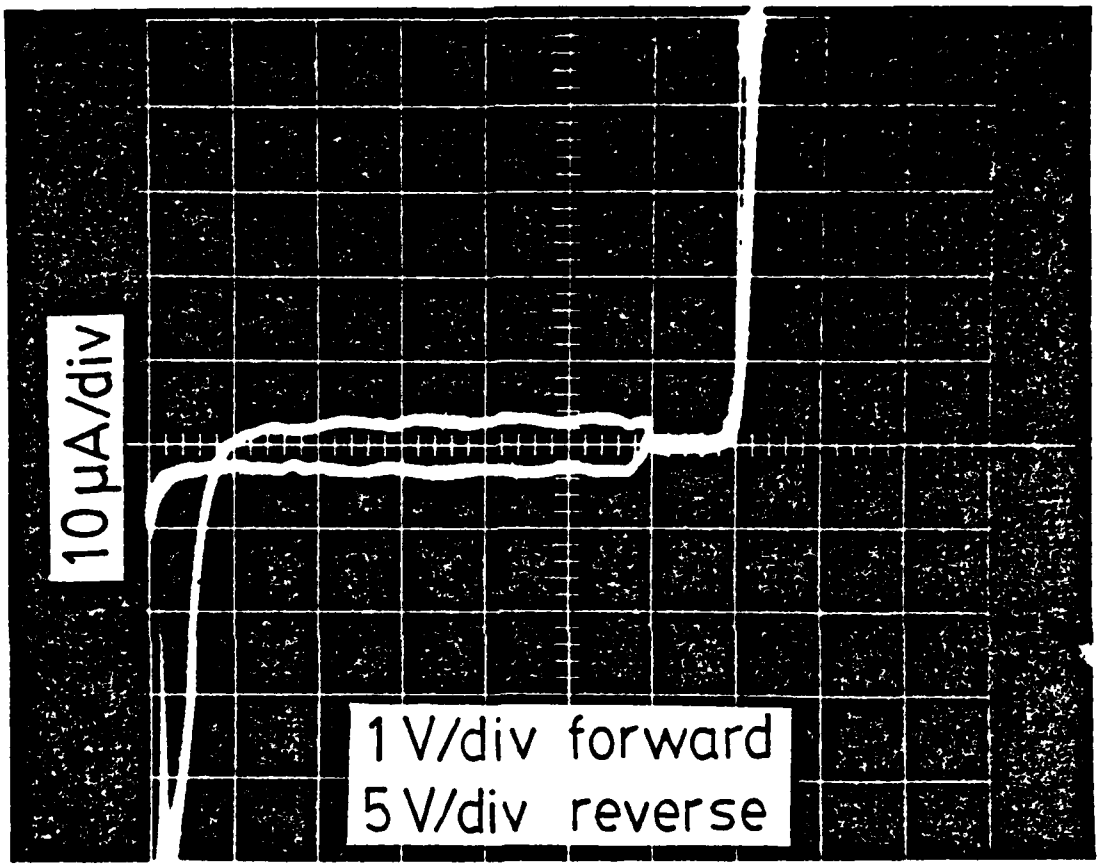

Figure 15: Gate-drain I-V characteristic of the CAMFET of Figure 14.

2×10^{17} cm^{-3}, and t = 100 Å. The p^+ doping was varied between 5×10^{17} and 2×10^{19} cm^{-3}.

Figure 16 shows the three terminal characteristic of a CAMFET with $N_a = 3.5 \times 10^{18}$ cm^{-3} and $N_d = 8 \times 10^{16}$ cm^{-3}, while Figure 17 shows the characteristic of a device with $N_a = 6 \times 10^{18}$ cm^{-3} and $N_d = 1.5 \times 10^{17}$ cm^{-3}. Both devices had $Al_{0.3}Ga_{0.7}As$ p^+ layers. The transconductance of the device with the more heavily doped p^+ layer is smaller and varies less with gate bias than does that of the more lightly doped device. This performance is consistent with the general trend that heavier p^+ dopings lead to smaller, more uniform transconductances. These results also agree with theory.

Figures 18 and 19 give both the experimental and theoretical capacitance-voltage characteristics for FATFETs fabricated on the same wafers as the devices of Figures 16 and 17, respectively, as well as experimental characteristics for aluminum Schottky barrier FATFETs with comparable channel dopings and identical geometries. The capacitance of the FATFET of Figure 18, which has the more lightly doped p^+ layer, is quite comparable with that of the MESFET. The transconductances, forward gate-source I-V characteristics, and source resistances were also very similar. These results are consistent with the CAMFET's theoretical zero bias barrier height of 0.85 V. In contrast, the capacitance as well as transconductance of the camel FATFET with the more heavily doped p^+ layer is smaller than that of the MESFET. The theoretical zero bias barrier height of this device was 1.35 V. Note the good agreement between theoretical and experimental capacitances in both figures.

The reverse gate-drain breakdown voltage of CAMFETs was very sensitive to p^+ doping. For large dopings, breakdown voltages of up to 30 V were obtained. In addition, the breakdown of these devices was very abrupt, charac-

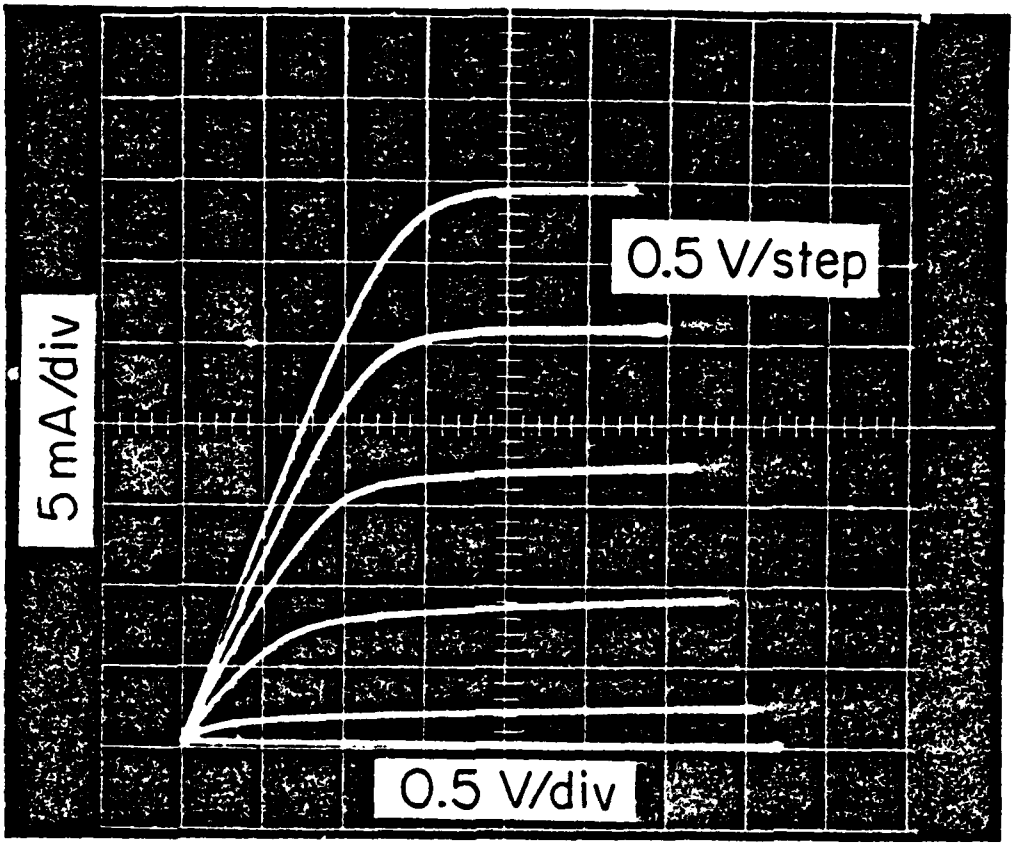

Figure 16: Three terminal characteristic of a CAMFET with $N_a = 3.5 \times 10^{18}$ cm^{-3} and $N_d = 8 \times 10^{16}$ cm^{-3}.

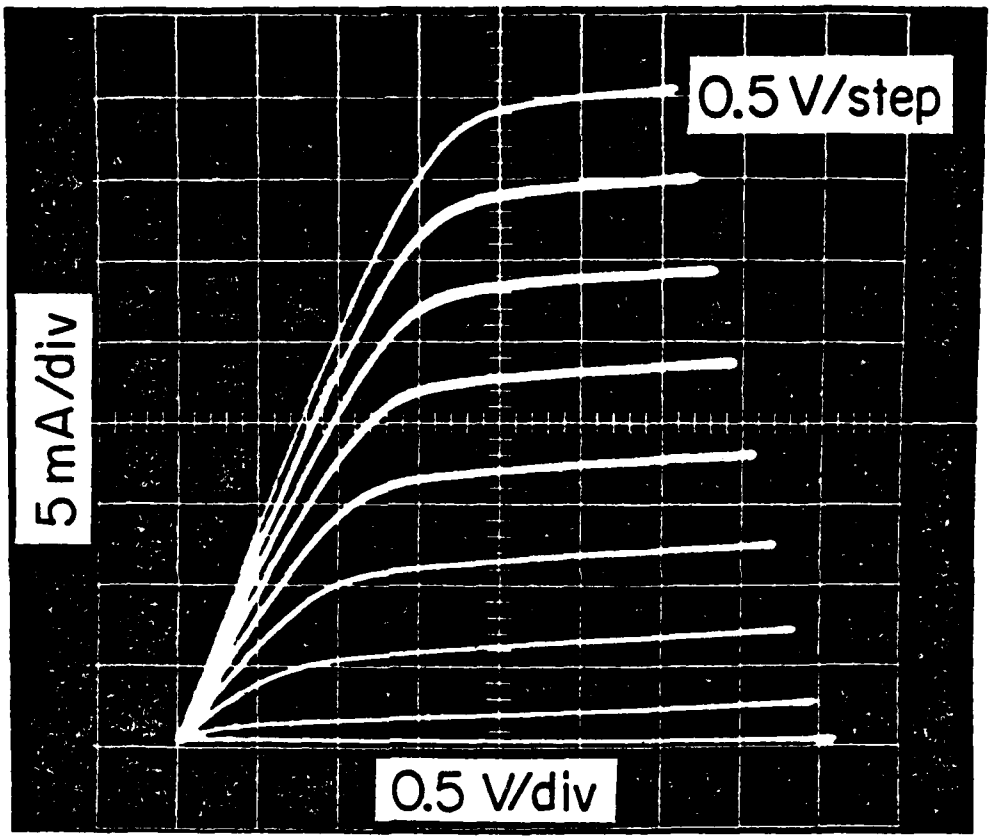

Figure 17: Three terminal characteristic of a CAMFET with $N_a = 6 \times 10^{18}$ cm^{-3} and $N_d = 1.5 \times 10^{17}$ cm^{-3}.

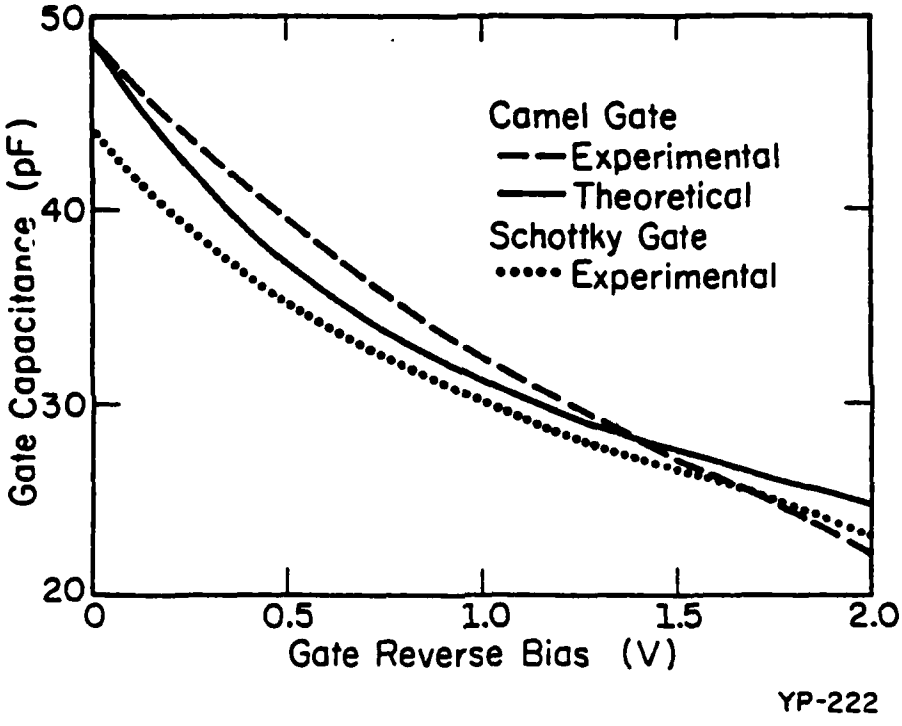

Figure 18: Experimental and theoretical gate capacitances for a FATFET fabricated on the same wafer as the device of Figure 16, as well as the experimental gate capacitance of a Schottky gate FATFET with identical geometry and similar channel doping. The FATFET area is 4.6×10^{-4} cm^2.

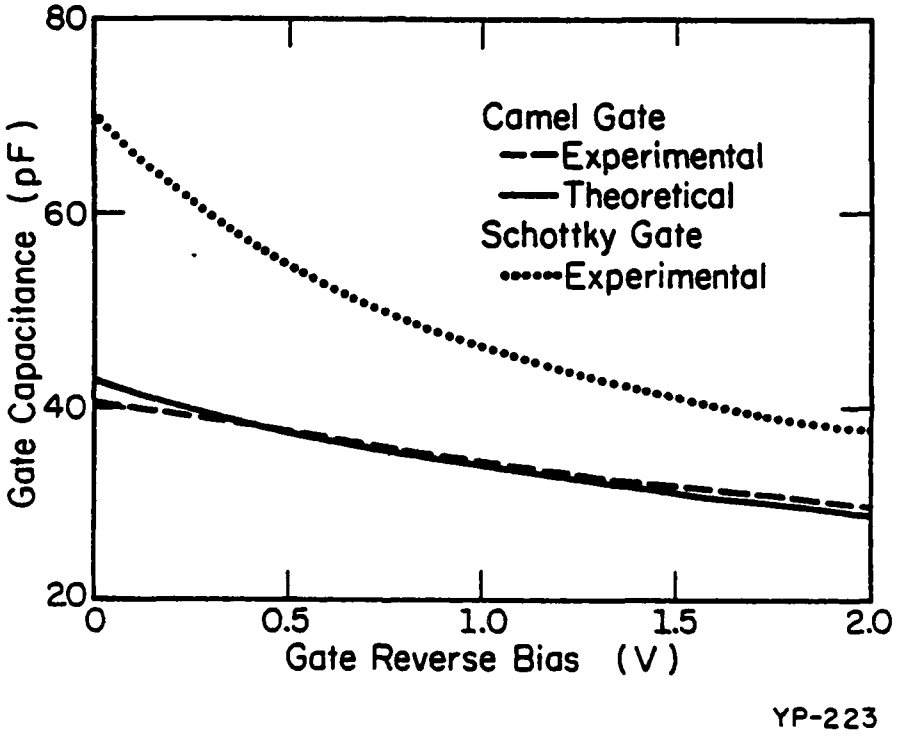

Figure 19: As in Figure 18, for a FATFET fabricated on the same wafer as the device of Figure 17.

teristic of avalanche breakdown. As the p^+ doping decreased, the breakdown voltage also decreased. For example, the device with the p^+ doping of 5×10^{17} cm^{-3} had a breakdown voltage of only 6 V. Further, the breakdown of the more lightly doped devices tended to have a "soft" exponential form. These results again agree well with theory, which predicts that for large p^+ dopings, appreciable barrier heights should be maintained even under large reverse bias conditions. In this case, avalanching due to excessive fields should be the breakdown mechanism. On the other hand, smaller p^+ dopings should result in the barrier becoming very small at relatively small reverse gate biases. This barrier lowering gives rise to the current conduction at breakdown and the "soft" breakdown characteristics.

The implications of the experimental results presented are that for power FETs, for which transconductances independent of gate voltage, large barrier heights, and large breakdown voltages are desirable, the p^+ layer should be heavily doped. For logic applications, the speed is related to g_m/C_{gs}. Because parasitics may dominate the C_{gs} term, a large g_m and thus smaller p^+ doping are indicated. Logic applications may also require larger barrier heights for compatibility with other circuits, and these may be obtained as well, although at the cost of a reduced g_m, unless an (Al,Ga)As p^+ layer is used.

C. Microwave Performance

In addition to DC and C-V measurements, some preliminary evaluation of the microwave performance of CAMFETs has also been carried out. The measurements were made by first mounting the FET in a microwave transistor test fixture and bonding connections to 50 Ω microstrip line. A Hewlett Packard 8409B Automatic Network Analyser was then used to measure the S-parameters at frequencies between 2 and 13 GHz. A de-embedding procedure was used to extract

the S-parameters of the FET.

Figure 20 shows the maximum available gain (MAG) versus frequency characteristic for a device similar to that of Figure 16. The gain is approximately 10 dB at 9 GHz, and the maximum frequency of oscillation is about 30 GHz. While not state of the art, these results are surprisingly good given that no attempt was made to optimize the FET structure for microwave performance.

D. Miscellaneous Experimental Results

i) Camel Gate Modulation-Doped FETs

In addition to conventional GaAs FETs, the camel gate concept was also applied to GaAs/(Al,Ga)As modulation-doped FETs. The top layer of the so-called "normal" modulation-doped structures is (Al,Ga)As, which oxidizes rapidly when exposed to air. Camel gates are particularly attractive in this application. Not only do they obviate the need for making a rectifying contact to (Al,Ga)As, but being grown in situ with the rest of the structure, they eliminate the possibility of oxidation as well. Camel gate modulation-doped FETs with good characteristics and transconductances (95 mS/mm for a 4 μm device) comparable to Schottky gate FETs have been obtained [19].

ii) Back-to-Back Diode Gate FET

Although larger p^+ doping-thickness products give larger barrier heights and a more voltage independent transconductance, eventually a product is reached for which the p^+ layer is no longer fully depleted. This results in shorting of the gate to the source and drain and necessitates etching of the n^+ and p^+ layers. The gate in this case consists of back-to-back p-n diodes. Devices with good DC characteristics can still be obtained; however, preliminary microwave measurements indicate relatively poor high-frequency performance.

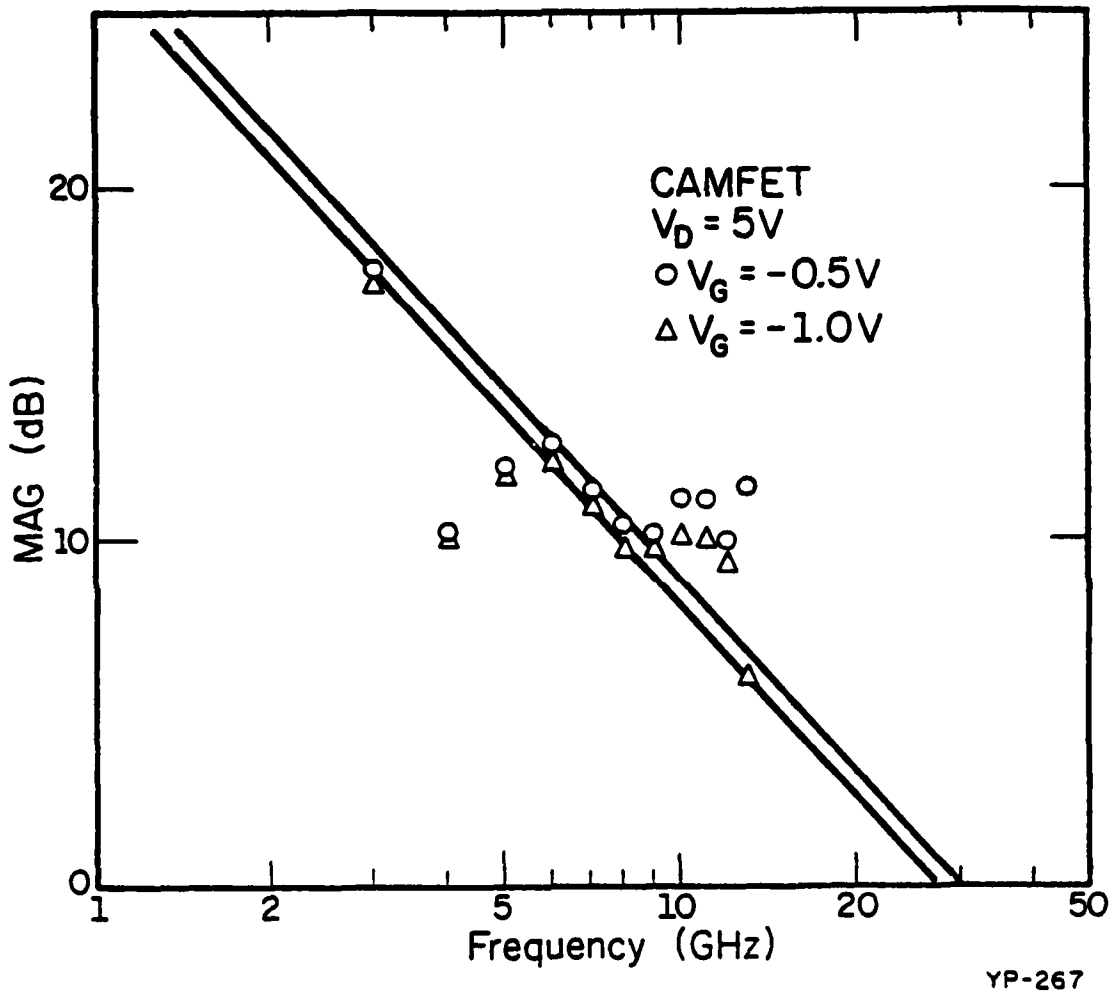

Figure 20: Maximum available gain vs. frequency for a CAMFET similar to that of Figure 16.

iii) Recessed-Gate CAMFETs

A standard technique to reduce the source resistance of MESFETs is to perform a gate recess, in which the Schottky metal is evaporated into an etched groove in the channel. Gate recessing in CAMFETs, although more difficult, is also possible. In this case, the FET channel layer is grown, removed from the MBE system, and a notch for the gate etched. The etched wafer is then returned to the MBE system and the n^+ and p^+ layers of the camel structure grown. Devices with reasonably good characteristics, although relatively small breakdown voltages, have been obtained using this procedure.

iv) n^+ Layer Depletion

In order to determine the maximum n^+ layer thickness which would still be fully depleted, a series of FET layers were grown with varying n^+ thicknesses. For a p^+ doping of 6×10^{18} cm^{-3}, this thickness was found to be about 600 Å. Calculation of the depletion by the surface potential and by the p^+ layer, assuming a surface potential of 0.7 V and a uniform doping profile, indicated an n^+ layer thickness of only 200 Å. The reason for this difference between the two values is not completely understood at this time, but may be due to surface segregation of the tin in the n^+ layer [20]. Surface segregation could result in a doping profile which increases away from the p^+ layer and thus in a larger depleted thickness than for a uniform profile.

v) Application to Other Material Systems

The camel gate concept is a general one, and may be applied to any material system. In particular, camel gates have promise for applications in some small bandgap semiconductors for which it is difficult to obtain Schottky barriers with acceptable characteristics. Preliminary work with one such semiconductor, $In_{0.53}Ga_{0.47}As$, has yielded CAMFETs with reasonably good characteristics, especially at 77 K.

E. Viability of the CAMFET

In spite of its many advantages, is the CAMFET a commercially viable device? There are many issues which must be dealt with in answering this question, most of which are beyond the scope of this research. However, possibly the most important issue regards the ability to obtain the required control over layer dopings and thicknesses. For many applications (i.e. logic circuits), very uniform, controllable FET characteristics over a large area are required. Clearly, the blessing of easy variation in CAMFET parameters with the p^+ layer doping-thickness product can become a curse if the dopings and thicknesses cannot be adequately controlled. Although a detailed analysis has not been performed, experimental results for MBE grown layers indicate the required doping profiles are obtainable. And with current MBE technology, which employs rotating substrate holders, the uniformity requirements should easily be satisfied, making CAMFETs competitive with MESFETs.

VI. RECOMMENDATIONS

Before CAMFETs see commercial application, additional experimentation and evaluation will be required. One of the most important issues to be addressed regards the application of camel gates in power devices. An initial study should involve examining operation of camel diodes under large forward bias. It has been suggested that camel gates may be subject to a regenerative process in which hole accumulation in the potential minimum in the p^+ layer, under heavy forward bias conditions, could result in collapse of the barrier and destruction of the gate by excessive currents. This would restrict the maximum input signal swing which could be applied to a camel gate. Although the minority carrier lifetimes in GaAs are likely short enough to prevent this from happening, a systematic study of current transport would nevertheless help to eliminate this reservation about the CAMFET. After these current studies, fabrication and testing of power CAMFETs should be undertaken.

A second area requiring further study is the microwave performance of CAMFETs. To accomplish this, deficiencies in our microwave transistor test fixture, which hindered interpretation of results, should be overcome. Optimization of the CAMFET structure for microwave performance should be attempted. Noise measurements should also be performed, so that noise figures and the associated gains, most useful for evaluating microwave performance, may be determined. The results of the S-parameter and noise measurements should then be used to obtain an equivalent circuit for the CAMFET.

Other issues which may be investigated include why CAMFETs exhibit such large breakdown voltages. An answer to this question might prove useful in the design of other devices. Finally, a comparative study of the reliabilities of CAMFETs, JFETs, and MESFETs should be attempted.

VII. CONCLUSIONS

This thesis has described an alternative FET structure to the JFET and MESFET, which uses the voltage-variable depletion width of a camel diode for modulating the FET current. The structure, fabrication, and performance of these devices, known as camel gate FETs or CAMFETs, have been presented.

Fabrication of CAMFETs is as simple as for MESFETs. In particular, no critical etching steps are required, and all metal contacts are ohmic and are made to n^+ GaAs; consequently, the submicron dimensions required for high-frequency operation are readily obtained.

One of the principal virtues of CAMFETs is the wide range of FET characteristics which may be obtained by varying the gate layer dopings and thicknesses. For given n^+ and channel layer dopings, a large p^+ layer doping-thickness product yields a large gate-drain breakdown voltage, a large barrier height to current conduction, and a relatively voltage-independent transconductance. A CAMFET with these features should perform well in power applications, yielding larger power output and reduced third harmonic distortion relative to MESFETs. Conversely, CAMFETs with smaller p^+ layer doping-thickness products provide larger transconductances, and thus are well suited to logic applications.

Camel gate FETs are still in the early stages of development, and much work remains before they are optimized. However, experimental results obtained to date together with the many advantages of CAMFETs appear to point to a promising future in both discrete and large scale integrated circuit applications.

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