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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This document reports the results of a one-year program, based on a technical proposal submitted to and accepted by DARPA, to develop a technology for realizing a GaAlAs/GaAs monolithic integrated optoelectronic transmitter for high-speed fiber-optic communications applications. The primary objectives were to: (1) determine a suitable approach for integrating optical and electronic devices in terms of compatible device processing and fabrication, (2) design a simplified high-speed transmitter based on the integra-

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20. tion approach which will serve as a building block for future more sophisticated designs, (3) develop the transmitter materials technology, (4) develop the transmitter device components, and (5) fabricate and demonstrate the integrated transmitter.

At the end of the program, all of the objectives were realized except for the demonstration of a functional transmitter. A selective epitaxial growth technique using a dielectric mask was developed for process/fabrication compatibility of the laser with planar ion-implanted GaAs electronic devices with 1 μm-type geometries. Based on this integration approach, a nominal 1-4 Gb/s transmitter set utilizing standard cleaved mirror lasers and field-effect transistor (FET)/Gunn logic drivers was designed, process/fabrication steps defined, and a fabrication mask set generated. Metalorganic chemical vapor deposition (MOCVD) of GaAlAs/GaAs was used in the selective epitaxial growth of double heterostructure lasers on semi-insulating GaAs substrate qualified for GaAs integrated circuits (ICs). Narrow-diffused stripe (NDS) lasers and planar, ion-implanted FETs and Gunn devices were developed for the transmitter application. NDS lasers and 1-μm gate FETs were separately realized on S.I. GaAs wafers with selective groove-grown MOCVD heterostructures. These results initiated the processing of wafers for the fabrication of integrated transmitters. Demonstration lots were undergoing process development at the end of the program.

Although the demonstration of an integrated transmitter as conceived in this program was not realized, the techniques developed establish the feasibility of integrating optical devices based on GaAlAs/GaAs epitaxial growths with high-speed GaAs electronic devices based on a planar, ion-implantation.

TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

SUMMARY

This document reports the results of a one-year program, based on a technical proposal submitted to and accepted by DARPA,[1] to develop a technology for realizing a GaAlAs/GaAs monolithic integrated optoelectronic transmitter for high-speed fiber-optic communications applications. The primary objectives were to: (1) determine a suitable approach for integrating optical and electronic devices in terms of compatible device processing and fabrication, (2) design a simplified high-speed transmitter based on the integration approach which will serve as a building block for future more sophisticated designs, (3) develop the transmitter materials technology, (4) develop the transmitter device components, and (5) fabricate and demonstrate the integrated transmitter.

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1.0 INTRODUCTION

As the technology of electronic data processing continues to advance at a phenomenal rate, the limitations of present data communications systems become more and more apparent. The evolution of VLSI and VHSIC chips with higher switching speeds, lower power consumption, and greater circuit densities leads to new generations of computers which, though physically smaller than their predecessors, have faster central processing units and larger memories. As a result, input-output data rates for state-of-the-art computers are steadily increasing. This trend could even accelerate over the next few years with the advent of the new GaAs IC technology, which can provide much higher speed and lower power dissipation than the traditional silicon circuits. Furthermore, with continuing advances in analog-to-digital conversion technology, the quantity of digital data which is available from the analog output of sensors continues to increase rapidly. All of these factors lead to requirements for higher and higher communication data rates in information processing systems.

Coaxial cables and twisted wire pairs are still the primary media for data communications, just as they were decades ago. Data rates for these electrical transmission lines are limited to a few megabits per second per kilometer of length. These relatively low data rates are not adequate to meet the requirements of many of our modern military information processing systems.

The new technology which is capable of overcoming these limitations is fiber optics communications. Since the first low-loss (20 dB/km) fibers were produced ten years ago,[2] an optical communication industry based on the use of semiconductor light sources and photodetectors and silica fibers has evolved. Fibers with losses as low as 0.2 dB/km have been produced in the laboratory,[3] with losses of 2 dB/km routinely achieved in production. Experimental links have been operated at data rates as high as 1.6 Gb/s over transmission line lengths in excess of 10 km.[4] Although fiber optics has not

yet made a large impact in data processing due to the relatively high cost of components, it is anticipated that lower costs and requirements for larger transmission capacity will combine to make the technology cost-effective for an increasing number of civilian and military computer systems in the years ahead.

Data rates of state-of-the-art optical transmitters and receivers are limited to less than 2 Gb/s, yet there are military requirements for data transmission at much higher rates. One example is the distributed computer network illustrated in Fig. 1.1, in which the terminals communicate with one another in a burst transmission mode. Best performance in such a system is obtained if data are transmitted on the interconnecting bus at very high rates, much higher than the input-output data rates for the individual processors. Performance improvements are realized because the use of a very high-data-rate bus makes it possible to minimize the interterminal delays for the data packets.

In order to achieve transmitter and receiver performance at data rates substantially in excess of 1 Gb/s, it will be necessary to implement new concepts in transmitter and receiver design. In particular, considerable effort must be devoted to interfacing the optoelectronic components (lasers and photodiodes) with high-speed electronic devices such as FETs and Gunn or transferred electron logic devices (TELDs). By integrating the optoelectronic and electronic elements on the same substrate, it will be possible to optimize performance for high data rates by eliminating or minimizing problems associated with impedance mismatch, excess lead inductances, stray capacitance, and propagation delay within a transmitter or receiver. The most suitable substrate material for such an "optoelectronic integrated circuit" is S.I. GaAs. The fabrication of high-speed electronic components on such substrates is well established, and it has recently been demonstrated that lasers can be integrated with simple FETs[5] and TELDs[6] on the same substrate. Although the successful implementation of high-data-rate transmitters and receivers will require significant advances in the state-of-the-art of device technology, the payoffs

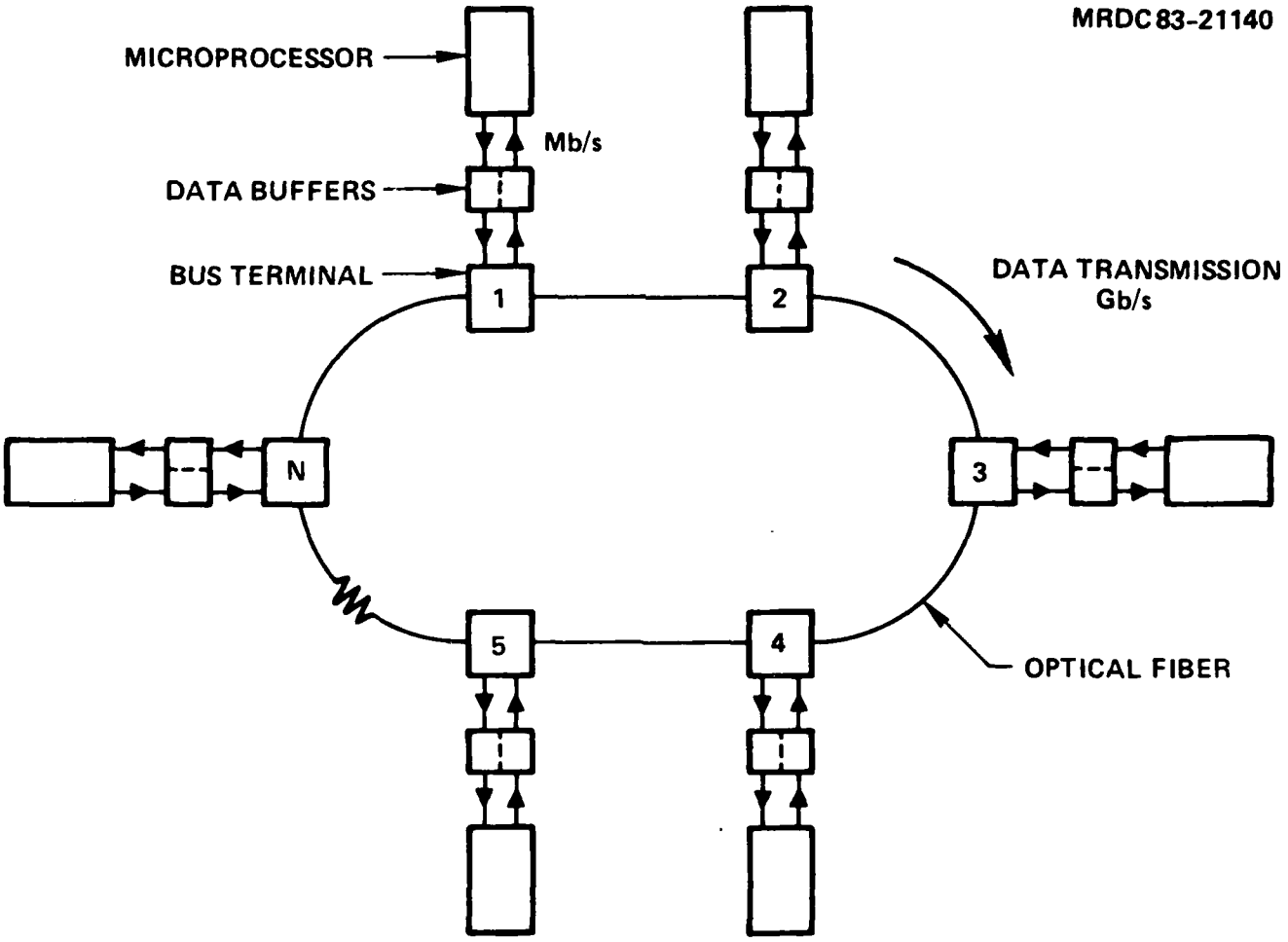


Fig. 1.1 Distributed computer network using a fiber optic bus.

in terms of performance and reliability for high-data-rate communications systems will be substantial.

This document reports the results of a one-year program to develop a GaAs monolithic integrated optoelectronic transmitter. The technology developed under this program serves as a basis for further transmitter work and application to integrated receiver development. These integrated optoelectronic components will be essential elements of high-speed fiber optical data buses for distributed computer networks as well as other wideband data transmission systems of interest to DoD.

2.0 MONOLITHIC OPTICAL/ELECTRONIC DEVICE INTEGRATION APPROACH

In this section a general monolithic integration scheme is formulated for realizing an optoelectronic transmitter. Current integration techniques are discussed, and a best approach for the short and long term development is presented. This approach utilizes a selective epitaxy on S.I. GaAs using a dielectric mask and was conceived to be compatible with planar, ion-implanted GaAs ICs which offer process and performance advantages. A simple high-speed integrated transmitter design is presented based on a standard cleaved-mirror laser structure chosen primarily for low-risk demonstration compatible with the short program duration. This transmitter design which incorporates the integration of selective optical device epitaxy with planar ion-implanted electronics serves as a basis for more complex, higher performance transmitter, receiver, and transceiver designs. The following sections describe in technical detail the development work of the monolithic integration approach and the specific integrated transmitter design.

2.1 Integration Concepts and Tradeoffs

Monolithic integrated optoelectronic circuits, which incorporate electronic and optical devices on the same substrate have potentially important advantages compared to conventional hybrid circuits. These include reduced size and complexity, potentially higher reliability, as well as significant improvements in speed and noise performance and reduced power requirements. The possibility of realizing complex, high performance electronic circuits in GaAs has motivated the development of integrated optoelectronic devices based on GaAlAs/GaAs optical sources and detectors for short distance optical communications applications.

Most of the GaAs integrated optoelectronics development work, to date, has focused on very simple structures. These include diode laser/FET[5] and diode laser/Gunn oscillator transmitters,[6] PIN/FET amplifier receivers[7]

and phototransistor/diode laser repeaters or transceivers.[8] Although S.I. GaAs is used as the common substrate for device isolation, most of the integrated structures have epitaxially grown electronic channels and non-planar configurations. Other integrated approaches use ion-implantation techniques after the epitaxial layers for the optical devices have been selectively etched away,[7] or, in the case of groove-grown epitaxy, the S.I. substrate surface is recovered by polishing.[9] However, these approaches are inherently difficult processing techniques in terms of control, uniformity, reproducibility, and yield.

In this program, we have considered integration techniques based on established technologies which offer performance as well as processing/fabrication advantages. GaAs electronic devices used for on-chip high-speed laser modulation require small gate lengths, on the order of 1 μm or less. Also if metal-semiconductor field-effect transistors (MESFETs) and Gunn logic devices are used on the same chip, different channel thicknesses are required. Typically, MESFETs have channel depths of a few tenths of a micron and Gunn channels are 1-2 μm thick. The use of epitaxial growth techniques for Gunn devices with MESFETs present processing and fabrication difficulties. In accommodating different types of high-speed device structures with small geometry features, the use of planar ion-implanted techniques facilitates fine-line lithography, area-selective channels with different depths, and channel uniformity and reproducibility. Ion-implanted channels have yielded high performance discrete MESFETs[10,11] and Gunn devices[12] and with selective implantation are also the basis for present high-speed GaAs monolithic microwave and digital ICs more routinely realized at the small to middle scale integration (SSI-MSI, 10-1000 gates) level.[13-17] However, in order to use planar, ion-implanted electronic structures in monolithically integrated optoelectronic devices, a process compatible optical device epitaxy must be developed. Such an epitaxial technique and its application to an integrated transmitter is described in this report.

2.2 Planar Selective Epitaxy and Ion Implantation

This work focused on the development of a monolithic optoelectronic transmitter based on an area selective epitaxial growth of GaAlAs/GaAs laser heterosructures and using established selective ion-implantation techniques in S.I. GaAs for the on-chip electronics.

2.2.1 Planar Implanted GaAs Devices and Integrated Circuits

High-speed GaAs devices such as MESFETs and Gunn devices based on planar, selective ion implantation into S.I. GaAs substrates offer key advantages over similar devices based on mesa-etched, implanted or epitaxially grown channels. These include (1) greater control, reproducibility and flexibility, (2) higher performance by eliminating the deleterious effects of a grown interface, and (3) its capability for integration into complex circuits. Selectively implanted MESFETs and resistors using Se and Si are well established techniques in GaAs monolithic microwave integrated circuits (MMIC) and digital IC technologies. Figure 2.1 describes schematically the type of microelectronic circuit structure realized from planar processing. For Gunn devices, very little work has been done up to now on planar implanted structures. Sulfur implanted/diffused Gunn devices with higher current drop ratios at lower carrier concentration-channel thickness products than epitaxial counterparts were reported.[12] Sulfur as an n-type dopant diffuses rather easily, and a combination implant/diffusion was used in that work to achieve the necessary depths of ~ 1 μm although the doping profile was very broad. The use of diffusion techniques, particularly for integrated electronic devices, is undesirable due to poor control, reproducibility, as well as temperature processing constraints. For purely implanted Gunn devices, higher implant energy and multiple-ionized species can be used to achieve the deep channel depths.[18]

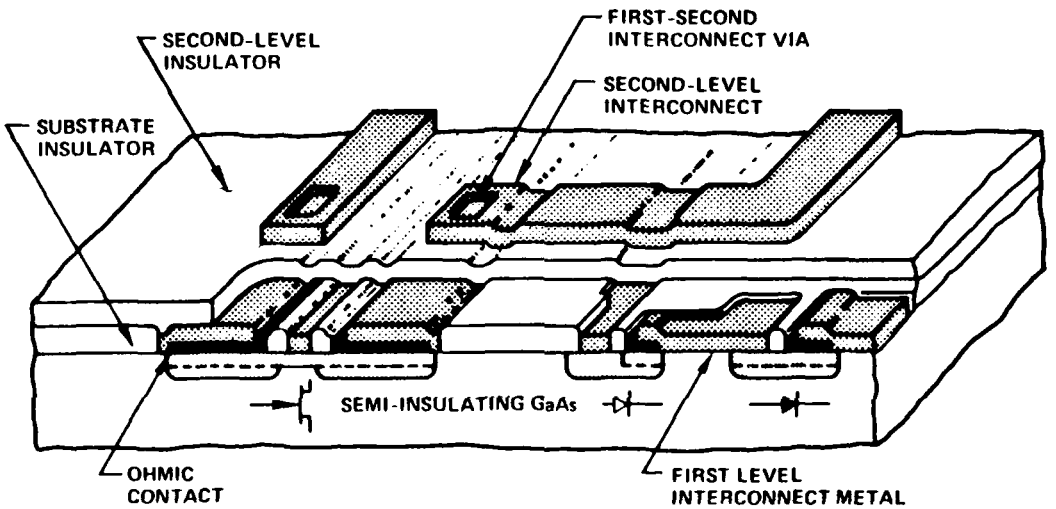


Fig. 2.1 Schematic diagram of planar ion-implanted GaAs IC structure.

2.2.2 Selective GaAlAs/GaAs Optical Device Epitaxy

The use of planar, implanted electronic devices for integrated optoelectronics requires a process compatible optical device epitaxy and fabrication. Area selective epitaxy and surface planarity are required for integration with fine-line lithography. The approach chosen in this work, as shown in Fig. 2.2, was to use a dielectric mask to delineate selective growth areas on the GaAs S.I. substrate[19] and epitaxial growth in an etched well or groove to achieve an effective surface planarity.

The optical device epitaxial technique chosen for growing standard GaAsAs/GaAs double heterostructure lasers was MOCVD.[20-22] This growth technique affords greater uniformity, control, and reproducibility compared to liquid-phase epitaxy (LPE), most commonly used today for laser fabrication of discrete and simple integrated transmitter devices. The use of MOCVD epitaxy is particularly important for the processing of large-area GaAs IC substrates (presently up to 3-inch wafers).

In delineating selective growth areas, the silicon nitride/silicon oxide mask simultaneously serves to cap the S.I. GaAs region which prevents surface deterioration and out-diffusion effects during the epitaxial growth. The polygrowth on the dielectric mask is removed by using a wet chemical etching technique. Although etch undercutting will result in a valley at the epitaxial-substrate boundary, the depth of ~ 2 μm is compatible with metallization step coverage. The overall result will be an area-selective epitaxy effectively planar with the S.I. substrate surface allocated for the electronic devices.

Details of this MOCVD selective epitaxy approach and its compatibility with planar implanted GaAs IC type processing for integrated optoelectronic device applications will be described in later sections.

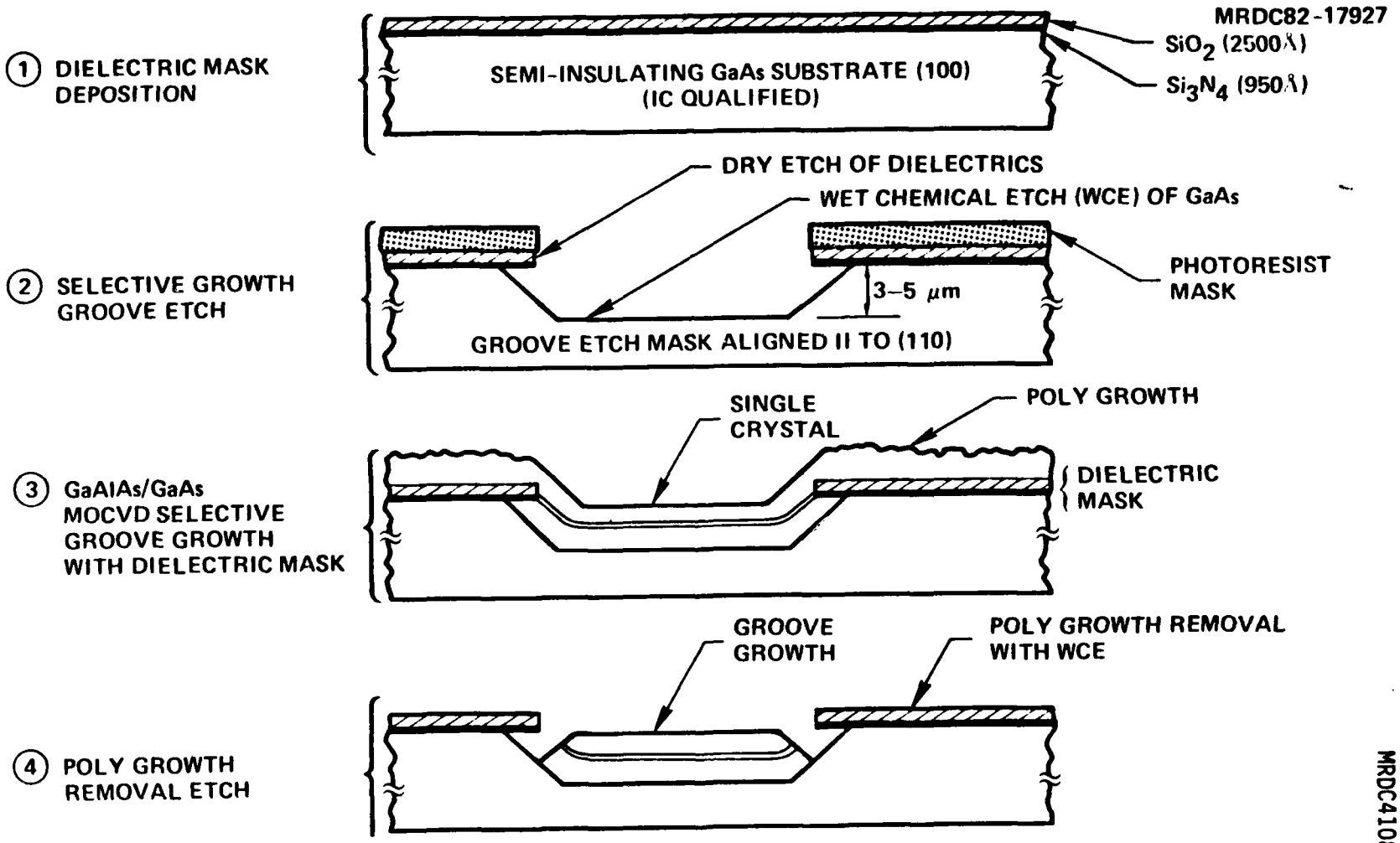


Fig. 2.2 Schematic diagram of GaAlAs/GaAs MOCVD selective groove-growth epitaxy compatible with planar GaAs IC process.

2.3 Integrated Transmitter Structure

In developing a high-speed integrated optoelectronic transmitter based on the diode laser, the need for a resonant cavity makes complex on-chip electronic circuits impossible if standard cleaved-mirror facets are used. Other integrable laser structures with "processed" mirrors (as differentiated from standard cleaved mirrors) which in principle do not limit overall chip dimensions and, thus, the ultimate chip complexity, include etched mirror lasers,[23] micro-cleaved lasers,[24] distributed Bragg reflector, and distributed feedback lasers.[25] Of these approaches, the etched-mirror lasers appear to be the most suitable for more near-term monolithic integrated transmitter applications. However, the threshold current of etched-mirror lasers are typically 1.3 to 1.5 that of cleaved lasers, and efficiencies are ~ 18% compared to 36% for cleaved counterparts.[23] The other integrable laser structures are inherently more complicated to process and fabricate and have low yield.

In this program, the integrated transmitter development focused on a standard cleaved-mirror laser structure in view of the immature technology of non-cleaved mirrors. The choice of the cleaved laser structure basically limits the complexity of the laser driver electronics through the chip dimensions (< 300 μm). Multi-gigabit laser drivers compatible with such cleaved mirror dimensions can be a MESFET, which functions as a high-speed current switch or a simple Gunn diode/resistor circuit which has the advantage of generating by itself short current/voltage pulses with automatic regeneration.[26-28] These properties of Gunn devices, also referred to as transferred-electron devices (TEDs), facilitate a variety of high speed logic operations to be carried out in one device, resulting in a considerable simplification of the circuit design compared to circuits with only bipolar or FET transistors. Figure 2.3 illustrates three simple drivers for a low threshold GaAlAs/GaAs laser. Figure 2.3a shows a TELD connected in series with the laser. When the gate of the TELD is pulsed, the driver moves from the quiescent operating point (1) to operating point (2). The laser which is biased above threshold

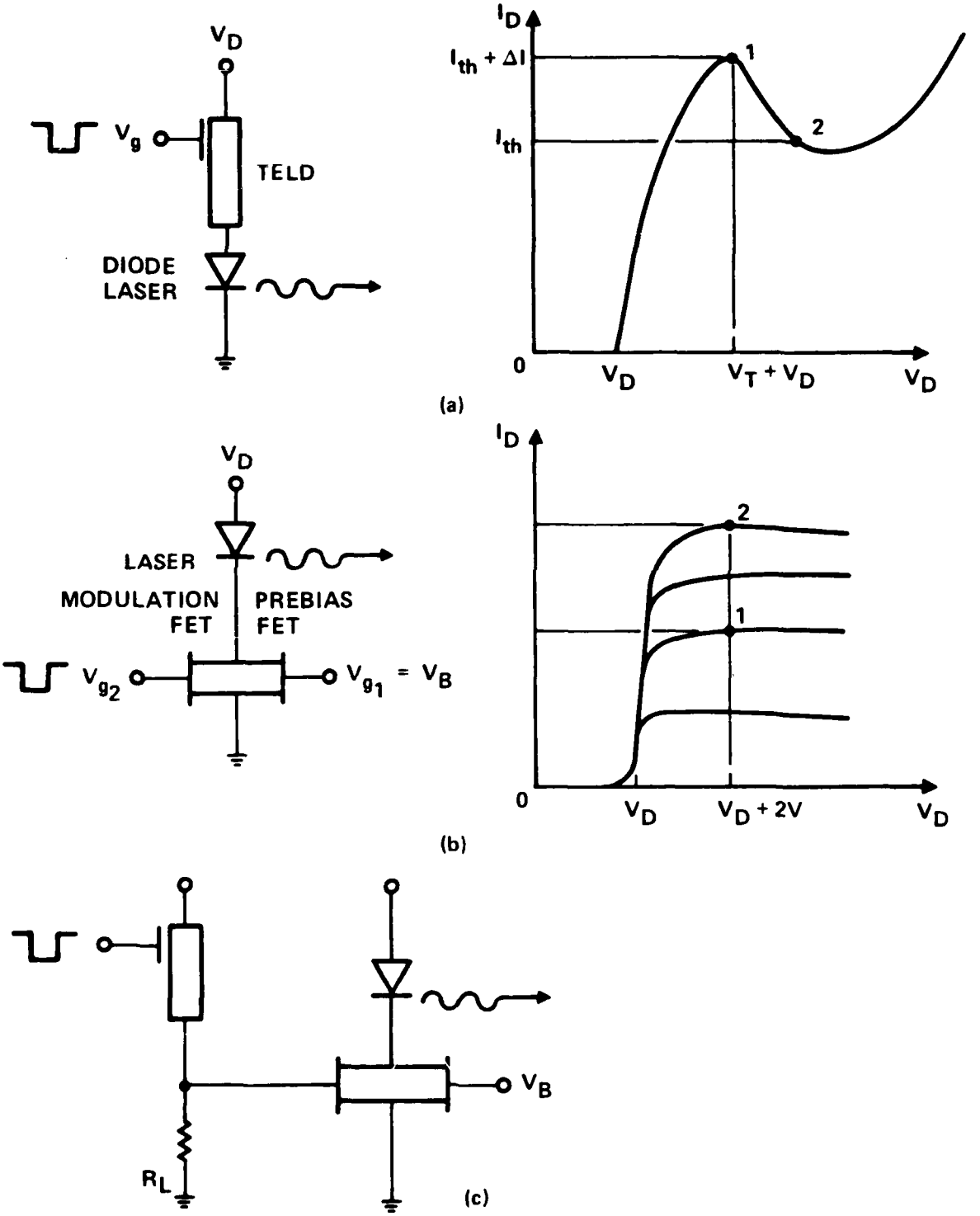


Fig. 2.3 Optoelectronic transmitter circuit configurations.

at (1) is turned off by this change in bias point. Thus, the laser produces a zero pulse for a negative going gate pulse. The duration of the pulse is the transit time of the Gunn domain in the device. The transmitter in Fig. 2.3b and Fig. 2.3c can be operated in either a positive or negative logic configuration depending on whether the drive FET is a depletion or an enhancement mode device. The logic pulse is applied directly to the FET gate, and no discrimination is used. In Fig. 2.3c, the pulse must be large enough to trigger a domain in the TELD. The design of elements for these transmitters depends upon the characteristics of the laser. Although the FET and Gunn devices require different electronic channel properties, the choice a FET/Gunn/resistor driver for integration with a cleaved laser structure serves as an important basis for developing future, advanced integrated transmitters utilizing either completely FET circuits or a combination of FET and Gunn logic devices.

3.0 INTEGRATED TRANSMITTER DESIGN

The integrated transmitter design is described in this section. It consists of a laser diode, with standard cleaved mirrors and an electronic driver composed of a laser prebias and modulation MESFETs, a Gunn device with a trigger gate (transferred-electron logic device or TELD), and a resistor. The complexity of the laser driver design was primarily constrained by the limited dimensions of a cleaved mirror laser (~ 300 μm wide cavity length). However, this transmitter design is particularly suitable for multi-gigabit operation due to its circuit simplicity and has the key elements which would serve as the building block for more sophisticated future designs.

In this section, the design criteria of circuit elements determining the overall optical transmitter performance and fabrication structure is discussed, a device fabrication structure based on the circuit design developed, device processing steps formulated, and a corresponding mask set generated for the actual lithographic fabrication of the transmitter design.

3.1 Circuit Design and Circuit Elements

The detailed circuit configuration for the integrated optoelectronic transmitter is shown in Fig. 3.1. In the circuit, depletion-mode MESFETs, presently well developed for GaAs, serve to prebias the diode laser above threshold for higher speed operation and perform signal switching or modulation function. The TELD is a simple high-speed negative current pulser which in conjunction with a load resistor provides negative voltage pulses to drive the gate of the modulation FET. Data can be generated by operating the TELD below threshold and using a trigger gate to activate the signal pulse. The input data is assumed to have a return-to-zero (RZ) pulse-code-modulated (PCM) format, with negative voltage pulses representing binary "ones." A negative voltage pulse causes the formation of a propagating domain in the TELD, with a reduction in current from V_{TELD} to ground. This results in a reduction in the negative potential across R_L, which drives the gate of the modulation FET.

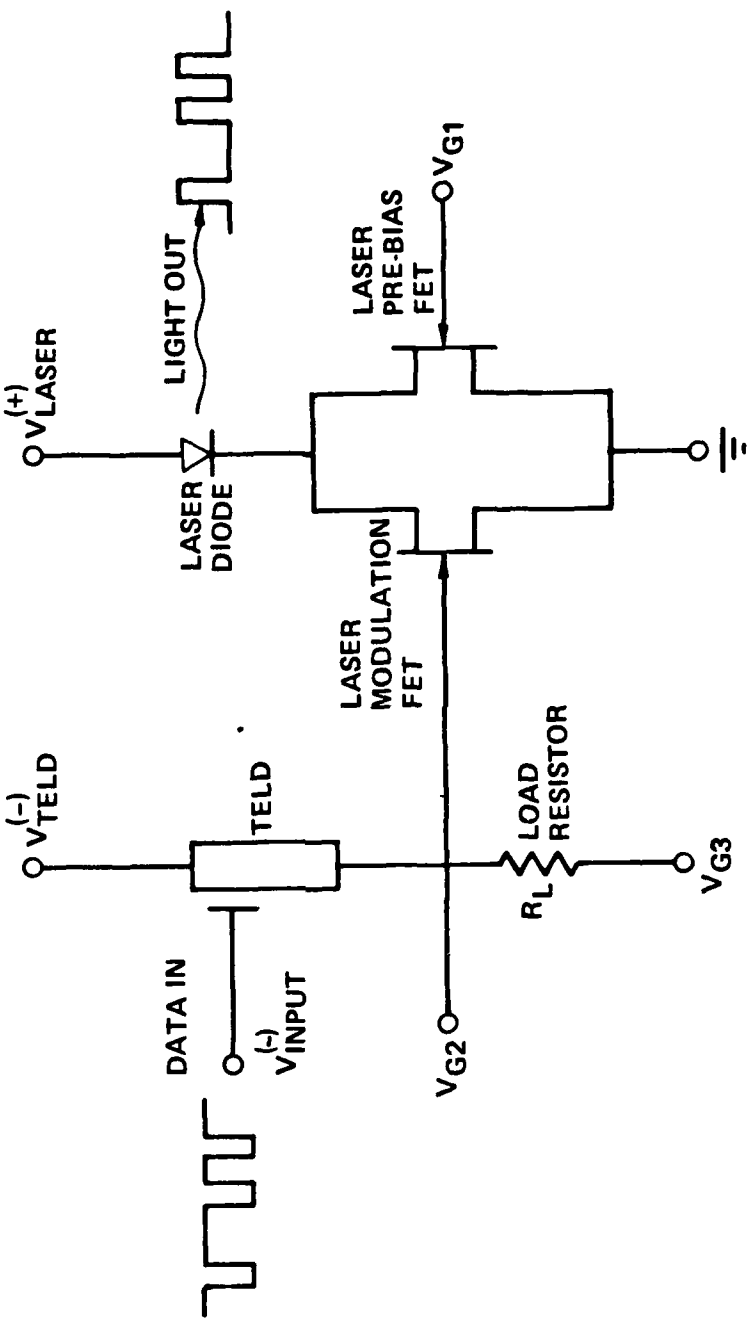


Fig. 3.1 Integrated optical transmitter circuit configuration.

The FET switches from "off" to "on," with a corresponding increase in current through the laser diode. This causes the generation of an optical output pulse, in response to the input data pulse.

3.1.1 Diode Laser

The GaAlAs/GaAs double-heterojunction (DH) injection or diode laser will be the basis for any near-term high-speed integrated optical transmitter. These lasers have demonstrated high performance, long life, and potential for integration with I.C. technology based on GaAs. Important laser performance characteristics which affect the design of the laser drive electronics include threshold current (power dissipation), the dependence of threshold current on temperature, the high-speed response, and the differential quantum efficiency of the particular laser structure.

A simple stripe-geometry GaAlAs/GaAs laser shown schematically in Fig. 3.2 serves to address key design issues. The device consists of four layers grown on a GaAs substrate. The first three layers which alternate between GaAlAs and GaAs define an optical waveguide which confines the optical energy to the central GaAs region due to the lower index refraction of the GaAlAs confining layers. The GaAlAs layers also serve another purpose. The n-type GaAlAs layer, because of its higher energy gap, serves as a carrier reflection barrier that tends to confine carriers injected into the active region near the junction. Similarly, the p-type GaAlAs barrier layer serves as a wide bandgap emitter which suppresses electron injection back into the p-type GaAlAs. This has the effect of causing all current flow to be dominated by the injection of holes into the n-type GaAs active region. The use of this structure has resulted in the extremely low threshold current densities of present GaAs lasers. Figure 3.3 shows the dependence of the threshold current density upon the active layer thickness, d.[29] Note that the threshold current density has a minimum value at an active layer thickness of approximately 700 to 800 Å. The data points shown on the figure represents the best values obtained by three different materials technologies for the various device

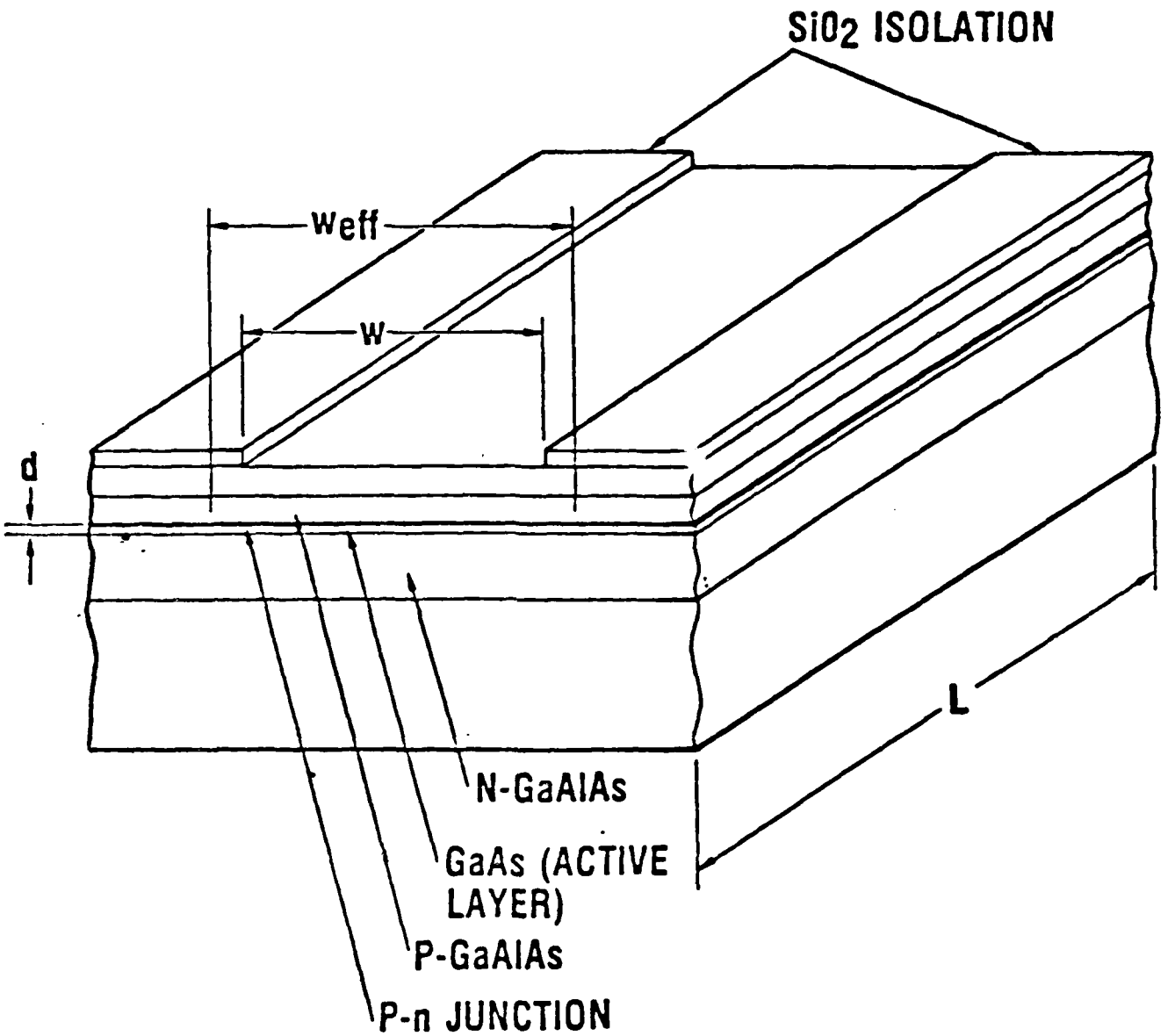


Fig. 3.2 Schematic diagram of a simple stripe geometry GaAs/GaAs laser.

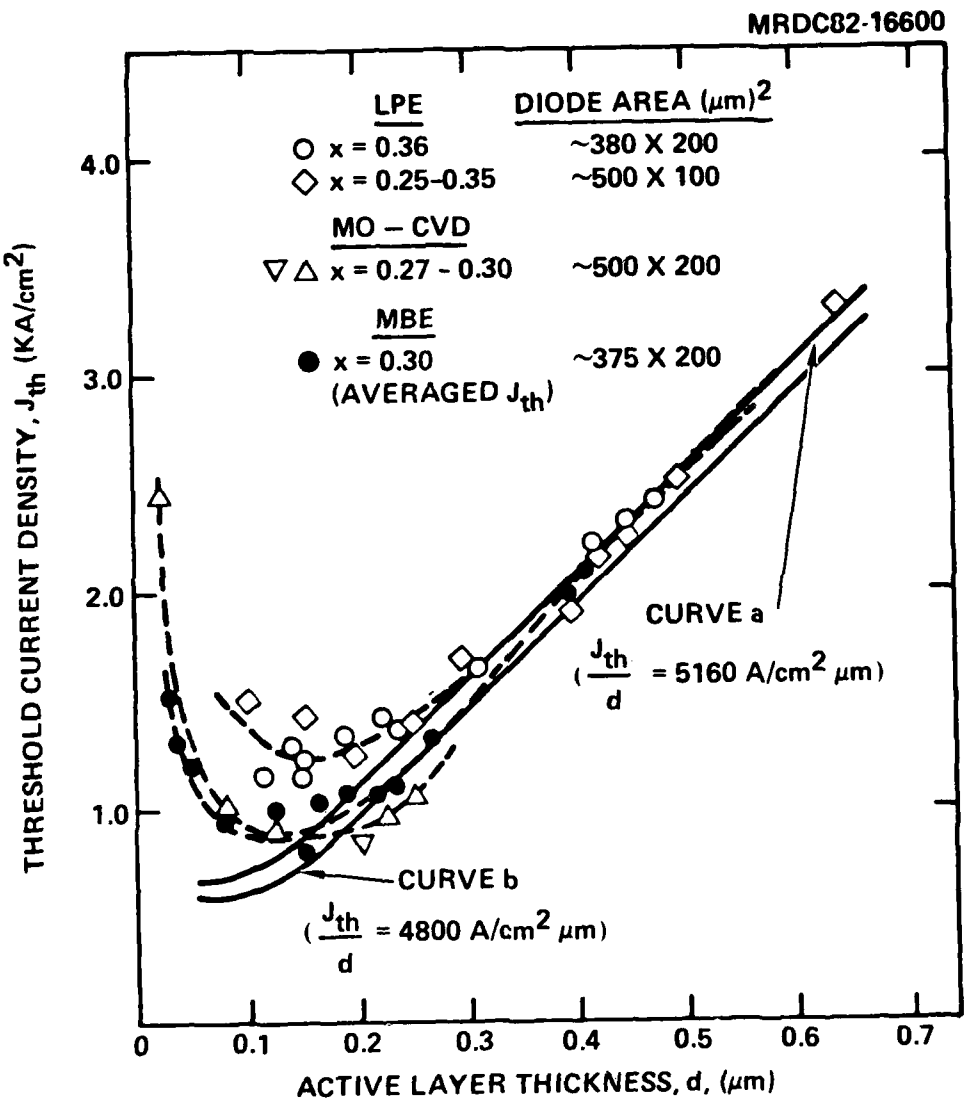


Fig. 3.3 Diode laser threshold current density dependence upon the active layer thickness.

parameters. There is generally good agreement between the experimental results and the theoretical calculations.

Current Threshold

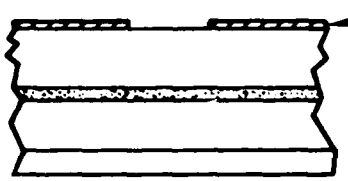
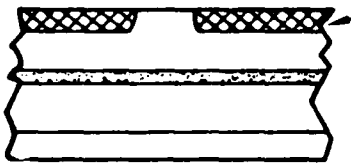
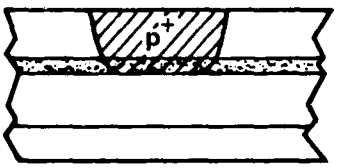
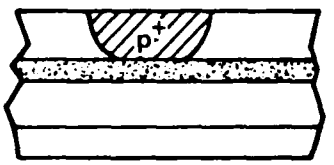
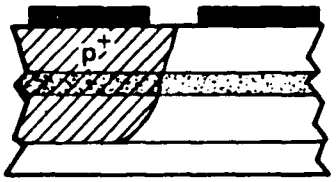
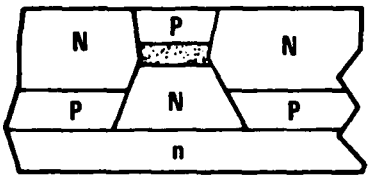
To achieve low threshold current devices, structures must be devised which maximize the confinement of the optical wave parallel to the junction and limit the total area of current flow. Several techniques to achieve this are shown schematically in Fig. 3.4.[22,30-44] Structures in which the current is confined by an oxide or by proton bombardment typically result in confinement of the optical wave owing to a variation of gain across the active region and are called gain-guided lasers. By comparison, device structures which utilize a change in the effective index of refraction across the active portion of the device are called index-guided or mode-controlled structures. A special case is the transverse junction stripe (TJS) laser which relies on index guiding to confine the wave in a direction parallel to the junction but upon gain guiding to control the mode in the direction perpendicular to the junction. Figure 3.4 also shows the lowest threshold current that has been obtained using each of the structures for nominal 200 to 300 μm long cavities.

Temperature Dependence of Threshold

Over the temperature range 0°C to 70°C, most double heterostructure lasers are dependent upon temperature as given in the following equation:

$$J_{th} = J_{th} \exp(T/T_0) \quad . \tag{3.1}$$

This empirically derived equation indicates that the threshold current can be a very strong varying quantity with temperature depending upon the value of T_0. T_0 in turn depends upon various device and technology related parameters. However, the best and average values of T_0 for each of the device structures are listed in Fig. 3.4. In each case, the most common T_0 value for

CROSS SECTION SCHEMATIC	STRUCTURE	I_{th} (mA)	T_o (K)	n_{ext}	f_{max} (GHz)	REF
	OXIDE STRIPE	70-100	140-170	40-50	1-2	30, 31
	PROTON BOMBARDED STRIPE	30-100	140-170	40-70	1-2	32
	DEEP DIFFUSED STRIPE	70-100	120	40-80	5	33,34
	NARROW DIFFUSED BIPOLAR STRIPE	30-50	170	80-90	2-3	22
	TRANSVERSE JUNCTION STRIPE	20-30	120	50	2-8	35-37
	BURIED HETERO-STRUCTURE	10-30	120-170	80-90	1-3	38-44

P(N) – p(n) - TYPE GaAlAs
p(n) – p(n) - TYPE GaAs

ACTIVE REGION
DIFFUSED P^+ REGION

Fig. 3.4 Diode laser structures and device characteristics.

a double heterostructure laser independent of the lateral guiding mechanism is 150K to 180K. On the other hand, both the TJS device structure and the deep diffused device structure have T_0s in the range of 120K. This results from parallel current leakage in the GaAlAs regions of the diffused junction's structure. It appears to be fundamental to the device structures and is a distinct disadvantage of these two devices.

Frequency Dependence

Semiconductor laser operation involves nonlinear interaction between the injected carrier density and the emitted photon population that strongly affects the frequency dependence of the device. Interaction between the photons in a laser mode and the active carrier density are governed by the following rate equations:[45,46]

$$\frac{dn}{dt} = \frac{J}{ed} - \frac{n}{\tau_{sp}} - g\,Sn^{\ell}$$

$$\frac{dS}{dt} = -\frac{S}{\tau_p} + \alpha V\frac{n}{\tau_{sp}} + Vg\,Sn^{\ell} \qquad (3.2)$$

where n(S) is the electron (photon) population; $\tau_{sp}(\tau_p)$ is the electron (photon) lifetime; g is the gain coefficient; V is the volume; and α is the fraction of spontaneous recombination emitted into the lasing mode.

These coupled nonlinear differential equations describe the simplest case of a uniform carrier and photon distribution in the semiconductor active region. Recent studies have shown that the effects of strong variations of either of these quantities within the active region can play a major role in modifying the frequency dependence of injection lasers. However, to describe the general characteristics of semiconductor lasers, we assume the uniform

excitation case. To determine the frequency dependence of a semiconductor laser, we consider small signal modulation by a sinusoidally varying current.

Figure 3.5 shows the dependence of the modulation efficiency as a function of frequency for several different values of the dc current.[34] Several features are worthy of note. Below threshold, the frequency dependance shows a falloff above a critical frequency, $f_c[f_c = (1/2\pi)(\tau_{sp}\tau_p)^{-1/2}]$. Above threshold, there is a marked resonance in the modulation efficiency whose frequency increases with the drive current above threshold. The peak frequency of this resonance is given by the following equation:[46]

$$f_r = \frac{1}{2\pi}\left[\frac{1}{\tau_{sp}\tau_p}\left(\frac{J}{J_{th}} - 1\right)\right]^{1/2} = f_c\left(\frac{J}{J_{th}} - 1\right)^{1/2} . \qquad (3.3)$$

Typical values for τ_{sp} and τ_p are 5 ns and 2 ps, respectively. This leads to a value for the characteristic frequency of $f_c \approx 1.5$ GHz. Thus, for operation at very high frequencies, biasing of the device well above threshold is required. On the other hand, higher frequency operation can also be achieved by reduction of the carrier lifetime or the photon lifetime. However, this usually results in an increase of the threshold current density. For example, a decrease by a factor of four in the photon lifetime or carrier lifetime results in a factor of two increase in f_c. On the other hand, these decreases will result in an increase of laser threshold and a decrease in differential quantum efficiency.

Several factors affect the height of the resonance including carrier diffusion,[47,48] nonuniform photon distribution,[47] and coupling between the carrier population and the spontaneously emitted photons in a particular mode.[46,49] However, for our purpose, it is important to note that the maximum frequency is determined to some extent by the drive conditions of the device and also by the device structure. Figure 3.5 also shows the best results

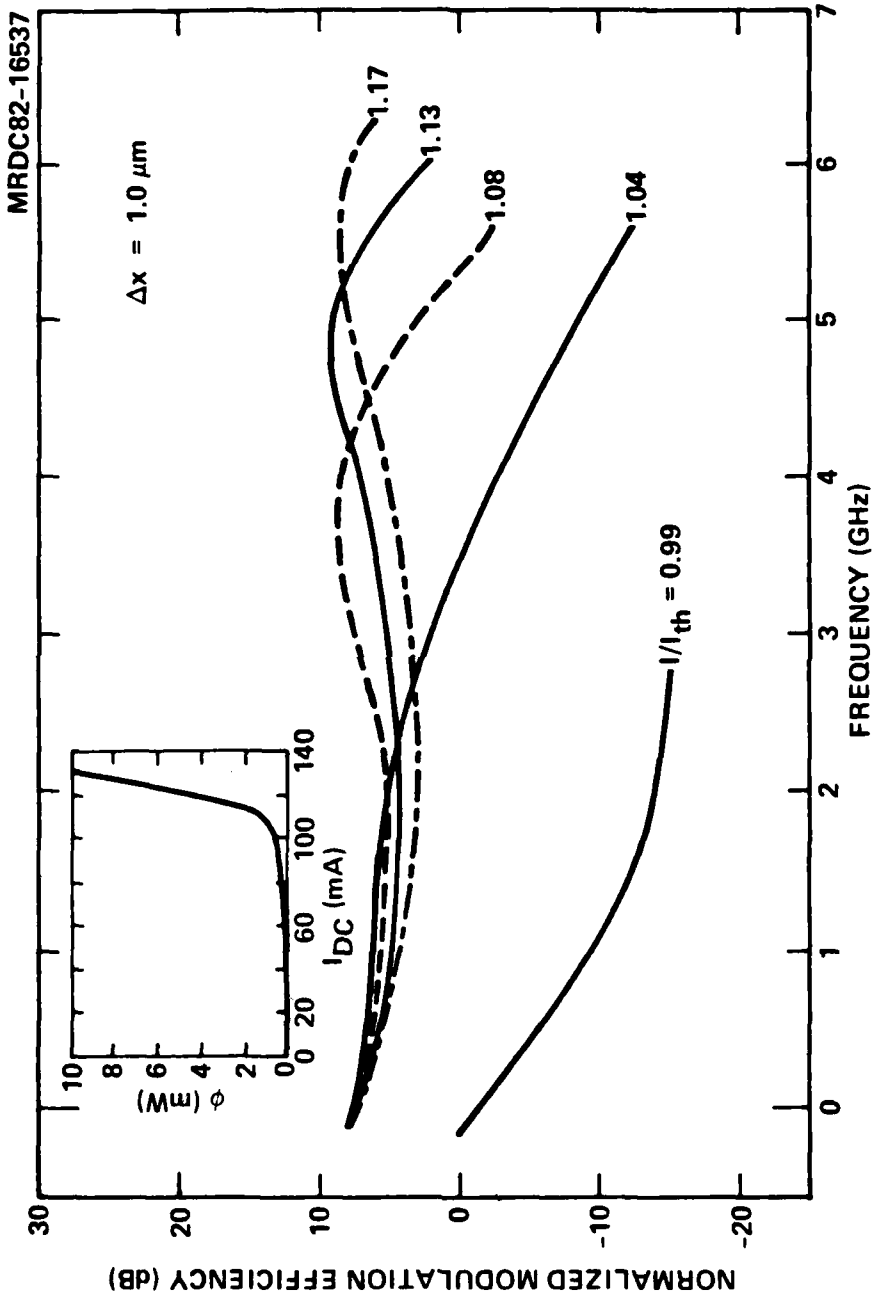


Fig. 3.5 Diode laser modulation characteristics.

obtained to date for the maximum frequency of operation, i.e., resonance frequency for each of the device structures.

The resonance peak exhibited in Fig. 3.5 also has a pronounced effect on the pulse response of these devices. The devices typically exhibit pronounced ringing at the onset of the turnoff of pulsed operation due to this resonance phenomenon. The frequency of the ringing is equal to the resonance frequency. These relaxation oscillations can contribute a significant pattern effect when attempting to pulse code modulate laser devices at high frequencies. Several schemes have been devised to mimimize such pattern effects. Adequate information is now available to reduce this to a manageable problem.

Differential Quantum Efficiency

The differential quantum efficiency of an injection laser is an important parameter for most applications. In the case of high-speed pulse code modulation, the differential quantum efficiency and the bias dependence of the frequency response determines the average power required to achieve modulation at some given frequency. The laser will usually be biased near threshold to some quiescent operating point and then modulated with a current pulse above this operating point. The average current drive then is determined by these operating parameters and the system sensitivity. For most optical link applications, the emitted power need not be more than 1 mW. However, it must be higher than the quiescent operating power to minimize the system sensitivity to noise. The differential quantum efficiency of various device structures is dependent upon the reflectivity of the laser mirrors and the internal losses of the device. The following equation gives an expression for the external quantum efficiency in terms of the internal quantum efficiency:[50]

$$\eta_{ext} = \eta_{int} \left[\frac{\frac{1}{2L} \ell n\left(\frac{1}{R}\right)}{\frac{1}{2L} \ell n\left(\frac{1}{R}\right) + \alpha} \right] \qquad (3.4)$$

where L is the device length, R is the mirror reflectivity, α the loss coefficient and n_{int} the internal quantum efficiency. Device structures which minimize the coupling of the optical wave with the active region of the device typically have very high differential quantum efficiencies owing to reduced free-carrier absorption losses. These structures can usually be obtained with very thin active regions and structures which are weakly confined in the lateral direction. However, the reduced coupling between the optical wave and the excited carrier density decreases the rate of stimulated emission and thus increases the threshold current. Figure 3.4 shows the highest differential quantum efficiency obtained with various device structures as well as the differential quantum efficiency observed at the lowest threshold current. In many cases, they are the same value. Clearly, differential quantum efficiency in the range from 40 to 90% can be obtained. The output power required for any particular application is usually determined more by the need to achieve low threshold or a certain speed of response.

Summary

A wide range of device structures exists which yield low laser thresholds, high speeds of response, and high differential quantum efficiencies. To permit laser operation at GHz frequencies as high as 4 GHz or higher, it will be necessay to monolithically integrate the laser with the drive circuitry. This monolithic integration is a key factor in determining which device structure is actually chosen.

3.1.2 TELD

The TELD, because of its inherent capability of generating short, high speed pulses may be important for use in the electronic driver of the optical transmitter. A TELD is a three-terminal Gunn or TED device, with an anode, a cathode, and a trigger electrode usually positioned near the cathode, as illustrated in Fig. 3.6. The active region is an n-type epitaxial or ion-implanted layer fabricated on an semi-insulating GaAs substrate. Operation of

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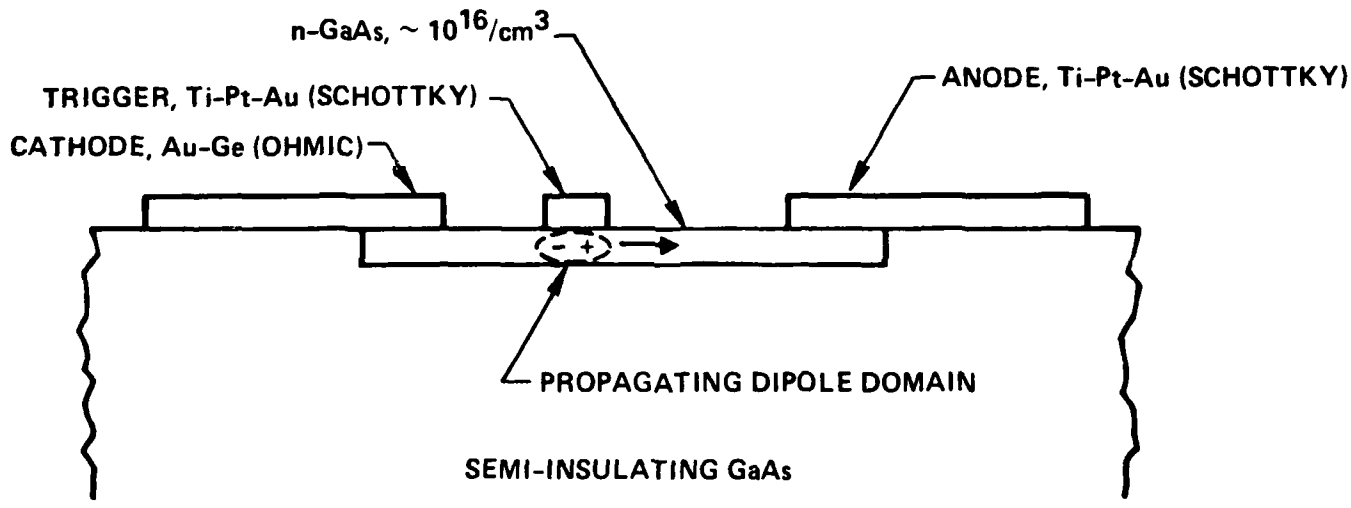

Fig. 3.6 Schematic diagram of a TELD.

the TELD is based on the negative differential mobility of GaAs resulting from the transfer of conduction band electrons from states of low effective mass to states of higher effective mass under the influence of a high electric field. The low effective mass states which predominate at low fields are associated with the conduction band energy minimum (Γ-point) at the center of the Brillouin zone, while the high effective mass states are associated with higher energy satelite minima (X-point) in the zone. Since the phenomenon depends upon the transfer of electrons from one conduction-band minimum to another, devices based on this effect are known as transferred electron devices (TEDs).

When a TED is biased above a certain threshold voltage V_t, dipole charge domains begin to form at the cathode and propagate to the anode, where current pulses appear. Only one propagating domain is present at any given time, and when one domain is extracted the next one forms at the cathode. The formation of a propagating domain results in a reduction in current through the device, while the current increases after a domain is extracted. As a result, the device acts as an oscillator, with fundamental frequency, f_o, given by $f_o = 1/\tau$, where τ is the transit time for a domain. In GaAs, the propagation velocity for a domain is close to 1.0×10^7 cm/s, so $f_o \approx 10^7/d$, where d is the anode-cathode separation.

A TELD is a TED with a Schottky barrier trigger electrode positioned between the anode and cathode. Under normal bias conditions, the electric field near the cathode is too small for domain formation. A negative voltage pulse applied to the trigger electrode causes an increase in depletion layer thickness in the region underneath the electrode, leading to an increase in the electric field near the cathode to a level above threshold for domain formation. The domain propagates from cathode to anode, and the current through the TELD is reduced for a period of time equal to the domain transit time. The response of the TELD to a negative trigger voltage pulse is therefore a negative current pulse of duration equal to the domain transit time.

The anode-to-cathode separation for the device is determined by the desired duration for the current pulses. For a transmitter designed for operation at a bit rate, B, the current pulse duration τ_p should satisfy

$$\tau_p < 1/B \quad . \tag{3.5}$$

In this example, we choose B = 4 Gb/s, so τ_p < 250 ps. To provide 50 ps margins for turn on and turn off of the TED, the design assumes a value of $\tau_p \sim 150$ ps. Since

$$d = 10^7 \tau_p \text{ (cm)} \quad , \tag{3.6}$$

with τ_p in seconds, then, in this case d = 15 μm. The threshold voltage can be calculated from

$$V_t = E_t d \quad , \tag{3.7}$$

where E_t is the threshold electric field. With E_t = 3300 V/cm in GaAs,[51] then V_t = 5 volts.

The doping level and dimensions of the active region affect the formation and stability of dipole domains and determine amplitude of the current pulses as well as the average (dc) power dissipation. It has been determined from studies of planar TED oscillators that, to ensure full domain formation and propagation, the product of carrier concentration n and length d of the active region should satisfy the relation[52]

$$nd > 10^{13} \text{ cm}^{-2} \tag{3.8}$$

while the product of n and the thickness t of the active layer should satisfy[53]

$$nt > 10^{12} \text{ cm}^{-2} \quad . \tag{3.9}$$

The influence of the dimension of the active layer on the series resistance R_S of the device is given by the relation

$$R_S = \frac{L}{e\mu nwt} \tag{3.10}$$

where e is the electronic charge (1.6×10^{-19} C), μ is the carrier mobility, t is the layer thickness, and w is the channel width. The dc current for bias near the threshold is then given by

$$I_t = \frac{e\mu ntwV_t}{d} = e\mu ntwE_t \quad . \tag{3.11}$$

Substituting numerical values into this equation, $E_t \approx 3300$ V/cm for GaAs and $\mu \sim 6700$ cm^2/V-s (typical for high-quality n-type channels in GaAs gives

$$I_t = 3.5 \times 10^{-12}\ ntw \quad . \tag{3.12}$$

For ion-implanted TELDs, typical design values would be $n \sim 5 \times 10^{16}$ cm^{-3}, $t \sim 8 \times 10^{-5}$ cm, and $w \sim 5 \times 10^{-3}$ cm, so that $I_t \sim 70$ mA and relationships (3.8) and (3.9) are satisfied. Assuming a conservative 30% drop in current when a domain is formed, the change in current is $\Delta I_{TELD} \sim 20$ mA. A series load resistance of 50-100 Ω would provide a useful FET gate modulation voltage of 1-2 volts. Power dissipation for the TELD and related circuit would be 500 mW to 1 W.

The choice of electrode materials is dictated by the desire to obtain stable operation under dc-biased conditions. The normal procedure would be to use ohmic electrodes for both anode and cathode, but experience with TED devices has shown that better dc-bias performance is obtained with a Schottky barrier node, due to hole injection at the node.[54] Thus, it is expected that best performance for the photodetector will be obtained with an ohmic contact,

such as Au-Ge, at the cathode and a Schottky barrier contact, such as Ti-Pt-Au, for the anode and the trigger electrodes.

3.1.3 MESFET

The MESFET is also a three-terminal device, but unlike the TED it has a dependence of output current on input voltage which is approximately linear over a fairly wide operating range.[55] The three terminals are designated source, gate, and drain, as indicated in Fig. 3.7. In GaAs, the electrodes are fabricated in a thin n-type layer, with ohmic contacts for source and drain and a Schottky barrier for the gate. When a bias voltage is applied between source and drain, a current flows through the n-type layer. The source-to-gate bias controls the source-to-drain current by regulating the thickness of the depletion layer under the Schottky gate electrode. No current flows in the depletion layer, so that increasing the negative gate bias decreases the drain current. The current is completely shut off for a negative gate voltage large enough to completely deplete the layer under the gate. This voltage is known as the "pinch off" voltage, V_{po}. For zero applied gate voltage, the region under the gate is partially depleted due to the Schottky barrier potential. The "built in" potential responsible for the depletion, V_{bi}, equals -0.8 V in GaAs. This depletion region disappears for a positive gate voltage of 0.8 V, in which case the source-to-drain current reaches its maximum, or saturated, level I_{sat}. This important parameter of the GaAs FET is given by

$$I_{sat} = nev_s wt \quad , \tag{3.13}$$

where n is the carrier concentration in the active layer, e is the electronic charge, v_s is the electron saturation velocity, w is the gate width, and t is the active layer thickness. The drain current is given in terms of the applied voltage by

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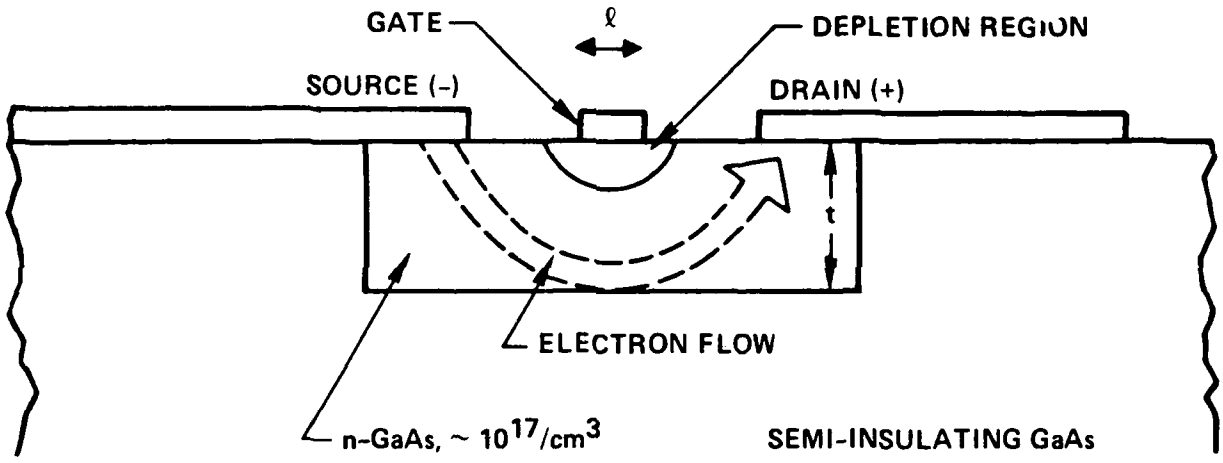


Fig. 3.7 Schematic diagram of a MESFET.

$$I_d = I_{sat}\left[1 - \frac{V_{gs} + V_{bi}}{V_{po} + V_{bi}}\right]^{1/2} \quad , \tag{3.14}$$

with V_{po} given by

$$V_{po} = \frac{-net^2}{2\epsilon} + |V_{bi}| \quad , \tag{3.15}$$

where ϵ is the dielectric constant of the material. The transconductance g_m is given by

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = -\frac{1}{2} I_{sat}[(V_{gs} + V_{bi})(V_{po} + V_{bi})]^{-1/2} \quad . \tag{3.16}$$

Another very important parameter is the input capacitance C_{gs}, given by

$$C_{gs} = \frac{\frac{1}{4}(2ne\epsilon)^{1/2}\, \ell\, w}{(V_{gs} + V_{bi})^{1/2}} \quad , \tag{3.17}$$

where ℓ is the gate length. This capacitance determines how large the input impedance to the FET can be, consistent with a given bandwidth.

In designing the FET for high-speed operation, it is desirable to maximize the transconductance-to-capacitance ratio. In fact, it can be shown that

$$g_m/C_{gs} \approx V_{sat}/\ell \quad . \tag{3.18}$$

Thus, the gate length ℓ should be as small as possible. The choice of $\ell < 1$ μm is consistent with present lithography capability in our laboratory using standard contact printing techniques. The active layer thickness should be considerably less than the gate length to assure uniform pinch-off; a thickness range of 0.2-0.3 μm is typical of implanted MESFET channels. Other parameters consistent with present medium power FET design and fabrication capability are $n \sim 1.5 \times 10^{17}$ cm^{-3} and the gate width $W \sim 1.5 - 3 \times 10^{-2}$ cm. These values typically yield implanted FETs with modulation frequencies $f_\tau \sim$ 3-5 GHz, pinchoff voltage ~ 3 - 7 V, saturation currents of ~ 25 mA/100 μm gate width, and sheet resistance of ~ 1000 Ω/square. The FET gate modulation voltage of 1-2 V from the TELD/receiver output is sufficient to yield laser current modulation up to 30 mA or 30-40% of the anticipated laser threshold currents.

3.2 Fabrication Structure

Based on the optoelectronic transmitter circuit proposed for this work (Fig. 3.1), the chip layout is guided by design rules to facilitate circuit performance as well as device fabrication. Although various chip designs can be envisioned, the limited geometry of a cleaved mirror laser basically restricts the possible circuit layouts. The FET/TELD/resistor elements and their corresponding bonding pads must be accommodated with geometrical and size considerations to allow speed and power dissipation requirements.

In this work, the chip layout was guided by general GaAs monolithic microwave and digital IC design rules. One optimized layout design is given in Fig. 3.8. The laser modulation FET is placed adjacent to the laser structure from high-speed considerations. One-micron gate features for the FET and TELD are oriented in a common direction to minimize alignment difficulty. High power dissipation elements such as the TELD and the load resistor are adequately dispersed on the chip to minimize heating effects. A dual gate FET structure, chosen to conserve space, facilitates laser prebias

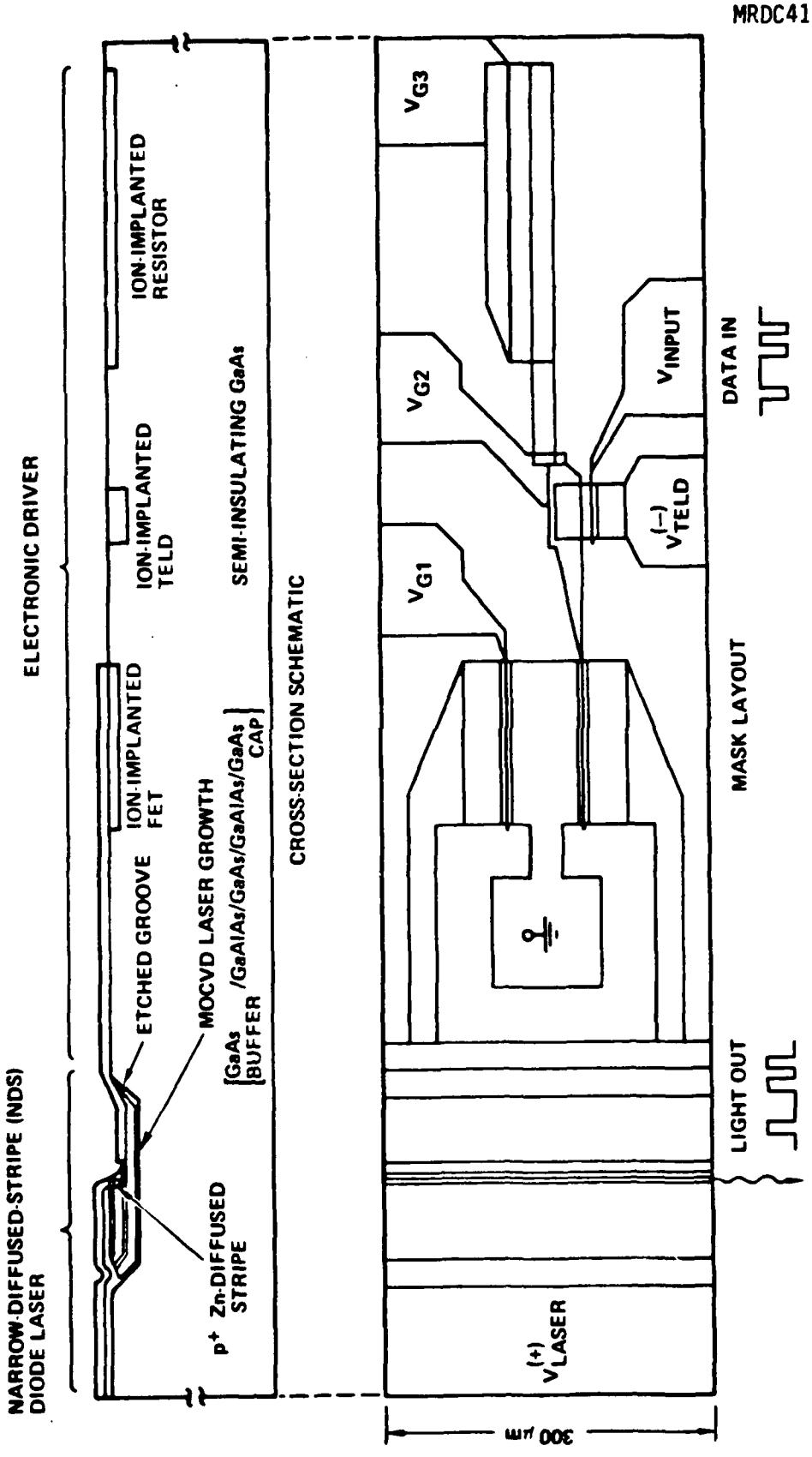


Fig. 3.8 Integrated optoelectronic transmitter/fabrication structure.

(V_{GI}) and laser modulation (gate connected to the TELD). An extra bonding pad allows bypassing of the TELD pulser for direct FET modulation of the laser. In the chip layout, although no detailed quantitative analyses of circuit interactions, parasitics or impedance matching were performed, these effects were addressed from a qualitative standpoint and guided by previous experience. The rather simple nature of the transmitter circuit would justify this approach.

The integrated transmitter design is effectively a planar fabrication structure as shown by the cross-sectional schematic of Fig. 3.8. Various laser structures can be realized in the selective groove growth region. Metallization connects the laser with the electronic driver section defined by selective ion-implantation into S.I. GaAs. The effective surface planarity facilitates device lithography using contact printing techniques.

3.3 Device Processing

In this section, the device processing steps required for the fabrication of the integrated optoelectronic transmitter are defined. The process sequence is used to generate a lithographic mask set, to be described in the following section. Figure 3.9 describes the basic integrated transmitter planar processing/fabrication steps. Steps A-C address the laser processing portion, while steps D-G describe the electronic driver processing. The key processing step which make the optical device compatible with planar implanted electronic devices is the selective epitaxy in a groove using the double dielectric (Si_3N_4/SiO_2) mask. This technique was discussed in detail in Section 2.2 and Fig. 2.2. The double dielectric is a well-established cap used in GaAs IC processing to prevent surface deterioration and out-diffusion effects during the implant activation/anneal step and serves a double purpose in this work as an epitaxial growth mask. Temperature cycling experiments with MOCVD epitaxy (750°C ~ 30 min), laser diffusion experiments (850° ~ 30 min) indicate a fairly wide margin of compatibility for laser and electronic device processing. That is, the groove growth epitaxy could be performed

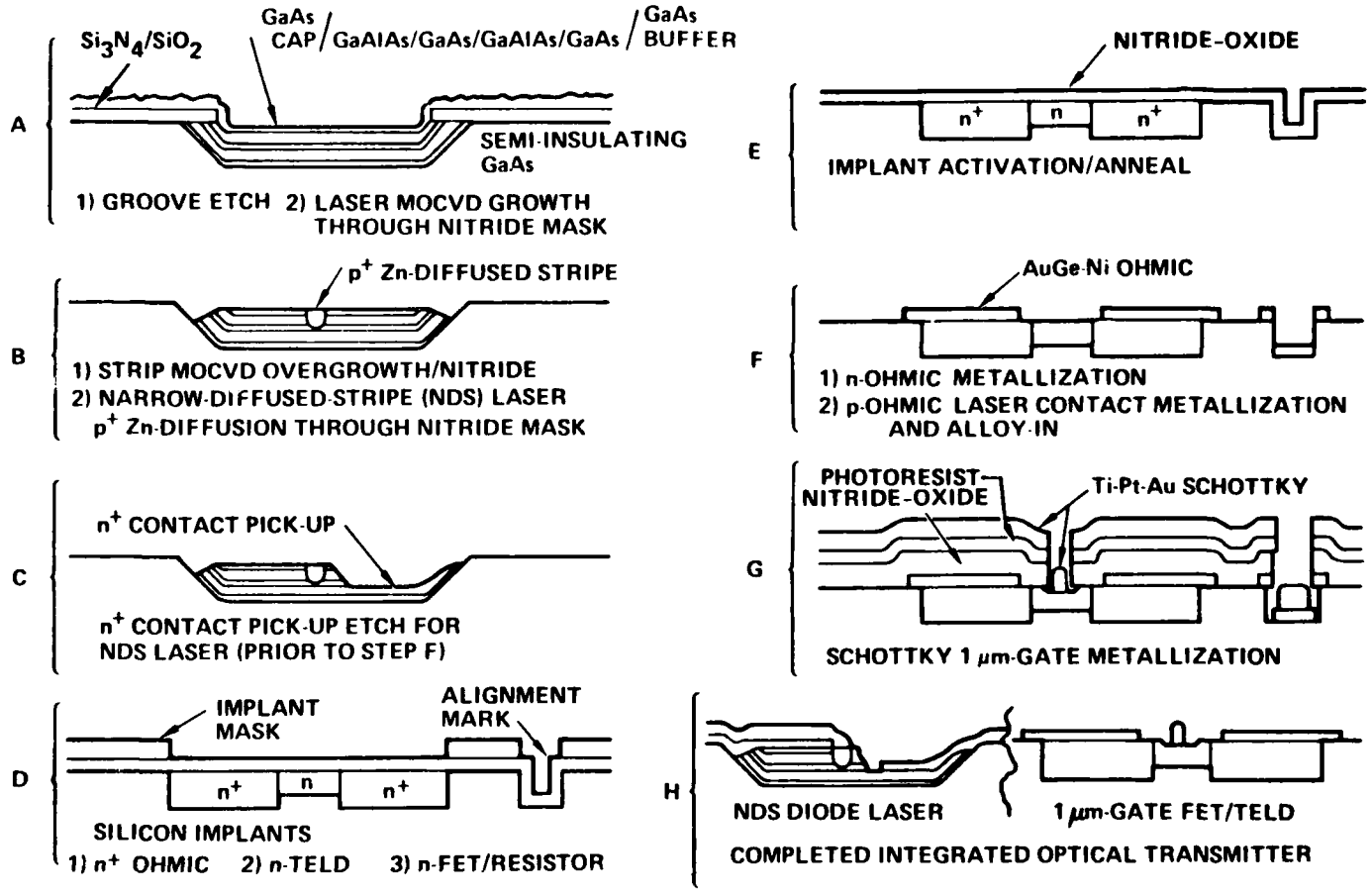


Fig. 3.9 Integrated optical transmitter planar processing/fabrication steps.

first followed by ion-implantations and activation/anneal or vice versa. The laser processing includes the transverse junction stripe and narrow-diffused stripe structures and the electronic device processing incorporates standard GaAs MMIC and digital IC techniques.

3.4 Mask Design

A mask set based on the integrated transmitter fabrication structure (Fig. 3.8) and the process steps (Fig. 3.9) is shown in Fig. 3.10. The mask set (designated IOET) has seven different variations of the basic layout design to facilitate flexibility in device development. Different device geometries accommodate various current ranges and laser modulation speeds. Designs 1, 3, 4, 6, and 7 use an FET to facilitate laser prebiasing current up to 100 mA (for typical medium-power microwave FET implants). Designs 2 and 5 facilitate off-chip resistor prebiasing which in principle do not limit the laser prebias level. The laser current modulation is determined by the modulation FET, TELD and resistor geometries. The channel widths for the FETs are nominally 150 μm to 400 μm and 50-75 μm for the TELDs which correspond to laser modulation up to twice the threshold current, although modulation levels of 10-20% are more practical. A separate metallization mask layer was designed to enable trimming of the resistor value which affects the FET gate modulation amplitude. The laser modulation speed is determined by the gate/channel lengths of the FET and TELD. Two gate/channel lengths designed for the FETs in the mask set are nominally 1 μm/4 μm and 1.5 μm/5.5 μm for gigabit performance. The corresponding TELD geometries for realizing repetitive current pulse from 1-4 Gb/s include 12 μm channel lengths, with 1 μm and 1.5 μm trigger gate lengths and 1.5 μm and 2 μm cathode to gate separations. Approximately 5 mask levels are related to the selective epitaxy and laser processing while some 8 levels are related to ion-implanted device processing for the laser driver.

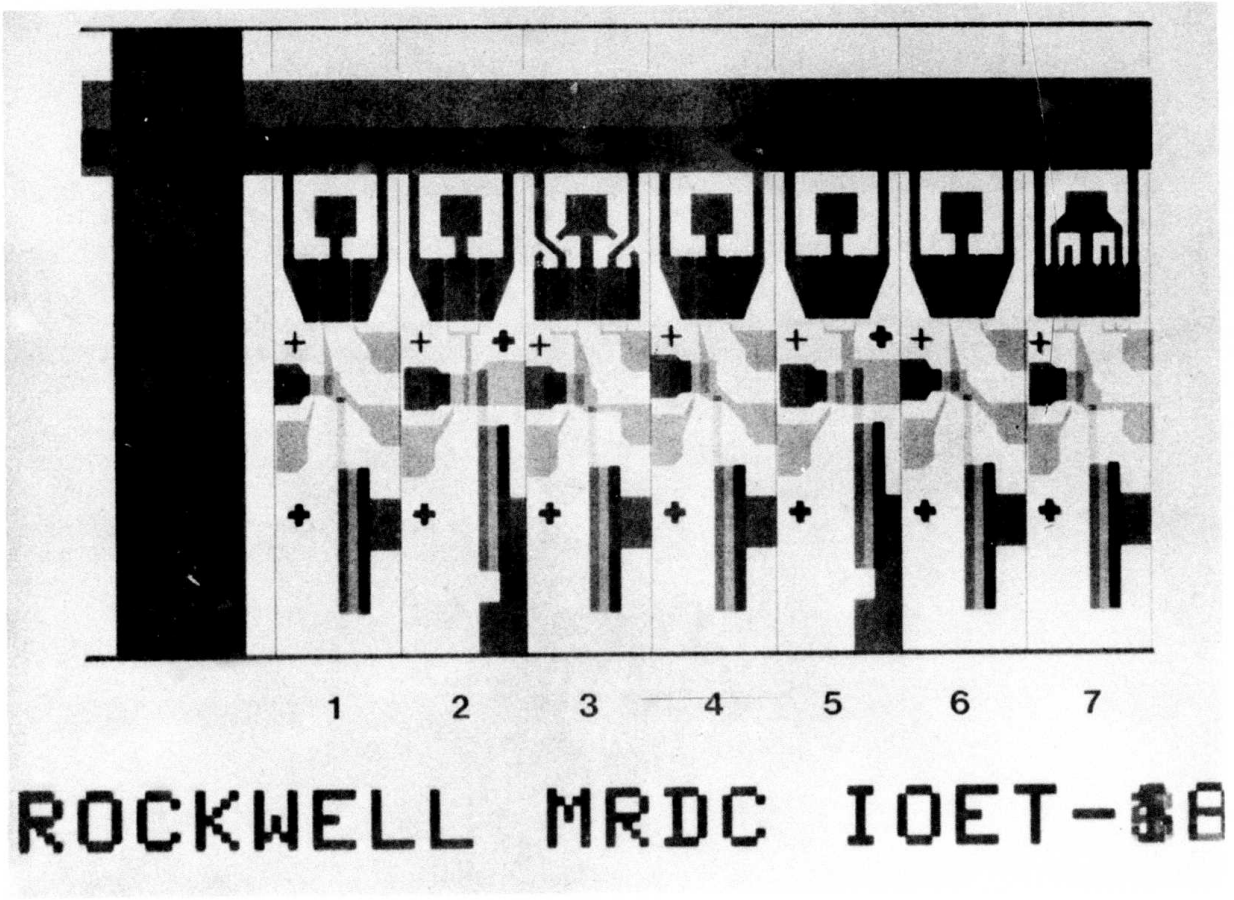


Fig. 3.10 Integrated optoelectronic transmitter mask set (IOET).

4.0 MATERIALS DEVELOPMENT

As in any semiconductor device development, the material aspects play a critical role, particularly in this work where optical device epitaxy has to be incorporated with substrates suitable for ion-implanted electronic devices. In this section GaAlAs/GaAs optical device epitaxy using the MOCVD technique and its application to selective area growths in S.I. GaAs is described. The compatibility of this selective epitaxy with planar, implanted GaAs device structures is demonstrated.

4.1 Substrate Material Requirements

The choice of the starting substrate for the integrated optoelectronic transmitter using MOCVD epitaxy and ion implanted electronics is dictated by the requirements of the electronic devices. Currently, S.I. GaAs substrates suitable for ion-implantation are the basis for high-performance discrete devices and ICs.[56,57] For the latter, a wide variety of low and high dose implants are required to fabricate components such as low noise and high-power MESFETs, Schottky diodes, varactors, switches, as well as passive elements for full circuit applications. Successful ion implantation involves recognition of the following substrate requirements:[56,57]

1. Reproducible, high-resistivity GaAs, thermally stable to permit planar processing.

2. Low background doping with respect to shallow donor and acceptor impurities.

3. Capability of producing abrupt implant carrier profiles with high electrical activation and carrier mobility for the implanted species.

4. Sufficiently high crystalline quality to avoid defect related impurity and processing problems.

5. Large and regular size slice shapes to permit high device yields and efficient device fabrication.

A set of material specifications satisfying the above criteria is defined as follows:

A. Resistivity

Following a thermal anneal at 850°C with 950 Å Si_3N_4 cap, the GaAs surface must not degrade to < 10^7 Ω/square and must retain n-type conduction.

B. Background Doping

Shallow donor and acceptor concentration must be < 5×10^{15} cm^{-3} by chemical analysis (SIMS) and have < 10^{15} cm^{-3} electrically active impurities. Compensation can be achieved with native deep centers such as EL2 or by intentional doping with deep level impurities such as chromium.

C. Ion Implant Tests

Bare surface implants with Se^+ or Si^+ must produce the following results:

1. Abrupt carrier profile which compares favorably with LSS profiles.

2. High degree of impurity activation (> 80%).

3. High degree of implanted dopant uniformity, < ± 10% in depletion voltage within implanted region.

4. Exhibit a high electron and drift mobility > 90% of theoretical mobility (after implant) and show an increase in drift mobility at the active layer-substrate interface.

D. Crystalline Perfection

The crystal must be free from major crystalline defects such as stacking faults, inclusions, precipitates, twins and low angle boundaries. Dislocation densities < 10^5 cm^{-2} are acceptable for ion implantation. For use in epitaxial growth, defect densities < 10^4 cm^{-2} are preferable.

In realizing integrated optoelectronic devices with sophisticated electronics, the need for such material specifications is critical as the circuit complexity approaches MSI and LSI levels. Semi-insulating specifications suitable for direct ion-implantation will hereafter be referred to as ICs "qualified" or "IC qualified." These substrates will have to be used for developing integrated sophistication in the associated GaAs electronics.

For the integrated transmitter work, IC qualified S.I. GaAs substrates have been procured both from commercial vendors (Caminco American, Mitsubishi-Monsanto, and Crystal Specialties) and Rockwell (in-house). These materials are grown by the liquid encapsulated Czochralski (LEC) method in both chromium-doped and undoped forms. The GaAs wafers available were 2 and 3 in. diameter wafers oriented in the <100> direction. The defect densities were typically between 1-3 × 10^4 cm^{-2} and less desirable for epitaxial growths. However, buffer layers are used to minimize the effects of the defects on the laser growth structures.

4.2 GaAlAs/GaAs MOCVD Epitaxy

The application of GaAlAs/GaAs MOCVD epitaxy for integrated optoelectronic devices have been motivated by the intrinsic advantages over traditional LPE techniques. These include (1) growth control, (2) large area uniformity, (3) reproducibility and (4) improved surface morphology.[20-22]

The MOCVD technique as applied to the growth of $Ga_{1-x}Al_xAs$ utilizes the metalorganics, trimethylgallium (TMGa), trimethylaluminmum (TMAl) and the hydride arsine (AsH_3), as starting materials. The mixtures of gases are pyrolyzed in the atmosphere of hydrogen at 700-800°C according to the following reaction.

$$(1 - x)[(CH_3)_3Ga] + x[(CH_3)_3Al] + AsH_3 \xrightarrow[\Delta]{H_2} Ga_{1-x}Al_xAs + CH_4 \uparrow \qquad (4.1)$$

The growth rate is determined by the mole fraction or partial vapor pressure of the column III metalorganic compounds. The composition, x, of the resultant epitaxial layer is determined by the relative partial pressures of the Ga and Al source compounds, and the relative incorporation rate of Ga and Al has been determined to be close to one. For doping, the most widely used p-type dopant is diethylzinc (DEZn) and for n-type doping, hydrogen selenide (H_2Se) is commonly used. The doping levels are dependent upon the vapor-phase partial pressures of the respective dopant sources.

A schematic diagram of the MOCVD reactor typically employed for the growth of AlGaAs is shown in Fig. 4.1. The metalorganics TMGa, TMAl and DEZn are liquids near room temperature with relatively high vapor pressures, and thus H_2 is used as a carrier gas to transport the source vapors into the reaction chamber. The substrates employed in the growth of devices are either Si-doped GaAs wafers with $n \sim 10^{18}$ cm^{-3} or S.I. (Cr-doped or undoped) GaAs substrates oriented in the (100) direction. The substrates are lapped and polished to a final thickness of 0.3 mm. Typical substrate area is 6 to 10 mm^2 and is usually determined by the size of commercially available substrates.

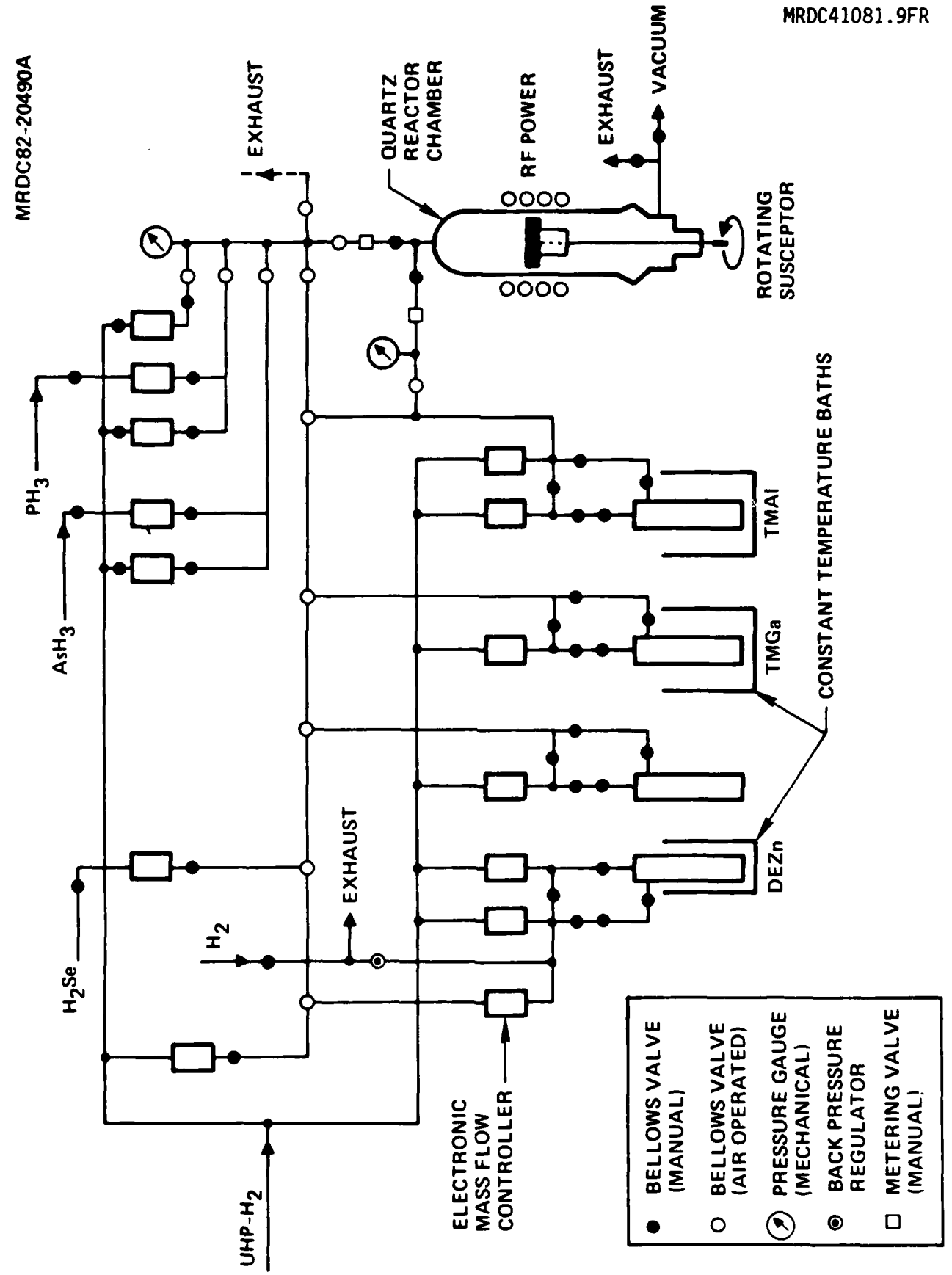


Fig. 4.1 Schematic diagram of GaAlAs/GaAs MOCVD vertical growth system.

The substrates are cleaned in standard solvents and etched in hydrochloric acid. After rinsing in deionized water, they are blown dry in N_2 and placed upon the silicon carbide-coated susceptor.

The reactor is then evacuated and backfilled with palladium diffused H_2. The susceptor is heated by an external RF coil, and the temperature is monitored by a digital infared thermometer. The AsH_3 flow is started when the suceptor temperature reaches 500°C. Calibrated electron mass flow controllers are used to ensure accurate and reproducible gas flow rates. Layer thicknesses are controlled by the timed sequencing of appropriate gas flow path valves. The growth rate typically employed are 300-3000 A/min.

One of the main advantages of MOCVD is the ease with which complicated multilayer heterostructures can be grown. This is because the gas sources can be injected or shut-off by means of very fast pneumatic valves and the growth rate and composition can be instantaneously varied by changing the current control on the electronic mass flow controllers. Our present system incorporates a microprocessor unit that controls the sequencing of the gas injection during the growth cycle. This capability to "program" the growth structure allows very complicated novel device structures to be grown. Examples of this device capability are superlattice heterostructures containing up to a few hundred layers and parabolically-graded-index heterostructure lasers.

The improved growth control, area uniformity, and reproducibility of the MOCVD technique over LPE in the growth of laser structures is uniquely inherent in the technology and stems from the following factors:

1. The composition is controlled by the reactive partial pressures of the source gases; in turn, these can be precisely controlled by electronic means.

2. The growth rate is determined by the flow rates of metal alkyls, which thus allow the growth thickness to be adjusted by

approximately one order of magnitude from 300 A/min to 3000 A/min, which result in excellent control of layer thickness down to 30 A.

3. The gases are completely mixed in the manifold and injected via a baffle at the inlet of the reactor tube, which thus ensures the homogeneity of the source material.

4. Uniform growth over large surface area is further enhanced by the use of a rotating susceptor. This serves to "average out" the remaining nonuniformity of the source material distribution above the susceptor.

The degree of material uniformity has been confirmed by various measurements. Among these are:

1. Thickness measurement of $Ga_{1-x}Al_xAs$ along a 4.3 cm bar cleaved from a DH wafer. It was found that the thickness varies by only ± 1.5% over 85% of the whole length, excluding the material around the edges of the wafer which show abnormal growth characteristics.

2. Auger electron spectroscopy in $Ga_{0.5}Al_{0.5}As$/GaAs quantum well heterostructure laser indicates that the transition width is as small as 14 A.

3. Threshold current density measured from 380 μm by 150 μm stripe lasers indicates a value of 1 kA/cm^2 with a variation of ± 2% for devices sampled over a 1 cm^2 wafer area.

4. Measurement of the composition of aluminum in the crystal, c_s vs the composition, x_v, in the vapor phase shows a unity slope with deviation of less than ± 2% over the entire range of $Ga_{1-x}Al_xAs$ investigated.

Another advantage of MOCVD is the superior morphology achieved. The layers grown on GaAs show mirror smooth morphology and are almost indistinguishable from the morphology of the substrate. This is extremely important from the device processing point of view, since irregular growth features such as terracing typically encounted with LPE presents some difficulty in lithographic work. Surface morphology along with the growth control uniformity and reproducibility of MOCVD materials are the main reasons that this growth technology has found a wide range of applications in electronic devices that require complex heterostructure growths over large areas. Examples of such devices are CCD imagers, GaAs FETs, solar cells, integrated optoelectronic transmitter and receivers.

4.3 Groove-Grown Selective Epitaxy

In this section results of the selective GaAlAs/GaAs optical device epitaxy using the MOCVD technique with the process sequence defined in Fig. 2.2 are discussed.[58] This technique yields effectively planar selective area growths compatible with planar ion-implanted electronic devices using contact lithographic techniques. The starting substrate preparation, epitaxial growth, and the selective epitaxy processing are addressed in detail.

4.3.1 Substrate Preparation

The procesing and fabrication of the integrated optoelectronic transmitter begins with preparation of the IC qualified S.I. GaAs substrate suitable for both selective MOCVD epitaxy and ion implantation. Starting wafers 2 or 3 in. in diameter are cleaved at an edge, and the orientation of the

cleavage, either <110> or <1$\bar{1}$0>, is determined from the structure of the chemically etched groove. In one direction the groove side walls etch inward, while in the perpendicular direction the groove walls etch outward. The latter is required in the selective epitaxy in the groove, since it facilitates metallization step coverage. Although the whole wafers could be processed at a time, it was more useful in this development work to cleave the wafers into smaller pieces, typically 1 in. squares.

Wafer chip processing begins with substrate cleaning followed by delineation of an implant alignment pattern using a photoresist mask and a GaAs wet chemical etch (phosphoric acid, hydrogen peroxide, and water in proportion of 1:1:10) and finally capping on both sides with silicon nitride to minimize wafer warping. The thickness of the sputtered nitride cap is determined by the implant requirements. Implantation through the nitride is preferred to keep the GaAs surface protected; however, implant energies have to be adjusted from bare implants. For implant activation/annealing, a final nitride thickness between 700-1000 Å is desired with actual thicknesses of 750 Å or 950 Å chosen for color advantages in processing. To ensure further cap integrity during the activation/anneal temperature cycle, 2500-3000 Å of sputtered or chemical vapor deposition (CVD) silicon dioxide is deposited over the nitride. This double dielectric cap also serves as a protective mask during the MOCVD overgrowth.

A selective MOCVD planar epitaxy is achieved by opening selected areas in the nitride/oxide double dielectric using dry etching techniques followed by wet etching of a groove in the GaAs substrate. Reactive ion-etching (RIE) and plasma etching are used to etch through the silicon dioxide and nitride, respectively. The groove in GaAs is wet chemical etched (WCE) using phosphoric acid (85%), hydrogen peroxide (30%), and water in 1:1:10 proportion, which yield high-quality controlled structures. Figure 4.2 shows the etched groove structures in the double dielectric and GaAs. The groove width is 200 μm wide, and the depth is between 3.5-5.25 μm deep depending on the growth structure. The dielectric overhang is observed over the groove

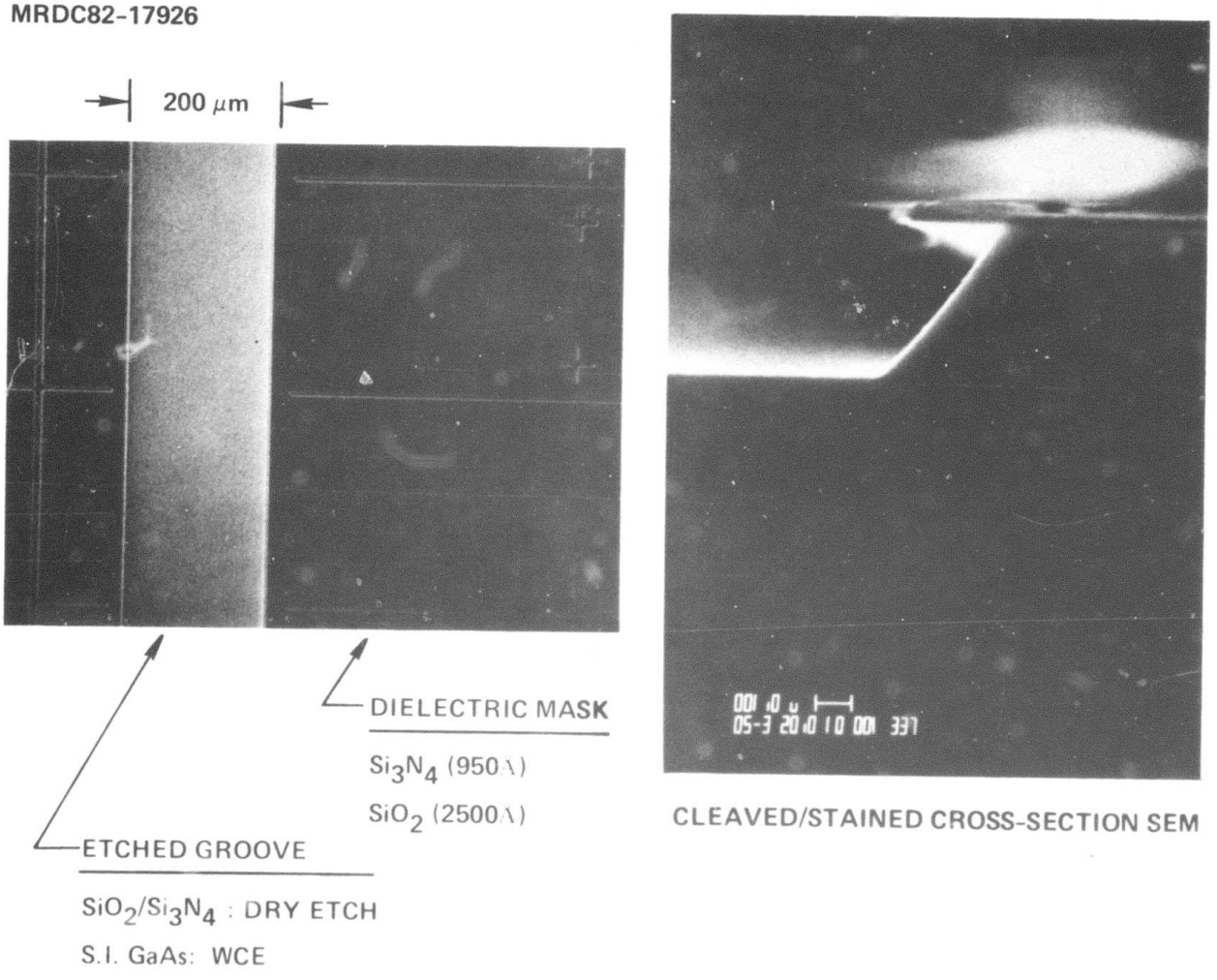


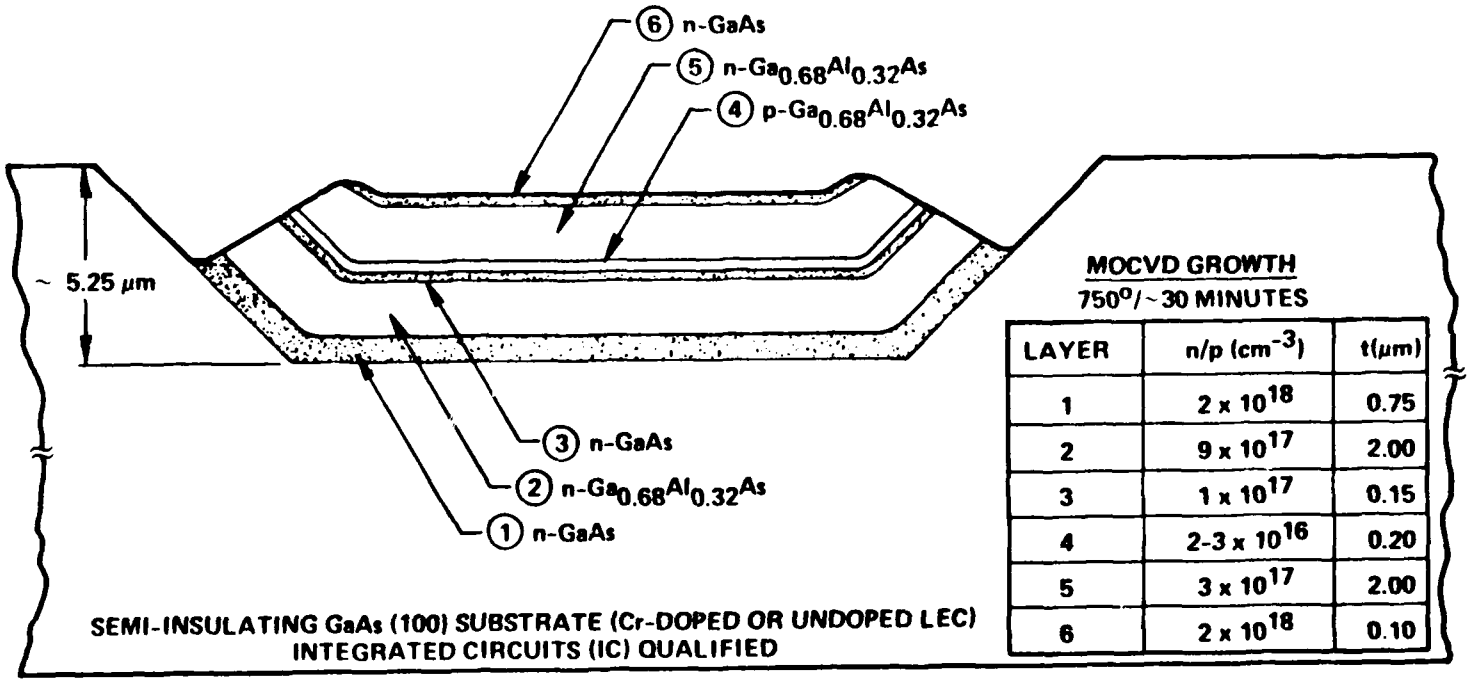
Fig. 4.2 Groove etch in S.I. GaAs with dielectric mask.

wall resulting from undercutting. The outward angle of the etched wall corresponds to aligning the groove length parallel to the <110> cleavage direction. This preferred direction allows subsequent groove growth to facilitate easier metallization step coverage over the groove edge region.

4.3.2 Epitaxial Growth

After the etched groove structure in the capped S.I. GaAs substrate has been prepared, the wafer is ready for the MOCVD optical device epitaxy as described in Section 4.2. For the integrated transmitter, standard GaAlAs/GaAs double heterostructures were used, compatible with processing TJS, narrow-diffused stripe, or oxide defined lasers. Figure 4.3 describes the nominal MOCVD growth structure used in the laser development work. The first n-GaAs layer serves as a buffer and bottom etched ohmic contact pickup, while the top GaAs facilitates p-ohmic contact formation; a good ohmic contact is difficult to achieve in GaAlAs. The laser junction is formed between n-GaAs and the p-GaAlAs with the doping configuration forcing laser emission from the n-GaAs region.

Results representative of the MOCVD GaAlAs/GaAs growth over the groove-etched GaAs substrate is shown in Fig. 4.4. Normarski phase contrast and scanning electron micrograph (SEM) photographs show the overgrowth with a single crystal region in the GaAs groove and polycrystalling growth over the dielectric mask region. The thickness of the growth is adjusted to fill the groove about 2000 Å below the surface of the masked substrate region. The SEM cross-section shows the basic characteristic of MOCVD (and molecular beam) epitaxy where growth occurs at all surfaces, unlike LPE which usually fills in grooves in a relatively planar fashion without wetting the dielectric. Of course, the tradeoff is material control, uniformity and surface morphology. Figure 4.5 compares the selective epitaxial growth structure for the growth grooves oriented in the two substrate cleavage directions. For the groove etched parallel to the ($\bar{1}10$) direction, the MOCVD overgrowth yields a groove edge structure incompatible with metallization step coverage processing.



MOCVD GROWTH
750°/~30 MINUTES

LAYER	n/p (cm^{-3})	t(μm)
1	2×10^{18}	0.75
2	9×10^{17}	2.00
3	1×10^{17}	0.15
4	$2\text{-}3 \times 10^{16}$	0.20
5	3×10^{17}	2.00
6	2×10^{18}	0.10

Fig. 4.3 Schematic diagram of GaAlAs/GaAs double heterostructure selective groove growth for narrow stripe laser application.

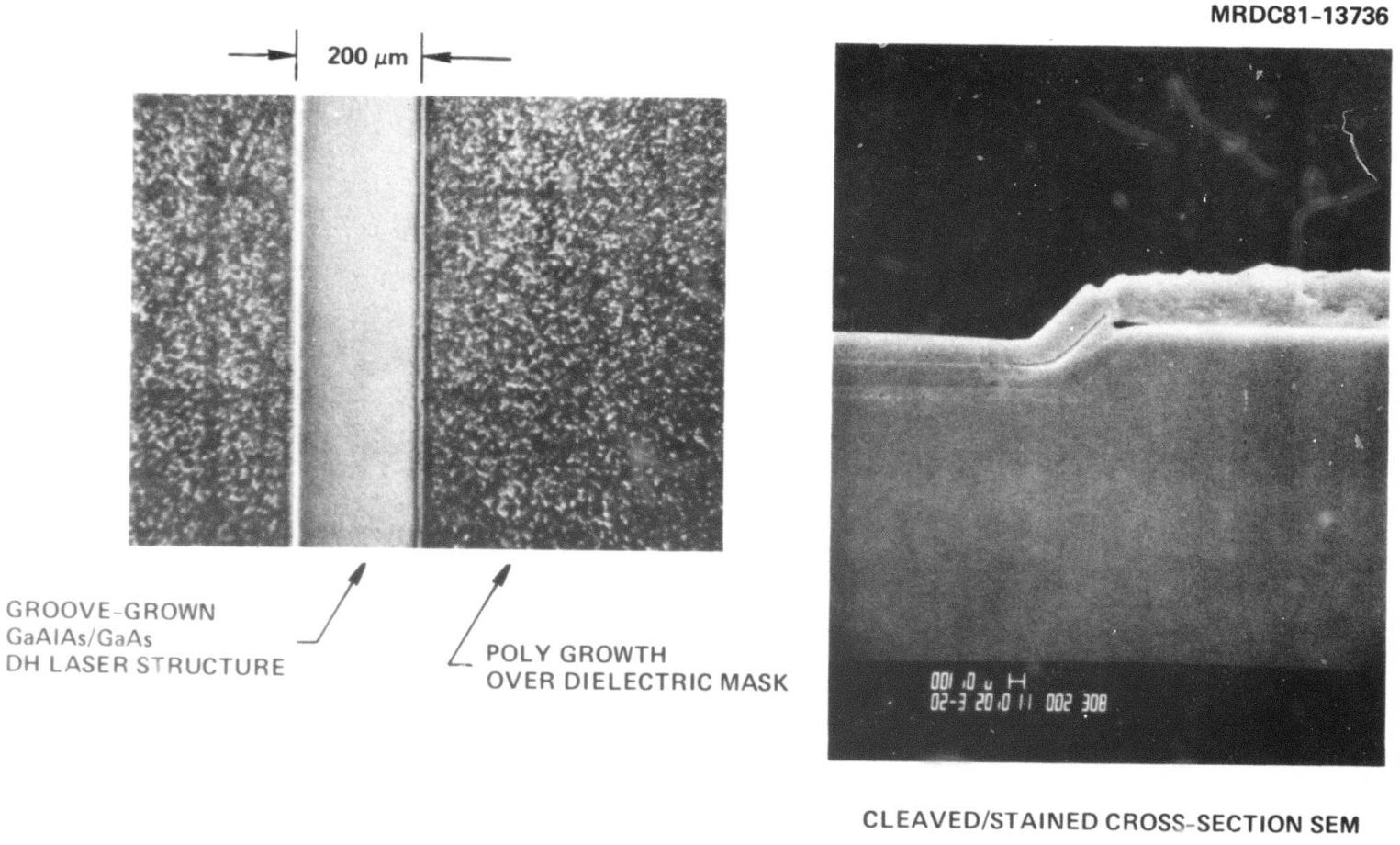


Fig. 4.4 GaAlAs/GaAs MOCVD selective groove growth with dielectric mask.

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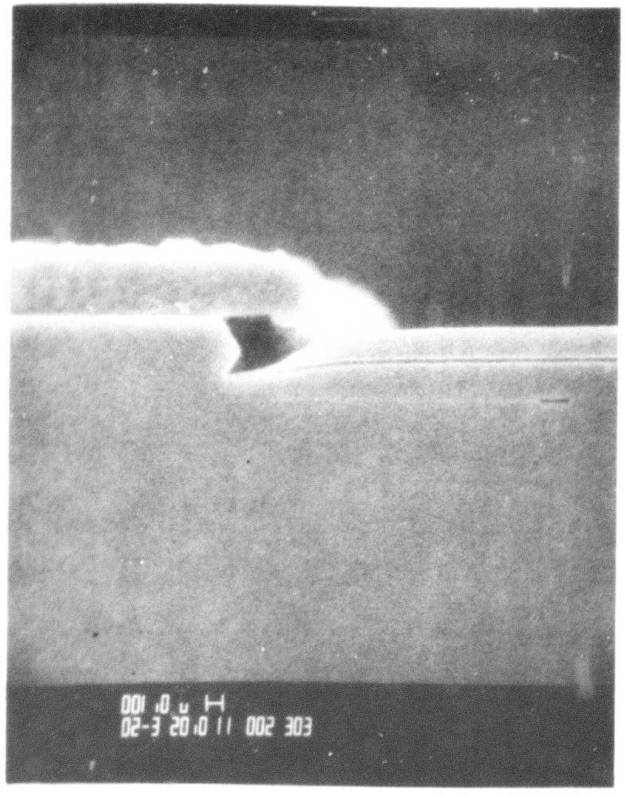
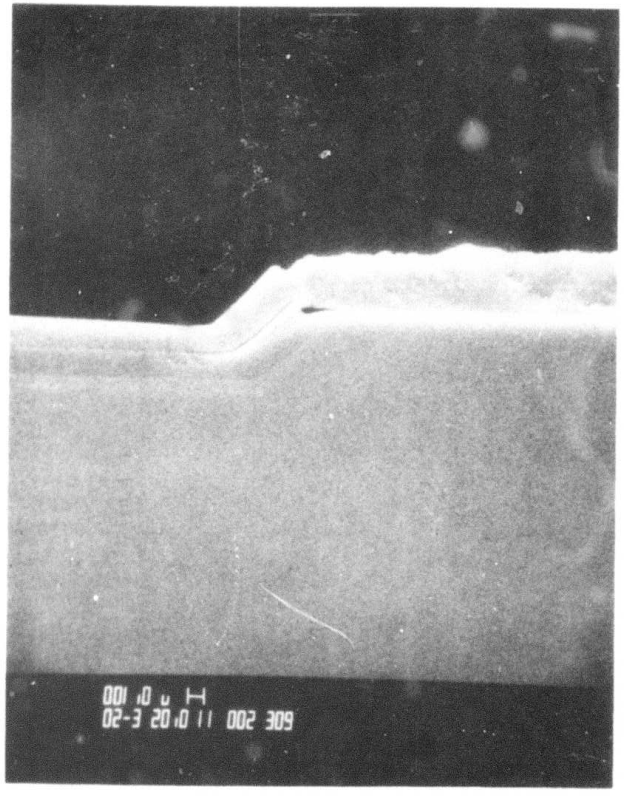


GROOVE PARALLEL TO (1$\bar{1}$0)



GROOVE PARALLEL TO (110)

Fig. 4.5 GaAs groove orientation and dielectric masked groove growth.

4.3.3 Selective Epitaxy Processing

The actual area selective epitaxy is realized by removing the polycrystalline growth over the dielectric masked areas of the S.I. GaAs substrate. This is accomplished by using a reverse photoresist mask to protect the groove growth regions and a GaAs wet chemical etch (same as used for the groove etch) to remove the polygrowth. Figure 4.6 shows the results of this polygrowth removal with the cleaved cross-section SEM revealing an etched growth structure typical of underetching even though the poly has disappeared. The valley results from etch undercutting, while the growth peaked feature is left from partial etching of the side wall growth. Increasing the polygrowth etching time can reduce such structures but at the expense of a deeper valley resulting from further undercutting, as shown in Fig. 4.7. However, such nonplanar structures at the groove edge with rounded peaks and valleys ~ 1 - 2 μm appear to be acceptable for planar electronic device processing. Improvements in the edge structure can be realized by reducing the overall thickness of the growth structure and hence the groove depth and polygrowth. The GaAlAs/GaAs MOCVD selective epitaxy groove-growth process sequence is shown in Figs. 4.8 and 4.9 using the integrated transmitter mask set. The nominal 1 in. square chips of Fig. 4.9 are typical of those processed in this work.

4.4 Selective Groove Growth and Planar GaAs Electronic Device Compatibility

The compatibility of the selective, groove-grown epitaxial processing with planar GaAs electronic devices is demonstrated by the fabrication of fine-line structures in wafers with such epitaxial growths. Figure 4.10 shows the integration of 1-μm gate laser driver structures with the laser groove-growth. The 1-μm type geometries were delineated using standard contact lithographic techniques with the IOET integrated transmitter mask set.

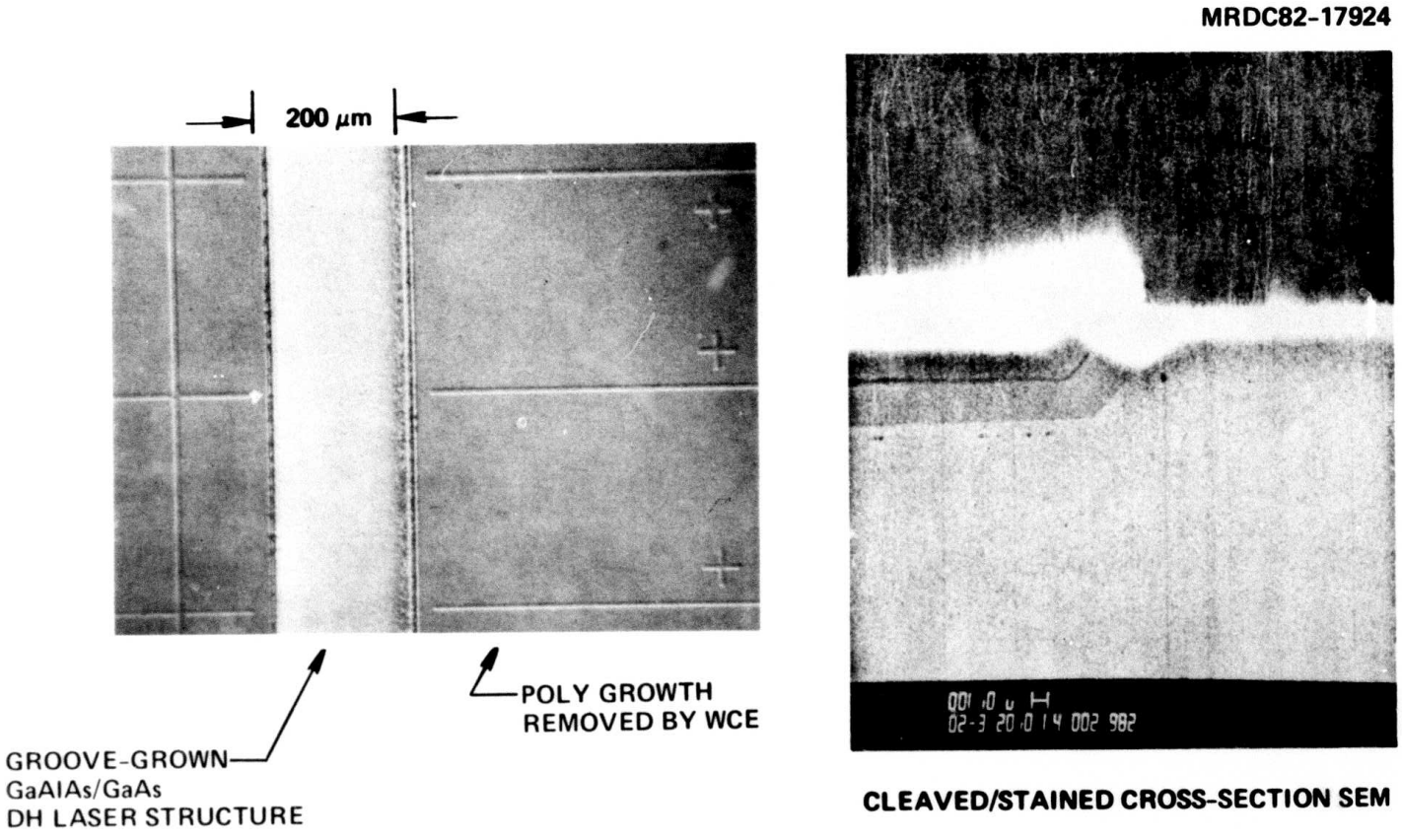


Fig. 4.6 Wet chemical etch removal of GaAlAs/GaAs polygrowth on dielectric mask.

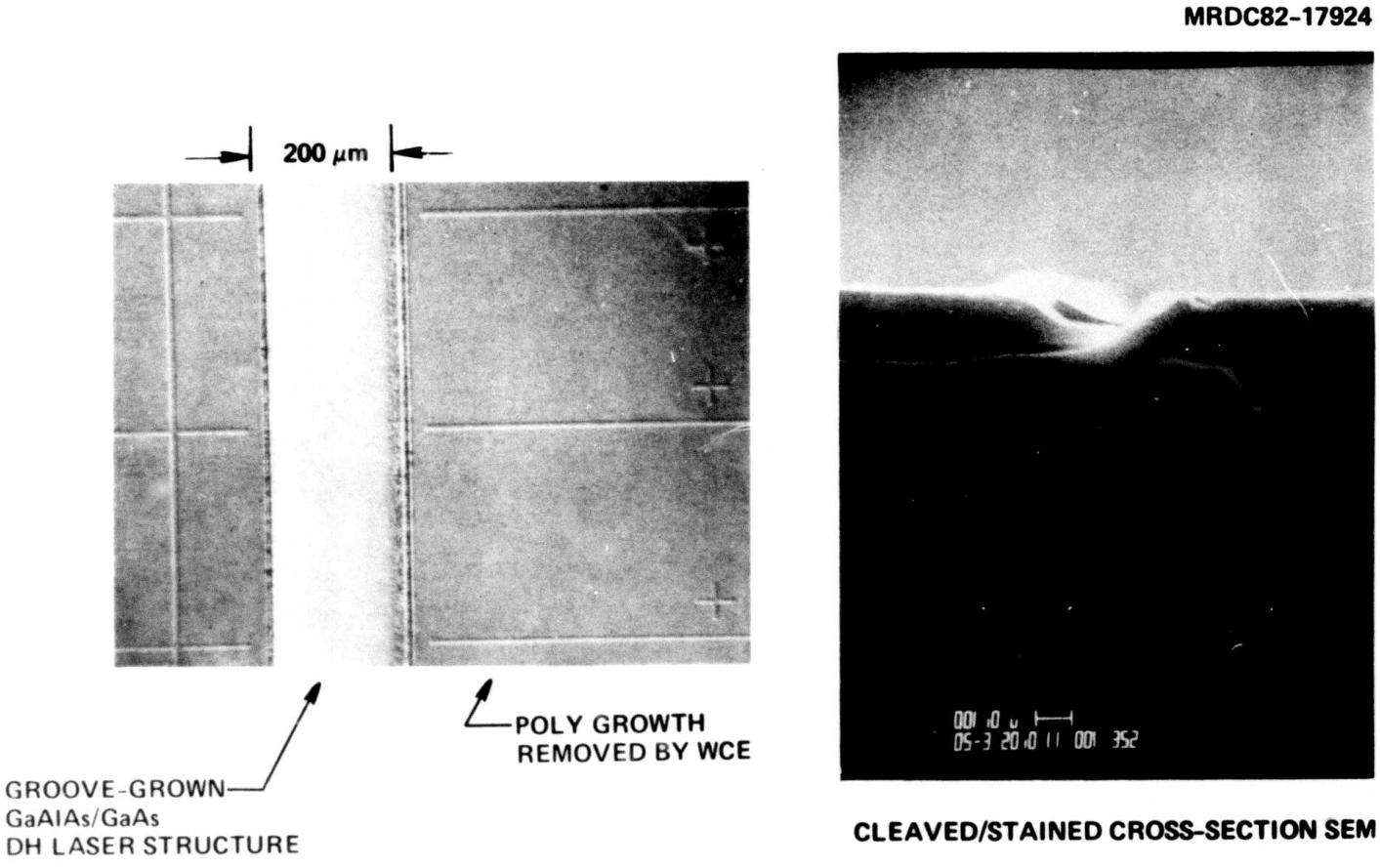


Fig. 4.7 Extended wet chemical etch removal of GaAlAs/GaAs polygrowth on dielectric mask.

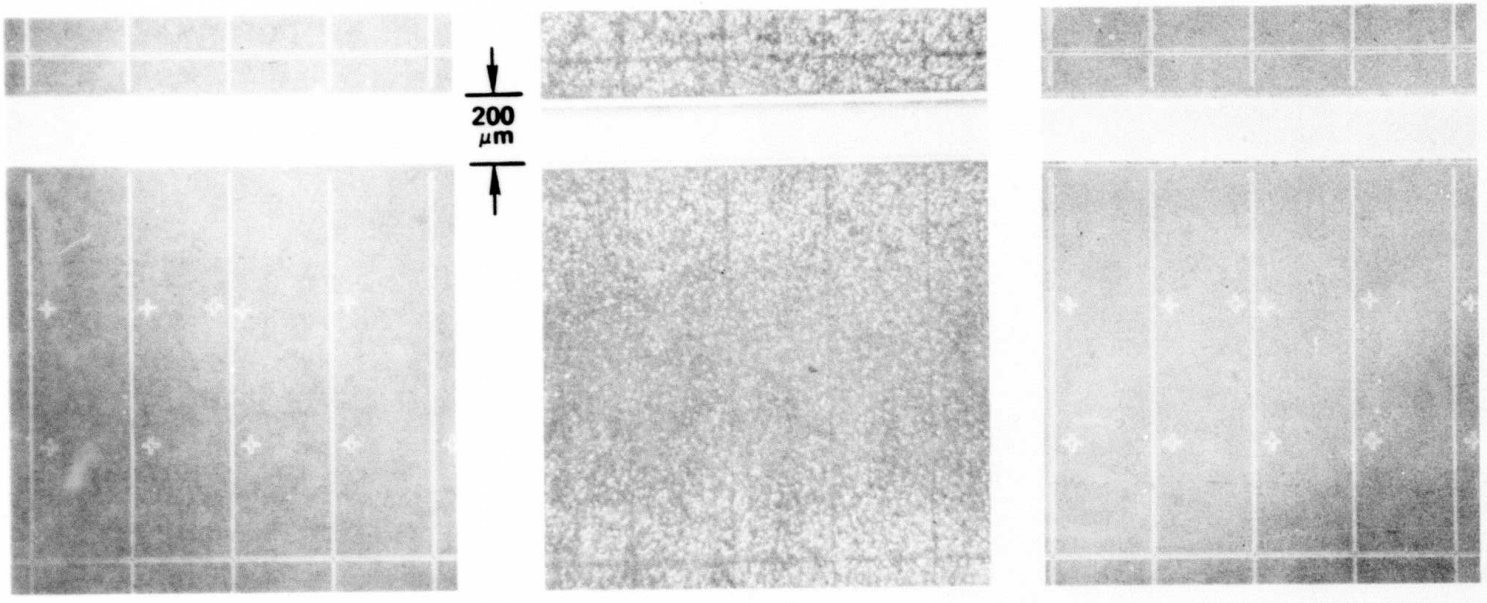


Fig. 4.8 Groove-growth process sequence using IOET mask set. (Normarski contrast photographs).

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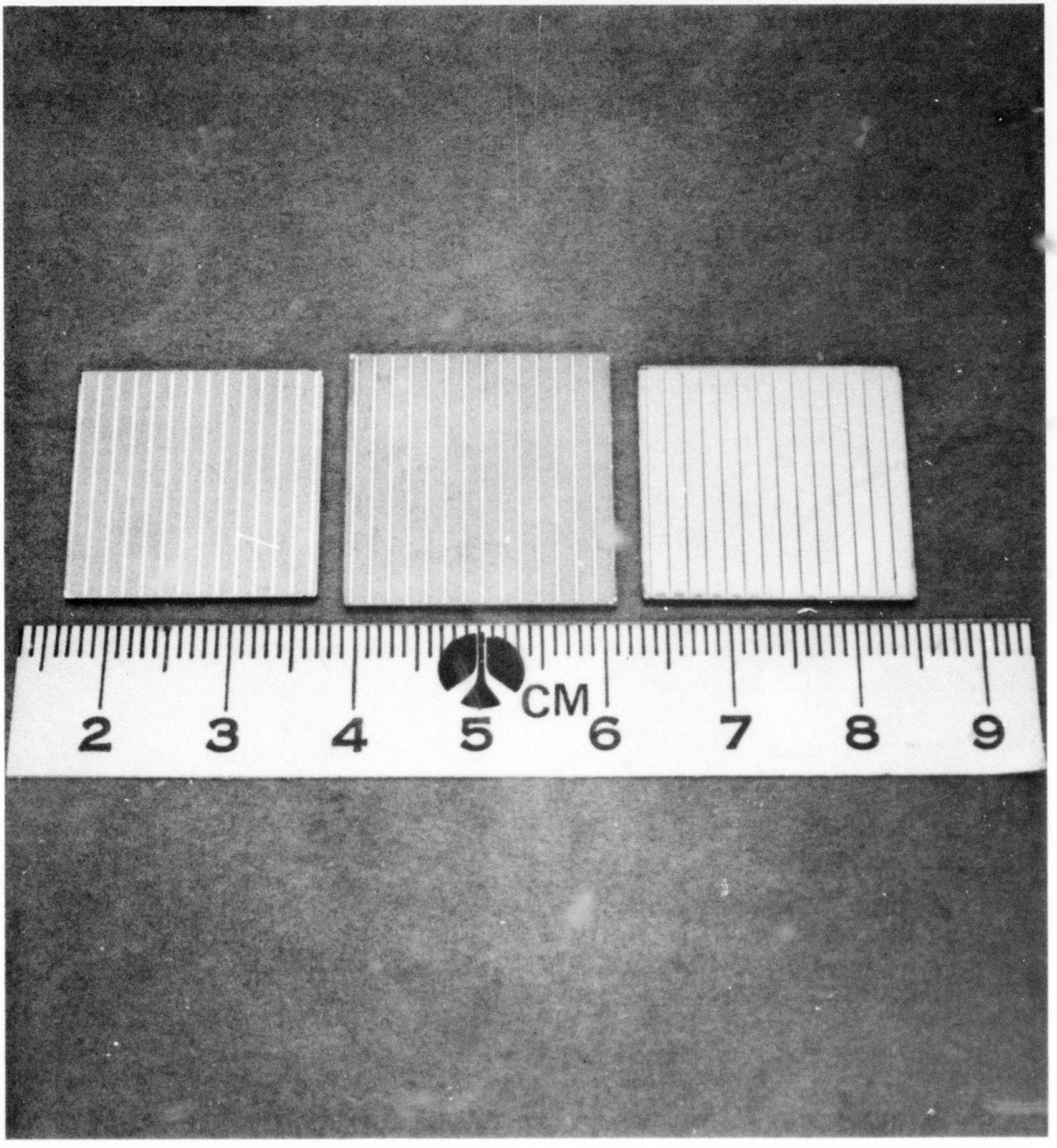

Fig. 4.9 Groove-growth process sequence using nominal 1-in. S.I. GaAs wafers.

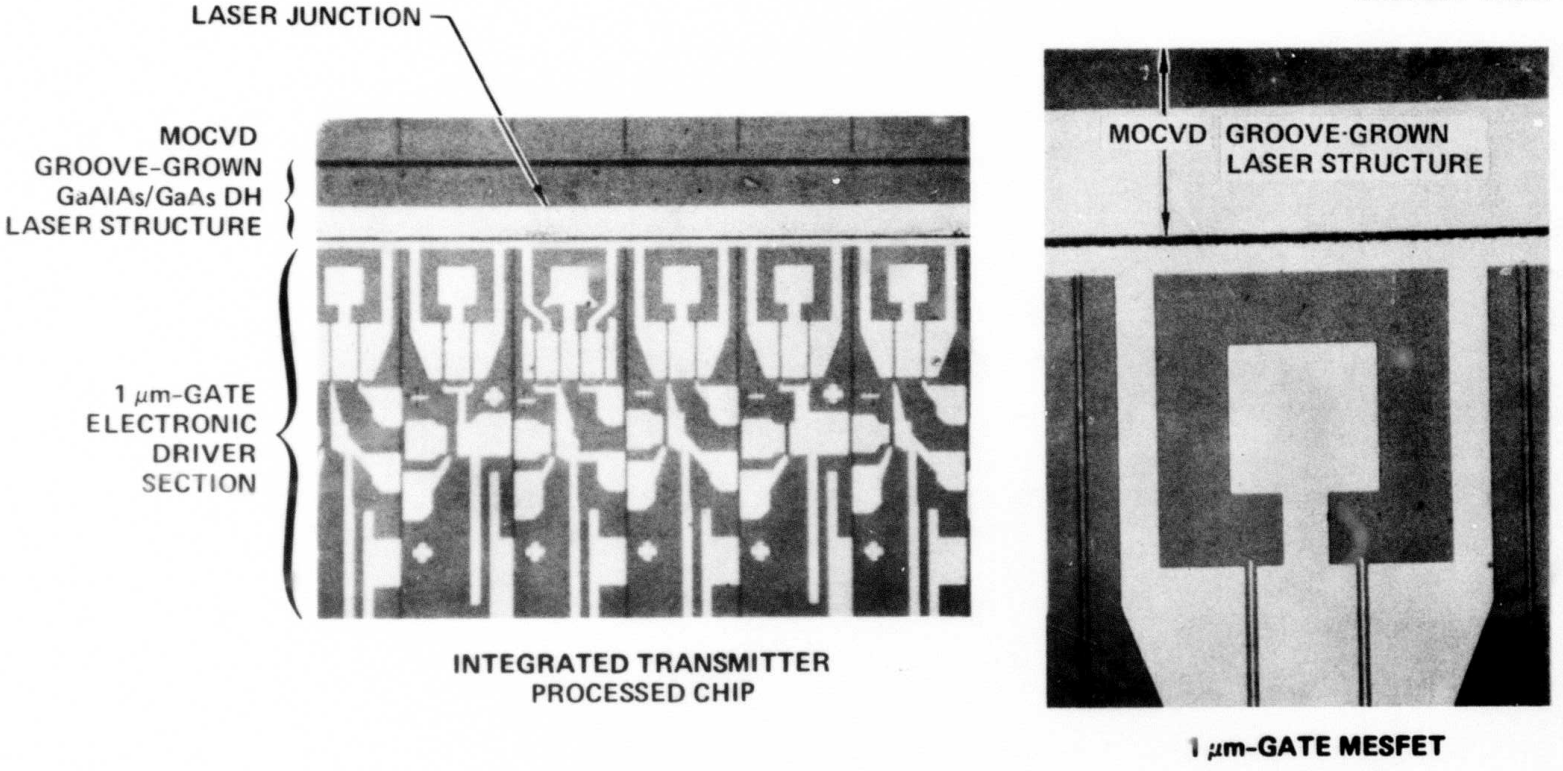

Fig. 4.10 Nominal 1-μm gate features realized in S.I. GaAs wafers with selective MOCVD GaAlAs/GaAs groove growth structures.

5.0 INTEGRATED TRANSMITTER COMPONENTS DEVELOPMENT

In this section, detailed development work on the transmitter components suitable for monolithic integration is discussed. Device processing, fabrication, and tests are described. The work primarily focused on low threshold laser development suitable for monolithic integration and the development of ion-implanted Gunn devices. Ion-implanted MESFET and resistor technology is well established, and no further development is required. Standard FET process/fabrication structures are utilized.

5.1 Laser Structures

Device performance and process/fabrication suitability are requirements in developing monolithically integrable diode lasers in the selective groove-grown heterostructure. Laser structures with milti-gigabit modulation capability with low threshold currents and top surface contacts are required. The TJS laser has the advantage of being a totally planar structure based on the diffusion of Zn into an n-type double heterostructure. Low threshold (~ 10-20 mA), single mode TJS lasers have been reported.[35-37] However, TJS lasers investigated in this work have yielded high threshold currents ~ 80-100 mA with skewed laser emission profiles. They are attributed to asymmetric junction doping profile and high losses resulting from a combination of sub-optimum active layer doping, initial surface concentration of the Zn source (source material) and diffusion steps (two-step drive-in). Continued work showed little improvement and an alternative NDS laser was developed which was found suitable for this work.[59]

The NDS laser as a monolithically integrable structure is shown in Fig. 5.1. Laser current flow is vertical; thus, a mesa etch has to be performed to expose and pick up the bottom contact. The processing requires an extra step; however, this NDS structure is relatively convenient to fabricate in terms of process control, ease, and reproducibility. In addition, it has

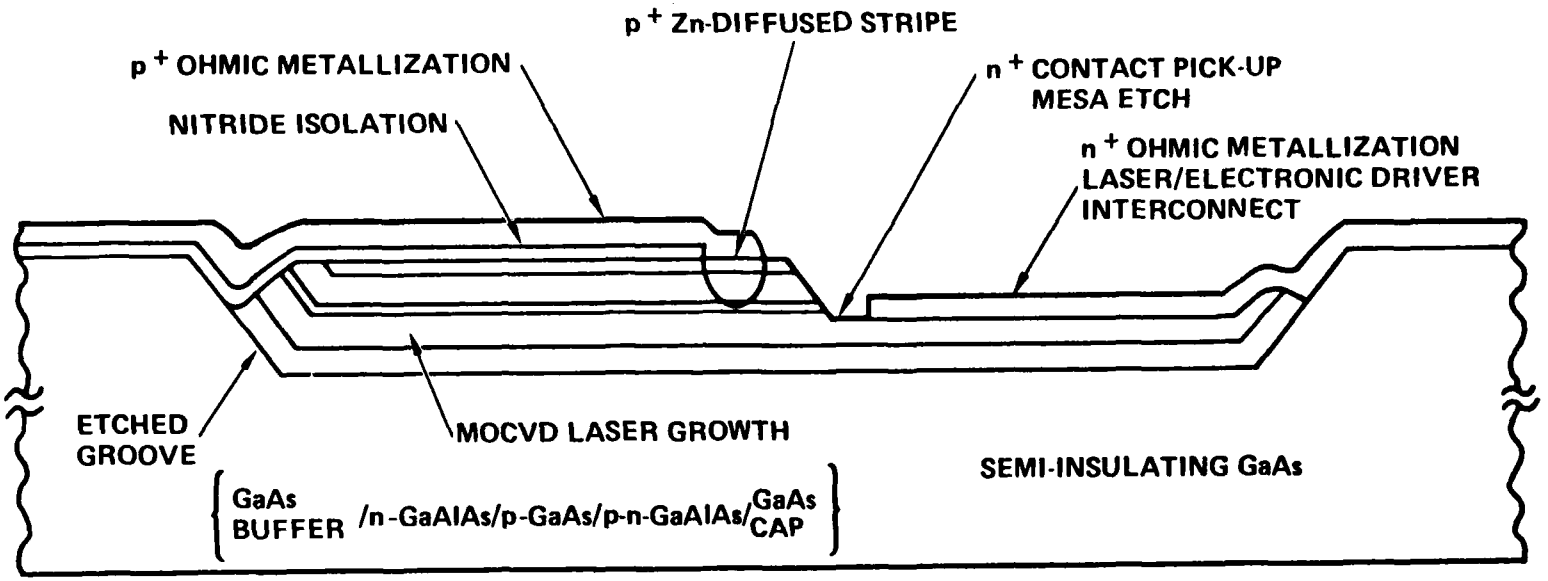

Fig. 5.1 Schematic diagram of narrow-diffused stripe (NDS) laser for monolithic integration implementation.

the desirable characteristics of relatively low threshold current ~ 40 to 50 mA, single-mode operation, high differential quantum efficiency, small temperature dependence of laser threshold (i.e., high T_o), and high output power. Narrow-diffused stripe geometries facilitate gigabit modulation capability.

The DH developed consists of an n-p-n grown structure, shown in Fig. 5.2, in which Zn is diffused through a narrow stripe to the p-active layer. The reverse biased junction outside the stripe region automatically minimizes the lateral shunt current leakage, while the presence of a grown p-n junction relieves the precise control necessary in diffusion for junction formation in deep-diffused striped (DDS) lasers with all n-type DH layers.[59,60] The six layer structure was consecutively grown on a (100)-oriented Si-doped GaAs substrate by MOCVD at a growth temperature of 750°C. It consisted of (1) 0.75 μm Se-doped (2×10^{18} cm^{-3}) n-GaAs buffer layer, (2) 2 μm Se-doped (5×10^{17} cm^{-3}) n-$Ga_{0.6}Al_{0.4}As$ confinement layer, (3) ~ 750 A Zn-doped (1×10^{18} cm^{-3}) p-GaAs active layer, (4) 0.1 to 0.3 μm Zn-doped (1×10^{18} cm^{-3}) p-$Ga_{0.6}Al_{0.4}As$ layer, (5) ~ 2 μm Se-doped (1×10^{17} cm^{-3}) n-$Ga_{0.6}Al_{0.4}As$ confinement layer, and (6) 0.1 μm Se-doped (2×10^{18} cm^{-3}) n-GaAs cap layer. The use of a thin p-type GaAlAs layer along with the p-GaAs active layer allows separate optimization of the current blocking layer and the active layer. This is the key to the structure and should be compared with the structures of Refs. 59-62. After growth, a plasma enhanced CVD Si_3N_4 film was deposited on the wafer to serve as a diffusion mask, and stripes aligned parallel to a cleaved edge were delineated in the Si_3N_4. A two-step diffusion process was used for the stripe formation. The sample was first sealed with a $ZnAs_2$ source in a quartz ampoule and diffused at 650°C for 15 ± 3 min. The second drive-in diffusion was performed at 820°C for two hr in an arsenic-rich atmosphere. The diffusions were followed by nitride mask removal and ohmic contact formation using Au-Ge/Ni/Au (alloyed) and Cr/Au on the back and front sides of the wafer, respectively. Individual diodes were defined by cleaving. Representative scanning electron microscopic photographs of the stained cleaved facets of finished devices with 2, 4, and 8 μm stripe widths are shown in Fig. 5.3. The second diffusion front extended

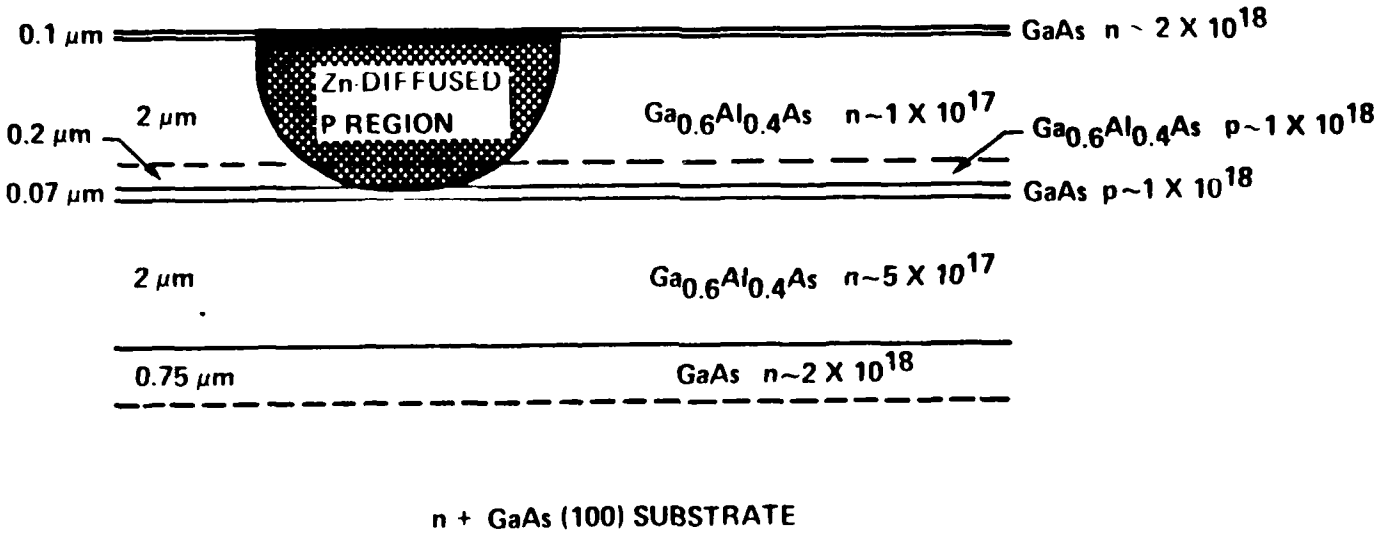

Fig. 5.2 Schematic diagram of a deep Zn-diffused stripe thin p-active layer GaAlAs/GaAs DH laser structure.

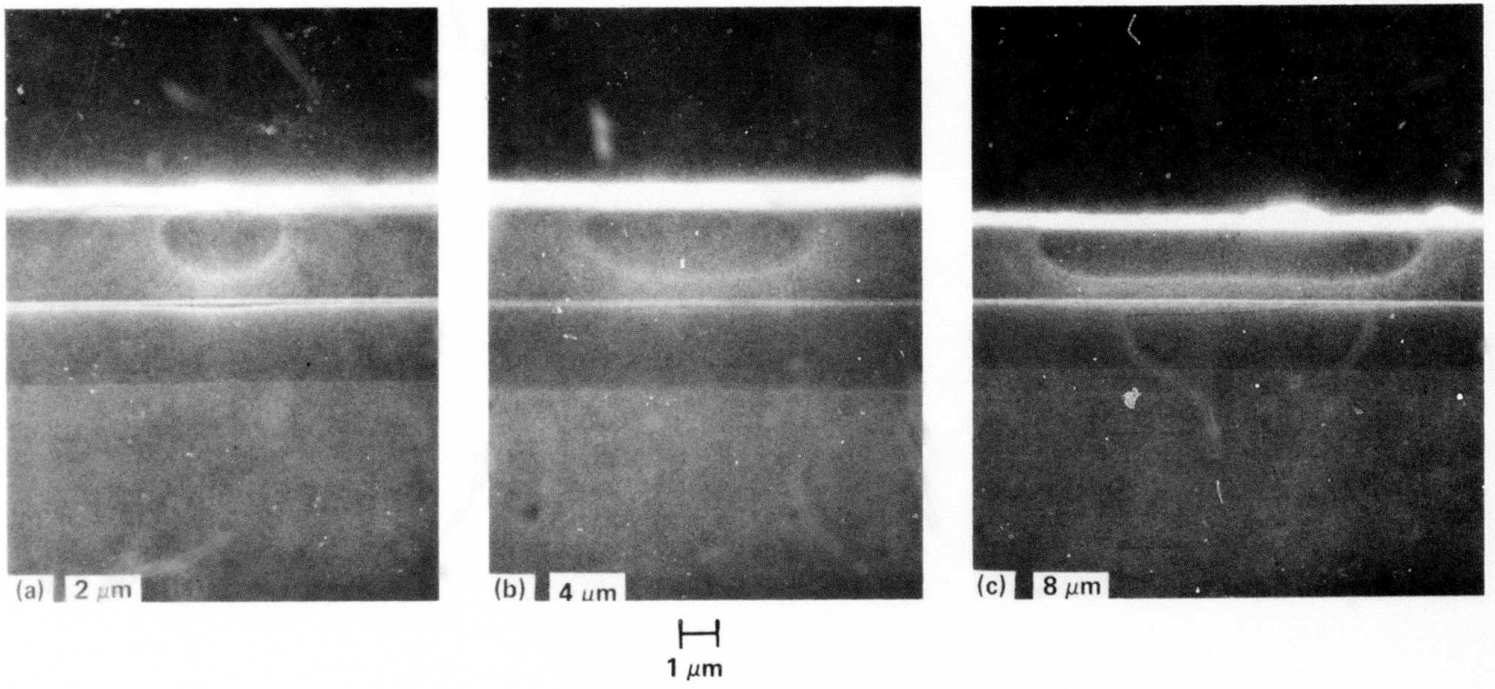

Fig. 5.3 SEM photographs of stained cleaved facets of NDS lasers with (a) 2, (b) 4, and (c) 8 μm stripe widths.

into the p-$Ga_{0.6}Al_{0.4}As$ confining the p-GaAs active layers with a well controlled tangential width approximately equal to the starting stripe width. The finished diodes were then bonded on a heat sink with In solder for subsequent testing.

Shown in Fig. 5.4 are typical curves of output power (per facet) vs input current for a 4 μm stripe laser with a 220 μm cavity for both pulsed (1 μs, 1 KHz) and dc operation. The observed cw threshold of a 45 mA is about 10% higher than the pulsed value and is comparable to similar devices (for a given diode length) with n-type active layers.[59,60] The temperature dependence of the pulsed threshold current is plotted in Fig. 5.5a. The measured characteristic temperature T_0 for typical devices is ~ 170°C. It should be noted that similar devices with n-type active layers have poor temperature dependence.[60] The dependence of threshold current on the laser cavity length is summarized in Fig. 5.5b. The threshold current is increased by ~ 50% by doubling the cavity length from 150 to 300 μm. Single longitudinal mode laser operation is observed at $I > 1.4\ I_{th}$. Representative emission spectra at various current levels are shown in Fig. 5.6 (pulsed operation). The lasing wavelength is ~ 8,650 Å and shifts to the longer wavelengths when the pumping current is increased.

For lasers that are ~ 220 μm long with 2, 4 and 8 μm stripe widths, the average threshold currents are 50, 43 ± 1, and 45 mA, respectively. The dependence of threshold currents on the stripe widths is not very significant. However, the far-field emission patterns parallel to the junction plane of these lasers are quite different. For example, shown in Fig. 5.7a-c are the typical far-field patterns of 2, 4 and 8 μm stripe lasers at various current (or power) levels. The pattern of the 8 μm laser is a normal Gaussian distribution. As the stripe width is reduced to 4 μm, the emission pattern exhibits two side lobes in addition to the main center peak indicating that the field component at the stripe edge starts to emerge due to an incease of current resistance at the stripe center. As the stripe is further reduced to 2 μm, the amplitude of the side lobes becomes greater than that of the center. This effect is similar to

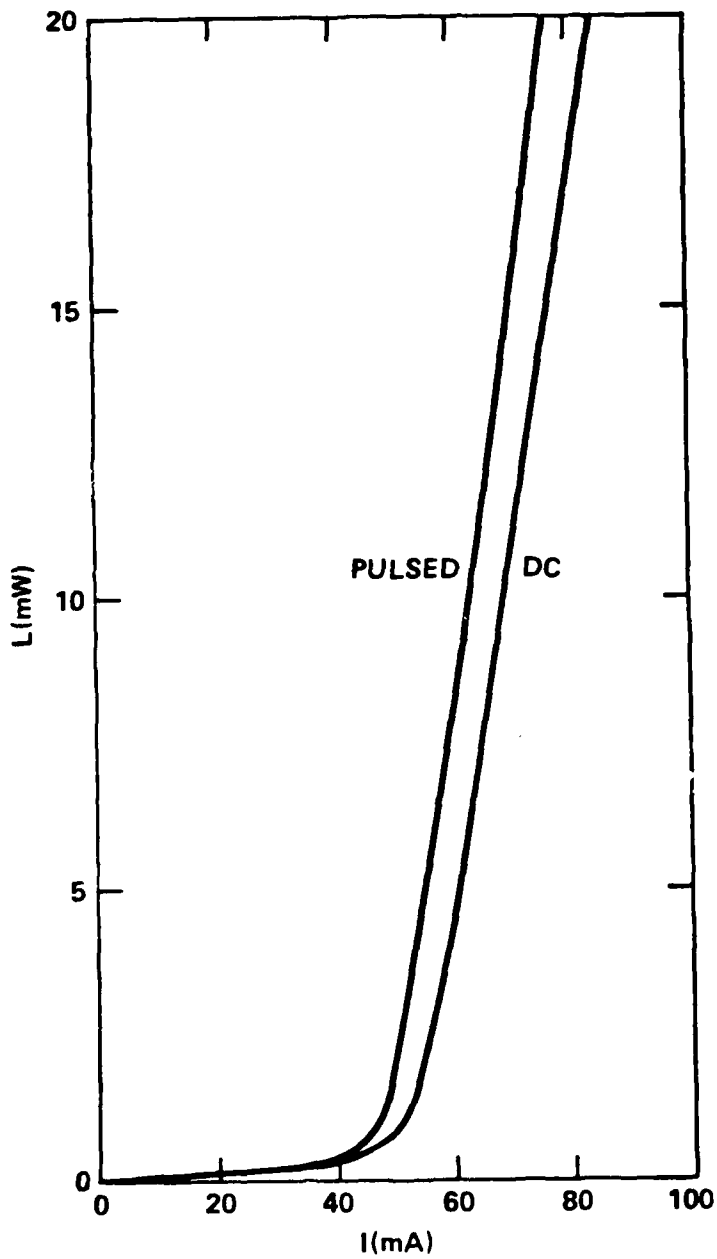

Fig. 5.4 Light/current characteristics of a 4 μm (stripe width) X 220 μm (cavity length) NDS laser.

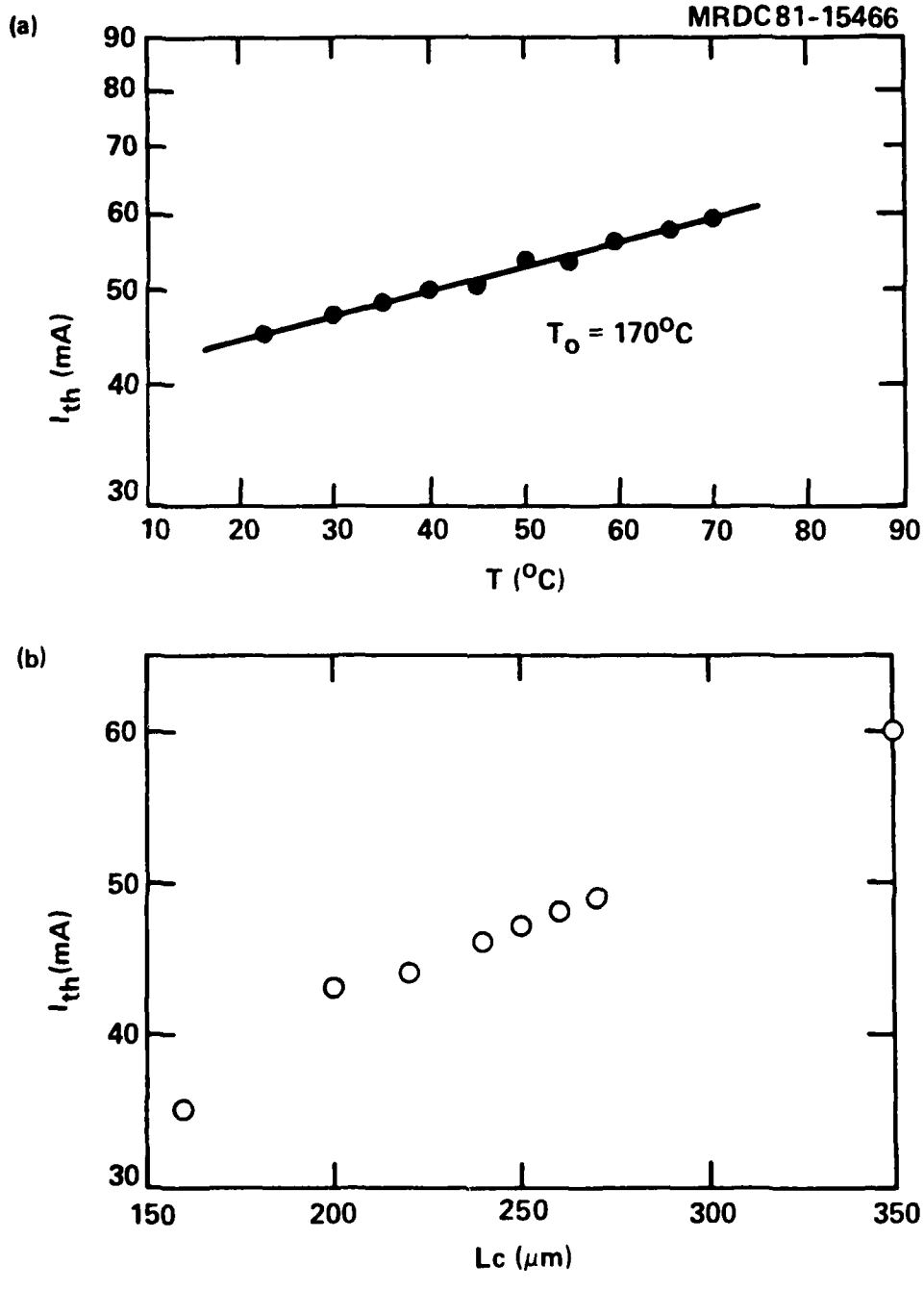

Fig. 5.5 Variation of NDS laser pulsed threshold current vs (a) heat-sink temperature and (b) laser cavity length.

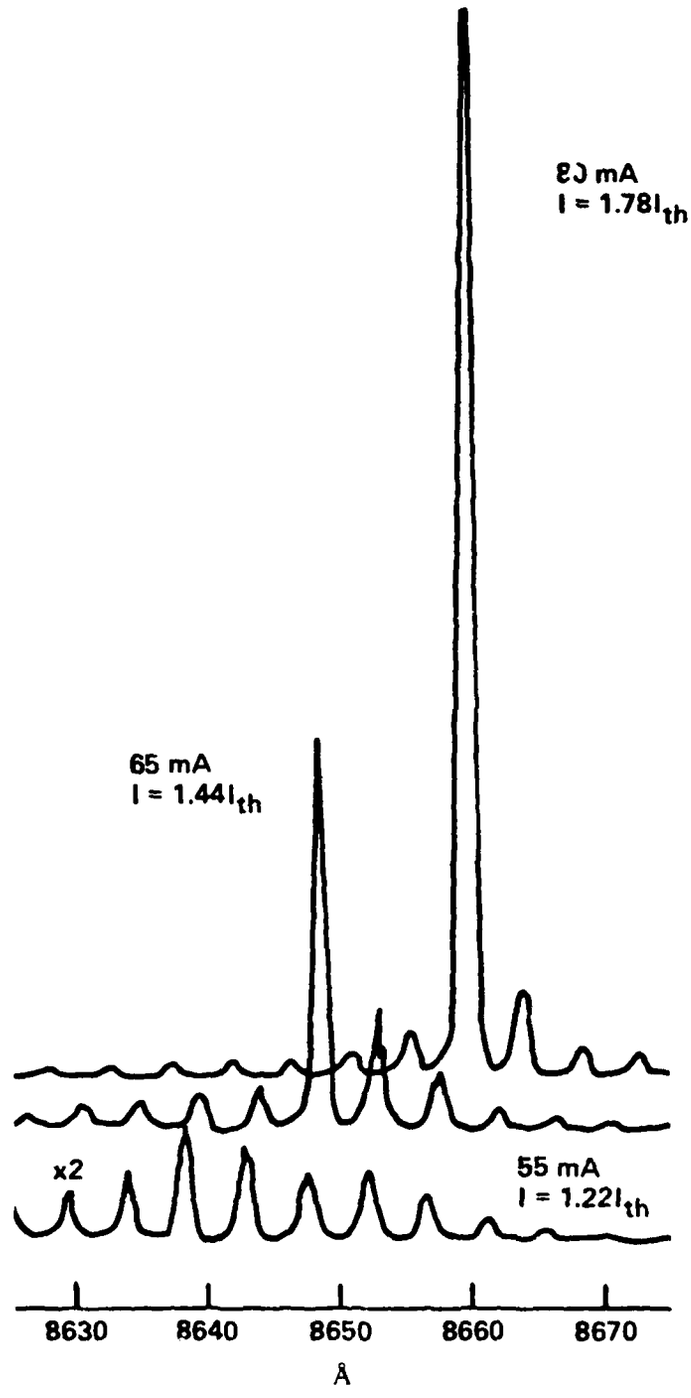

Fig. 5.6 Emission spectrum of NDS laser operated between 1.22 and 1.78 threshold current (pulsed).

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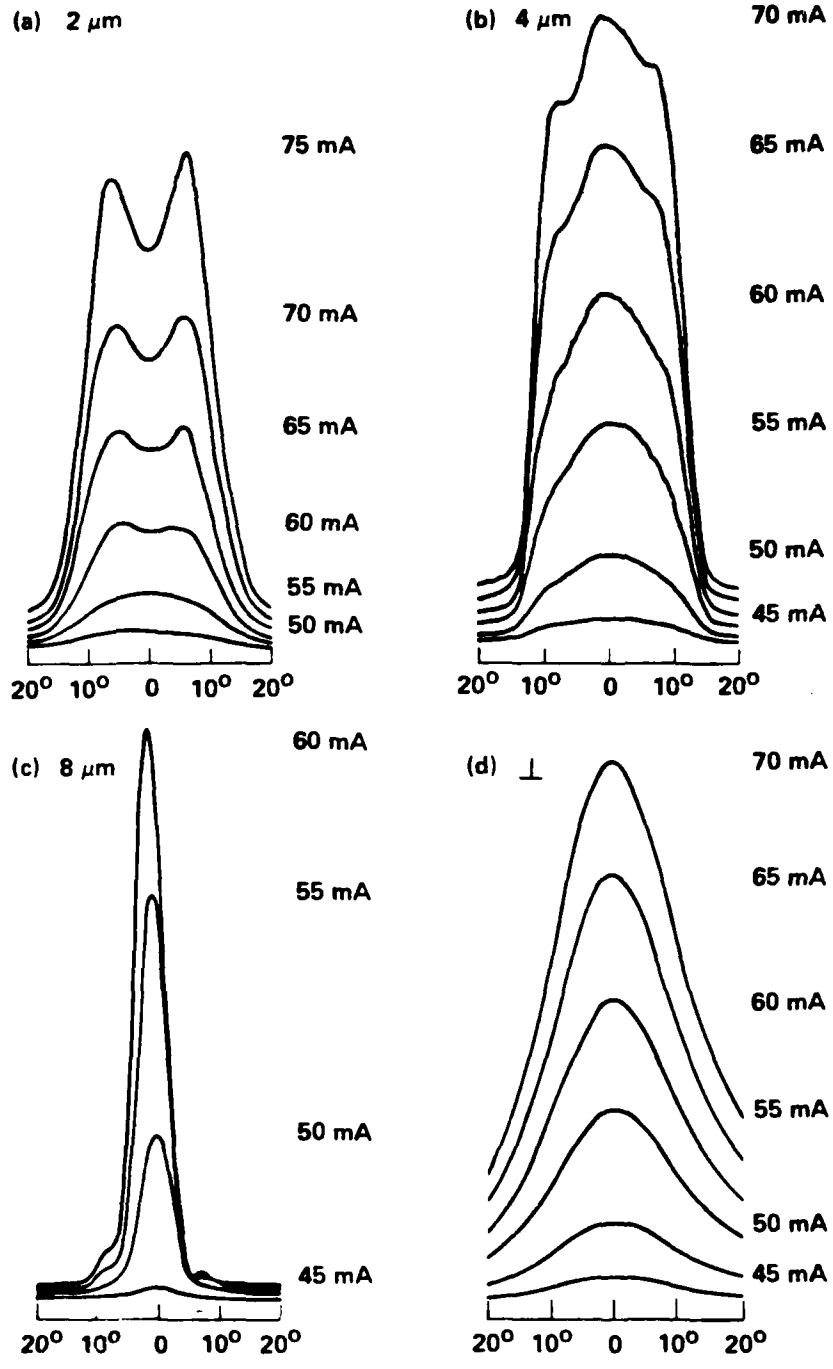


Fig. 5.7 Far-field emission patterns perpendicular (d) and parallel to the junction plane of (a) 2, (b) 4, and (c) 8 μm NDS lasers.

that which occurs in narrow oxide-defined center geometry lasers.[63] The overall divergence angles θ at FWHP measured from these stabilized patterns are ~ 22°, 23° and 6° for 2, 4 and 8 μm stripe lasers, respectively. For reference, the far-field emission pattern perpendicular to the junction plane of these lasers is shown in Fig. 5.7d. The corresponding value θ is measured to be ~ 25°.

One important feature of these diodes is the extremely high quantum efficiency. The measured external differential quantum efficiency was about 40-45% per facet from Fig. 5.4 as compared to the 20-30% for normal DH lasers[64] and 30-40% for buried heterostructure lasers.[42] We believe that the high efficiency is obtained because of large spreading of the optical field in the low absorption cladding $Ga_{0.6}Al_{0.4}As$ layers which results from the thin active layer. According to our estimation, ~ 80% of the total mode power is contained in the cladding layers. A thin active layer also favors high output power operation, because the threshold power level for catastrophic mirror damage is increased when the optical field is distributed across more of the mirror facet. For these devices, linear, kink-free L-I characteristics were observed up to a cw power of 40 mW from each uncoated mirror facet. A thin active layer also results in a less divergent output beam[65] which is desirable for coupling the laser output to a single-mode optical fiber.

Two important aspects of the laser diodes developed for this program are the uniformity and high-speed modulation characteristics. It is worth noting that the reproducibility of the devices developed here has been substantially improved when a grown junction instead of a diffused junction is used in the structure. In this manner, precise control of diffused dopings is minimized. The wafer used in the uniformity experiment is illustrated in Fig. 5.8 along with its positions to the susceptor in the MOCVD growth and the ampoule in the first diffusion. The 4 μm stripes are defined parallel to the long side of the wafer (or roughly in the radial direction of the susceptor). We have cleaved two 220 μm bars from positions 1 and 3 as indicated in Fig. 5.8. This initial test spans ~ 10 mm parallel and 12.5 mm perpendicular

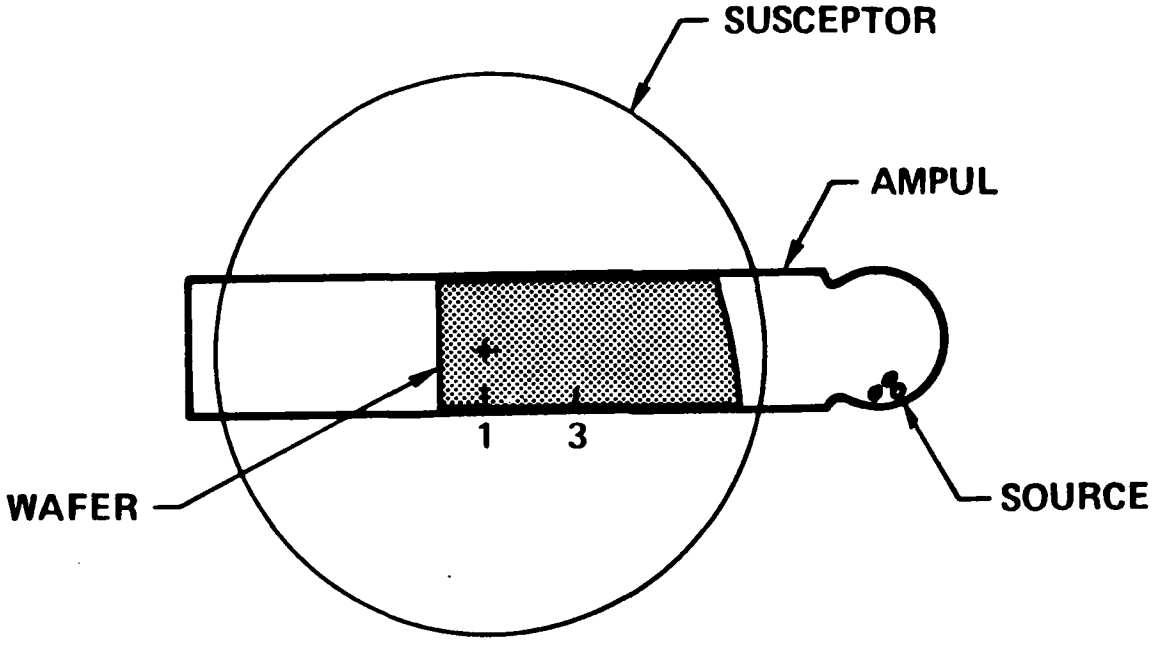


Fig. 5.8 Superimposed configurations of the wafer on the MOCVD susceptor during growth and in the ampoule during diffusion.

to the radial direction in the wafer. It is found that the uniformity of threshold currents in the radial direction is about 2 to 3%. The uniformity in the perpendicular direction is slightly higher. Shown in Fig. 5.9 are the cw L-I curves for six consecutive diodes covering a distance of 3 mm on a particular bar.

For high-speed modulation experiments, the laser was mounted on a 50 Ω microstrip line and fed with very short current pulses at a frequency of 100 MHz. Figure 5.10a shows the pulse response of the laser with a pulse width of 220 ps. No relaxation oscillations were observed with these lasers as the bias current was increased. These lasers could be used at digital bit rates > 2 Gb/s without pattern effect interference. We also employed an optical signal processing technique which uses a Fabry-Perot (FP) interferometer to isolate the laser signal and the modulation induced sidebands when the laser is dc biased and rf modulated. For example, Fig. 5.10b shows the detector output when the laser is measured with a confocal FP interferometer which has a free spectral range of 8-9 GHz and a narrow bandpass of 53 MHz. The center peak represents the throughput carrier frequency, and the two minor peaks are the sideband signals at 2.26 GHz. Each sideband contains 11% of the total power which corresponds to a modulation index of nearly 0.4.

5.2 Electronic Driver

The implementation of area-selective or localized ion-implantation techniques offer important device processing and performance advantages over epitaxial and mesa defined approaches in fabricating electronic devices in GaAs. Selective implantation technology offers excellent control over the doping charactristics and the thickness of thin active layers. Also in this approach the active-layer-substrate is never exposed during the processing, thereby avoiding many potential problems associated with this interface. Area-selective implanted channels define planar structures and are particularly advantageous to use when electronic circuits require device components with different doping densities and channel thicknesses such as

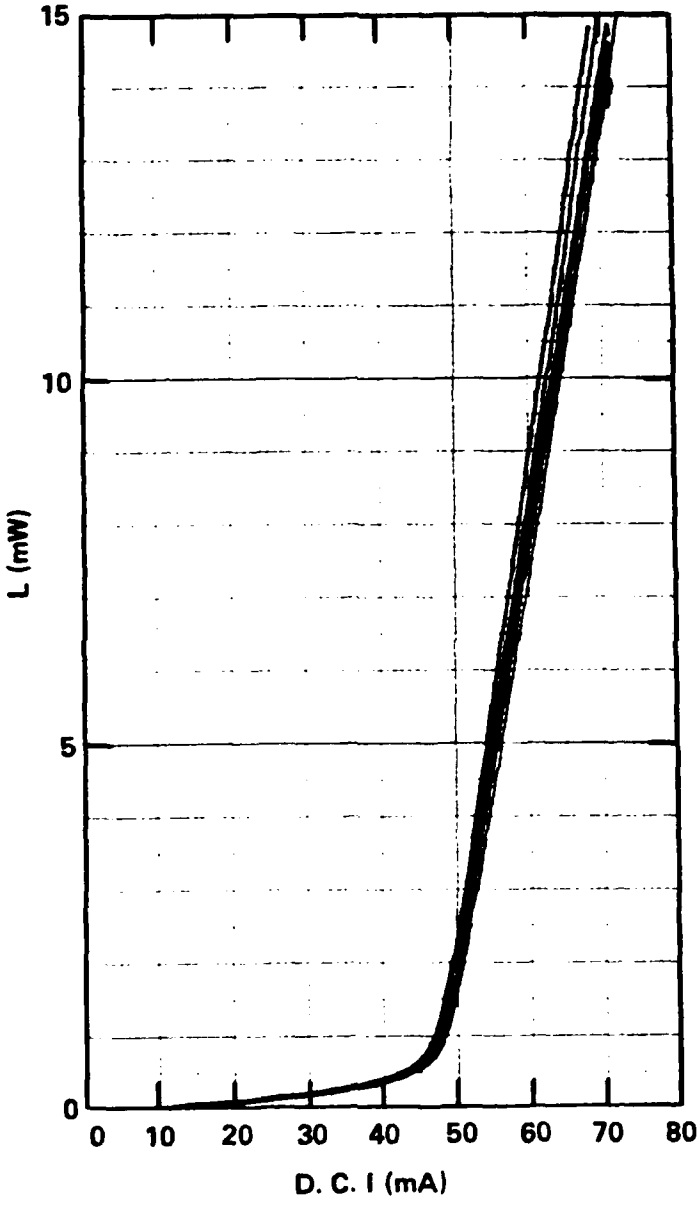


Fig. 5.9 CW L-I characteristics for six consecutive NDS lasers cleaved from a particular wafer bar.

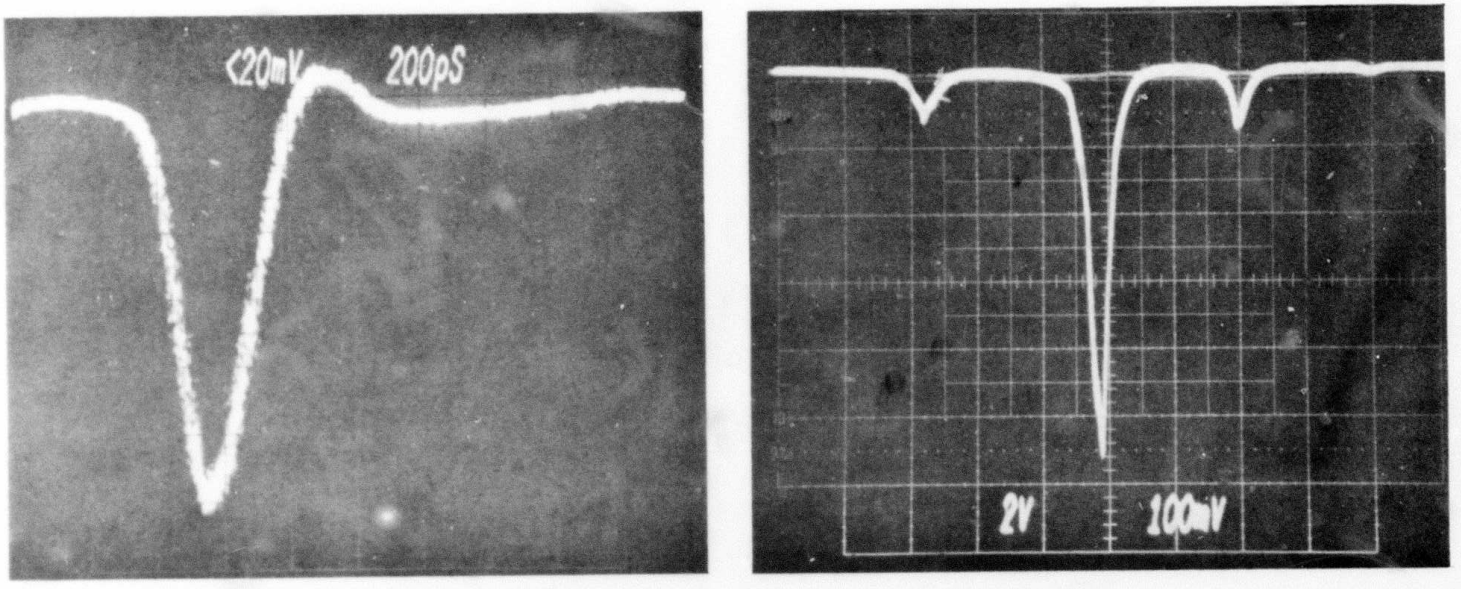


Fig. 5.10 (a) Pulsed response for a 4 μm NDS laser. (b) Signal from detector showing sideband generation with RF modulation.

MESFETs and Gunn logic devices. Established GaAs IC technologies like MMIC and digital IC use active devices such as Schottky diodes and FETs with a common implanted channel configuration. Up to now, no work has been conducted on ICs incorporating FET and Gunn devices which use planar implanted techniques. In this section, the development of FET/ resistor and Gunn devices using planar implanted techniques suitable for integrated electronic driver appications is described.

5.2.1 MESFET/Resistor

Planar implanted GaAs MESFETs are well established devices in discrete form as well as in monolithic microwave and digital ICs. A resistor is effectively an FET without a gate and the same passive device behavior is achieved by using the FET in an "active load" configuration where the source or drain is tied to the gate. In this work, the laser current drive requirements ~ 40-50 mA favor FETs with moderate power requirements and lead to device structures similar to those of discrete microwave FETs.

The detailed FET/resistor device fabrication parameters were defined from the laser threshold requirements and the TELD designs of the transmitter mask set IOET. Two-dimensional modeling based on a modified Pucel analysis[10,66] was used to evaluate implantation profiles and MESFET characteristics suitable for the laser driver designs. The device modeling and experiments have confirmed that a peaked profile of a single dose implant can yield high performance devices equal to or better than those with flatter multiple implants. Selenium and silicon are both well established implant dopants used for n-type channels. A nominal FET saturation current of ~ 20 mA per 100 μm of gate width and a nominal sheet resistance of about 1000 Ω/square were determined to be generally useful for the various laser driver designs on the transmitter mask set. These device requirements define a set of implant parameters, 3×10^{12} Si ions cm^{-2} implanted at an energy of 300 keV to yield peak carrier concentrations ~ 10^{17} cm^{-3} and implant depth ~ 0.25 μm. Implant

experiments and evaluation of Schottky diode depletion capacitance generally confirmed these modeling studies.

The implanation of the MESFET/resistor channels through the nitride is followed by silicon oxide capping (as described earlier in Section 4.0) and the activation/anneal cycle at 850°C for 25 min. Experiments conducted by the GaAs digital IC have shown that Si implant distributions remain effectively unchanged for activation/anneals as long as 2 hours. Typically 90% electrical activity is achieved.

The MESFET/resistor electrical contacts are formed by first dry etching through the nitride/oxide cap. Low resistance source drain ohmic contacts, ~ 10^{-5}-10^{-6} $\Omega \cdot cm^2$ specific resistance, are realized by alloying an eutectic composition of Au-Ge at 450°C. A multi-component gate metal system (Ti/Pt/Au) is used to promote device reliability.

The fabrication of discrete MESFETs and resistors using planar implanted techniques is well established in our laboratory; therefore, work on these devices was reserved for wafers with selective groove-grown epitaxial structures.

5.2.2 TELD

The technology of planar implanted Gunn logic devices is less established. Gunn devices as discussed in Section 3.1.2 require significantly deeper channels, ~ 1-2 μm, compared to ~ 0.2-0.3 μm for FETs. Higher energies on the order of 800-2000 keV, are required to achieve such implant depths, and ion implanters with these capabilities are not readily available. For this work, requirements for specialized apparatus was circumvented by using a more conventional implanter having a maximum energy of 390 keV and using a doubly ionized Si specie to achieve depths of about 1 μm and multiple singly-ionized Si implants to produce the necessary nt > 10^{12} cm^{-2}. Figure 5.11 shows the results of a triple Si implant profile using single and double ionized species to achieve implant depths to ~ 0.8 μm for two carrier concentration levels, n ~ 3 × 10^{16} cm^{-3} and n ~ 7 × 10^{16} cm^{-3}.

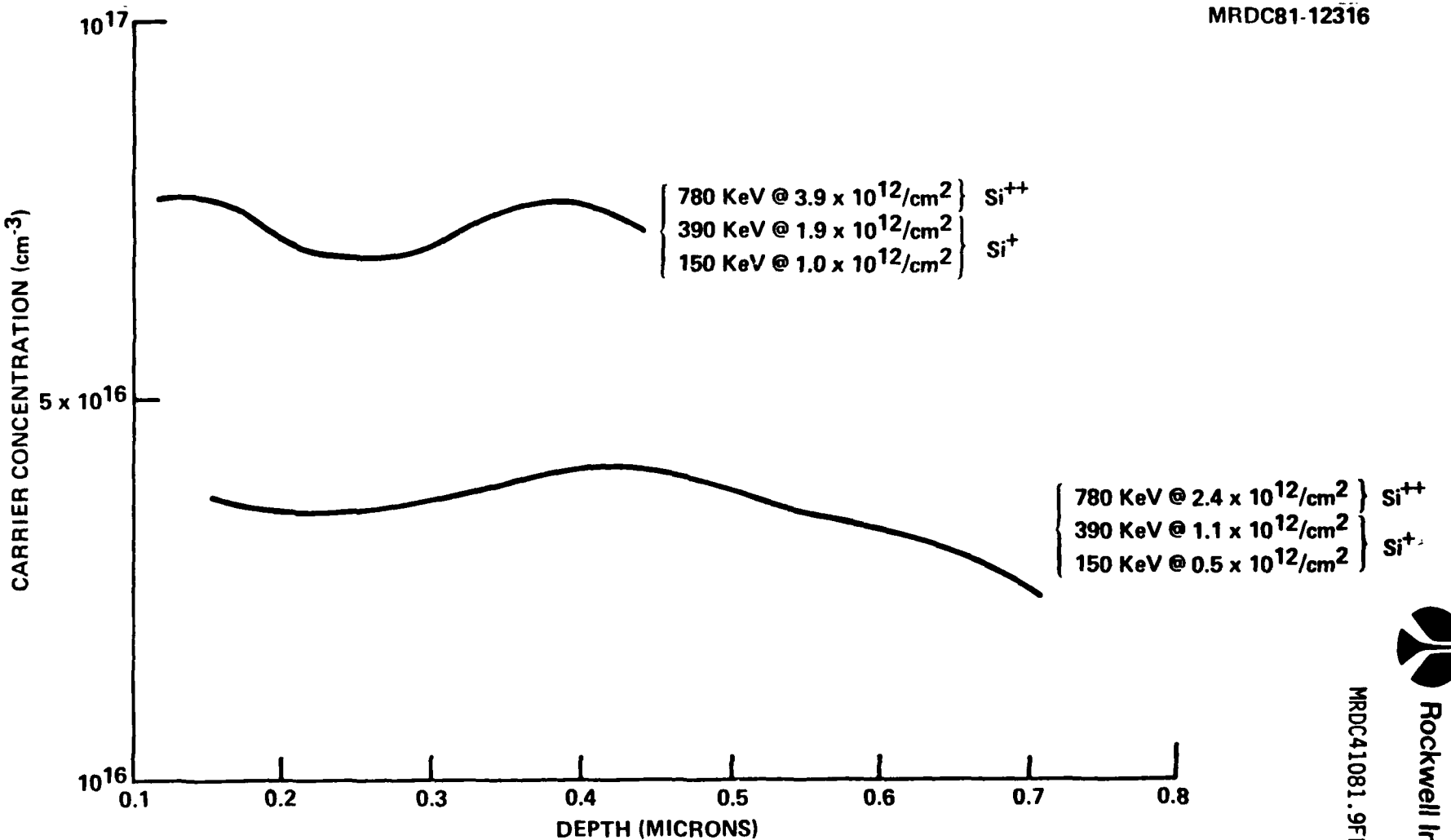
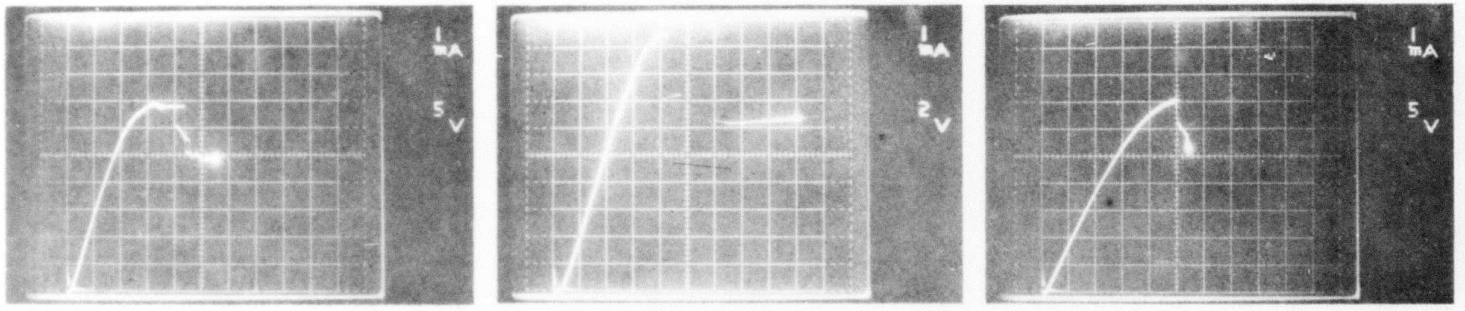


Fig. 5.11 Si implant profiles for GaAs implanted TELD device development.

Development of Gunn devices based on ion-implanted channels first began with mesa delineated structures followed by planar selective implant devices. Figure 5.12 shows dc current-voltage characteristics of mesa etched Gunn devices for various carrier concentrations using wafers from both in-house and commercial sources. The current drop ratios were in the range of 30 to 40%. Implantation parameters developed using the mesa delineated Gunn devices were extended to planar structures. Selective or localized implant requires masking of wafer areas. In this work, a photoresist ~ 3 μm thick was found to be a useful implant mask for stopping 780 keV Si. Figure 5.13 shows the implant profile and the resulting IV characteristic of a TELD device from the IOET transmitter mask set. The current drop ratio is about 15%.

TRIPLE Si IMPLANTS: FLAT PROFILE
Si^{++} (390 keV) DEEP IMPLANT $t \cong 0.8\ \mu m$

MRDC 83-21141



$n \cong 4.5 \times 10^{16}/cm^3$
CRYSTAL SPECIALTIES

$n \cong 6.5 \times 10^{16}/cm^3$
ROCKWELL LEC

$n \cong 7.0 \times 10^{16}/cm^3$
CRYSTAL SPECIALTIES

Fig. 5.12 GaAs implanted Gunn devices with mesa isolation.

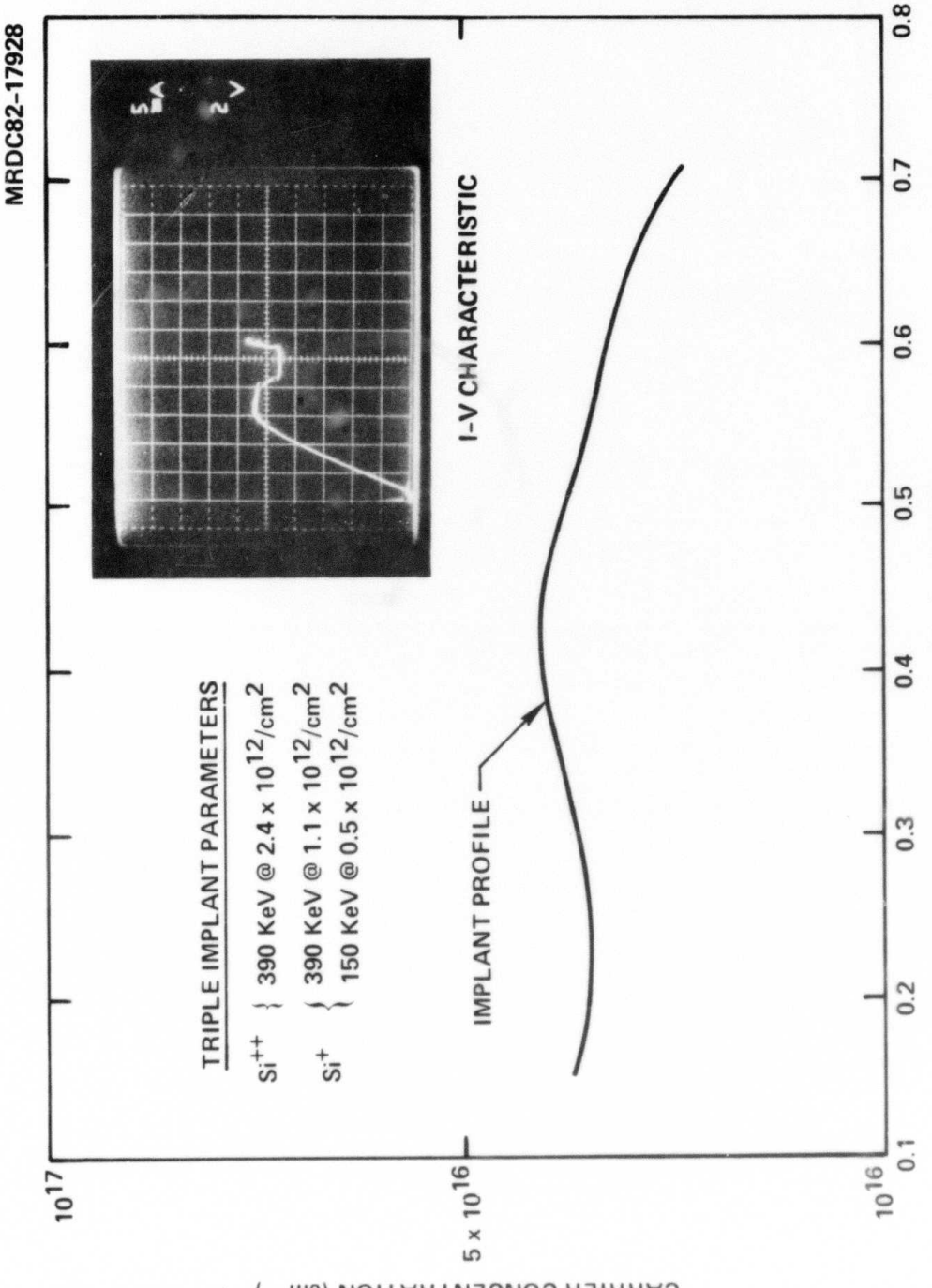


Fig. 5.13 GaAs Planar selective implanted Gunn device.

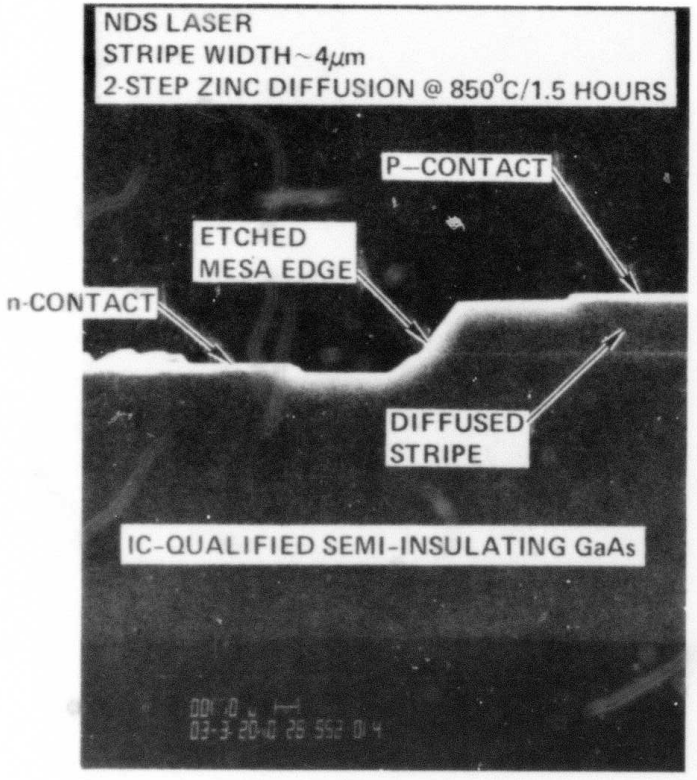
6.0 INTEGRATED TRANSMITTER DEVELOPMENT

The nominal device performance and process/fabrication requirements for the individual transmitter components support a monolithic integration capability. The development status of the GaAs MESFETs/resistors, TELDs and diode lasers as component devices described in Section 5.0 indicates functional usefulness of the transmitter circuit. Planar, implanted MESFETs are well-established devices. In the implanted TELD development work here, the dc current drops ratios achieved are between 15-40%. It is anticipated that even the lower values will facilitate useful modulation of diode lasers having cw threshold currents of 50-60 mA, such as those developed in this work. From the standpoint of device processing and fabrication a common planar processing based on selective channel implants appears to be quite practical for a mix of FET and Gunn logic devices used for the elecronic driver. The on-chip integration of various laser structures, even the mesa-etched structures such as the NDS laser, appears feasible. However, one of the more important requirements which would seem to facilitate the monolithic integration of lasers and implanted electronic devices is the processing temperature compatibility. A fairly safe margin appears to exist for GaAs implant activation/anneal temperature cycle (850°C/30 min and up to 2 hours), MOCVD laser epitaxy (750°C/30 min) and any laser diffusions (850°C/2 hours).

The choice of laser structures without the need for diffusions, such as oxide-defined or buried heterostructure lasers, would facilitate an integration process sequence in which the laser selective epitaxy could precede or follow the electronic device implantation and activation/anneal steps. In this work, the success with narrow-diffused stripe lasers has defined an integration process/fabrication sequence in which the selective laser epitaxy and the initial NDS diffusions are first-performed followed by the ion-implantation and activation/anneal temperature cycle which also completes the NDS laser diffusion.

The viability of the monolithic integration approach developed here can be supported by the realization of key optoelectronic devices using the planar, selective epitaxial structures on S.I. GaAs using the existing transmitter mask set. In one set of experiments, cleaved mirror NDS lasers were fabricated in the groove grown GaAlAs/GaAs regions of the wafer. An SEM cross-section of the NDS laser and the L-I curve are shown in Fig. 6.1. The devices have J_{th} ~ 60 to 70 mA, (corresponding to a long cavity length of ~ 340 μm) which are comparable to the J_{th} of similar devices fabricated on n^+-GaAs control wafers. In another set of wafers with groove-grown laser structures and which were subjected to laser processing temperature cycles, planar, selectively implanted MESFETs were subsequently fabricated in the S.I. regions. The FET devices have nominal gate length of 1 μm and were fabricated using the process described in Section 5.2.1. The fabricated FET and corresponding dc characteristics are shown in Fig. 6.2. The saturation current is ~ 50 mA and g_m ≈ 35 mS/mm for the device shown. Currently these device characteristics are adequate for the integrated transmitter designs proposed in this work.

Although the use of the selective groove-grown epitaxial structures to demonstrate NDS lasers and planar, implanted 1-μm gate FETs involved different wafers, these results indicate the feasibility of realizing the complete integrated transmitter. At the close of this program, complete transmitter processing was in progress.



SEM CROSS-SECTION OF NDS
LASER ETCHED MESA EDGE

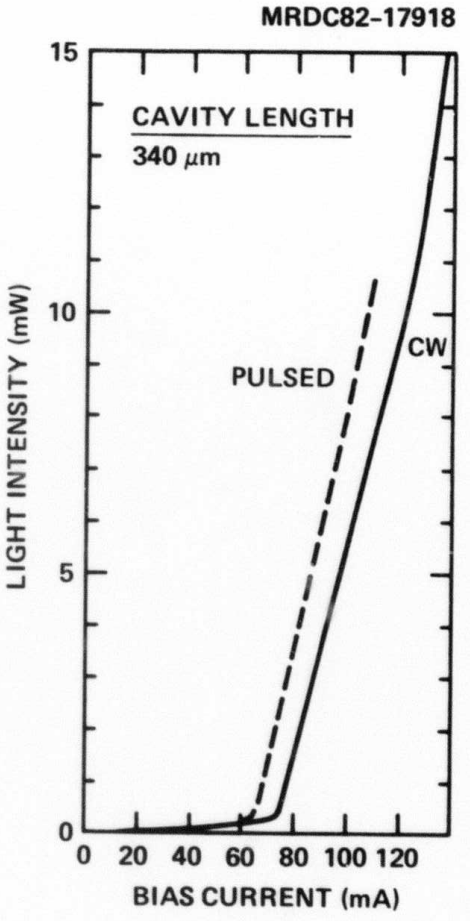
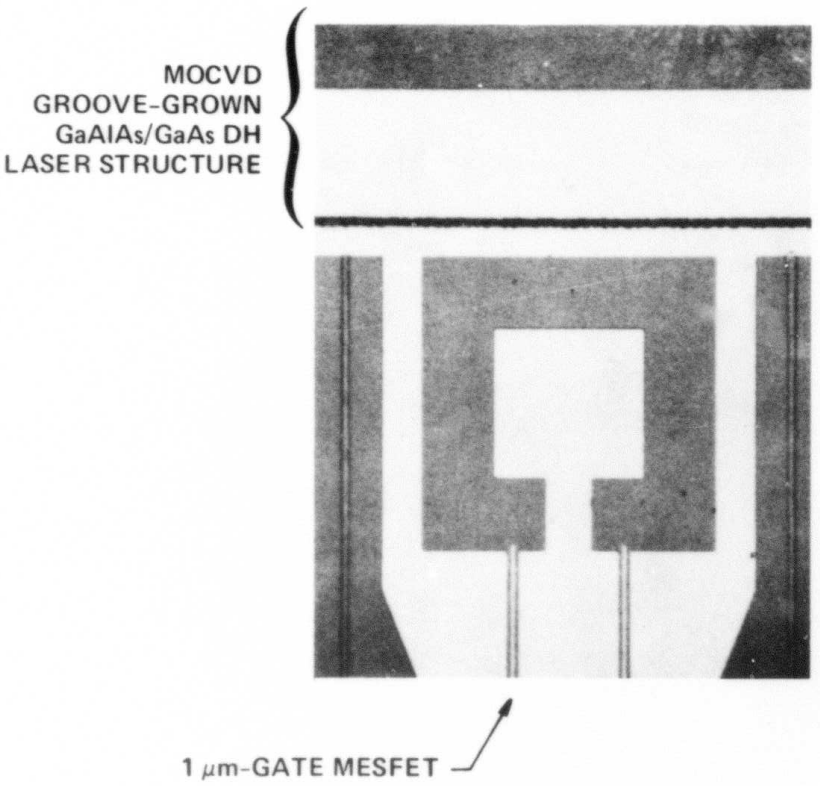


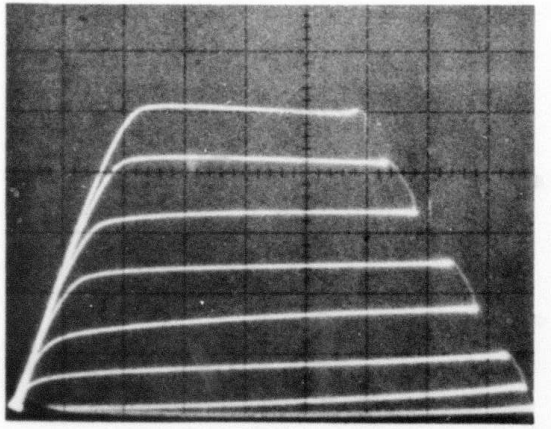
Fig. 6.1 NDS DH laser fabricated in selective MOCVD groove-grown GaAlAs/GaAs structure.



Si IMPLANTED CHANNEL

ENERGY: 300 KeV DOSE: 3×10^{12} cm^{-2}

n(PEAK) ~ 8×10^{16} cm^{-3} @ DEPTH ~ 0.3 μm



MESFET: I-V CHARACTERISTICS

I_{DSS} = 10 mA/Div
V_{DS} = 2 V/Div
V_{GS} = -1V/STEP
V_{PO} = -6.5V

Fig. 6.2 Planar, implanted 1-μm gate MESFET fabricated in S.I. GaAs structure with selective MOCVD GaAlAs/GaAs groove growth.

7.0 CONCLUSIONS AND RECOMMENDATIONS

This work focused on developing a technology for realizing a GaAsAs/GaAs monolithic integrated optoelectronic transmitter for high-speed fiber optic communications applications. Although a functional integrated optoelectronic transmitter was not realized at the end of the program, the techniques developed established the feasibility of integrating two well-established technologies, optical devices based on GaAlAs/GaAs epitaxial growths and high-speed GaAs electronic devices based on planar, ion-implantation. As a result of this work, general and specific conclusions and recommendations are presented in this section.

7.1 Conclusions

Major conclusions are drawn from the primary objectives addressed in this work. They are as follows:

1. Determine a suitable approach for integrating optical and electronic devices in terms of compatible device processing and fabrication:

   Various integration approaches were investigated and a selective epitaxial groove-growth technique using a dielectric mask was found to be the most suitable with planar GaAs electronic device processing which employ ion-implantation and 1-μm geometries.

2. Design a simplified high-speed transmitter based on the integration approach which will serve as a building block for future, more sophisticated designs:

   A nominal 1-4 Gb/s transmitter utilizing standard cleaved mirror lasers and FET/Gunn logic drivers was designed, process/fabrication steps defined, and a fabrication mask set

generated. Although integrated GaAs electronics utilizing Gunn devices such as TEDs and TELDs facilitate high-speed capability with circuit simplicity, the process complexity and high power dissipation make mixed FET/Gunn device circuits less attractive than purely FET circuits. MMIC and digital ICs utilizing FET based logic are well-established compared to circuits which also incorporate Gunn devices. For true monolithic integration with complex on-chip electronics capability, lasers without standard cleaved mirror facets will be needed, such as etched-mirror structures.

3. Develop the transmitter materials technology:

MOCVD of GaAsAs/GaAs was used in the selective epitaxial growth of DH lasers on S.I. GaAs substrates qualified for ion-implanted ICs. The MOCVD technique has inherent advantages of growth control, uniformity and reproducibility as well as excellent surface morphology. However, its growth over all exposed surface, including the dielectric mask, requires an extra removal process step.

4. Develop the transmitter device components:

NDS lasers and planar, ion-implanted MESFETs and Gunn devices were developed for the transmitter application. NDS lasers with cw thresolds ~ 60-70 mA (~ 340 μm cavity) and 1-μm gate FETs were separately realized on S.I. GaAs wafers with selective, groove-grown heterostructures. Although the performance of these devices is compatible with the integrated transmitter design, more practical applications will necessitate lower laser thresholds, ~ 10-20 mA or less. Planar, ion implantation for FETs is well-established; however, for Gunn devices, the

requirements for significantly deeper channels/implant energies make this technique less desirable.

5. Fabricate and demonstrate the integrated transmitter:

   At program end the integration technique developed appeared quite feasible for realizing a functional integration transmitter based on an NDS laser and a FET/TELD electronic driver for Gb/s operation.

7.2 Recommendations

The recommendations that result from this work are concerned with the continued technology development that must be performed to make high-speed optical links based on integrated optoelectronics a reality. In this work, the feasibility of an integrated transmitter based on an NDS laser and planar implanted FET/TELD driver was demonstrated. The fabrication and demonstration completion of a Gb/s transmitter as originally conceived in this program would serve to verify the integrated technology approach.

In order to realize more practical transmitter structures further work must be performed. The key to the integrated optoelectronics device technology is refinement and optimization of the selective-groove growth epitaxy and processing techniques which are useful not only for laser transmitters but also for integrated receivers. For the transmitter development, very low threshold lasers based on the TJS, buried-heterostructure, or quantum-well structures are required. The goal of this work would be to realize integrable lasers with less than 10 mA threshold current and high quantum efficiency operation. Lasers without standard cleaved mirrors are requisite for true integration capability. Etched-mirror lasers appear to have potentials for more near term applications. The development of a new transmitter design utilizing an all FET electronics would make device processing more simplified and consistent with standard GaAs MMIC and digital IC technology.

For the Gb/s optical link, an integrated optoelectronic receiver must also be developed. The selective groove-growth technique developed for the integrated transmitter is directly applicable. However, the integrated receiver is less critical based on the requirements of the detector structure compared to the laser/transmitter. A low-capacitance photodiode (PIN) must be realized for high-speed response; however, the receiver preamplifier can utilize standard GaAs MMIC or digital IC techniques. With the development of integrated optoelectronic receivers and transmitters, a demonstration of a Gb/s optical link will establish the baseline operational characteristics of these devices.

At this time a sustaining technology development effort is needed to achieve multi-gigabit/s optical links using integrated optoelectronic components. The recommendations discussed here would lead to the realization of the first generation high-speed optical links based on GaAs integrated optical transmitters and receivers. These devices and the related technology will serve as the basis for future higher performance and more sophisticated transmitters, receivers and transceivers.

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