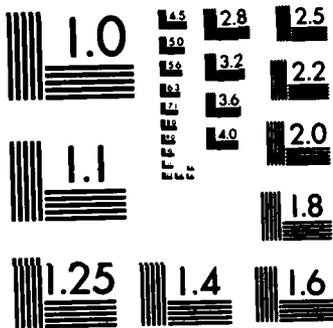END

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Report NADC-78159-40

AD A123766

PIN DIODE SWITCHABLE CAPACITANCE ARRAYS

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Final Report

JAN 25 1983

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Capacitor/Pin Diode Array,
Tuning element for electronically tuned filter

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The contract requirement was the development of a monolithic
10 capacitor/pin diode array to be used as a tuning element
in an electronically tuned filter. The initial integrated
circuits exhibited stray capacitances between the circuit
elements through the high resistivity silicon substrate and
the MOM capacitors did not have a high enough Q for optimium

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circuit performance. Therefore, the remaining effort was directed toward the development of a discrete PIN diode with a low enough RF resistance in conjunction with the required capacitance value to combine with high Q micro-wave capacitors in a hybrid circuit. This diode/capacitor array fits into a 0.6 x 0.4 inch area which reduced the number of available devices to six from ten due to the size of the units. This is the array which was finally delivered.

The hybrid array occupies much more area than the proposed integrated circuit, but it appears to be the best way to reduce the parasitics of the capacitor/diode array. Therefore, we recommend that the package be redesigned so that it becomes an integral part of the filter circuit.

I. INTRODUCTION

The contract requirement is to design, develop, fabricate and deliver an integrated monolithic capacitor/pin diode array. The circuit schematic is shown in Figure 1. It shows that ten diodes and capacitors are required. The array will be used as the tuning element in a multi-octave, high power, electronically tuned filter. A package for the circuit must also be designed. It should not exceed 0.1 inches in height with access to input and control terminals.

The pin diode and capacitor characteristics are listed in Table 1.

TABLE 1

1. RF Resistance (Forward Bias) - 0.2 ohms with a design goal of 0.1 ohm at 20 milliamps up to a frequency of 400 MH_z.

2. Diode CAPACITANCE - 0.2 picofared maximum when reverse biased.

3. Inductive Component - 0.2 nanohenries maximum between each capacitor and its corresponding diode.

4. Diode Voltage Breakdown - 500 volts minimum.

5. Power Input - Nominal signal handling capability of the array to be 10 watts.

6. Capacitor Q Factor - 2000 nominal at 500 MH_z.
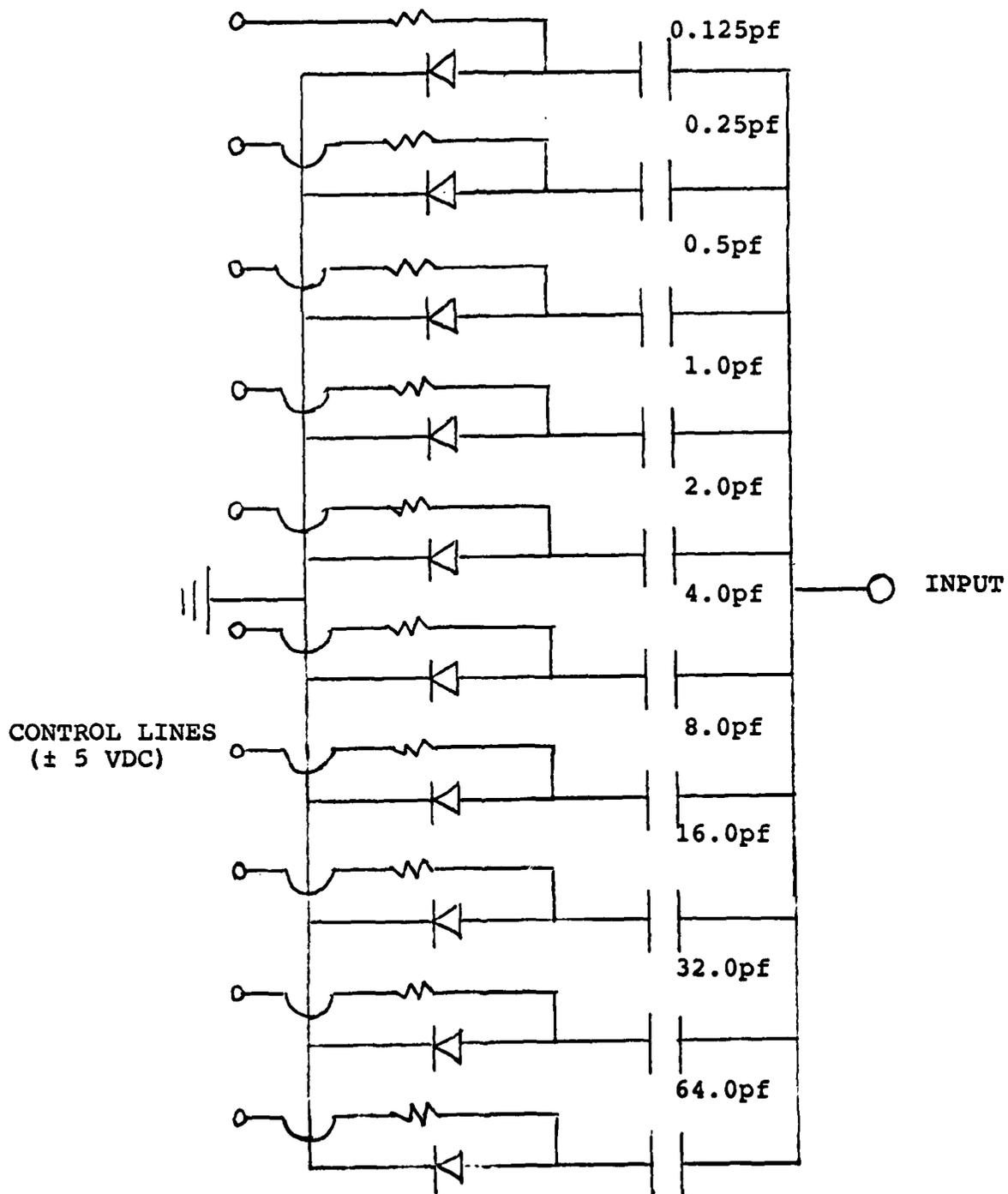
0.125pf

0.25pf

0.5pf

1.0pf

2.0pf

4.0pf INPUT

8.0pf

16.0pf

CONTROL LINES
(± 5 VDC)

32.0pf

64.0pf

Figure 1

2

II.   CIRCUIT CONCEPTION, DESIGN AND RESULTS

Discrete diode and MOS capacitor masks were designed to test the concept of the filter operation using these devices and to check the RF resistance values that we might be expected to obtain concurrent with the required 0.2 pf capacitance.   The Q of the capacitors could be inferred from the circuit operation.

Both planar and mesa etched PIN diodes were processed on epitaxial N/N+ wafers where the N resistivity was > 200 ohm cm.   The mesa diodes and MOS capacitors with values of 0.4, 0.8, 1.6, 3.2 and 6.4 pf were mounted and bonded in a package with five control terminals as shown in Figure 2.   These arrays were sent to Zeta Laboratories for evaluation.
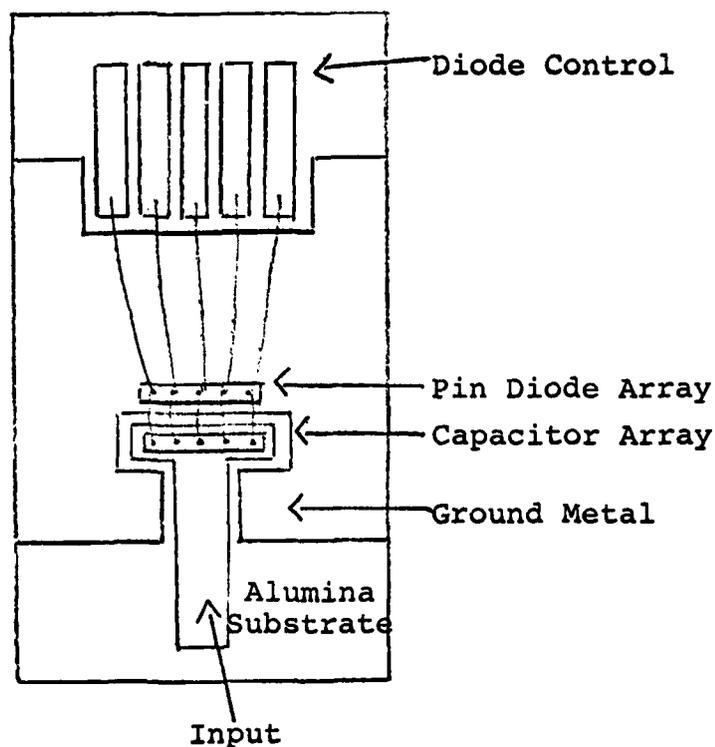

Figure 2

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A. First IC Design

While these units were being evaluated, the initial monolithic circuit was designed. It employs lateral PIN diodes and MOM capacitors all processed on a high resistivity N type silicon wafer rather than the epitaxial N/N+ wafers used in the preliminary evaluation. The cross section of a typical lateral PIN diode is shown in Figure 3.
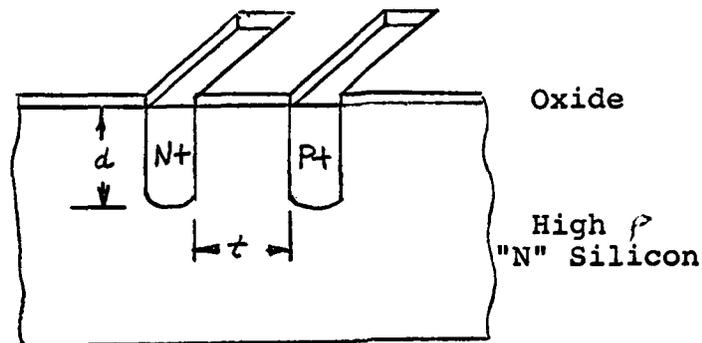

Figure 3

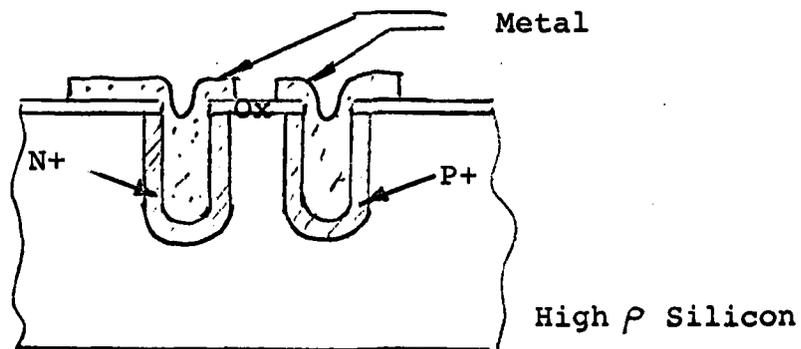An alternate process is to etch wells in the silicon prior to P+ and N+ diffusion as shown in Figure 4.

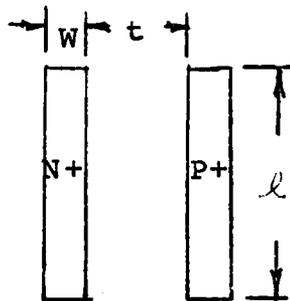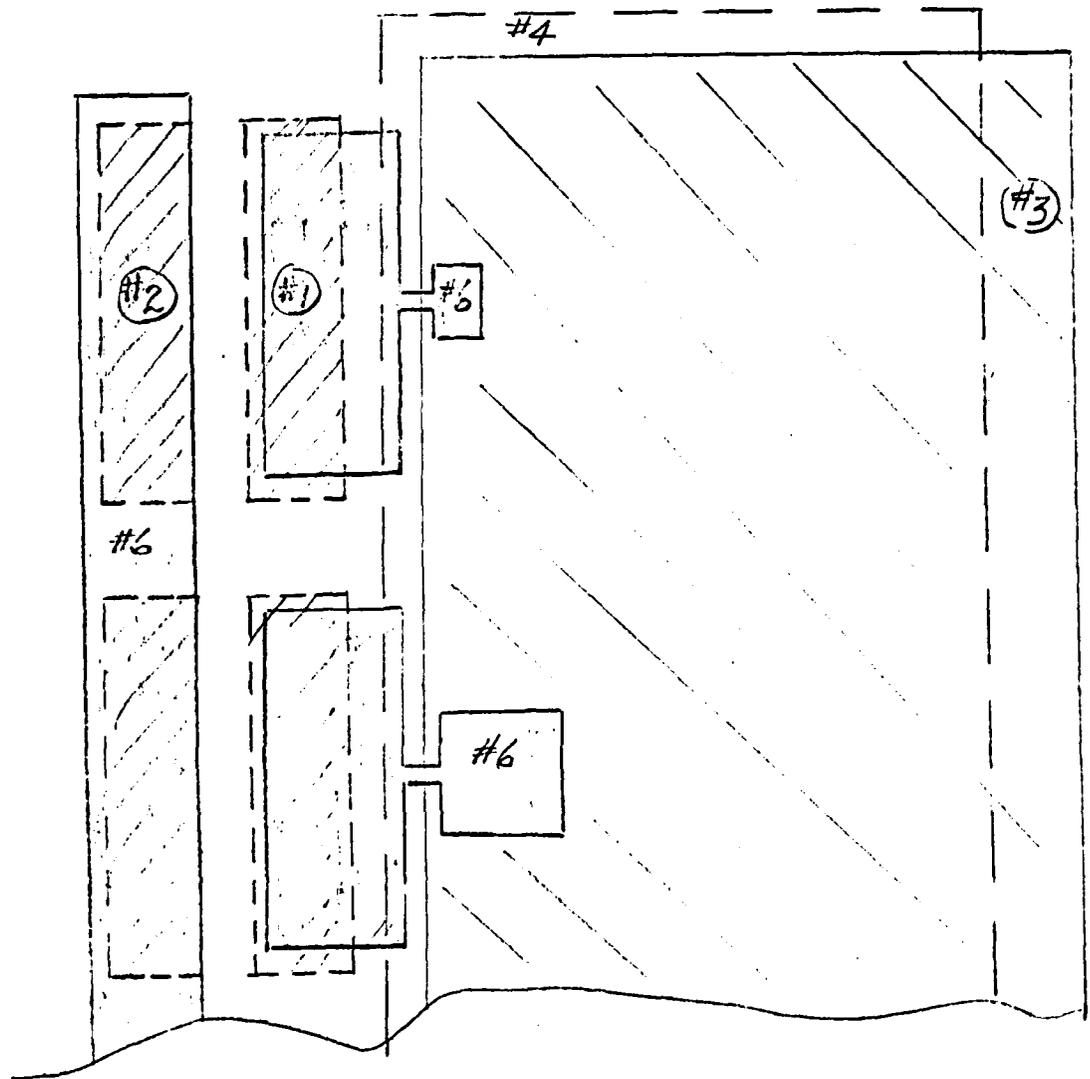Figure 4

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The top view of the diode is shown in Figure 5.

Figure 5

The capacitance and resistance of the PIN diode are
dependent on the active area, the i layer thickness (t)
and the lifetime in the silicon. The length of the diode
(ℓ) was fixed at 20 mils and the width (w) at 5 mils, while
3 i layer thicknesses 1.6, 2.0, and 2.4 mils were selected
to check the effect on diode characteristics. The diffusion
depth (d) can be varied to change the area of the diode.
This design using a high resistivity silicon substrate was
selected for two reasons. The bulk high resistivity silicon
can be obtained with a higher lifetime and resistivity than
epitaxial material which should reduce the resistance of the
PIN diode and improve the isolation between the diodes and
capacitors in the circuit.

The capacitor areas are designed to use either an Al_2O_3
or SiO_2 dielectric layer. The capacitance for 5000 $\overset{o}{A}$ of
Al_2O_3 or 11,000 $\overset{o}{A}$ of SiO_2 is approximately 0.1pf/mil^2. The
areas of the top plates of the capacitors were calculated to
yield the desired capacitances of 0.125, 0.25, 0.5, 1.0, 2.0,
4.0, 8.0, 16.0, 32.0 and 64.0pf. The top view of two of the
units is shown in Figure 6. The chip size is 57 by 258 mils.

#1 P+ Well
#2 N+ Well
#3 CAP Plate
#4 Dielectric
#6 Top Metal

Figure 6

Resistors were not included in the first design. A
package to contain this array was also designed. It
consists of a gold pattern plated onto an alumina sub-
strate. This package is pictured in Figure 7.

ALUMINA
SUBSTRATE
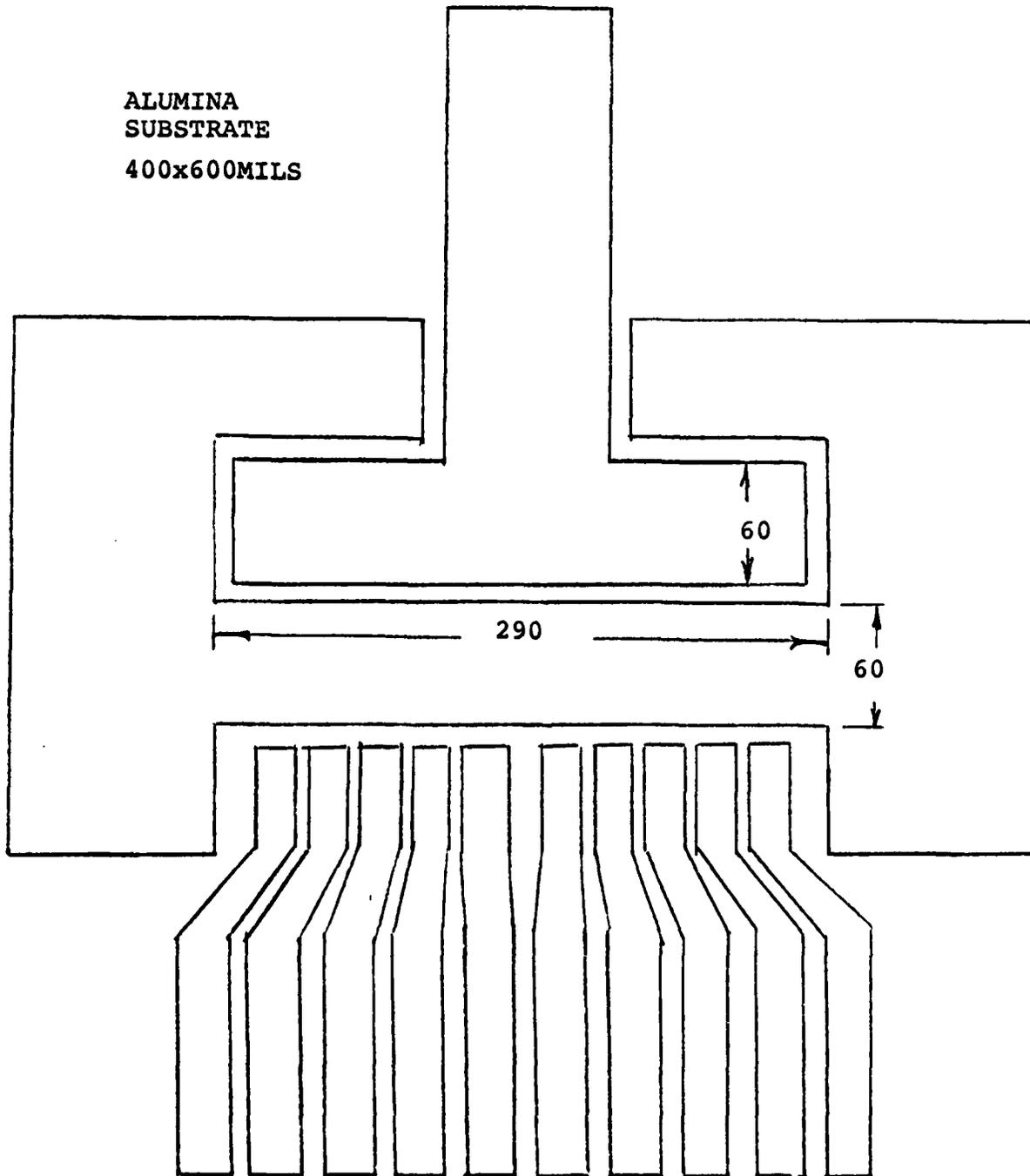400x600MILS

60

290

60

Figure 7

The initial effort was directed toward process development for this circuit. A method was devised for uniformly etching the P+ and N+ holes to a depth of 0.6±0.1 mils. Following the P+ and N+ diffusions the wells were metallized and gold plated. This was followed by deposition of the bottom capacitor plate, followed by either CVD silicon dioxide or sputtered alumina and top metal to contact the P+ and N+ areas as well as formation of the top capacitor plate. A cross section of one of these devices is shown in Figure 8.
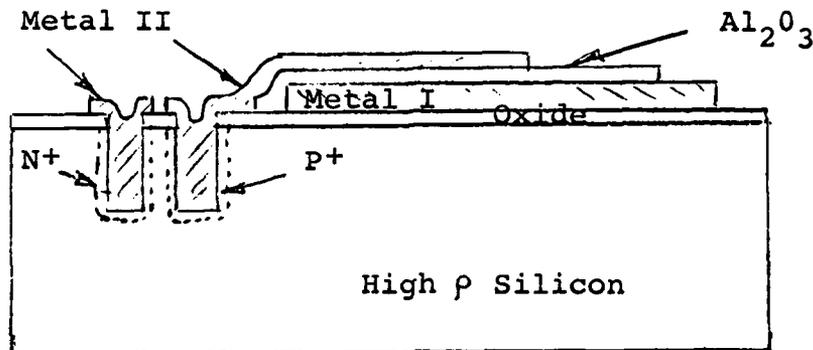
Figure 8

B. Second IC Design

While this process development was being completed, the filter operation of the discrete PIN diode array was being evaluated at Zeta Laboratories, Inc. Their report indicated that the diodes made on epitaxial n/n+ wafers and the MOS capacitors had high parasitics i.e. high parasitic diode capacitance and low Q capacitors. In addition the overall parasitic capacitance of the array was 7.3pf, approximately twice the design goal. About half of this capacitance was calculated to be due to package leads and the area which the array is mounted on. Because of these results, another IC mask was designed using only a five diode capacitor array to

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insure better yield and give the option of two types of
lateral diodes--one with the original rectangles and one
with a circular design. The area of the rectangular diodes
was also reduced by halving the length and reducing the
width to 1.5 mils from 5 mils. Capacitance readings on the
initial IC diodes indicated that the width as well as the
length and diffusion depth of the P+ area affected the
capacitance even when the well was etched prior to diffusion.
Therefore, the circular diode was also included in the second
design to take advantage of the full perimeter of the P+ area.
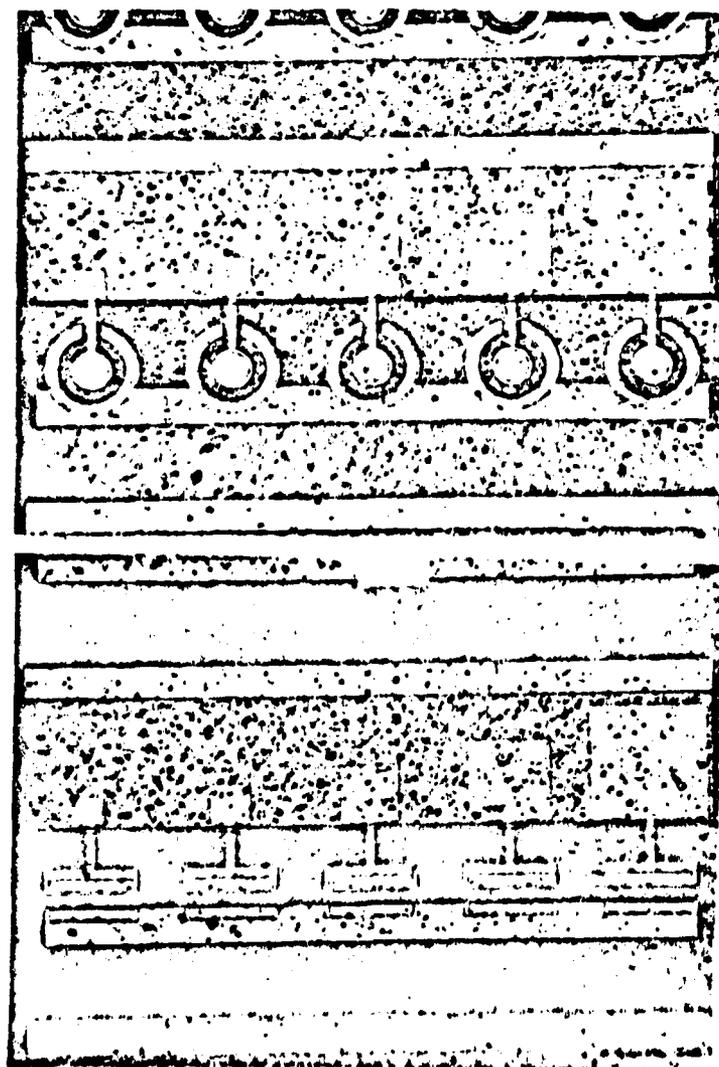Two completed arrays are shown in Figure 9.

Figure 9

All P+ areas are 15.2 mils^2 and the P-N spacing is 1.0, 1.4 and 1.8 mils. The capacitor values were chosen to be 1,2,4, 8 and 16 pf. The five device chip size is 40 x 85 mils.

As soon as these new masks were received fabrication was started using the processes which were developed for the ten diode array. Using high resistivity n type silicon the planar diode shown in Figure 3 was diffused and the diode contacts were silicided using platinum. Then the capacitor plate metal was defined and sputtered alumina was deposited for the capacitor dielectric. This was followed by de-position and etching of the top metal pattern. Following back etching to thin the wafer, additional holes were etched beneath the diode area. A cross section is shown in Figure 10.
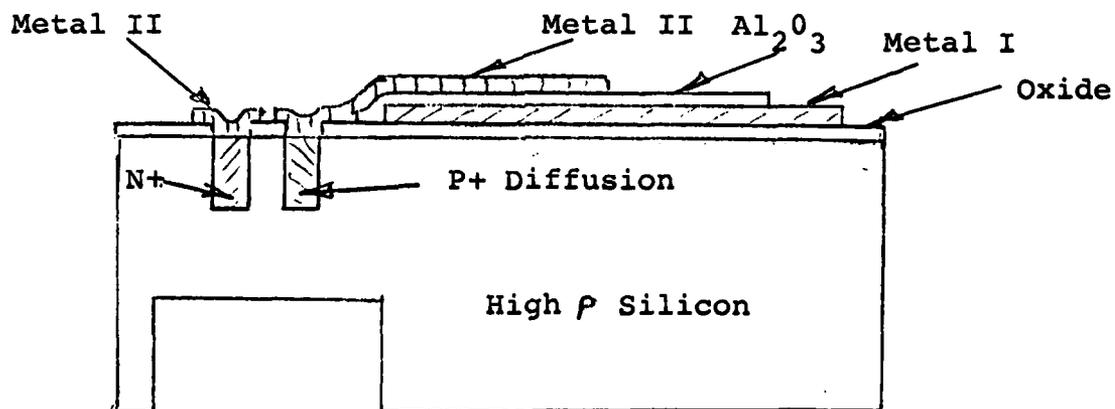

Figure 10

Some typical capacitor values are shown in Table 2. These values indicate that there is a constant capacitance in parallel with each capacitor. Assuming a constant value of 0.65 pf and subtracting it from the observed reading, Table 2 indicates that the designed and calculated values would then be in agreement.

TABLE 2

CAP	PF	(pf - 0.65)	Re-Calculated Ratio	Designed Ratio
1	1.40	.75	1	1
2	2.12	1.47	1.96	2
3	3.66	3.01	4.01	4
4	6.76	6.11	8.15	8
5	14.0	13.35	17.8	16

We can also observe from this table that the observed corrected capacitances are lower than expected. Since the alumina thickness was measured as 5000 Å, this means that the dielectric constant is only 7.5 instead of the assumed 9.0. Resistance readings were read on a Boonton bridge and they were in the 100,000 ohm range which is lower than expected.

When the diode capacitances were measured, we observed that the readings varied depending on which MOM capacitor they were connected with. Some typical values are shown in Table 3 with the capacitors connected and disconnected.

TABLE 3

Bar Diode (1.0 mil Space)	Capacitance Pf @-2V	Diode Capacitance with Capacitor Disconnected
1	0.915	0.379
2	1.438	0.421
3	2.314	0.425
4	3.845	0.418
5	6.189	0.391

Dot Diode (1.0 Mil Space)		
1	0.855	0.273
2	1.772	0.276
3	2.552	0.268
4	5.500	0.280
5	7.442	0.259

Even though the diodes in Table 3 have the same area, the circular diodes have lower capacitance. Other typical capacitances were also measured relative to the substrate. For example, the bottom capacitor plate/substrate capacitance was 15.5 Pf with diodes attached and 10.5 Pf with diodes disconnected. Since these high parasitic capacitances were observed, discussions were initiated with Zeta Laboratories, Inc. to see if circuit changes could be made to evaluate these arrays. Dr. Ho suggested reversing the input and groung terminals as shown in Figure 11. This required reversal of the P+ and N+ diffusion wells for the PIN diode. In addition to doing this, we also processed some wafers with a modified metal pattern which disconnected the previous common diode ground as shown in Figure 12. Seven of these monolithic circuits were sent to Zeta Laboratories for evaluation. Despite all the changes which were made, the circuits still did not perform. Therefore, in order to meet the contract requirements a decision was made to separate the diodes and capacitors by fabricating them on separate silicon wafers.
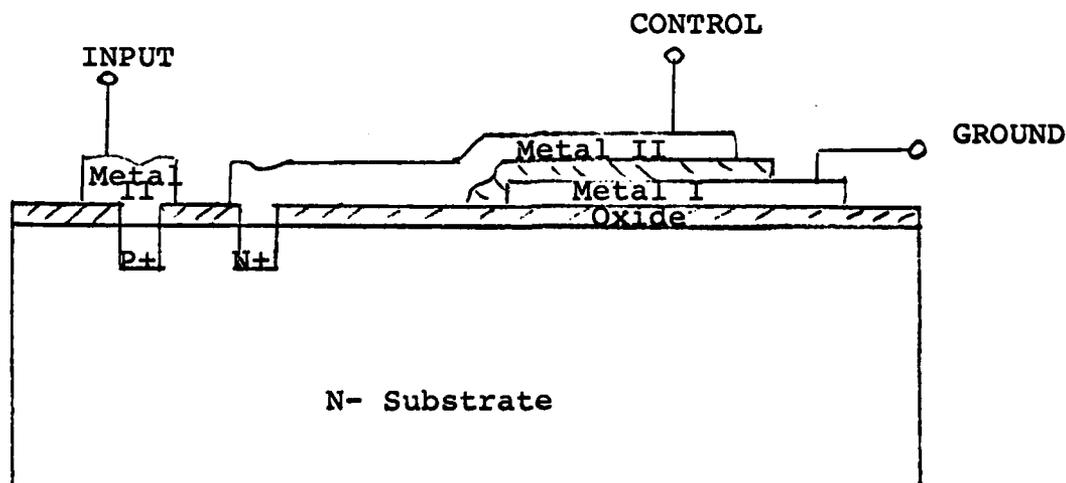
Figure 11

12
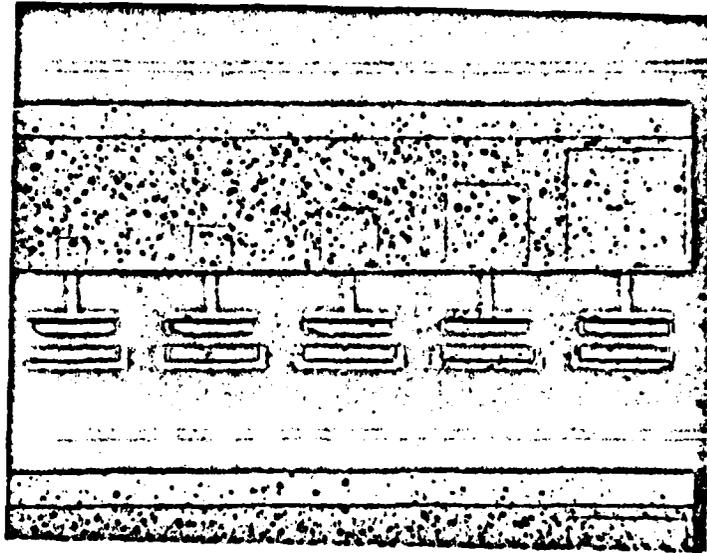
Figure 12a

Figure 12b

13
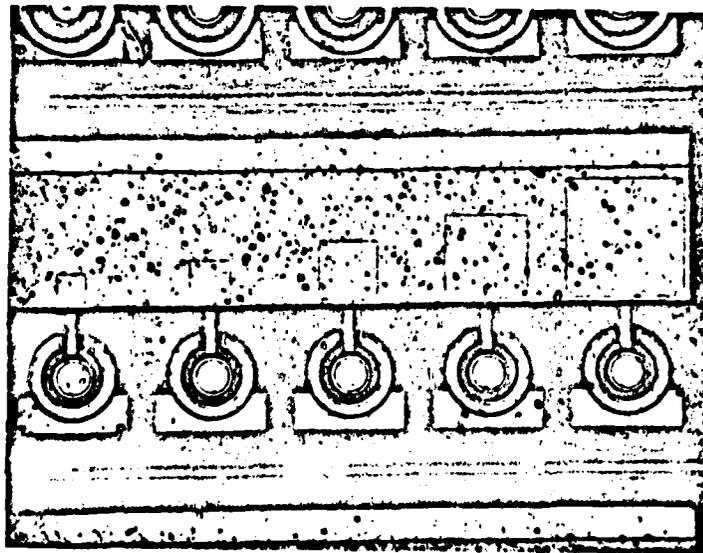
C. Hybrid Circuit

Some capacitors were fabricated by anodizing an aluminum film which was evaporated onto a silicon wafer and then evaporating and patterning the top aluminum plate on film. Some of these capacitor readings are shown in Table 4. The resistance of these capacitors was higher than that obtained with the sputtered alumina, but not all wafers exhibited these values.

TABLE 4
Typical Capacitor Wafer P-1 Readings

Capacitance (pf)	Resistance (Ohms)
31.3	500K
15.2	600K
7.3	800K
3.5	800K
1.7	800K
17.0	800K
7.9	1000K
4.0	1500K
2.0	1500K
0.96	1500K

Diodes were fabricated on 4000 ohm cm N type silicon wafers by double diffusion. A mesa diode is shown in Figure 13; planar diodes were also processed.

Figure 13

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The initial wafer was thinned to approximately 7 mils and then a 4 mil hole was etched into the back side in order to reduce the i region thickness to ∿3 mils.

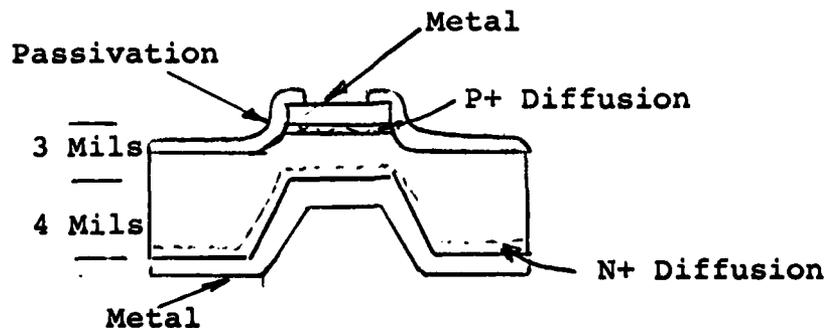Six sizes of diodes were patterned using the original discrete diode masks. Due to the mask layout a five diode array of identical sizes could not be obtained. They could only be cut into arrays having 2 sizes. These were 3 and 4 mil diameter dots, 5 and 6 mil diameter dots and 7 and 8 mil diameter dots. Typical capacitance readings for these diodes ranged from 0.03 to 0.15 pf for the smallest to largest diodes. Although these values are well within the specification for the capacitance, DC measurements of the forward resistance indicated that the RF resistance would be high. In order to check this, three diode-capacitor arrays were mounted on the five conductor package. Two of the capacitor arrays had anodized aluminum dielectric while the third array was made with the original sputtered alumina. Evaluation of these circuits still indicated a high RF resistance and low capacitor Q.

Therefore, the next diodes were processed with larger active areas and a source of high Q capacitors was located at Dielectric Laboratories, Inc.. However, as these capacitance values increase so does the size of the capacitor; this limits the number of capacitors which can be mounted in the 10 lead package shown in Figure 7 where the mounting areas is only 270 mils long. The 16 pf capacitor can be as wide as 40 mils, and the 8 pf - 30 mils. Therefore, this limits the package capacity to 6 devices using 0.5, 1,2,4,8 and 16 pf capacitors. Attempts to fabricate high Q parallel plate capacitors were unsuccessful and this is the only method available to reduce the area occupied by the larger capacitors.

Before combining these diodes and capacitors into the array, a method was devised to measure the diode RF resistance at the NADC laboratory. The chips were mounted on a 1/4 x 1/8 x 1/8 inch alumina block which was metallized as shown in Figure 14.

Metallization
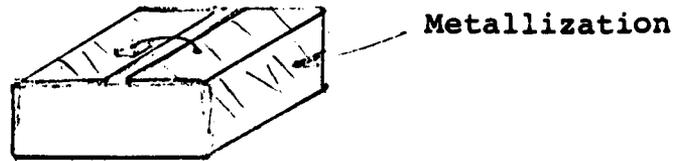
Figure 14

The test fixture was mounted in a Boonton 34A Coaxial line and effective series resistance (ESR) for the diode and the test fixture was measured.

Results obtained from NADC are shown in Table 5.

TABLE 5

Fixture Number	ESR @ 20 MA	ESR @ 40 MA	ESR @ 60 MA	ESR @ 90 MA	Status
1	*				*
2	–	3.35			
3	3.39	2.35			*
4	0.98	.69	.58		
5	2.4	1.59	1.03	.86	*
6	3.46				
7	–	1.34			
8	4.13	2.19	1.55		
9	–				*
10	2.6				*
11	3.96				
12	4.11				*
13	4.27				
14	–	2.51			*
15	–				
16	1.97	1.225	.966	.772	
17	–				
18	3.64				
*	Destroyed				

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The results in Table 5 reveal that units 4,5,7,10 and 16 exhibit the lowest resistance. Even though they are much higher than required, some trends can be determined from these results.

1. Unit 4 has an i region $= 48 \, \mu$.
   All other units are 90-95 μ.

2. Units 7 and 16 are 12 mil squares.
   All other units are round.

3. Units 5 and 10 have the largest diameter
   of the round devices - 15 mils.

4. All remaining units have a diameter of 11 mils
   or less.

5. All units except 5 and 10 met the 0.2 pf or lower
   capacitance specifications.

6. All of these units were diffused into high resistivity
   silicon.

The forward biased i region resistance may be calculated from the following equation:

$$R = \frac{W^2}{2 \, \mu_{AP} \, \tau \, I_o} \qquad (1)$$

We note that the resistance increases as the square of the i region thickness and is theoretically independent of area. However, as the area is reduced, the lifetime decreases because recombination occurs more rapidly at the closer perimeter of the smaller device. Processing and increased current density may also decrease the lifetime. Thus we see that many factors must be optimized to obtain minimum diode resistance. As the diode area is increased and the i region thinned to reduce resistance, the diode capacitance will increase. The measured

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RF resistance is the sum of the diode resistance plus the contact and bulk resistances of the P+ and N+ regions. Therefore, when the diode resistance is minimized it must be combined with the lowest possible bulk and contact resistances including mounting and bonding effects. In order to check the validity of the conclusions reached from the data in Table 5, a lot was then processed using the largest available square pattern (14 mils). It was diffused from both sides to leave a 35-45 μ i region. The yield was not too high on these devices because a hole approximately 2 mils thick has to be etched into the back of a 5-5.5 mil wafer in order to get the required i region. The hole has to line up with the P+ diffusion in the top side and it also makes the wafer fragile. The finished device is similar to that shown in Figure 13, except that it is square rather than round and the overall wafer thickness is less.

Resistance and capacitance readings for some of these devices are listed in Table 6.

TABLE 6
Resistance in ohms at

Wafer	Unit	23ma	48ma	72ma	97ma	Capacitance pf
DZ4-1	1	1.43	0.98	0.82	0.72	0.39
	2	1.48	1.16	0.86	0.75	0.28
	3	1.61	1.21	0.95	–	0.27
DZ4-3	4	1.24	0.88	0.75	0.65	0.35
	5	1.16	0.8	0.67	0.61	0.30
	6	1.03	0.69	0.59	0.51	0.35

The calculated i region width for DZ4-1 is 40-45 μ and for DZ4-3 is 35 μ. The length of the diode active area is 12.4 mils. These resistances read on a new style of test fixture were still excessively high; probably due to the processing and handling difficulties of the thin wafer required to obtain a 40 μ i region; therefore, a decision was made to use high resistivity epi of thicknesses 35, 45 and 55 microns and a

square active area for the next devices. Four sizes of squares were selected with areas of approximately 500, 400, 300 and 200 square mils. The larger sizes will be used to reduce the diode and contact resistances even though the capacitance will be increased above 0.2 pf. While the silicon wafers and masks were being manufactured, some devices were processed on available epi wafers 200 ohm-cm and 14 microns thick. A 14 mil square mask and 12 mil diameter circular mask were used. These devices were processed to work on process improvements to increase yield and reduce contact resistances. A chip from lot DZ7 exhibited a lower resistance as shown in Table 7, however, due to the thin i region, the capacitance is high, approximately 1.2 pf.

TABLE 7
Typical DZ7 Diode Resistance

Current	RF Resistance (ohm)
10 ma	0.75
20 ma	0.42
60 ma	0.31

Some chips from this wafer were mounted on the 10 connector packages along with six capacitors from the Dielectric Laboratories with values from 0.5 to 16 pf. These were sent to Zeta Laboratories for evaluation. Further tests on these circuits indicate that the mounting and bonding of the chips is also contributing to the performance degradation.

The resistances from Table 7 are plotted in Figure 15 as a function of $1/I$. The intercept of a plot of diode resistance vs $1/I$ should equal the total combined contact and bulk resistances of the P+ and N+ regions. This is 0.25 ohms for DZ7 and is lower than any value obtained on the previous diodes.
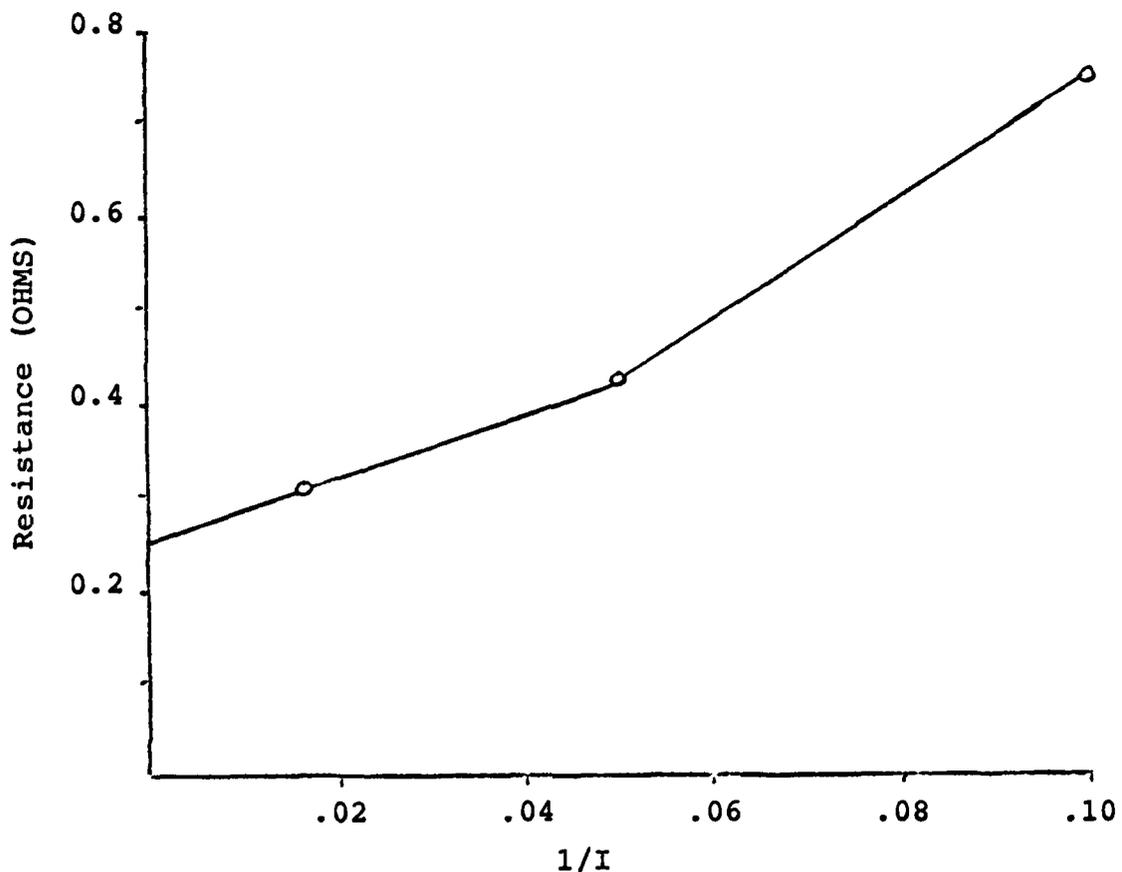
Figure 15

Some typical resistance readings obtained from the first wafers processed with the new multi area mask and epitaxial silicon are shown in Figure 16. Back contact problems were encountered on these wafers and this is indicated by the high value of the intercept resistances 0.3 - 0.4 ohms. The reduction of resistance by increasing diode size is shown on these curves.

A wafer was then processed using the following sequence:

1. Starting material - N/N+ 52 μ > 250 ohm-cm
2. Implant Boron and anneal
3. Form Platinum silicide on P+
4. Deposit and pattern P+ metal, electroplate gold
5. Mesa etch diodes
6. Passivate diodes
7. Thin wafer from N+ side
8. Deposit back contact metal and sinter
9. Saw diodes into matching pairs.

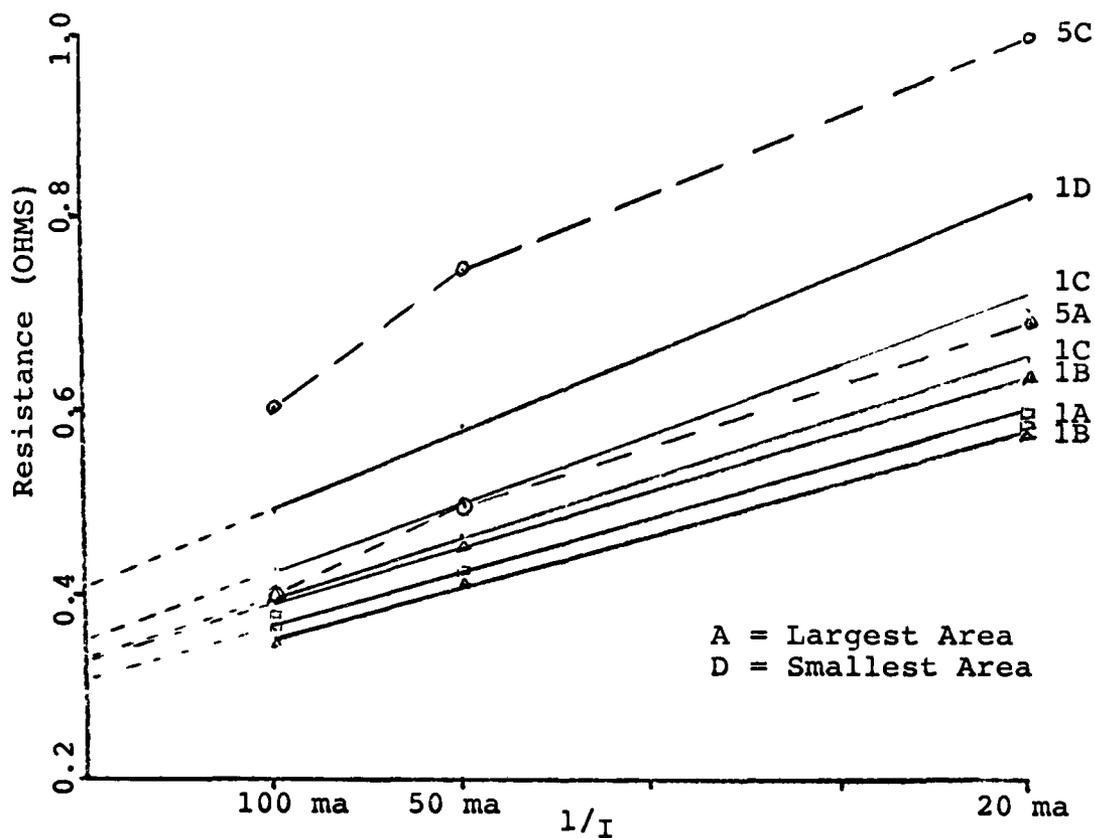Diodes from this wafer were used in the final Pin-Diode-Capacitor arrays.

Figure 16

A = Largest Area
D = Smallest Area

The assembly process was changed and the diodes were mounted with eutectic gold solder rather than silver filled epoxy. Twenty five of these diodes arrays containing six diodes and capacitors each have been mounted on the ten lead package for circuit evaluation. This completes the contract. requirement for delivery of 30 total circuits.

III. CONCLUSIONS AND RECOMMENDATIONS

Due to the high parasitic capacitances of the monolithic PIN diode-capacitor array, the original concept of a monolithic circuit had to be abandoned. The use of alumina as the capacitor dielectric also did not give a sufficiently high Q capacitor for the application. Therefore, a hybrid approach was required. After preliminary process work a diode mask was designed with varying sizes of square patterns. These diodes were processed on high resistivity epitaxial N/N+ wafers. The processing experiments were directed towards reducing contact resistances and maintaining lifetime in the diode. However, the goal of obtaining 0.2 ohm RF resistance with 0.2 pf diode capacitance could not be met. Instead the acceptable capacitance was raised to 0.5 pf and a best effort was made to reduce the resistance to 0.2 ohms.

The diode chip is 40 mils square, therefore 10 diodes will no longer fit into the package designed for the diode-capacitor array. Only six diodes will fit into this area. In addition, the commercially available Di-Caps® from the Dielectric Laboratories are 40 mils wide when they exceed 12 pf; therefore the only way to obtain the required 10 pin diode-capacitor array would be to increase the package size.

Improvements might be made in the diode characteristics through the use of high resistivity n type silicon for the i layer rather than epitaxially deposited silicon. Although

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we tried using this type of material by selectively thinning
the diode area and diffusing or implanting the P+ and N+
contacts, this process was very difficult to control and the
diffusions probably degraded the quality of the silicon.
An alternate process would be to epitaxially deposit the N+
layer followed by thinning the i region to the desired
thickness. Then the i side could have a P+ layer epitaxially
deposited, implanted or diffused. Implantation is preferable
to diffusion. When the implanted P+ is used, it would be
desirable to pulse anneal the implant to minimize the time
at elevated temperatures which degrades the bulk character-
istics of the high resistivity i region.

All of the capacitors might also be fabricated on a common
plate by using the proprietary Hi Q dielectric and then
forming the desired capacitors by varying the sizes of the
top plates. Then we could have all of the diodes on one
chip and all of the capacitors on a single plate. This would
facilitate assembly and assure that the diodes are matched.
The bonding must be done with wide ribbon wire to reduce this
source of resistance. The package should be designed in
conjunction with the filter circuit. If these changes are
implemented, then the circuit performance should be greatly
improved.