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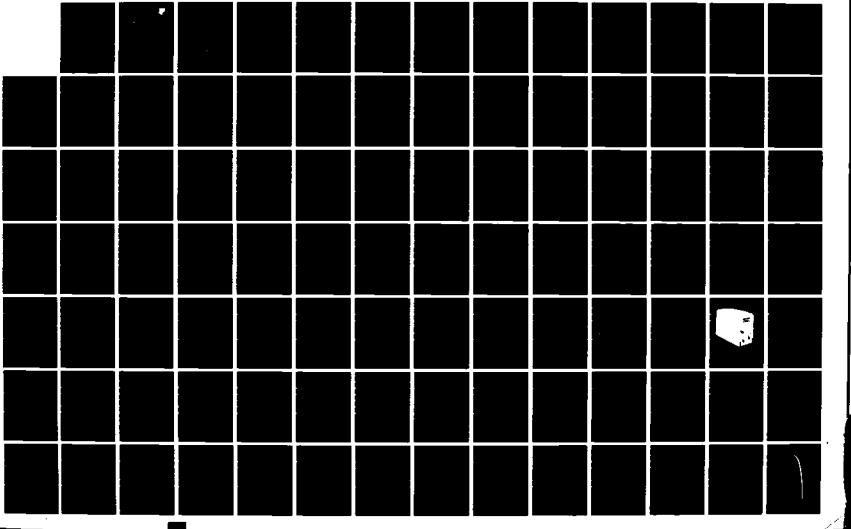

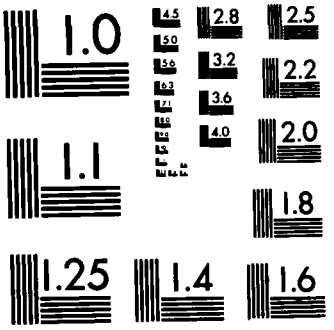

RADC-TR-82-280
Final Technical Report
November 1982

SOLID STATE EMC TECHNOLOGY DEVELOPMENT

Magnavox

John G. Mohr
Richard W. Stroud

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ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Critical superheterodyne receiver parameters were studied and evaluated to extend the dynamic range and reduce the spurious responses of UHF receivers operating in a high-level RF environment.

An up-conversion receiver front end using a surface acoustic wave filter for initial IF selectivity was assembled and evaluated.

A single conversion receiver was evaluated using high-level, low-distortion

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elements. Also, a low-noise, high-level, synthesizer/VCO was designed for receiver local oscillator injection and transmitter frequency excitation.

A solid state transmitter was modified to minimize the spurious output and broadband noise levels. A solid state demonstration receiver/transmitter suitable for airborne testing was assembled using the optimized circuits and electrical tests were made on the completed transceiver.

Sensitivity of the receiver with -95 dBm specification input signal was maintained at better than 10 dB over the 225 to 400 MHz band with an interfering signal of ±15 to +25 dBm displaced 2% f_o from the center frequency.

Transmitter output was maintained at 10 watts minimum over the 225 to 400 MHz range with minimized spruious responses and broadband noise.

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT)

LIST OF FIGURES

LIST OF FIGURES (CONT)

LIST OF TABLES

LIST OF TABLES (CONT)

SECTION I
INTRODUCTION AND SUMMARY

The goal of the EMC Technology Design contract was to extend and advance the solid state transmitter/receiver designs developed on prior RADC study contracts F30602-76-C-0076, F30602-79-C-0145, and F30602-78-C-0228, and to integrate these designs into a complete transceiver that has advanced EMC capability. The resulting experimental radio set will serve as a vehicle for test and evaluation in the dense airborne C^3 electromagnetic environment and will provide a baseline transceiver for future EMC radio designs.

The work under this contract included the engineering study and investigations necessary to develop new techniques for improving the transmitter spectral purity and receiver susceptability performance of UHF solid state radios.

The study phase of this program included VMOS, LSI, and synthesizer technology and their applicability to circuit design techniques resulting in improved EMC characteristics. Primary emphasis was placed on determining optimum circuits for reducing transmitter broadband noise and spurious outputs and on improving solid state receivers in the areas of out-of-band interference handling capability, cross-modulation performance, and spurious responses.

An experimental model transceiver was built using the optimized circuits derived from the study phase of the contract. This transceiver was designed to meet the requirements of the statement of work and to operate in an airborne environment.

Extensive data was taken on the experimental model radio, especially in the area affecting its compatibility in an environment which includes co-located highly sensitive receivers and high-power transmitters. This data shows that performance of the Experimental Model EMC Technology Transceiver, operating in such an environment, would be superior to conventional solid state radios.

Signal-to-noise ratio of the receiver over the 225 to 400 MHz band with an input of -95 dBM, modulated 30 percent at 1000 Hz, was 12.5 to 15.5 dB. A 10 dB signal-to-noise ratio was maintained over the band while being jammed by a 30 percent modulated, (400 Hz) interferring signal at 2 percent of center frequency, at a level of +16.5 to 24.9 dBM.

A total of three receiver spurious responses were found at five test frequencies. These three responses were well within the required limits. Receiver image rejection is -77 to -110 dB.

Transmitter output exceeded 10 watts at all frequencies. Broadband noise output of the transmitter was at or below the requirements of Statement Of Work for all test frequencies within ±15 MHz of center frequency. Beyond ±15 MHz, the broadband noise did not exceed 6 dB above the specification limit with the level at most frequencies well-below the specified level.

Other than close-in power supply switching frequency harmonics, a maximum of two low-level spurious responses were found each side of the transmitted carrier.

SECTION II
ENGINEERING STUDY PHASE

The study phase of the contract was directed at investigating specific areas of receiver design, transmitter design, and synthesizer/VCO design as related to their impact on the overall EMC characteristics of an airborne transceiver. Some of the studies were continuations of investigations that were conceived or started, but not completed, in prior RADC study contracts.

In the following paragraphs the highlights and results of the studies are described.

RECEIVER STUDIES

Stacked Varactor Tuned Filter

In any varactor tuned filter, the power handling capability of the filter is limited by the magnitude of the peak RF voltage relative to the applied DC tune voltage. Two undesirable effects occur. First, because of the non-linear characteristic of varactor diodes, high-level signals will produce undesired third order intermodulation products in the receiver passband. Secondly, if the levels are sufficiently high to cause the diodes to be forward biased, a DC error voltage results and causes the filter to be detuned. To overcome this phenomena, a filter was constructed where several varactor diodes were stacked in series. The principal was that the RF voltage would be evenly distributed across each diode and, thereby, reduce the likelihood of reaching a sufficiently high-signal voltage to cause rectification.

The filter design was a three-pole unit using 12 stacked diodes for control of each of the tuned circuits. This filter had acceptable insertion loss and would pass +20 dBm signals without rectification. A problem did occur as a result of the inductive coupling system used in an

attempt at maintaining a constant bandwidth. A return about 60 MHz below the resonant frequency of the filter was noted which was only about 40 dB below the desired response at center frequency.

The tuned filter approaches were abandoned in preference to a PIN switched wideband filter approach for the experimental model receiver.

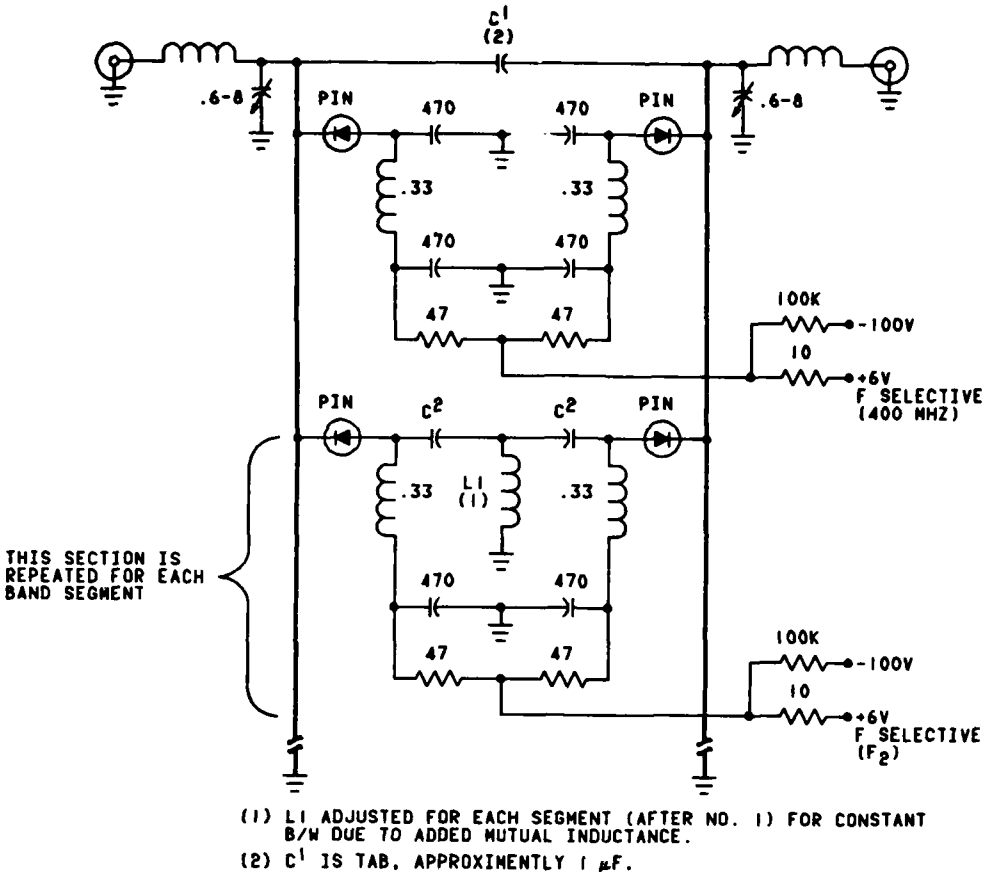
Diode Switched High-Level Filter

One of the problems associated with varactor tuned filters is the limited power capability of such a unit, usually being limited to a few milliwatts. A filter was designed and a prototype constructed and evaluated which used power PIN doides, rather than varactor diodes, as the control elements. The PIN diodes, when commanded, shorted segments of a high Q-inductor to ground, as shown in Figure 1, to become a tuned quarter wave line.

The upper set of diodes in Figure 1 control the highest frequency of interest, such as 400 MHz. The L/C network at the input and output connectors match the filter to the 50-ohm line and sets the initial resonance point. C1 sets the bandwidth of the highest frequency band segment.

To proceed to the next lower band the first set of diodes is highly back biased to prevent conduction and the next lower pair of diodes, which are strategically placed, are forward biased. L1 is then adjusted to maintain the same bandwidth as the first filter section. This system is repeated for each band by turning on the proper diode pair and back biasing all diodes above them.

The limitations are the physical line length and the critical location of the shorting diodes for proper band overlapping.



(1) L1 ADJUSTED FOR EACH SEGMENT (AFTER NO. 1) FOR CONSTANT B/W DUE TO ADDED MUTUAL INDUCTANCE.
(2) C^1 IS TAB, APPROXIMENTLY 1 μF.

Figure 1. Diode switched high-level filter

The filter is capable of handling a power of several watts as the shorting PIN diodes are at the low-voltage points of the active line section and all other diodes are reverse biased at -100 volts. The power capability is limited only by the current capability of the active diodes and by the breakdown of the variable trimmer capacitors.

The prototype built covered 345 to 400 MHz in three band segments with a nearly constant bandwidth of 16 to 20 MHz. Insertion loss was 0.6 to 0.8 dB and VSWR through the filter was no worse than 1.6:1. The output power of the ARC-164 radio, 10 watts nominal, was operated through the filter with no heating or ill effects.

This filter approach looks very promising, although the diode control circuit would be somewhat complex for complete 225 to 400 MHz band coverage. The entire band could be covered with multiple switched filters.

High Power, Low Noise, FET and Bi-Polar Amplifiers

It is known that in any high-level receiver design, any front-end amplifier stage must be able to amplify all incoming signals within the passband of the system linearly until they can be further filtered in a following stage. Without good linearity, third order products are generated which cannot be later filtered. For this program, receiver front-end amplifiers or any amplifier following the first mixer prior to appropriate selectivity must be able to handle input signal levels of up to +20 dBm. A further requirement is that these amplifiers must have low-noise figures as their noise contributes directly to the receiver noise figure.

Several devices, both FET and bi-polar, were evaluated for use as RF or IF amplifiers during the study phase of the program. Among these were the MRF 5174, MWA-130, 2N5109, VMP4, CTC 4-28 and LT2001. Of particular interest was the TRW TP491 which exhibited a noise figure of less than 2 dB while operating at a relatively high-collector current of 20 to 25 milliamps. These are normally conflicting parameters. Also the Teledyne Crystalonics CP 643 yielded a good noise figure (4 to 5 dB) with high current and, at the same time, presented a constant resistive input near 50 ohms. This device was eventually used for the 70 MHz IF amplifiers in the experimental model radio and is discussed later.

Conventional High-Level Mixers

In general, the dynamic range of any receiver is limited by the power handling capability of the mixer because this is the first truly nonlinear element in the received signal path. Consequently, to achieve a high-level receiver front end design, it is best to keep any amplification ahead of the mixer to a minimum because this serves to increase the level of the signal that the mixer must handle. If the system noise figure requirements can be met with the mixer as the first major noise contributor, it is an advantage to use no RF amplification.

In general, for best EMC performance, a balanced type mixer is preferable to a single-ended mixer because of the isolation provided between ports. The doubly balanced mixer affords the best performance in this regard.

Currently several manufacturers make double-balanced, ring-diode mixers that are designed for local oscillator powers of up to +27 dBm and are capable of handling input signal levels linearly up to about +20 dBm. It is believed that this type of mixer offers the best compromise between dynamic range, moderate LO power, noise figure, and port isolation.

There are studies currently being conducted by manufacturers of VMOS devices which use VMOS power units as active elements in singly balanced mixer arrangements. Test data on the mixers show that they provide some improvement in the third order intercept when compared to a double-balanced, ring-diode mixer and this type of mixer does provide gain, or at least no serious loss. No known test data exists when this type mixer is operated in the 225 to 400 MHz frequency band.

Based on available data, the doubly-balanced ring-diode mixer is felt to be the best choice for the EMC Technology receiver design because the gain of a VMOS mixer increases the likelihood of degradation due to strong inband interference, and a VMOS singly balanced mixer will dissipate 1 to 2 watts of power.

The double-balanced mixer affords added isolation between ports which translates to fewer spurious responses in the overall receiver. Further, the double-balanced design has demonstrated the capability of meeting the goals of this program by use in previous high-level receiver designs.

Image Reject High-Level Mixer

With both the varactor tuned discriminator rejection system and the broadband input receiver approaches there is an advantage in having additional inherent rejection at the first image frequency. Toward this goal, a customized image reject high-level mixer was purchased from Merrimac

Industries, their part IRM/27104. This mixer was designed for a +27 dBm local oscillator level and was phased for cancellation of the high-side image with the injection frequency 70 MHz above the operating frequency.

Insertion loss of the mixer was about 7.5 dB and the image attenuation varied considerably over the 225 to 400 MHz operating band exhibiting decreasing attenuation of the image with increasing operating frequency. Table 1 details pertinent features of the mixer.

TABLE 1. IMAGE REJECT MIXER DATA

Operating frequency (MHz)	Image frequency (MHz)	Insertion loss	Image attenuation (dB)	LO level at RF port (dBm)	LO level at IF port (dBm)
225	365	7.5	30	-29	-16
230	370	7.5	33		
240	380	7.4	36		
250	390	7.5	34	-27	-14
260	400	7.5	36		
270	410	7.5	35		
280	420	7.5	33		
290	430	7.5	28		
300	440	7.5	27	-20	-20
310	450	8.0	26		
320	460	7.6	23		
330	470	7.8	20		
340	480	7.5	19		
350	490	7.5	16.5	-17	-15
360	500	7.6	15		
370	510	7.6	13		
380	520	7.6	12		
390	530	7.7	10		
400	540	7.6	9	-15	-15

NOTE: Merrimac IRM/27014 mixer with +27 dBM local oscillator injection

This mixer also showed a rejection of 43 dB to the 70 MHz IF frequency.

Although this mixer has little rejection at the higher frequencies, it could be used in conjunction with a low-pass antenna filter, as normally used in a receiver/transmitter for transmitter harmonic rejection, for overall image rejection. Such a filter for UHF operation normally cuts off sharply at about 440 MHz.

First Mixer Harmonic Spurious Generation

It was found that the high-level mixers used with various breadboard receivers generated a very high-level signal on the "R" (RF input) port which was a harmonic of the applied local oscillator signal. The LO frequency was multiplied by the diodes in the mixer, and, because the harmonics were outside the operating range of the mixer, little balancing suppression was afforded to the harmonic frequencies. By specifying a mixer which is balanced to the higher frequencies (2000 MHz or above) the harmonic level is reduced.

"R" port levels for a typical mixer with +27 dBm LO input (Merrimac DM-8) are shown in Table 2.

TABLE 2. FIRST MIXER HARMONIC GENERATION

LO frequency (MHz)	"R" port level (dBm)
320 (LO)	-16 (43 dB below LO Level)
640 (2 X LO)	-28.5
960 (3 X LO)	-27
1280 (4 X LO)	-17 (44 dB below LO Level)

Because these harmonic signals are of such amplitude and are directly in the RF path to the antenna where they could be reradiated, additional filtering of these signals is required in a modern high-level receiver design.

The demonstration radio described later uses a receiver first mixer (Mini-Circuits SAY-11) which is balanced to 2400 MHz, and also a low-pass filter between the antenna and mixer "R" port to eliminate all LO harmonic reradiated signals.

Discriminator Rejection System

A method of interference rejection was examined wherein a conventional varactor tuned front-end filter is automatically offset to reduce interference from strong off-channel signals. A block diagram of this system is shown in Figure 2.

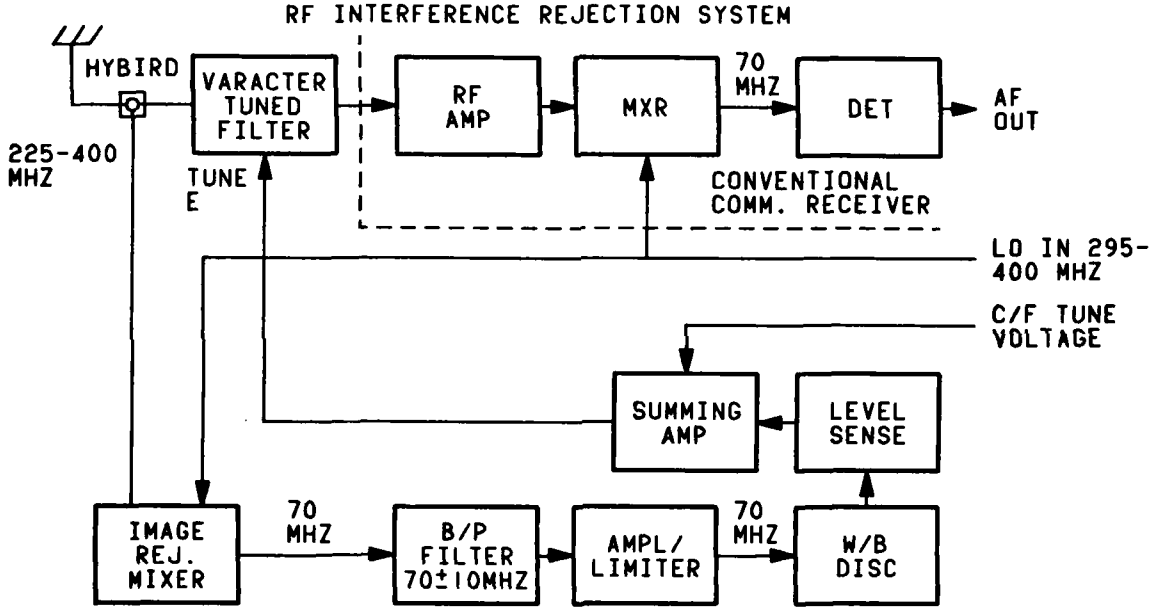


Figure 2. Discrimination rejection system

This system uses a three-pole varactor tuned filter, ideally with a flat nose response of 10 to 12 MHz. The filter is tracked with the passband centered to a nominal frequency/voltage curve.

A second mixer system, using an image reject style mixer is connected to the antenna line, along with the normal receiver input, through a hybrid splitter. Injection for the second mixer is supplied by the receiver synthesis system in addition to the normal receiver mixer requirements. The output of the image reject mixer, centered at 70 MHz, is filtered to obtain a 60 to 80 MHz passband. Any signal derived from the image reject mixer and passing through the filter is amplified and limited. After limiting, the signal is applied to a wideband discriminator, with the DC output proportional to the frequency offset of the interferring signal. This DC output, above a set level, is summed with the center frequency tune voltage to offset the varactor filter away from the interference. The intention was to move the filter passband to the opposite side of center frequency to just include the desired center frequency on the filter slope nearest the interference, thereby dropping the interference down the skirt of the filter.

On-frequency (desired) signals cause no discriminator output and thus the varactor filter passband is centered at the operating channel. Only high-level interference is of interest so no amplification is required ahead of the image reject mixer.

This system was assembled and demonstrated with fair success. The wideband discriminator centered at 70 MHz is a key block in the system and several models were built and evaluated. Bandwidth of these discriminators varied from 6 to 15 MHz on each side of center frequency.

The only problem encountered with the system was in the ability to control the offset of the filter equally at all frequencies due to unequal front-end filter bandwidths. Also with nearly equal amplitude jamming signals on each side of center frequency, the filter could be steered from one interferring signal directly into another. If multiple jamming signals were of the right level, or if the spacing was exact, it was possible to cause the system to oscillate. With one strong signal on either side of center frequency however, a rejection of up to 16 dB could be

achieved. When used with an ARC-164 receiver, this was sufficient rejection to meet the requirements of the statement of work at most frequencies (see Table 3). With an improved filter (steeper skirt response) the SOW requirement could be easily exceeded.

TABLE 3. JAMMING SENSITIVITY, ARC-164 WITH DISCRIMINATOR REJECTION SYSTEM

(-95 dBM) Operating frequency (MHz)	(+20 dBM) Jamming frequency (MHz)	S+N/N sensitivity (dB)
225	220.5	7.6
	229.5	8.4
260	254.8	10.2
	265.2	10.6
300	254.0	11.9
	306.0	12.2
380	372.4	12.6
	387.6	12.1

This system was not used in the expermental model receiver because it was later determined that the goal could be met with less complexity, and also because of the possible problems that could arise with multiple jamming signals.

Up-Conversion Front-End Investigation

Figure 3 is a block diagram of an up-conversion front end that was assembled and evaluated in the course of the receiver studies. The basic approach was to translate the desired signal, after fixed RF input filtering, up to a higher IF frequency where it passed through a SAW filter for further selectivity. All frequencies passing through the passband of the filter (approximately 200 kHz) were down-converted to a standard IF frequency of 70 MHz. This design totally eliminates a varactor tuned front end which can be a source of intermodulation and desensitization.

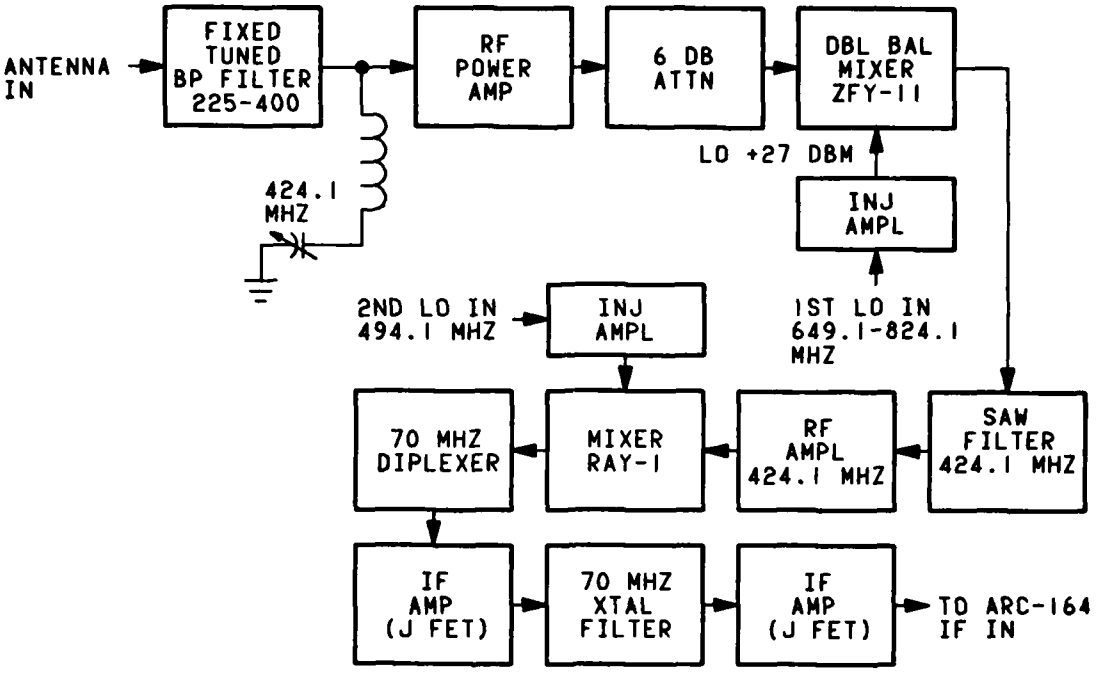


Figure 3. High-level up-conversion receiver front end

This approach has some advantages in the area of spurious signal generation, however, as detailed later, other problems precluded its use for the demonstration radio receiver.

The fixed tuned bandpass filter of Figure 3 is a combination low-pass/high-pass design such that the 225 to 400 MHz band is passed with an attenuation of less than 1.5 dB while the undesired frequencies below and above the band are attenuated sharply. The series tuned trap following the bandpass filter prevents receiver responses at the first IF frequency of 424.1 MHz.

The RF power amplifier following the filter was a power bi-polar device, MRF5174, used only to assure a useable system noise figure. Gain of this amplifier is about 10 dB and noise figure in this application was 4.5 dB.

The amplifier stage was necessary because the losses of the first mixer and SAW filter were cascaded which would result in a poor overall noise figure. The front end was also evaluated with the amplifier placed directly after the first mixer, but the arrangement shown was superior. The 6-dB pad after the RF amplifier terminated the amplifier resistively for improved intermodulation performance and provided a non-reactive input port termination for the double-balanced mixer. The mixer, Mini-Circuits ZFY-11, is a unit balanced for operation to 2400 MHz and was operated with a local oscillator level of +23 to +27 dBm.

Injection for the mixer was first developed by a laboratory generator/ amplifier combination at 649.1 to 824.1 MHz. Receiver noise due to the wideband amplifier was excessive without tuning the output however, and a high-power oscillator (VCO) covering this range was purchased from Texscan (Model VTS-50). This oscillator was phase locked to the signal generator for further testing, but phase noise still influenced the sensitivity level.

The injection noise degrading the sensitivity of the receiver was one of the reasons this system was later abondoned. Also generating the LO frequency "clean" and at a high level in a complete operational radio would be somewhat complex because of the different frequency ranges required for transmit and receive functions, switching associated filters, etc. Output of the first mixer is routed through a surface wave filter to select the desired mixer output signal (424.1 MHz). The SAW filter has internal input and output matching networks for 50-ohm operation. This IF frequency was chosen because it is above the operating band and outside the passband of the front end filter. Also half the operating frequency is below the operating band and therefore harmonics of strong in band signals will not generate spurious responses. The -3 dB bandwidth of the filter is about 200 kHz, the insertion loss is 5 dB, and the ultimate rejection is approximately 55 dB.

After the 424.1 MHz center frequency signal passes through the SAW filter it is amplified by a second low-noise power amplifier (LT-2001) and routed to a second high-level mixer. Injection to this mixer (Mini-Circuits RAY-1) is about +20 dBm at a frequency of 494.1 MHz, or 70 MHz

above the first IF frequency. This LO signal was developed first by a laboratory generator, then by a crystal oscillator/multiplier chain which provided superior results, completely eliminating the second injection noise as a factor in the overall measurements.

The 70 MHz output of the second mixer is routed through a diplexer which resistively terminates the mixer at all frequencies of interest and passes the desired IF frequency on the to the IF stages (CP 643) for amplification. Two similar IF amplifiers are used with an 8-pole crystal filter between them. The CP 643 is a junction power FET which has a characteristic input impedance very close to 50 ohms. This properly terminates the diplexer and crystal filter. Noise figure of the 70 MHz IF stages is about 4.5 dB and gain is 10.5 dB. Output of the last JFET amplifier (and the up-conversion front end) is passed on to an ARC-164 IF system for further amplification, AGC generation, detection, and audio amplification.

Table 4 shows the up-conversion system sensivity with and without jamming and with the first injection signal filtered with a 4-pole Telonic 3 percent bandpass filter.

TABLE 4. UP-CONVERSION FRONT-END SENSITIVITY WITH -95 DBM INPUT

	Amplifier injection no LO filtering		Amplifier injection LO filtered (4 pole B/P)	
Operating frequency (MHz)	No jamming (dB)	+20 dBm, +2% Fo jamming (dB)	No jamming (dB)	+20 dBm, +2% BW jamming (dB)
225	9.5	1.5	13.8	7.0
300	10.6	1.4	14.5	7.2
360	10.8	1.5	14.8	7.2

The up-converter design was discontinued primarily because of the inability to achieve the required clean local oscillator signal, the incompatibility imposed on the synthesizer which requires the transmit signal source to be in the frequency range of 225 to 400 MHz and the receiver

injection in the range of 650 to 825 MHz. Also the SAW filter has a maximum recommended power level which would be very close to the levels expected in this system.

Single Conversion Front-End Investigation

Figure 4 is a block diagram of the single conversion front-end approach using switched tubular bandpass filters for block RF selectivity. With this system, performance is determined primarily by the signal handling capability and noise figure of the double-balanced mixer and IF amplifier directly following the mixer. No RF amplifier or varactor tuned circuits at the incoming RF frequency are used. This is the approach that was used for the demonstration radio receiver front end.

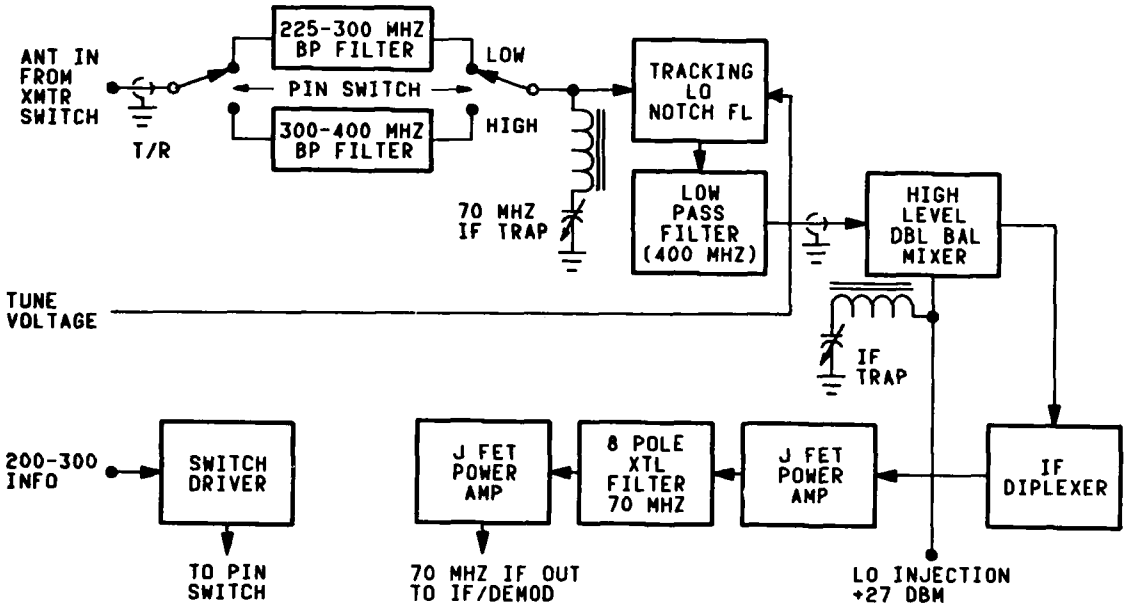


Figure 4. Single conversion receiver front end

A bandpass tubular filter, CIRQTEL FB/2-262.5/85-6/40-28A/28A is used to limit the incoming frequencies to those in the band of 225 to 300 MHz and a CIRQTEL FBT/2-350/120-8/50-28A/28A filter is used for the high band, 300 to 400 MHz. The filters are switched by the PIN diode switches of Figure 5 and the PIN driver circuit of Figure 6. PIN switch performance data is shown in Table 5. The filters have an insertion loss of less than 1 dB and provide the receiver image rejection by reducing the level of the signals displaced 140

MHz above the operating frequency. Also rejection is provided at some frequencies, to the local oscillator injection frequency of 70 MHz above the operating channel. This reduces the injection frequency level which appears on the "R" port of the mixer about 35 dB below the LO level of +27 dBm. As some LO frequencies pass through the tubular filters with little or no attenuation, it is necessary to further reduce the LO level to prevent reradiation by the antenna. The filter to reduce this signal level is in the form of a dual notch which is tuned by stacked varactor diodes. The two notch sections are separated by a short length of 50-ohm line. Also in this assembly is a 70-MHz notch which attenuates any incoming IF signal on the antenna input beyond that acheived by the tubular filters. A schematic diagram of the notch filter assembly is shown in Figure 7 and data is shown in Table 6.

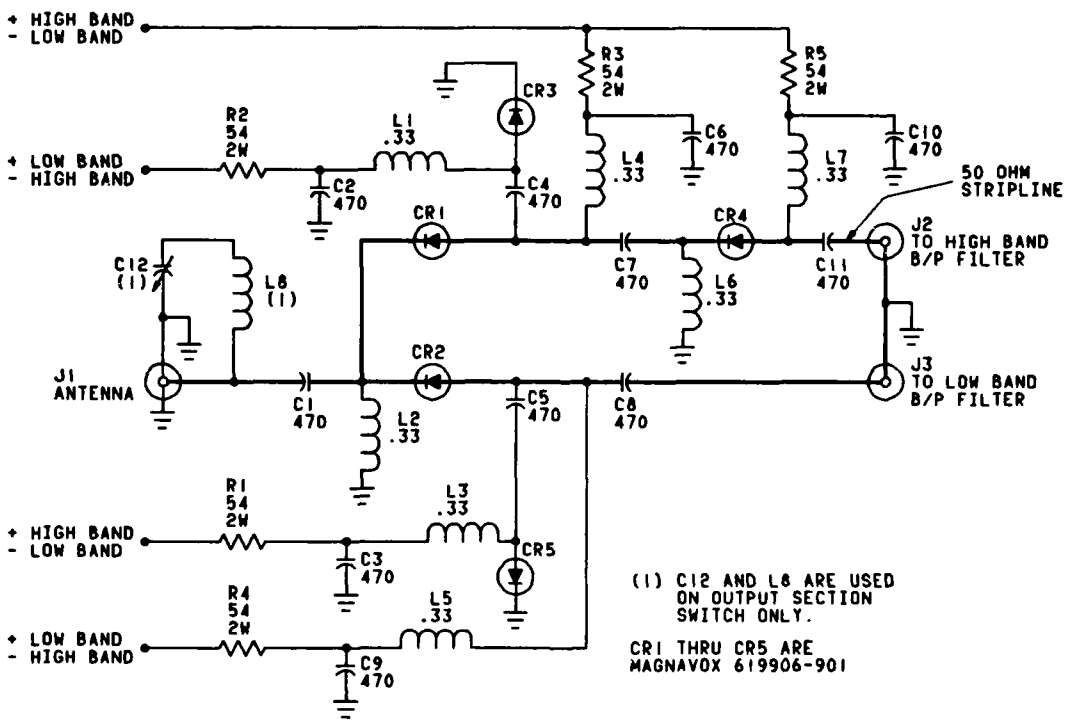


Figure 5. Pin diode filter switch section

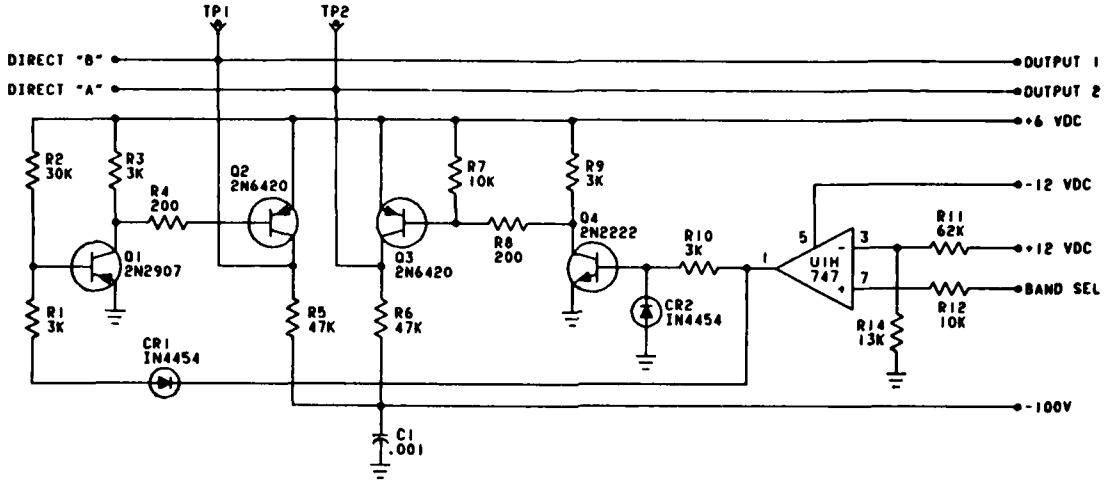


Figure 6. Pin switch driver

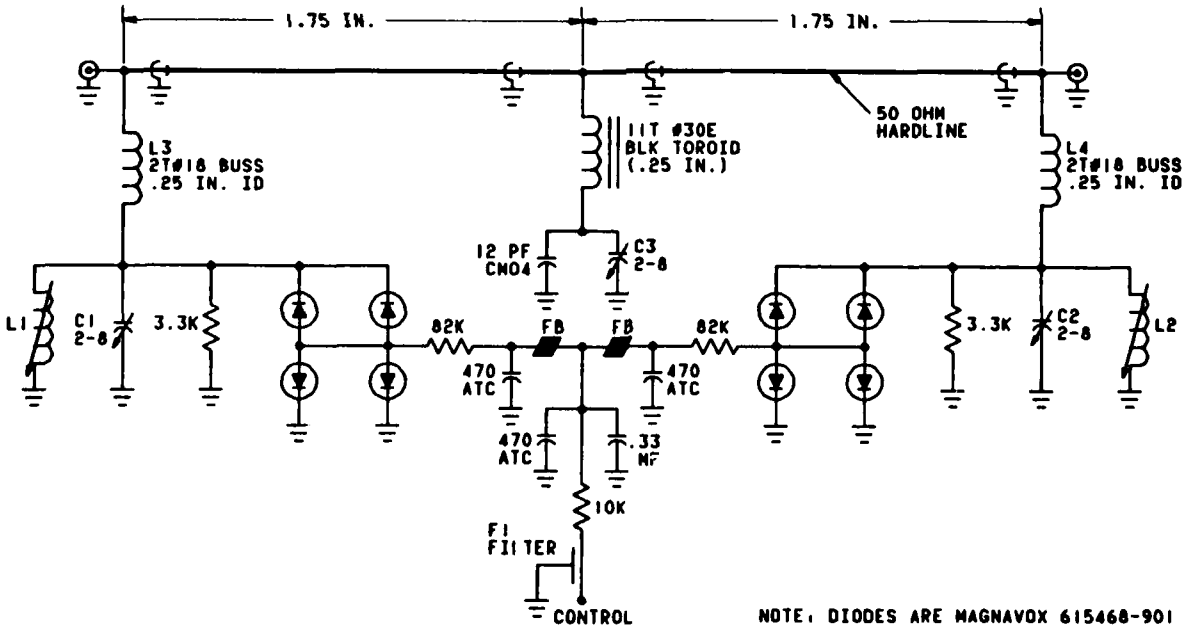


Figure 7. LO notch filter schematic

TABLE 5. PIN SWITCH PERFORMANCE

Frequency MHz	High Band Iℓ (dB)	Isolation, conducting low band path to open high band port (dB)	Low band Iℓ (dB)	Isolation, conducting high band path to open low band port (dB)
200	.4	>70	.3	45
250	.4	>70	.3	43
275	.4	69	.3	43
300	.5	66	.3	42
325	.5	64	.3	41
350	.5	63	.3	40
375	.5	62	.3	39
400	.5	60	.3	38
425	.4	59	.3	36
450	.4	57	.4	35
475	.4	56	.4	35
500	.5	55	.4	33

As mentioned previously, the high-level first mixer generates strong harmonics of the LO signal on the "R" and "I" ports due to unbalance and diode multiplication. To prevent these harmonics from appearing on the antenna, a low-pass filter with a cut-off frequency of 420 MHz is placed between the mixer and notch filter. These harmonic levels are then reduced by the low pass, as well as the switched bandpass filters. An IF series tuned notch filter is placed across the LO port of the mixer to reduce the level of any 70-MHz component which may appear on the injection port. Without trapping, any low level 70-MHz spurious signal on the injection could be amplified by the following stages, pass through the crystal filter and cause interference to a desired incoming signal.

A 70-MHz diplexer is used to properly terminate the output of the double-balanced mixer at all frequencies of interest and to pass only the desired IF signal to the following amplifier stage. The resistive

TABLE 6. NOTCH FILTER PERFORMANCE DATA

f_o	Required peak -tune E	Peak actual (-)	Notch (dB)	±6 dB BW MHz	Desired attn (dB)
225 (set)	3.10	3.06	48	2.85 - 3.26	.8
30	3.42	3.28	49		.7
35	3.72	3.69	48		.8
40	4.03	4.01	48		.9
45	4.37	4.33	48		.9
50	4.81	4.75	48		.9
55	5.13	5.06	48		.9
60	5.50	5.48	48		.9
65	5.85	5.91	48		.9
70	6.28	6.32	48		.9
75	6.65	6.64	48		1.0
80	7.10	7.09	48		1.0
85	7.48	7.51	48		1.0
90	7.87	7.83	48		1.0
95	8.25	8.24	48		1.0
300	8.70	8.67	47	8.41 - 9.03	1.0
05	9.15	9.09	48		1.0
10	9.61	9.51	47		.9
15	10.00	9.93	47		.9
20	10.45	10.35	47		1.0
25	10.91	10.88	47		1.0
30	11.30	11.30	47		1.0
35	11.75	11.73	47		1.0
40	12.29	12.25	47		1.0
45	12.82	12.78	47		1.1
50	13.39	13.31	48		1.1
55	14.00	13.97	48		1.1
60	14.54	14.61	48		1.1
65	15.39	15.45	48		1.1
70	16.36	16.18	48		1.0
75	17.35	17.13	48		1.0
80	18.41	18.29	48		1.0
85	19.70	19.66	48		1.0
90	21.60	21.50	47	20.1 - 23.2	1.0
95	23.70	23.80	47		1.0
399.0 (set)	26.50	26.40	47		1.0

NOTE: 70 MHz ATTN. = 28 dB

termination is needed to realize the maximum intermodulation performance of the mixer and filtering the signal to the amplifier reduces overload and spurious generation by that stage. The diplexer schematic and associated input VSWR is shown in Figure 8 and Table 7.

Output of the diplexer is routed to a JFET (CP 643) IF amplifier, Figure 9, with a gain of 10.5 dB and noise figure of 4.5 dB. Input impedance of this device in the grounded gate configuration is very close to 50 ohms resistive up through 500 MHz. The amplifier operates at a current of 30 milliamperes and provides very good intermodulation performance.

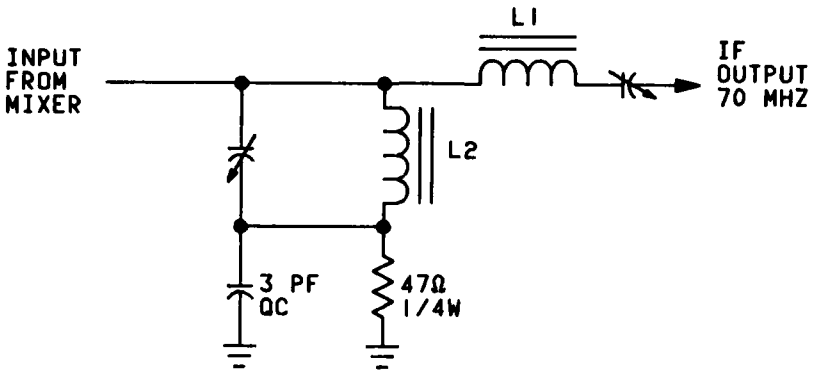


Figure 8. IF diplexer schematic

TABLE 7. DIPLEXER VSWR VS. FREQUENCY

Frequency (MHz)	VSWR
5	<1.5:1
10	<1.5:1
20	1.6:1
30	2.0:1
40	3.0:1
50	3.0:1
60	3.0:1
80	2.0:1
90	3.0:1
100	3.0:1
200	<1.5:1
300	<1.5:1
400	<1.5:1
500	<1.5:1
550	<1.5:1

Output of the amplifier is passed through an 8-pole, 70-MHz crystal filter to establish the basic IF selectivity and is again amplified by an identical JFET IF amplifier. Insertion loss of the crystal filter is 6

dB with a passband as shown in Table 8. Output of the second JFET amplifier is passed to the IF/detector section of the receiver. With this system, the requirements imposed on the receiver by the statement of work are easily met.

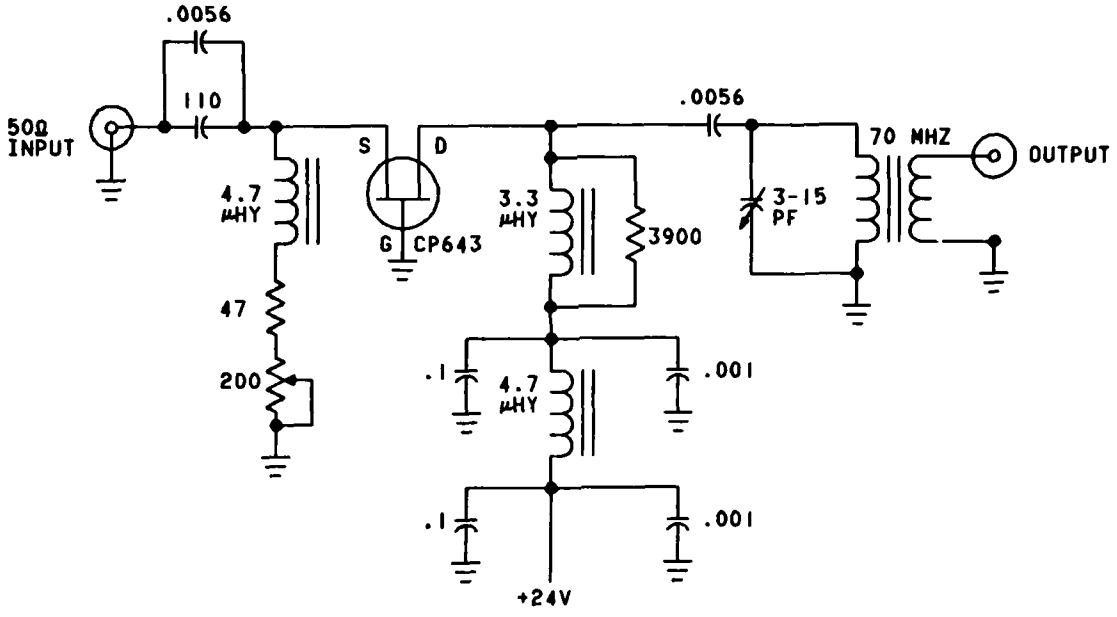


Figure 9. J-FET IF amplifier schematic

TABLE 8. DEVELOPMENT MODEL RECEIVER 70-MHZ IF FILTER CHARACTERISTICS

McCoy Model 80B107, SN 52997-1	Characteristic
CF Insertion Loss	6.6 dB
Ripple	0.4 dB
-3 dB bandwidth	33.4 kHz
-6 dB bandwidth	35.8 kHz
-20 dB bandwidth	38.9 kHz
-40 dB bandwidth	42.4 kHz
-60 dB bandwidth	48.4 kHz

TRANSMITTER STUDIES

The transmitter studies have centered around the problem of achieving low broadband noise. The problem of reducing spurious levels, while not to be minimized, has been shown in prior studies to be primarily related to effective filtering and decoupling.

Consequently, an extensive amount of effort was made on broadband noise reduction during the study phase of the program. Also, considerable shielding and filtering of the RF sensitive areas of the demonstration model transceiver was included to minimize spurious output levels.

Constant VSWR Modulator

The purpose of this investigation was to improve the VSWR of the AM modulator, because the changing input impedance, as a result of applied modulation signals, of a PIN diode modulator (the type commonly used in solid state AM transmitters) causes the oscillator source driving the modulator to be frequency modulated because the resonant frequency of the oscillator is load dependent. Present designs typically have VSWR variations of 3:1.

A constant impedance pi-attenuator shown in Figure 10 was constructed and tested over the frequency range of 225 to 400 MHz. Tests were performed with an input level of +2 dBm and with a matching network designed for a 50-ohm system. The key design parameter is to select diodes having a specific resistance vs. current characteristic to achieve the desired constant VSWR. Diodes tested for this application included the Hewlett-Packard device 5082-3101, Unitrode devices U76202B and UM7301B, and GHz Devices 40498-15 and 40498-30.

The best matching results were obtained with the GHz 40498-15 device which has the following resistance versus current characteristic: resistance (ohms) is proportional to $35I^{-0.74}$ where I is the forward current in millimperes.

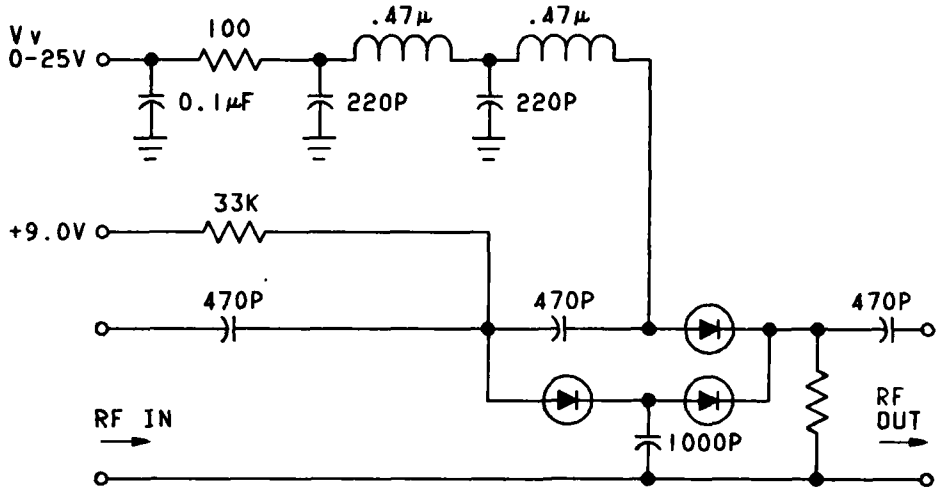


Figure 10. Constant impedance attenuator network

Table 9 for the three frequencies of 200, 300, and 400 MHz shows the input reflection coefficient, S11, and the attenuation of the network as the variable voltage V_v is changed from 0 to 24 volts. The table shows that the maximum attenuation is 30 dB at 400 MHz, 36 dB at 300 MHz, and 38 dB at 200 MHz. Based on this test data, the maximum variation in input VSWR over the entire attenuation range is less than 1.5 to 1 which is a substantial improvement over present designs.

Subsequent tests, however, showed that this attenuator did not perform correctly when installed in a transmitter automatic level control (ALC) loop. The problem was determined to be the time delay introduced by the special diodes with the desired RI characteristic. The conclusion was that the type of voltage controlled attenuator used in the present ARC-164 modulator or a high-level equivalent described in subsequent paragraph would be used in the EMC Technology Transceiver. This makes it imperative to provide sufficient isolation between the modulator and the oscillator driving source to minimize incidental frequency modulation related to the desired AM modulation.

TABLE 9. CONSTANT IMPEDANCE NETWORK ATTENUATION AND REFLECTION CHARACTERISTICS

	200 MHz S11		300 MHz S11		400 MHz S11	
Atten. (dB)	Magnatude	Phase	Magnatude	Phase	Magnatude	Phase
2	.15	0	.15	43	.18	38
3	.08	0	.12	50	.12	58
4	.01	0	.1	90	.1	90
6	.05	180	.12	135	.12	122
7	.05	180	.12	145	.1	130
8	.03	180	.12	145	.1	130
10	0		.1	125	.07	115
12	.03	0	.08	95	.05	65
14	.08	0	.07	60	.07	32
16	.12	0	.1	32	.1	20
18	.18	0	.1	30	.15	20
20	.2	0	.15	28	.18	15
22	.2	0	.18	25	.2	10
24	.22	0	.2	20	.22	10
26	.24	0	.21	20	.22	10
28	.25	0	.22	20	.23	10
30	.25	0	.22	20	.23	10
32	.25	0	.22	20		
34	.25	0	.23	19		
36	.25	0	.23	19		
38	.3	0				

High-Power VCO

The purpose for investigating high-power VCO's is that most solid-state transmitters have large amounts of broadband gain which amplify the input broad-band noise (both from the RF source and the amplifier internal noise) to excessive levels at the output. By starting with a higher level RF source (high-level VCO) the broadband gain can be reduced with a subsequent reduction of broadband noise.

Figure 11 shows the circuit used in the high-power VCO. It was designed to tune from 225 to 400 MHz in one band. The varactor tuning voltage varies between -3.5 and -25V and the output power is +22 dBm. The transistor used in this stage is the 2N5109.

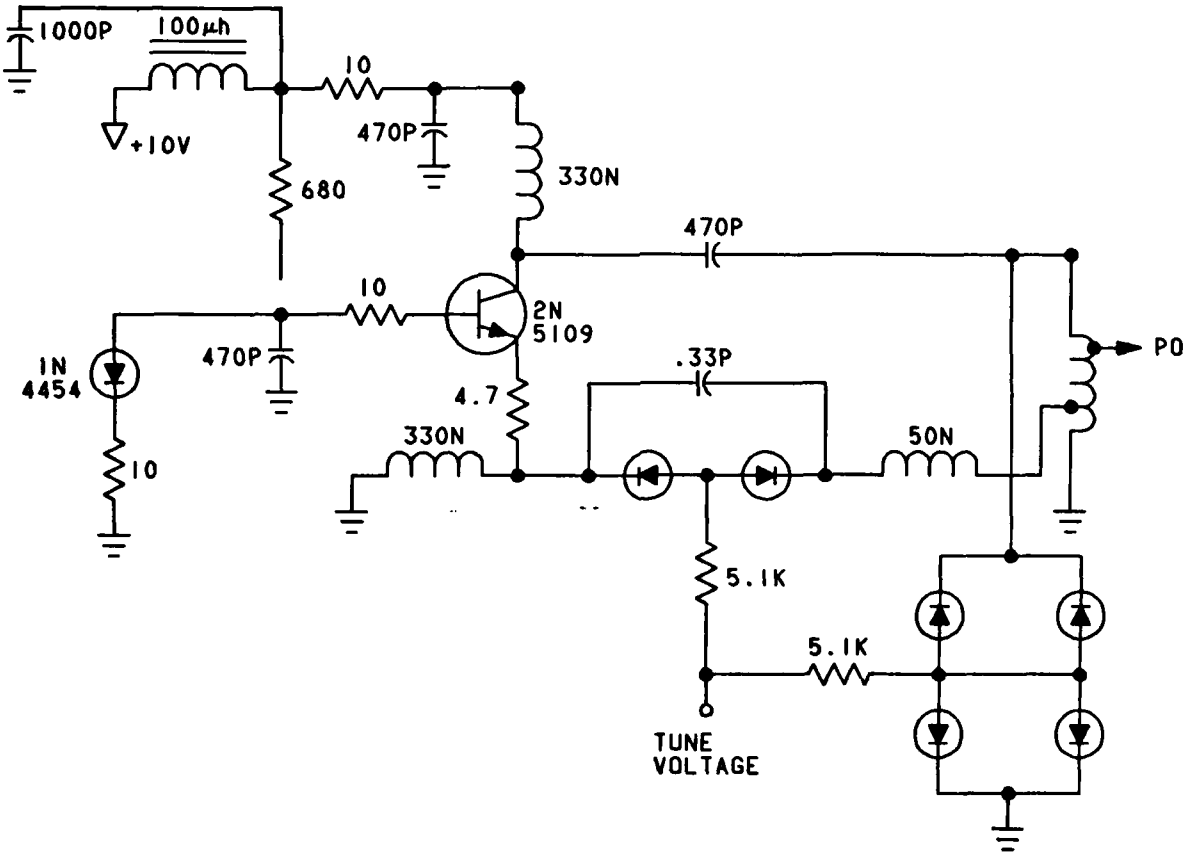


Figure 11. High-power VCO circuit

The noise developed by this stage is of two types. The first is thermal noise determined entirely by the transistor noise figure and the gain of the stage. The output noise of the 2N5109 has been measured using the test circuit shown in Figure 12. At frequencies between 225 and 400 MHz the noise of the circuit shown in the schematic of Figure 11 with feedback removed, averages -156 dBm/Hz. This is the noise power which appears at the output port when the device is connected as an amplifier and with no carrier applied to the input. With the 2N5109 connected as an oscillator, as shown in Figure 11, additional SSB phase noise power closer to the carrier is introduced at the output. This is due to phase modulation of the carrier by the device noise. Its magnitude is determined by the transistor noise figure and by the feedback circuitry associated with the oscillator. The power level of this noise is described as L (fm) which is the ratio of phase noise power/Hz to carrier power at frequency fm removed from the carrier and it can be calculatd from the following equation:

$$L\ (fm) = \frac{1}{2}\left[1 + \frac{1}{fm^2}\left(\frac{fo}{2Q}\right)^2\right] S_{\Delta\theta}$$

Where

f_o = carrier frequency

f_m = offset frequency

Q = the loaded Q of the oscillator feedback circuit

$S_{\Delta\theta}$ = phase noise spectral density/Hz which is equal to the ratio of the transistor noise power/Hz referenced to the input port to the feedback signal power at the port.

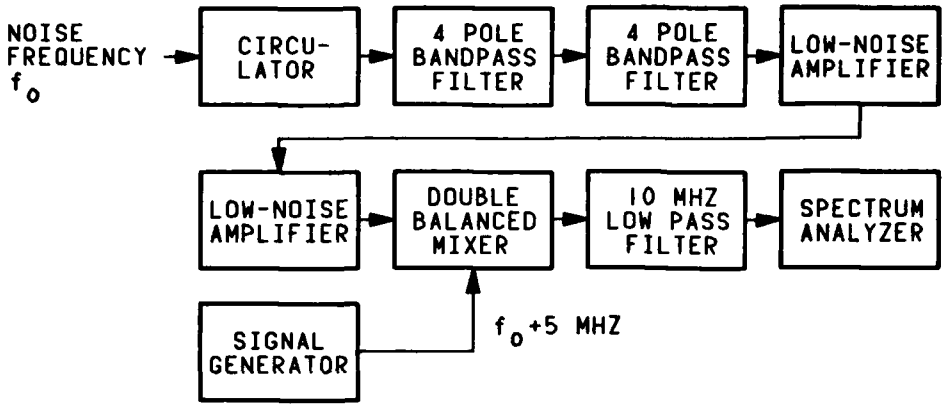


Figure 12. Noise measurement test circuit

The transistor has a 3 dB noise figure, and the feedback signal power based on an output level of +22 dBm and 12 dB of gain, is 10 Mw. Using these numbers 10 log $S\Delta\Theta$ is equal to 181 dBm.

Figure 13 shows the VCO output noise power/Hz. One curve gives the phase noise calculated from the preceding formula and the other gives the noise power/Hz which results from the transistor thermal noise. As can be seen from the figure, the two noise curves intersect at a frequency between 10 and 20 MHz removed from the carrier. At frequencies further removed from the carrier, the phase noise contribution becomes negligible while closer to the carrier the phase noise is predominent. The third curve in Figure 13 gives the total VCO noise power/Hz and the thermal noise/Hz.

The test circuit shown in Figure 12 was used to measure the VCO noise power at frequencies removed more than 10 MHz from the carrier. The results of this measurement are given in Figure 14. Comparing the measured results with the calculated results shows that at frequencies more than 20 MHz removed from the carrier the noise power levels are within 1 dB. At frequencies closer to the carrier than 20 Hz, the measured noise power is higher than the calculated power. It is also rising with a steeper slope as the carrier frequency is approached. The source of this higher noise level close to the carrier is not yet known, but may be due to an additional phase noise component which is empirically described by a corner frequency

f_c. For frequencies below this corner frequency, the phase, noise spectral density increases with f_m^{-1}. This corner frequency is device dependent and it will modify the $S\Delta\Theta$ previously defined by the multiplication factor $(1 + \frac{fc}{fm})$, and therefore affect the phase noise power for fm < fc.

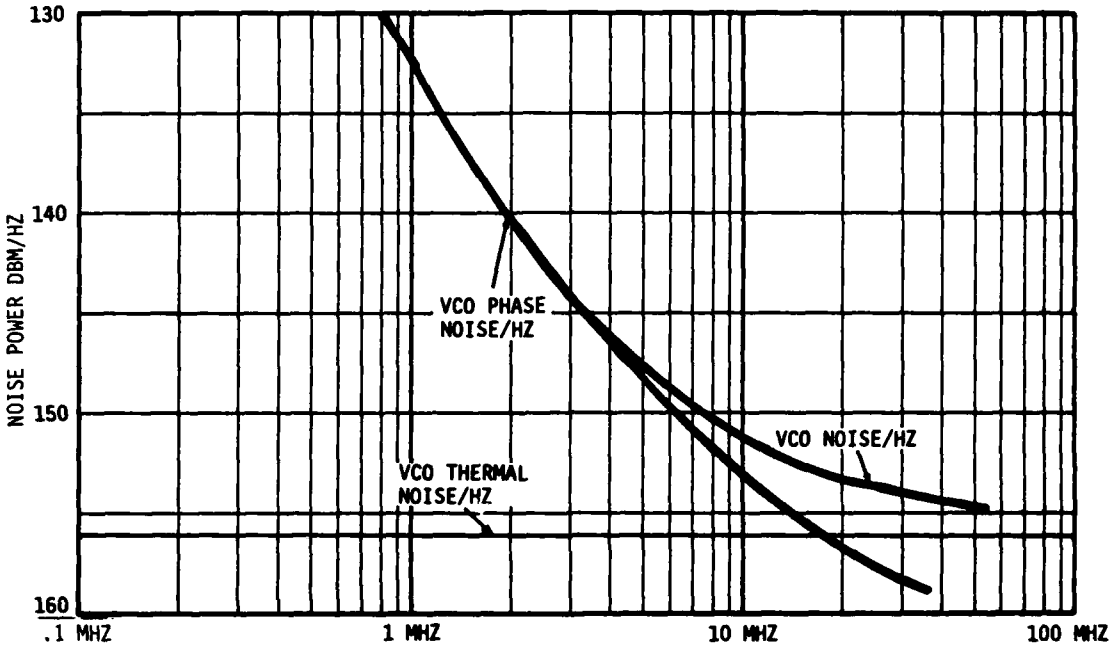


Figure 13. Calculated VCO noise power 300 MHz

In general, the broadband noise of the VCO is sufficient to meet the EMC design goals for broadband noise >±15 MHz from the carrier and will also be less than the specified -110 dBm/Hz level for frequencies between ±8 MHz of the carrier to ±15 MHz of the carrier.

High-Power Tuned Amplifier

The purpose of investigating high-power tuned amplifiers is basically the same as high power VCO's, i.e. to reduce broadband noise at the input to the power amplifier. In the case of a high-power tuned amplifier, the

object is to reduce the input noise of a low-level source by amplification with bandpass filtering. The problem associated with this approach is that the output RF levels (+20 dBm) that must be filtered are sufficient to sometimes cause rectification in the varactors and consequently detuning of the filter.

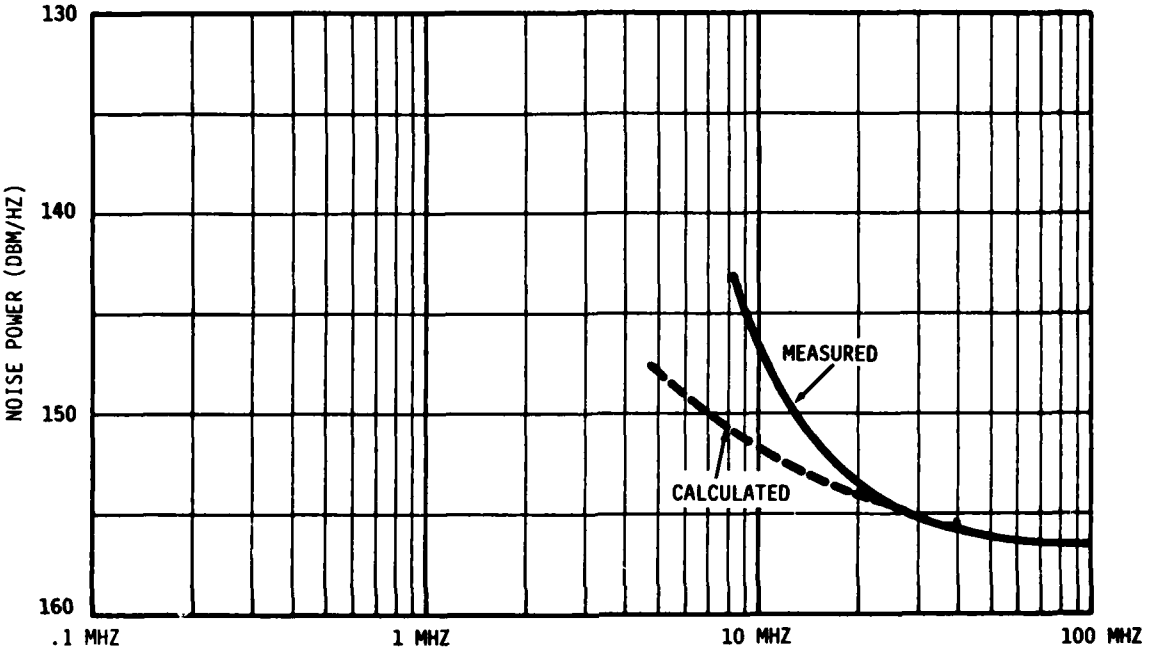


Figure 14. Measured VCO noise power, 300 MHz

Figure 15 is a block diagram of a high-power tuned amplifier. The input to the amplifier is obtained from a low-level source, such as a synthesizer, at a power level of approximate +5 dBm. The overall amplification of about 19 dB provides +24 dBm of power at the output. The output noise power was measured and is shown in Figure 16 for a 300-MHz center frequency. This curve was obtained experimentally by optimizing the signal-to-noise at the modulator output with the three tuned circuits in the modulator chain.

The essential result is that away from the carrier (±30 MHz for example), the tuned amplifier is equivalent to or better than the high-power VCO. But at ±15 MHz, the higher power VCO just meets the requirement

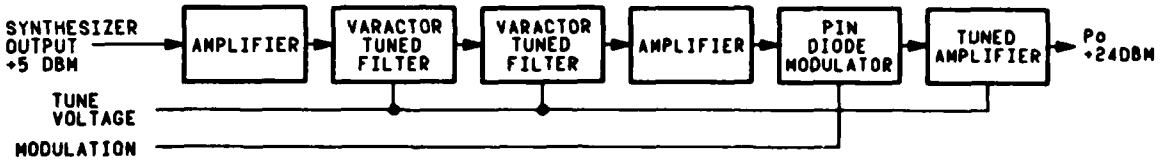


Figure 15. Tuned amplifier modulator block diagram

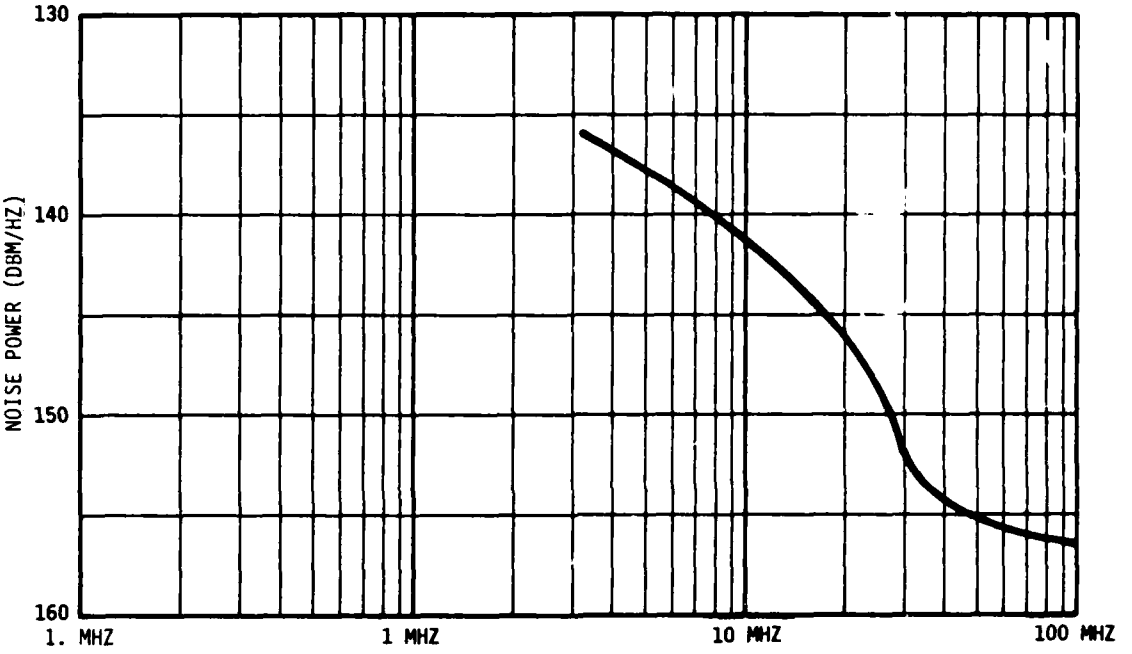


Figure 16. Measured tuned amplifier modulator output noise

(approximately - 152 dBm/Hz), whereas the tuned amplifier would not meet the specification by about 6 dB. The reason is that within the bandwidth of the amplifier, the source noise is amplified rather than attenuated.

VMOS Transistor Studies

In the tracking filter modulator approach (high-power VCO locked to the synthesizer), Figure 17, in which broadband gain follows a relatively low-noise VCO), the noise figure of the broadband amplifiers can contribute significantly to the overall modulator output noise power. For this reason,

VMOS power FETS have been investigated as replacements for the bipolar power transistors in this application. The devices investigated in this study were the Siliconix DV2805, DV1205 and the CTC CF4-28. The available gain for the DV1205 was found to be 7 dB at 410 MHz, while that for the DV2805 was 9 dB. These devices are therefore not suitable for this application since a minimum gain of 10 dB is required between 200 and 410 MHz. The available gain of the CF4-28 varied between 16.5 dB at 220 MHz and 10.5 dB at 410 MHz. Since this device is suitable from a gain standpoint, the noise performance of the CF4-28 was compared to that of the MRF5174 transistor which was the device used in the prototype tracking filter modulator. The noise comparison of these two transistors is shown in Figure 18.

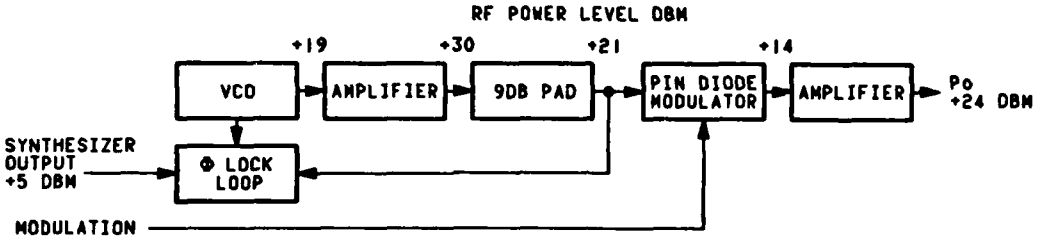


Figure 17. Tracking filter modulator block diagram

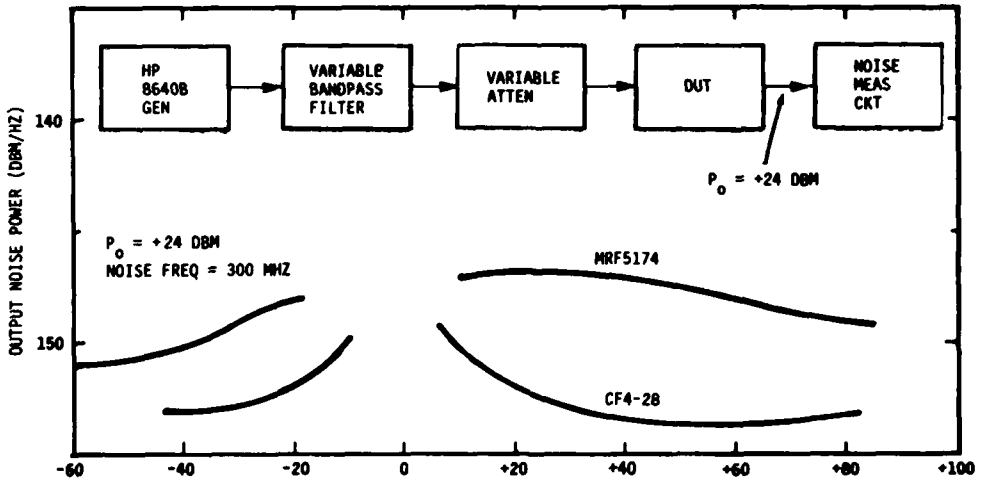


Figure 18. CF 4-28 and MRF 5174 noise comparison

The comparison was made using the connections shown in the block diagram of Figure 12. The low-noise generator signal is applied to the device being tested through an 8-pole variable bandpass filter. The attenuator is then varied until the output power of the tested device is +24 dBm. The filter insures that the generator noise at the device input, outside of the filter bandpass, is sufficiently below the device noise so that the device being tested can be considered driven by a noise free carrier. The curves were obtained by varying the generator frequency between 225 and 400 MHz and tracking the generator with the variable bandpass filter, while observing the output noise power/Hz at 300 MHz. The result of this measurement shows that the CF4-28 FET has a lower noise output power than the MRF5174 transistor under the condition of equal output power.

The tracking filter modulator requires an output of +24 dBm. Two dB of overall gain, assuming a VCO output of +22 dBm, must therefore follow the high-power VCO. The calculated noise output of the modulator with VMOS amplifiers for the gain stages is shown in Figure 19. The measured output noise of the breadboard tracking filter modulator with the carrier frequency at 300 MHz is given in Figure 20. The measured result is consistent with the noise measurement made on the MRF5174 transistor. It shows that with this transistor the modulator output noise is generated almost entirely in the final modulator stage, and consequently can be slightly improved with VMOS devices.

It was planned, therefore, to use VMOS devices in the model EMC Technology transceiver where these characteristics can be used to advantage.

A present difficulty with the use of VMOS is that device manufacturers aren't characterizing the device above 175 MHz so all parameters must be measured in the laboratory. However, this aspect is expected to change as the use of VMOS becomes more wide spread.

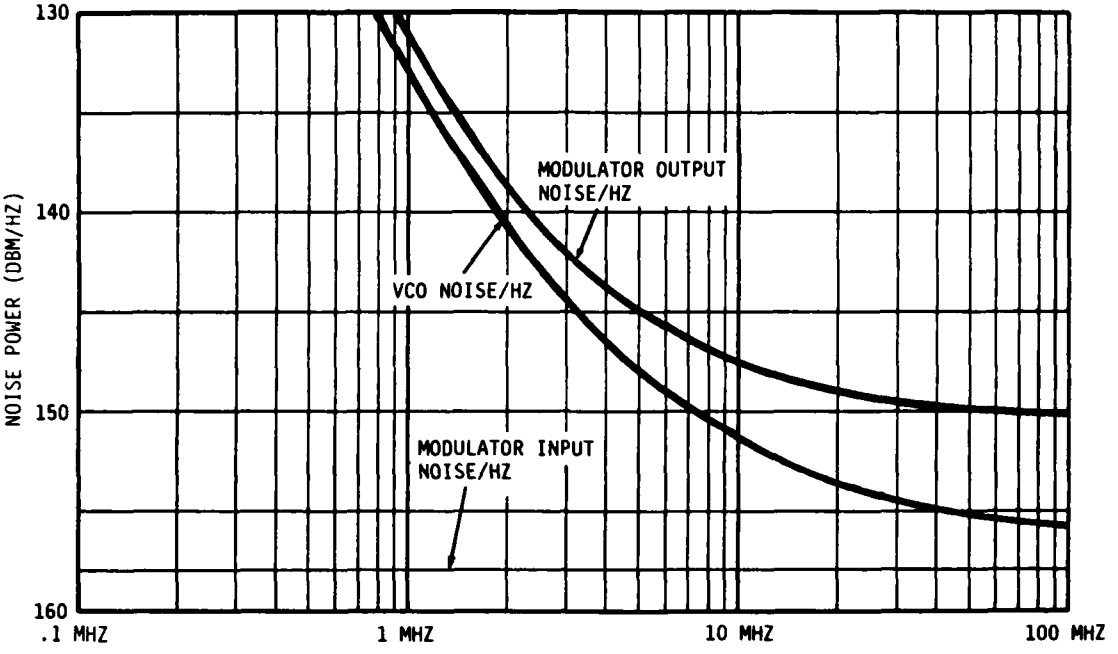


Figure 19. Tracking filter modulator/VCO combined

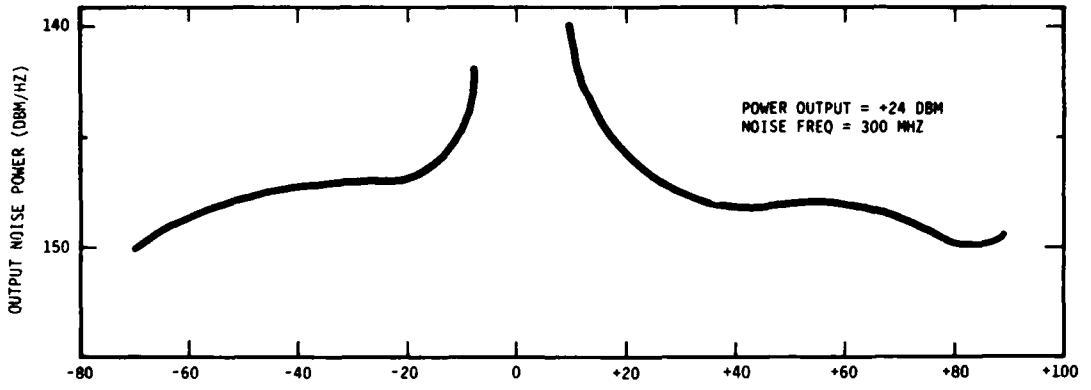


Figure 20. Measured noise, tracking filter modulator

High-Level Modulator

The equivalent noise power of the modulator in Figure 17 referenced to the VCO output is -154 dBm/Hz. This is based on the gain distribution shown and on a noise figure of 10 dB for the amplifier stages in the chain. Figure 19 is a graph of the combined noise power of the VCO and modulator

referenced to the input and output of the modulator. The output noise shown is obtained by adding the noise power/Hz from the VCO to the equivalent noise power/Hz of the modulator and raising this power level by 2 dB which is the overall modulator gain. The curves show that a significant contribution to the modulator output noise power is made by the circuitry between the high power VCO port and the modulator output. The noise at this output is 2 dB above the VCO noise if the ratio of VCO to modulator noise is sufficiently high. This is practically true within 3 MHz of the carrier, but at 10 MHz distance the ideal condition has been degraded by 4 dB.

The block diagram in Figure 21 gives a modulator chain which comes closer to the ideal performance described above. The diagram shows the gain distribution in the modulator chain and also shows the noise power/Hz at various points of the chain based on amplifiers having a 10-dB noise figure. The calculated modulator output noise which can be obtained with the high-level modulator is shown in Figure 22. Comparing this graph with Figure 19 for the low-level modulator it is seen that the equivalent noise power at the modulator input has been reduced from -154 to -158 dBm. This results in approximatley 2-dB improvement at frequencies sufficiently removed from the carrier.

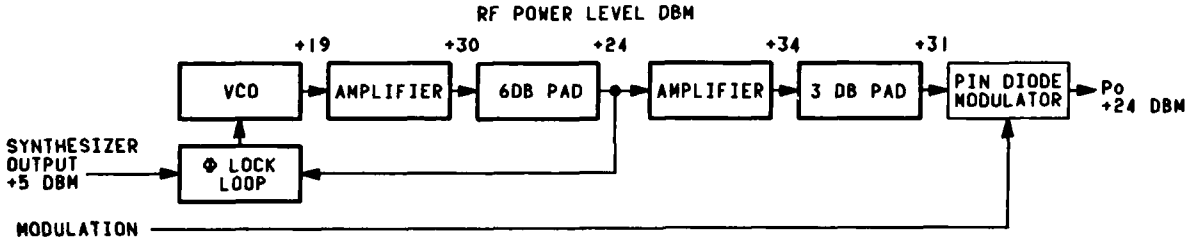


Figure 21. Tracking filter high-level modulator block diagram

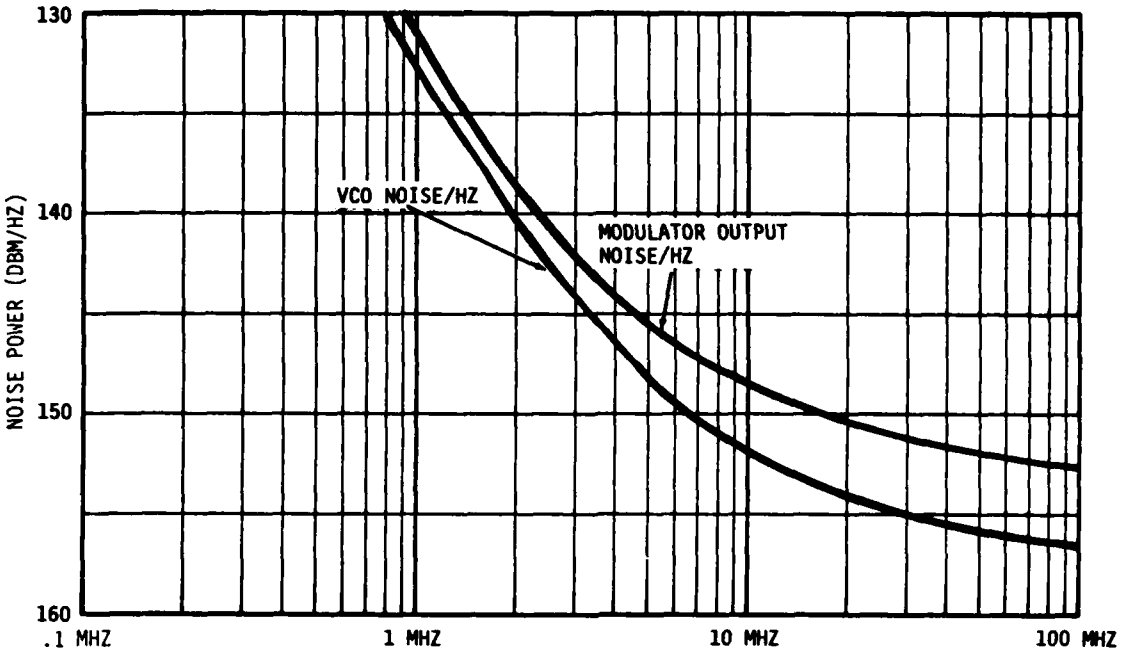


Figure 22. Calculated high-level modulator noise power tracking filter modulator

The high-level modulator used in this application is shown in Figure 23. The carrier input at a level of +31 dBm is applied to one port of a 90-degree hybrid coupler. This coupler divides the RF input at port 1 equally to ports 3 and 4. When the shunt PIN diode is reverse biased or zero biased and the series PIN diode is forward biased, the RF power flows to ports 1 and 2 of the output 3 dB 90-degree hybrid coupler. The output coupler combines these inputs to port 4, the output port. Reversing the bias condition causes the pin diodes to absorb some of the input power while also reflecting some of it back to ports 3 and 4 of the input coupler. The remainder of the RF input is combined in the output coupler at the RF output port. That portion of the RF input reflected by the diodes to the input coupler is combined at port 2, which is terminated with a 50 Ω load. Thus, ideally, none of the reflected RF input appears at the input port even under the condition of maximum attenuation.

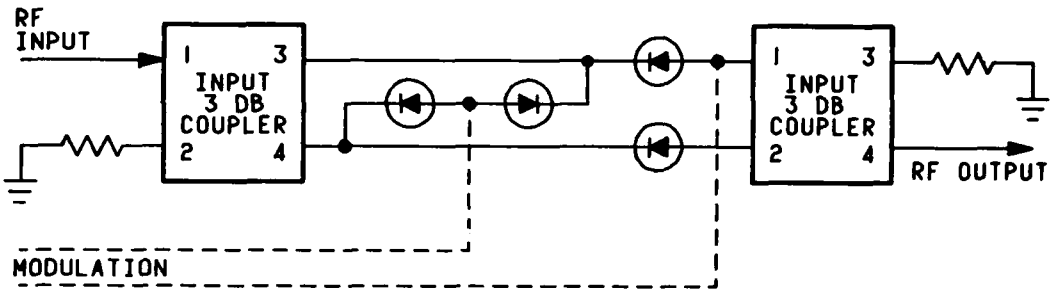


Figure 23. Non-reflective pin diode attenuator simplified block diagram

With no modulating signal applied to the modulator, the attenuation in each pin diode attenuator is 7 dB. Under this condition ports 1 and 2 of the output hybrid coupler will each see +21 dBm of RF power. These inputs are combined at port 4 by combining in phase two RF signals each at a level of +18 dBm resulting in a +24 dBm/RF output.

SYNTHESIZER STUDIES

The synthesizer in a UHF transceiver contributes to the overall EMC problem in two distinct areas: Spurious signals and noise.

Spurious signals are from two primary sources in applications using a phase-locked synthesis approach. (This approach is the most common in present day UHF transceivers). First of all, spurious signals removed from the carrier by an amount equal to the reference frequency, or harmonics thereof, are generated by direct coupling from the phase detector to the voltage controlled oscillator. The second source of spurious signals is the ripple noise at the switching mode regulator frequency in the power supply modulating the VCO generating spurious signals. Spurious signals can also result from frequency divider outputs that are coupled in the VCO.

Noise on the synthesizer output effects both receiver performance and transmitter broadband noise. The noise on the output of the synthesizer is typically a broadband component for offsets from the carrier greater than ±15 MHz and phase noise for signals within the frequency range of ±15 MHz of the carrier. These two noise characteristics will be discussed in greater detail in subsequent paragraphs.

The problem of reducing spurious signals at the output of a synthesizer is primarily related to appropriate filtering on the VCO control line to reduce reference frequency spurious signals and power supply post regulation and decoupling to reduce power supply spurious signals. Careful shielding and isolation of the VCO are also required. These spurious signals are only to a very limited degree related to the design approach and instead are primarily related to circuit design and fabrication and packaging techniques. As a result, during the study phase of the contract these parameters were given only limited attention, but during the development of the EMC Technology Transceiver, the control of these spurious signals were given careful attention.

In this regard, however, new high-density LSI synthesizers were investigated in the study phase of the contract. The principal explored was that new synthesizer integrated circuits contain the frequency counter, phase detectors, and storage latches to retain the desired frequency count. The expectations are that with a substantial amount of the digital circuitry in a synthesizer being contained in a single IC, it will be considerably easier to control spurious emanations. Noise on the synthesizer output effects both receiver dynamic range and transmitter noise floor. It has been determined that the noise on the synthesizer output is chiefly a function of the output VCO design and associated buffer amplification. As a result, during the study phase of the contract considerable effort was directed at, first of all, characterizing the VCO noise requirements so that a specification for the VCO can be determined and secondly, actual breadboarding and testing was done to verify the performance.

In summary, synthesizer studies have been conducted in two primary areas:

(1) Evaluation of new high-density LSI synthesizer circuits.
(2) VCO characterization and design.

Highlights of these studies are discussed in the following paragraphs.

High-Density LSI Synthesizer Circuits

Several manufacturers of integrated circuits have been developing families of phase locked loop frequency synthesizer circuits. These circuits have built into a single chip, many of the functions that formerly required a dozen or more integrated circuits. It was believed that these new circuits could be used to advantage in the EMC Technology Transceiver because with all of the digital circuits contained in a single circuit, decoupling of spurious signals would be considerably simpler. A survey of devices from National Semiconductor, Motorola Semiconductor, and Signetics was conducted. In general, the National devices and Motorola devices have much in common. They are in general CMOS devices and provide for either parallel load of the frequency data or serial load of the frequency data. These devices typically contain a programmable reference divider that devides the standard reference frequency from a crystal source down to the desired phase comparator frequency, a main counter and a swallow counter that is used to control a variable modulus prescaler, a phase detector (generally of the charge pump type), and a phase lock detector.

The Signetics LSI synthesizer devices were developed by Mullard Labs in England and are being manufactured by Signetics on a sample basis only at this time. These devices use a LOCMOS technology and embody some very advanced design capability. These include the implementation of two phase detectors on the circuit. One phase detector is used during lock-up and provides for very fast lock-up time. After lock-up occurs

the second phase detector is energized, and this phase detector is specifically designed to achieve low-noise performance. These devices were procurred on a sample basis and only limited investigation was performed.

During the study phase of the contract, a complete synthesizer was breadboarded using a Motorola MC145156 integrated circuit. The only other circuits required to complete the divider chain in the synthesizer were a divide by 10/11 counter and a divide by 8 variable modulus pre-scaler controller (three integrated circuits in all). Results obtained from this test were encouraging and it appears that significant reduction of the electronics in a synthesizer can be achieved. This will also make it much easier to shield the entire synthesizer and make it ea ier to control spurious emanations, both conducted and radiated.

The integrated circuit used in the breadboard model used serial data input to the device.

VCO Characterization and Design

To a very large extent the broadband noise from the transmitter is responsible for the degradation of the sensitivity of co-located receivers. In prior study contracts it was shown how the output broadband noise of a transmitter was essentially the broadband noise associated with the synthesizer signal amplified by the gain of the transmitter. Thus, it was determined at an early stage, that improvement in the output noise of a transmitter would require improvement of the output noise of the synthesizer.

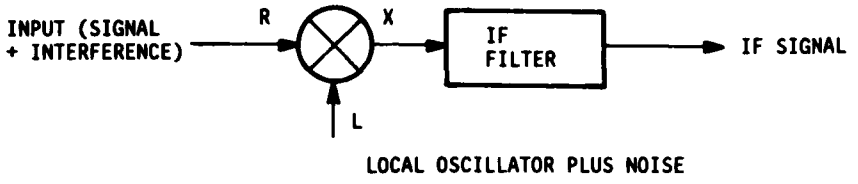
During the study phase of the present contract it was determined that the close-in noise (5 to 10 MHz from the carrier) on the synthesizer signal becomes the limiting parameter in achieving the expected receiver dynamic range.

Thus, the synthesizer VCO is perhaps the most important single circuit as related to the overall EMC noise performance of the transceiver in either transmit of receive operation.

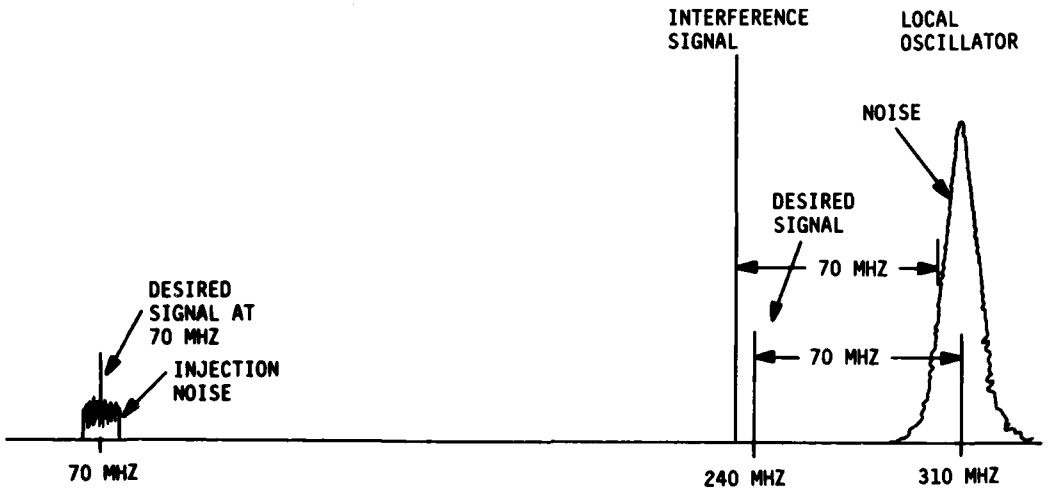
The following paragraphs summarize the results of the VCO studies as related to receiver performance and present some of the theoretical and experimental background that were used for the development of the voltage controlled oscillator used in the EMC Technology Transceiver.

VCO Characterization

First, an effort was directed at determining the limitation on dynamic range caused by noise on the local oscillator signal and to establishing a requirement for this level. Figure 24 shows what is believed to occur. The schematic on Diagram A shows the conventional down-conversion process in a receiver. The spectrum diagram shows what is happening in the frequency domain.



(A) SCHEMATIC DIAGRAM



(B) SPECTRUM DIAGRAM

Figure 24. Local oscillator receiver noise relationship

A desired signal at 240 MHz is mixed with a local oscillator at 310 MHz and down converted to 70 MHz. In addition, an interfering signal at 240 MHz Δf is present and acts as the local oscillator that translates the noise at 310 MHz Δf down to 70 MHz. This noise contaminates the desired signal and reduces sensitivity.

To quantify this degradation process, a test was performed to determine the conversion loss from the mixer L port to the mixer X port with a strong signal at the R port. The test circuit is shown in Figure 25. Basically the 310-MHz signal was acting as the conventional local oscillator; the 235.2 MHz was acting as an interfering signal with variable level, and the 305.2 MHz signal was simulating noise on the local oscillator signal (but at a level convenient for measurement). The results are shown in Table 10 and Figure 26. Note that with the 310-MHz signal off, the 235.2 MHz acts as an LO with slightly higher loss than normal, but in the presence of the +27 dBm, 310 MHz signal, the mixing process from L to X is not as efficient. At high levels, the process is nearly linear (10 dB reduction in interference) and results in a 12 dB reduction in conversion gain.

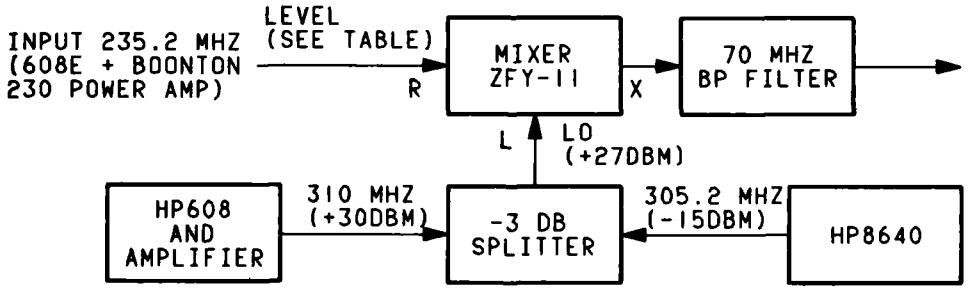


Figure 25. Mixer "L" to "X" conversion loss

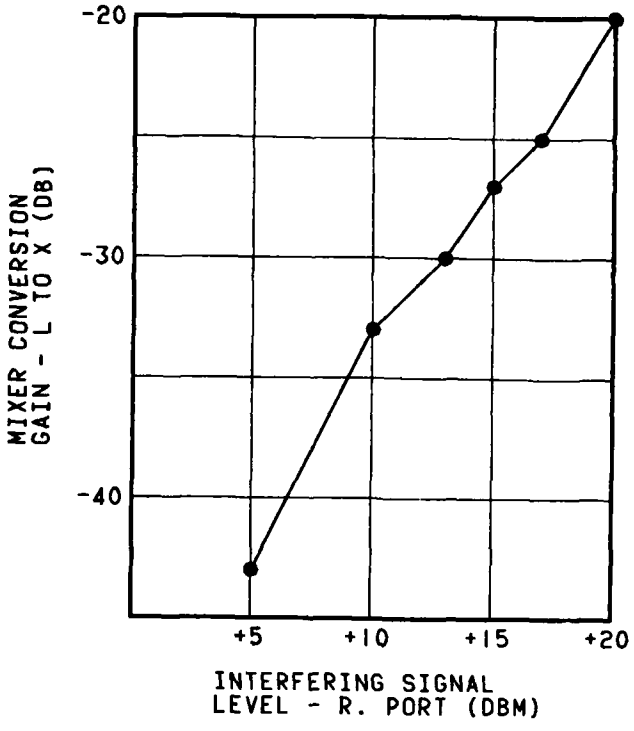


Figure 26. Mixer "L" to "X" gain vs. interferring signal

TABLE 10. TEST RESULTS OF CONVERSION LOSS

310 MHz level (L port) (dBm)	235.2 MHz level (R port) (dBm)	Conversion gain (L to X) (dB)
OFF	+20	- 9
+27	+20	-21
+27	+17	-25
+27	+15	-27
+27	+12	-30
+27	+10	-33
+27	+ 5	-42

Based on this data, a calculation was made of the level of noise on the local oscillator which will result in a 3-dB degradation in sensitivity. The model is shown in Figure 27. For quantities expressed in dB, the noise at IF is:

$$Nif = Nin - IL - Gm + N1 - G1$$

where

Nif = Noise at the IF frequency

Nin = Equivalent input noise at the antenna

IL = Filter insertion loss (1 dB assumed)

Gm = Mixer conversion gain -R to X (7 dB assumed)

N1 = Noise on local oscillator

G1 = Mixer conversion gain = L to X (function of interference level - See Table 1)

$$Nin = NF + kT$$

NF = Noise figure

kT = Thermal input noise (-174 dBm/Hz assumed)

For 3-dB degradation in sensitivity:

$$Nin - IL - Gm = N1 - G1$$

from which:

$$N1 = Nin - IL - GM + G1$$

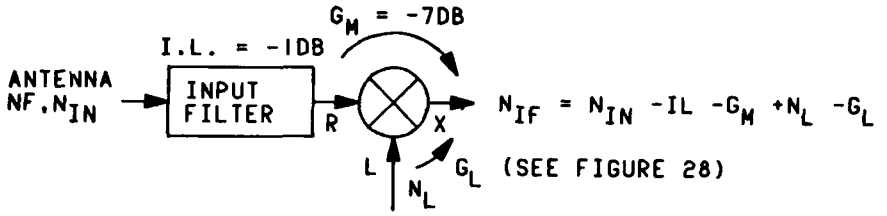


Figure 27. Mixer noise model

The results of the calculation are shown in Table 11 for several levels of interference and two different noise figures. Note that for improved noise figure, the local oscillator noise must be improved accordingly.

Preliminary testing somewhat substantiates the levels predicted by Table 10, but in general, these levels are from 5 to 7 dB conservative. The conclusion is that for a 15 dB noise figure receiver operating in the presence of a -20 dBm interference (removed in frequency from the desired signal by 2 percent), the local oscillator noise at an offset from the carrier of from 4.5 to 8 MHz needs to be approximatley -173 dBc (assume local oscillator level of +27 dBm) for no more than 3-dB degradation of sensitivity.

By way of comparison the noise of a typical ARC-164 synthesizer, 4 to 8 MHz away from the carrier is about -156 dBc/Hz and a HP 608 signal generator is -164 dBc/Hz. In the absence of substantial improvement in UHF VCO design, it appears that the best approach to meet the required levels is a VCO followed by a tuned filter.

Table 12 lists some results showing the effect of filtering on the LO. Figure 28 shows the schematic diagram of the test set up and the estimated noise level on the local oscillator (dBc/Hz) for the various configurations. When the estimated carrier-to-noise ratios are compared with the permitted levels shown in Table 11 one would predict about 3 dB degradation in sensitivity with the 5 pole filter installed, about 5 dB to 8 dB degradation in

TABLE 11. CALCULATED LOCAL OSCILLATOR SIGNAL-TO-NOISE RATIO FOR NO MORE THAN 3 DB DEGRADATION IN SENSITIVITY FOR VARIOUS NOISE FIGURES AND INTERFERENCE LEVELS

Interfering signal level (dBm)	Noise figure (dB)	Local oscillator Noise[3] (maximum) for 3 dB degradation (dBm/Hz)	Local oscillator noise relative to +27 dBm level (dBc/Hz)
+20	20[1]	-141	-168
+20	15[2]	-146	-173
+17	20	-137	-164
+17	15	-142	-169
+15	20	-135	-162
+15	15	-140	-167
+12	20	-132	-159
+12	15	-137	-164
+10	20	-129	-156
+10	15	-134	-161
+5	20	-120	-147
+5	15	-125	-152

(1) 20 dB is maximum noise figure permitted by design goal.
(2) 15 dB is typical noise figure of receiver achieved on first study.
(3) Noise is 2% removed in frequency from local oscillator.

sensitivity with the 2-pole filter installed and about 10 dB degradation in sensitivity with the 1 pole filter installed. Thus, these tests seem to substantiate the calculated noise levels to achieve specified performance criterion.

TABLE 12. EFFECTS OF LOCAL OSCILLATOR FILTERING

Injection source	No jamming sensitivity (dB)	Sensitivity with +20 dBm jammer (dB)
Wideband Amplifier (No filtering)	1.3	0
Telonic 5-pole 2% bandwidth	13	9
2 Pole Cavity (1)	12.8	4
1 Pole Cavity (2)	12.6	0

NOTES:

(1) 3 dB Bandwidth = 4.6 MHZ
(2) 3 dB Bandwidth = 5.485 MHz

F_o = 240 MHz @ -95 dBm

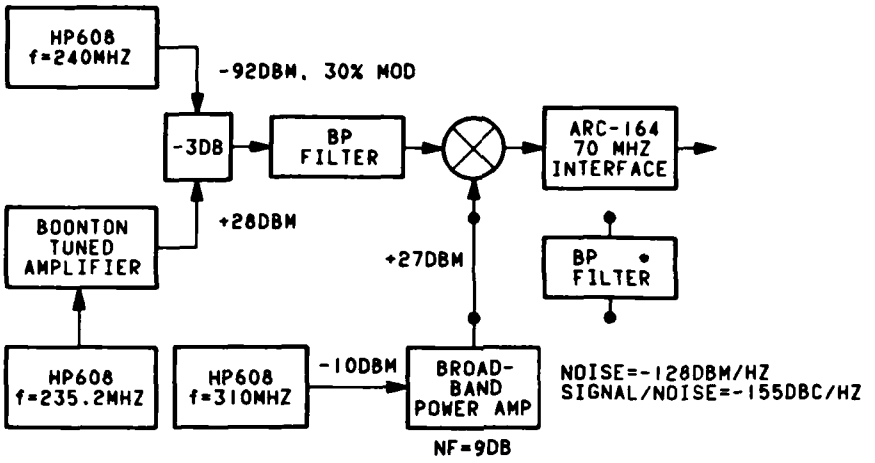
F_{LO} = 310 MHz @ 27 dBm

F_J = 235.2 MHz at +20 dBm

(See Figure 28)

VCO Design Parameters

The single-sideband phase noise characteristics that are required to meet the interference rejection levels specified for the receiver are almost entirely dependent on the phase noise performance obtainable from the voltage controlled oscillator that generates the receiver first injection frequency. This is true for offsets from the carrier of approximately 5 kHz to 20 MHz. Above 20 MHz, if required, output circuit tuning can further reduce the noise. In designing the VCO, it is therefore necessary to determine the performance limiting effects that can be expected and how closely the requirements determined in the prior section can be realized. Accordingly, the following discussion identifies the major factors contributing to VCO phase noise and what can be achieved in the way of performance.



Bandpass filter Bandwidth (3 dB) (MHz)	Number of Poles	Attenuation (EST) 4.8 MHz away from 310 MHz (dB)	Carrier-to-noise Ratio (EST) 4.8 MHz Away from 310 MHz (dBc/Hz)
No Filter	--	--	-155
6.2	5	18	-173
4.6	2	12	-167
5.5	1	8	-163

Figure 28. Test connections for local oscillator filter tests

The phase noise sidebands exhibited by an oscillator are primarily determined by:

(1) The loaded Q of the resonator.

(2) The noise generated by the active device at both low and high frequencies. That is at baseband frequencies up to the half-bandwidth of the loaded resonator and at the frequency of oscillation.

Within this bandwidth, the relationship between the single sideband power in a 1-Hz bandwidth at offset frequency of (Psfo) and the total output power (Pc) is:

$$\frac{Psfo(1Hz)}{Pc} = 1/8 \left(\frac{Vn}{V1}\right)^2 \left(\frac{fc}{fo}\right)^2 \left(\frac{1}{\text{Loaded Q}}\right)^2$$

$$= 1/8 \left(\frac{Vn}{V1}\right)^2 \left(\frac{fc}{fo}\right)^2 \left(\frac{1}{Qun} + \frac{Pc + Pin}{(2\pi f_c)\ (0.5\ Cr\ V_r^2)}\right)^{2*}$$

where: Vn is the active device equivalent noise voltage in a 1-Hz bandwidth at frequency, fo, referred to the active device signal limiting port. V1 is the oscillation maintaining feedback signal at the active device signal limiting port. The oscillator output frequency is fc. The offset frequency of Psfo is fo. Qun is the unloaded Q of the resonator. Pc is the output power taken from the oscillator. Pin is the power fed back to the active device input. Cr is the total capacitance of the resonator including all parasitic elements. Vr is the peak RF voltage across Cr.

The 1st factor is indicative of the phase jitter that is introduced in the oscillation maintaining signal by the noise signal generated by the active device.

The 2nd factor is simply a scaling factor taking into account the oscillator operating frequency.

The 3rd factor is the ratio of the total power extracted from the resonator to the total reactive "power" present in the resonator. That is, the reciprocal of the loaded Q.

The relationship is valid for offset frequencies below the loaded resonator half-bandwidth frequency, provided that the noise voltage, Vn, is adjusted to account for flicker noise effects at low frequency offsets. Above the loaded resonator half-bandwidth frequency the noise sidebands are additionally reduced by 6 dB per octave provided that the output signal is derived directly from the resonator.

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* D. Schere, "Today's Lession - Learn About Low-Noise Design", Microwaves (April 1979)

Within the passband of the resonator, a minimum threshold level will be set by the loaded resonator thermal noise resistance. The equivalent noise voltage of this source in conjunction with the amplitude of the resonator RMS voltage swing define the maximum oscillator output signal-to-sideband noise ratio that is obtainable.

The active device also contributes a wideband noise signal that will generally be larger than the resonator noise.

Resonator Characteristic

The equation defining the loaded Q of the resonator is:

$$\frac{1}{Q} = \frac{1}{Qun} + \frac{Pc + Pin}{(2\pi fo)(0.5\ Cr\ Vr^{2})}$$

This expression shows the desirability of maximizing both the resonator tuning capacitance and the voltage swing across the resonator while minimizing the feedback and output power taken from the resonator. In this design, where both the close-in and far-out phase noise are important this presents a conflict. High-power output is desirable from the viewpoint of minimizing the effects of the noise introduced by the succeeding amplifiers. This amplifier noise may be the most significant noise source outside of the oscillator bandwidth at least up to an offset frequency where tunable filtering has an effect.

The maximum oscillator power output that can reasonably be expected is about +20 dBm and then only if a resonator peak voltage swing of about 20 volts can be obtained. A total tuning capacitance of about 80 pf would then result in a resonator loaded Q of 400, neglecting all other Q degrading effects.

If this is attainable, a wideband output phase noise floor of perhaps -190 dBc is possible assuming a 4-dB noise figure for the succeeding amplifier. Tuning of the amplifier stages could further reduce this floor outside of the tuned bandwidth.

Active Device Characteristics

Consideration of the important resonator characteristics leads to a definition of the desired active device parameters other than, of course, good RF characteristics:

(1) High breakdown voltage.

(2) Low-noise figure at frequencies below 1 MHz.

(3) A signal limiting mechanism that does not introduce excessive Q degradation of the resonator and maximizes the ratio of V1 to Vn.

(4) An output impedance that does not unduly degrade the resonator Q.

(5) A power gain of at least 10 since any feedback power subtracts from the available output power.

In order to provide a reference of obtainable performance within the resonator bandwidth, consider an oscillator with the following parameters:

Vn = 3nV/Hz (Typical low-noise FET noise voltage referred to input)

V1 = 1 VRMS (FET input limiting voltage)

fc = 400 MHz (Center frequency)

fo = 100 kHz (Offset frequency)

Loaded Q = 200 (Includes power out and feedback power losses)

This loaded Q allows for 100 mW oscillator power output and equal losses from all other sources associated with the resonator.

Then:

$$\frac{Psfo(1\ Hz)}{Pc} = \frac{1}{8}\left(\frac{3\times10^{-9}}{1} \times \frac{400}{0.1} \times \frac{1}{200}\right)^2$$

$$= 4.5 \times 10^{-16} \text{ or } -154 \text{ dBc}$$

Since the power ratio varies at 6-dB per octave of offset frequency, the expected phase noise characteristic of this oscillator would be as shown in Figure 29 up to an offset frequency fo approximately 600 kHz where the thermal noise of the active device becomes predominant. Above 1 MHz the bandwidth of the resonator then introduces an additional 6 dB per octave cut-off. Also included in Figure 29 is the estimated level required for the EMC Technology Transceiver.

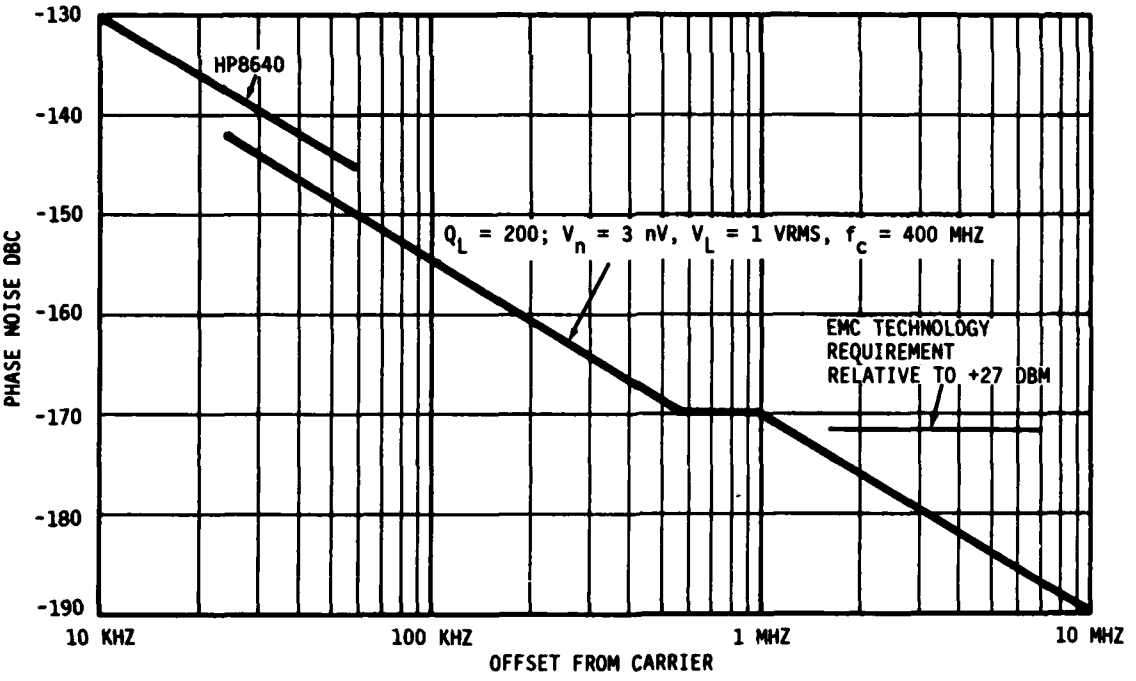

Figure 29. SSB phase noise estimation

It would be relatively easy to obtain this level of performance in a fixed tuned or mechanically tuned oscillator at 400 MHz. (Compare the characteristics of the HP8640 cavity oscillator which has similar performance down to -145 dBc at which point other circuits determine the phase noise.) However, with present day components, a wideband varactor tuned VCO with this level of performance is not feasible.

Considerations of large resonator voltage swing and Q dictate that any varactor used must be heavily reverse-biased to prevent forward conduction and operation in low-Q regions. Consequently, the amount of varactor reactance change that can be obtained is severely limited. This, in turn, restricts the resonator tuning range obtainable with a varactor to only a few percent.

The total tuning range can be extended by switching appropriate amounts of fixed reactance into the resonator circuit to generate step changes of the oscillator frequency, with the varactor providing continuous tuning within the step intervals. This approach is particularly appealing if a binary form of reactive element switching is used. Four switched elements are then capable of introducing 15 equal tuning steps.* This condition occurs when the resonator tuning capacitance is held constant and the tuning is obtained by switching shunt inductors across the parallel resonator circuit.

The limitation to this approach is determined by the resonator Q degradation caused by the resistive losses in the switches used to introduce additional reactance into the resonator circuit. The problem is aggravated by the desirability of having a low-reactance resonator circuit, which increases the Q degrading effect of the switch resistance.

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* This technique was used by Hewlett-Packard in the Synthesized Signal Generator, HP 8662A

For example, in the preceding example a reasonator reactance level of about 5 ohms (80 pf) was suggested as suitable at 400 MHz for a 100-mW output power level. If such an oscillator was designed to tune from 320 to 400 MHz in steps of 10 MHz (increments of 10, 20 and 40 MHz) the largest tuning step required would be from 320 to 360 MHz. If the resonator tuning capacitance was held constant at 80 pf, then the parallel inductive reactance to be switched in needs to be about 26 ohms at 360 MHz for resonance to shift to 360 MHz. A switch resistance of 0.5 ohm results in a Q of 52 for switched elements. The maximum Q of the resonator is then about 250, neglecting all other losses. In this case paralleling two switches would give a resonator Q of 500 and allow a practicable solution. If, however, a tuning step from 220 to 310 MHz is considered at the same capacitance level (C_T = 80 pf) the switched inductive reactance is about 13 ohms giving a Q of 26 for a 0.5 ohm switch. The total resonator reactance is 6.4 ohms and the maximum resonator Q is about 100. Five parallel switches would then be required to increase the Q to 500. This would be adequate considering only the one switch. If the loading due to additional switches is taken into account, an even lower switch resistance must be obtained to provide a viable solution.

Based on these considerations it appeared to be impracticable to tune one oscillator over the 225 to 400 MHz range, while maintaining a minimum resonator loaded Q of 200 and an output power of 100 mW.

A VCO was built, using these principles, to cover the frequency range of 225 to 470 MHz in 5 bands using PIN diode switching of the inductive elements to maintain the required Q. Stripline and tuned coaxial elements were evaluated for the inductors with the coaxial approach being somewhat easier to integrate with the diode band switching requirements.

This VCO, using a power field effect transistor and operating at a power level of 2 watts, had a noise floor capable of meeting the radio requirements as previously determined and a modified version of this VCO was eventually used in the experimental model transceiver and is described further in Section 3.

SECTION III
EXPERIMENTAL MODEL DEVELOPMENT

EXPERIMENTAL MODEL DESIGN (MECHANICAL)

The mechanical approach used for the experimental model UHF transceiver is the modular slice concept as used in the basic AN/ARC-164 radio. This mechanical package has demonstrated excellent compatibility with airborne environments such as temperature, vibration, and mechanical shock and has also demonstrated excellent EMC characteristics with interslice shielding and overall case electrical continuity.

In this mechanical approach each functional module is packaged in a self-contained modular "slice" that is protected by an aluminum frame which also provides shielding for electromagnetic integrity. Each mating surface of these aluminum frames contains a groove for EMI gasketing. The gaskets are made of monel mesh formed to fit the grooves and are compressed when the radio is assembled.

There are a total of seven modules, all of which are approximately 5 inches wide. The synthesizer, VCO, and receiver are each 7½ inches high, while the transmitter and data converter are each 4 3/4 inches high. The audio amplifier and power supply, which are mounted above the data converter and power supply respectively, increase the height above these modules to the 7½ inch outline (see Figure 30). The overall radio length is about 11 1/8 inches making the basic dimensions approximately those of a short-half ATR.

The basic elements that established the module height are the tubular bandpass filters in the receiver assembly. These are purchased assemblies of fixed size, and the modules are raised over a standard AN/ARC-164 module size to accommodate these filters.

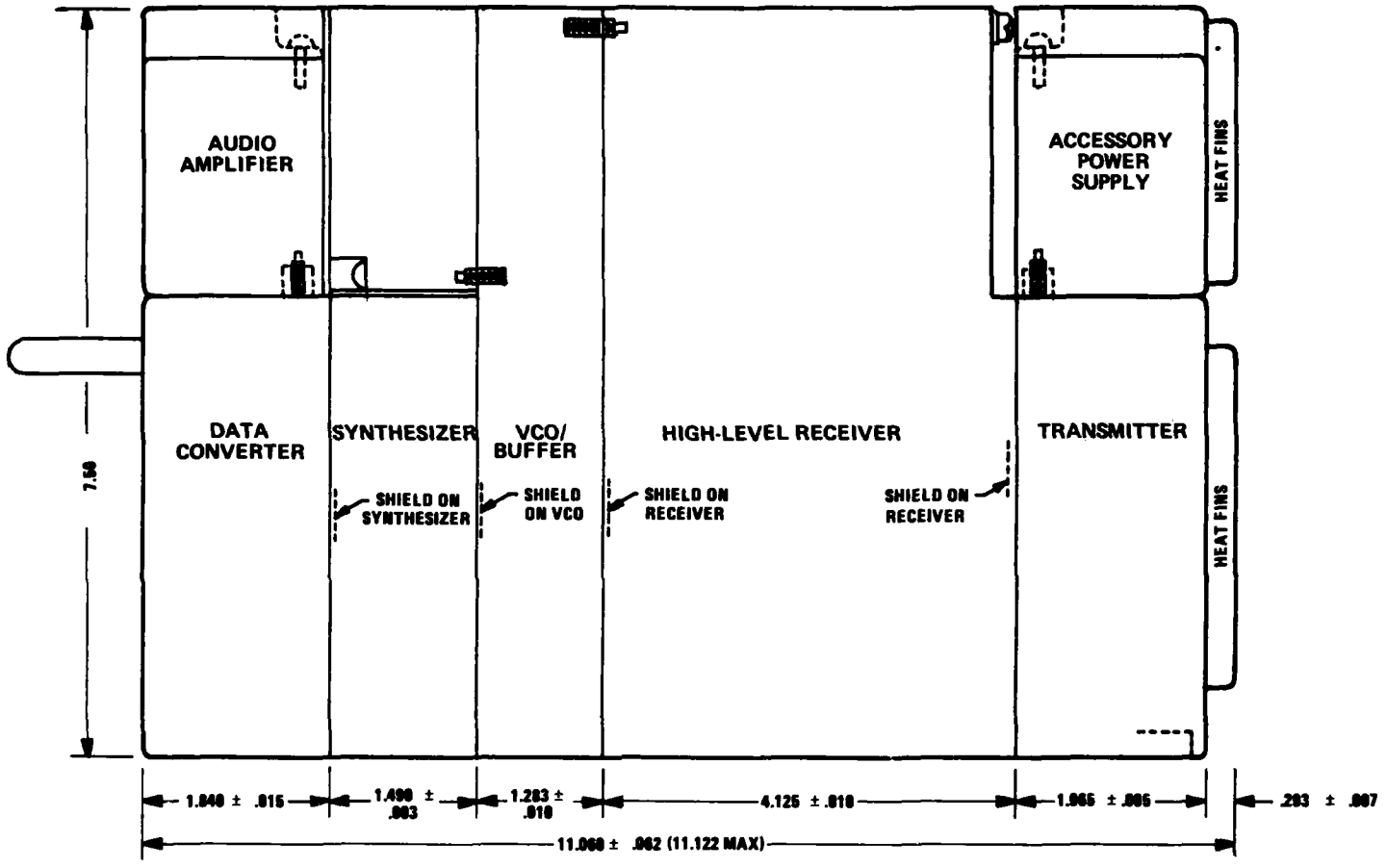


Figure 30. Experimental radio physical dimensions

The slices are mechanically joined together by four horizontal thru bolts plus four vertical bolts which hold the audio amplifier and power supply in place. Electrical connections are made to the bottom of each slice by means of a wire harness extending along the bottom of the radio and up to the power supply module at the rear of the radio. The audio amplifier has a removable connector with electrical access made through the data converter power connector. The transmitter, receiver, and VCO modules use filtered connectors and all RF interconnections are made with removeable coaxial cable.

The slices are designed such that heavy components are located near the periphery of each slice. The PW boards are mechanically affixed to the frames with screws, washers, and lockwashers which firmly support and ground the boards. Standup shields which further increase the printed wiring board stiffness and provide low-impedance grounds are used on the PW boards. Double-sided printed wiring boards are used in the model for most assemblies. Where necessary, additional interconnections on the boards are made by "green wire" connections. All loose wires, large components and vibration sensitive RF components are secured by RTV cement.

The weight of the complete experimental model radio is 18½ pounds. Finish is standard flat black with white marking. The experimental model radio is shown in Figure 31.

EXPERIMENTAL MODEL DESIGN (ELECTRICAL)

The Experimental Model EMC Transceiver is an amplitude modulated (AM) receiver-transmitter providing operation on any frequency selected from the 7000, 25-kHz spaced channels between 225.000 and 399.975 MHz. The radio set is designed to meet the electrical specifications of Table 13 and is compatible with the usual line of sight command radios. The transceiver is designed for airborne use.

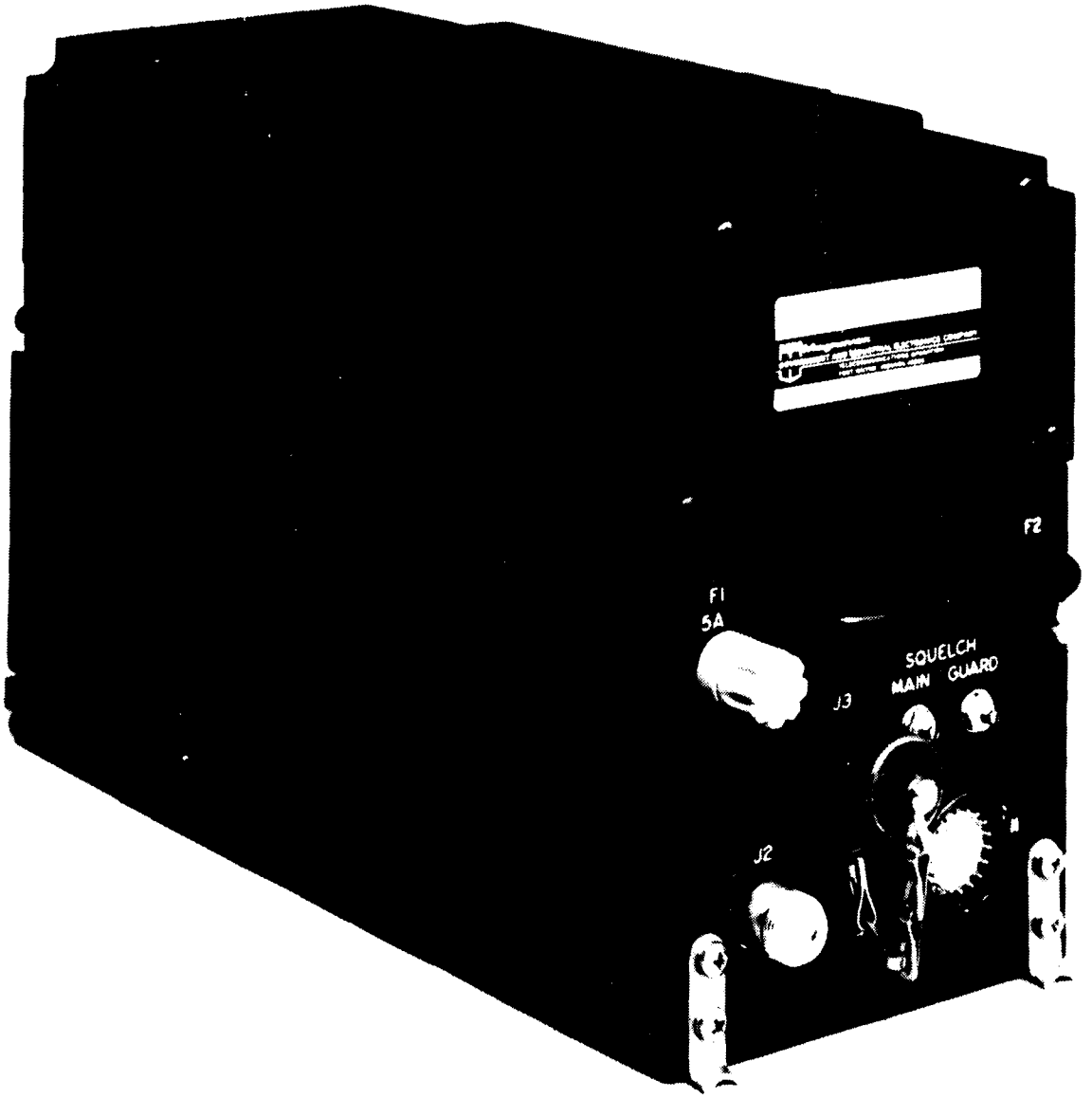


Figure 31. Experimental radio

TABLE 13. ELECTRICAL PERFORMANCE CHARACTERISTICS

Item	Characteristic
Frequency Range	225 to 400 MHz
Tuning Interval	25 kHz (7000 channels).
Tuning Control	Synthesizer using manual, and present control, tuning time shall not exceed 0.25 seconds.
Transmitter Power Output	10 watts into 52-ohm load (nominal)
Modulation Capability	Tone and amplitude modulated voice (minimum of 80% negative and 80% positive modulation).
Transmitter Spurious Outputs	
Within $f_o \pm 15$ MHz	-110 dBc (Where f_o is the transmitter carrier frequency)
From $f_o \pm 15$ MHz to 400 and 225 MHz	-130 dBc.
Transmitter Broadband Noise	
From $f_o \pm 100$ kHz to $f_o \pm 15$ MHz	-70 dBm/Hz at $\pm$ 100 kHz decreasing at a rate of 20 dB/decade to -125 dBm/Hz at $f_o \pm 15$ MHz
from $f_o \pm 15$ MHz to $f_o \pm 35$ MHz	-125 dBm/Hz or less
From $f_o \pm 35$ MHz to 400 and 225 MHz	-133 dBm/Hz or less
Receiver Sensitivity	-95 dBm (or lower) input for 10 dB $\frac{S+N}{N}$ output. The input signal shall be modulated 30% at a 1-kHz rate.
Receiver Degradation	No more than 3 dB of degradation from a modulated interfering signal of +20 dBm located as close as 2% of any tuned frequency in the 225 to 400 MHz range.
Input Impedance	52 ohms (nominal).
Receiver Spurious Responses	Greater than 70 DB down from the response at center frequency.
Frequency Accuracy	The center frequency of the transmitter/receiver shall not deviate more than $\pm$ 0.0025 MHz from the nominal frequency of the channel selected.

Control of the EMC Technology Transceiver is by means of a standard AN/ARC-164 radio set control such as the C-9533. This control box provides for frequency selection, preset channel operation, and the ON/OFF switching function.

A block diagram of the experimental EMC Transceiver is shown in Figure 32. This block diagram shows the various modules within the RT unit and their functional relationships. The following paragraphs offer a functional description of the experimental EMC technology transceiver. Control and power connector pinouts of the experimental transceiver are the same as the remote ARC-164 Radio, RT-1145.

Reception

During reception, incoming signals from the antenna are routed through the receive/transmit switch in the Transmitter Module before application to the receiver circuits. The receiver circuits consist of the RF Front End Assembly and the IF/Demodulator. These assemblies together form a receiver system operating over the frequency band 225.000 to 399.975 MHz that provides for voice AM, tone AM, or secure AM reception.

In the receiver, the received signal is passed through either a bandpass filter passing the frequencies 225 to 300 MHz or a filter passing the frequencies 300 to 400 MHz. These filters are switched in and out according to the operational frequency selected. In addition, this assembly contains a tuned trap to reduce the amplitude of the receiver injection signal leakage to the antenna.

The RF signal from the selected bandpass filter is routed to a high-level mixer that down-converts the incoming RF signal to an IF frequency of 70 MHz. The output of the mixer is passed through a high-level amplifier which, together with the mixer and filter losses, establishes the noise figure of the receiver. The output of the amplifier is passed through an 8-pole crystal filter at 70 MHz, which is followed by another high level 70-MHz amplifier before being passed on to the IF/Demodulator Assembly.

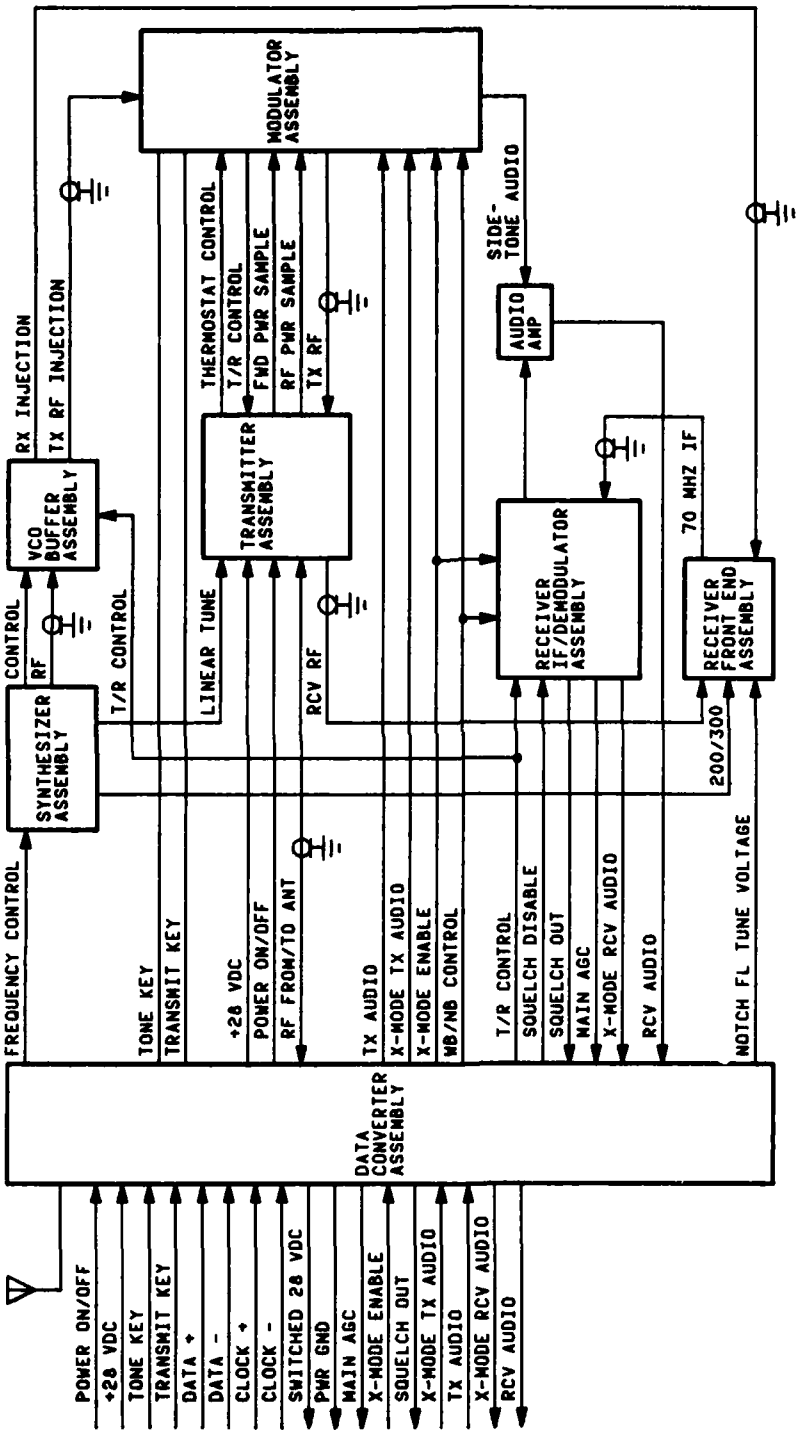


Figure 32. EMC experimental transceiver block diagram

The receiver injection signal is supplied by the VCO/Buffer Assembly at a level of +27 dBm. A high-side injection approach is used in the receiver with injection at 295 to 469.975 MHz.

In the Receiver IF/Demodulator Assembly, the 70-MHz signal is further down-converted to an IF frequency of 30.112 MHz where the signal is passed through a narrowband crystal filter. Following the crystal filter are the IF amplifiers and AM demodulator circuits. These functions are provided by a single integrated circuit.

A noise operated primary squelch system is used. The squelch level is adjustable from the front panel. On/Off control of the squelch function is provided from the control box. Audio circuits include a wideband amplifier for operation in secure voice mode and a common transmitter sidetone/receiver normal mode audio amplifier.

Transmission

The tranmission circuitry is contained in the Modulator Assembly and the Transmitter Assembly. The Modulator Assembly is physically located, along with the Power Supply, within the Transmitter Assembly. The Modulator Assembly contains the audio processing circuits, tone oscillator, the low-level RF stages, and a voltage variable attenuator used for automatic level control (ALC) and for impressing AM modulation on the carrier.

The Transmitter Assembly also contains the broadband power amplifiers, output lowpass filter, the receive/transmit antenna switch, and a directional coupler.

In the transmit mode of operation, the VCO buffer assembly provides a nominal +3 dBm signal, at the desired operating frequency, to the Modulator where the RF signal is amplitude modulated by a voice (or secure voice) signal that has been amplified, clipped, and filtered prior to being applied to the modulation circuitry. Following modulation, the RF signal is passed through an RF amplifier and applied to the Transmitter Assembly for still further amplification.

In the Transmitter Assembly, the signal is amplified to a nominal carrier level of 10 watts before being applied to the output low-pass filter and the receive/transmit switch. Following the receive/transmit switch is a directional coupler which samples the forward and reflective components of the transmitter output. The samples are injected into a feedback loop located on the Modulator Assembly, where they are compared with preset reference levels to form a control signal that maintains constant output power across the frequency band. During amplitude modulation, the feedback loop also linearizes the transmitter to minimize envelope distortion. In addition, the feedback loop protects the power amplifier from damage due to excessive load VSWR.

The demodulated AM envelope from the incident power sample of the transmitter output is used to provide sidetone in AM voice or tone operation. The sidetone audio is routed to the audio amplifier assembly for amplification. The sidetone circuit is disabled in secure voice operation.

Frequency Synthesizer/VCO

Frequency synthesizer functions are accomplished by circuitry located in the VCO Assembly and Synthesizer Assembly. The frequency synthesizer circuits generate the transmitter RF injection and main receiver first injection. The synthesizer also contains a digital to analog converter which generates the tune voltage for the electronically tuned filters in the transmitter. Tune data is supplied to the synthesizer on parallel inputs from the Data Converter Assembly. The Synthesizer Assembly also contains the TCXO and digital divider circuitry required for the synthesizer function.

The VCO Assembly contains the high-power VCO and buffer amplifier required to generate the transmitter and receiver injection at the required level and spectral purity.

Data Converter Assembly

The Data Converter Assembly converts incoming serial data from the control box to the various control signals required by the other modules in the radio set. All audio signals and primary power are also routed through the Data Converter Assembly. The data converter assembly also contains the antenna connector. The PROM for control of the receiver LO notch filter frequency is located within the Data Converter.

The Data Converter Assembly is the front panel for the EMC Technology Transceiver. It provides interface between the remote control box and the radio set. The receiver squelch adjust is also in the assembly.

The Data Converter Assembly (see Figure 33) is used to convert the serial data input from the control box to the parallel control lines required by the radio set. The functions controlled are:

(1) Synthesizer frequency
(2) Bandwidth control
(3) Squelch disable
(4) COMSEC mode

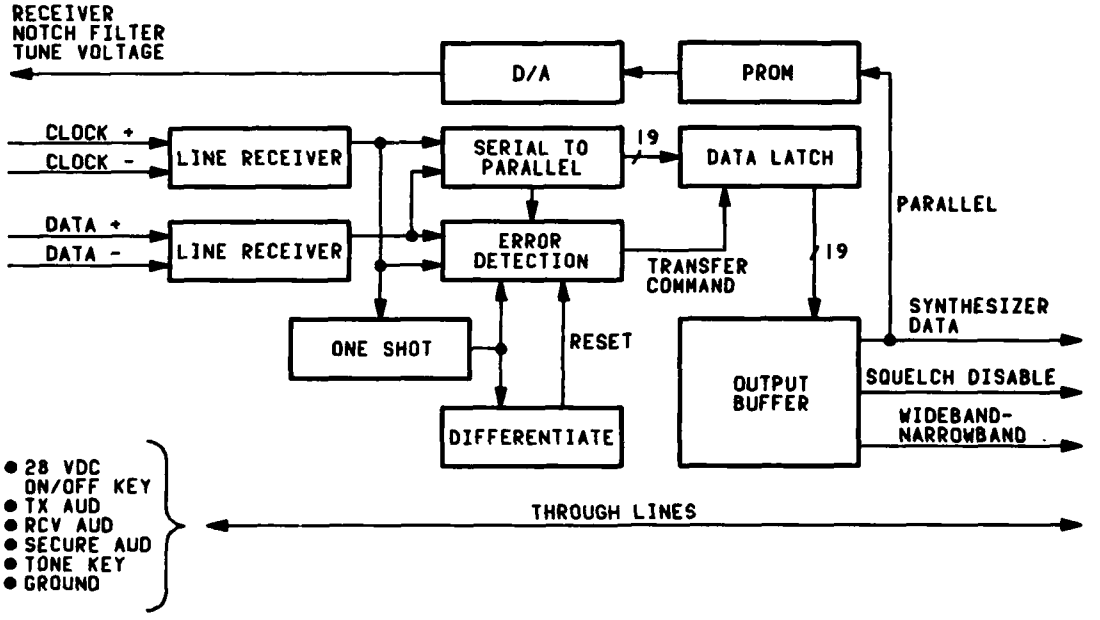


Figure 33. Data converter assembly block diagram

Most of the circutry in the Data Converter Assembly is similar to the same circuitry in the AN/ARC-164. The serial data stream is a 32-bit stream. Error protection is provided in that, two consecutive identical words have to be received before the data is latched out to the radio set. Synchronization is achieved by the absence of 8 clock bits.

In addition, the +28 volt power for the radio, transmit key control, and all audio signals are routed through the Data Converter Assembly.

Power Supplies

The DC voltages required by the circuitry in the EMC Technology Transceiver are supplied by a switching mode regulator module located in the Transmitter Assembly and a second unit mounted on top of the transmitter slice. The power supplies are the same as that used in the standard AN/ARC-164 transceiver. This switching mode regulator has been used in prior EMC studies and has proven satisfactory. Due to the increased current requirements of the VCO and PIN switch circuits in the receiver, the second power supply was required.

The following paragraphs present a discussion of the critical assemblies in the Experimental Model Transceiver.

Receiver Design

The receiver used in the EMC Technology Transceiver uses many of the techniques developed on this and prior RADC Study Contracts to achieve the required high-dynamic range. The receiver circuits are contained in two basic sub-assemblies which are the RF Front-End Assembly, and the IF/Demodulator Assembly. The receiver RF front-end design is essentially that previously described in the receiver study phase as the single conversion front end.

The receiver is a dual-conversion design with a 70 MHz first IF and a 30.112 MHz second IF. These IF frequencies are the same as have been used in the AN/ARC-164 receiver and have been shown to be superior in terms of spurious frequencies, image rejection, and crystal filter requirements.

The receiver is required to produce an output signal with a 10 dB signal plus noise-to-noise ratio with an input of -95 dBm at 30 percent modulation. This translates to a required noise figure of between 20 and 21 dB based on an assumed audio bandwidth of 3 kHz. The noise figure is reached with some margin with a noise figure of about 15 dB being achieved.

The receiver uses a high-side injection scheme wherein the injection frequency varies from 295.000 to 469.975 MHz. The ratio of receive frequency to local oscillator frequency for these combinations of frequencies varies from .76 to .85, and based on a mixer spurious analysis, the worst case mixer spurious signal in this band is a 7th order product.

The image rejection, which is greater than 75 dB at all frequencies, is determined by the pin switched tubular filters in the RF Front End Assembly. Other spurious responses are at least 73 dB down.

The out-of-band signals are rejected by a 70-MHz crystal filter in the RF Front-End Assembly and are further rejected by crystal filters in the Receiver IF/Demodulator Assembly. The limiting parameter for intermodulation and cross-modulation has always been the linearity of the front-end stages of a receiver. In this case, these circuits include the receiver mixer and first 70 MHz IF amplifier. Since there is no gain ahead of the first mixer, the problem is minimized. A high-level mixer is used with a correspondingly high-injection level (+27 dBm). Following the mixer is a high-level J-FET amplifier, crystal filter, and second J-FET amplifier. The goal was to achieve an intercept point prior to the 70-MHz crystal filter of at least +27 dBm to minimize sensitivity to intermodulation and cross-modulation interference.

Figure 34 is a diagram of the receiver dynamic range characteristics. On the diagram are traced the respective levels of a -95 dBm input signal on-channel, a -30 dBm signal on-channel, and a +20 dBm interferring signal. Based on this chart, the required dynamic ranges of the various amplifiers are established to assure that no limiting will occur within the receiver. The effects of the various filters in the receiver are graphically shown as the off-channel interference signal is substantially attenuated as it passes through the receiver.

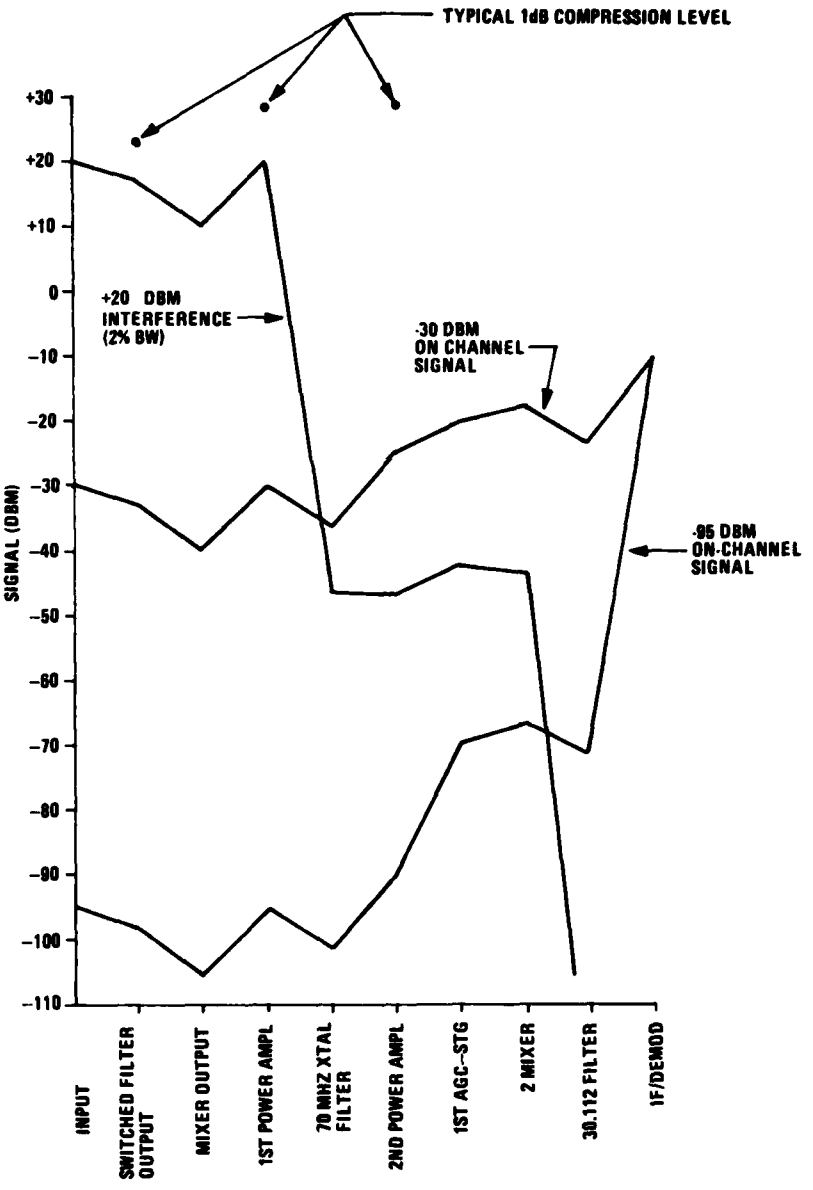


Figure 34. Receiver dynamic range

Receiver RF Front-End Assembly

Figure 4 shows a block diagram of the Receiver RF Front-End Assembly.

The RF Front-End Assembly contains two bandpass filters covering the frequency ranges of 225 to 300 MHz and 300 to 400 MHz. These filters are switched in and out, using PIN switching diodes, corresponding to the selected operating frequency band. A diode switch section is shown schematically in Figure 5. The switch driver circuitry is also located in the RF Front-End Assembly. The function of the filters is to attenuate frequencies outside these bands; these filters provide the basic image rejection of the receiver.

Following the switched filters is a 70-MHz series resonant trap to attenuate any 70-MHz signals at the input to the receiver and also a two-section tracking notch filter. The tracking notch filter is a notch at the local oscillator frequency and is used to attenuate the local oscillator signal, which is conducted back through the double-balanced mixer, to prevent local oscillator reradiation. Tune voltage for the varactors of the notch filter is developed by a PROM located in the data converter module. Third order intermodulation products developed by the notch filter are greater then 70 dB below the input signal operating in the notch passband. Attenuation at the desired channel frequency and at the LO frequency is shown in Table 6. This also shows the control voltage and notch bandwidth. A schematic diagram of the notch filter is shown in Figure 7. Following the tracking notch filter is a low-pass filter which attenuates high-level harmonics of the LO which are generated in the mixer. These harmonic levels as measured on the "R" port of the mixer with a +27 dBm local oscillator signal are shown in Table 2. Without the filter, these harmonics would also be conducted to the antenna and be radiated.

The two bandpass filters are purchased assemblies. These filters have a typical in-band insertion loss of 0.5 dB and are 7-pole designs.

The incoming signal from the low-pass filter is applied directly to a high-level mixer which down-converts the incoming signal to an IF freqency of 70 MHz. The mixer uses a +27 dBm local oscillator signal which is supplied by the synthesizer/VCO modules and is designed to handle input signals up to +20 dBm, a diplexer is used after the mixer to terminate the mixer at all frequencies of interest, thus reducing intermodulation products otherwise generated in the mixer. The diplexer mixer circuit is shown in Figure 35.

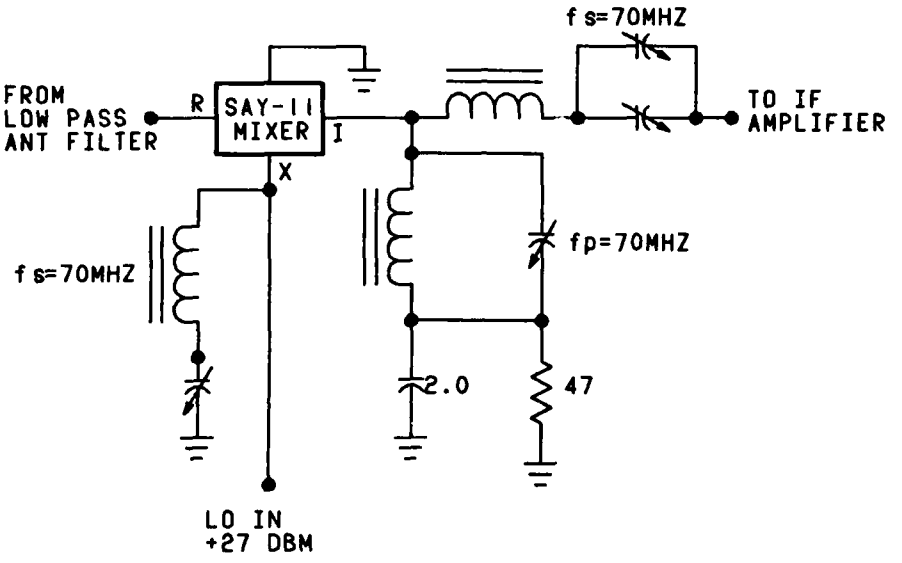


Figure 35. Diplexer-mixer schematic diagram

Following the mixer and diplexer is a J-FET power amplifier circuit (Figure 9). This amplifier helps to achieve the receiver noise figure prior to additional losses in the receiver. This amplifier has an output intercept point of approximately +27 dBm.

Following the power amplifier is an 8-pole crystal filter which substantially attenuates out-of-band signals. This filter has a bandpass response as shown in Table 8. This filter is followed by another J-FET power amplifer identical to the first. The input impedance of the J-FET amplifiers is very close to 50 ohms resistance and thus properly terminates the diplexer and crystal filter.

Receiver IF/Demodulator Assembly

Figure 36 is a block diagram of the EMC Technology Receiver IF/ Demodulator Assembly. Applicable portions of the main receiver module from the AN/ARC-164 transceiver are used to perform this function. This circuit was used satisfactorily in all prior testing on the receiver technology development contract and performed well on the study phase of this contract.

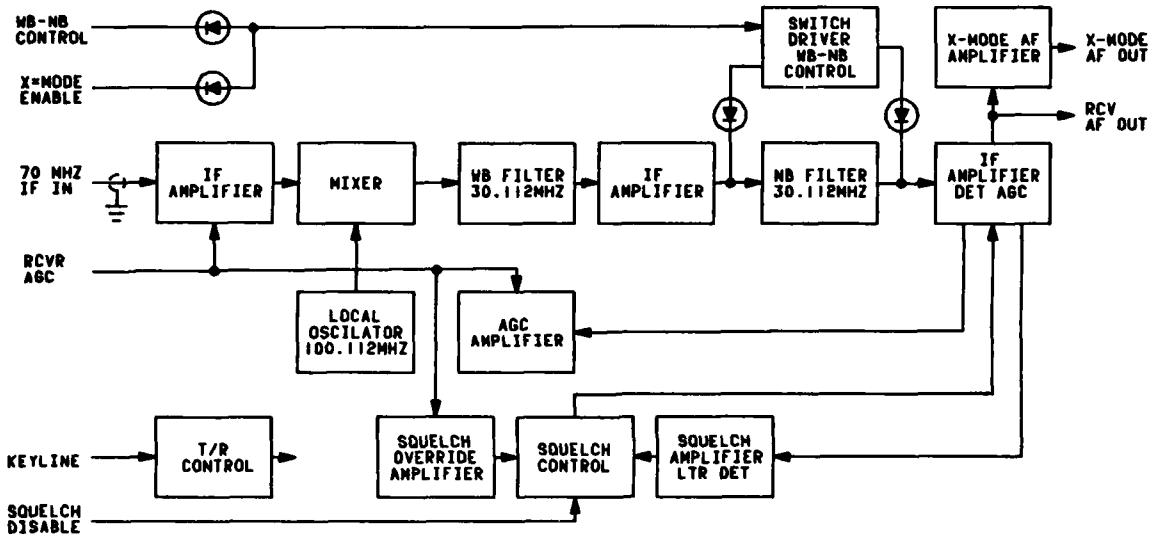


Figure 36. Receiver IF/demodulator assembly block diagram

The 70-MHz IF signal is passed through an IF amplifier which has AGC capability. The output of this amplifier is supplied to a mixer which down converts the 70-MHz signal to an IF frequency of 30.112 MHz. The local oscillator for the mixer is supplied by a 100.112 MHz crystal oscillator. The significant feature of this crystal oscillator is that only one harmonic of the oscillator frequency occurs in the receiver frequency band of 225 to 400 MHz. The oscillator circuit is shielded and bypassed to reduce the effects from this harmonic signal.

The Receiver IF/Demodulator Assembly contains 2 narrowband crystal filters. 1 crystal filter is approximately 80-kHz wide, and the other filter is approximately 25-kHz wide. The narrower crystal filter is used for operation in normal AM voice and baseband secure speech operations. For diphase secure voice operation, the narrowband crystal filter can be switched out.

Following the crystal filters, the 30.112 MHz IF signal is applied to an integrated circuit which contains IF amplification and the AM detector. An IF signal is also applied to a second integrated circuit which contains a limiter-amplifier and FM discriminator detector. The latter circuit is used to detect amplifier noise which controls the noise operated squelch circuit. A back-up (CLIMAX) squelch circuit is AGC operated and becomes effective with approximately 20 microvolts RF input at the antenna.

The demodulator circuit has an audio output for normal speech operation and an X-mode audio output for secure speech operation. The low-level, normal speech audio signal is routed to the audio amplifier module for amplification and shaping. Power output is set to approximately 6 volts across a 150-ohm termination. A 600-ohm output can also be selected by means of jumper connections within the audio amplifier module. Frequency response of the normal audio channel is 300 to 3500 Hz and distortion is 5 percent maximum. The X-mode audio level is 2 volts nominal (500 ohms), 70 Hz to 20 kHz.

Transmitter Design

The transmitter circuits are contained in the Modulator Assembly and the Transmitter Assembly. The modulation approach used is the conventional modulator as used in the ARC-164 radio. The approach which had shown promise during early transmitter tests wherein PIN diode modulation was performed at a high level to reduce broadband noise was not used in the experimental model transceiver due to IFM to the high power VCO by modulation peaks. Resistive isolation and amplification was required between the VCO output and the PIN diode modulator to avoid the IFM and the noise

improvement was reduced. Because of this it was decided to use the standard level modulator approach. Broadband noise improvement with the approach used is obtained by tuned bandpass amplifiers in the low-level stages preceding the modulator and a tuned emitter power amplifier following the modulator.

During this and prior studies, effort was expended on investigations of a tracking filter (high level VCO phase-locked-loop) as the transmitter drive source. The advantage of such an approach is that it can be used in a system to "clean-up" an existing synthesizer. In the EMC technology Transceiver, a new synthesizer system was designed, and it includes a new high-power, low-noise VCO.

The Modulator Assembly contains all of the audio processing circuitry and the AM modulator. Varactor tuned filters are included in this assembly to reduce the spurious and broadband noise levels. The transmitter automatic leveling control circuitry is also contained in this assembly. The Transmitter Assembly contains the RF Power Amplifier circuits that are required to raise the output of the Modulator Assembly (nominally +20 dBm) to the required 10-watt Carrier level. The Transmitter Assembly also contains the output low-pass filter, the antenna receive-transmit switch, and a dual directional coupler that is used to provide the control inputs to the transmitter automatic level control circuit and transmitter protection circuit. The primary switching mode regulator power supply is also contained in the Transmitter Assembly.

Modulator Assembly

A block diagram of the Modulator Assembly is shown in Figure 37. The audio inputs, either plain or secure, are fed to the audio amplifier and switching circuit. The latter circuit selects the desired audio input and applies it to the common audio limiter. The 1020-Hz oscillator output is also routed through this circuit.

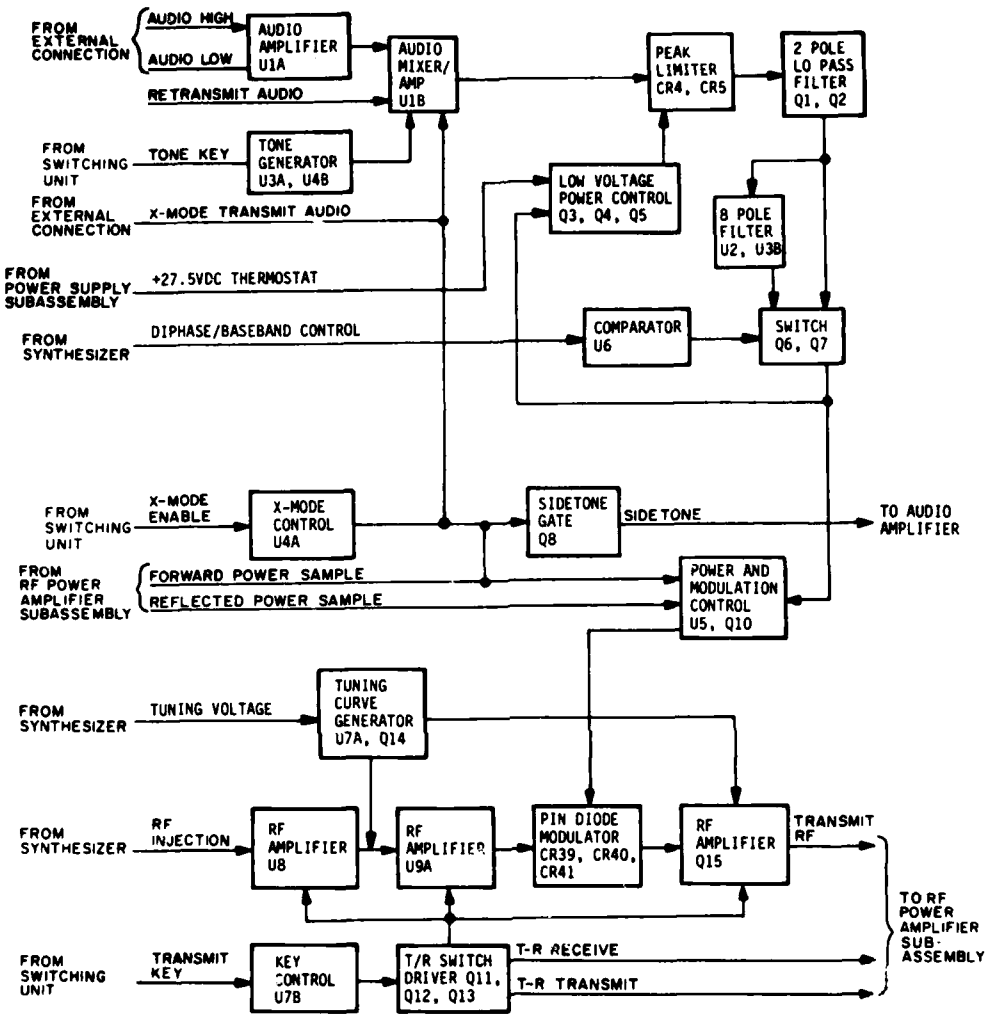


Figure 37. Modulator assembly block diagram

The switching circuit controls are a function of the baseband and diphase inputs and are generated in the diphase/baseband circuit. Either diphase or baseband secure voice mode is selected by a logic 0 on the appropriate control line. Normal audio is selected by a logic 1 on both lines.

The diphase/baseband control also selects the appropriate premodulation filter following the audio limiter.

The level control amplifier summing network combines five inputs at the base of the level control amplifier. These are the audio signal, the DC reference voltage, the detected forward power, the detected reflected power, and a transmit-receive control. The transmit-receive control adds attenuation in the PIN-diode attenuator during receive operations.

When no audio signal is fed to the summing network, the forward and reflected inputs to the network are at fixed DC levels. With this condition, these DC levels are combined and act as an automatic level control on the level control amplifier input. When an audio signal is applied to the summing network, the detected modulation envelope is superimposed on the DC level at both the reflected and forward inputs. These inputs constitute a negative feedback to the audio at the audio input.

Combining these three signals at the input of the level control amplifier has the effect of linearizing the final transmitter output with respect to the applied audio modulation.

The power control block in the block diagram is used to reduce the forward RF power when the temperature exceeds a certain limit. This is performed by one DC output of the block which is connected to the level control amplifier input. The second power control output is used to prevent overmodulation under the condition of reduced output power by changing the audio clipping level and, therefore, also the audio voltage peaks seen by the pin diode attenuator.

The RF input to the Modulator is nominally +3 dBm. This signal is amplified in a tuned bandpass amplifier and is then applied to the PIN diode attenuator. For carrier only, the RF output of the modulator is nominally +21 dBm. At 100-percent modulation, the positive modulation peaks will be nearly +27 dBm.

Transmitter keying is accomplished by a logic 0 being applied to the T/R switch circuit. A logic 0 at this input causes the PIN-diode attenuator to be set to the nominal attenuation level for transmit. A logic 1 at this input forces the PIN-diode attenuator to the maximum attention. In addition, two control signals are fed to the Transmitter Assembly to provide T/R switching for that module.

Transmitter Assembly

The RF power amplifiers in the Transmitter Assembly (see Figure 38) amplifies the modulated 0.2 watt RF signal from the Modulator Assembly to the 10-watt carrier level, which is applied to the antenna. This power amplification is obtained with two broadband amplifiers; the driver amplifier, and the power amplifier. The Transmitter Assembly also includes a T/R switch, a low-pass filter, a dual directional coupler, and a power sampler. The T/R switch is used to either route the output of the power amplifier to the low-pass filter in the transmit mode or to route the output of the bilateral low-pass filter to the receiver RF port in the receive mode. The T/R switch mode is determined by the T/R receive and T/R transmit levels which originate in the Modulator Assembly.

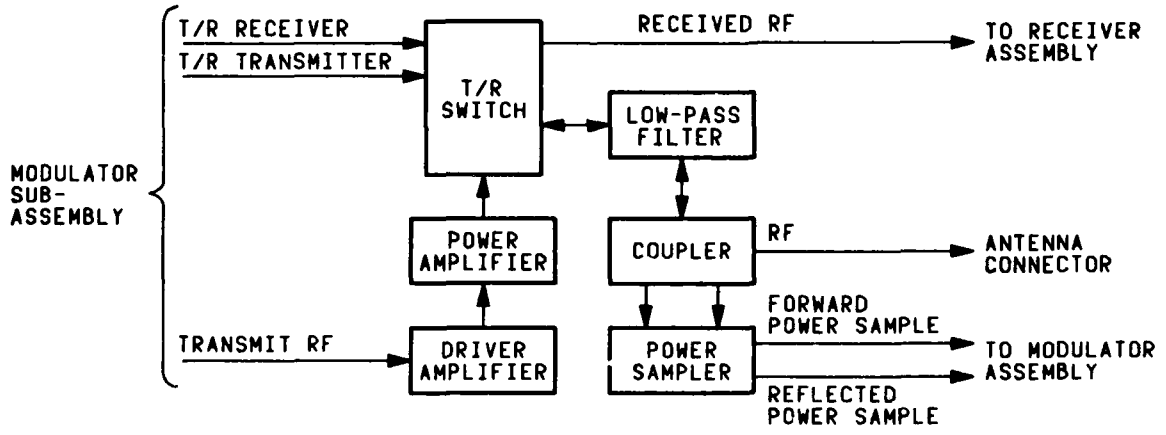


Figure 38. Transmitter assembly block diagram

The low-pass filter which follows the power amplifier and T/R switch reduces the carrier harmonics to an acceptable level during the transmit mode and provides additional image rejection in receive mode.

A dual directional coupler is connected between the low-pass filter and the antenna connector. This coupler is used to provide a sample of the forward power and any reflected power which is present. These samples are rectified and fed to the High-Level Modulator Assembly where they provide automatic level control and also linearize the RF carrier with respect to the applied audio modulation.

The power amplifiers in the subassembly are broadband from 225 to 400 MHz. The peak output power capability is 50 watts. This is required in order to achieve full amplitude modulation of the RF carrier. The power amplifier assembly from the ARC-164 radio is used as the power amplifier in the EMC Technology Transmitter Assembly. These transistors have been selected to give somewhat higher output than is required in this application.

Overall, approximately, 21 dB of gain is required. This is sufficient to overcome losses in the output low-pass filter and T/R switch. Figure 39 is a diagram showing the gain distribution in the transmitter circuits.

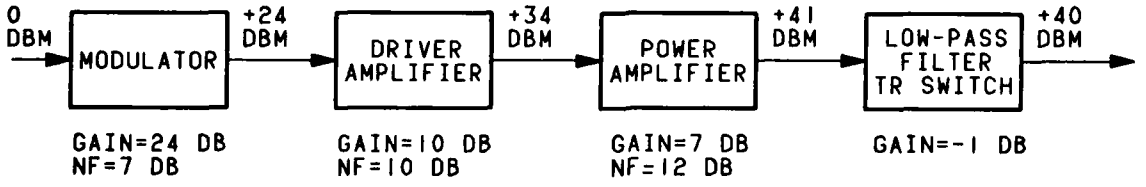


Figure 39. Transmitter amplifier chain block diagram

The noise figure of the transmitter RF chain is about 22 dB giving an equivalent input noise level of -152 dBm/Hz. The broadband noise level from the VCO Buffer Assembly is about -155 dBm/Hz. Thus the total input level is about -150 dBm/Hz. The net transmitter gain is about 13 dB, so the output noise should be about -137 dBm/Hz. This varies somewhat across the band due to variations in gain, but the specified requirement of -133 dBm/Hz is generally met.

The Transmitter Assembly also contains the primary power supply module. This is the same power supply as used in the ARC-164. Basically, it is a switching mode regulator operating at about 15 kHz. The output voltages are +12, +28, -12, +6.3 and -46 Vdc.

Frequency Synthesizer/VCO Design

The experimental transceiver Synthesizer/VCO generates the necessary LO injection signals to permit reception and transmission on the 7000 25-kHz channels in the frequency band 225.000 to 399.975 MHz.

The basic synthesizer design, essentially the same as that used in the ARC-164 radio set, is used to control the frequency of a high-power VMOS FET voltage controlled oscillator (VCO). The synthesizer is a digital phase-locked loop indirect synthesizer with all frequencies being derived from a single temperature compensated crystal oscillator (TCXO) at 3.2 MHz. The TCXO is the same as the one used in the ARC-164 radio and has a frequency accuracy of ±3 parts per million over the temperature range of -55°C to 85°C. This insures that the center frequency of the transmitter will not deviate more than ±1200 Hz from the nominal frequency of the channel selected.

The high-power FET VCO is phase-locked to the synthesizer output to provide a signal that is frequency coherent with the synthesizer output,

but has the higher output level and improved noise characteristics necessary for the injection signals for the receiver circuits in the experimental model transceiver.

In the receive mode, the VCO output is supplied as an injection signal to the receiver first mixer and is offset higher in frequency than the desired operating channel by an amount equal to the receiver first IF (70 MHz). In the transmit mode, the VCO output is supplied to the transmitter at the operating frequency.

Functional Operation

The frequency synthesizer/VCO functions are contained in two assemblies: the Synthesizer Assembly and the VCO/Buffer Assembly. The VCO/Buffer Assembly contains a five band high-power VMOS FET VCO and a low-noise FET buffer amplifier. The Synthesizer Assembly contains the reference crystal oscillator, all digital synthesizer circuits, and the loop integrator/low-pass filter. The synthesizer uses a high-speed ECL variable-modulus prescaler to divide a low-level VCO frequency (in the synthesizer) down to a lower frequency which feeds a main counter and swallow counter. This technique of frequency synthesis is fairly conventional and will not be described in detail.

A basic block diagram of the frequency synthesizer VCO system is shown in Figure 40. The basic phase locked loop synthesizer is shown in Figure 41. The logic control for the selected frequency is supplied from the Data Converter Assembly to a logic network that generates the required code for the synthesizer. The logic circuitry contains the offset count that is required to offset the synthesizer frequency by 70 MHz in the receive mode.

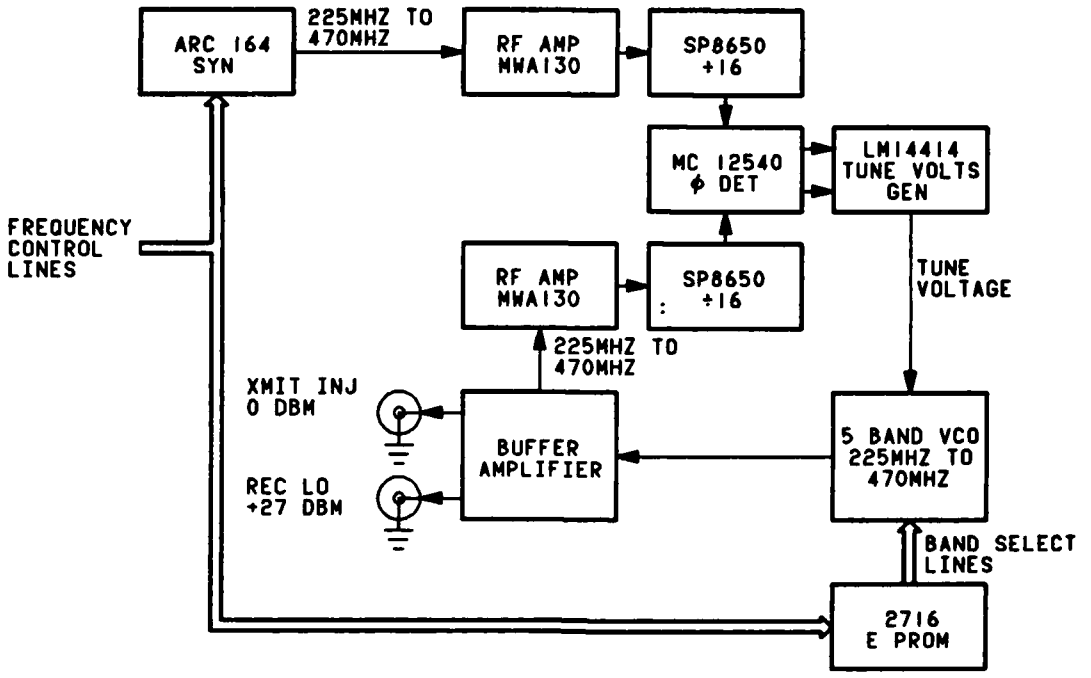


Figure 40. Frequency synthesizer/VCO block diagram

In prior RADC study contracts, the synthesizer has been found to be a source of many of the transmitter spurious signals, especially at the reference frequency rate. The techniques developed on those contracts are applied to this synthesizer design and additional filtering and RF shielding has been included as required. A principle feature is that all power into the synthesizer and VCO assemblies is post regulated within the respective module. RF filtering, shielding, and decoupling is extensive in the VCO and buffer amplifier assemblies. A filtered connector is used for power and control entry into the high-power VCO.

VCO/Buffer Assembly

The VCO/Buffer Assembly contains the most important circuit in terms of achieving the overall goals of the EMC Technology Transceiver. This assembly contains the voltage controlled oscillator which basically determines all close-in noise properties of the transmitter and is critical

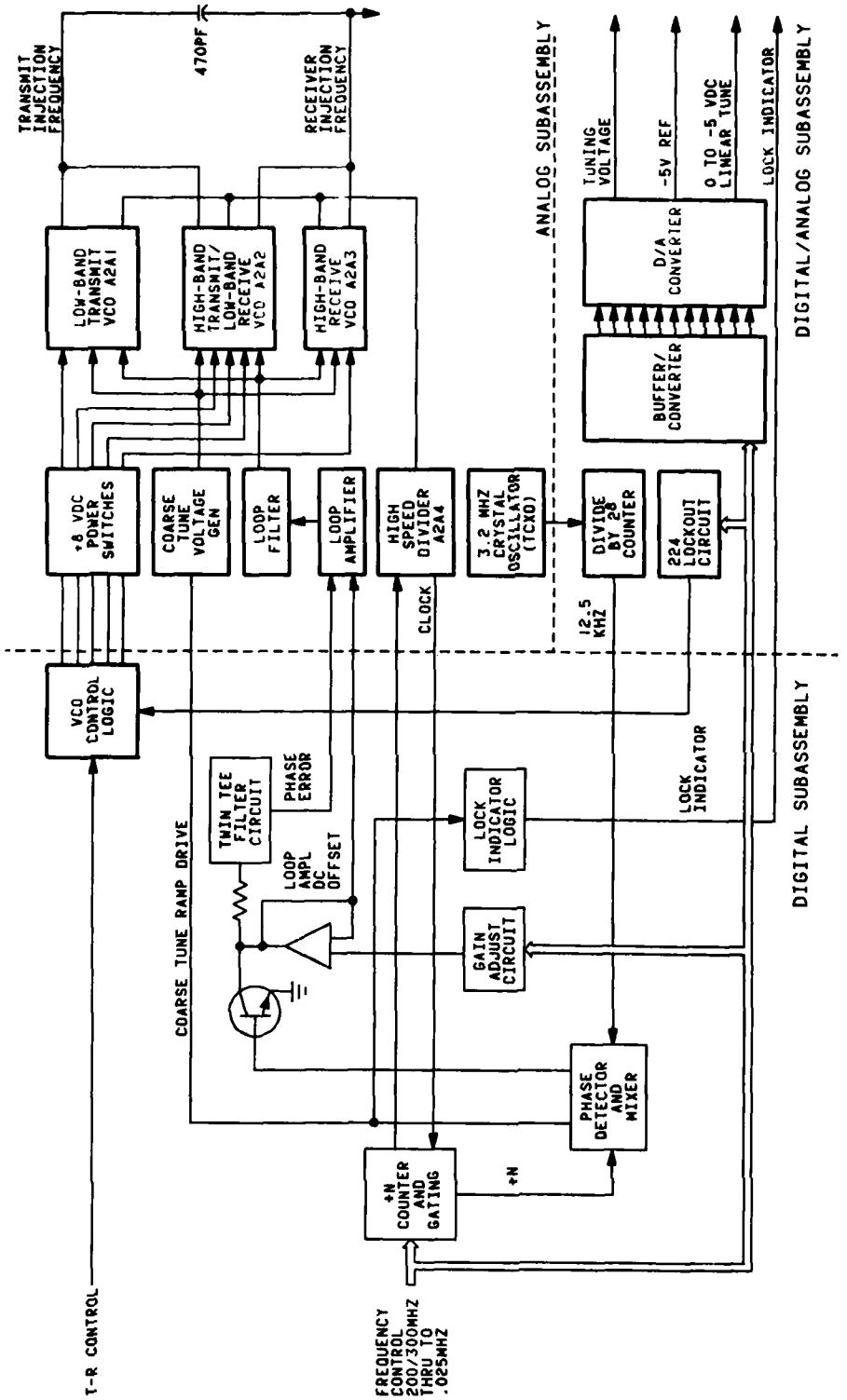


Figure 41. Synthesizer assembly block diagram

to achieving the interferring signal requirements of the receiver. In the study phase of the contract, considerable effort was directed towards the development of a VCO that would meet the needs of this system.

A five-band voltage controlled oscillator is used in the assembly. This approach limits the tune range of the oscillator such that varactors with a small tuning ratio but correspondingly higher Q's can be used. Achieving a high Q is the most critical factor in the design of the oscillator. The varactors are operated at higher bias levels where Q is maximized. The varactors are stacked to further increase the control voltage and thus the Q. Individual varactor groups are used for tuning each of the five bands. This is to avoid additional losses in the PIN switching network which is used to switch band elements. To achieve a high Q for the inductive tuning elements, shorted coaxial transmission lines are used. A schematic diagram of the VCO is shown in Figure 42.

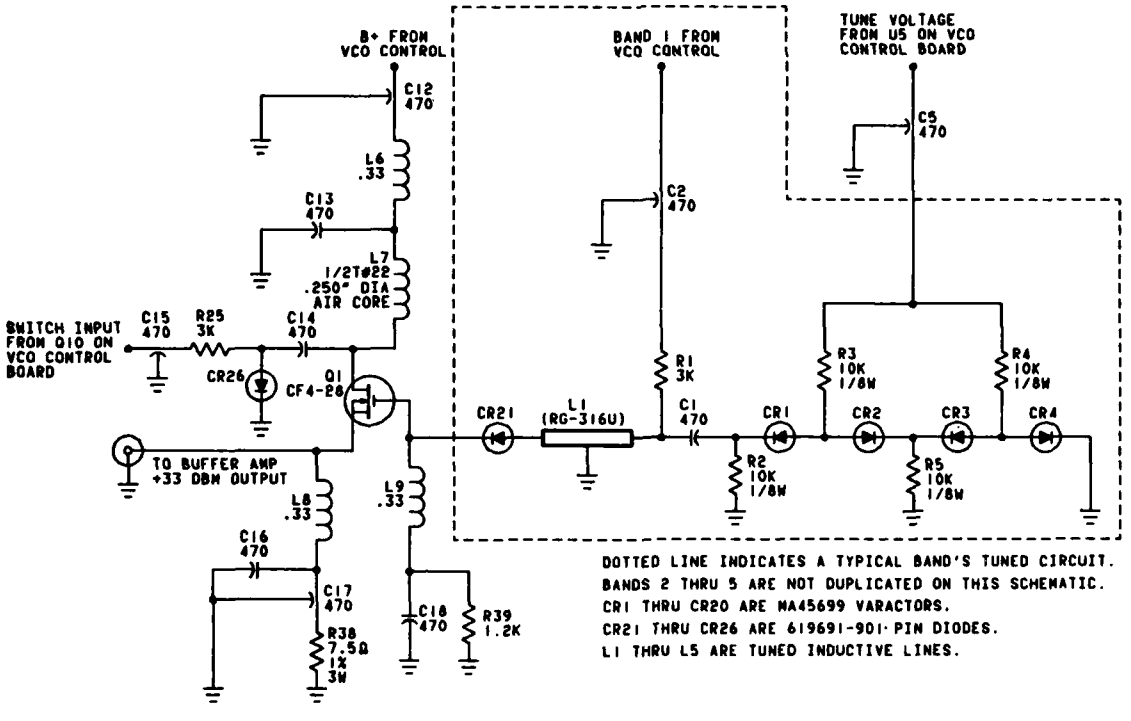


Figure 42. VCO schematic diagram

The VCO operates at a power level of 2 watts which is resistively padded to drive a low noise, low Q, FET buffer amplifier (Figure 43). The output of the amplifier is then further divided to supply injection to the receiver at a level of +27 dBm and to the transmitter at a nominal level of +2 dBm. A sample of the VCO output is buffered, divided down, and phase compared to the reference frequency input from the synthesizer module.

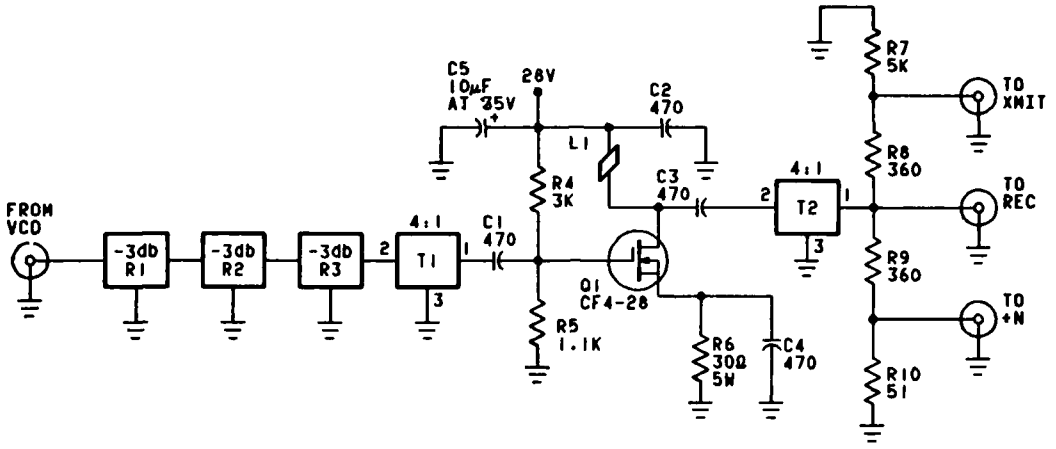


Figure 43. VCO buffer amplifier schematic diagram

Noise level measurements of the +27 dBm output of the VCO/Buffer Assembly are shown in Table 14.

The buffer amplifier contributes a small amount of noise to the injection signal and was not originally planned in the experimental transceiver design. It was discovered in early system tests of the transceiver that strong (+20 dBm) interferring signals injected at the receiver antenna modulated the VCO and caused IFM which decreased the receiver off-channel rejection. The interferring signal reached the receiver double balanced mixer and varied the LO port impedance at the modulation rate, thus causing IFM to appear on the LO signal. To correct this an isolator was tried with very good results, however, an isolator covering the entire frequency range and of a useable physical size was not available. The alternative was to add considerable isolation between the VCO and receiver mixer and the buffer amplifier was developed. This arrangement was not as effective as using the isolator, however, it was found the receiver requirements could be met with this approach.

Table 14. VCO/BUFFER OUTPUT NOISE MEASUREMENTS

Channel frequency (MHz)	Test frequency (MHz)	Noise level (dBm/Hz)
VCO BAND 1		
225 XMT	220.5	-151
	229.5	-146
	250	-154
	300	-152
	350	-154
	400	-155
237 XMT	225	-155
	232.75	-150
	241.75	-146
	250	-154
	300	-153
	400	-153
248 XMT	225	-155
	243.04	-154
	252.96	-152
	300	-154
	400	-156
225 RCV	225	-155
	250	-155
	290.5	-142
	299.5	-142
	400	-155
VCO BAND 2		
249 XMT	225	-153
	244.02	-152
	253.98	-152
	300	-153
	400	-154
258 XMT	225	-153
	252.84	-153
	263.16	-152
	300	-153
	400	-154
273 XMT	225	-153
	250	-153
	267.54	-154
	278.46	-153
	300	-152
	400	-154
260 RCV	225	-153
	250	-154
	324.8	-150
	335.2	-150
	400	-155

Table 14. VCO/BUFFER OUTPUT NOISE MEASUREMENTS (CONT)

Channel frequency (MHz)	Test frequency (MHz)	Noise level (dBm/Hz)
VCO BAND 3		
274 XMT	225	-152
	250	-153
	268.52	-152
	279.48	-151
	300	-153
	400	-154
289 XMT	225	-155
	250	-154
	283.22	-145
	294.78	-145
	300	-154
	400	-155
313 XMT	225	-153
	250	-154
	300	-154
	306.74	-146
	319.26	-145
	400	-155
300 RCV	225	-153
	250	-154
	300	-154
	364	-149
	376	-149
	400	-154
VCO BAND 4		
314 XMT	225	-153
	250	-154
	300	-155
	307.72	-152
	320.28	-153
	400	-155
350 XMT	225	-154
	250	-155
	300	-155
	343	-152
	357	-153
	400	-156
360 RCV	225	-153
	250	-153
	300	-154
	400	-155

Table 14. VCO/BUFFER OUTPUT NOISE MEASUREMENTS (CONT)

Channel frequency (MHz)	Test frequency (MHz)	Noise level (dBm/Hz)
VCO BAND 5		
389 XMT	225	-153
	250	-154
	380	-154
	381.22	-150
	396.78	-150
	400	-150
399.975 RCV	225	-153
	250	-154
	300	-154
	400	-155

SECTION IV
EXPERIMENTAL MODEL TEST DATA

The following test data was derived from the experimental model radio with a nominal input voltage of 27.5 volts. Primary input current at this voltage is 2.25 amps in receive and 4.2 amps in transmit.

Table 13 lists the electrical performance characteristics specified in the Statement of Work. All tests were performed per the Equipment Test Plan dated 13 January, 1982.

Results of the Transmitter Spurious Output are shown in Figure 44. The following list indicates other tests performed and results of each of these tests may be found in the associated table.

Table no.	Title
15	Transmitter and receiver basic performance
16	Transmitter modulator capability
17	Tuning time
18	Transmitter broadband noise
19	Receiver degradation performance
20	Receiver spurious responses
21	LO reradiated levels
22	Receiver image and IF rejection
23	Tuning interval tests

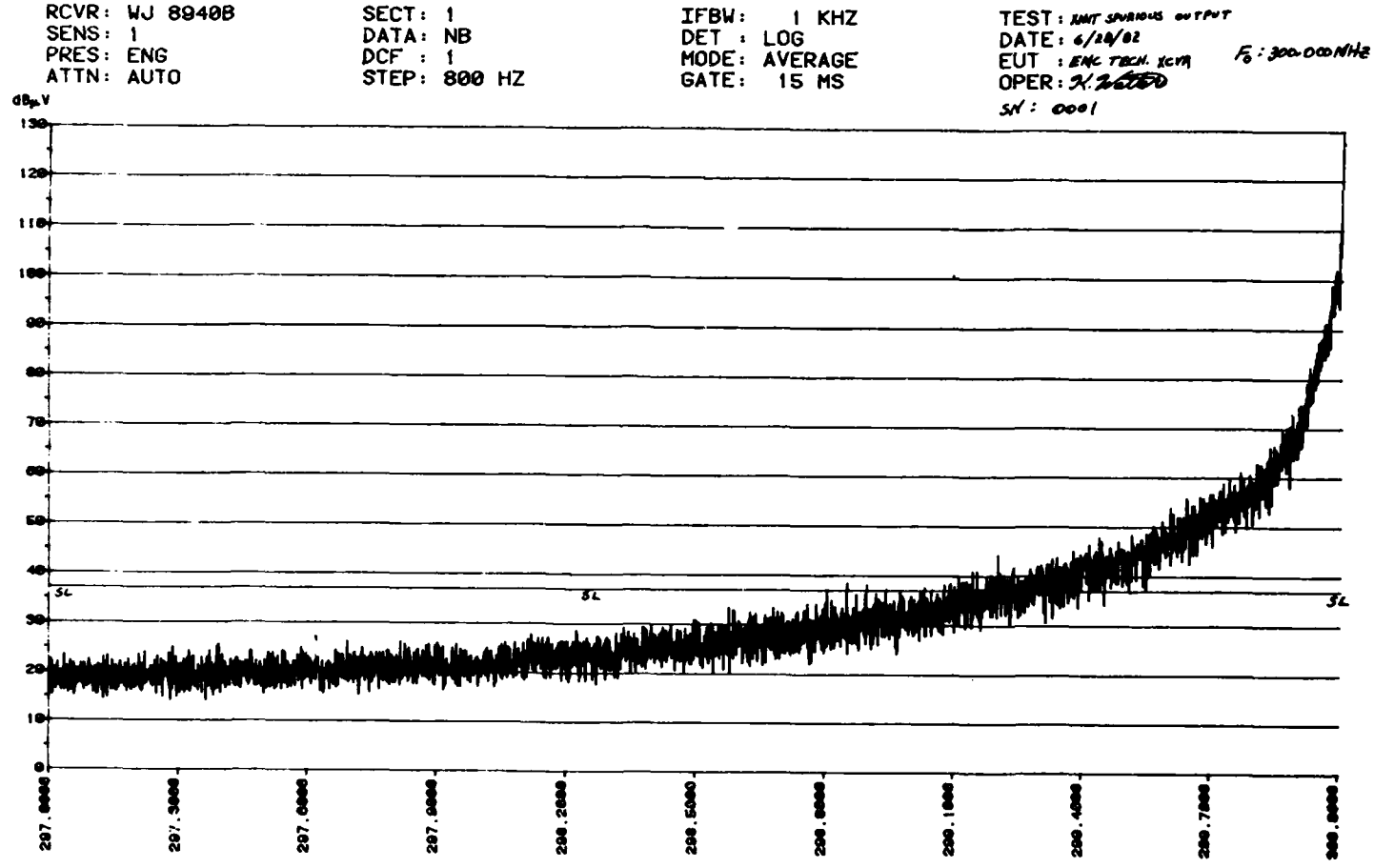
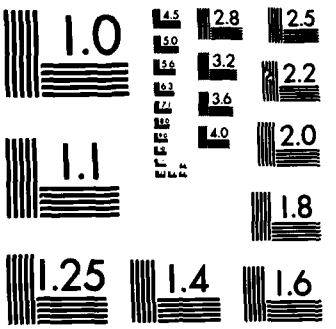


Figure 44. Transmitter spurious output, 300 MHz (1 of 14)

AD-A123 705 SOLID STATE EMC TECHNOLOGY DEVELOPMENT(U) MAGNAVOX CO 2/2
FORT WAYNE IND J G MOHR ET AL. NOV 82 FWD82-4284A
RADC-TR-82-280 F30602-80-C-0136

UNCLASSIFIED F/G 17/2.1 NL



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

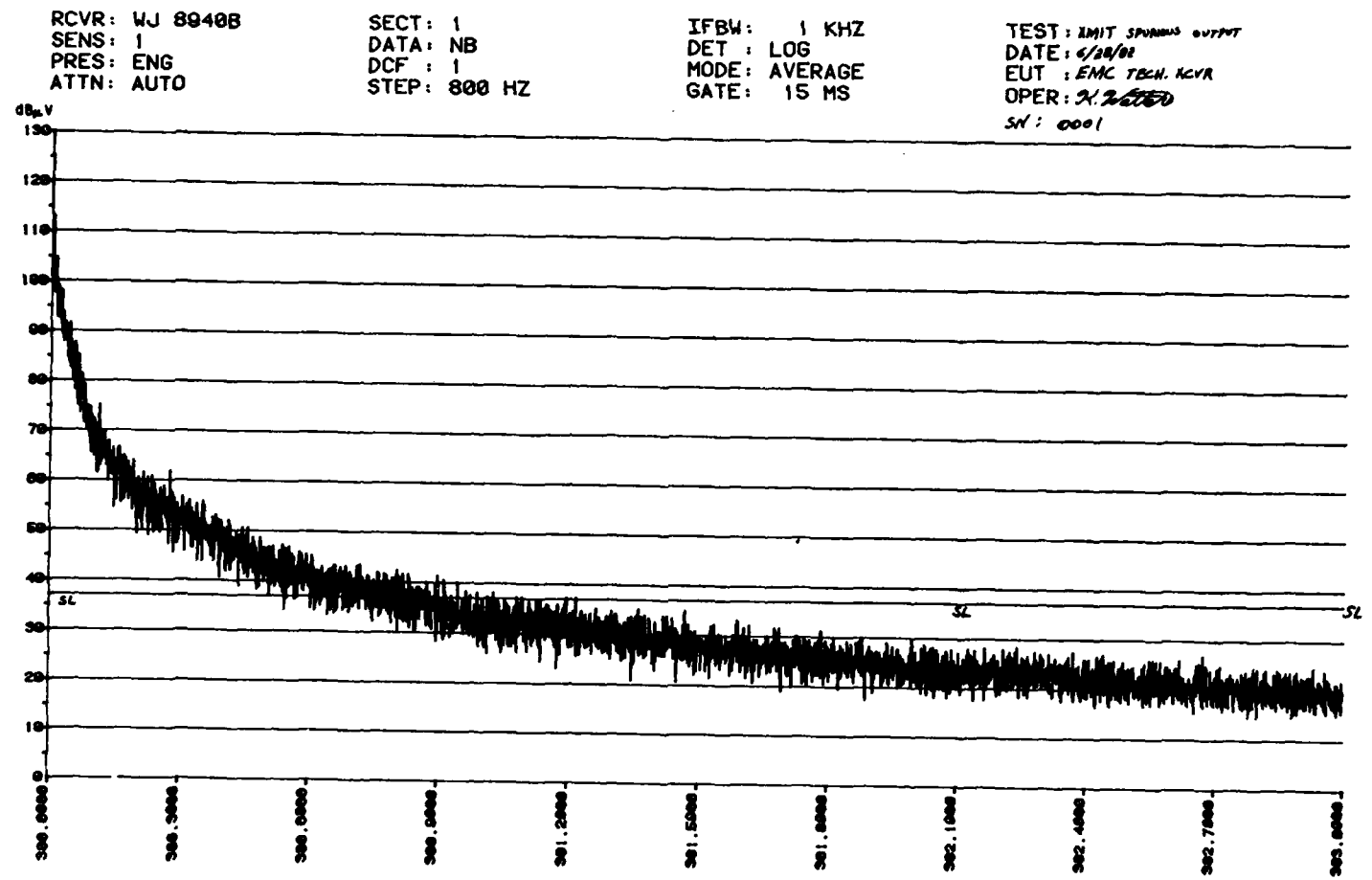


Figure 44. Transmitter spurious output, 300 MHz (2 of 14)

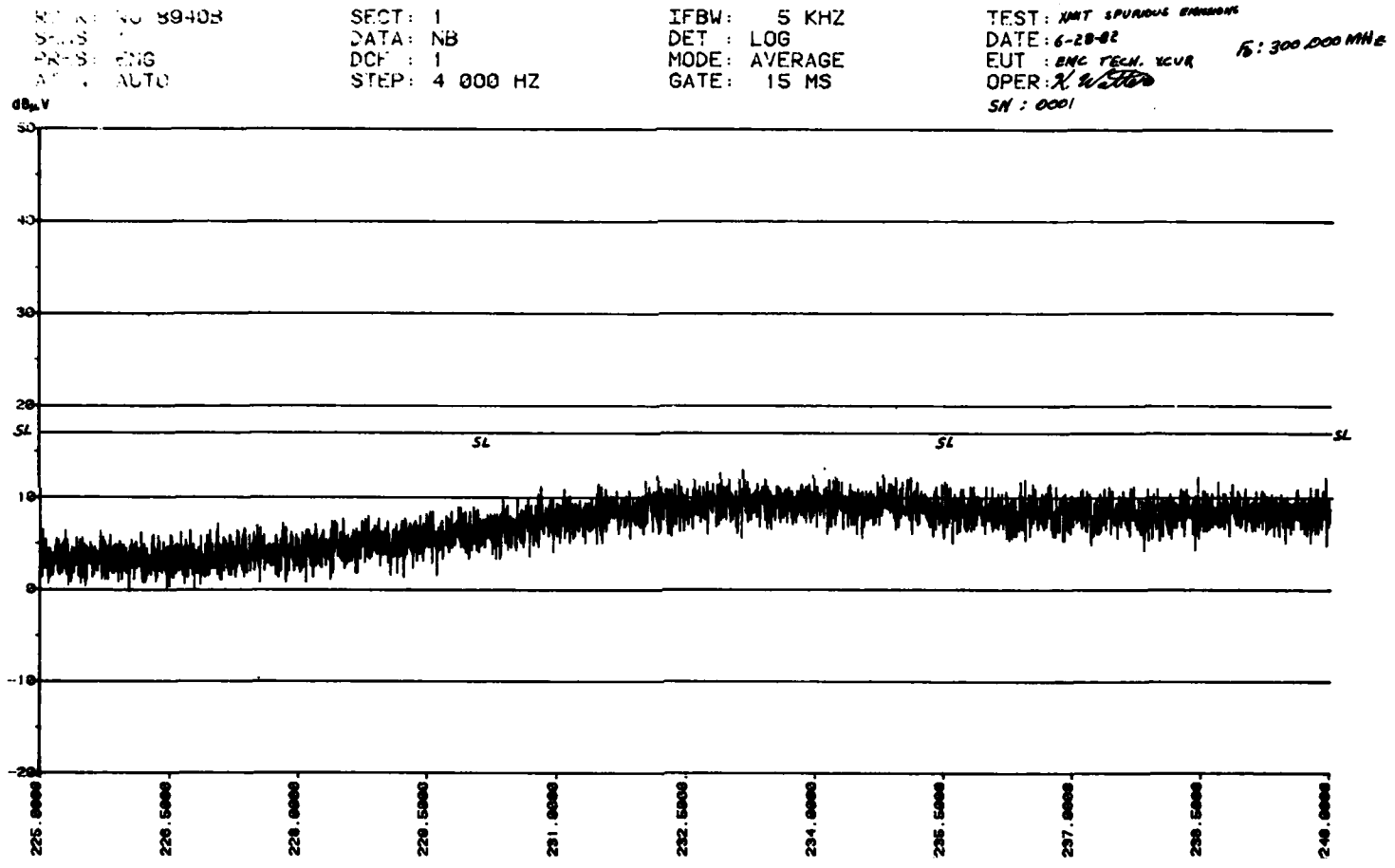


Figure 44. Transmitter spurious output, 300 MHz (3 of 14)

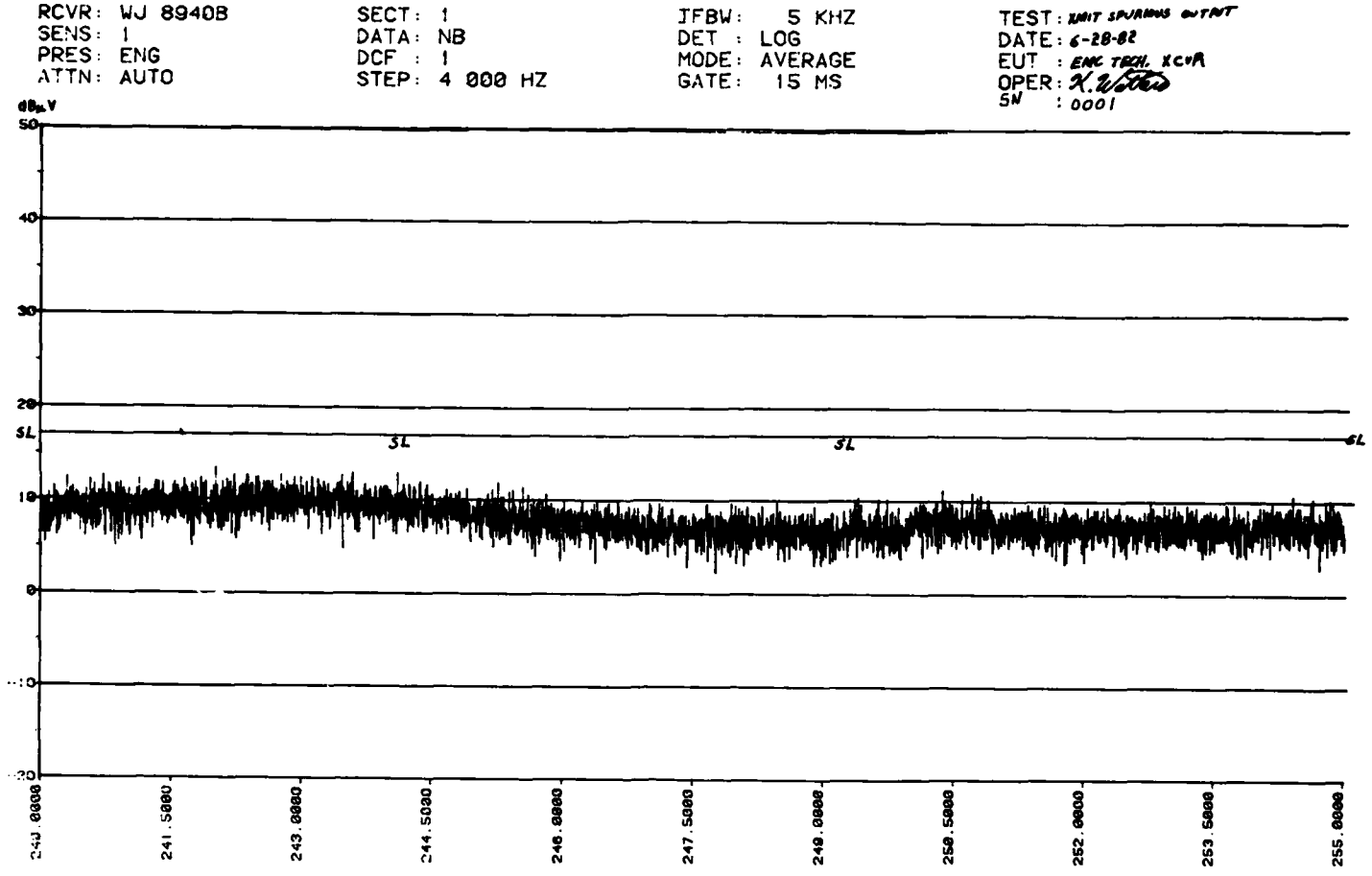


Figure 44. Transmitter spurious output, 300 MHz (4 of 14)

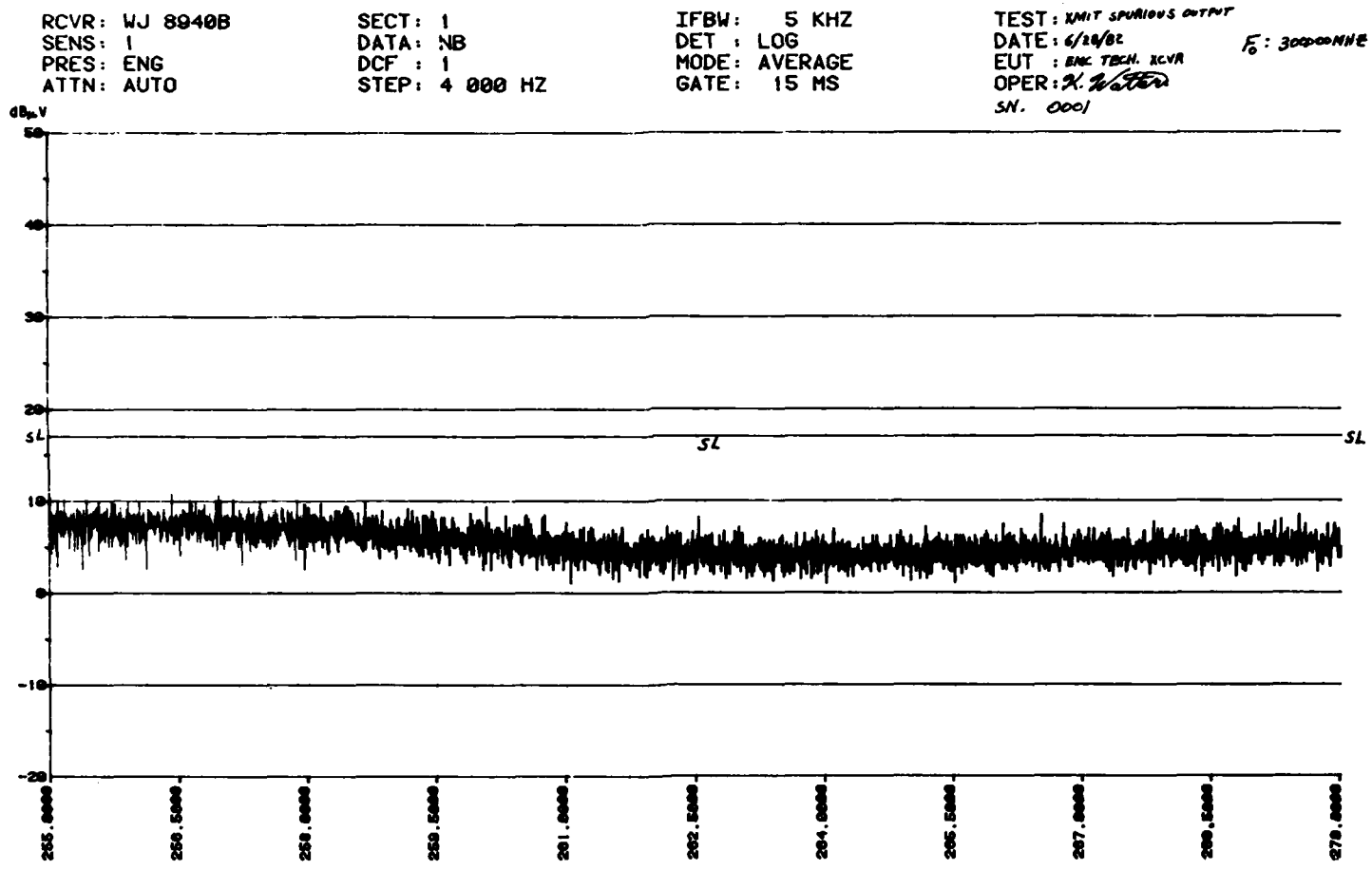


Figure 44. Transmitter spurious output, 300 MHz (5 of 14)

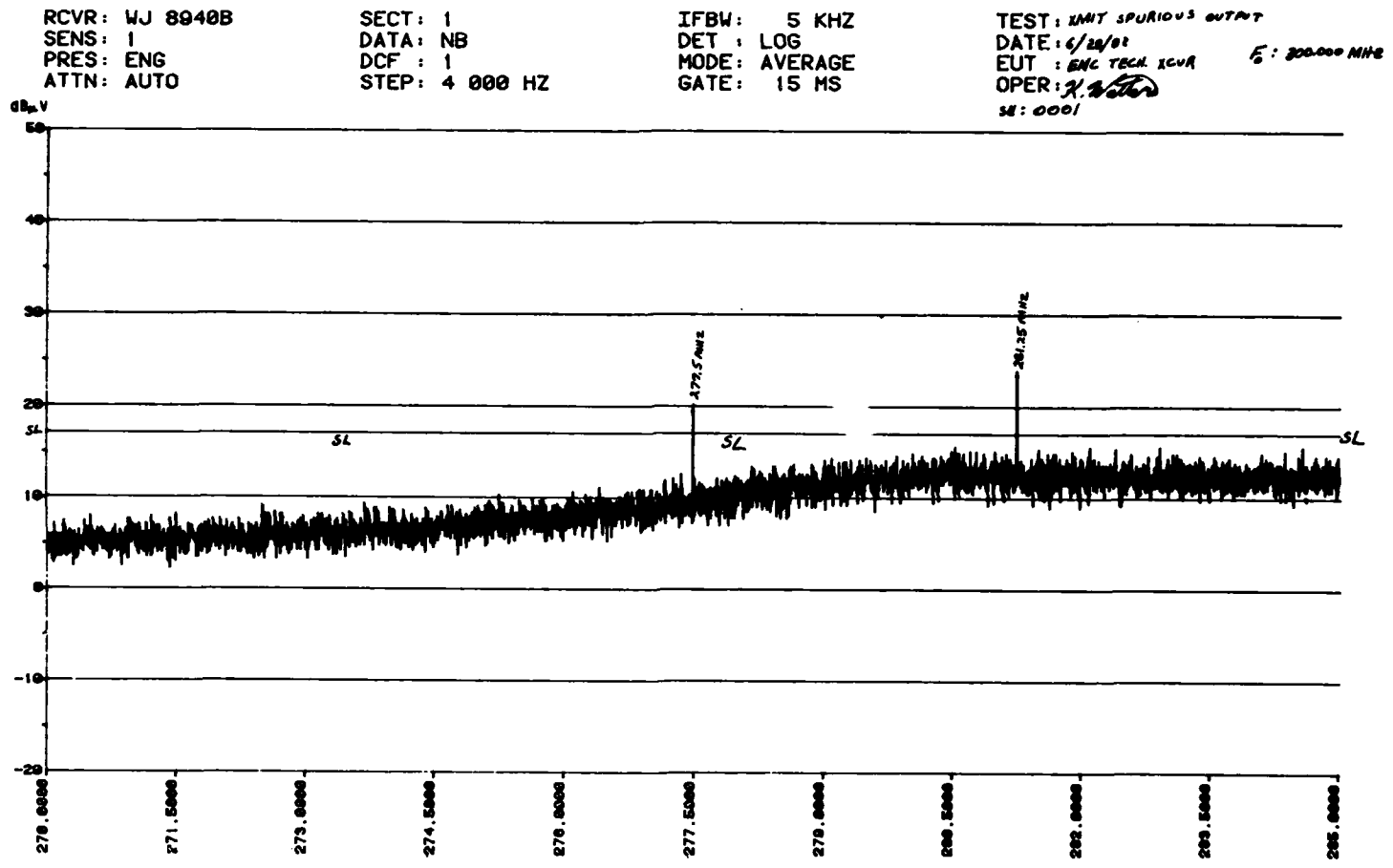


Figure 44. Transmitter spurious output, 300 MHz (6 of 14)

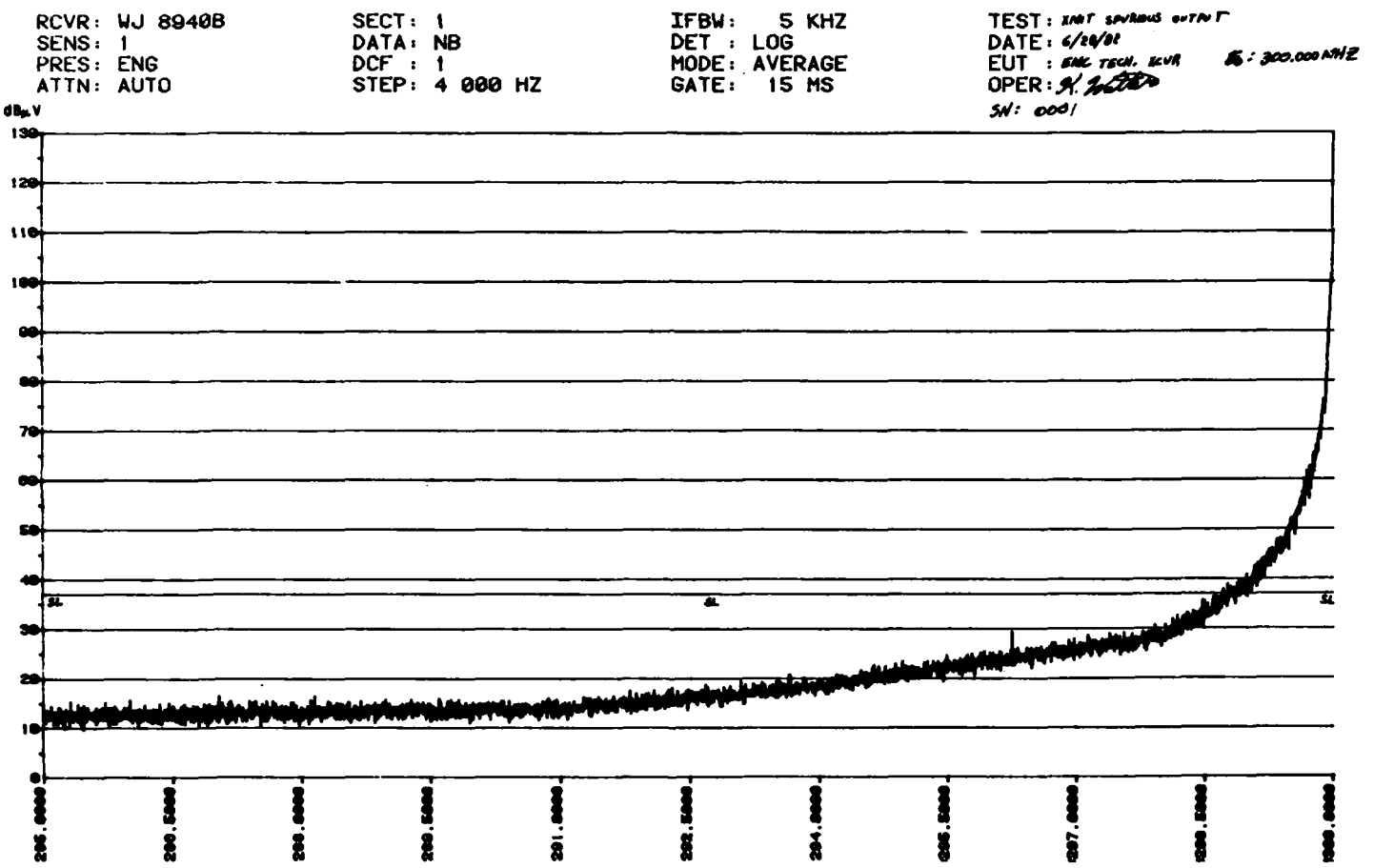


Figure 44. Transmitter spurious output, 300 MHz (7 of 14)

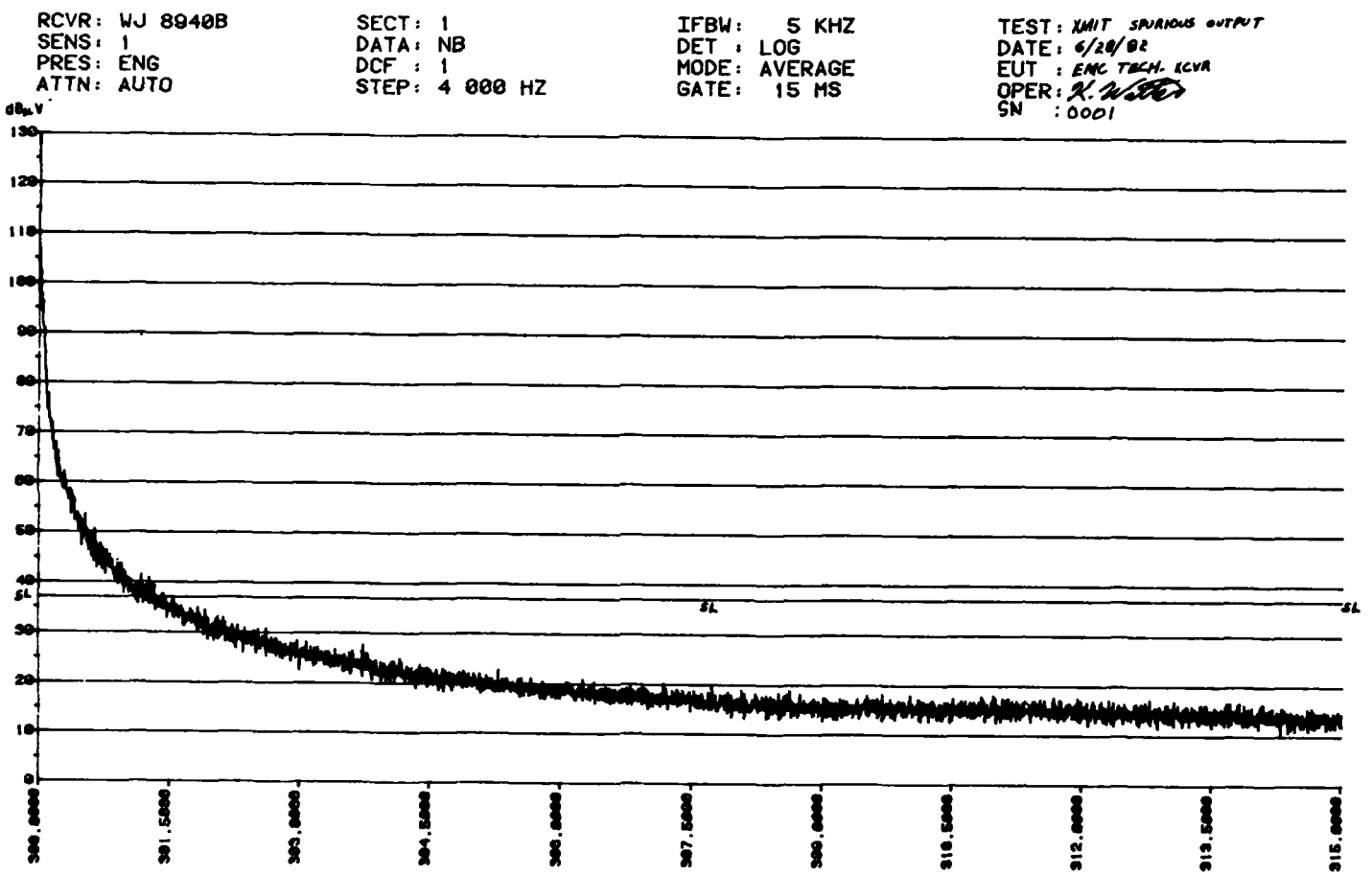


Figure 44. Transmitter spurious output, 300 MHz (8 of 14)

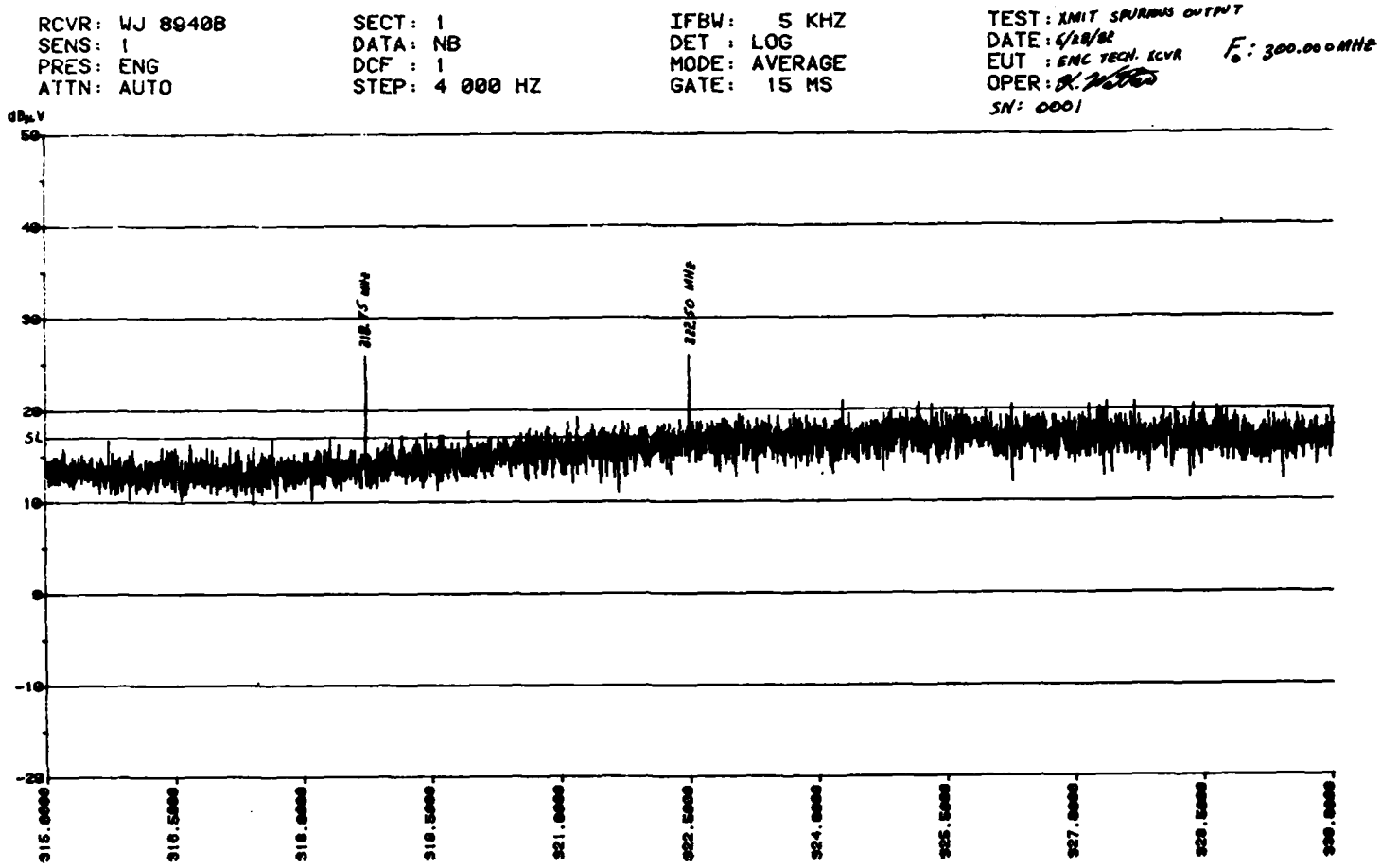


Figure 44. Transmitter spurious output, 300 MHz (9 of 14)

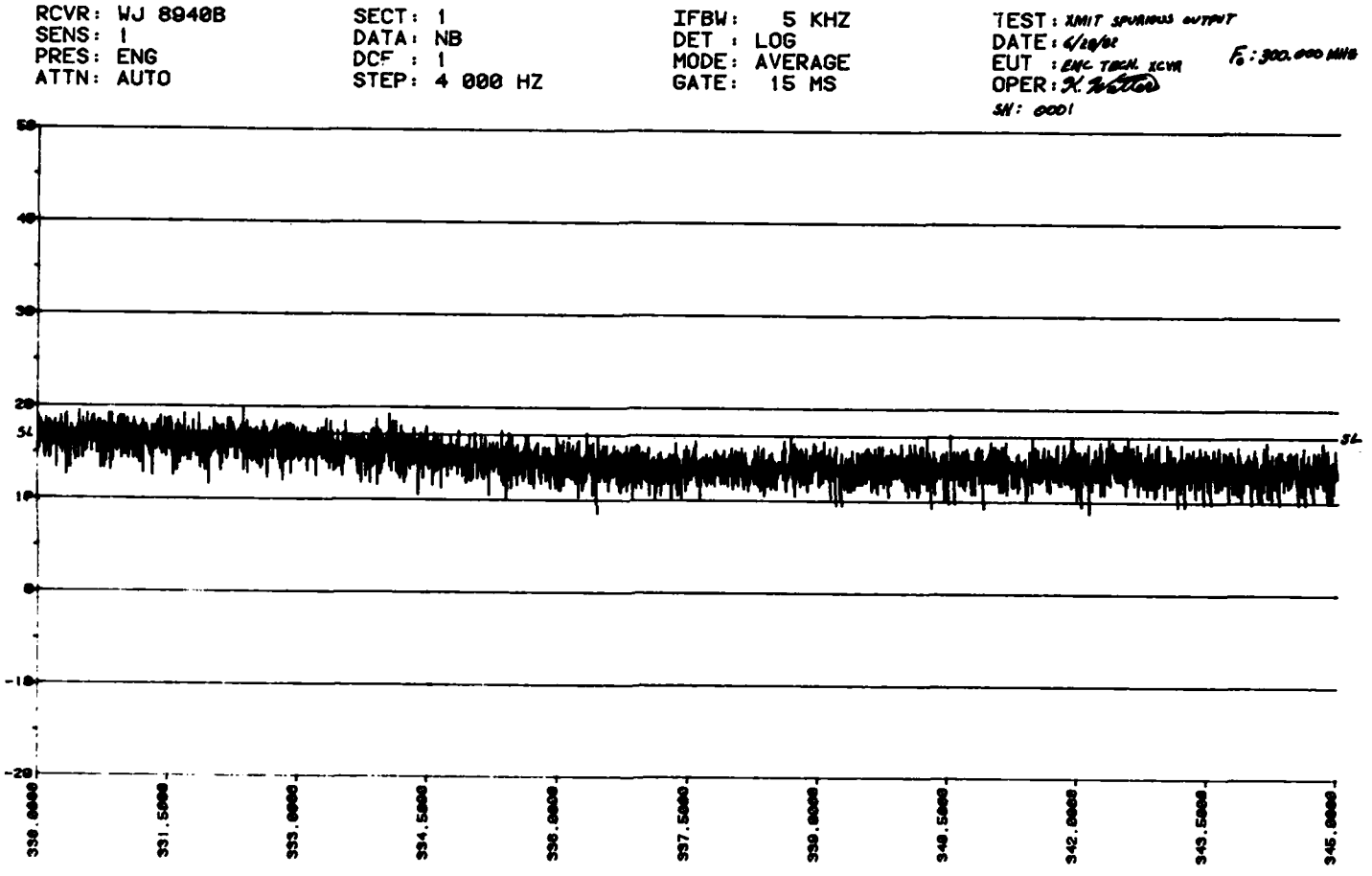


Figure 44. Transmitter spurious output, 300 MHz (10 of 14)

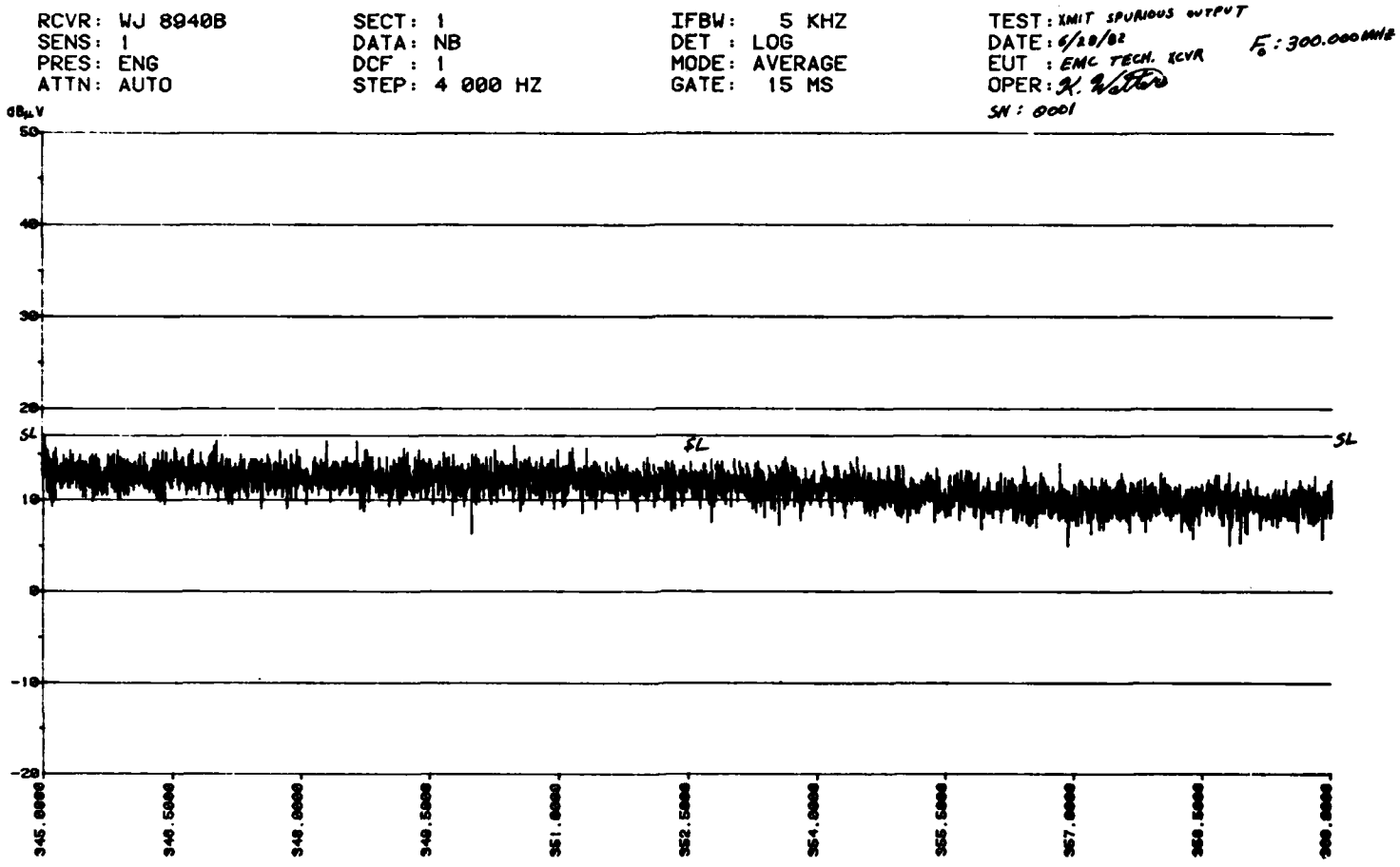


Figure 44. Transmitter spurious output, 300 MHz (11 of 14)

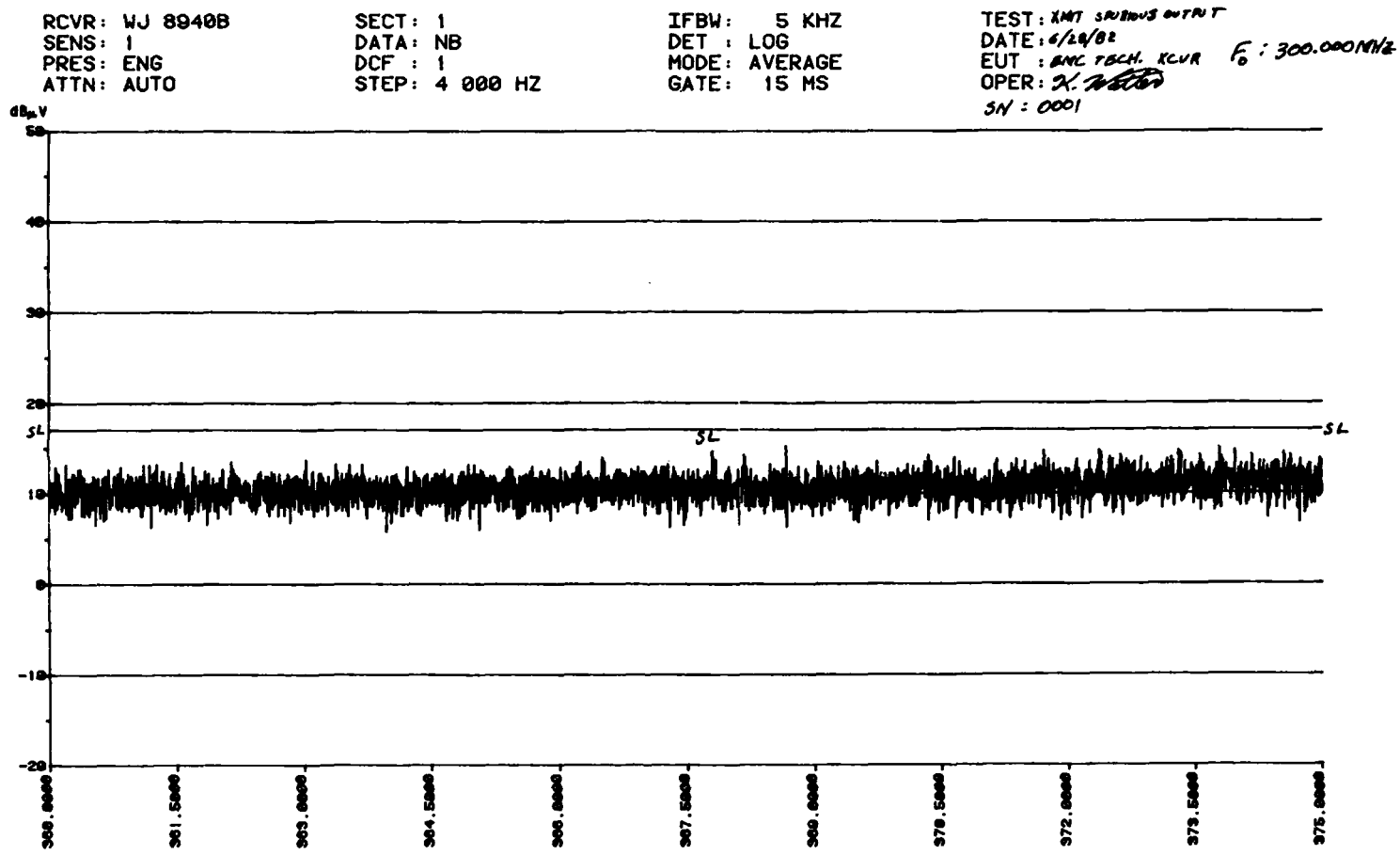


Figure 44. Transmitter spurious outp[illegible] [illegible]12 of 14)

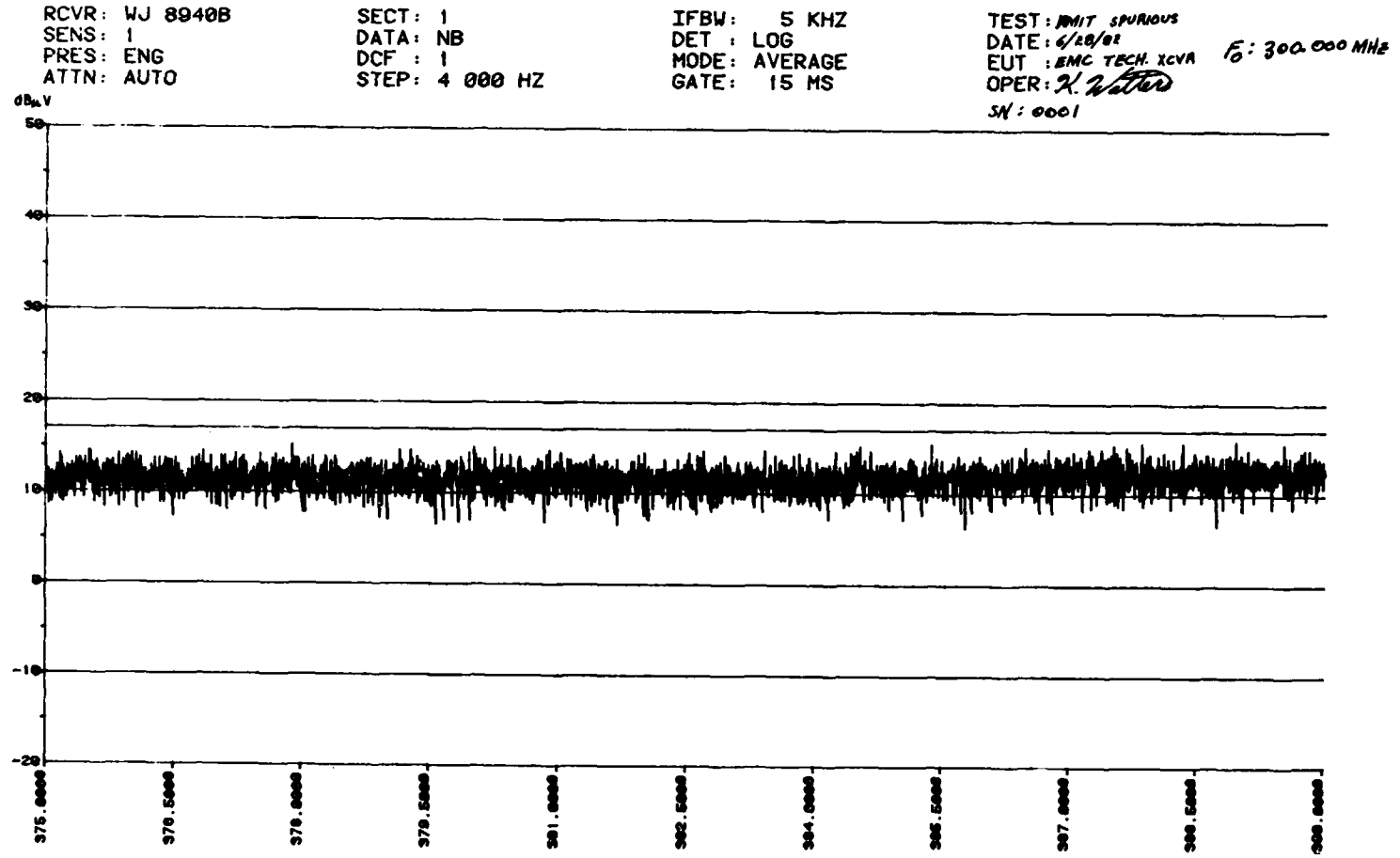


Figure 44. Transmitter spurious output, 300 MHz (13 of 14)

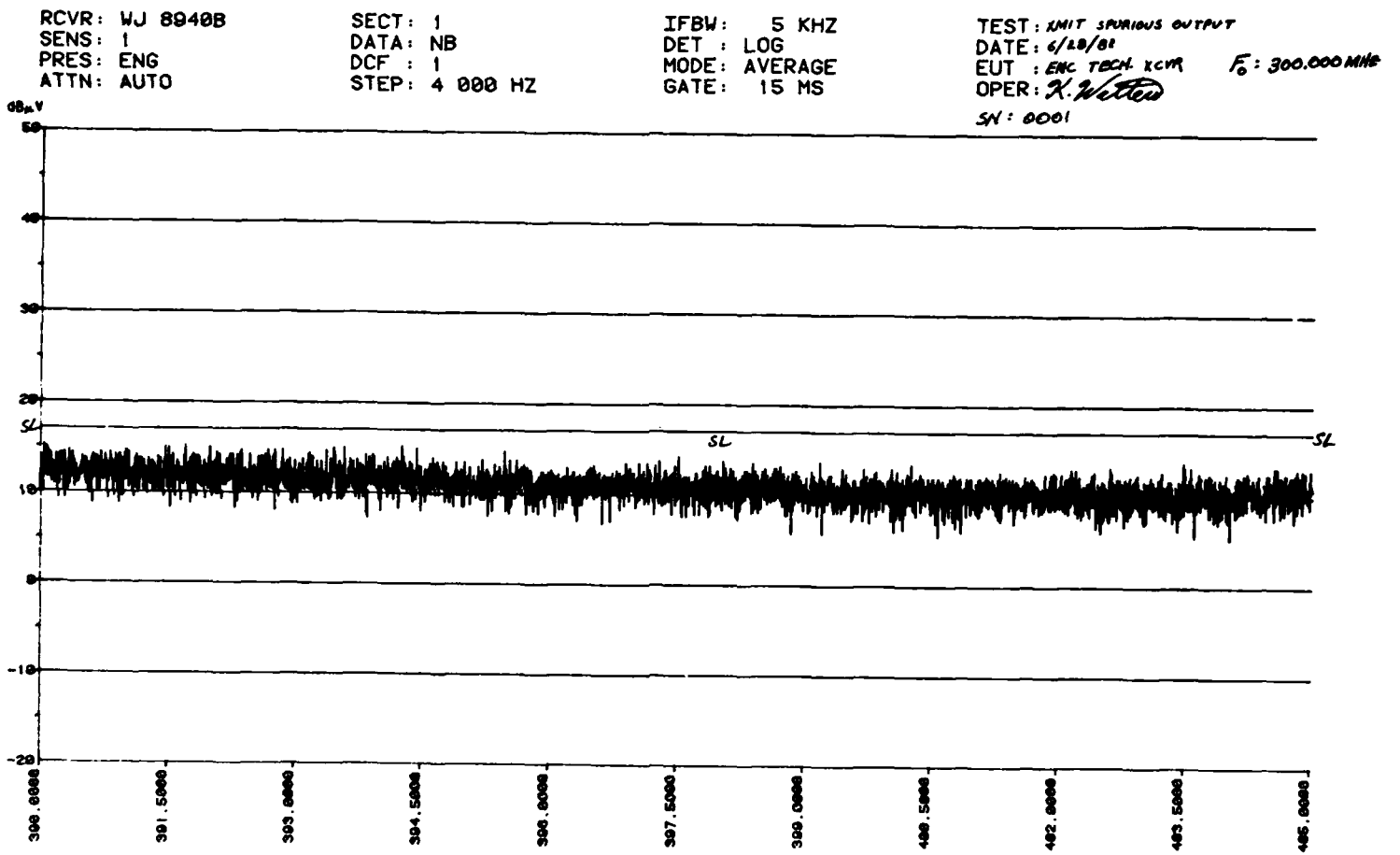


Figure 44. Transmitter spurious output, 300 MHz (14 of 14)

TABLE 15. TRANSMITTER AND RECEIVER BASIC PERFORMANCE

Nominal channel frequency (MHz)	Transmitter power output (watts)	Frequency accuracy (MHz)	Receive sensitivity (dB)	Input impedance
225	12	224.9997	15	<2.0:1
230	12	229.9997	15.5	<1.5:1
240	12	239.9997	15.2	<1.5:1
250	11.75	249.9997	13.5	<1.5:1
260	11.75	259.9997	14.0	<1.5:1
270	11.5	269.9997	13.0	<2.0:1
280	11.5	279.9996	12.5	<1.5:1
290	11.5	289.9996	14.0	<2.0:1
300	11.25	299.9996	13.5	<2.0:1
310	11.25	309.9996	14.0	<1.5:1
320	11.5	319.9996	13.0	<1.5:1
330	11.5	329.9996	13.0	<1.5:1
340	11.5	339.9996	14.0	<2:1
350	11.25	349.9995	14.5	<2:1
360	11.25	359.9995	14.5	<1.5:1
370	11.0	369.9995	14.0	<1.5:1
380	10.6	379.9995	13.5	<1.5:1
390	10.5	389.9995	13.2	<1.5:1
399.975	10.5	399.9745	12.5	<1.5:1

TABLE 16. TRANSMITTER MODULATION CAPABILITY

Frequency (MHz)	Positive modulation (%)	Negative modulation (%)
225	86	89
260	84	88
300	86	89
360	85	88
399.975	88	89

TABLE 17. TUNING TIME

Frequency (MHz)	Transmit to receive (ms)	Receive to transmit (ms)
225	15	32
260	17	20
300	20	20
360	25	22
399.975	25	10

TABLE 18. TRANSMITTER BROADBAND NOISE AT VARIOUS FREQUENCIES

CHANNEL FREQUENCY AT 225 MHz

Test frequency (MHz)	True power (dBm/Hz)	Spec limit (dBm/Hz)
210.0	-129	-125
211.0	-128	-124
212.0	-127	-123
213.0	-126	-122
214.0	-121	-121
215.0	-124	-119
216.0	-123	-118
217.0	-122	-116
218.0	-121	-114
219.0	-120	-112
220.0	-119	-110
221.0	-118	-107
222.0	-117	-104
223.0	-115	-99
223.5	-113	-96
224.0	-111	-91
224.5	-104	-84
224.8	-89	-76
225.2	-91	-76
225.5	-103	-84
226.0	-112	-91
226.5	-114	-96
227.0	-117	-99
228.0	-119	-104
229.0	-121	-107
230.0	-123	-110
231.0	-123	-112
232.0	-123	-114
233.0	-123	-116
234.0	-123	-118

TABLE 18. TRANSMITTER BROADBAND NOISE AT VARIOUS FREQUENCIES (CONT)

Test frequency (MHz)	True power (dBm/Hz)	Spec limit (dBm/Hz)
235.0	-124	-119
236.0	-124	-121
237.0	-124	-122
238.0	-124	-123
239.0	-124	-124
240.0	-125	-125
Fo	---	---
245	-127	-125
255	-129	-125
265	-129	-133
275	-130	-133
285	-133	-133
295	-134	-133
305	-124	-133
315	-131	-133
325	-130	-133
335	-130	-133
345	-133	-133
355	-131	-133
365	-129	-133
375	-129	-133
385	-129	-133
395	-130	-133
CHANNEL FREQUENCY AT 260 MHz		
245.0	-128	-125
246.0	-128	-124
247.0	-128	-123
248.0	-128	-122
249.0	-128	-121
250.0	-128	-119
251.0	-128	-118
252.0	-128	-116
253.0	-128	-114
254.0	-126	-112
255.0	-123	-110
256.0	-121	-107
257.0	-119	-104
258.0	-117	-99
258.5	-114	-96
259.0	-111	-91
259.5	-106	-84
259.8	-91	-76
260.2	-94	-76
260.5	-106	-84
261.0	-112	-91

TABLE 18. TRANSMITTER BROADBAND NOISE AT VARIOUS FREQUENCIES (CONT)

Test frequency (MHz)	True power (dBm/Hz)	Spec limit (dBm/Hz)
261.5	-115	-96
262.0	-118	-99
263.0	-120	-104
264.0	-122	-107
265.0	-126	-110
266.0	-129	-112
267.0	-130	-114
268.0	-131	-116
269.0	-132	-118
270.0	-132	-119
271.0	-133	-121
272.0	-133	-122
273.0	-133	-123
274.0	-133	-124
275.0	-133	-125
225	-133	-133
230	-130	-125
240	-128	-125
Fo	---	---
280	-133	-125
290	-136	-125
300	-140	-133
310	-138	-133
320	-132	-133
330	-127	-133
340	-128	-133
350	-130	-133
360	-130	-133
370	-130	-133
380	-131	-133
390	-132	-133
400	-133	-133
CHANNEL FREQUENCY AT 300 MHz		
285.0	-131	-125
286.0	-131	-124
287.0	-132	-123
288.0	-132	-122
289.0	-132	-121
290.0	-132	-119
291.0	-131	-118
292.0	-131	-116
293.0	-130	-114
294.0	-128	-112
295.0	-125	-110
296.0	-121	-107

TABLE 18. TRANSMITTER BROADBAND NOISE AT VARIOUS FREQUENCIES (CONT)

Test frequency (MHz)	True power (dBm/Hz)	Spec limit (dBm/Hz)
297.0	-118	-104
298.0	-113	-99
298.5	-109	-96
299.0	-102	-91
299.5	-91	-84
299.8	-77	-76
300.5	-90	-84
301.0	-101	-91
301.5	-107	-96
302.0	-112	-99
303.0	-117	-104
304.0	-120	-107
305.0	-123	-110
306.0	-126	-112
307.0	-127	-114
308.0	-127	-116
309.0	-128	-118
310.0	-129	-119
311.0	-129	-121
312.0	-129	-122
313.0	-129	-123
314.0	-129	-124
315.0	-129	-125
225	-139	-133
230	-138	-133
240	-135	-133
250	-135	-133
260	-137	-133
270	-137	-125
280	-133	-125
Fo	---	---
320	-129	-125
330	-128	-125
340	-129	-133
350	-131	-133
360	-132	-133
370	-131	-133
380	-131	-133
390	-132	-133
400	-132	-133

TABLE 18. TRANSMITTER BROADBAND NOISE AT VARIOUS FREQUENCIES (CONT)

Test frequency (MHz)	True power (dBm/Hz)	Spec limit (dBm/Hz)
CHANNEL FREQUENCY AT 360 MHz		
345.0	-128	-125
346.0	-128	-124
347.0	-128	-123
348.0	-128	-122
349.0	-128	-121
350.0	-128	-119
351.0	-128	-118
352.0	-127	-116
353.0	-125	-114
354.0	-123	-112
355.0	-120	-110
356.0	-117	-107
357.0	-116	-104
358.0	-112	-99
358.5	-110	-96
359.0	-108	-91
359.5	-102	-84
359.8	-92	-76
360.2	-91	-76
360.5	-100	-84
361.0	-109	-91
361.5	-112	-96
362.0	-115	-99
363.0	-118	-104
364.0	-119	-107
365.0	-122	-110
366.0	-125	-112
367.0	-127	-114
368.0	-127	-116
369.0	-128	-118
370.0	-128	-119
371.0	-128	-121
372.0	-128	-122
373.0	-128	-123
374.0	-128	-124
375.0	-128	-125
225	-140	-133
230	-139	-133
240	-137	-133
250	-135	-133
260	-137	-133
370	-138	-133
280	-139	-133
290	-138	-133
300	-137	-133

TABLE 18. TRANSMITTER BROADBAND NOISE AT VARIOUS FREQUENCIES (CONT)

Test frequency (MHz)	True power (dBm/Hz)	Spec limit (dBm/Hz)
310	-136	-133
320	-133	-133
330	-131	-125
340	-128	-125
Fo	---	---
380	-131	-125
390	-135	-125
400	-135	-133
CHANNEL FREQUENCY AT 399.975 MHz		
385.0	-126	-125
386.0	-126	-124
387.0	-126	-123
388.0	-126	-122
389.0	-126	-121
390.0	-126	-119
391.0	-126	-118
392.0	-126	-116
393.0	-125	-114
394.0	-123	-112
395.0	-121	-110
396.0	-118	-107
397.0	-116	-104
398.0	-113	-99
399.0	-100	-91
399.5	-99	-84
399.7	-89	-79
400.175	-88	-76
400.500	-100	-85
401.000	-108	-92
401.500	-111	-96
402.000	-113	-99
403.000	-116	-104
404.000	-118	-107
405.000	-121	-110
406.000	-123	-112
407.000	-124	-114
408.000	-124	-116
409.000	-125	-118
410.000	-125	-119
411.000	-125	-121
412.000	-126	-122
413.000	-127	-123
414.000	-128	-124
415.000	-129	-125
225	-136	-133

TABLE 18. TRANSMITTER BROADBAND NOISE AT VARIOUS FREQUENCIES (CONT)

Test frequency (MHz)	True power (dBm/Hz)	Spec limit (dBm/Hz)
230	-134	-133
240	-133	-133
250	-135	-133
260	-139	-133
270	-141	-133
280	-141	-133
290	-139	-133
300	-138	-133
310	-135	-133
320	-132	-133
330	-132	-133
340	-133	-133
350	-132	-133
360	-127	-133
370	-121	-125
380	-122	-125

TABLE 19. RECEIVER DEGRADATION PERFORMANCE

(-95 dBm input)	Jamming level required at f_o -2%		Jamming level required at f_o +2%	
Channel frequency (fo) (MHz)	for 8 dB S/N (dBm)	for 10 dB S/N (dBm)	for 8 dB S/N (dBm)	for 10 dB S/N (dBm)
225	21.6	19.5	18.0	16.5
260	21.2	20.6	21.0	20.7
300	22.0	21.6	22.1	21.8
360	22.3	20.9	24.1	23.1
399.975	21.4	20.5	25.8	24.9

TABLE 20. RECEIVER SPURIOUS RESPONSE

Channel frequency (MHz)	Interference frequency (MHz)	Rejection (4) (dB)
225	260 (1)	73
260	None	
300	335 (2)	76
360	None	
399.975	289.984(3)	85

(1) 2 x LO - 2 x Input = IF
(2) 2 x LO - 2 x Input = IF
(3) 2 x LO - 3 x Input = IF
(4) Rejection requirement 70 dB minimum

TABLE 21. LOCAL OSCILLATOR RERADIATED LEVELS

Channel frequency (MHz)	LO frequency (MHz)	LO radiated level
225	295	1 mV
250	320	250 μV
275	345	30 μV
300	370	105 μV
325	395	250 μV
350	420	240 μV
400	470	1 mV

TABLE 22. RECEIVER IMAGE AND IF REJECTION

Operating frequency (MHz)	Image rejection (dB)
225	>110
250	>110
300	77
350	>110
390	>110

Note:

(1) 70 MHz IF rejection = 107 dB (worse case, 300 MHz)

(2) 30.112 MHz IF rejection >110 dB

TABLE 23. TUNING INTERVAL TESTS

TRANSMIT

Nominal frequency (MHz)	Measured frequency (MHz)	Power output (watts)
225.000	224.99969	12
225.025	225.02469	12
225.050	225.04969	12
248.975	248.97467	12
249.000	248.99966	11.75
249.025	249.02466	11.75
249.050	249.04966	11.75
249.075	249.07466	11.75
273.975	273.97465	11.75
274.000	273.99962	11.50
274.025	274.02462	11.50
274.050	274.04962	11.50
313.975	313.97456	11.50
314.000	313.99954	11.50
314.025	314.02455	11.50
389.975	389.97445	10.50

RECEIVE

Channel frequency (MHz)	Receiver sensitivity (dB)
320.000	13.5
320.025	13.5
320.050	13.5
399.975	13.0

SECTION V

CONCLUSIONS

It was found during this program that considerable improvement can be made in the design of solid state receivers and transmitters to improve their operation in a crowded RF environment such as is encountered aboard C^3 aircraft. These aircraft systems typica'ly employ several UHF high-power transmitters and very sensitive receivers. Because of the close proximity and resultant coupling between antennas, RF interference is a major problem which degrades overall operation of the system.

Major improvement can be made in the dynamic range of modern receivers by the use of high-level mixers, low-noise, high-intercept amplifier stages, low-loss bandpass RF filtering techniques, and low-noise, high-power local oscillators.

It was discovered that double-balanced ring mixers used for the first conversion function should be rated much higher in frequency than the LO injection or RF input in order to reduce harmonic levels which are generated by LO multiplication by the diodes. The circuitry is normally balanced by the manufacturer to reduce this effect over an advertised operating range. In any case, a low-pass filter should be included in the design to prevent LO harmonic signals from reaching the antenna and being radiated. Although these LO harmonics are out of the UHF communications band, interference could be caused to navigation equipment aboard the aircraft if the harmonic signals were permitted to radiate. A filter is also required to lower the local oscillator fundamental radiation. Routing of the antenna cable is critical within the radio as part of the high-level (+27 dBm) LO signal is coupled across the cables rather than through the normal path to the antenna.

AGC is not required ahead of the low-level IF amplifier stages providing the dynamic range of all devices prior to this, is sufficient to

handle the expected levels, and if the AGC range of the following IF system will control the large input variations.

In the experimental transceiver no AGC is applied prior to the IF/ Demodulator assembly with the dynamic range of the two active 70-MHz IF stages in the receiver front end accepting the large varations in input signal without serious distortion. Input limiting from an on-channel signal does not occur below about -5 dBm at the antenna.

Operation of the receiver in a high-level interference environment depends directly on the noise component of the injection system. The required noise level can be closely calculated. Special techniques are required to generate the low-noise injection signal. A VMOS FET voltage controlled oscillator appears to be the best approach at this time. To generate the LO signal for the full 225 to 400 MHz range several tuned elements are required which enables the tuning varactors to operate at the Q levels required for low-noise operation.

A low-nose injection is also required for driving the transmitter as any noise on the injection will be amplified by the gain of the transmitter amplifier stages. Tuning of the low-level stages by varactor tuned filters improves the noise content beyond a few megahertz of center frequency.

Also considerable filtering of the transmitter power supply is required to minimize modulation of the output signals by the power supply switching frequency and its harmonics.

All of these technologies were built into the experimental EMC transceiver developed on this contract. The resulting transceiver meets or exceeds nearly all of the specification requirements and in general shows substantial improvement over existing solid state radios in such important areas as receiver dynamic range and transmitter noise and spurious output.

SECTION VI

RECOMMENDATIONS

To improve the design of the EMC Technology Transceiver or a similar EMC oriented radio, the following items should be examined and possibly applied. These are problems or ideas that surfaced late in the program and could not be incorporated, or are dependent on state-of-the-art component improvements which, if used, would improve performance of the radio.

Several spurious signals appear within a few hundred hertz of the carrier at all operating frequencies. These were traced to power supply switching frequency harmonics. All power leads were heavily filtered and conetic material was used between the power supply module and the low-level modulator and audio circuitry. This helped the situation considerably, but did not eliminate it. It is felt that physical isolaton of the power supply and modulator would further decrease the power supply related spurious. Also conetic material could be used for the power supply enclosure which is now steel.

The development of galium arsinide varactor diodes should be monitored closely as these units have Q's several times that of the silicon diodes as used in the experimental model radio. The GaAs diodes now available however fall short in tuning range, with hyper abrupt types just now being developed by the manufacturers. When available the use of these diodes should improve the Q of the VCO tank circuits and thus the noise component of the VCO output. This results in lowered transmitter noise and improved receiver operation under jamming conditions.

VMOS field effect power transistors, as used in the high-power VCO and buffer amplifier circuits, at this time are characterized only to 175 MHz. Each transistor must be individually evaluated for proper operation in these low-noise, high-frequency applications. It is assumed that the upper frequency of these devices will be extended in the near future and possibly, as the devices are characterized and the range extended, the

noise figure will decrease. This technology should be monitored closely for improvements which will lower the noise output of the injection system.

It was found that with very strong modulated receiver jamming signals the modulation varied the LO port impedance of the double-balanced first mixer. This varying impedance reflected to the VCO causing the VCO to shift frequency slightly (IFM) at the modulation rate, thus degrading performance of the receiver. This problem was improved in the experimental radio by use of the FET buffer amplifier, however tests showed that still more improvement was possible if an isolator was used to reduce the effect of the impedance change at the mixer. The only isolators available were physically large units with smaller versions available only on a long-lead basis from off-shore sources. Improvement can be made to the receiver jamming tolerance by use of the isolator and it is felt an isolator in the transmitter injection path would also improve transmitter performance. The isolator would replace the buffer amplifier with its associated noise contribution.

The double-balanced mixer in the receiver operates with an LO level of +27 dBm. As mixers are developed for operation with still higher LO levels, they should be evaluated as an increased LO level will further improve the intermod characteristics of the radio. It is important however that the mixer be balanced to at least 2000 MHz.

With the high-injection levels involved throughout the radio, local oscillator leakage to the antenna becomes a prominent design consideration. With totally shielded assemblies, cross coupling still occurs between coaxial cables. It is possible that multiple shielding of the cables would be beneficial. Also, to further reduce the LO antenna radiated levels, additional sections could be added to the tuned notch filter. This would be at a penalty of slightly decreased receiver sensitivity.

It was proven during the study phases of the program that the transmitter noise level can be reduced by PIN diode modulating at a higher level than is normally done, thereby reducing the broadband amplification required after the modulator. Two problems surfaced with this approach during the study. First the impedance of the PIN modulator must be kept constant to avoid IFM to the high-level VCO driving the modulator. Secondly the feedback system, associated with linearizing the transmitter and setting power levels and modulation percentages, is affected by the higher power and becomes unstable. For this reason the high-level modulator approach was not used in the experimental model transceiver. It is felt that by use of the isolator, as described earlier, between the high-power VCO and PIN modulator the first problem can be eliminated. If the feedback loop instability problem is overcome, the high-level modulator approach would markedly improve the radiated broadband noise floor.

A major improvement in the transmitter broadband noise with this design can be made by electrically relocating the receiver front-end filters. In the experimental model transceiver, two tubular filters are PIN diode switched to provide block RF filtering for the receiver in two bands. If these filters are arranged to be also in the transmit path the broadband noise in the opposite band is essentially eliminated. This configuration was breadboarded into the experimental transceiver and the transmitter noise floor was measured with and without the filter in the transmit path, and is shown in Figure 45. For this data the transmitter was at 260 MHz and the noise floor is charted from 300 to 400 MHz. The filters are rated by the manufacturer at 20 watts. The transmitter and PIN switches are capable of this operation, however, the VSWR of the filters in this application must be no more than 1.1:1 to prevent transmitter power reduction due to the protection circuitry. This approach could be further expanded by using four or more tubular filters to limit the noise bandwidth even further.

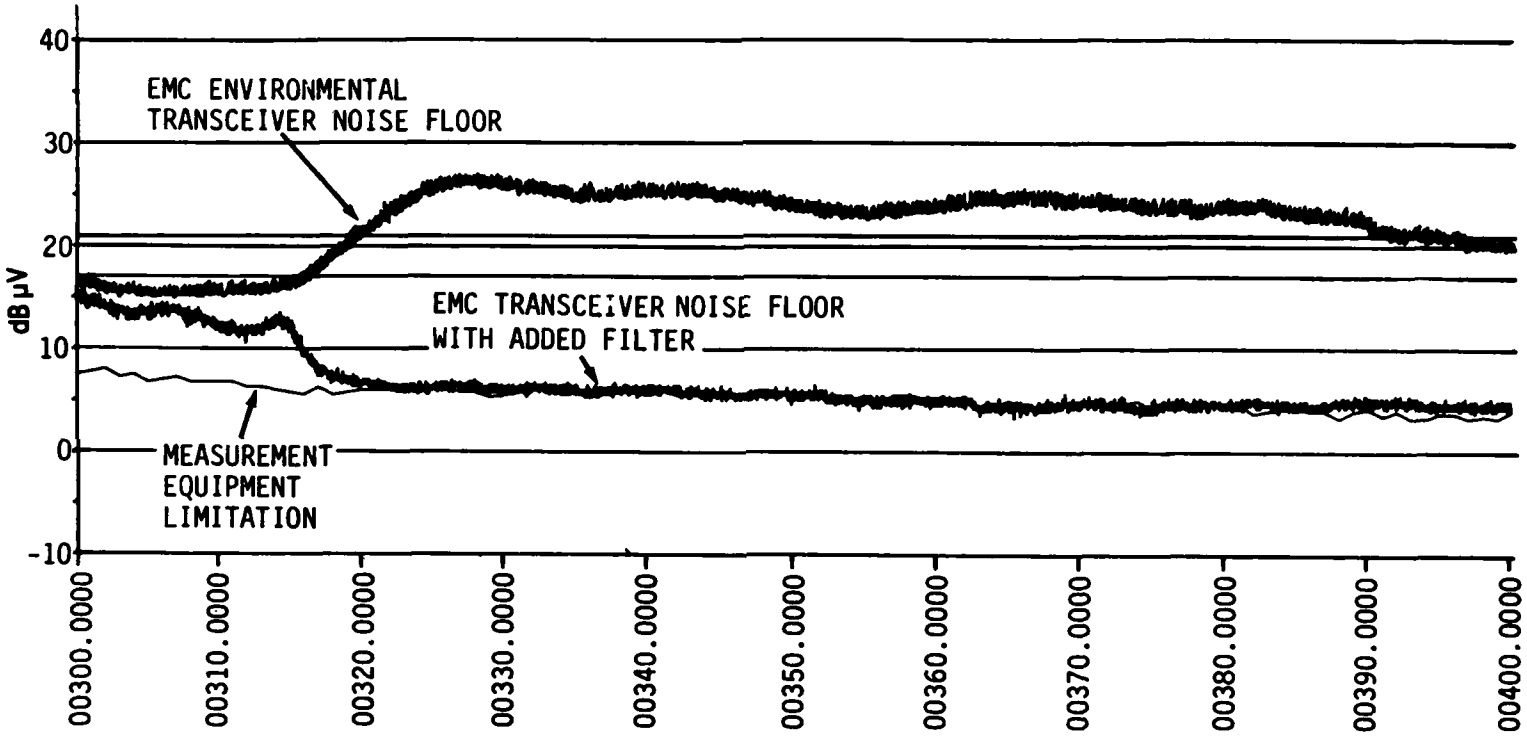


Figure 45. Transmitter BB noise improvement with added filter, transmitter frequency 260 MHz

293.0	-130	-114
294.0	-128	-112
295.0	-125	-110
296.0	-121	-107