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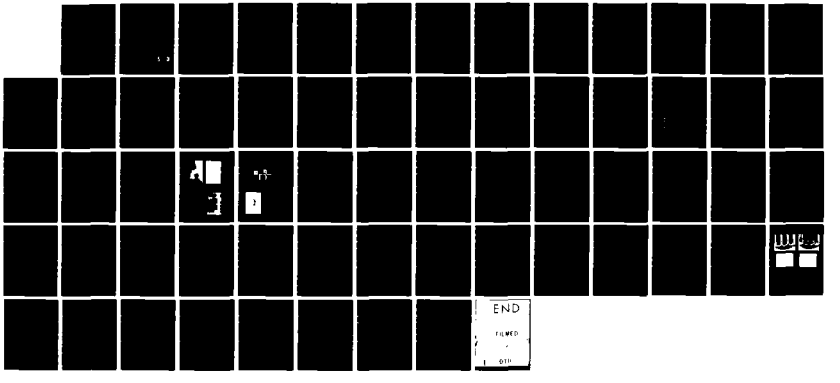

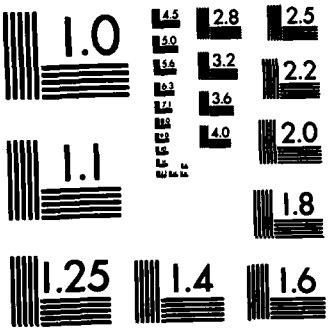

ANNUAL TECHNICAL REPORT

5/1/81 - 4/30/82

Contract #F49620-77-C-0069

MICROWAVE SEMICONDUCTOR RESEARCH -

MATERIALS, DEVICES, CIRCUITS

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This program covers the growth and assessment of Gallium Arsenide, and related compounds and alloys, for use in microwave, millimeter, and optical devices. It also covers the processing of the material into devices, and the testing of the devices. Both molecular beam epitaxy (MBE) and organo-metallic vapor phase epitaxy (OMVPE) are used for growth. Modulation doped heterostructures and very short gate field effect transistors are two areas covered. The following is a list of tasks pursued.

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Task 1 Growth and characterization of GaAs for high performance microwave devices

Task 2 Investigation of microwave field-effect transistor performance limits set by layer composition and contact geometry

Task 3 Use of MBE tailored profiles for GaAs power FET's for improved performance

Task 4 MBE multiple GaAs-$Al_xGa_{1-x}As$ heterojunctions for confinement of electrons for improved FET performance

Task 5 High speed receivers for optical communications

Task 6 Dynamic and spectral characteristics of semiconductor laser materials and structures

Task 7 Carrier dynamics in compound semiconductors studied with picosecond optical excitation

Task 8 Advanced design techniques for microwave GaAs FET amplifiers

Task 9 Wide band circuits and systems

Ballistic Task - Gallium arsenide ballistic electron transistors.

WORK STATEMENT

TASK 1 Grow and characterize GaAs for high performance microwave devices.

TASK 2 Determine the effect of design and processing on GaAs power FET performance limitations.

TASK 3 Use MBE tailored profiles for improved GaAs power FET performance.

TASK 4 Investigate MBE multiple GaAs $Al_xGa_{1-x}As$ heterojunctions for confinement of electrons.

TASK 5 Develop high speed receivers for optical communication using optical field effect transistors and large area epitaxial photoconductive detectors.

TASK 6 Model and construct components and subsystems which can be useful as transmitters in optical communication systems.

TASK 7 Develop advanced design techniques for microwave GaAs FET amplifiers.

TASK 8 Improve direct method of broad band circuit design.

TASK 9 Use optical excitation to study carrier dynamics in compound semiconductors.

TASK 10 Study ballistic electron effects in transistors for high frequency operation.

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Task 1 GROWTH AND CHARACTERIZATION OF GaAs FOR HIGH PERFORMANCE MICROWAVE DEVICES

L. F. Eastman and D. W. Woodard

Objective

Overall objectives are improved GaAs epitaxial materials for microwave devices and further understanding of substrate properties and their relation to interface and layer properties. The approach taken has been to employ deep level transient current spectroscopy ("current DLTS") to study the presence of traps in FET devices made with various implanted or epitaxial starting materials.

Progress

The technique of conductance DLTS was automated and made more sensitive. Sophisticated analysis routines (modified Boxcar, Fast Fourier Transform and Method of Moments), were developed and applied to the DLTS data in order to identify deep levels in GaAs MESFETs. Many levels found have never been reported. Conductance DLTS theory was developed to enable the calculation of trap densities thus obtaining trap density profiles in the active region of the FETs. The conductance DLTS experiment was also extended to temperatures as low as $15^{o}K$ to observe traps with smaller activation energies than previously possible. Electron traps and hole traps with energies less than 50 meV were observed for the first time in GaAs. Some of these levels can possibly be identified by comparison of the DLTS and photoluminescence data.

MESFETs fabricated from ion-implanted, MBE, VPE and LPE material were analyzed by obtaining trap profiles to enable determination of

the effects of deep levels present on the device's performance. Looping, dc drift and light sensitivity of the I-V characteristics were correllated with large densities of deep levels located at the surface and at the active region - buffer layer (or substrate) interface. Trap populations were shown to be deleterious to power applications of the devices by causing premature breakdown through impact ionization processes. It was seen that buffer layers, while decreasing the density of traps coming from the substrate, were not sufficiently opaque to eliminate them. By knowing the locations and energies of the traps in the channel, the contribution of specific deep levels to microwave performance has been calculated. Traps with energies between .07 and .2 eV contribute to the minimum excess noise figure between 1 and 80 GHz. Deeper traps, depending on their emission rates, can affect the performance of the devices down to the dc characteristics.

Electron and hole traps introduced as a result of Si_3N_4 surface passivation have been identified and profiled. Nitride capping and annealing of ion implanted material was found to introduce various low energy surface traps. The effects of these traps on microwave performance were calculated.

Degrees

G. N. Maracas, Ph.D., Jan. 1982

Publications

1. "Investigation of Deep Levels in GaAs MESFETs Introduced by Device Processing", G.N. Maracas, J.G. Tenedorio, A.O. Tenedorio and L.F. Eastman, Proc. 8th Biennial Conf. on Active Microwave Semiconductor Devices and Circuits, Cornell University, Ithaca, NY (Aug. 11-13, 1981); 149-158 (1982).

2. "The Analysis of Exponential and Nonexponential Transients in Deep-Level Transient Spectroscopy", P.D. Kirchner, W.J. Schaff, G.N. Maracas and L.F. Eastman, J. Appl. Phys., 52 (11) 6462-6470 (Nov. 1981).

3. "A Comparison of Selected Analysis Techniques for Exponential and Nonexponential Transients in Deep Level Transient Spectroscopy", W.J. Schaff, P.D. Kirchner, G.N. Maracas, L.F. Eastman, T.I. Chapped and C.M. Ranson, Proc. 8th Biennial Conf. on Active Microwave Semiconductor Devices and Circuits, Cornell University, Ithaca, NY (Aug. 11-13, 1981); 159-168 (1982).

Task 2 INVESTIGATION OF MICROWAVE FIELD-EFFECT TRANSISTOR PERFORMANCE LIMITS SET BY LAYER COMPOSITION AND CONTACT GEOMETRY

L. F. Eastman and D. W. Woodard

Objective

The objectives of this task have been to investigate experimentally and analytically the performance limits of GaAs microwave power FET devices. The approach taken has been to explore structural and materials related determinants of the breakdown voltage and output conductance.

Progress

In previous reports, FET structures having 2 micron gates and drain-source breakdown voltages of 85 volts at pinch-off were described. During the current period, the breakdown voltage of optimally designed structures was studied as a function of gate length down to 0.8 microns.

The breakdown voltage of a MESFET may be calculated by considering the operation of the device under pinched-off condition. Under these conditions a simplified electrostatic model can be used. Such a model would numerically evaluate the ionization integral over an approximate field distribution. Ladbrooke[1] has performed such computer calculations which take into account the effect of gate length on breakdown voltage. These calculations predict that the gate-to-drain breakdown voltage of the MESFET will decrease with decreasing gate length. Optimum breakdown voltages observed during the course of this work for short gate lengths (.8-1.0 microns)

indicate that this is indeed the case. Figure 1 is a plot of breakdown voltage at pinch-off as a function of gate length. The plot illustrates the calculations by Ladbrooke[1] as well as the results of this work. Also indicated is the result of Tiwari[2], at Cornell, who achieved 85 volts breakdown at pinch-off for a 2 micron gate. The results of this work, as well as the results of Tiwari, are for undoped LPE GaAs buffer layers 2.5 micron th k. As was previously discussed, this is at the optimum undoped ffer layer thickness necessary for high breakdown voltage and w leakage current. All of the data indicated is for a doping c x10^{16}cm^{-3}, where the breakdown voltages for power FET structures used in this work have been shown to have a maximum.[2] Thus, this figure is based on an optimum power structure and doping. It, therefore, indicates the best possible breakdown voltages that can be achieved given the present state-of-the-art.

Both the experimental results of this work and the theoretical results of Ladbrooke show a strong linear dependence of breakdown voltage on gate length. This result is very important for high power and high frequency MESFET design since higher frequency devices must have shorter gate lengths in order to operate at these higher frequencies, but the corresponding reduction in breakdown voltage capability with decreasing gate length limits the maximum output power of the device. There is, therefore, a trade-off between high frequency and high power performance that must be considered when designing a device for high frequency power amplification. Figure 1 can be used as a design guide to predict the breakdown voltage of a device for a given gate length.

Also studied during the present period was the microwave performance of power FET structures with 175 micron maximum finger width per cell, and airbridged source interconnects employed to combine cells up to 1100 micron total periphery. Figures 2-6 summarize the results output power versus gate periphery and gain versus frequency for device fabricated under the present program. Also included for comparison are measurements made on devices obtained from Narda Microwave Corp. and Fujitsu Laboratories.

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Degrees

J.G. Tenedorio, Ph.D., May 1982

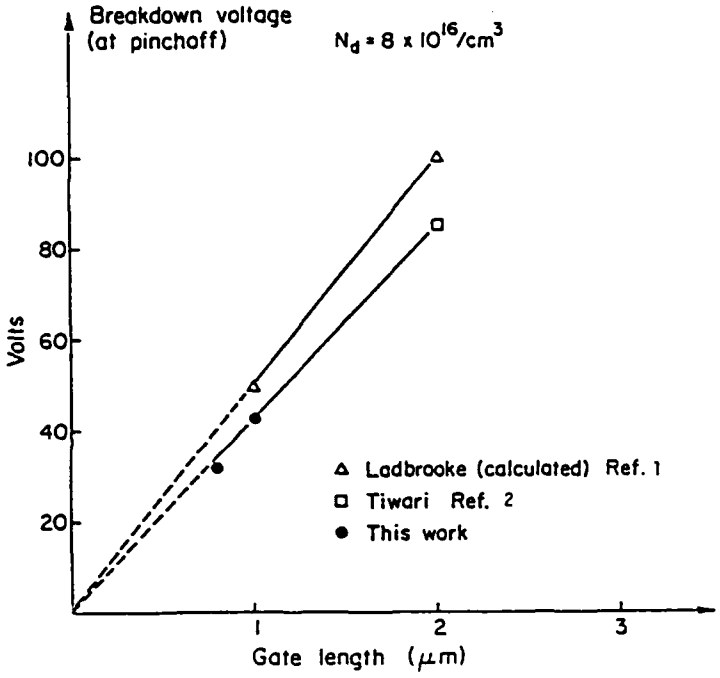

Figure 1 Plot of Breakdown Voltage (at pinchoff) as a function of gate length (N_d=8 x 10^{16} cm^{-3}).

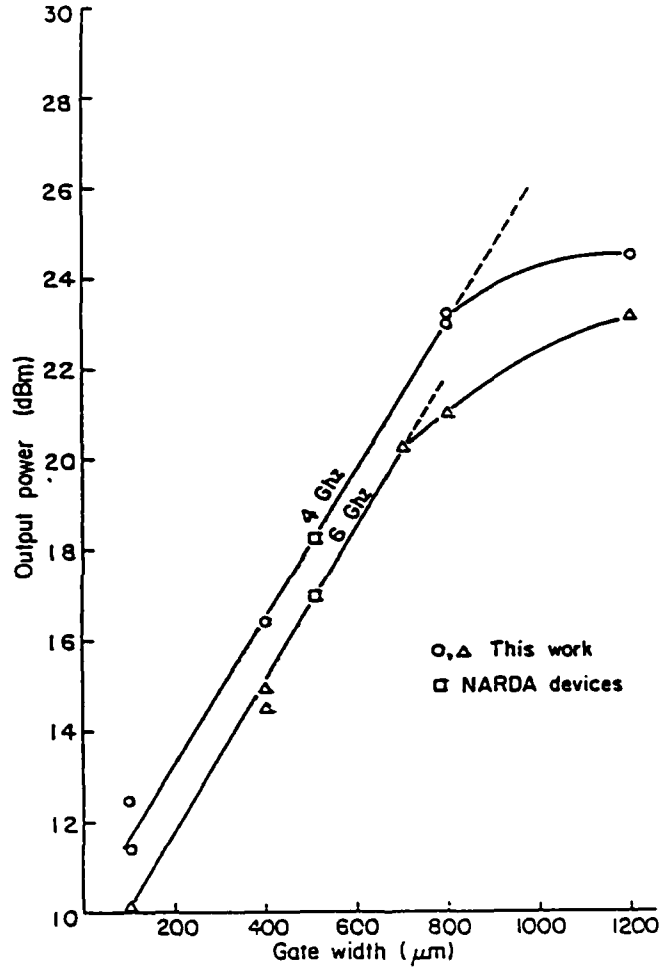

Figure 2 Output power at unity gain plotted against total gate width, for both 4 Ghz and 6 Ghz.

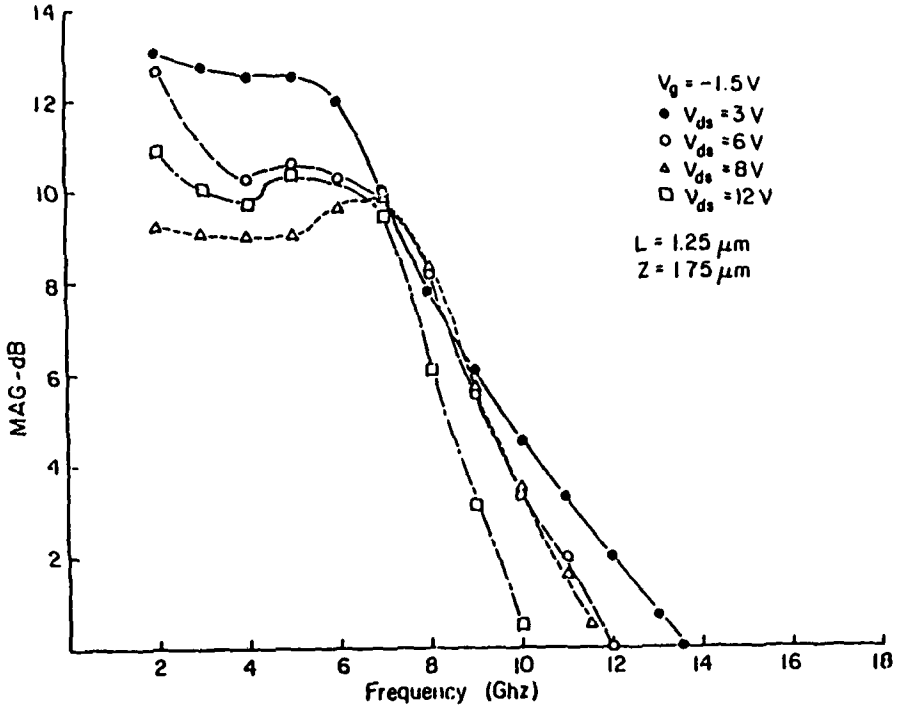

Figure 3 Maximum available gain plotted as a function of frequency for V_{ds} = 3 V, 6 V, 8 V, and 12 V.

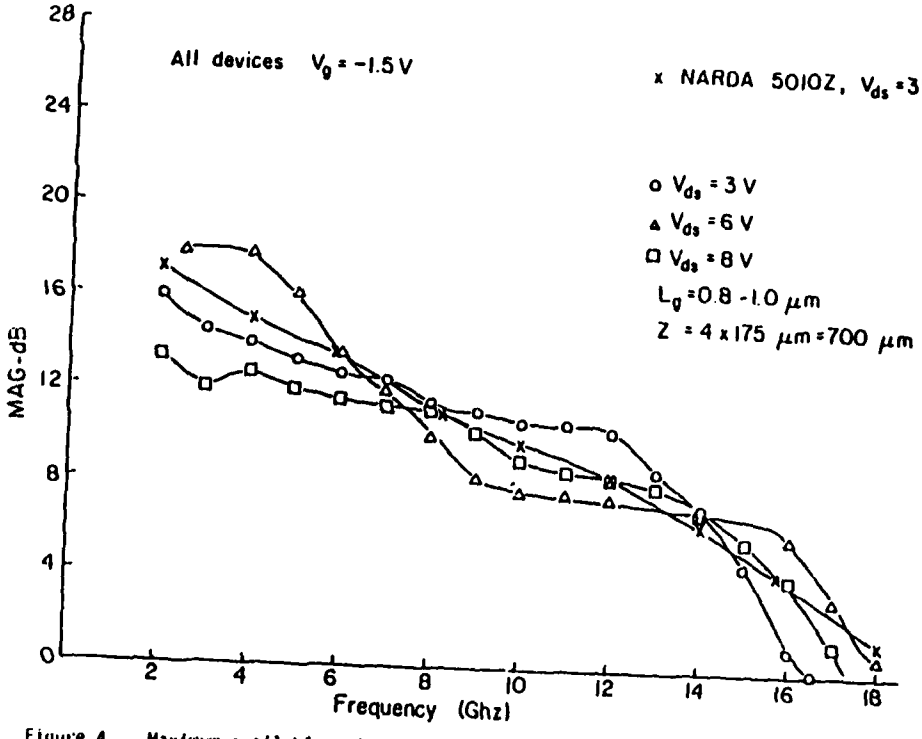

Figure 4 Maximum available gain plotted as a function of frequency for a power structure device (Z = 4 x 175 μm = 700 μm) for V_{ds} = 3 V, 6 V, and 8 V.

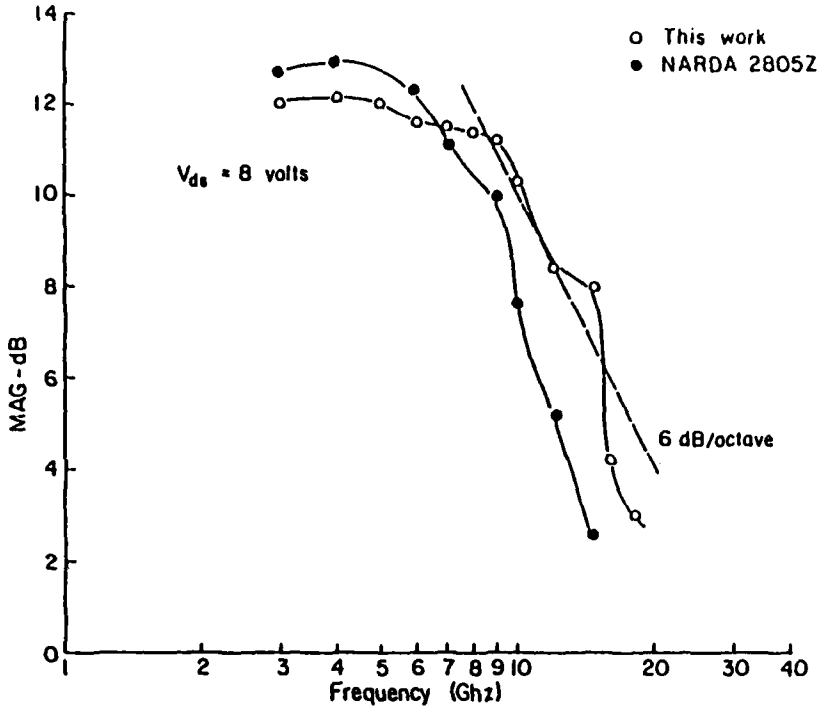

Figure 5 Maximum available gain plotted against log frequency for devices of Figure 4.8 at V_{ds} = 8 volts. (Note 6 dB/oct drop).

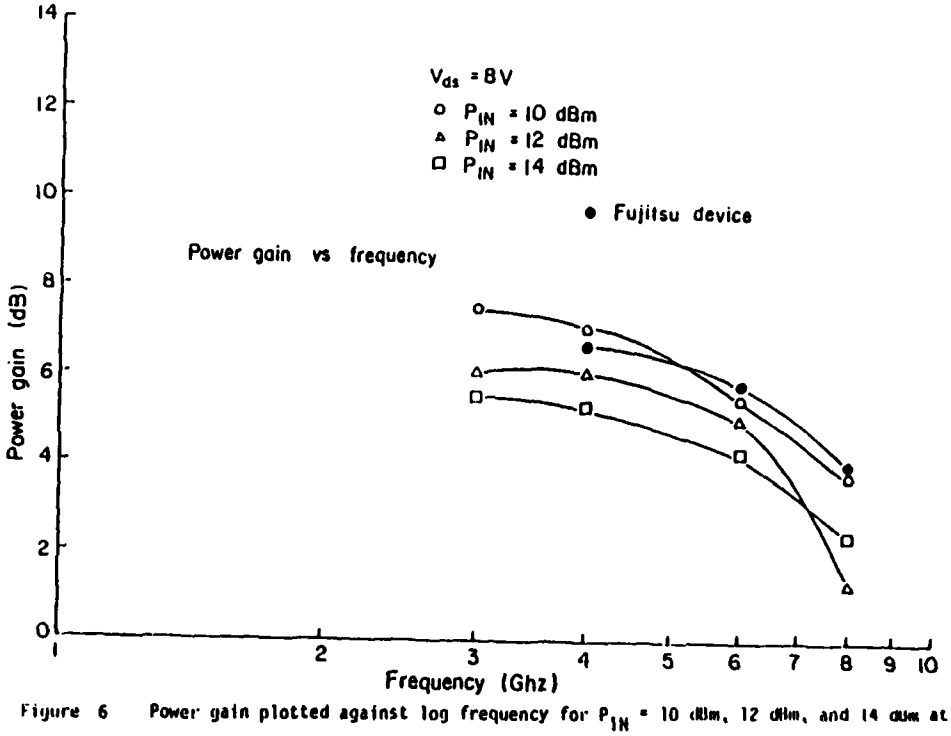

Figure 6 Power gain plotted against log frequency for P_{IN} = 10 dBm, 12 dBm, and 14 dBm at V_{ds} = 8 V. (Note slope is 4 to 5 dB/oct).

Task 3 USE OF MBE TAILORED PROFILES FOR GaAs POWER FET's FOR IMPROVED PERFORMANCE

L.F. Eastman, C.E.C. Wood and G. Wicks

Summary of Accomplishments

Following the success in our laboratory by Stall et al. of achieving extremely low contact resistances to GaAs ($\rho_c < 10^{-7}$ Ω-cm^2), an MBE grown Ge layer, a similar approach for contacts to AlGaAs was investigated. The abrupt Ge-AlGaAs heterojunction was found to have a high specific interface resistance.

For AlAs mole fractions between 14% and 37% interface resistances were between 0.08 and 8 Ω cm^2. These results indicate that the abrupt Ge-AlGaAs interface is not a low resistance ohmic contact to AlGaAs. However, by grading the AlGaAs to GaAs then depositing Ge, contact resistances to AlGaAs on the order of those to GaAs may be achieved.

GaAs layers, grown by MBE on superlattice buffer layers have been characterized by photoluminescence (PL) and found to be superior to those grown on AlGaAs or GaAs buffers. The superlattice buffer simultaneously alleviates the major problem of the GaAs buffer: the outdiffusion of impurities from the substrate, and that of AlGaAs buffers: structural problems which propagate into the subsequently grown GaAs.

Degrees

D. DeSimone, Ph.D., January 1982.

Publications

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2. "Magnesium and Calcium Doping from Dissociative Captive Sources or 'Now You See It, Now Your Don't'", C.E.C. Wood, D. DeSimone and K. Singer, Third Workshop on MBE, Santa Barbara, CA.

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7. "Manganese Incorporation Behavior in Molecular Beam Epitaxial Gallium Arsenide", D. DeSimone, C.E.C. Wood and C.A. Evans, Jr., J. Appl. Phys. (Feb. 1982).

8. "Carrier Compensation at Molecular Beam Epitaxy Interfaces", N.J. Kawai, C.E.C. Wood and L.F. Eastman, J. Appl. Phys. (Feb. 1982).

Task 4 MBE MULTIPLE GaAs-$Al_xGa_{1-x}As$ HETEROJUNCTIONS FOR CONFINEMENT OF ELECTRONS FOR IMPROVED FET PERFORMANCE

L.F. Eastman, C.E.C. Wood and G. Wicks

μ_{77} figures for modulation doped structures are routinely in excess of 100,000 cm^2/v-sec.

Annealing of modulation doped structures, necessary to achieve ion implanted self aligned FET's, was investigated. It was found that the electric field which is built into the structure causes the silicon donors in the AlGaAs to drift toward the GaAs-AlGaAs junction. When the donors reach the GaAs, the junction interdiffuses which drastically reduces the mobility of the structure. A heavily doped p-type layer added to the top of the structure inhibits the movement of the silicon donors by reversing the field in the AlGaAs layer. This allows the structures to retain their high mobility after anneals of 800^{o}C for 10 minutes or longer.

Problems in the reproducability of the barrier heights of planar doped barriers (PDB's) were traced to impurity outdiffusion from substrates. Substrate pre-baking at T > 700^{o}C in H_2 was found to solve the problems allowing the growth of PDB layers with high yield (~ 90%) and good reproducability.

Degrees

W.I. Wang, Ph.D., January 1982

G.W. Wicks, Ph.D., August 1981

Publications

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2. Surface and Interface Proximity Effect on Quantum Well Electron Mobilities in Modulation Doped GaAs/$Al_xGa_{1-x}As$ Heterostructures", W.I. Wang, N. Dandekar, C.E.C. Wood and L.F. Eastman, J. Vacuum Sci. & Tech., 19, 576 (1981).

3. "Molecular Beam Epitaxial GaAs-$Al_xGa_{1-x}As$ Heterostructures: The Influence of Growth Conditions on Interface States and Mobility Enhancement", W.I. Wang, N.V. Dandekar, S.H. Xin, C.E.C. Wood and L.F. Eastman, Electron. Lett. (Feb. 1982).

4. "Instabilities in the Growth of $Al_xGa_{(1-x)}As/Al/Al_yGa_{(1-y)}As$ Structures by MBE", K. Okamoto, L. Rathbun, C.E.C. Wood and L.F. Eastman, J. Appl. Phys. (March 1982).

5. "Evolution and Trends for M.B.E. Materials and Devices", C.E.C. Wood (invited paper), NATO-ARI on Microelectronics Meet., Les deux, France (March 1982).

Task 5 HIGH SPEED RECEIVERS FOR OPTICAL COMMUNICATIONS

J. Ballantyne and D. K. Wagner

High Speed Detector and Amplifier for Optical Communications

A GaAs MESFET amplifier has been integrated with four different types of fast photoconductive detectors of the OPFET geometry. Fabrication processes are described which yield successful integration of the different photodetectors with the GaAs MESFET amplifiers.

The four different photoconductive detectors integrated are all of the OPFET geometry. They include small OPFETs with and without notches, and interdigitated OPFETs with and without notches. The real response of the interdigitated detectors taken with a scanning laser microscope is relatively uniform, showing they behave as expected and are suitable for receiving light from optical fibers. (See Appendix 1). Gain for the interdigitated OPFET detectors was measured at about 14 (low frequency). High-speed testing of the discrete detectors was temporarily delayed due to lack of a satisfactory low capacitance carrier. However, suitable modification of existing commercial SMA end launches proved successful. Recent results show the slower detectors without notches have response speeds on the order of 200 ps. Measurements are in progress on the much faster notched detectors, which are expected to have response times of less than 100 ps.

Standard MESFET's have been successfully integrated and quite reliably fabricated with 1 micron length gates, gate widths of 50-250 microns, and transconductances of 80-90 ms/mm. The processing sequence for the monolithic circuit consists of four steps.

First, moats are etched around transistor and detector areas using a 3:1:1 methanol :H_2O_2:H_3PO_4 etch for electrical isolation. A more conventional mesa etch was not used due to technical problems in fabricating larger clear areas in masks by e-beam lithography. The moat etch is highly successful in isolating the components, however. Ohmic contacts consisting of layers of about 500 Å of AuGeNi, 500 Å Ag, 1500 Å Au are then thermally evaporated onto the substrate and annealed at 600°C for 90 s. This second step, which in addition to the normal optical photolithography also includes a liftoff of excess metallization in acetone, provides ohmic contacts and virtually all of the required metallization. The third step consists of defining uniform 1 micron gates using a projection mask aligner, etching self-aligned notches in the transistors to lower quiescent currents, evaporating about 1000 Å of Au for the Schottky barrier gates, and performing a liftoff of the excess gate metallization. The last step is a notch etch (if desired) performed on the photoconductive detectors.

At the present time a ceramic carrier has been made incorporating 50 ohmic microstrip transmission lines. The GaAs wafers have been both successfully cleaved or alternatively sawed up (with a higher yield) to obtain individual circuits. Methods of applying DC bias to the chip so that the leads are suitably bypassed at the 5-10 GHz range is a problem which is being studied at present.

In the near future the chips will be tested electrically by injecting electrical pulses and when the biasing problems have been worked out, with optical picosecond pulses. Future work will also include noise measurements and evaluation of the system.

MOCVD Growth of GaAs and AlGaAs

In work joint with Professors Eastman and Tang, the MOCVD system for the growth of uniform and large-area thin layers of III-V compounds was completed to the first phase. The system has been used to grow state-of-the-art layers of GaAs and AlGaAs. (See Appendix 2). Mobilities exceeding 90,000 cm^2/V sec at 77^oK are measured in layers of GaAs grown on the system, with total impurity levels well below $10^{15}cm^{-3}$ reproducibly achieved. High quality layers of AlGaAs are also grown on this system by the incorporation of a unique Ga/Sn/Al bubbler to remove unwanted O_2 from the source gas flows.

The system is being used to grow layers for high speed transistors and opto-electronic devices. Work is in progress to install In and P sources for growing optoelectronic materials in the GaInAlAsP alloy system.

Personnel

J. M. Ballantyne, D. K. Wagner, S. Wojtczuk, R. Shealy, K. Chan, A. von Lehmen and C. Harding

Publications and Talks

1. "Homostructure Planar-Doped-Barrier Diode as an Optical Detector", A. von Lehmen and J.M. Ballantyne, postdeadline paper at the Joint Meeting of the NSF Grantee-User Group on Optical Communications and the Department of Commerce Optical Communications Task Force, May 27-29, 1981, Washington Univ., St. Louis, MO.
2. "Photoconductive and Planar-Doped-Barrier Optical Detectors in III-V Compounds", J.M. Ballantyne, invited talk, U.S.-France Workshop on GaAs Microstructures and High Performance Devices,

Boston, MA, June 8-10, 1981.

3. "Microfabrication Techniques for Devices", J.M. Ballantyne, invited seminar, Comsat Laboratories, 9 July, 1981.
4. "Monolithically Integrated Active Optical Devices", J. Ballantyne, D.K. Wagner, B. Kushner and S. Wojtczuk, Conference on Optical Information Processing for Aerospace Applications, Aug. 1981, NASA Conference Publication 2207, p. 275.
5. "Advanced Active Devices for Optical Communication", J.M. Ballantyne, Invited seminar at General Telephone and Electronics Lab, Waltham, MA, November 6, 1981.
6. "Research and Resource at the National Submicron Facility", E. Wolf and J.M. Ballantyne, Book chapter, Microstructure, Science and Engineering/VLSI, Ed. N.G. Einspruch, Academic Press, pp. 129-182, 1981.
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APPENDIX 1

NASA Conference Publication 2207

Optical Information Processing for Aerospace Applications

Proceedings of a NASA conference
held at Langley Research Center
Hampton, Virginia
August 18-19, 1981

NASA
National Aeronautics
and Space Administration

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Information Branch

1981

MONOLITHICALLY INTEGRATED ACTIVE OPTICAL DEVICES*

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SUMMARY

We discuss considerations relevant to the monolithic integration of optical detectors, lasers, and modulators with high-speed amplifiers. Some design considerations for representative subsystems in the GaAs-AlGaAs and GaInAs-InP materials systems are described. Results of a detailed numerical design of an electro-optical birefringent filter for monolithic integration with a laser diode is described, and early experimental results on monolithic integration of broadband MESFET amplifiers with photoconductive detectors are reported.

INTRODUCTION

A number of workers have been involved in the monolithic integration of detectors and lasers with amplifiers for applications in optical communication.[1] The work reported here is specifically aimed at circuits and subsystems suitable for use in very-high data rate applications. The OPFET class of photoconductive detectors in III-V compounds shows picosecond response time coupled with internal gain and low noise. In order to realize the potential of these detectors in a practical system, monolithic integration with high-speed, low-noise preamplifiers is probably a necessity. In addition, there is a need for integration of laser diodes with high-speed amplifiers in order that complete opto-electronic systems can be constructed.

Frequency tunable lasers are useful for FM communication, for frequency multiplexed systems, and offer outstanding potential for very-high data rate transmission.[2] These may be constructed by suitable combinations of gain, birefringent and electro-optical components in the laser cavity.[3,4]

Two materials systems seem especially attractive for monolithic integration of opto-electronic subsystems. They are the GaAs-AlGaAs and GaInAs-InP heterostructure systems. The first system is useful because well-characterized opto-electronic components and amplifiers have been constructed in this system, and much is known about the materials problems which must be overcome to construct successful subsystems. The GaInAs-InP heterostructure system, lattice-matched to InP substrates, is interesting because of its potential application for longer wavelength communications, where optical fibers show minimum dispersion. A further reason for interest in this system is the very high electron saturation

*Portions of this work were supported by NASA Langley Research Center, The National Science Foundation, and the Joint Services Electronics Program at Cornell University. Facilities of the National Research and Resource Facility for Submicron Structures and the Materials Science Center at Cornell University were employed in this work.

velocity, which was shown to be the greatest for any of the GaInAsP quaternaries grown lattice-matched to InP. In previous work we showed that the electron saturation velocity in GaInAs is nearly double that of GaAs for comparable carrier densities at room temperature.[5] This enables one to construct photoconductive detectors with higher internal gain, and transistors with higher G_m and speed in the GaInAs system than in the conventional GaAs system. A drawback to the GaInAs-InP system is that unsolved materials problems must be overcome to construct successful monolithic opto-electronic circuits, and the individual devices are much less developed in this materials system, particularly the transistor technology.

SOME DESIGN CONSIDERATIONS FOR MONOLITHIC OPTO-ELECTRONIC SUBSYSTEMS

Monolithic integration of optical and amplifying devices requires semi-insulating substrates if the well-developed MESFET technology is to be utilized for amplifiers. Such substrates are readily available in both GaAs and InP; however, problems immediately arise for MESFET type transistors on InP substrates. From initial considerations, it might seem that a simple GaInAs, InP heterostructure interface would be useful for both optical and electrical confinement, and would be suitable for construction of MESFETs. One of the problems with such interfaces grown by MBE is shown in Fig. 1,[6] where it is seen that in an abrupt GaInAs-InP interface substantial leakage currents can flow which prevent construction of good transistors. In these MBE grown layers the interfacial currents were linked with the growth process for the interface, which may result in an InAsP interfacial layer with poor electrical characteristics. These problems were initially solved by incorporating Al into the system to provide an AlInAs interfacial layer between the GaInAs active region and the InP substrate.

While this approach solved problems with leakage current in transistors, it raises further problems for laser diodes. A schematic diagram of a proposed heterostructure system for monolithically integrated opto-electronic circuits on indium phosphide substrates is shown in Fig. 2. The structure indicated schematically there has the potential for producing good transistors for amplifiers, good optical detectors, and good lasers. The requirements for OPFET type detectors are similar to those of the MESFETs, which are that one be able to construct low-leakage Schottky barrier gates on active layers which are thin enough to be pinched off at a reasonable voltage, and that the structure show no excessive leakage currents through interfaces. The structure shown in Figure 2 meets these requirements. The AlInAs layer under the gate serves to make a good Schottky barrier as was previously demonstrated.[7] Fig. 2 is schematic in the sense that details of the ohmic contacts and Schottky barriers are not shown. Under the contacts, the undoped upper layers must either be removed, doped, or consumed in the contact alloying process. There are various approaches for doing these steps, the details of which are not discussed here. The requirement for pinching off the active FET layer at a reasonable gate voltage means that the thickness of the layer must be 0.2 microns or below for a doping of $10^{17}cm^{-3}$, or that the doping must be reduced for thicker active layers.

The AlInAs layer between the substrate and active layer serves to reduce the leakage currents in the transistor to reasonable values. It also serves to provide excellent carrier and optical mode confinement for the laser structure. One advantage of this material system for the TJS laser structure shown is that the cladding layers can be easily made semi-insulating, providing excellent current confinement in the TJS laser diode. Another advantage of the structure shown for the TJS laser is that it incorporates two-dimensional index guiding, which should give extremely good mode confinement. The parallel metal stripes on the surface serve as a slot waveguide to confine the lasing mode in the direction parallel to the surface. We have done extensive calculations and modeling on various geometries of these slot waveguides, some of the results of which are included in the following section.

The problem with the AlInAs interlayer is that in cases studied to date, it reduces the quality (in terms of luminescence linewidth and efficiency) of the GaInAs active layer.[8] However other workers have shown that this is not a fatal limitation[9] Substantial materials work remains to be done to solve this problem.

SLOT WAVEGUIDES FOR MONOLITHIC INTEGRATION

The slot waveguide configuration shown schematically in Fig. 2 appears to be extremely promising for monolithic integration in III-V compounds. The reasons for this are the experimental demonstration of stable guiding with very low threshold injection lasers in the AlGaAs heterostructure system[10], the compatibility with TJS lasers as shown in Fig. 2, and the obvious compatibility with electro-optic devices employing planar surface electrodes.

We have done extensive numerical calculations on the properties of slot waveguides in various geometries, and confirm that excellent low-loss waveguides can be made in various III-V compound heterostructure systems. These waveguides contain as an inherent component the electrode structures necessary for inducing electro-optic effects, or pumping TJS lasers. A further advantage of this waveguide geometry is that it is compatible with optical pumping, which is convenient for fundamental investigations. The basic geometry of the slot waveguide system we analyzed is shown in Fig. 3. The long direction of the slot is oriented along a <110> direction so that electric fields applied by the electrodes are along along <110> directions as required for usable electro-optic devices. The various guide geometries we analyzed are shown in Fig. 4. These waveguides are not only useful to provide a passive guide for a laser structure, but are also suitable for combining an electro-optically active device within a laser cavity, such as a Q-switch or a tunable birefringent filter (which will provide a frequency tunable diode laser).

We previously demonstrated the feasibility for rapid electro-optic frequency tuning of diode lasers,[3] and are now constructing a monolithically integrated version of this system. While the simple slot waveguide geometry shown as Type I can provide good guiding and low enough loss for a laser cavity, additional considerations arise when one considers electro-optic devices. (See Fig. 5 for the results in the simple system). Two additional considerations of importance for electro-optic devices are achievement of phase matching between TE and TM modes so that good conversion efficiency can be obtained on application of an electric field, and the requirement for some electro-optic structures that both TE and TM modes exhibit low loss. These requirements led to the investigation of the other waveguide geometries shown as Types II through VI. The only geometries which meet both of these requirements, of good phase matching and low loss for TE and TM modes, are Types V and VI, with Type VI being the preferred guide. As shown in Figs. 6 and 7, both of these systems can provide good phase matching; however, the Type VI

guide appears to have relaxed fabrication tolerances as compared to Type V. The fabrication tolerances are very sensitive functions of the Aluminum content in the cladding layers. Decreasing Al content relaxes these tolerances. The mode confinement for a representative Type VI guide is shown in Fig. 8 and the electro-optic coupling efficiency for TE to TM modes is shown in Fig. 9. As shown in Fig. 5, the simpler waveguide types I-IV show a great difference between loss for TE and TM modes. Such a structure would be particularly useful for Q-switching a diode laser in a monolithically integrated configuration.

INTEGRATED SUBSYSTEMS

In Figs. 10 and 11 we show the circuit diagram and photograph of a finished circuit of a monolithically integrated OPFET detector and three stage wide bandwidth amplifier. This system has been designed to give a voltage gain of 7, a power gain of 250 (over 23 dB), and a frequency response exceeding 5 GHz. One unique feature of this chip is the inclusion of a new type of interdigitated OPFET detector shown in Fig. 12. The areal response of this detector is shown in Fig. 13 which is the photocurrent due to a HeNe laser spot, raster scanned over the detector. The low frequency gain measured in this experiment was 14, which is most likely a factor of 2 larger than would be measured at high speeds. Such high speed measurements are now in progress. In Figs. 14 and 15 we show the circuit diagram and layout for an integrated laser/driver-transistor circuit being fabricated in the materials structure shown in Fig. 2. The two small FETs connected in series on the gate of the driver transistor provide a convenient, area-and-power-efficient method for setting the bias level on the laser diode.

CONCLUSIONS

In this paper we have identified what we consider to be viable approaches for the monolithic integration of detectors, lasers, amplifiers, and electro-optic components in two material systems which operate in quite different wavelength regions. For the first time, we have carried out extensive numerical calculations on slot waveguide structures in III-V compounds, and have computed parameters which are useful for the design of guides for electro-optic components in the systems. The results of these computations give information on the confinement of various geometry guides, the attenuation and the electro-optic coupling parameters of these guides. Finally, we have fabricated the most complex monolithic integrated opto-electronic circuits so far reported in III-V compounds, and have verified their performance at low frequency. We expect these circuits to give good operation at gigahertz speeds.

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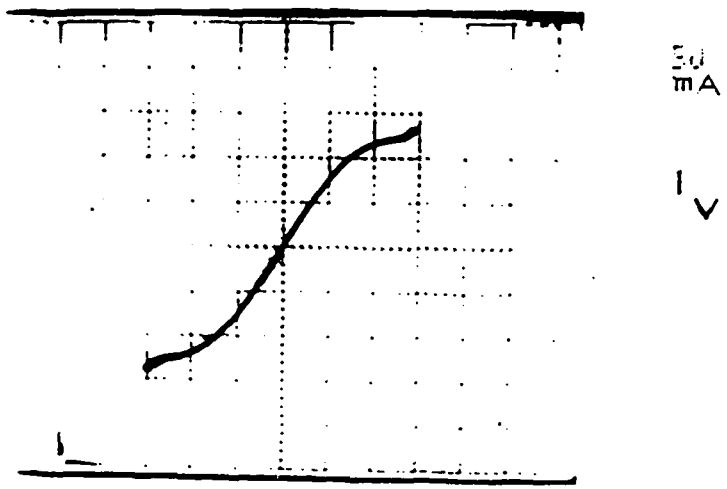


Fig. 1 I(V) curve of a GaInAs OPFET grown on an InP substrate by MBE[6]. Rise in current at end of trace is due to leakage through the substrate-epilayer interface.

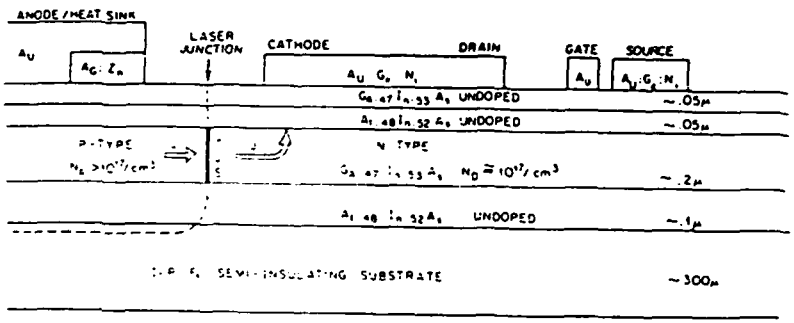
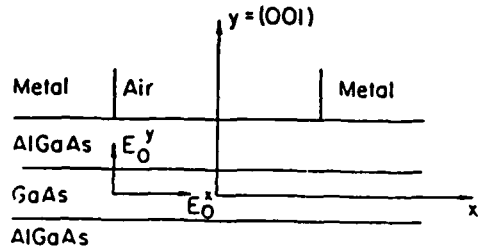
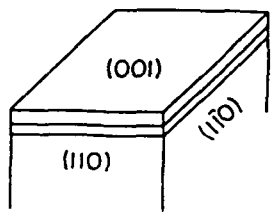


Fig. 2 Schematic diagram of proposed heterostructure system for monolithically integrated opto-electronic circuits on InP substrates.



(a)



(b)

Fig. 3 Basic geometry of a slot-waveguide structure compatible with monolithic electro-optic devices in III-V compounds.

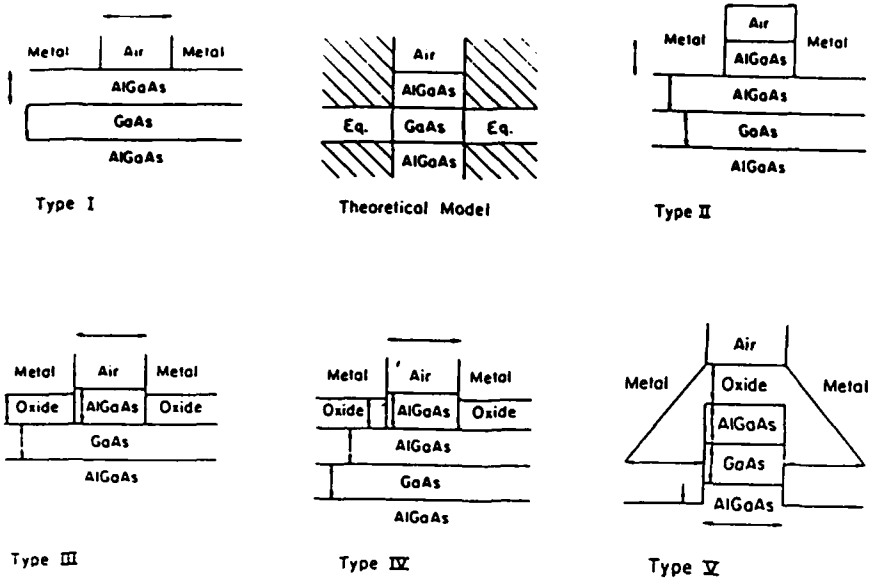
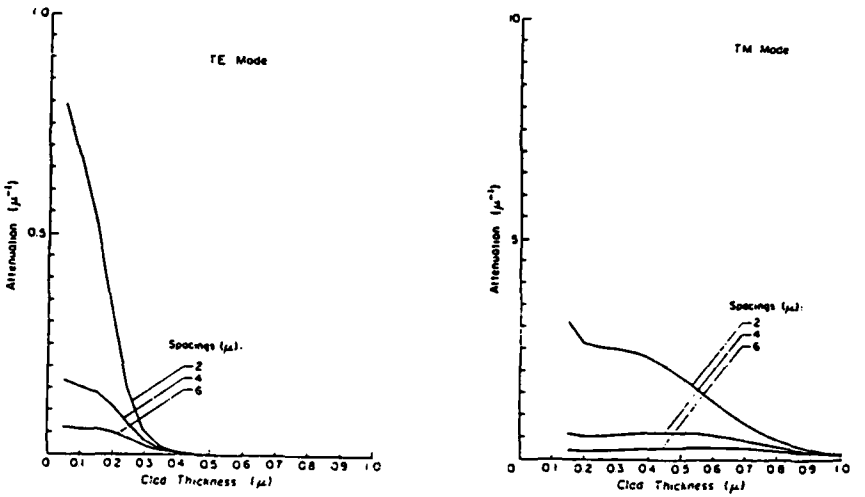
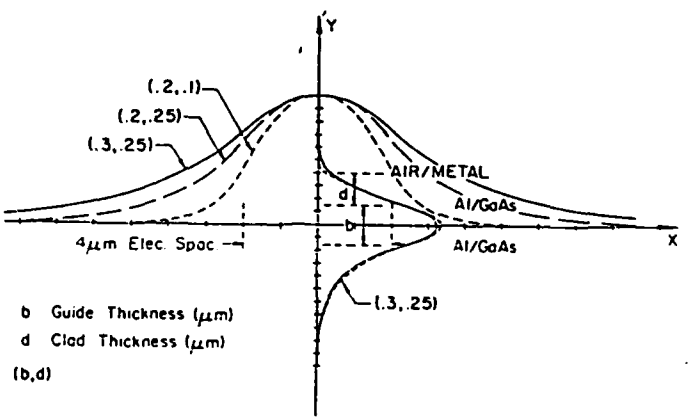


Fig. - Slot-waveguide geometries for which analysis was carried out, along with basic models used for two classes of guides.



a) Attenuation vs. clad thickness for several electrode spacings.



b) Mode confinement.

Fig. 5 Results for modes in Type I waveguide.

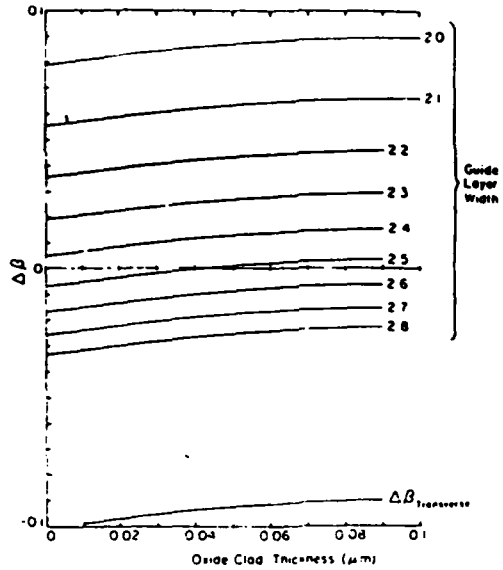


Fig. 6 Phase difference, Δδ, between TE and TM modes in Type V waveguide. Δδ is zero for a 2.5 μm wide guide and an oxide clad of 0.04 μm. Note sensitivity to fabrication tolerances.

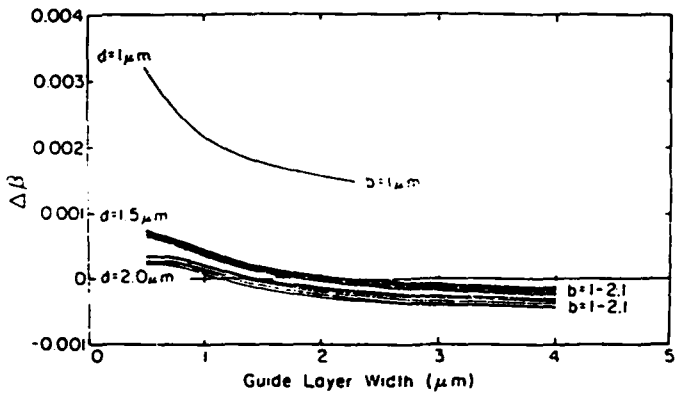


Fig. 7. Phase difference, Δδ, between TE and TM modes in Type VI waveguide: Oxide and $Al_xGa_{1-x}As$ thickness are d and b respectively. Case illustrated is for x = .05. Note large tolerances in d, b, and width to allow Δδ to be nearly zero.

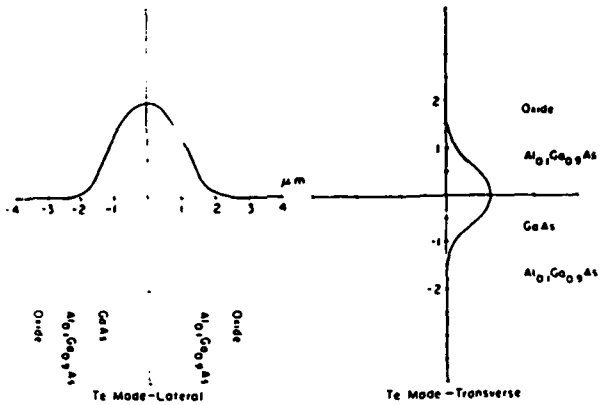


Fig. 8. Mode confinement for a representative Type VI waveguide. Amplitudes are normalized.

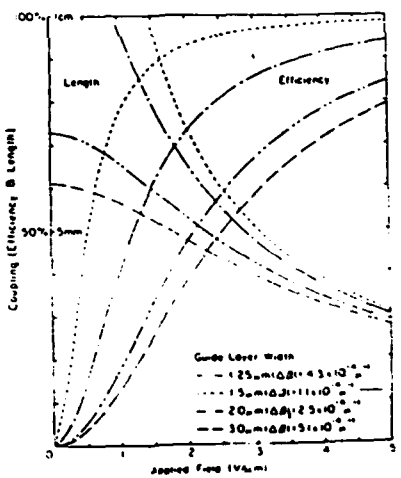


Fig. 9. Efficiency for coupling TE to TM modes in Type VI guides via the electro-optic effect.

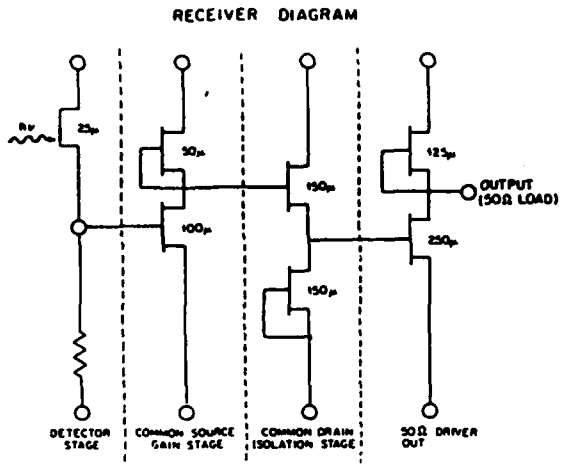


Fig. 10 Circuit diagram of a monolithically integrated receiver combining an OPFET with a 3-stage amplifier.

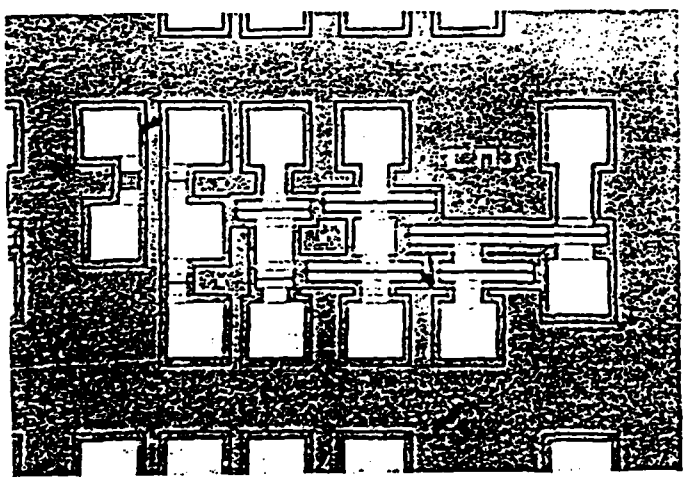
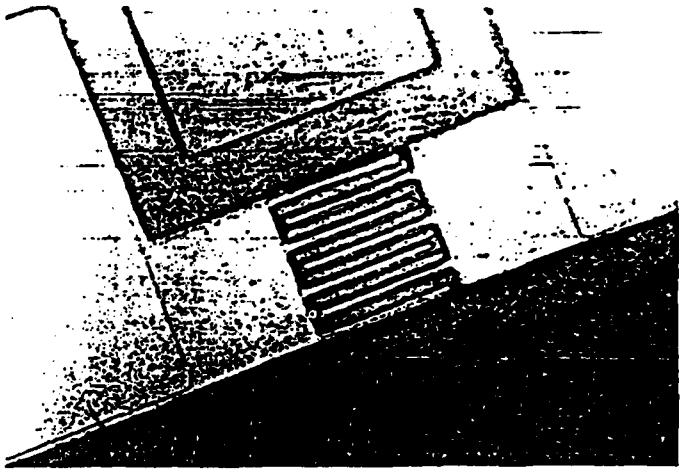
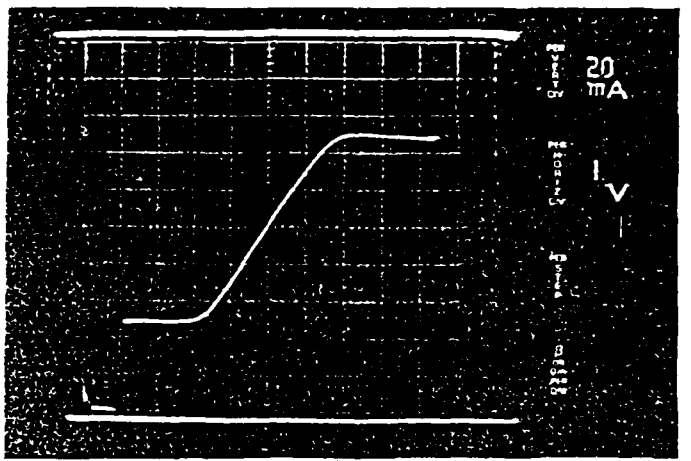


Fig. 11 Photograph of receiver of Fig. 10. Gates are missing in this photograph.



(a)



(b)

Fig. 12 Interdigitated OPFET with grooves between fingers (a), and I(V) curve of detector (b).

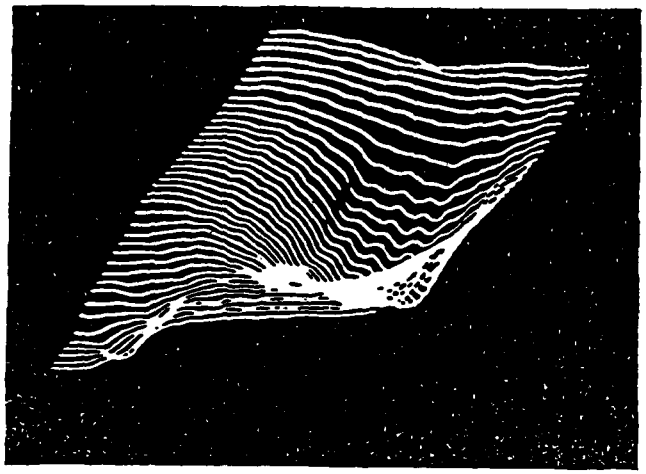


Fig. 13 Spatial response of detector in Fig. 12. Increasing response is downward. Response in lower left is an artifact due to light reflecting from bonding wire.

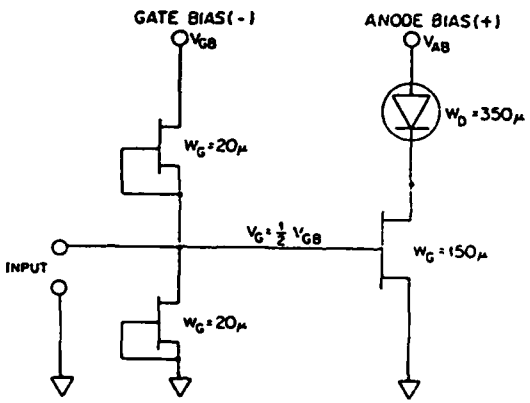


Fig. 14 Circuit diagram for an integrated laser-driver circuit being constructed in materials systems of Fig. 2.

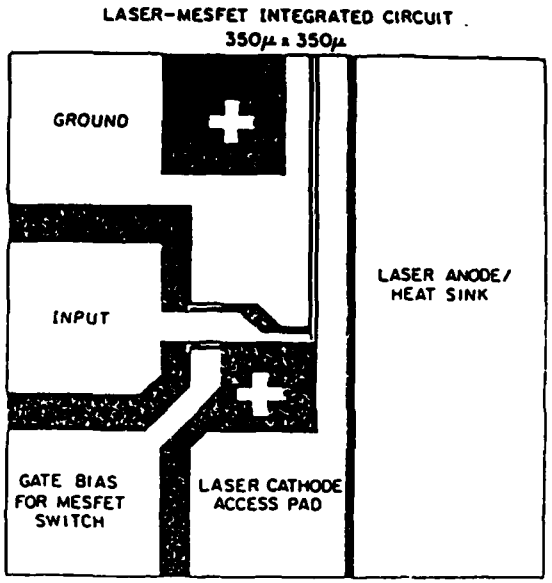


Fig. 15 Layout of circuit of Fig. 14.

Albuquerque, NM 9/19-22 Uncorrected version

APPENDIX 2

Characterization of High-Purity GaAs Grown by Low-Pressure OMVPE

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Abstract High-purity epitaxial films of GaAs have been grown by OMVPE under a reduced hydrogen pressure. These films exhibit fine exciton structure in low-temperature photoluminescence (PL) spectra and high electron mobilities (~93,000 $cm^2/V.s$) at 77K. The dominant residual impurities in undoped films have been determined by PL and far-infared photo-ionization spectroscopy for the acceptors and donors, respectively. The effects of the growth temperature, As:Ga mole ratio, arsine prepyrolysis, and in-situ etching have been investigated. Carbon-free films have been obtained with the starting sources trimethylgallium and arsine under suitable growth conditions. Finally, results on the interface abruptness of selenium-doped films grown at low pressure with high gas velocities are discussed.

1. Introduction

Organometallic vapor-phase epitaxy (OMVPE) has received an increasing amount of attention as a source for epitaxial layers of III-V compound semiconductors since its introduction by Manasevit in 1968 [1]. A variety of device structures obtained by OMVPE spanning both microwave and optical applications has been realized by workers on III-V compound semiconductor alloy systems such as GaAs/AlGaAs [2] and InP/GaInAs or GaInAsP[3]. Recently, the OMVPE process has been successfully used for the epitaxial growth of the above materials under reduced hydrogen pressure [4,5]. The use of reduced pressure in OMVPE has the potential advantages of better uniformity in thickness and doping, reduced transients when changing doping levels and alloy compositions, and the reduction of parasitic reactions encountered in premixing reactants prior to their reaching the deposition zone [6]. Devices requiring interfaces of a few monolayers, such as quantum well lasers and modulation doped FET's, have recently been realized using OMVPE [7,8,9]. In addition, OMVPE has potential for the growth of epitaxial layers with sufficient uniformity for optical and microwave integrated circuits.

In this paper, we report the optimization of the growth of high-purity GaAs at a reduced hydrogen pressure. The conclusions resulting from this investigation are applicable to multilayer device structures incorporating GaAs and other III-V compounds. For example, we have determined that by using in-situ etching and a high As:Ga mole fraction, the optical quality of epitaxial GaAs at a given growth temperature can be improved substantially.

2. Experimental

The epitaxial growth apparatus is similar in design to low-pressure reactors used by Duchemin et. al. for GaAs and InP growth with the following exceptions:
(i) During operation at low pressure, no flow restrictions are present between the sources and the reactor cell. A hydrogen manifold and all gas sources (i.e. AsH_3 and dopants) are maintained at 4 psig. The gas expands as the pressure is dropped across the mass flow controllers (MFC) to the growth pressure (76 Torr for all experiments except in-situ etching). The trimethylgallium (TMG) bubbler is downstream from its MFC which results in a reduced pressure (~ 76 Torr) over the liquid in the bubbler. This increases the TMG transport in the hydrogen carrier gas by approximately one order of magnitude compared to the same mass flow at atmospheric pressure.
(ii) Between growth experiments provision has been made to bake the reactor cell with a furnace to a temperature of 900°C at atmospheric pressure for cleaning. Any poly GaAs material left after baking is removed by introducing a small amount of HCl (~ 10sccm) into the hot cell and is condensed on a water-cooled baffle near the exhaust. This proceedure avoids the problem of disassembling the reactor cell for cleaning.

The substrates used in all experiments were (100) Cr-O doped. In addition, un-doped LEC semi-insulating substrates were used in in-situ etching experiments. The wafers were prepared by: degreasing in organic solvents, chemically etching in 5:1:1(H_2SO_4:H_2O_2:H_2O) for 15 minutes, treating in warm DI H_2O for 30 min for a native oxide growth, and submerging in 3:1 (HCl:H_2O) for 5 min to remove the native oxide. Loading was accomplished in a dry N_2 ambient. Experiments were carried out consisting of a preanneal in arsine, followed by etching in HCl and arsine (when etching was used), then GaAs epitaxial growth. The hydrogen carrier flow throughout each part of this sequence was maintained at 7 slm. During the preanneal a flow of approximately 6 sccm of arsine was used to prevent any surface decomposition of the GaAs substrate. The 15 min preanneals were done at atmospheric pressure at a substrate temperature of 650°C for layers grown without the in-situ etch and 900°C for layers grown with an in-situ etch. When used, the in-situ etching followed the preanneal at 900°C and was carried out at atmospheric pressure. The etch was done by adding 2 sccm of HCl gas into the reaction chamber and resulted in an etch rate of 2000 Å/min. Typically 2 mm of surface was removed prior to the growth. Following the preanneal and the etching steps, the reactor pressure was decreased to 76 Torr, the substrate temperature and arsine flow adjusted and stabilized, and the TMG was introduced into the reactor to initiate the GaAs growth. The TMG temperature was maintained at -14.3°C and the hydrogen flow through the TMG bubbler was 2.5 sccm for all experiments. These conditions produced a growth rate of approximately 400 Å/min with a uniformity across a 2" wafer of ± 3%.

Experiments were done to determine the effect on film properties of in-situ etching, arsine cracking, substrate temperature during growth, and V:III ratio. The arsine cracking was done in a hot-wall silica tube heated to a temperature of 750°C. The substrate temperature range investigated was from 600 to 700°C. The V:III ratio was varied from 5-120 by changing the arsine flow. Changes in these growth parameters had little effect on the growth rate. The epitaxial film thicknesses were typically around 10 mm for all the characterization studies.

The carrier concentrations were evaluated by capacitance-voltage and Hall measurements. Hall mobility data were taken on conducting films at 300 and 77K a magnetic field of 2kG. The optical quality of the GaAs epitaxial layers was assessed by high-resolution (.2Å), low-temperature (3K) photoluminescence measurements. Photoluminescence measurements at 12K were performed to determine the dominant residual acceptor impurities. Far-infrared photo-ionization data were taken on an undoped film grown under optimum conditions in order to determine the dominant residual donor species. The deep levels in the epitaxial layers and their concentrations were evaluated by DLTS experiments. Finally, the interface abruptness between doped regions was evaluated from C-V data at room temperature and compared to the expected Debye tails calculated for the doping levels obtained.

3. Results and Discussion

In order to reduce the contamination from the GaAs substrate surface from chemical cleaning and impurity redistribution effects, HCl in-situ etching was used prior to epitaxial growth. Without in-situ etching, substantial concentrations of Fe, Mg, Cr, and Mn have been observed at the interfaces of epitaxial layers grown by OMVPE on semi-insulating substrates [10]. With etching, the build up of carbon at the growth interface has been reduced to non-detectable limits, as observed by a SIMS analysis.[11] Figure 1 illustrates the effects of a preanneal and in-situ etching on GaAs semi-insulating substrates used in this study. The temperature of 900°C was chosen for the etch to ensure a mass-transport-limited process which has previously been shown to eliminate surface faceting due to a kinetically-controlled reaction [12].

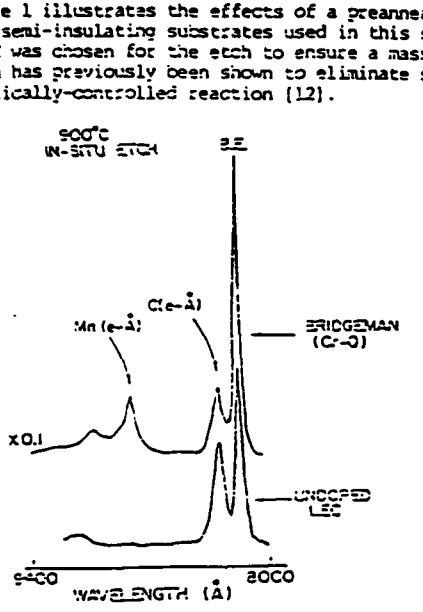


Fig. 1. Photoluminescence data at 3K on semi-insulating substrate after HCl vapor etching. The excitation wavelength and illumination intensity were 6421 Å and ~30W/cm² respectively.

The PL efficiency of each substrate was improved over an order of magnitude as a result of the anneal and etching treatments, indicating a reduction in the non-radiative defect centers in these materials. As seen in the figure, the Bridgeman Cr-O doped substrate has manganese present near the surface, and the PL intensity is 20 times that of the undoped LEC substrate. The manganese concentration in the Bridgeman material was not sufficient to thermally convert the surface. Carbon is also present in each substrate before and after the annealing and etching but its PL signature relative to the bound exciton peaks is reduced after the etching step. This result is useful in interpreting the origin of carbon observed in the PL of the epitaxial layers to be discussed later.

As reported by Dapkus et.al.[13] a much higher arsenic mole fraction is required in the growth ambient for reduced-pressure growth than is normally required at atmospheric pressure. Because high V:III ratios make inefficient use of the AsH_3 source, we have investigated in detail the effects of V:III ratio on electrical and optical properties of undoped films at relatively low ratios for which it is practical to operate the reactor. Also we have determined that the V:III ratio can be reduced substantially when the AsH_3 is prepyrolized.

Hall data were taken on films grown at 650°C under various V:III ratios, and film thicknesses. The results are shown in Table I. The best films were obtained for V:III ratios near 70 and have 77K mobilities of 93,000 $cm^2V^{-1}s^{-1}$. Little dependence on the film thickness is observed as demonstrated by the two films grown with V/III = 72. However, the thinner film (4.1μm) did not conduct at room temperature. As indicated by Table I, as the V:III ratio decreases, the total number of shallow impurities (N_d+N_a) increases faster then the net (N_d-N_a), meaning the concentration of shallow acceptors increases with decreasing V:III ratio.

Table 1. Hall data on undoped GaAs films grown at 650°C

V:III Ratio	Conductivity Type	Thickness (μm)	Mobility ($cm^2V^{-1}s^{-1}$) 300K	77K	Carrier Concentration (cm^{-3}) Net	Total
72	n	11.5	8000	93,000	$2(10^{14})$	$7(10^{14})$
72	n	4.1	*	88,000	$2(10^{14})$	$7(10^{14})$
55	n	7.8	7300	61,000	$2(10^{14})$	$2(10^{15})$
36	n	12.0	6500	37,000	$5(10^{14})$	$4(10^{15})$
24	p	6.5	340	3,250	$1(10^{15})$	- - -
5	p	21.0	300	3,170	$7(10^{15})$	- - -

*film did not conduct at 300K.

These residual acceptors have been identified by PL as carbon and zinc. Their relative concentrations are strongly dependent on the V:III ratio as indicated by Figs. 2a and 2b. This behavior is expected since at higher V:III ratio, i.e. arsenic-rich conditions, the incorporation of carbon on an arsenic site is less likely, due to the higher arrival rate of arsenic at the growth interface. Similarly, the incorporation of zinc on a gallium site is favorable under arsenic-rich conditions. However, from the Hall data it was determined that the total acceptors, carbon and zinc, decrease with higher V:III ratios indicating that carbon is the dominant acceptor species grown under lower V:III ratios and that its concentration decreases with increasing V:III ratio. As a result, by using sufficiently high V:III ratios we have obtained carbon-free films for the first time with the starting sources TMG and arsine. The photoluminescence spectra for these films are shown in Fig. 2b for a V:III ratio of 120 and in-situ etching. Similar PL spectra have been observed on films grown under similar conditions with triethylgallium (TEG) and arsine [14].

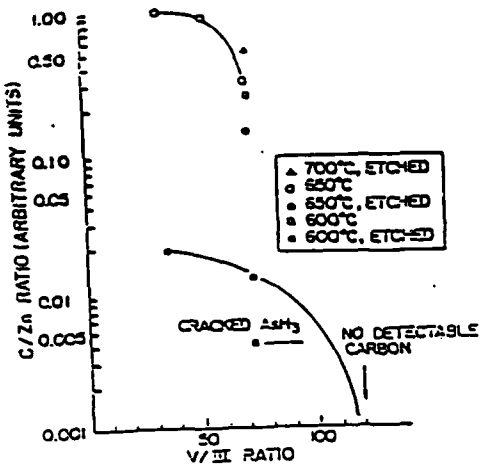


Fig.2(a) C:Zn ratios as deduced from photoluminescence data at 12K. Excitation wavelength and illumination intensity were 6421Å and 30W/cm², respectively.

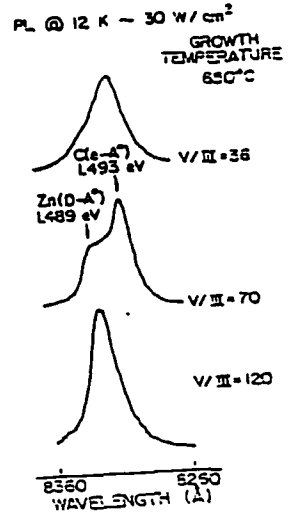
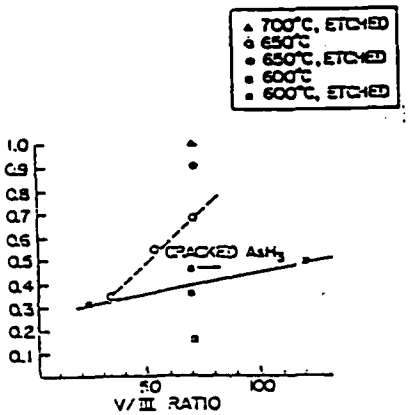


Fig.2(b) Photoluminescence data at 12K with same excitation wavelength. GaAs films were n-type and in-situ etched.

Fig. 2a shows the increase in C:Zn ratio with increasing growth temperature. We attribute this behavior to an increase in carbon concentration from the decomposition of organic radicals on the surface at higher temperatures. In addition, a strong dependence of the C:Zn ratio is observed when in-situ etching was used. This effect is more pronounced at lower growth temperatures. We believe that carbon is present on the chemically-cleaned substrate surface and is eliminated by in-situ etching. It is difficult to explain how the carbon concentration at the surface (which is as much as 10 μm away from the growth interface) is reduced by the in-situ etch but the data reflect this trend over a broad range of growth conditions. It is seen from Figs. 2a and 3a that the arsine pre-pyrolysis at 750°C effectively increases the V:III ratio by over 50% when the substrate temperature is 600°C. No other effects were observed by the arsine pyrolysis: however, an increase of silicon contamination would be expected from the hot silica wall if higher pyrolysis temperatures were attempted.

The effects of the V:III ratio and in-situ etching on the band edge PL at 3K are shown in Figs. 3a and 3b. As indicated, the in-situ etching improves the PL efficiency of the free exciton (FE) transition by a factor of 3 and 1.4 for growth temperatures of 600 and 650°C, respectively. Also the PL efficiency (FE) increases when higher V:III ratios and higher substrate temperatures are used. The effect of V:III ratio is more pronounced at higher growth temperatures. For a growth temperature of 650°C, the exciton structure at the band edge changes with the V:III ratio as shown in Fig. 3b. At low V:III ratios where the carbon concentrations are the largest, the exciton-bound-to-carbon-acceptor transition dominates the PL spectrum. At the other extreme at high V:III ratios, where little or no carbon is detectable by PL, the exciton-bound-to-donor transitions dominate the PL spectrum. Other transitions observed in the spectrum are labeled in a similar fashion as was done by Bhat et.al. in earlier work [14].



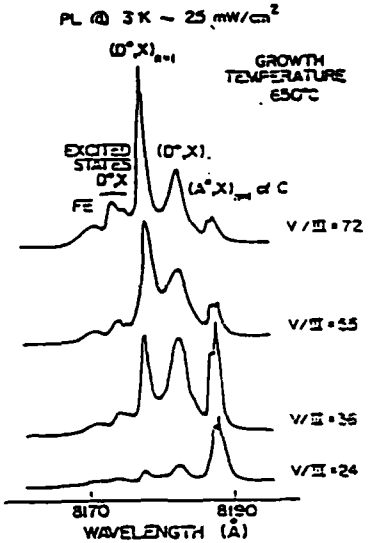


Fig. 3(a) Free exciton PL efficiency vs V:III ratio of undoped GaAs films. Excitation wavelength was 6421Å and illumination intensity was 25 nW/cm². (b) PL data on undoped films at 3K. (Without in-situ etching.)

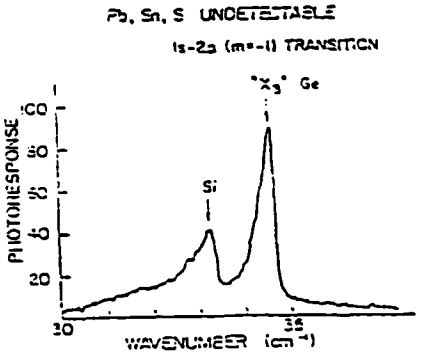


Fig. 4. Far-infered photoionization data indicating the residual donor species in a GaAs film grown at 650°C with a V:III ratio of 72. The mobility of this film at 77K was 93,000 $cm^2v^{-1}s^{-1}$.

The residual donors were identified on an undoped film grown with a V:III ratio of 72 and a growth temperature of 650°C by far-infared donor spectroscopy [15]. The result is shown in Fig. 4. The spectrum is dominated by the "X_3" center which has been observed in all OMVPE GaAs. Silicon donors are also present in undoped layers as shown. Attempts to identify the "X_3" center using transmutation doping experiments[16] suggest that it may be due to the presence of Ge donors. However, no Ge acceptors or silicon acceptors have been observed in the PL spectrum. The silicon acceptors may be masked by the presence of larger quantities of Zn, but with Ge, which occupies both Ga and As sites, it appears that the acceptor should be detectable with PL when relatively large concentrations of the donor species are present. Some question as to the exact species responsible for the X_3 center and its origin still remains. Also indicated by the figure, common impurities in OMVPE GaAs such as Pb, Sn and S are undetectable in these films.

The characterization of the GaAs films for interface abruptness and deep level contents were accomplished on films doped with Se using hydrogen selenide as a source. Several films were prepared at different V:III mole ratios with an intentional doping level of ~ $5(10^{16})cm^{-3}$ for the DLTS experiments. Using optical stimulation, no hole traps were detectable by DLTS experiments. The sensitivity of the DLTS measurement was ~$5(10^{12})cm^{-3}$ trap concentrations. With electrical stimulation, the presence of "EL2" was detected in epitaxial layers grown on semi-insulating or n^+ substrates. As observed previously[17], the concentration of EL2 increases with the V:III mole ratio. For example, our films grown at 650°C with V:III mole ratios of 24, 35 and 72 have an "EL2" concentration of approximately $5(10^{12})$, $2.2(10^{13})$, and $4.0(10^{13})$ cm^{-3} respectively. These "EL2" concentrations are comparable to the state of the art achieved by OMVPE at atmospheric pressure[17]. The "EL2" concentration appears to be more sensitive to the growth temperature than the V:III mole ratio. For example, increasing the substrate temperature from 600 to 700°C at a V:III mole ratio of 55, the concentration of EL2 increases almost one order of magnitude.

A primary consideration for the use of low-pressure in OMVPE is the interface abruptness which can be obtained between regions of different doping. Figures 5a and 5b illustrate the interface abruptness obtained for layers grown without stopping the growth as measured by C-V

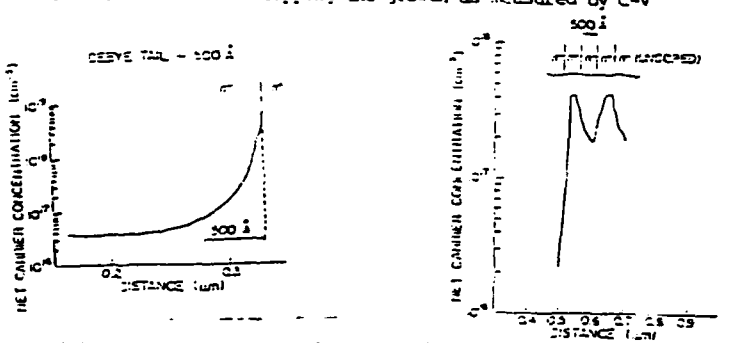


Fig. 5(a) C-V doping profile of a vertical FET structure grown by OMVPE using H_2Se doping; (b) C-V doping profile of an alternating doped-undoped structure.

measurements at 300K. In Fig. 5a, the measured Debye tail at the n^--n^+ interface corresponds closely to the calculated value of 500 Å, suggesting that the interface region is less than 100 Å. In Fig. 5b, a C-V profile of a repetitive structure consisting of 500Å of alternating doped and undoped regions is shown.

4. Conclusions

The growth of GaAs by OMVPE at reduced pressure has been optimized for the best optical and electrical properties. Fine exciton structure in low-temperature PL is obtained on samples grown over the entire range of substrate temperatures and V:III mole ratios at reduced pressure. Best mobilities and lowest background carrier concentrations were obtained on films grown at 650°C with a V:III ratio of 72. Deep level concentrations in these films are below 10^{14} cm^{-3} when the substrate temperature is less than 650°C. Arsine cracking at 750°C reduces by as much as 35% the amount of arsine required for optimum film quality. Finally, in-situ etching using HCl has significantly reduced the carbon content in the films and increased PL efficiency. Using in-situ etching, carbon free layers are reproducibly obtained with the starting sources TMG and arsine.

Acknowledgements

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Task 6 DYNAMIC AND SPECTRAL CHARACTERISTICS OF SEMICONDUCTOR LASER MATERIALS AND STRUCTURES

C. L. Tang

Summary of Accomplishments

I. The ultimate speeds of semiconductor electronic and optic devices depend upon the relaxation time of hot electrons in the conduction band and the transit time of ballistic electrons over submicron distances in semiconductors. These are in the sub-picosecond (10^{-13} to 10^{-12} sec) range. Thus, to determine these time constants, a time resolution less than 0.1 psec (10^{-13} sec) is required in the measurements. In a related project sponsored mainly by the National Science Foundation, we have recently developed a technique[1-4] that allows one to measure certain optical processes in liquids and solids down to 60 femtoseconds (6×10^{-14} sec), which is more than an order of magnitude faster than any optical phenomena previously measured. Work is under way to extend such experiments to semiconductor electronic and optic devices. This work is carried out partly under the auspices of the JSEP program.

II. Luminescence decay and injected carrier lifetime in the high injection region of AlGaAs laser diodes have been measured.[5] Using an optical gating technique, decays in the high injection region of laser diodes following current pulse excitation were measured with a 100 ps time resolution. The observed luminescence decay is shown to be strongly affected by the gain in the active region. It is also shown that both monomolecular and bimolecular carrier recombination must be considered. A model has been developed

that takes these effects into account and is shown to accurately describe the steady-state and decay spontaneous emission intensities from laser diodes. A procedure is outlined for determining the necessary device and material parameters for interpreting laser diode characteristics.

III. In a related project, a nondestructive optical technique that is accurate and direct for measuring the diffusion profiles of photo-generated electrons and holes in semiconductors has been developed. The time evolution of the diffusion profile of electrons and holes in GaAs has been measured for the first time with a time resolution of 0.5 nsec. The results are being prepared for publication. Combination of this type of measurements with the optical-gating technique described above (II) will allow one to study the relaxation of hot electrons in semiconductors and thus help to determine the ultimate speeds of response of semiconductor devices.

IV. Coherent optical interference effects in external-cavity semiconductor lasers have been observed and interpreted.[6] A broadening of the apparent linewidth of semiconductor laser modes with external optical feedback is observed. This is shown to be due to the coherent nature of the feedback and multiple reflections in the external cavity. A theory for the steady-state behavior of the external-cavity semiconductor laser taking into account such coherent optical effects is developed. The inclusion of these effects is also important in the interpretation of the threshold data of such lasers.

V. Pulses on the order of 6-8 psec are obtained in an actively mode-locked external-cavity antireflection (AR) coated semiconductor laser. We also report the mode-locking of a ring-cavity

semiconductor laser.[7,8]

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3. "Observation of light induced refractive index change in molecular liquids by femtosecond interferometry", C.L. Tang and J-M. Halbout, invited talk, XIIth International Conference on Quantum Electronics, Munich, Germany (June, 1982).

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Task 7 CARRIER DYNAMICS IN COMPOUND SEMICONDUCTORS STUDIED WITH PICOSECOND OPTICAL EXCITATION

G. J. Wolga

This reporting period was the first year in which we had JSEP support. The primary objectives for the period were to set up laboratory facilities for generating tunable, picosecond optical pulses in the red - near infrared spectral region corresponding to the bandgaps of common compound semiconductor materials, to set up diagnostic facilities for measuring the special pulse duration and characterizing the shape of the pulse, and to commence setting up the first experiments. A synchronously mode locked, tunable dye laser pumped by a mode locked Krypton ion laser was purchased. After some delay in receiving the laser system, we were limited in operating it until several months had passed because of inadequate electrical service in the laboratory. Subsequently, this problem was eliminated and the laser has been operating very satisfactorily. As delivered and installed, the dye laser was producing 1-1.5 picosecond pulses at an 82 MHz pulse repetition rate in the 7000 Å region. We have obtained continuous tunability over a 900 Å range with a single dye. An additional limitation during the first year was that essentially the entire budget was allocated to procurement of the laser system and thus no graduate students were supported. Two students did associate themselves with the project and are now receiving support from JSEP funds.

To measure the dye laser pulse duration we designed an optical Michelson interferometer with calibrated variable spacing in one arm.

This apparatus permits us to measure optical pulse duration by observing the autocorrelation between an optical pulse and a time delayed optical pulse obtained from it. We have designed the interferometer with both a sinusoidal time delay (using an audio speaker cone to provide the motion) of variable amplitude for rough measurements and tuning up of the laser, and with calibrated linear time delay (using a dc servo motor driving a precision translation stage) for precise measurements. The interferometer functions properly and has been incorporated as a permanent part of the laser apparatus.

Experimental studies are planned in two areas. The first involves the use of photoexcited fast photoconductors coupled by strip lines as pulsed current generators and as sampling gates to study charge carrier relaxation in compound semiconductors. The basic structure involves a strip line deposited on a semiconductor film with a ground plane beneath. Gaps in the strip line form fast photoconductors when radiation damaged. The photoconductors are illuminated with pico second pulses generating electron-hole pairs causing conduction across the gaps. By delaying the optical excitation of one gap with respect to the other, the delayed gap acts as a sampling gate permitting autocorrelation of the current pulse to be accomplished. The detected autocorrelation pulse shape and width is a function of pulse propagation on the strip line and can be analyzed to characterize the material properties of the strip line. As described above, fast photoconductors illuminated with pico second optical pulses form the building blocks (pulse generators and sampling gate) for pico second electronic systems. We plan to extend

these techniques to the study of new materials, more complex circuits, and to the development of a measurement system for the characterization of ultrahigh speed electronic devices.

To date our progress in this area includes the development of suitable fabrication techniques for microstrip transmission lines with micron size gaps. The substrate preparation is done with a two step lithography-lift off process. High quality 11 micron wide transmission lines with 3 micron gaps have been fabricated and mounted in a versatile substrate fixture. The optical components required to focus one or more beams with variable time delay in at least one beam path have been assembled. The present configuration is suitable for device measurement via autocorrelation techniques. The adjustable path length can be adjusted with 1 micron precision. A semiinsulating InP substrate with 11 micron wide microstrip and a 3 micron gap has been tested. InP was chosen because it was believed to have very fast electron relaxation without additional processing. The response of the gap to a 3 psec, 1 n joule pulse has been directly measured with a 24 psec resolution sampling oscilloscope. We observed a scope limited (< 50 psec) rise time and a much longer exponential decay. The decay indicated that our fixture requires some improvement and we are redesigning it. A two gap transmission line structure is currently under investigation with the goal of initiating autocorrelation studies.

The second area of work involves picosecond optical excitation of compound semiconductor materials across the bandgap and observation of luminescent decay. We are setting up a low temperature optical device to hold the sample with both direct

observation of the luminescence and the capability for autocorrelation measurements. Initial experiments will include discrimination of the hot electron tail in photoluminescence, and observation of bandedge shifts under high power excitation. We are also planning a study of variation in luminescence as the optical excitation promotes electrons below and above the upper valley in Gats.

Task 8 ADVANCED DESIGN TECHNIQUES FOR MICROWAVE GaAs FET AMPLIFIERS

W. H. Ku

Objectives

The primary objectives of this research program are to develop advanced and integrated analytical and computer-aided design (CAD) techniques for the synthesis and design of microwave GaAs MESFET amplifiers leading to monolithic microwave integrated circuits (MMICs). A secondary objective of this research program is to fabricate GaAs MESFETs and circuits in microstrip and monolithic realizations using both low-noise and high-power submicron gate-length MESFETs to verify the integrated design approach developed in the main portion of this JSEP program.

Progess (or Results)

Significant progress was made during the year in both theoretical and experimental work on the sub-half-micron single-gate and dual-gate GaAs MESFETs and amplifiers. Using optical lithography, sub-half-micron GaAs MESFETs have been successfully designed and fabricated. 0.2 micron length mushroom gate GaAs MESFETs are fabricated using a new single-level photoresist techniques. Measured gate resistance from this test device was 6.1 Ω/mm gate width which is the lowest value ever reported for gates of equal length. Using this technique, GaAs single-gate and dual-gate MESFETs with 0.3 microns long mushroom gates have been fabricated. At 18 GHz, maximum available gain of 9.5 dB in the single-gate FET and maximum stable gain of 19.5 dB in the dual-gate FET have been measured.

In the areas of GaAs MESFET amplifier design, we have completed the development of large-signal broadband amplifier design techniques resulting in the successful fabrication of two medium-power ultra-wideband amplifiers in microstrip. These amplifiers cover 2-8 GHz and 2-10 GHz frequency bands and the experimental results verify the computer-aided design techniques involving broadband large-signal characterizations of the FETs. During this reporting period we have initiated the design of MMIC broadband amplifiers using the APPLICON in the Submicron Facility at Cornell. The submicron gate-length FETs will be fabricated using the optical lithography techniques.

Based on the sub-half-micron GaAs MESFETs developed at Cornell University, we have also developed new design techniques for the design of direct-coupled feedback amplifiers and distributed amplifiers. New computer-aided synthesis and design programs are being developed which will incorporate both lumped and distributed circuit elements and nonlinear models of the active devices. Specific applications for these new programs include the design of mixers and monolithic power amplifiers.

Publications

1. "Modelling of Dual-Gate MESFETs with Second Gate Forward Biased", P.C. Chao and W.H. Ku, Electronics Letters, Vol. 17, No. 16, pp. 574-576, August 6, 1981.

2. "Computer-Aided Synthesis of Monolithic Microwave Integrated Circuits (MMICs)", L.C.T. Liu and W.H. Ku, Proceedings of the Eighth Biennial Cornell Conference on Active Microwave Semiconductor Devices and Circuits, pp. 283-295, Ithaca, NY, August 11-13, 1981.

3. "High Aspect-Ratio 0.1 Micron Gate Structures for Super Low-Noise GaAs MESFETs", P.C. Chao and W.H. Ku, Proceedings of the Eighth Biennial Cornell Conference on Active Microwave Semiconductor Devices and Circuits, pp. 189-198, Ithaca, NY, August 11-13, 1981.

4. "A Submicron Gate-Wall Structure for Low-Noise MESFET's", P.C. Chao and W.H. Ku, Proceedings 1981 IEEE International Electron Devices Meeting (IEDM), pp. 92-95, Washington, D.C., December 7-9, 1981.

5. "A High Aspect-Ratio 0.1 Micron Gate Technique for Low-Noise MESFET's", P.C. Chao, W.H. Ku and J. Nulman, IEEE Electron Device Letters, Vol. EDL-3, pp. 24-26, January 1982.

6. "Experimental Comparison in the Electrical Performance of Long and Ultrashort Gate Length GaAs MESFET's", P.C. Chao, W.H. Ku and J. Nulman, IEEE Electron Device Letters, Vol. EDL-3, pp. 187-190, August 1982.

7. "A Pile-Up Masking Technique for the Fabrication of Sub-Half-Micron Gate Length GaAs MESFET's", P.C. Chao, W.H. Ku and C. Lowe, Accepted for publication in the October 1982 issue of the IEEE Electron Device Letters.

Task 9 WIDE BAND CIRCUITS AND SYSTEMS

H. J. Carlin

General

The research under this task has been primarily concerned with two basic applications of circuit techniques. The first concerns the fundamental limitations on broad band equalizers plus the use of computer aided design (CAD) techniques to obtain optimum equalizers within these constraints. Particularly emphasized are the implementation of the general methods for the design of microwave FET amplifiers.

The second topic is concerned with a new approach to disspersion analysis in wide band dielectric waveguide (e.g., graded index dielectric guide) using distributed parameter circuit modeling.

Wideband Equalization (H.J. Carlin and B.S. Yarman)

As a consequence of the Ph.D. research of Siddik Yarman under this contract we have obtained a new and general analytic gain-bandwidth theory for the double matching problem. This concerns the case where a complex source feeds a complex load and is basic for the design of interstage equalizers in broadband amplifiers. We have implemented certain aspects of the double matching problem into a "Real Frequency" CAD procedure which avoids many of the difficulties inherent in the implementation of the analytic theory.

In connection with this research a basic paper has been accepted for publication by the CAS Trans of IEEE entitled "The Double Matching Problem: Analytic and Real Frequency Solutions". We believe this paper represents a breakthrough in that a simple and complete

theory of the difficult wideband double matching problem has been delineated. Furthermore our Real Frequency procedure of single matching has been extended to the double matching problem resulting in a viable CAD method for obtaining practical interstage equalizer designs.

A version of this CAD method applied to multistage microwave FET amplifiers was presented at the May 1982, IEEE MTT Symposium in Dallas. Finally an IEEE MTT Trans paper entitled "A Simplified Real Frequency Technique Applied to Broadband Multistage Microwave Amplifiers" by B. S. Yarman and H. J. Carlin has been accepted for publication.

Circuit Modeling of Dielectric Guide for Dispersion Analysis (H. J. Carlin and H. Zmuda)

A new and simple network approach for computing the dispersion characteristics of multi-step and continuous graded index dielectric slab waveguide has been studied. The analysis is performed from an electromagnetic wave and circuit theoretic point of view. Thus, compared to a ray optic approach, a somewhat different perspective as to the physical mechanisms underlying the phenomenon of improved dispersion characteristics are obtained. The transverse geometry of the slab is modeled using a cascade transmission line circuit, each line having a characteristic impedance which is frequency dependent. Circuit analysis of this cascade directly yields the eigenvalue equation of transverse resonance analysis. The transmission line system in fact emulates the performance of the actual graded index structure by exhibiting a terminal plane on one side of which the lines propagate and beyond which they are cut off. The location of

this plane depends on the spatial distribution of dielectric constants, the free space wave number, and the mode in question. Indeed, in this model it is the existence of this transverse cutoff which gives the graded index slab its desirable dispersive properties. The relatively poor dispersion characteristics of the uniform dielectric slab can be attributed to the abrupt step discontinuity at the air/core interface. In the graded index case, an evanescent section of lines existing between the propagating lines and air provide shielding which in effect prevents the propagating section of lines from "seeing" the abrupt dielectric discontinuity at the air/dielectric interface. The propagating portion of the line system on the other hand functions like an impedance matching transformer. The exact electromagnetic field solution for the graded index slab with dielectric permitivity varying as $1-x^2$ is given by confluent hypergeometric functions. Computational difficulties arise for such functions in a frequency range of interest (specifically, a normalized frequency of $K_0 d = \omega \sqrt{\mu_0 \epsilon_0 d} = 100$ which corresponds to an operating wavelength of approximately 1000 nm for a typical guidewidth of d = 15 μ). The transmission line circuit model that we are investigating yields an excellent approximation to the exact structure for only a 10-line cascade. The table below compares the deviation from asymptotic group delay τ_g (= dβ/dKo) with $K_0 = 20$, and $\frac{\epsilon_m}{\epsilon_0} = 2.45$. At this frequency the exact solution is "well behaved" numerically and a comparison is readily made for the first five TE symmetric modes as below (in nanoseconds/meter)

Mode	$t_g - \sqrt{\epsilon_m/\epsilon_o}$	$t_g - \sqrt{\epsilon_m/\epsilon_o}$
1	2.129×10^{-3}	1.676×10^{-3}
2	34.37×10^{-3}	34.83×10^{-3}
3	125.9×10^{-3}	127.2×10^{-3}
4	277.3×10^{-3}	278.5×10^{-3}
5	499.7×10^{-3}	501.0×10^{-3}
	10 line cascade	exact

At a typical operating frequency of $K_o = 100$ (normalized) the deviation from asymptolic group delay for the first five TE symmetric modes via a 10-line model are (in nanoseconds per meter)

Mode	$t_g - \sqrt{\epsilon_m/\epsilon_o}$
1	0.2240×10^{-3} ns/m
2	0.7819×10^{-3} ns/m
3	1.149×10^{-3} ns/m
4	1.545×10^{-3} ns/m
5	2.897×10^{-3} ns/m

The intrinsically simple form of the cascade allows easy computation of the group delay at any frequency possibly on a computing machine as simple as a hand calculator, but the true beauty of the technique is that arbitrary grading profiles should be readily analyzable even in instances where an exact solution of the differential equation is impossible and numerical solutions of such equations difficult at best.

Transfer of Information

1. In December 1981 our gain bandwidth technique was used by R.C.A. Government Systems Division in the design of broadband microwave antenna equalizers.
2. H.J. Carlin presented an invited paper at the European Circuits Conference, The Hague, August 1981, on some of the wideband equalization methods developed under this program.
3. H.J. Carlin gave invited seminars at the Institute for System Analysis, Turin, Italy, January 1982, on wideband equalizers and circuit modeling of dielectric waveguide.
4. H.J. Carlin gave a seminar on gain bandwidth techniques at RCA, David Sarnoff Research Center, March 1982.

Technical Publications

1. H.J. Carlin and P. Amstutz, "Broadband matching", Ann. Telecommunications, V. 36, No. 5-6, May-June 1981, pp. 281-294.
2. H.J. Carlin and S. Yarman, "The double matching problem: analytic and real frequency solutions", to be published IEEE Trans. CAS.
3. B.S. Yarman and H.J. Carlin, "A simplified real frequency technique applied to broadband multistage microwave amplifiers", to be published IEEE Trans. MTT.

Degrees

1. B.S. Yarman completed his Ph.D. program. Dissertation: "Broadband Matching a Complex Generator to a Complex Load", January 1982.
2. H. Zmuda completed his M.S. program. Thesis: "Simplified Dispersion Analysis of the Multistep and Graded Index Dielectric Slab Waveguide", May 1982.

Task 10 GALLIUM ARSENIDE BALLISTIC ELECTRON TRANSISTORS

L.F. Eastman, D.W. Woodard, C.E.C. Wood and G. Wicks

Progress

A multilayer heterojunction photo-transistor (HPT) structure has been grown by molecular beam epitaxy (MBE) with a double base structure. The first base region close to the $Al_xGa_{1-x}As$ emitter layer is $Al_yGa_{1-y}As$ with $y < x$. ($x = 30\%$, $Y \simeq 12\%$), Be doped $p \simeq 10^{17}$ cm^{-3}. The second base region 1000 Å thick is GaAs Be doped 10^{19} cm^{-3}. The aluminum mole fraction ratio is graded between the emitter and $Al_yGa_{1-y}As$ base region. The interface between the two base regions is abrupt. With this double base region configuration, the heterojunction transistor has exhibited a typical dc current gain β of 175. Moreover $\beta = 1$ for a current density as low as 10^{-3} A cm^2 due to a lower recombination current in wide gap depletion region. Very small area transistors has been fabricated with an interdigited structure. Emitter base junction area is 6 x 30 μm^2 and base collector area, is 30 x 40 μm^2. The capacitance measured at 1 MHz for these devices are a $C_{EB}^{(0V)} = 0.5$ pF and $C_{BC}^{(0V)} = 1.6$ pF (including the pads).

The transition frequency of the device has been inferred from S parameter measurements $f_T = 7$ is close to 8 Hz. $I_C = 5$ mA and $V_{CE} = 8$ V.

The response speed of the phototransistor has been tested by a syncronously pumped dye laser. The pulse width is 3 ps with a wavelength of 720 nm.

As compared to previous work, the response time is very short, τ

= 250 ps for a load resistance R_L of 1 Ω. The dc current gain is 15 and optical current gain is evaluated to 10-12. The dependence of the response time on bias conditions shown that the response time, in this optimum configuration, is given by $\tau \simeq \beta \tau_{ec}$, where τ_{ec} is the total emitter to collector transit time.

Work was done with graduate student Susan Palmateer on the growth of planar doped barriers in GaAs and the effects of impurity out diffusion from substrates on the diode characteristics. PDB's were grown by MBE and processed for characterization as ballistic electron launchers, however this work remains incomplete.

Work was also done on a new type of rectifying heterojunction structure in the AlGaAs-GaAs system. The structure is a triangular barrier n-n heterojunction exhibiting unipolar transport which has applications in barrier transistors, ballistic electron launchers, and possibly tunnel diodes.

Diode structures have been fabricated by MBE. Diodes have been processed and characterized by DC I-V measurements. Rectification has been observed at room temperature for a number of AlGaAs composition.

A computer model based on thermionic emission has been developed which provides rough agreement with experimental data.

Attempts to realize vertical microwave transistors in GaAs with various sizes have been made by MIT-Lincoln Labs., Westinghouse and Cornell. For mm-wave performance sub-micron technologies have been primarily directed towards gate length control.

A novel vertical electron transistor (VET) which combines for the first time both lateral and vertical submicron dimensions was

done (figures 1 and 2). It major advantages are:

i. The submicron drain to source contact spacing allows for the first time to study the impact of near-ballistic electron transport on transistor performance.

ii. The technology is amenable to the incorporation of hot electron launchers via MBE or MOCVD.

iii. The unique technological approach allows the fabrication of different channel slopes to optimize the intrinsic device configuration for mm-wave applications.

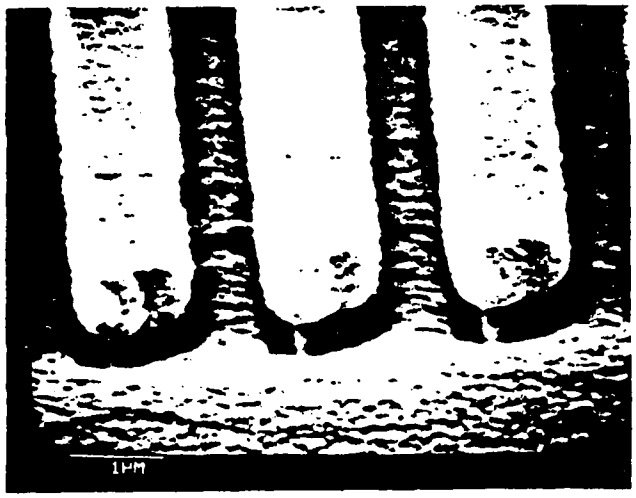
iv. The use of thick Schottky gate metallization minimizes gate resistance.

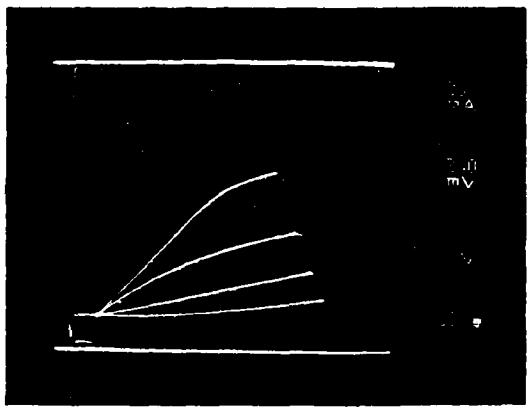
First devices were fabricated by MBE with 0.5 micron active layers of two doping levels sandwiched between n^+ contact layers. Patterning of the submicron channel configuration was done by optical lithography and a combination of dry and wet etching. Rectangular and trapezoidal channel cross-sections were realized. (See figures 1(a) and 2(a)). The Schottky gate was angle-evaporated onto the channel side walls.

The device characteristics are summarized below (also see figures 1(b) and 2(b)).

Active layer doping	7×10^{15} cm^{-3}	5×10^{16} cm^{-3}
Gate periphery	640 microns	640 microns
Source drain spacing	0.5 microns	0.5 microns
Gate length	0.15 microns	0.15 microns
g_m	47 mS/mm	81 mS/mm
Gate-drain breakdown	~ 10 v	~ 10 v
Active input cap. at 1 MHZ		$\leq$ 0.33 pF

Fig. 1



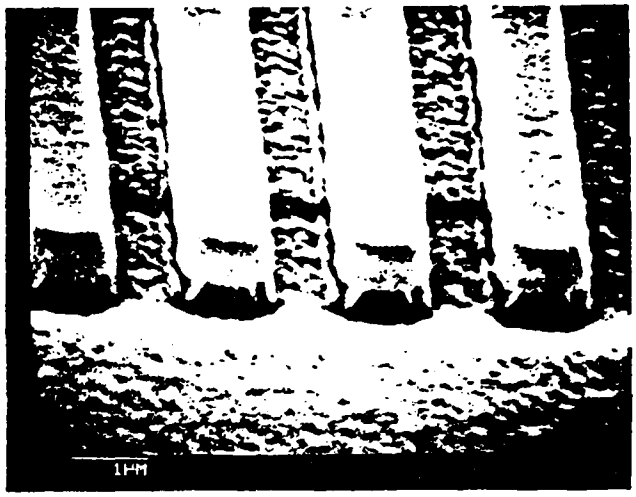


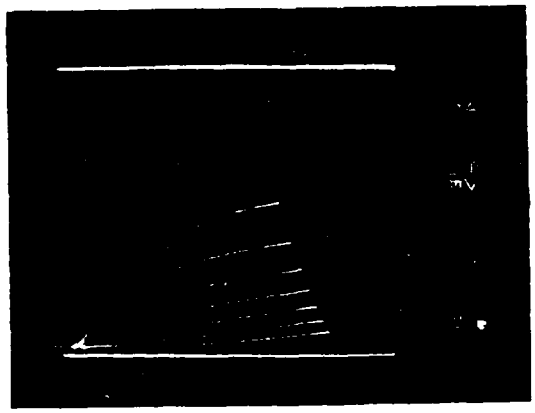
(b) gate offset +0.5V

channel doping:

$N = 5 \times 10^{16}\ cm^{-3}$

Fig. 2





(b) gate offset +0.5V

channel doping:

$N = 7 \times 10^{15}\ cm^{-3}$

Back contact is the drain

Fingers form the source

Recessed metallization is the gate contact

The measurements on 5 x 10^{16} cm^3 devices conservatively predict an f_T of 24 GHz. In the 7 x $10^{15}cm^3$ devices, electron average velocity appears to be around 3 x 10^7 cm/s based on current flow considerations. Subtracting parasitic elements leads an estimated intrinsic f_T of around 50 GHz. Further device analysis and microwave measurements are currently being undertaken.

Work was aimed at developing planar ion-implanted self-aligned submicron GaAs MESFETs. Our initial fabrication process development for these devices at Hughes was done. Sputtering of TiW with good adhesion to GaAs and plasma etch, using a metal etch mask, with good control of etch rate and undercut in a CF_4-O_2 plasma was done. Successful ion implantation and capped annealing of these structures was demonstrated with both SiO_2 and Si_3N_4 encapsulants. Diodes fabricated by this process had slightly better electrical characteristics than those originally reported by Yokoyama et al. at Fujitsu. Processing of some wafers for ring oscillator measurements were done at Hughes. When completed, these wafers had propagation delays as low as 25 ps at 300^{o}K, the fastest all-GaAs digital circuits to date. These results were reported at the 1982 Device Research Conference, and have been submitted for publication in Electron Device Letters.

At Cornell work focussed on capless annealing, alternative refractory gate metalizations, and submicron gate structures, all aimed at using this self-aligned gate process to achieve ultrashort electrical gate lengths with enhanced electron velocity.

Capless annealing studies were undertaken in several different areas. C-V profiling was used to evaluate relative activation

efficiencies for implanted Si^+ ions into GaAs under different capless anneal schedules (temperature/time), so that a suitable annealing schedule could be chosen. Studies were done of annealed TiW diodes on MBE GaAs, with encouraging results. The stability of GaAs/TiW and GaAs/Ti/Mo interfaces under capless annealing conditions was evaluated by RBS and by electrical measurements. Capless annealing of various modulation-doped structures were also done in order to evaluate their suitability for post-implant annealing.

Plasma etching and RIE of TiW under an aluminum etch mask was performed, using the etching systems at Cornell and was found to be feasible to begin device fabrication.

The first working ion-implanted SAGFET devices made at Cornell were processed during April 1982. These were entirely fabricated by E-beam lithography, using ion-implanted active layers and sputtered TiW done at Hughes. These represent the first such devices done by E-beam lithography, and the first to employ arsenic-overpressure capless annealing. In addition to process test patterns (for measurement of gate resistance, n^+ sheet resistance, device isolation, etc.), these wafers included an array of 8 test FETs with various gate lengths. The two wafers processed had electrical gate lengths (the spacing between implanted n^+ regions) ranging between 0.5 and 1.4 microns. Transconductances of 80-100 ms/mm were observed, but the devices also had an undesirably high output conductance, and exhibited a marked decrease in threshold voltage with decreasing gate length. DC measurements seemed to offer some possible preliminary evidence of enhanced electron velocity in the 0.5 micron FETs.

Related Work

The planar doped barrier transistor was proposed as a new device structure in which to study electron motion in the realm of "near ballistic" transport.

Conclusion of study of manganese in GaAs experimentally and theoretically - Mn was originally chosen as a p-type dopant to be used in the PDB structures as an alternaive to Be which is highly toxic. Mn for a number of reasons (i.e., diffusion, surface segregation and electrically inactive ($T < 300^{o}$ K)) is not a suitable dopant for the growth of PDB structures.

Growth of PDB diode structures on 360 MBE system - Si used as n-type dopant, Be p-type dopant. Due to variation of fluxes across a wafer there were large variations in doping uniformity and layer thickness which resulted in a variation of ϕ_{BO} across a 1" wafer of 50%. Symmetric around 0.5 eV-1.0 eV PDBD's were grown and analyzed.

Growth of PDBD's initiated on new Generation II MBE system - Continuous azimuthal rotation necessary for precise control of doping and thickness uniformity across a 2" GaAs wafer. Initially there was no reproducibility of designed barrier heights which was found to be substrate related. SIMS showed that the Be (p^{+}) plane in layers grown on Si-doped (around 4×10^{18} cm^{-3}) Bridgeman GaAs substrates diffused around 200 Å not observed in layers grown on Sn-doped, Cr-doped or undoped substrates. This is attributed to defect enhanced diffusion. Reproducibility of ϕ_{BO} in layers grown on Sn-doped (around 4×10^{17} cm^{-3}) Bridgeman GaAs substrates was found to be growth parameter dependent. Fast growth rate (1.6 micron/hr compared to 0.95 micron/hr) and high substrate temperature (around $640^{o}C$)

resulted in the most reproducibility. High T_s volatile unintentional impurities desorb from growth surface. Fast growth rate in the growth surface outruns substrate-epilayer interface effects and related fields which can effect impurity incorporation in the intrinsic regions. Precise control and excellent uniformity on designed barrier heights was achieved by heat-treatment of semi-insulating substrates (and removal of converted surface) (Cr-dped and undoped) prior to MBE growth. A Be cell transient was identified. The Be flux is a factor of 2.5 x higher for 10 second-1 minute shutter times as compared to infinite shutter times. The transient is reproducible from run to run.

Design, processing, measurements, and analysis of GaAs planar-doped barrier ballistic electron transistors - The epi-layer for the first successful prototype of the planar-doped barrier (PDB) transistor was grown in a Varian 360 MBE machine by Dr. Roger Malik at the U.S. Army ERADCOM in Ft. Monmouth, NJ in mid-May, 1981. The intended emitter barrier height was 0.25 V, the intended collector barrier height was 0.2 V, and the V base width was 1000 Å. The wafer was delivered to Cornell where it was processed and measured by graduate student Mark Hollis. The transistor, which is a vertical current flow device, uses two mesa etches followed either by deposition of an insulator (Al_2O_3) or by a proton bombardment step to achieve contact pad isolation. The prototype transistor exhibited no power gain at room temperature, but at $77^{o}K$ it displayed a maximum DC power gain of 2.5 dB and a maximum common-base current gain α of 0.15.

In an effort to improve on this performance, six more transistor

layers were grown at ERADCOM and processed at Cornell between July 1981 and October 1981. Measurements after processing revealed that both the emitter and the collector barriers in all six layers were effectively nonexistent (i.e., shorted out). In October 1981, work was begun at Cornell by graduate student Susan Palmateer, senior research associate Colin Wood and Mark Hollis to solve the apparent MBE materials growth problems responsible for the barrier height reduction. In December, a new Varian Generation II MBE machine was put into operation at Cornell. From January to April a large number of PDB calibration diode layers were grown on this machine. Using a procedure developed by Mark Hollis, the resulting I-V characteristics of these diodes were fitted to a thermionic emission model in order to determine the effective barrier heights and leverage ratios of the diodes. The barrier heights of these diodes were observed to vary randomly by as much as a factor of 2 or 3. In April 1982 this nonreproducibility problem was shown to be related to the outdiffusion of impurities and/or deep levels from the substrate during growth. The problem was solved by baking the wafers at 750^{o}C for 24 hours and polishing off a few microns of material before MBE growth.

The thermionic I-V model has also been instrumental in explaining the disappointing performance of the prototype PDB transistor. The real emitter barrier height has been ascertained to be 0.46 V which is well above the intervalley scattering threshold of 0.34eV, and the base doping was actually found to be roughly $10^{18}cm^{-3}$ which is a factor of 2 or 3 higher than desired. These facts combined to yield the poor α observed in the device.

All of the early planar-doped barrier problems had now been solved, and renewed PDB transistor work was begun at Cornell in late April 1982.

Degrees

R. Malik, Ph.D., August 1981

M. Hollis, M.S., May 1981

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