

AD-A114 802

ROYAL SIGNALS AND RADAR ESTABLISHMENT MALVERN (ENGLAND)
A TRUE LOGARITHMIC IF AMPLIFIER FOR RADAR APPLICATIONS.(U)

F/G 17/9

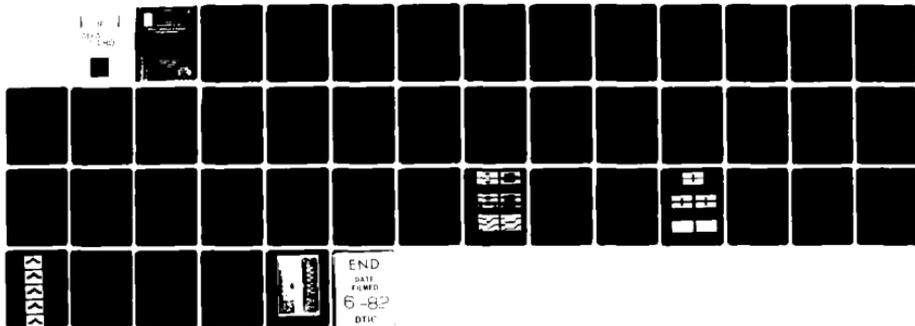
1981 L M DAVIES, E W SCOTT

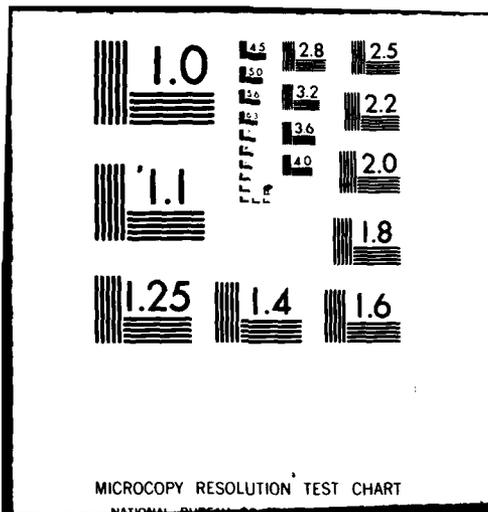
UNCLASSIFIED

RSRE-MEMO-3400

DRIC-BR-82754

NL





MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS-1963-A

AD A114802

ROYAL SIGNALS AND RADAR ESTABLISHMENT

Memorandum 3400

Title: A TRUE LOGARITHMIC IF AMPLIFIER FOR RADAR APPLICATIONS
Authors: L M Davies and E W Scott
Date:

SUMMARY

The availability of VX(M)9410 True Logarithmic IF amplifier stages as integrated circuits has enabled IF logarithmic amplifiers to be constructed by cascading stages with more than 60 dB's of dynamic range. True logarithmic amplifiers have an advantage over normal successive detection logarithmic amplifiers as the compression is achieved at Intermediate Frequency and not at Video Frequency thus preserving the phase information. Logarithmic amplifiers are required in many applications where phase and amplitude is of importance, examples are monopulse, MTI and ECM Radars. For multichannel receivers the requirement is to minimise phase shift through the logarithmic amplifier with change of signal level. This report describes measurements carried out on a number of true logarithmic amplifiers, and particular attention has been given to measurements of phase and amplitude tracking of amplifiers. The Constant False Alarm Rate (CFAR) properties have also been investigated.

This memorandum is for advance information. It is not necessarily to be regarded as a final or official statement by Procurement Executive, Ministry of Defence

Copyright
C
Controller HMSO London
1981



Accession For	
NTIS GRA&I	<input checked="" type="checkbox"/>
DTIC TAB	<input type="checkbox"/>
Unannounced	<input type="checkbox"/>
Justification	
By _____	
Distribution/ _____	
Availability Codes	
Dist	Avail and/or Special

A TRUE LOGARITHMIC IF AMPLIFIER FOR RADAR APPLICATIONS

L M Davies and E W Scott

LIST OF CONTENTS

- 1 Introduction
- 2 Measurement and Results of 6 Stage Logarithmic Amplifiers
- 3 Gain and Bandwidth Measurements of 6 Stage Log Amps
- 4 Dynamic Range Measurements of 6 Stage Log Amps
- 5 Measurement of Phase Response and Differential Phase Response of 6 Stage Log Amps
- 6 Measurement of Phase Characteristic of 6 Stage Log Amps on ANA at Room Temperature
- 7 Measurement of Phase Change of 6 Stage Log Amps on ANA with Constant Input Signal Level -30 dBm and with Temperature Changes of -50°C to +50°C
- 8 Measurement of Gain Change of 6 Stage Log Amps on ANA at Room Temperature
- 9 Measurement of Gain Change of 6 Stage Log Amps on ANA with Constant Input Signal -30 dBm, and with Temperature changes of -50°C to +50°C
- 10 Measurements and Results of 7 Stage Log Amps
- 11 Gain and Bandwidth Measurements of 7 Stage Log Amps
- 12 Dynamic Range Measurements of 7 Stage Log Amps
- 13 Measurement of Phase Response and Differential Phase Measurement of 7 Stage Log Amps
- 14 Measurements and Results of 8 Stage Log Amps
- 15 Gain and Bandwidth Measurements of 8 Stage Log Amps
- 16 Dynamic Range Measurements of 8 Stage Log Amps
- 17 Measurement of Phase Response of 8 Stage Log Amps
- 18 Pulse Response of 6 and 8 Stage Log Amplifiers
- 19 Circuit Diagram
- 20 Conclusions
- 21 Acknowledgements

Appendix A An Evaluation of the CFAR Properties of the VX(M)9410 True Logarithmic IF Amplifier

- A.1 Introduction
- A.2 Examination of Detector Diodes
- A.3 Dynamic Range Measurements of 6 Stage Log Amps with CW and Noise Input Signals
- A.4 Measurement of CFAR Characteristics of 6 Stage Log Amps with Noise Input Signals
- A.5 Measurement of CFAR Characteristics of 6 Stage Log Amps with Noise Input Signals on a Spectral Analyser
- A.6 Conclusion
- A.7 Reference

Appendix B

- B.1 Logarithmic Integrated Circuits
- B.2 Electrical Characteristics of VX(M)9410 Integrated Circuit
- B.3 Circuit Description of VX(M)9410 Integrated Circuit
- B.4 Circuit Description of 6 Stage Logarithmic Amplifier and Output Buffer Stage
- B.5 Acknowledgement

LIST OF FIGURES

- 1A Dynamic Range Measurements of 6 Stage Log Amps at 30 MHz. Detected O/P
- 1B Dynamic Range Measurements of 6 Stage Log Amps at 60 MHz. Detected O/P
- 1C Dynamic Range Measurement of 6 Stage Log Amp at 60 MHz. Peak to Peak Output at IF
- 2 Measurement of Phase Response and Differential Response of the 6 Stage Log Amp
- 3A Measurement of Phase Characteristic of 6 Stage Log Amps on ANA at Room Temperature Amp^r No 1
- 3B Measurement of Phase Characteristic of 6 Stage Log Amps on ANA at Room Temperature Amp^r No 2
- 4A Measurement of Phase Change of 6 Stage Log Amps on ANA with Constant Input Signal Level -30 dBm and with Temperature Changes -50°C to +50°C Amp^r No 1
- 4B Measurement of Phase Change of 6 Stage Log Amps on ANA with Constant Input Signal Level -30 dBm and with Temperature Changes -50°C to +50°C Amp^r No 2
- 5A Measurement of Gain Change of 6 Stage Log Amps on ANA at Room Temperature Amp^r No 1
- 5B Measurement of Gain Change of 6 Stage Log Amps on ANA at Room Temperature Amp^r No 2
- 6A Measurement of Gain Change of 6 Stage Log Amps on ANA with Constant Input Signal -30 dBm, and with Temperature Changes of -50°C to +50°C Amp^r No 1
- 6B Measurement of Gain Change of 6 Stage Log Amps on ANA with Constant Input Signal -30 dBm, and with Temperature Changes of -50°C to +50°C Amp^r No 2
- 7A Dynamic Range Measurements of 7 Stage Log Amps at 30 MHz
- 7B Dynamic Range Measurements of 7 Stage Log Amps at 60 MHz
- 8 Measurement of Phase Response and Differential Phase Measurement of 7 Stage Log Amps
- 9A Dynamic Range Measurements of 8 Stage Log Amps at 30 MHz
- 9B Dynamic Range Measurements of 8 Stage Log Amps at 60 MHz
- 10 Measurement of Phase Response and Differential Phase Measurement of 8 Stage Log Amps
- 11 Pulse Response of 6 Stage and 8 Stage Log Amps
- 12 Circuit Diagram

Appendix A

- A.1 CW Input v Output Response for AEI Diode DC1554 Measured at 60 MHz
- A.2 Pulse Response of 6 Stage Log Amps No 1 and 2
- A.3 60 MHz CW Input v DC Detected Output of Log Amps No 1 and 2
- A.4 Noise Input v DC Detected Output of Log Amps No 1 and 2
- A.5 Noise Input v RMS Detected Output of Log Amps No 1 and 2
- A.6 Spectrum of 6 Stage Log Amplifier and 4 MHz Bandwidth Filter when subjected to White Noise Input

Appendix B

- B.1 Dual Gain Stage Schematic
- B.2 Dual Gain Transfer Characteristic
- B.3a Cascaded Dual Gain Stage
- B.3b Transfer Characteristic
- B.3c Output Characteristic of the Log Amp^r
- B.4 Dual Gain Stage
- B.5 Circuit Diagram Dual Gain Stage
- B.6 Printed Circuit Board

1 INTRODUCTION

Under sponsorship of VX(M)9410, Constant Phase Wide Dynamic Range Amplifier, a True Logarithmic IF amplifier integrated circuit was developed by Plessey Research (Caswell) Limited funded by MOD (DCVD). Stage A samples (WXC106) have already been evaluated by the industrial sponsor, Plessey Radar Limited, who constructed experimental 6- and 8-stage amplifiers with a purpose-built 50 ohm output buffer. This report refers to further evaluation of 6-, 7- and 8-stage amplifiers at RSRE using VX(M)9410 Stage A samples. The amplifiers have been measured for dynamic range, and phase change with signal level. The 6 stage amplifiers have been tested over the temperature range -50°C to $+50^{\circ}\text{C}$ and the phase and amplitude tracking has been examined.

True logarithmic amplifiers have an advantage over the normal successive detection type logarithmic amplifiers as the compression is achieved at IF and not video thus preserving the phase information. True logarithmic amplifiers are required in many applications where phase, and amplitude is of importance. Examples are monopulse and MTI systems and for radar ECCM receivers.

For multichannel receivers the requirement is to minimise phase shift through the logarithmic amplifier with change of signal level at IF. Differential Phase and gain tracking have been examined on a pair of amplifiers.

2 MEASUREMENTS AND RESULTS OF 6 STAGE LOGARITHMIC AMPLIFIERS

Two 6 stage logarithmic amplifiers were constructed to enable a minimum dynamic range of 60 dB's to be achieved. These amplifiers were measured in the laboratory for Gain, Bandwidth and Dynamic range, and measurements were made on the Automatic Network Analyser to examine the gain and phase tracking characteristics with change of signal level and temperature.

3 GAIN AND BANDWIDTH MEASUREMENTS OF 6 STAGE LOG AMPS

Gain and Bandwidth measurements were carried out initially on the Polyskop at room temperature. For 6 stages at 10 dB/stage the expected gain of the Log-strip would be 60 dB's, but it was found necessary to attenuate the signal to the output buffer section to maintain amplitude and phase linearity resulting in an overall gain of 26 dB's.

4 DYNAMIC RANGE MEASUREMENTS OF 6 STAGE LOG AMPS

The dynamic range was measured at 30 MHz and 60 MHz with CW signal inputs and results are attached as Figs 1A and 1B. The slopes were set up for 0.5 volt output at 0 dBm input and the curves are displaced for clarity. It can be seen that greater than 60 dB's of dynamic range was achieved over an input signal level of -65 dBm to 0 dBm to an accuracy of < 2 dB. The above graphs were measured after a Siverts Detector Type PM 7520 for ease of measurement. The CW IF input v PK to PK IF output was examined for a 6 stage logarithmic amplifier and the same dynamic range was achieved see Fig 1C.

5 MEASUREMENT OF PHASE RESPONSE AND DIFFERENTIAL PHASE RESPONSE OF THE 6 STAGE LOG AMPS

Measurements of Phase v Signal level were carried out in the laboratory at 30 MHz and 60 MHz with a Hewlett Packard Vector Voltmeter Model 8405A. Change of Phase v Signal level was measured over the range -60 dBm to 0 dBm ie over the logarithmic dynamic range of the receiver. Results are attached in Fig 2 and amplifiers 1 and 2 exhibited a phase change of 4° at 30 MHz and

6.5° at 60 MHz. Amplifiers 1 and 2 were used to measure differential Phase and Signal level at 30 MHz and 60 MHz and results are attached in Fig 2 and it can be seen that they maintain < 1° at 30 MHz and < 1.5° at 60 MHz over the dynamic range -60 to 0 dBm.

6 MEASUREMENT OF PHASE CHARACTERISTIC OF 6 STAGE LOG AMPS ON ANA AT ROOM TEMPERATURE

The phase characteristic of amplifiers No 1 and 2 were examined on the Automatic Network Analyser over the frequency range 45 to 100 MHz and with input signal levels of -50 dBm to -10 dBm. Results are attached as Figs 3A and 3B. Similar results were obtained from both amplifiers and the phase change was < 5° over the signal range but the tracking was < 2°.

7 MEASUREMENT OF PHASE CHANGE OF 6 STAGE LOG AMPS ON ANA WITH CONSTANT INPUT SIGNAL LEVEL -30 dBm AND WITH TEMPERATURE CHANGES OF -50°C TO +50°C

The phase characteristics of amplifiers No 1 and 2 were examined on ANA over the frequency range 45 to 100 MHz from -50°C to +50°C with an input level signal constant at -30 dBm. Results are attached as Figs 4A and 4B, and it can be seen that there is a steady change of phase with change of temperature of approximately 40° with a fixed input level of -30 dBm for both amplifiers. The phase tracking was within 8°.

8 MEASUREMENT OF GAIN CHANGE OF 6 STAGE LOG AMPS ON ANA AT ROOM TEMPERATURE

The gain characteristics of amplifiers No 1 and 2 were examined on ANA over the frequency range 45 to 100 MHz and with input signal levels -50 dBm to -10 dBm. Results are attached as Figs 5A and 5B. Identical results are achieved on both amplifiers.

9 MEASUREMENT OF GAIN CHANGE OF 6 STAGE LOG AMPS ON ANA WITH CONSTANT INPUT SIGNAL -30 dBm, AND WITH TEMPERATURE CHANGES OF -50°C TO +50°C

The gain characteristics of amplifiers No 1 and 2 were examined on ANA over the frequency range 45 to 100 MHz from -50°C to +50°C with an input level constant at -30 dBm. Results are attached as Figs 6A and 6B. At 60 MHz there is a steady change of gain of 2 dB, and tracking is within 0.5 dB.

10 MEASUREMENTS, AND RESULTS OF 7 STAGE LOG AMPS

Three 7 stage log amps were constructed to enable a minimum Dynamic Range of 70 dB's to be achieved. These amplifiers were measured in the laboratory for Gain, Bandwidth and Dynamic Range. Measurements were also carried out in the laboratory of the phase response over the dynamic range of the amplifier at 30 MHz and 60 MHz.

11 GAIN, AND BANDWIDTH MEASUREMENTS OF 7 STAGE LOG AMPS

Gain and bandwidth measurements were carried out in the laboratory at room temperature. For 7 Stages at 10 dB/stage the expected gain would be 70 dB's but it was found necessary to attenuate the drive signal to the buffer output stage to maintain amplitude and phase linearity resulting in an overall gain of 27 dB's.

12 DYNAMIC RANGE MEASUREMENTS OF 7 STAGE LOG AMPS

The dynamic range was measured at 30 MHz and 60 MHz with CW signal inputs, and results are attached as Figs 7A and 7B. The slopes were set up for 0.5 volt output at 0 dBm input, and the curves are displaced for clarity. It can be seen that greater than 70 dB's of dynamic range was achieved over an input signal level of -70 dBm to 0 dBm to an accuracy of 3 dB. The above curves were measured after a detector for ease of measurement.

13 MEASUREMENT OF PHASE RESPONSE AND DIFFERENTIAL PHASE MEASUREMENT OF 7 STAGE LOG AMPS

Measurements of Phase v Signal level were carried out in the laboratory at 30 MHz and 60 MHz with a Hewlett Packard Vector Voltmeter Model 8405A. Change of Phase v Signal level was measured over the dynamic range -60 dBm to 0 dBm ie over the limits of the Vector Voltmeter. Results are attached in Fig 8. Amplifiers 1, 2 and 3 exhibited a phase change of $< 4^\circ$ at 30 MHz and $< 7^\circ$ at 60 MHz.

Amplifiers 1 and 2 were used to measure differential Phase v Signal level at 30 MHz and 60 MHz and results are attached on Fig 8, and it can be seen that they maintain $< 0.5^\circ$ at 30 MHz and $< 1^\circ$ at 60 MHz over the dynamic range -60 dBm to 0 dBm.

14 MEASUREMENTS AND RESULTS OF 8 STAGE LOG AMPS

Three 8 stage log amps were constructed to enable > 70 dB's of dynamic range to be achieved. These amplifiers were measured in the laboratory for gain, bandwidth and dynamic range. Measurements were also carried out in the laboratory of the phase response over the dynamic range of the amplifier at 30 MHz and 60 MHz.

15 GAIN AND BANDWIDTH MEASUREMENTS OF 8 STAGE LOG AMPS

Gain and bandwidth measurements were carried out in the laboratory at room temperature. For 8 stages at 10 dB/stage the expected gain would be 80 dB's but it was found necessary to attenuate the drive signal to the buffer output stage to maintain amplitude and phase linearity resulting in an overall gain of 27 dB's.

16 DYNAMIC RANGE MEASUREMENTS OF 8 STAGE LOG AMPS

The dynamic range was measured at 30 MHz, and 60 MHz with CW signal inputs and results are attached as Figs 9A and 9B. The slopes were set up for 0.5 volt output at 0 dBm input and the curves are displaced for clarity. It can be seen that greater than 70 dB's of dynamic range was achieved over a range of -75 dBm to 0 dBm but that the amplifiers are approaching saturation at -5 dBm.

Experiments were conducted to include a bandpass filter in the cascaded amplifier chain to reduce the wideband noise from saturating the last stage but this had little effect, and the major effect of cascading 8 stages seems to be the bandwidth reduction factor in cascading stages.

17 MEASUREMENTS OF PHASE RESPONSE OF 8 STAGE LOG AMPS

Measurements of Phase v Signal level were carried out in the laboratory at 30 MHz and 60 MHz with a Hewlett Packard Vector Voltmeter Model 8405A.

Change of Phase v Signal level were measured over the dynamic range -60 to 0 dBm ie over the limits of the Vector Voltmeter. Results are attached in Fig 10. Amplifiers 1, 2 and 3 exhibited a phase change of $< 5.5^\circ$ at 30 MHz and $< 11^\circ$ at 60 MHz.

Amplifiers 2 and 3 were used to measure differential Phase v Signal level at 30 MHz and 60 MHz and results are attached in Fig 10 and it can be seen that they maintain $< 1^\circ$ at 30 MHz and $< 1^\circ$ at 60 MHz over the dynamic range -60 dBm to 0 dBm.

18 PULSE RESPONSE OF 6 AND 8 STAGE LOG AMPLIFIERS

A 1 μ Sec and 10 μ Sec pulse was examined before and after a 6 and 8 Stage log amp. A Hewlett Packard PIN attenuator was used to obtain a good 80 dB on/off ratio at the input to a receiver system and results are given in Fig 11. The pulses were measured on a Tektronix Wideband oscilloscope. The top picture illustrates the input pulses to the 6 and 8 stage log amps and the next photograph down illustrates the output pulse of the 6 stage and 8 stage log amplifier. The bottom picture shows the detected video responses after a Sivers Detector Type PM 7520. The peak of the response is detected, but the back edge of the pulse is stretched.

19 CIRCUIT DIAGRAM

A circuit diagram of the logarithmic amplifier is attached as Fig 12 and it will be observed that the 6th stage is driven harder than the first 5 stages and this is also the case for the 7th and 8th stages where applicable.

On the 6 stage amplifier +9 v supply was used, but on the 7 and 8 stage amplifier a +12 v supply was preferred to enable the later stages to be driven harder.

20 CONCLUSIONS

Stage A samples of the VX(M)9410 (WXC106) circuits have been evaluated at RSRE in prototype 6, 7 and 8 stage logarithmic amplifiers with a 50 ohm buffer output stage. These circuits were designed to operate at 60 or 70 MHz and appear to meet the target specification for gain, phase shift and dynamic range. The 6 stage log amps gave at least 60 dB's of dynamic range to an accuracy of 2 dB and good phase and gain tracking results were obtained with change of signal level at room temperature and also with a change of temperature and fixed input signal level.

The 7 stage log amps gave at least 70 dB's of dynamic range to an accuracy of 3 dB and good phase and gain tracking results were obtained with change of signal level at room temperature and also with change of temperature and fixed input signal level.

The 8 stage log amps did not yield any increase in dynamic range over the 7 stage version. The amplifiers tended to saturate at -5 dBm CW Input signal level. An experiment was conducted to minimise the noise content from saturating the last stage by using a bandpass filter in the cascaded amplifier circuits, but this did not yield any improvement in dynamic range. We think that the lack of improvement is due to the bandwidth reduction factor, and also due to the fall off in frequency response of the cascaded amplifiers which is evident even on the 6 stage log amplifiers.

Good differential tracking of phase was measured on amplifier pairs at 30 and 60 MHz for 6, 7 and 8 stage amplifiers.

The IF pulse response was good for the 6 and 8 stage amplifiers.

Evaluation of the latest VX(M)9410 Stage A samples has shown improved performance with respect to dynamic range than that achieved on earlier devices. With the earlier device, on which the Plessey Semiconductors' product - SL 531 - is based, little improvement in dynamic range occurred when the strip was extended from 6 to 7 devices. With the latest device, a definite improvement in dynamic range occurs when the strip is increased from 6 to 7 devices but little improvement occurs in going from 7 to 8 devices.

The output buffer stage will be redesigned to have better signal handling capability.

21 ACKNOWLEDGEMENTS

The authors would like to thank Mr G Parkes for measurements on the Hewlett Packard Automatic Network Analyser.

APPENDIX A

AN EVALUATION OF THE CFAR PROPERTIES OF THE VX(M)9410 TRUE LOGARITHMIC IF AMPLIFIER

A.1 INTRODUCTION

The True Logarithmic amplifier has been evaluated for CW and pulsed CW conditions; a characteristic very close to the desired logarithmic law was achieved at IF and also when a detected output was measured. Further tests have been carried out using high level noise signals to examine the Constant False Alarm Rate (CFAR). An ideal logarithmic amplifier when subjected to thermal noise at its input has a video output whose standard deviation is independent of input noise level, and whose mean value is proportional to the logarithm of the input noise level.

A.2 EXAMINATION OF DETECTOR DIODES

RSRE examined a number of commercial detector diodes for use at the output of a 6 stage logarithmic amplifier. The response to CW and pulsed CW was examined for dynamic range and also to obtain the best rise and fall times on pulses.

Fig A.1 shows the input v output response for an AEI Zero Bias Detector Diode Type DC 1554 which is mounted in a Sivvers Lab PM 7520 coaxial mount. Fig A.2 shows the pulse responses of two 6 stage logarithmic amplifiers designated Serial No 1 and 2. The top picture shows an input pulse at -20 dBm and is 2 μ S wide. This pulse is obtained at RF with a Hewlett Packard Signal Generator and PIN modulator giving a good 80 dB on/off ratio which is essential for examining the pulse response of logarithmic amplifiers to avoid CW break through. This RF pulse is fed via a low noise RF amplifier to an RF mixer and head amplifier which down converts to 60 MHz. This signal is then fed via a 4 MHz bandwidth filter and an IF attenuator to the logarithmic amplifier under test. Power level measurements are made immediately before the logarithmic amplifier with a power meter.

The next two pulses on Fig 2 show the output pulse at 60 MHz of log amp No 1 and 2. The bottom two pictures show the detected output pulse of log amp No 1 and No 2. Good pulse rise times may be observed and the trailing edge shows the delayed response which is typical of logarithmic amplifiers.

A.3 DYNAMIC RANGE MEASUREMENTS OF 6 STAGE LOGARITHMIC AMPLIFIERS WITH CW AND NOISE INPUT SIGNALS

Fig A.3 shows the response of log amps No 1 and 2 with 60 MHz CW input signal level v detected output. Similar results were obtained on both amplifiers and the results are displaced for clarity.

Fig A.4 shows the response of log amps No 1 and 2 with noise input signals v detected output.

Similar results were obtained on both amplifiers and the results are almost identical to Fig A.3, which is the expected result.

A.4 MEASUREMENT OF CFAR CHARACTERISTICS OF 6 STAGE LOGARITHMIC AMPLIFIERS WITH NOISE INPUT SIGNALS

Fig A.5 shows the response of log amps No 1 and 2 with 60 MHz white noise input signal level v detected output. Similar results are obtained on both amplifiers. The detected output signal was connected to a Hewlett Packard 3400A RMS meter via a 4 μ F capacitor to isolate the DC component of the response.

It will be observed that the AC RMS component of the noise increases until the normal operating point 20 dB up the logarithmic curve is reached at -50 dBm. This is the part of the characteristic that changes from a linear to a log Rayleigh distribution. Thereafter the RMS variation on log amplifier No 1 and No 2 is 2.5 dB's.

A.5 MEASUREMENT OF CFAR CHARACTERISTICS OF 6 STAGE LOG AMPS WITH NOISE INPUT SIGNALS ON A SPECTRUM ANALYSER

The same arrangement as in para 4 was used to check the spectrum measurements at the IF output of the log amplifier at 60 MHz. The noise input signal was fed via a 4 MHz bandpass filter, and an IF attenuator to the log amplifier under test. Power level measurements were made immediately before the log amplifier with a power meter. The output spectrum of the log amplifier was measured on a Hewlett Packard Spectrum Analyser 8552A/8553L. The spectrum analyser was used in the logarithmic mode so that the Y display represents 10 dB/cm and the scan width was set at 5 MHz/cm. The white noise input power was 0 dBm to the logarithmic amplifier for zero attenuation. Photographs of the spectra were recorded over the range 0 dBm to -40 dBm in 10 dB steps, see Fig A.5. The centre of the display is set at 60 MHz, and over the above signal input range the spectrum level was constant to less than 3 dB, and there was no notifiable change in the spectrum width. Beyond this signal range the spectrum level and width changes as the amplifier is operating on the linear part of the output characteristic.

The response of logarithmic amplifier to noise signals has been examined previously at RSRE¹, and thus established that there was no change in the amplitude when good CFAR is achieved. The observed constancy of the output spectrum confirms the good quality of the CFAR performance measured in para 4 after the detector diode.

A.6 CONCLUSIONS

There are radar applications where the CFAR performance of the amplitude characteristic is of importance as well as the phase characteristic. The True Logarithmic amplifier combines both these qualities and has advantages over the successive detection logarithmic amplifier.

A.7 REFERENCE

- 1 RSRE Memo 2727 'The Response of Logarithmic Amplifiers to Noise Signals' L M Davies and E W Scott.

APPENDIX B

B.1 LOGARITHMIC INTEGRATED CIRCUITS

The VX(M)9410 true logarithmic amplifier is a broadband amplifier designed in silicon microcircuit form and mounted in a TO5 package.

Receiver systems require a wide dynamic range of input signals but signals close to noise require large gain whereas large input signals would be severely distorted if this gain were used. Typical radar and ECM receivers have to process signals that consist of short pulses with random heights and times of arrival. In such systems AGC loops are only of restricted use and limiting amplifiers eliminate pulse height information.

In a typical logarithmic amplifier an input dynamic range of 70 to 80 dB's is compressed by log action to an output range of about 20 dB's. In the past these requirements have been met with 'Successive Detection Amplifiers' but the disadvantage of this processing is that Phase Information on the IF signal is lost. True logarithmic amplifiers apply the log function to the IF signal, and preserve Phase Information. For MTI radar systems, where it is required to detect moving targets the phase information is important hence the logarithmic output must be at Intermediate Frequency. In order to preserve the phase information the phase shift or delay through the log amplifier should not vary more than a few degrees over the dynamic range of input signal level.

The method used to obtain a true logarithmic function at IF frequencies is to cascade amplifiers consisting of dual gain stages. Each stage consists of a limiting amplifier with Gain A in parallel with a unity gain amplifier the outputs of which are summed as shown in Fig B.1 which gives the soft limiting function shown in Fig B.2. For small input signals the gain is around 10 dB and this drops to unity when the input signal exceeds a certain value. A practical circuit will not have a function of two straight lines but will curve between the two sections, and this helps to reduce the ripple in the log characteristic when stages are cascaded.

Cascading N identical stages will give the type of transfer characteristic shown in Fig B.3b this consists of a series of straight lines with break points where each limiting amplifier limits.

Considering an N stage amplifier using dual gain stages with the mth stage just limiting then we can obtain the locus of the break points.

For a single stage - not limiting:

$$V_o = (A + 1)V_{in} \quad (B.1)$$

where A = small signal gain of limiting amplifier. When limiting the output is given by:

$$V_o = V_L + V_{in} \quad (B.2)$$

$$V_L = \text{limiting voltage}$$

At the point of just limiting

$$V_{in} = \frac{V_L}{A}$$

$$\therefore V_o = V_L \left[1 + \frac{1}{A} \right]$$

This is of course the output of the m^{th} stage in the N stage amplifier under consideration.

$$\therefore V_{o_m} = V_L \left(1 + \frac{1}{A} \right) \quad (\text{B.3})$$

This signal now passes through a further $(N - m)$ stages to the output each of which are limiting hence Equation B.2 applies to each stage.

$$\begin{aligned} \therefore V_o &= (N - m)V_L + \left(1 + \frac{1}{A} \right) V_L \\ V_o &= \left[N + \frac{1}{A} - (m - 1) \right] V_L \end{aligned} \quad (\text{B.4})$$

It is now necessary to eliminate m from this expression. At the input to the m^{th} stage which is just limiting

$$V_{in_m} = \frac{V_L}{A}$$

This signal has been amplified linearly by $(m - 1)$ stages

$$\begin{aligned} \therefore \frac{V_L}{A} &= V_{in} (A + 1)^{m-1} \\ \therefore m - 1 &= \log_{A+1} \left[\frac{V_L}{AV_{in}} \right] \end{aligned} \quad (\text{B.5})$$

Substitute (B.5) into (B.4)

$$V_o = \left\{ N + \frac{1}{A} - \log_{A+1} \left[\frac{V_L}{AV_{in}} \right] \right\} V_L$$

which can be rearranged to give

$$V_o = \left\{ N + \frac{1}{A} + \log_{A+1} \left[\frac{AV_{in}}{V_L} \right] \right\} V_L$$

The breakpoints in Figure B.3b all lie on the logarithmic curve given by the above expression. The dynamic range is $(A + 1)^N$. It will be noticed from Figure B.3b that there is an error due to the straight line approximation which is dependent on small signal gain $(A + 1)$ of the dual gain stage. This is

more obvious in Figure B.3c which shows the output of the log amplifier versus the log of the input level, the slope of which is

$$\frac{V_L}{20 \log (A + 1)} \quad \text{v/dB} \quad .$$

The output is now shown as a series of ripples. The maximum log error referred to the input is also shown in Figure B.3c; note that this error is independent of the number of amplifier stages in limiting. Computer analysis was used to simulate cascaded ideal dual gain stages. This simulation demonstrated that in order to obtain a log amplifier with an accuracy of ± 1 dB a total dual gain stage gain of 10 dB is required, ie $A + 1 = 3.16$. Figure B.3c also demonstrates that for a good logarithmic characteristic it is essential that A and V_L are well matched between stages; furthermore, the unity gain must be accurately defined.

B.2 ELECTRICAL CHARACTERISTICS OF THE VX(M)9410 INTEGRATED CIRCUIT

Test conditions unless otherwise stated
 Frequency 60 MHz
 Supply Voltage 9 volts
 Temperature (ambient) 25°C

Characteristic	Value		Units	Conditions
	Min	Max		
Small signal gain	8	12	dB	$V_{in} = -40$ dBm
High level gain	-0.5	+0.5	dB	$V_{in} = 0$ dBm
Upper cut off frequency	250	-	MHz	$V_{in} = -40$ dBm
Lower cut off frequency	-	10	MHz	$V_{in} = -40$ dBm
Supply current	-	25	mA	
Phase variation	-	± 2.5	degrees	$V_{in} = -60 \rightarrow +10$ dBm
Limited output	100	125	mV	
Input impedance	2.5 pF in parallel with 1 K Ω			
Output impedance	1.5 Ω in series with 25 nH			
Max input signal		+13	dBm	

B.3 CIRCUIT DESCRIPTION OF INTEGRATED CIRCUIT VX(M)9410

A dual gain stage can be realised by using two emitter coupled pairs driving a common load as shown in Fig B.4. The unity gain stage uses resistors R_E to define the unity gain. The ratio of I_2 to I_1 depends on the number of stages to achieve the required dynamic range. For 80 dB's of dynamic range 8 stages are required, and hence $I_2 = 8I_1$.

A good phase response is achieved by matching the phase shift through the limiter and unity gain stage, and the limiter should exhibit minimal phase change as it goes into limiting. Fig B.5 shows a complete circuit for a dual gain stage and circuit design requirements were that the limiting transistors should have a high F_T and a low base resistance $r_{bb'}$. Wide bandwidth is required to allow for the bandwidth reduction that occurs when stages are cascaded. In the circuit T_1 and T_2 are composite transistors forming the two long tailed pairs with T_3 and T_4 providing current sources for the limiting amplifier and the unity gain stage respectively. The output stage is a simple emitter follower. For normal operation the bias on R8 is connected to the internal line. Internal decoupling capacitors are used and R_{11} and C_2 provide a low pass filter on the supply line. This internal decoupling minimises the number of external components required to produce a multistage logarithmic amplifier only small coupling capacitors being required between stages.

B.4 CIRCUIT DESCRIPTION OF THE 6 STAGE LOGARITHMIC AMPLIFIER AND OUTPUT BUFFER STAGE

The VX(M)9410 integrated circuits are cascaded on a printed circuit board having a ground plane on the upper side, and circuit connections on the lower side. All components and integrated circuits are mounted on the ground plane of the PCB with leads passing through clearance holes in the PCB. Plated through holes have been used to provide the shortest DC path to earth.

A two stage buffer amplifier is used to match the high output impedance of the VX(M)9410 to a 50 ohm output. This buffer amplifier consists of an emitter follower driving a common base output stage. This circuit was designed by Plessey Radar to have good stability, a good phase characteristic and, to isolate the previous stages from variations in load impedance. The circuit diagram of the logarithmic amplifier which consists of 6 cascaded VX(M)9410 integrated circuits and a buffer output stage is shown in Fig 12 of the main report. The circuit connections on the printed circuit board and the component layout on the earth side of the printed circuit board are attached as Fig B.6.

B.5 ACKNOWLEDGEMENT

We would like to thank Mr W L Barber and Mr E R Brown, Plessey Research Caswell, for their contribution towards this appendix.

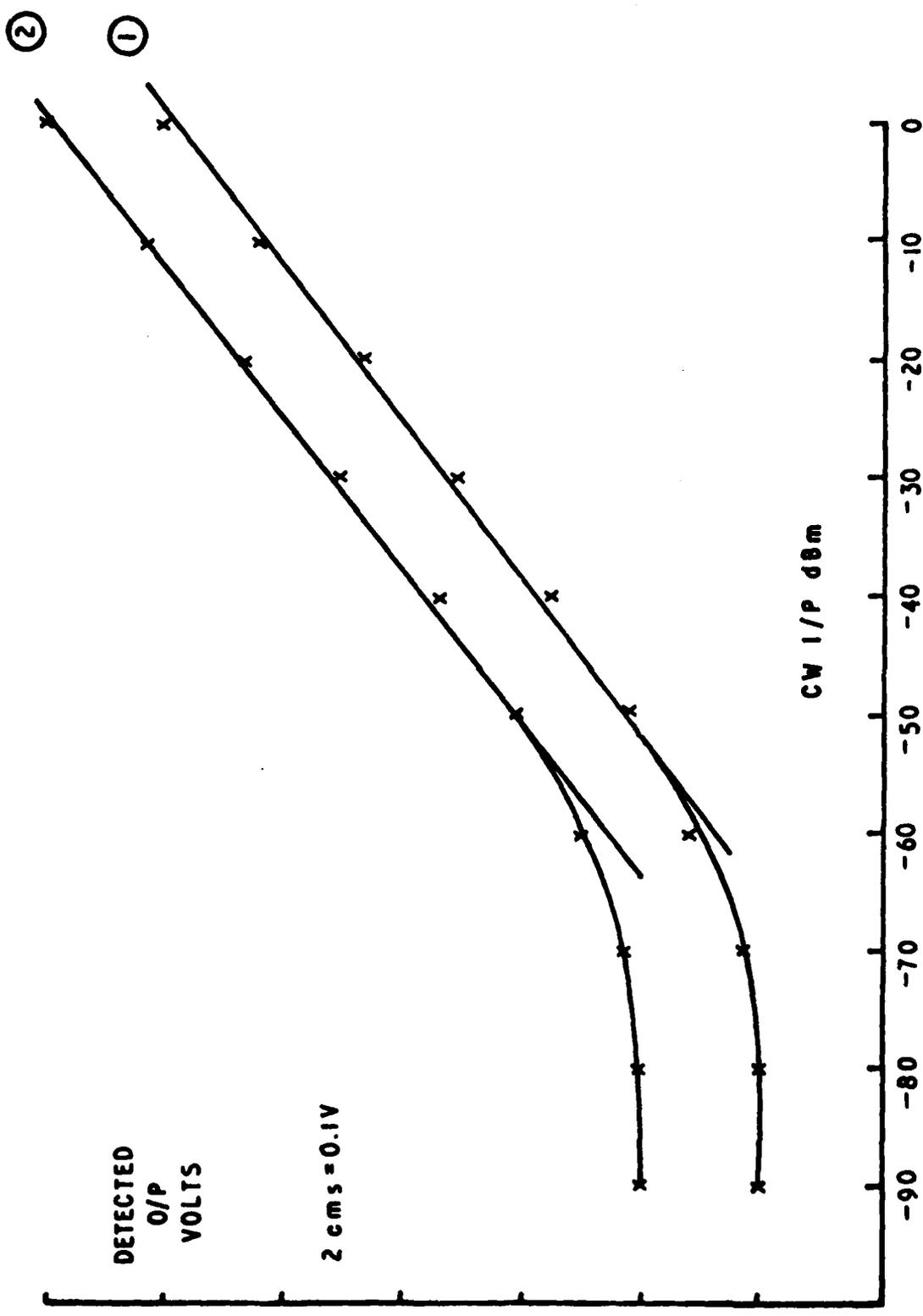


FIG. 1A DYNAMIC RANGE OF 6 STAGE LOG AMPS. AT 30 MHz I/P AMPRS. No. 1 AND No. 2
DET. O/P

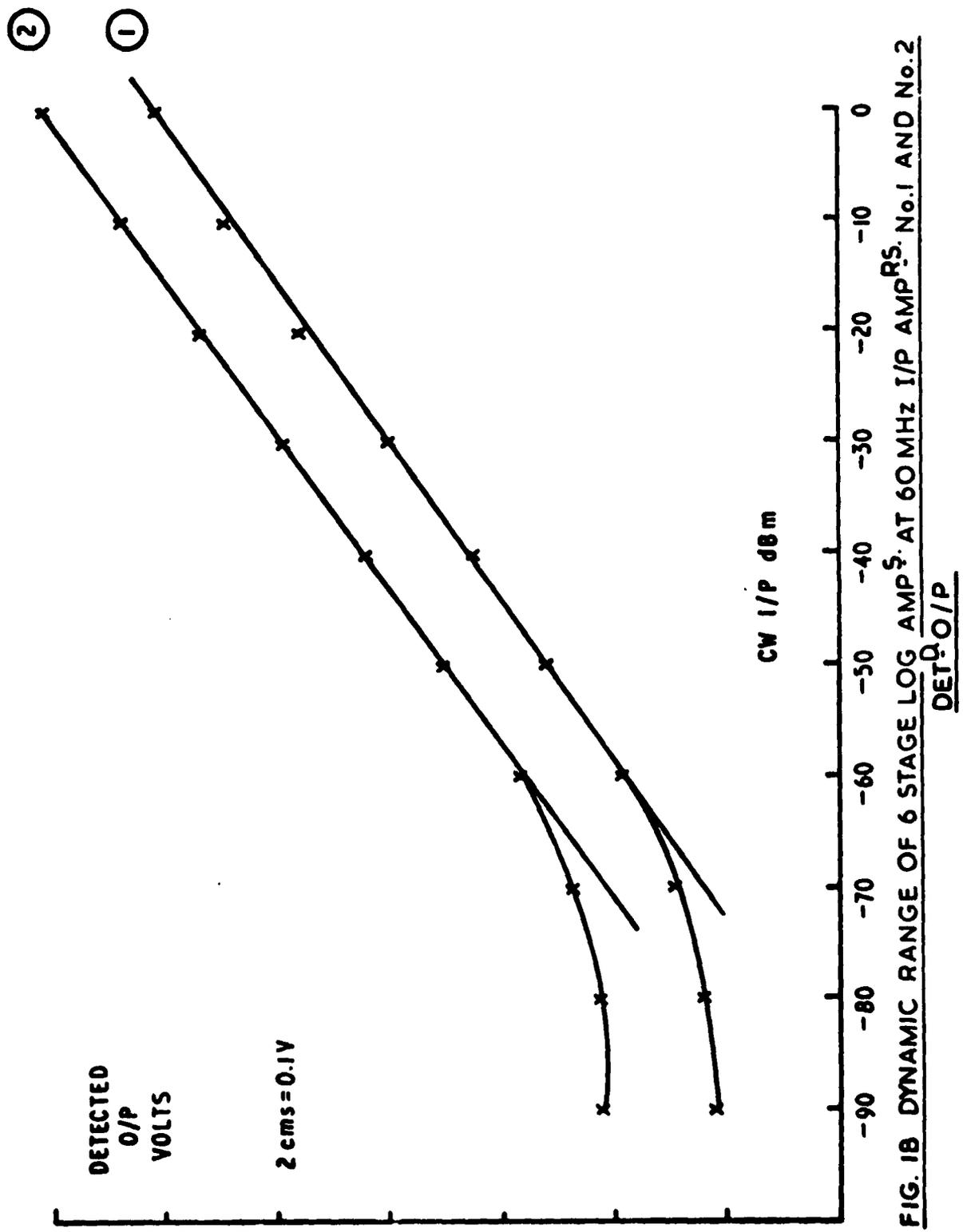


FIG. 1B DYNAMIC RANGE OF 6 STAGE LOG AMP'S AT 60 MHz I/P AMP'S. No.1 AND No.2

DET. O/P

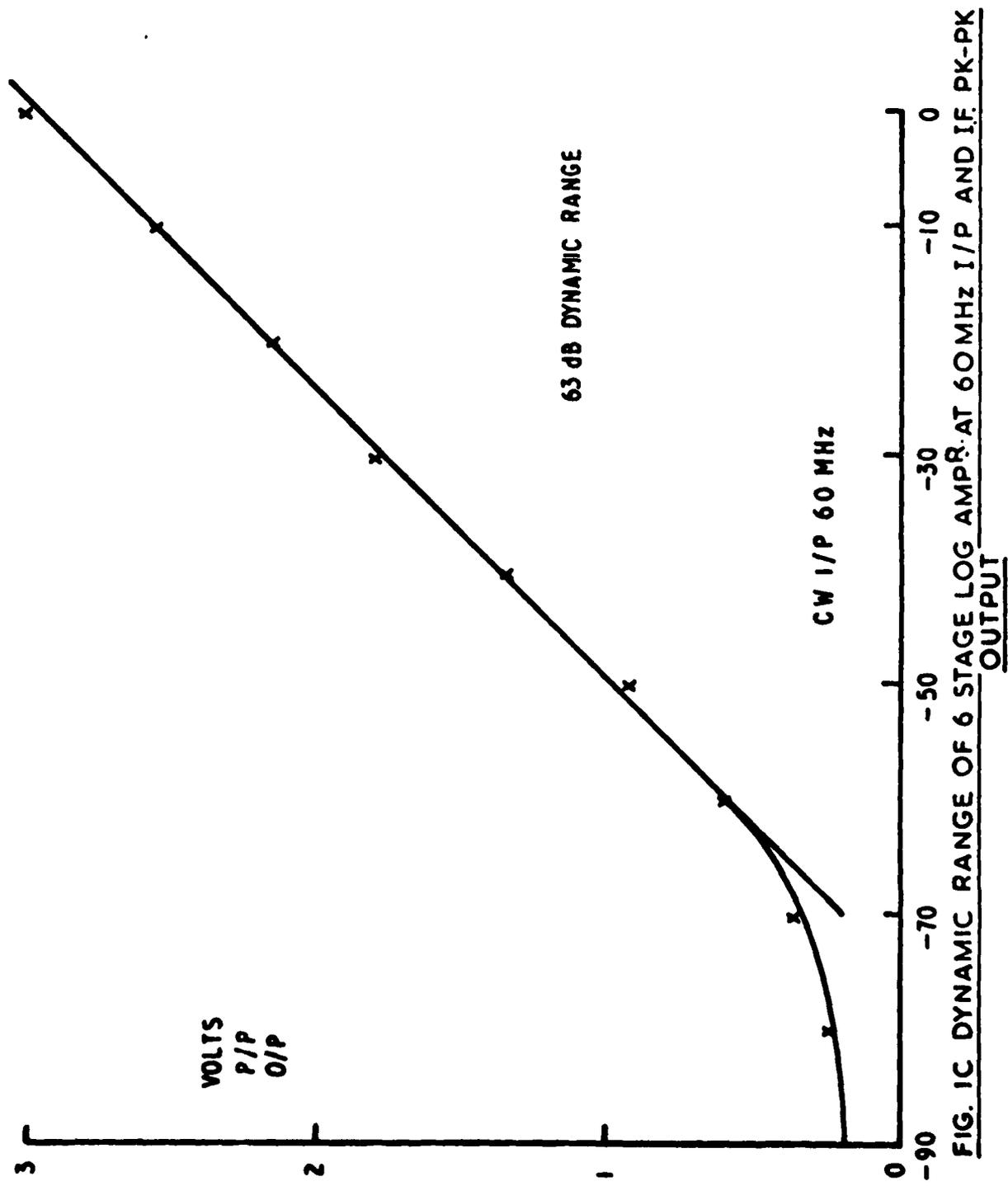


FIG. 1C DYNAMIC RANGE OF 6 STAGE LOG AMPR. AT 60MHZ I/P AND I.F. PK-PK OUTPUT

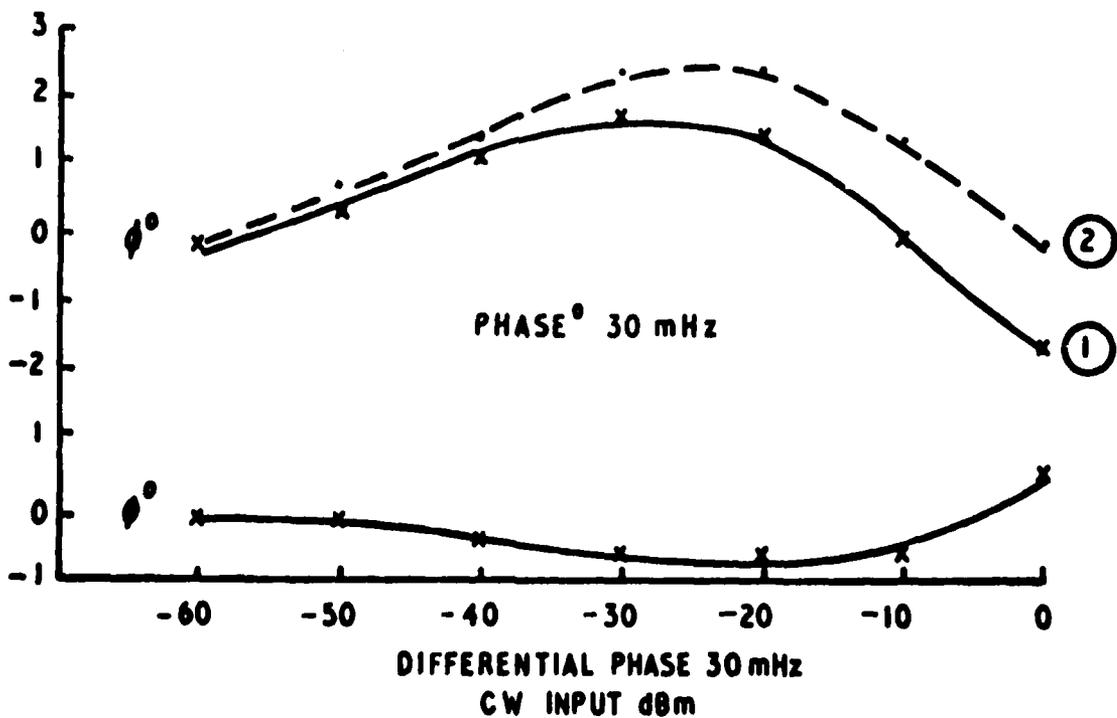
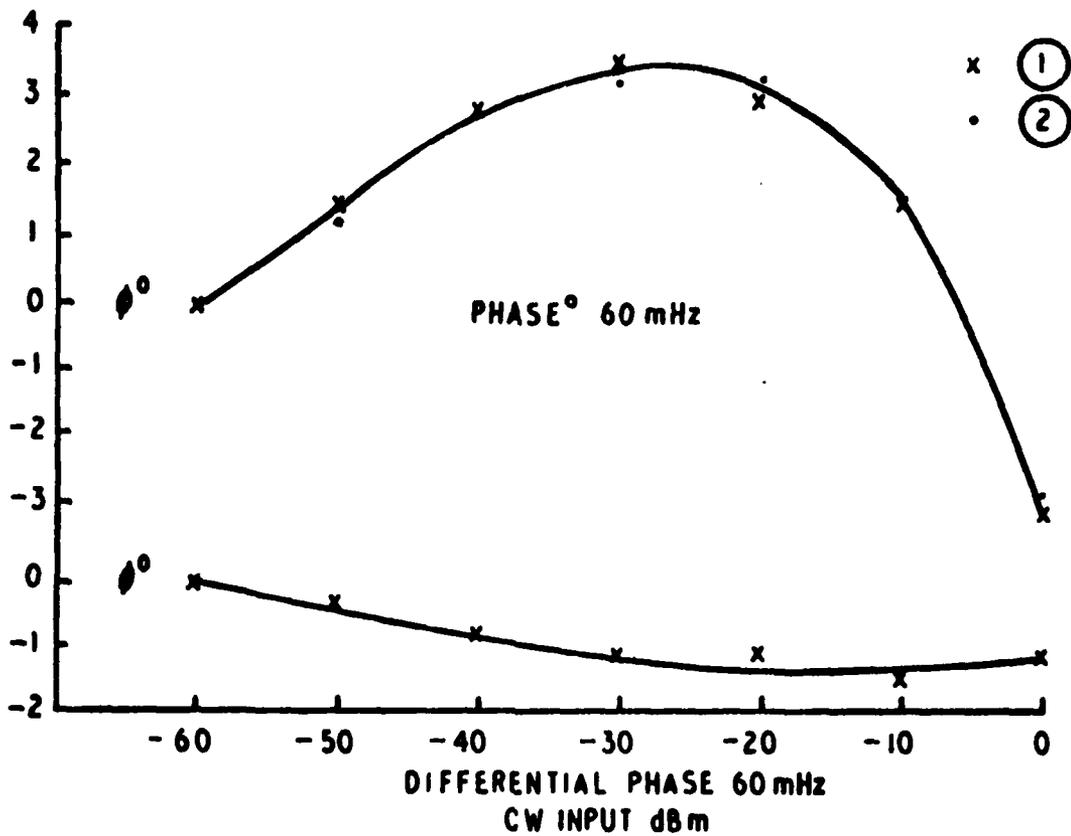


FIG. 2 6 STAGE AMP^R SERIES Nos. 1 AND 2

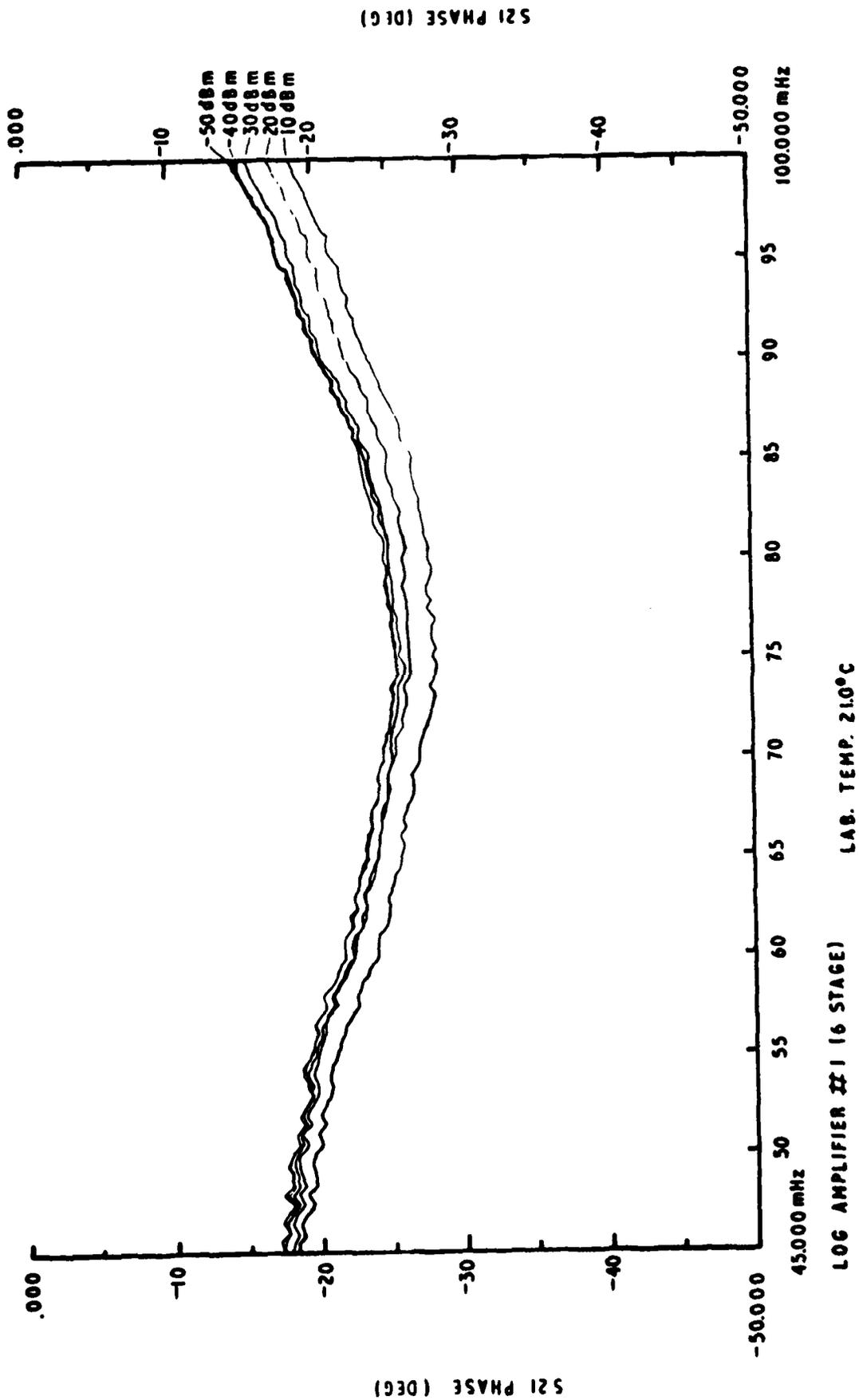
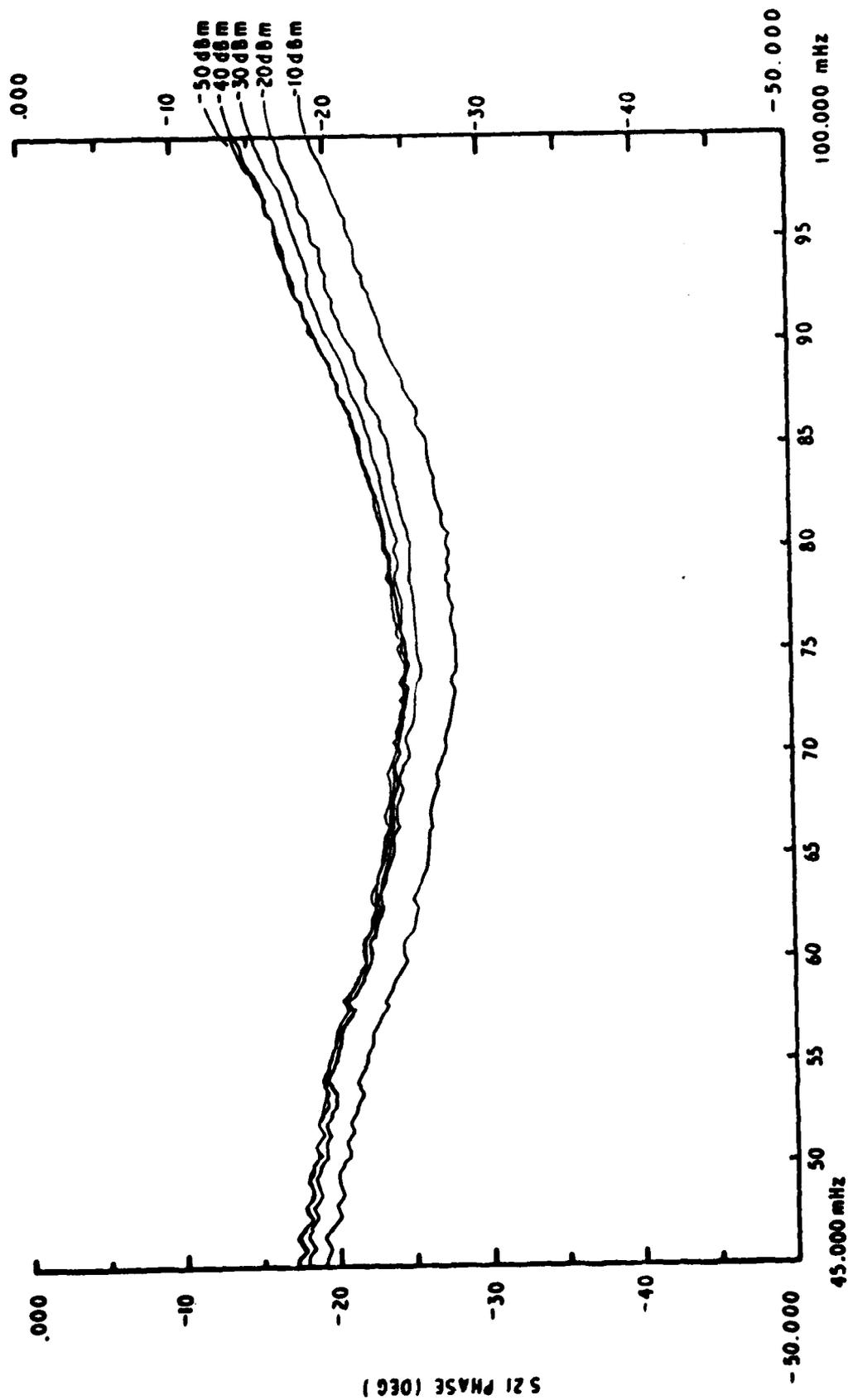


FIG. 3A MEASUREMENT OF PHASE CH^C v SIGNAL LEVEL CONSTANT TEMP^R.



LOG AMPLIFIER #2 (6 STAGE)

LAB. TEMP. 21.0 DEG. C

FIG. 3B MEASUREMENT OF PHASE CH^C v SIGNAL LEVEL CONSTANT TEMP.

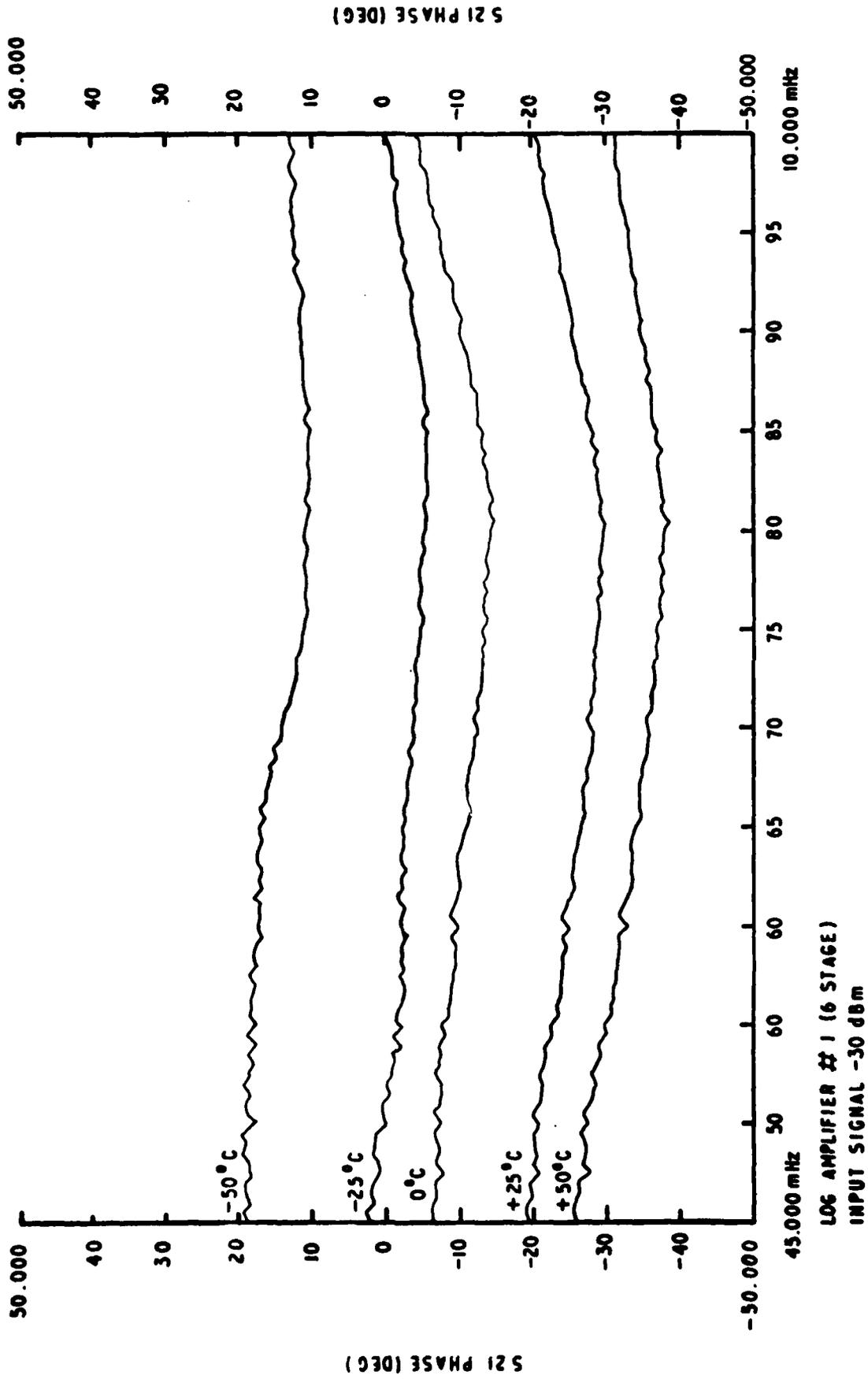


FIG. 4A MEASUREMENT OF PHASE CHANGE v TEMP^R. CONSTANT I/P SIGNAL

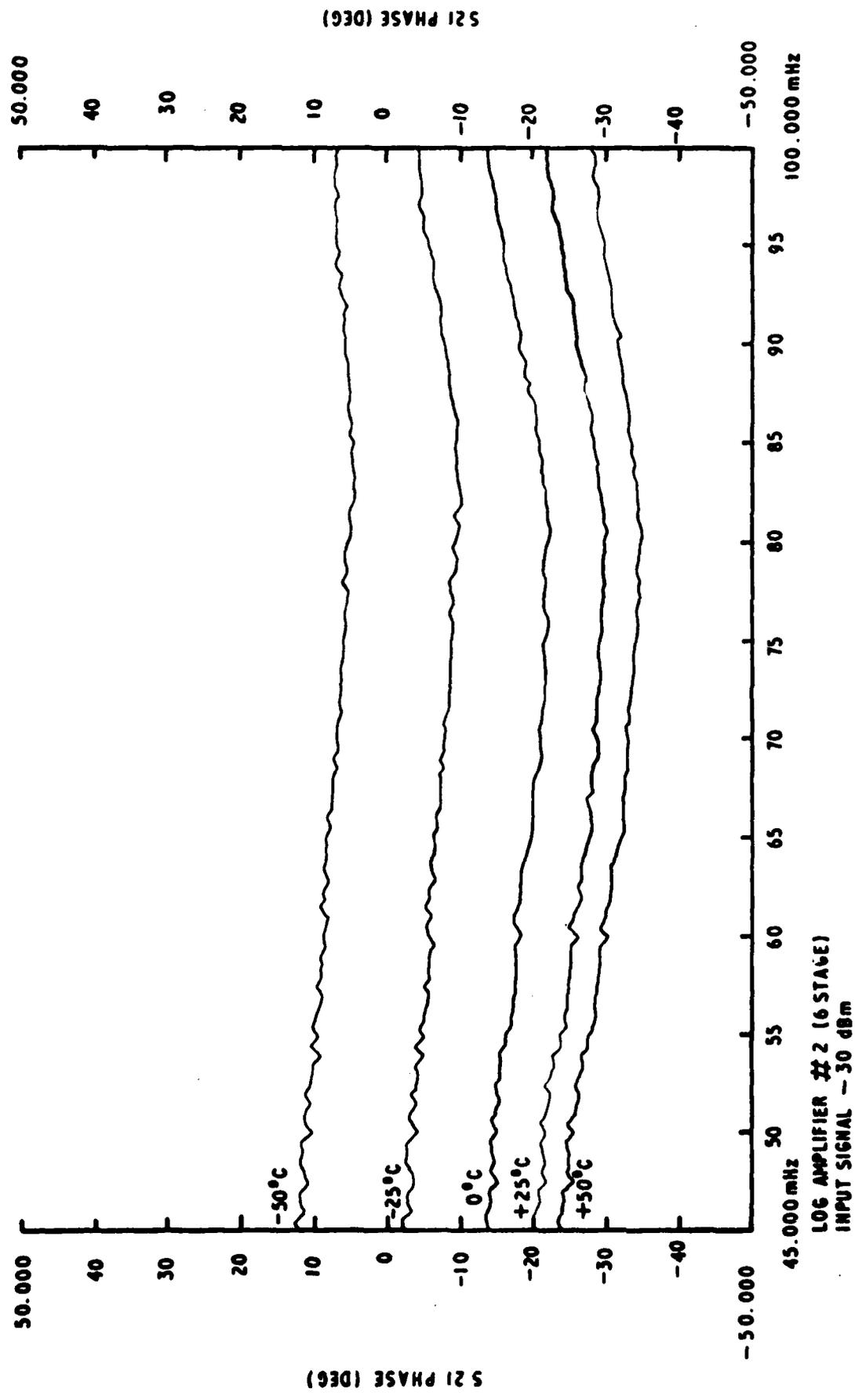


FIG. 45 MEASURE OF PHASE CHANGE v TEMP. CONSTANT I/P SIGNAL

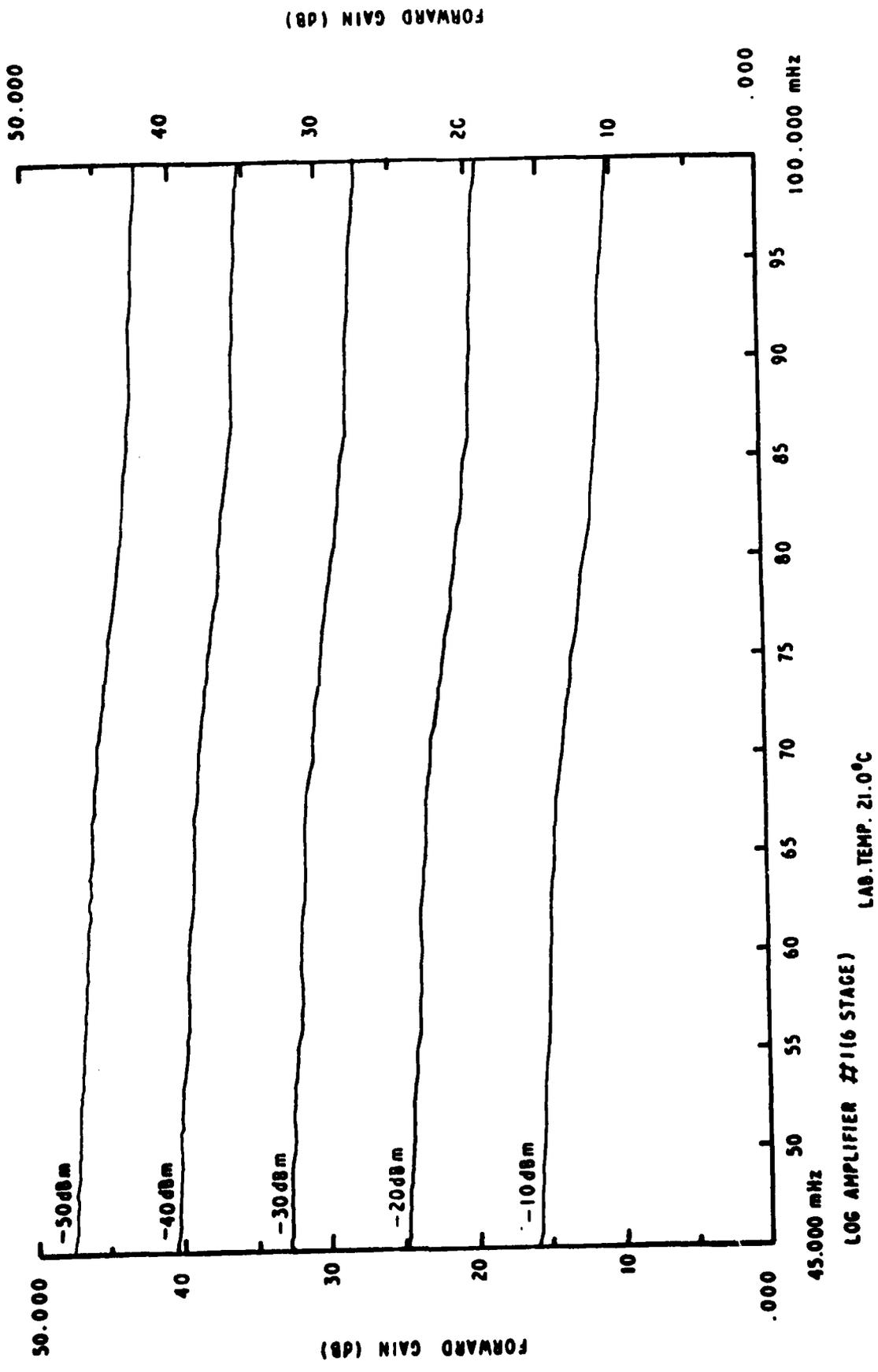


FIG. 5A MEASUREMENT OF GAIN CHANGE v SIGNAL LEVEL CONSTANT TEMP.

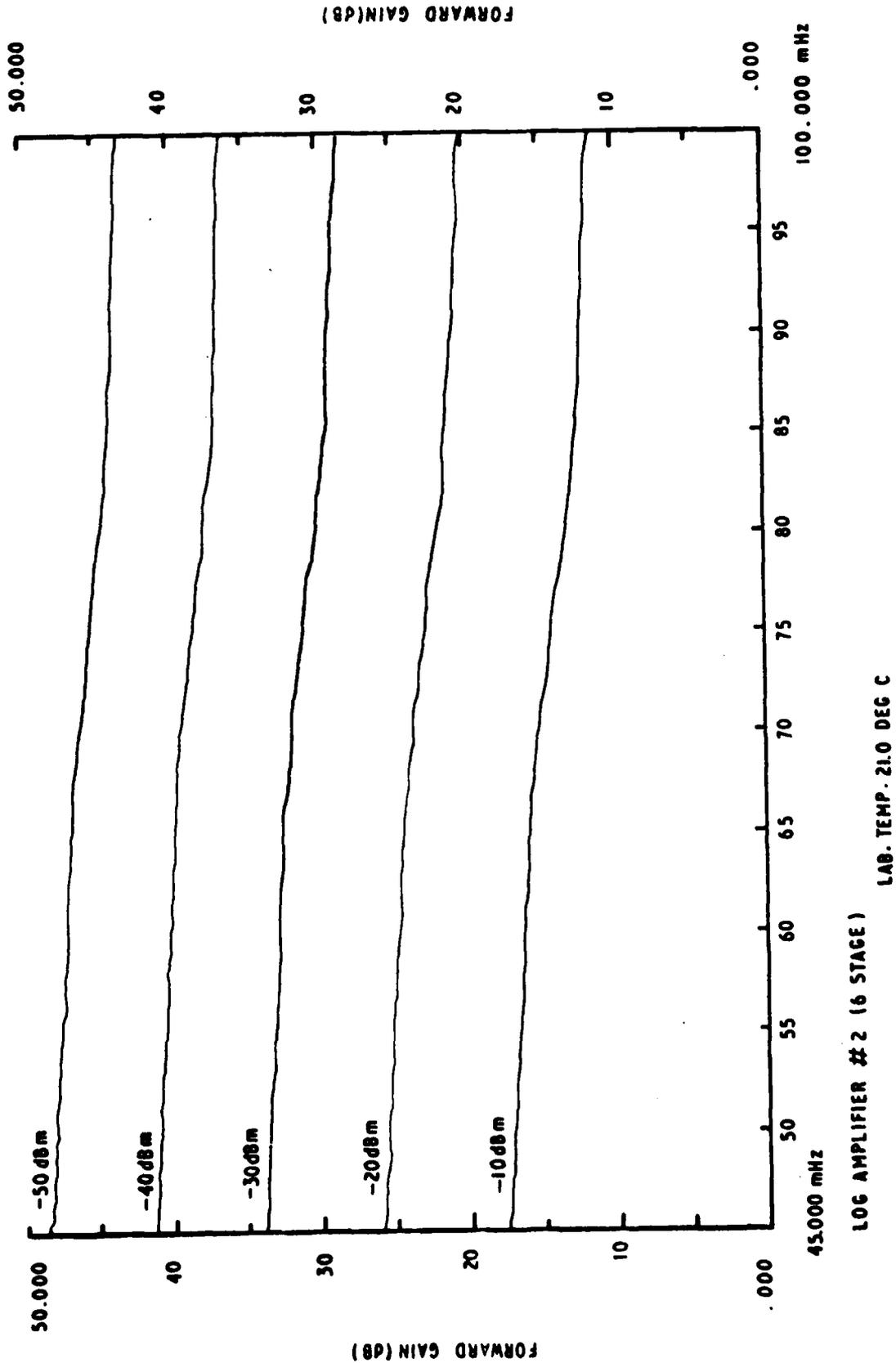


FIG. 5B MEASUREMENT OF GAIN CHANGE V SIGNAL LEVEL CONSTANT TEMP.

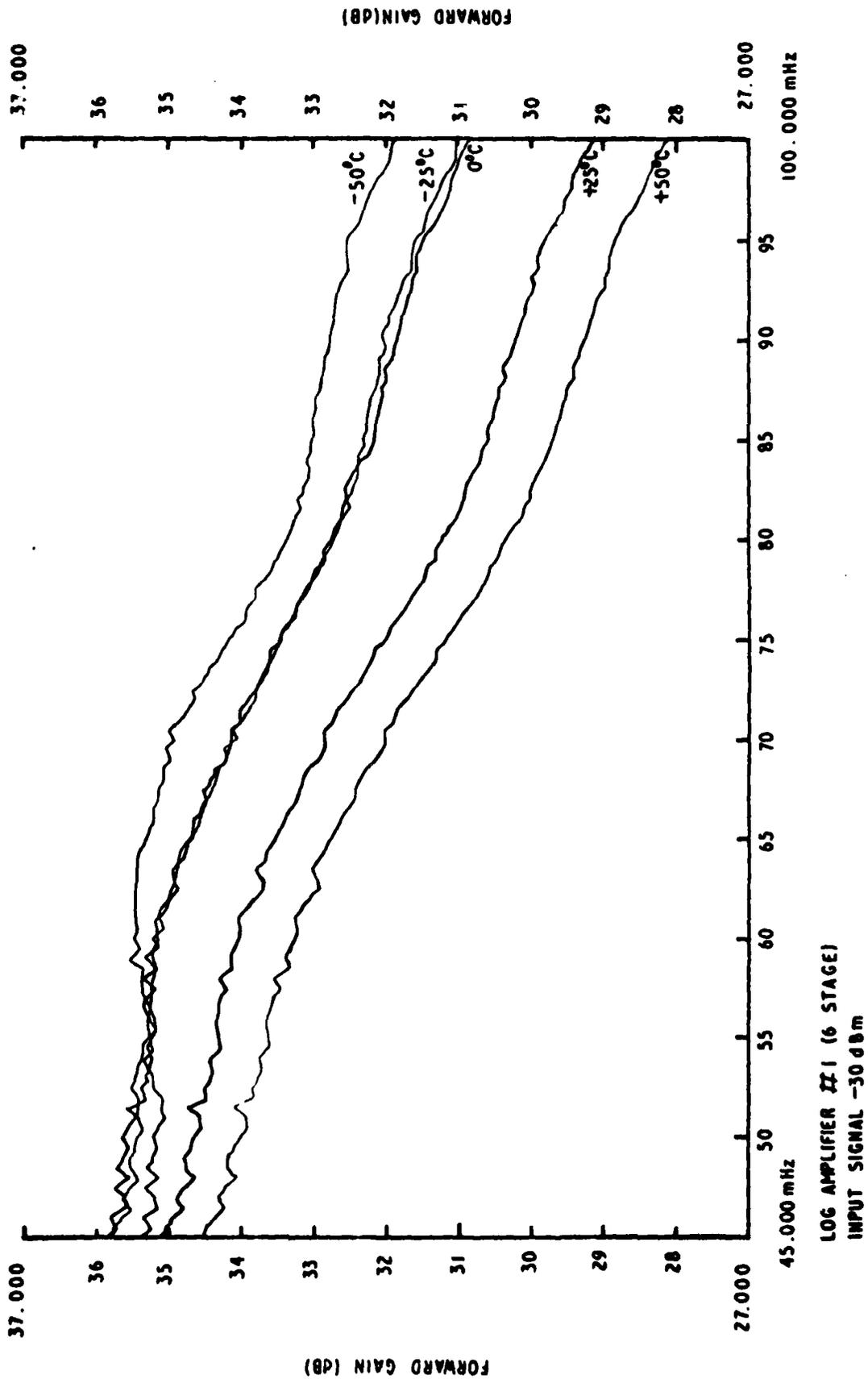
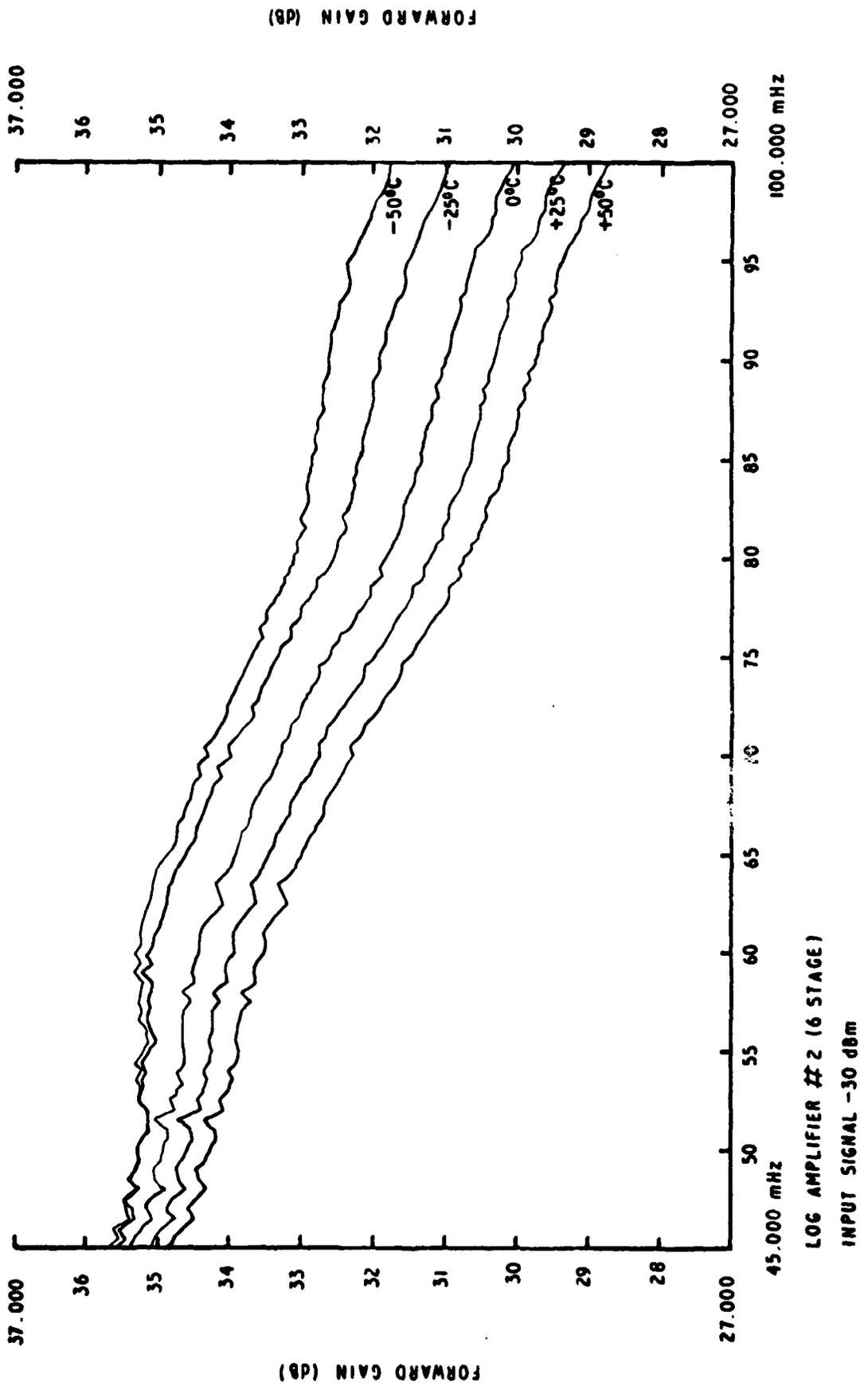


FIG. 6A MEASUREMENT OF GAIN CHANGE v TEMP^R CONSTANT I/P SIGNAL



LOG AMPLIFIER #2 (6 STAGE)
 INPUT SIGNAL -30 dBm

FIG. 6B MEASUREMENT OF GAIN CHANGE v TEMP. CONSTANT I/P SIGNAL

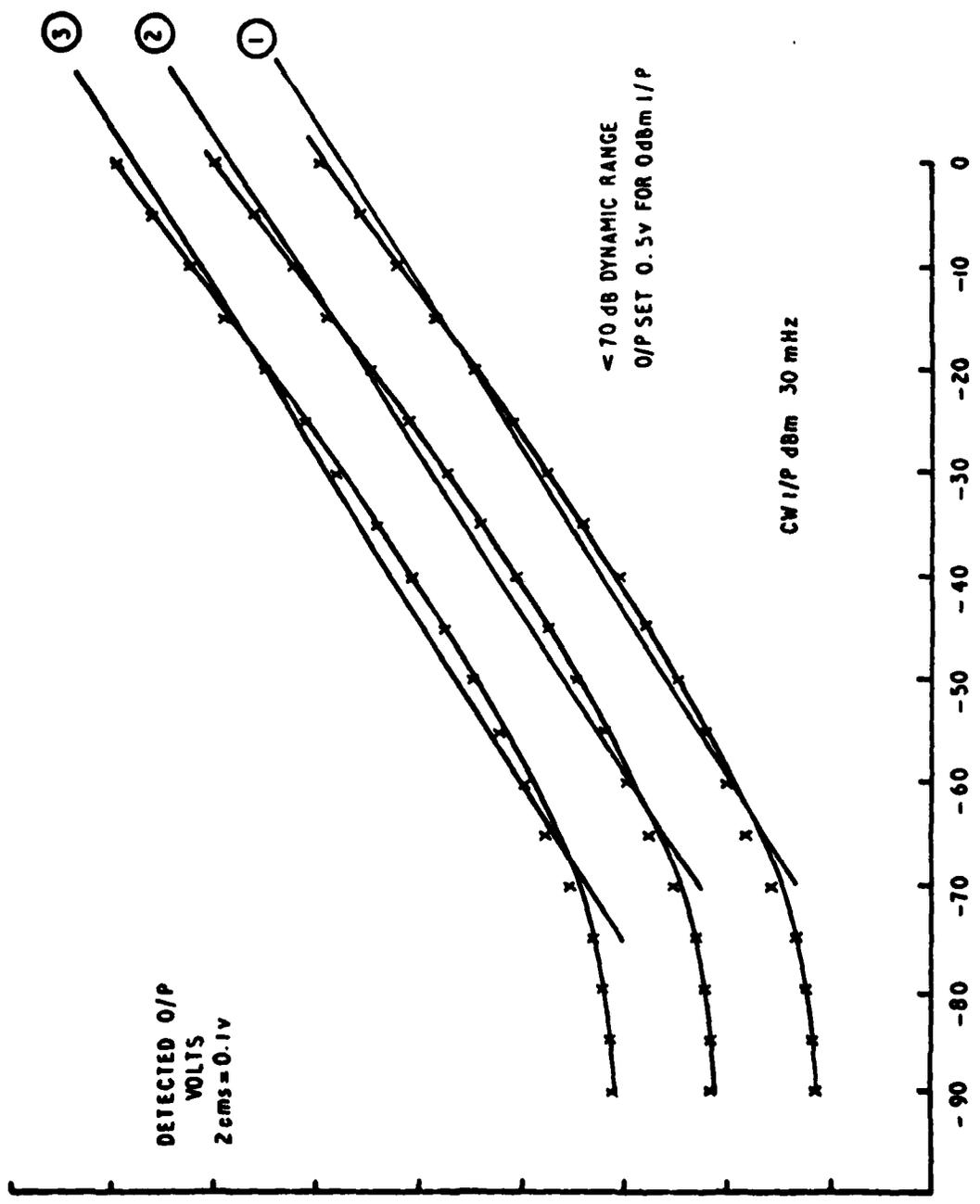


FIG. 7A DYNAMIC RANGE OF 7 STAGE LOG AMPERS. AT 30 mHz I/P AMPERS. Nos. 1, 2 AND 3 DET O/P

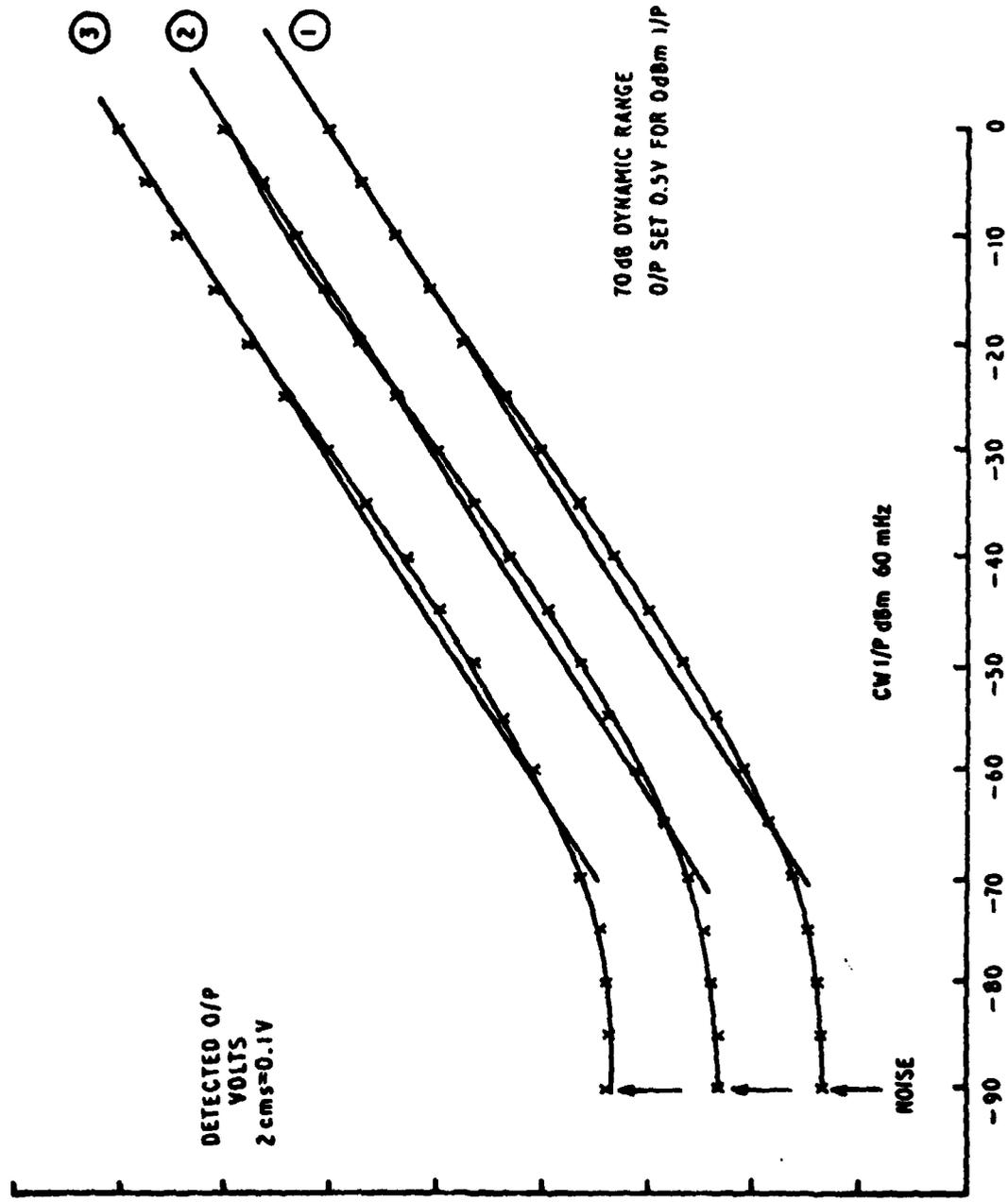


FIG. 7B DYNAMIC RANGE OF 7 STAGE LOG AMP'S. AT 60 MHz I/P AMPRS. Nos. 1, 2 AND 3 DET'D O/P

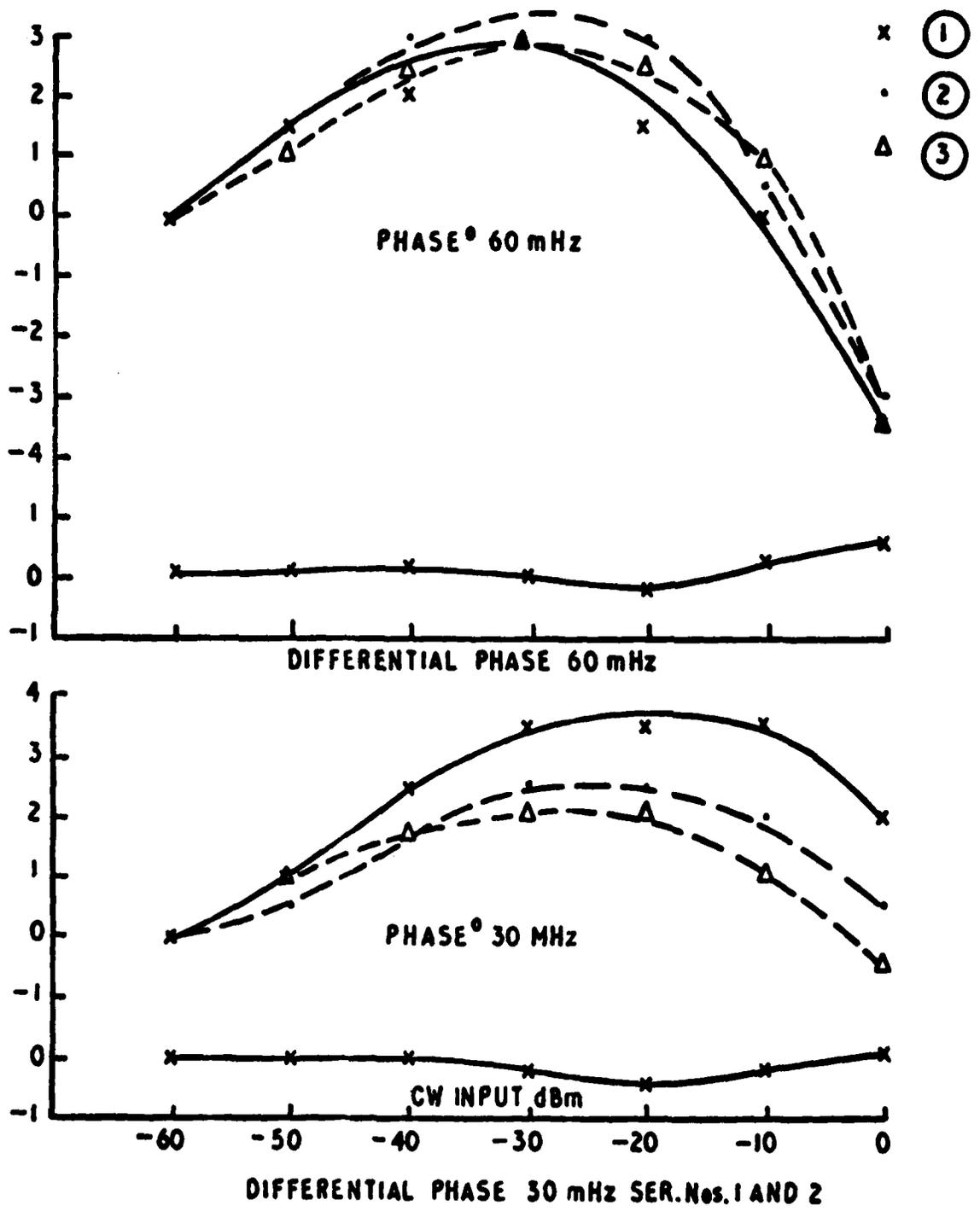


FIG. 8 7 STAGE AMP^R. SER. Nos 1, 2 AND 3

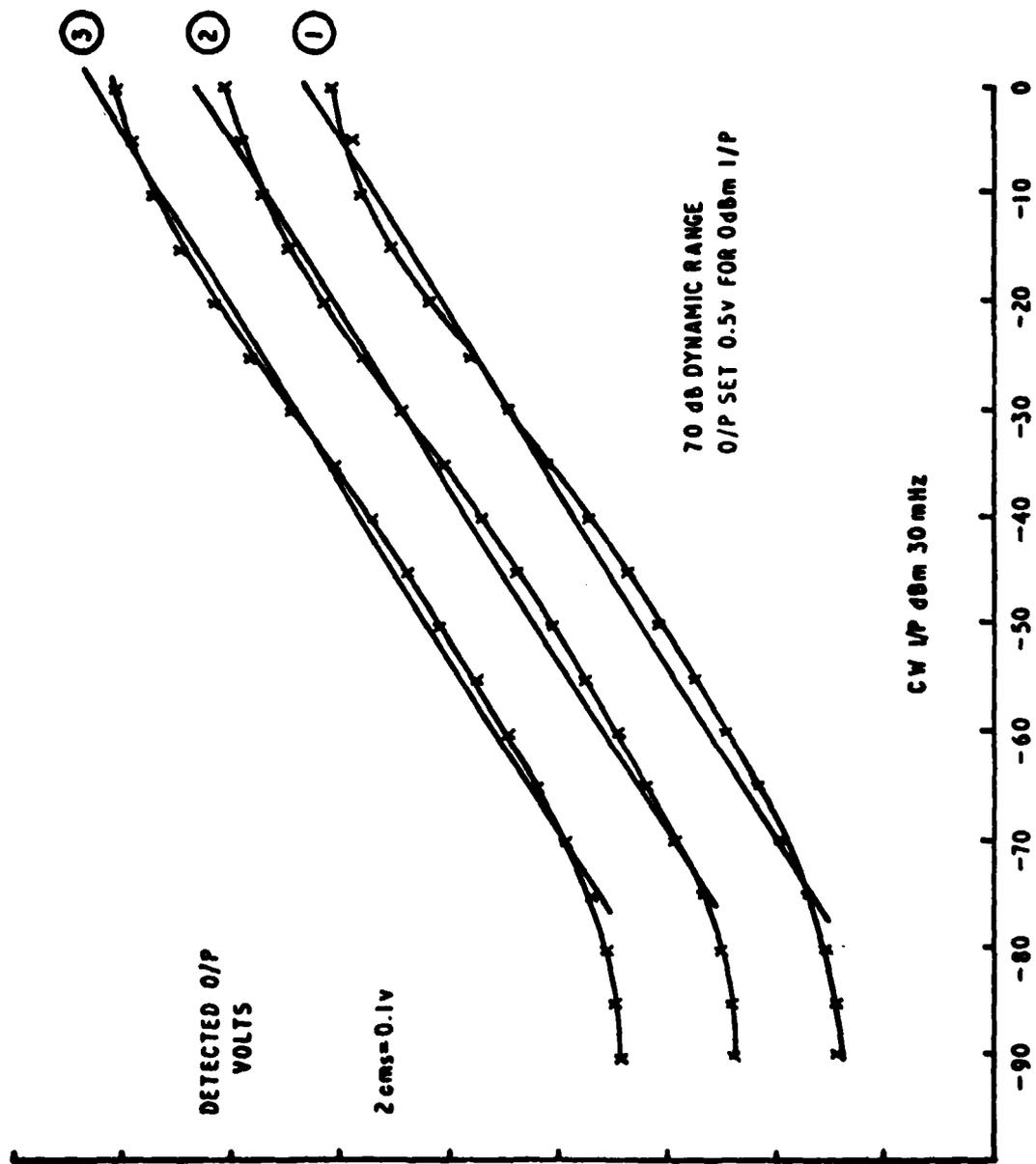


FIG. 9A DYNAMIC RANGE OF 8 STAGE LOG AMP'S. AT 30 MHz I/P AMP'S. Nos. 1, 2 AND 3 DET'D. O/P

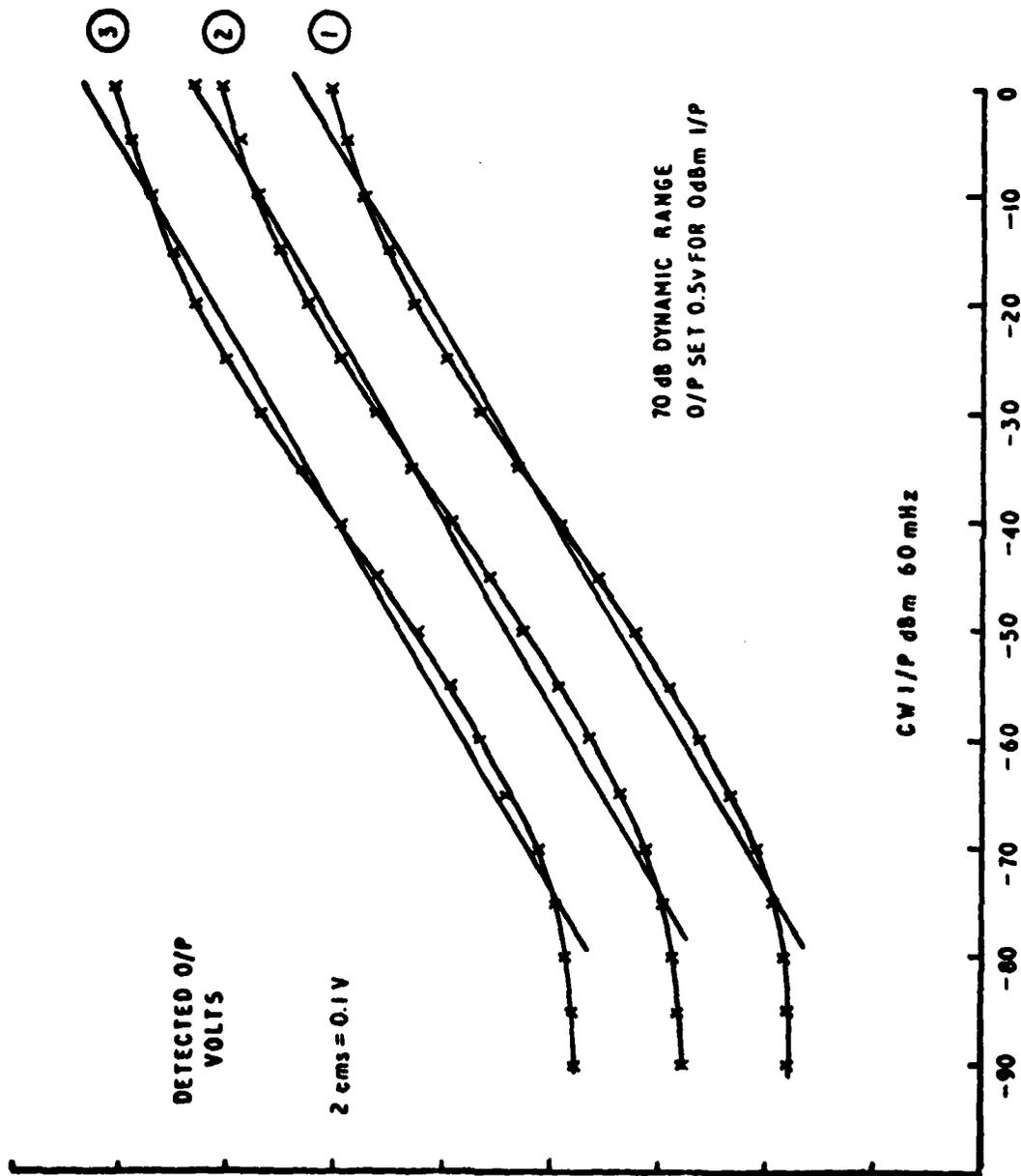


FIG.9B DYNAMIC RANGE OF 8 STAGE LOG AMPRS. AT 60 MHz I/P AMPRS. Nos.1,2 AND 3 DET O/P

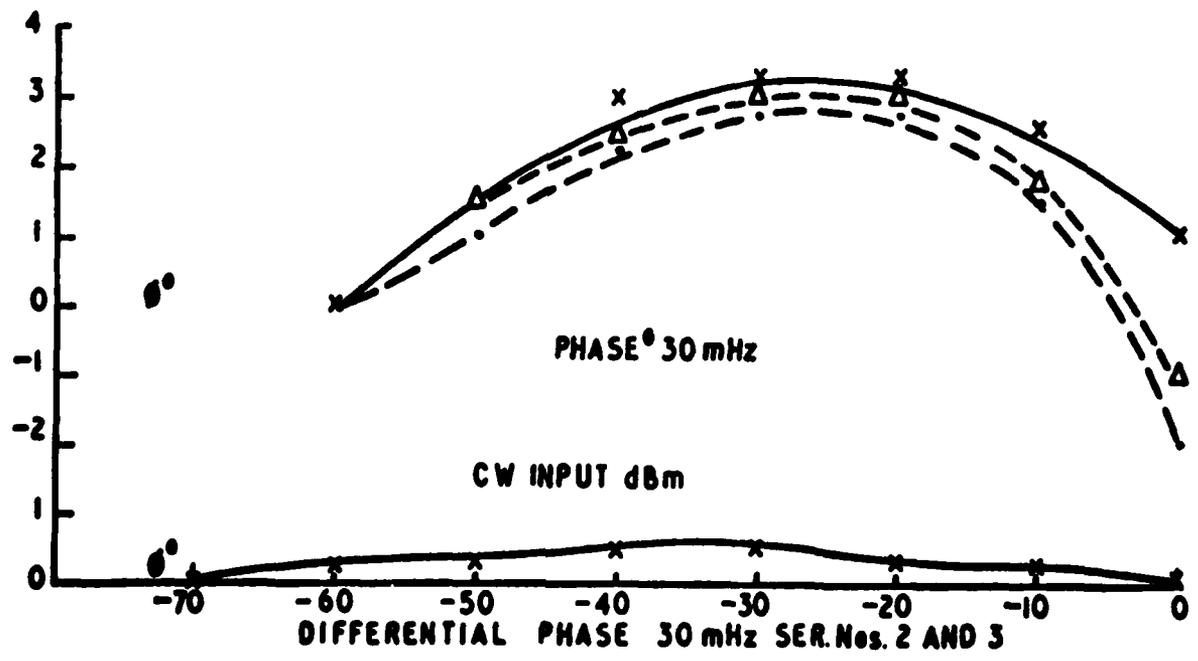
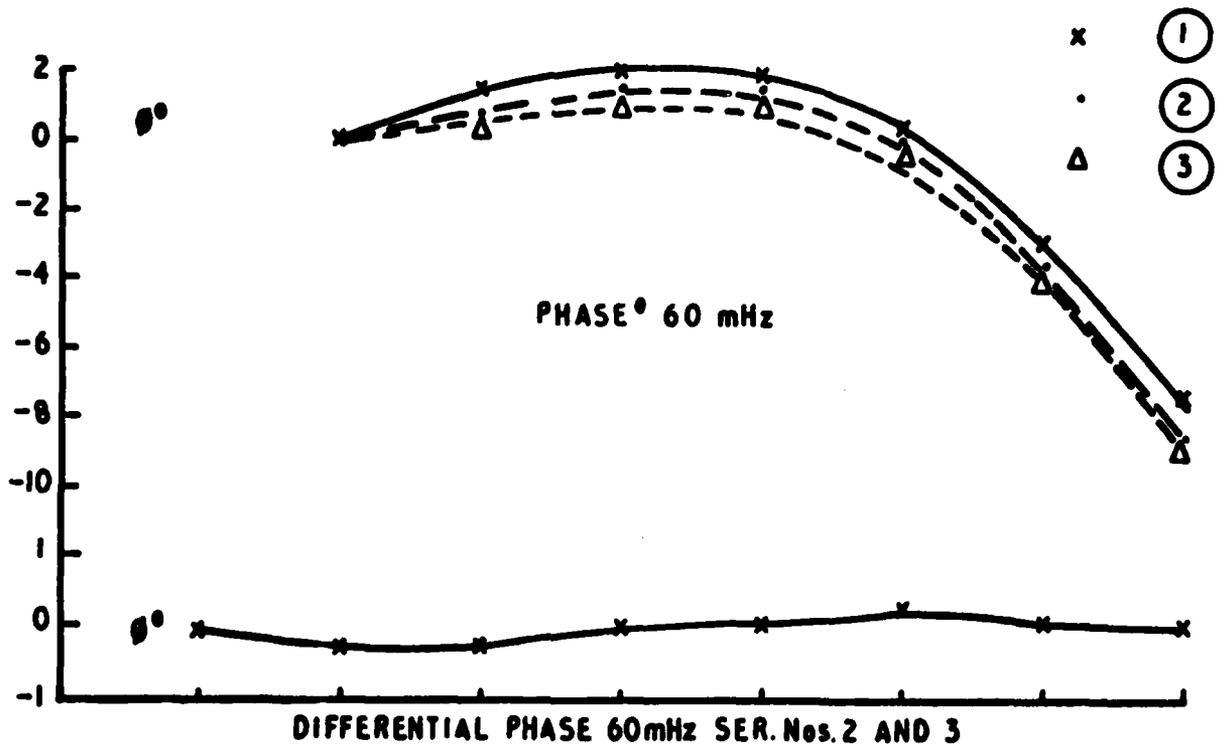
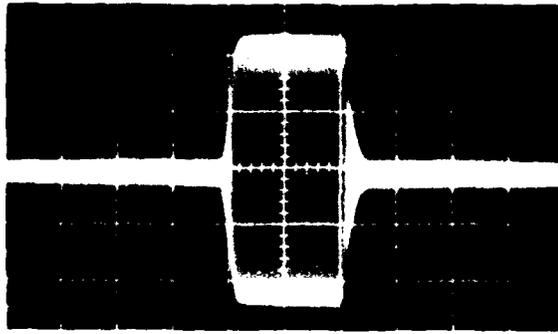
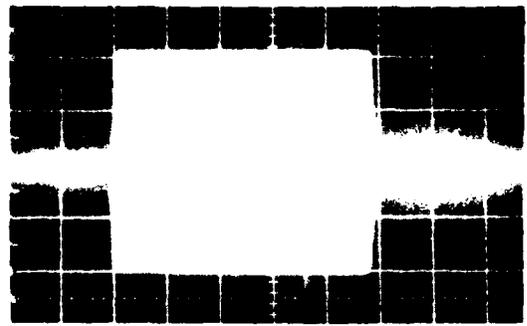


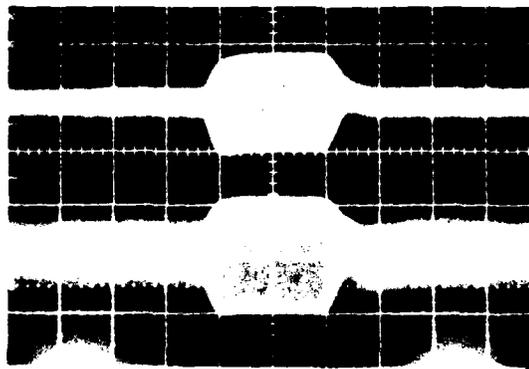
FIG. 10. B STAGE AMP^R SER. Nos. 1, 2 AND 3



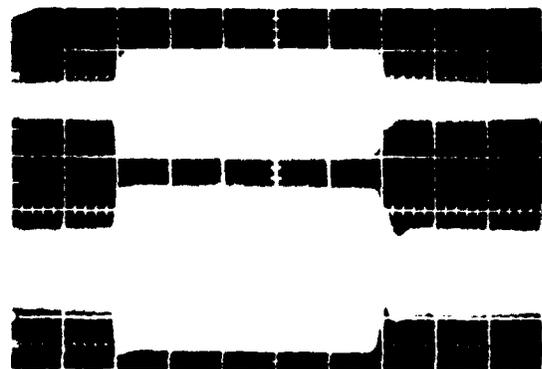
1 μ /s I/P PULSE



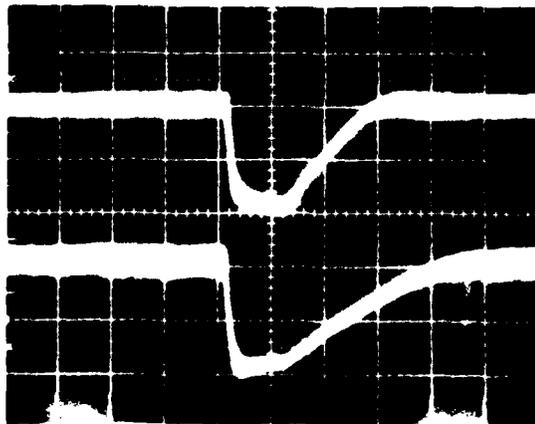
10 μ /s I/P PULSE



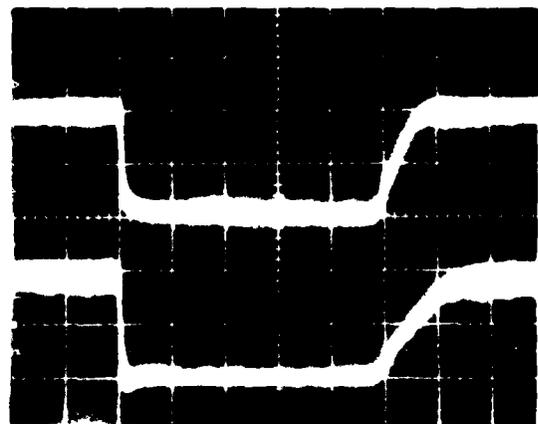
1 μ /s O/P PULSE
6 STAGE AND 8 STAGE AMPR.



10 μ /s O/P PULSE
6 STAGE AND 8 STAGE AMPR.



1 μ /s O/P PULSE
6 STAGE AND 8 STAGE AMPR.



10 μ /s O/P PULSE
6 STAGE AND 8 STAGE AMPR.

FIG. 11

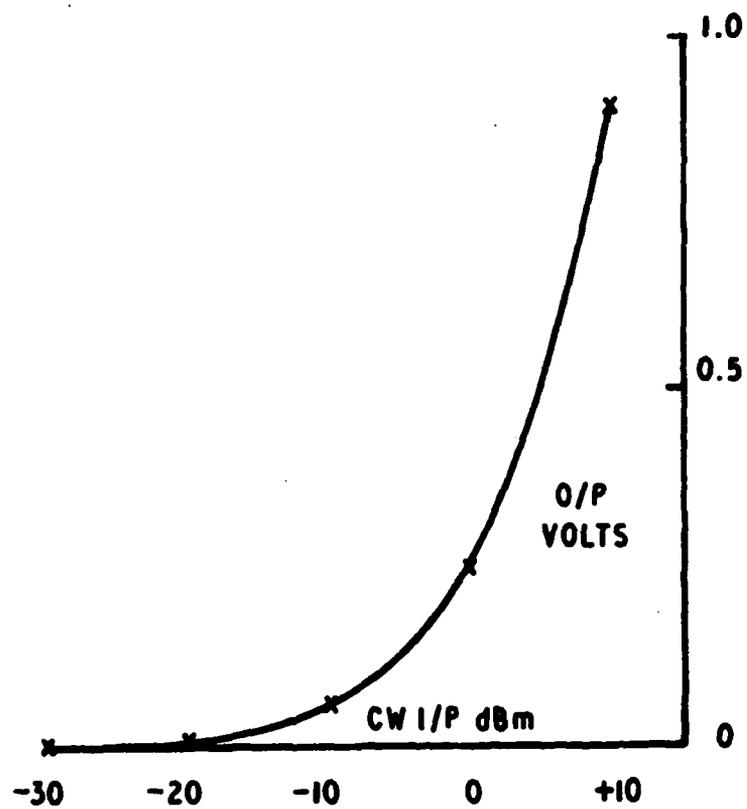
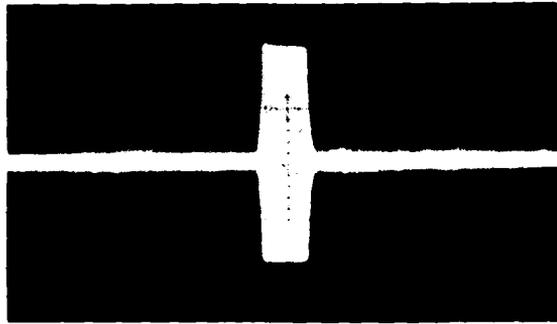
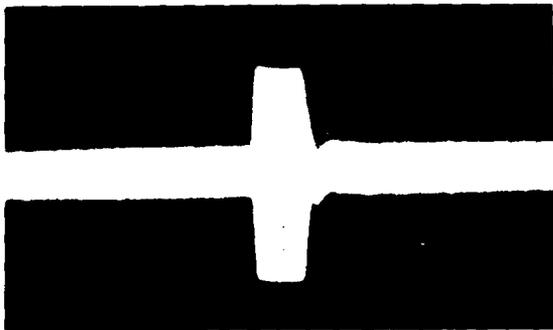


FIG. A1 DIODE DC1554 IN SIVERS COAXIAL MOUNT
AT 60 MHz



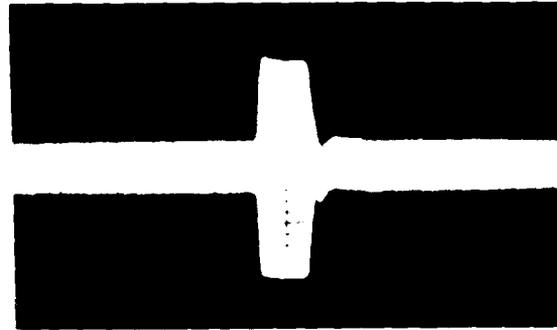
I/P PULSE - 20 dBm
 $2\mu\text{s/cm}$ 50mv/cm

No. 1

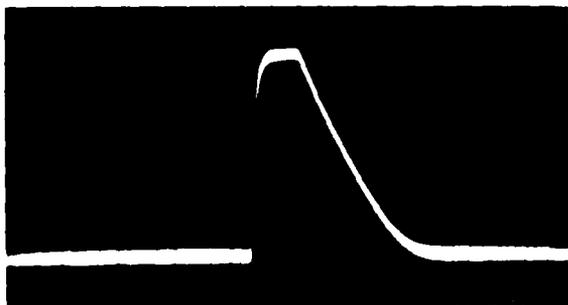


O/P PULSE
 $2\mu\text{s/cm}$ 0.5v/cm

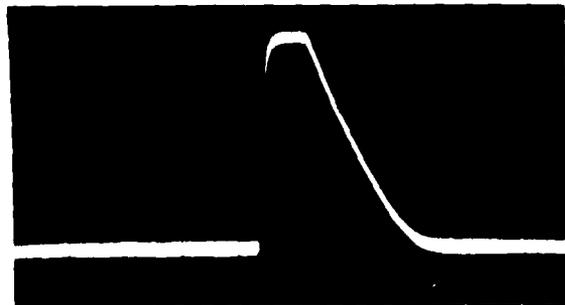
No. 2



O/P PULSE
 $2\mu\text{s/cm}$ 0.5v/cm



DETECTED O/P PULSE
 $2\mu\text{s/cm}$ 0.1v/cm



DETECTED O/P PULSE
 $2\mu\text{s/cm}$ 0.1v/cm

FIG. A2 TRUE LOG AMP^R. SERIES Nos. 1 AND 2 PULSE RESPONSE

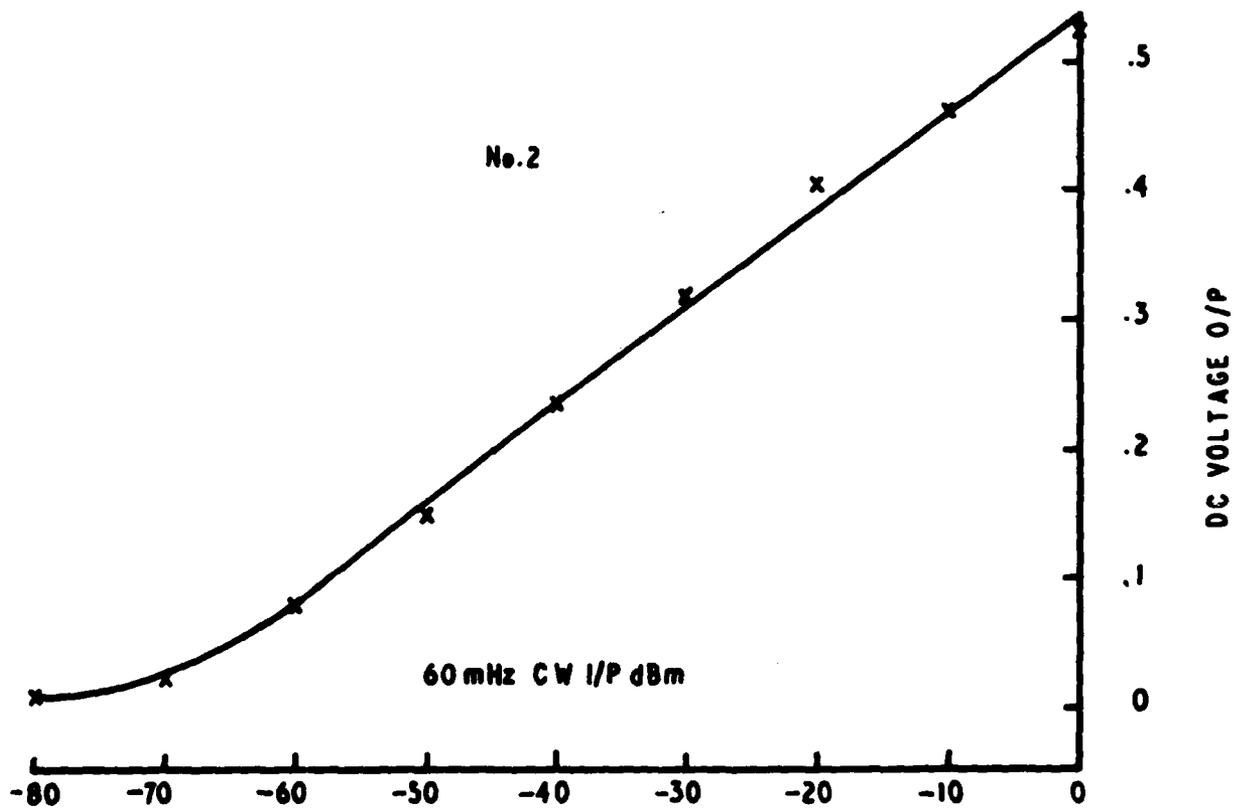
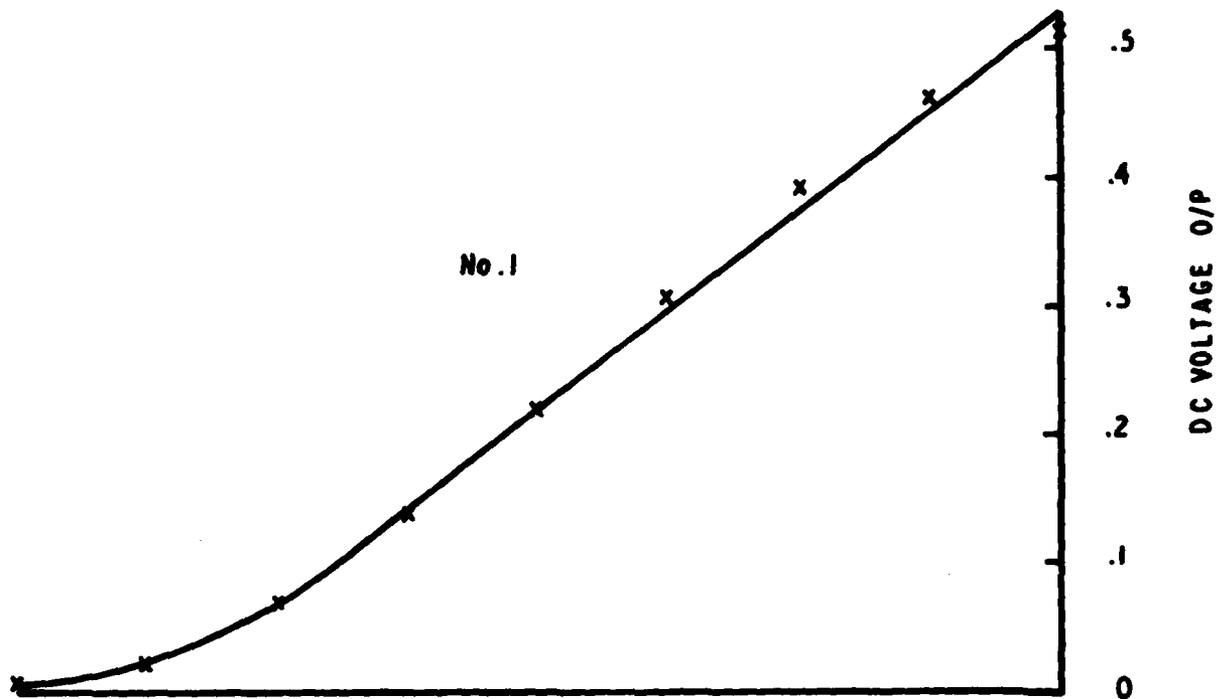


FIG. A3 TRUE LOG AMP^R. SERIES Nos. 1 AND 2 CW I/P v DETECTED O/P

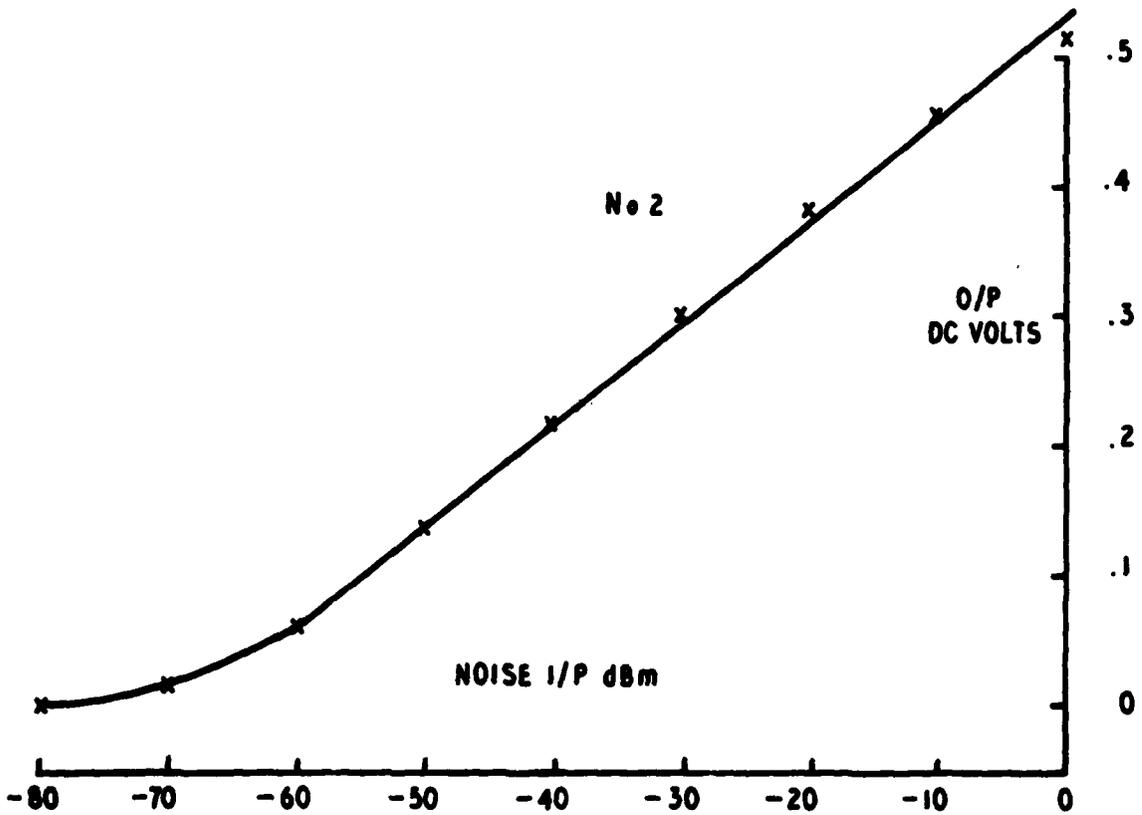
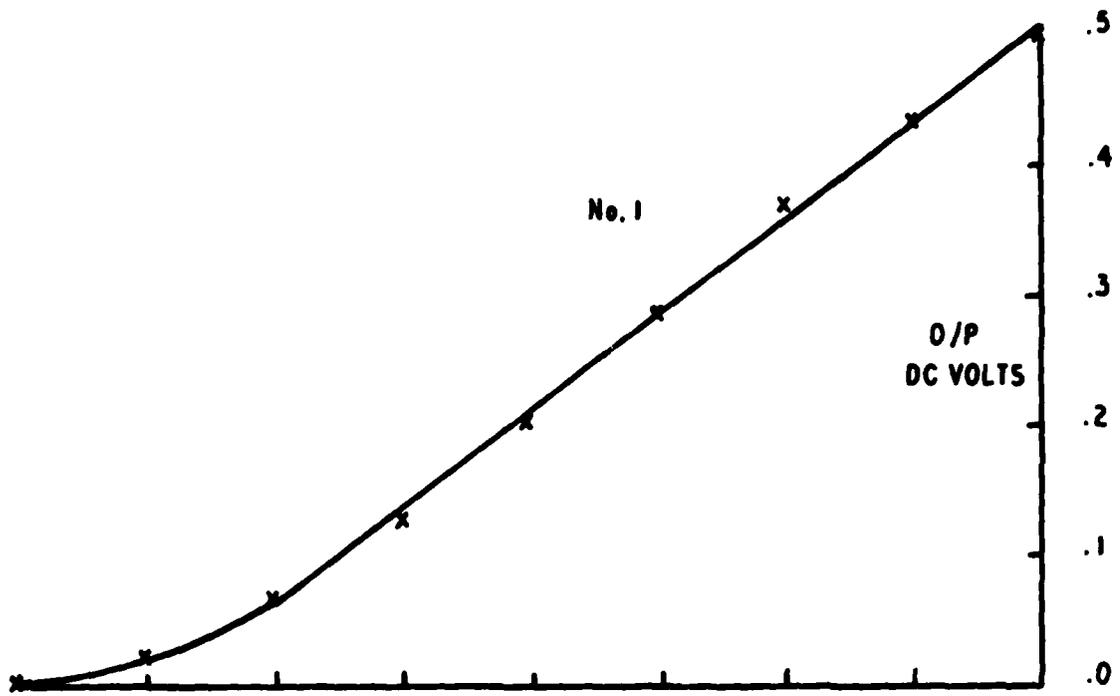


FIG. A4 TRUE LOG AMPR. SERIES Nos. 1 AND 2 NOISE I/Pv DETECTED O/P

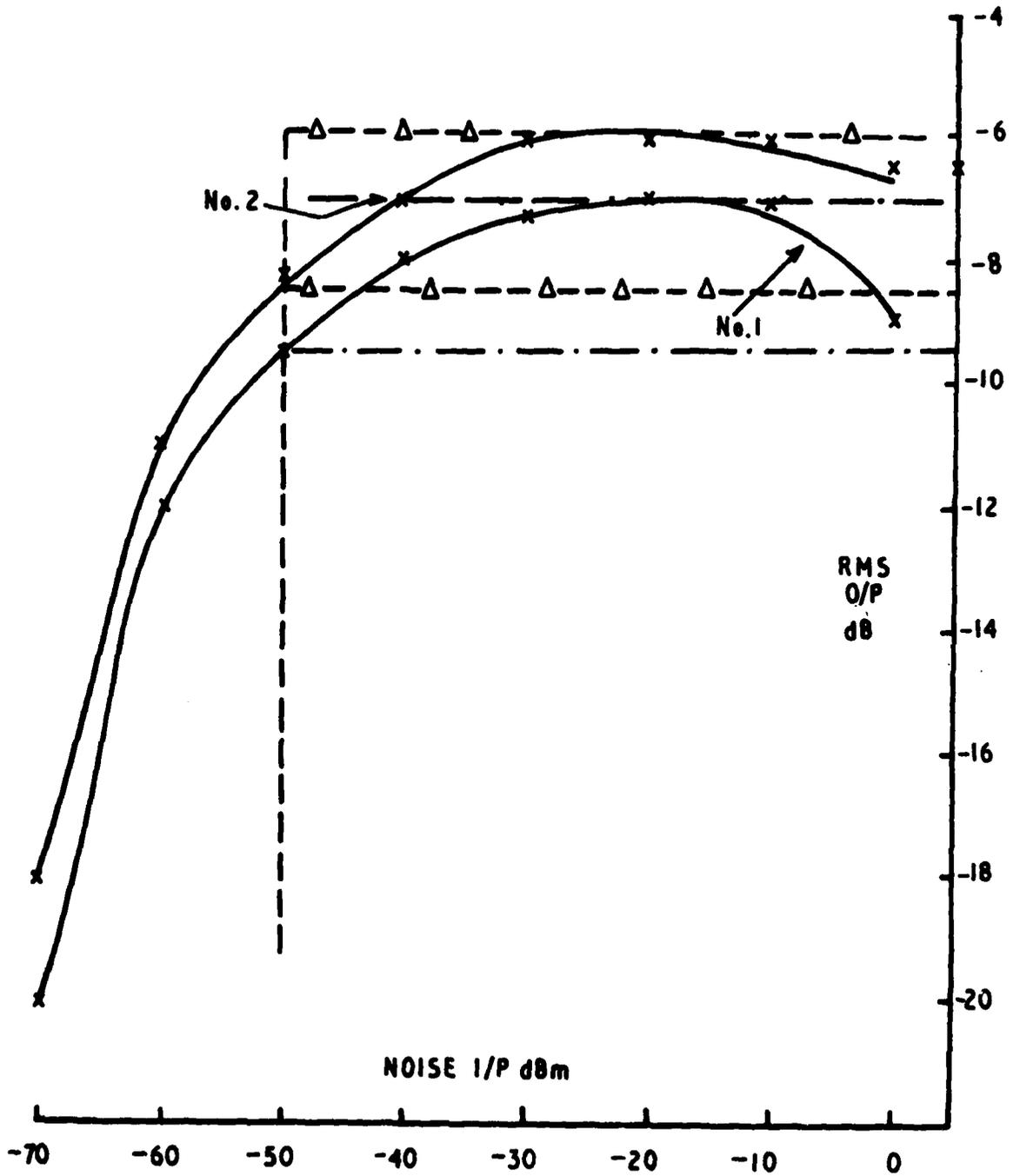
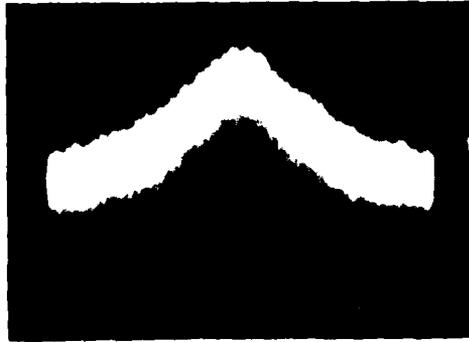


FIG. A5 TRUE LOG AMP. SERIES Nos. 1 AND 2 NOISE INPUT v R.M.S. OUTPUT

FIG. A6 SPECTRUM OF 6 STAGE
TRUE LOG AMP. AND 4 MHz BW.
FILTER WHEN SUBJECTED TO
WHITE NOISE INPUT



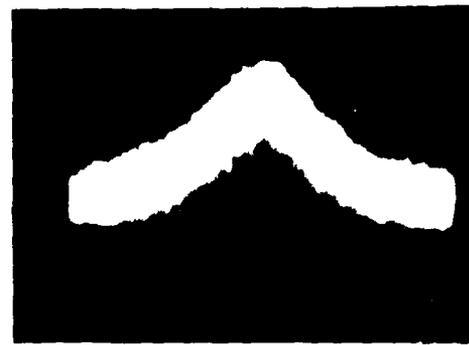
0 dBm



-10 dBm



-20 dBm



-30 dBm



-40 dBm

10 dB/cm
5 MHz/cm

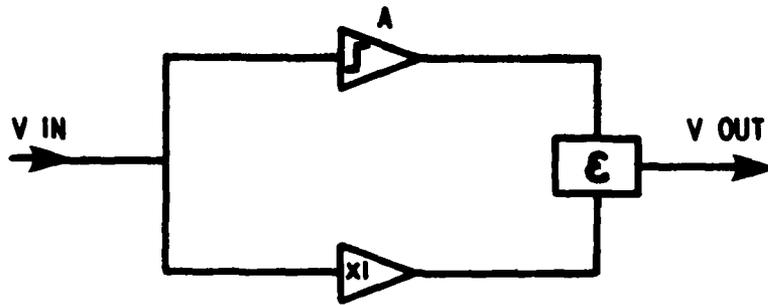


FIG. B1 DUAL GAIN STAGE SCHEMATIC

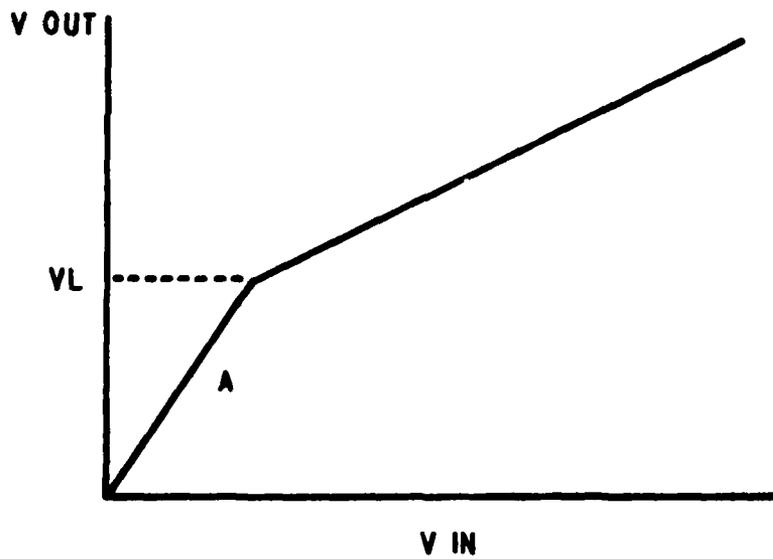
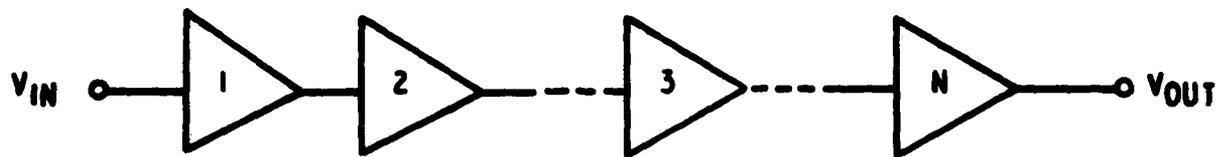
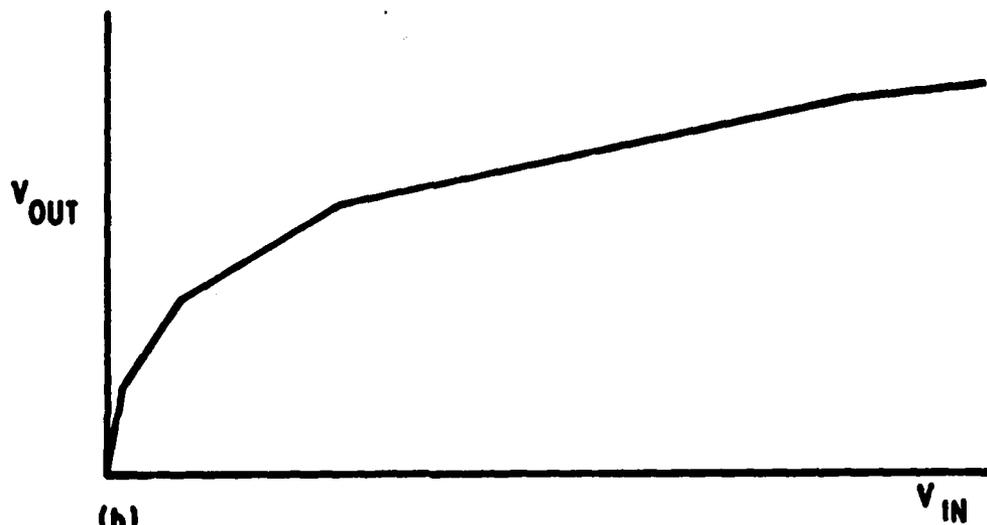


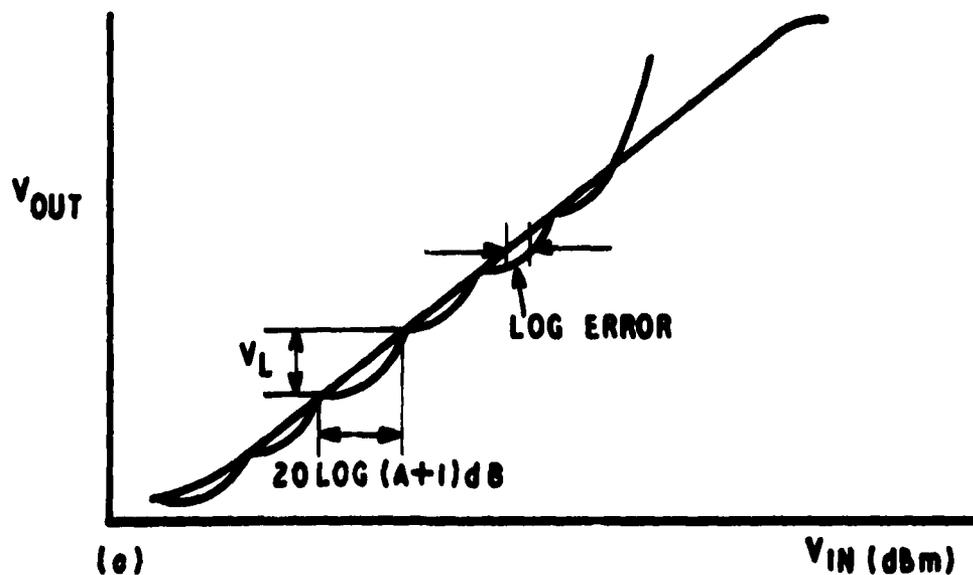
FIG. B2 DUAL GAIN TRANSFER CHARACTERISTIC



(a)



(b)



(c)

FIG. B3 (a) CASCADED DUAL GAIN STAGE AMPLIFIER
(b) TRANSFER CHARACTERISTIC
(c) OUTPUT CHARACTERISTIC OF THE LOG AMP.

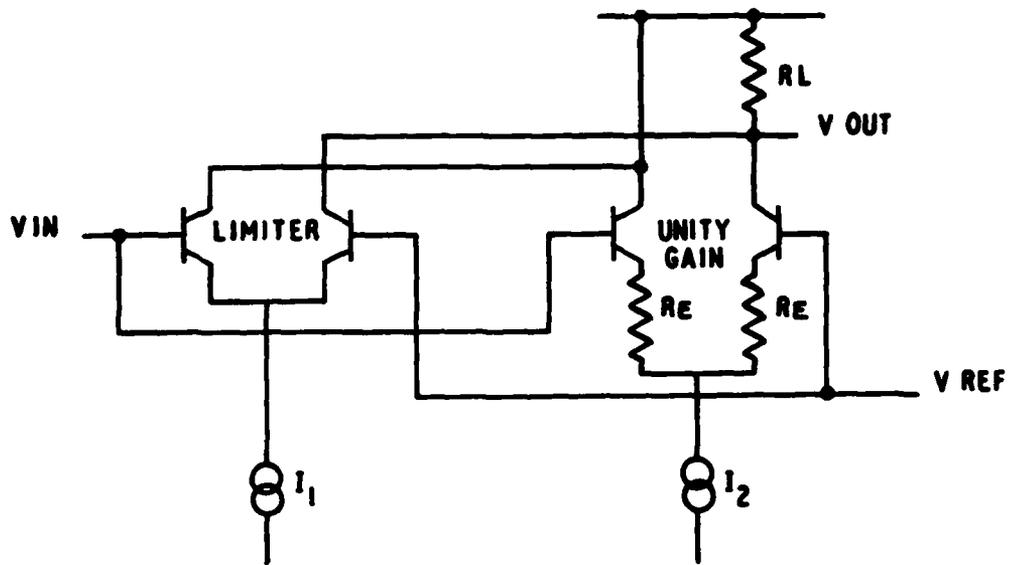


FIG. B4 DUAL GAIN STAGE

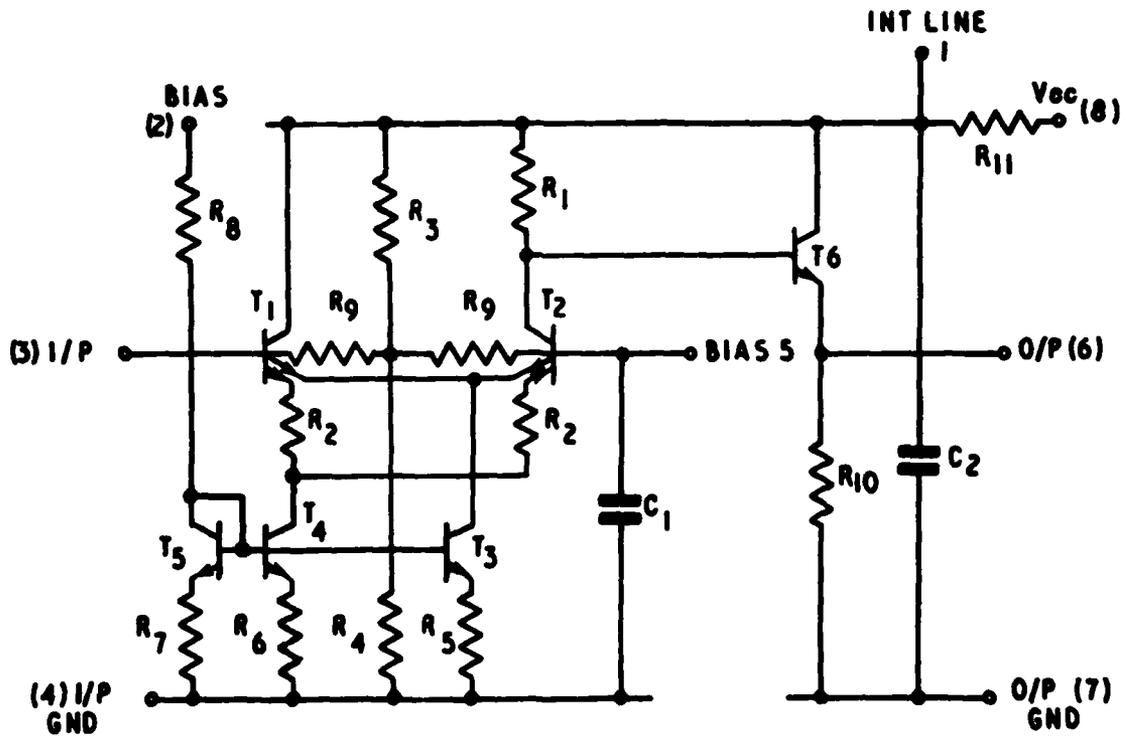


FIG. B5 CIRCUIT DIAGRAM GAIN STAGE

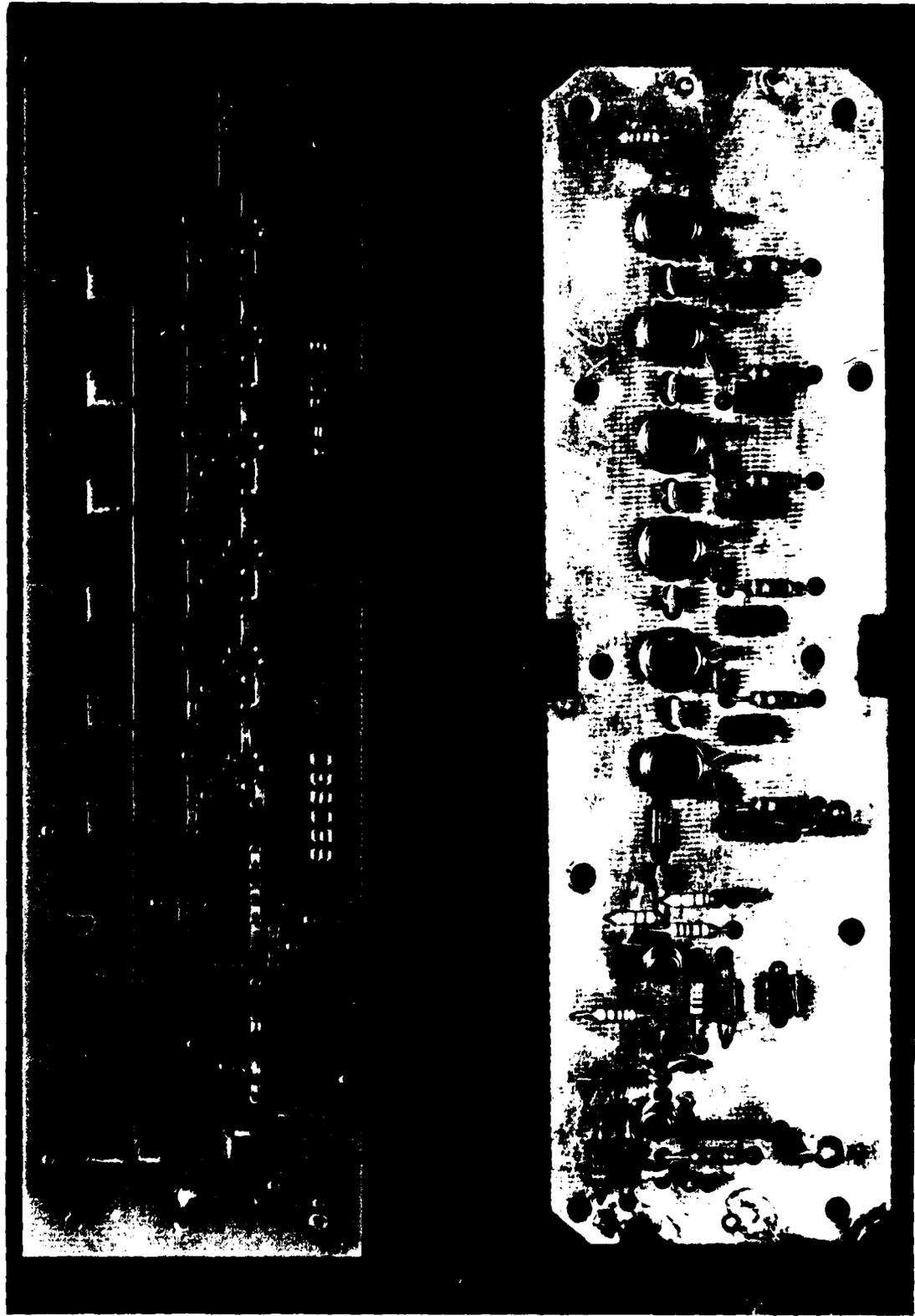


FIG B.6 Circuit Connections on Printed Circuit Board and Component Layout on Earth Side of the Printed Circuit Board.