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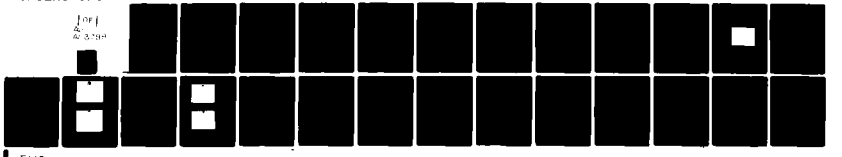

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ADVANCED SUBMICRON FETs

SEMI-ANNUAL REPORT

(May - October 1981)

Prepared by:

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Replacing the mushroom gate profile with a better collimated evaporation has resulted in FETs with equivalent performance. Balanced FETs have been fabricated with equivalent dc performance to their unbalanced counterparts, but with inferior rf performance.

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I. INTRODUCTION

This report describes the initial work done on a new ONR Contract N00014-81-C-0270, which continues two previous ONR contracts. These contracts were N00014-77-C-0655 (Submicron FETs Using Molecular Beam Epitaxy) and N00014-80-C-0391 (Integrated Balanced FETs for Broadband Millimeter Wave Amplifiers). For the sake of continuity, the work described in this report slightly overlaps work described in the final reports on these two contracts.

Under contract 0655, the performance of low-noise FETs using a conventional device structure with dual gate pads (Fig. 1) and a mushroom profile for the gate had been improved at 8 GHz to a 1.1-dB noise figure with 13.9 dB of associated gain. Better performance than this had been expected, extrapolating the performance obtained with devices having very much higher (six times) the gate resistance, i.e., without the mushroom gate profile. The possibilities of inadequate measurement techniques, as well as electron-beam damage to the channel needed to be investigated. At the start of this reporting period, the feeling was that the technology had advanced to the point of having no first-order deficiencies (e.g., high gate or source resistances, etc.), and that further improvements in measured noise figure would have to come from either second-order corrections or improved measurement techniques, or both.

Under contract 0391, a balanced FET mask set was designed (Fig. 2) and devices were fabricated to match the dc characteristics of the sub-half-micron gate FETs of contract 0655, but expected to outperform them at rf frequencies by virtue of lower gate resistance, lower source inductance, cancellation of feedback capacitance, and possibly lower source resistance when operated in the balanced or push-pull mode. Preliminary device results were obtained which will be reported below, along with further analysis based upon s-parameter measurements.

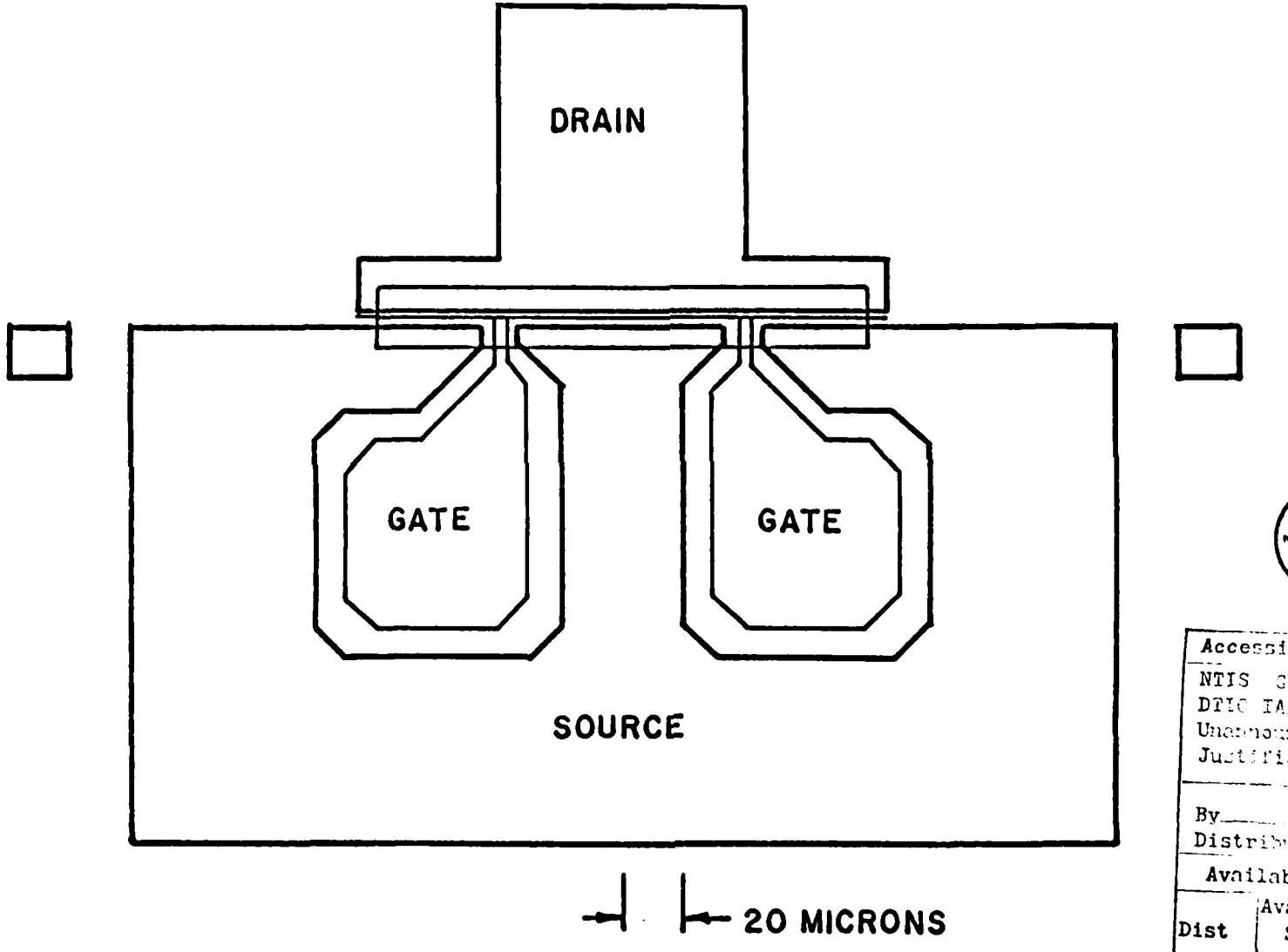


Fig. 1 Dual gate pad geometry.

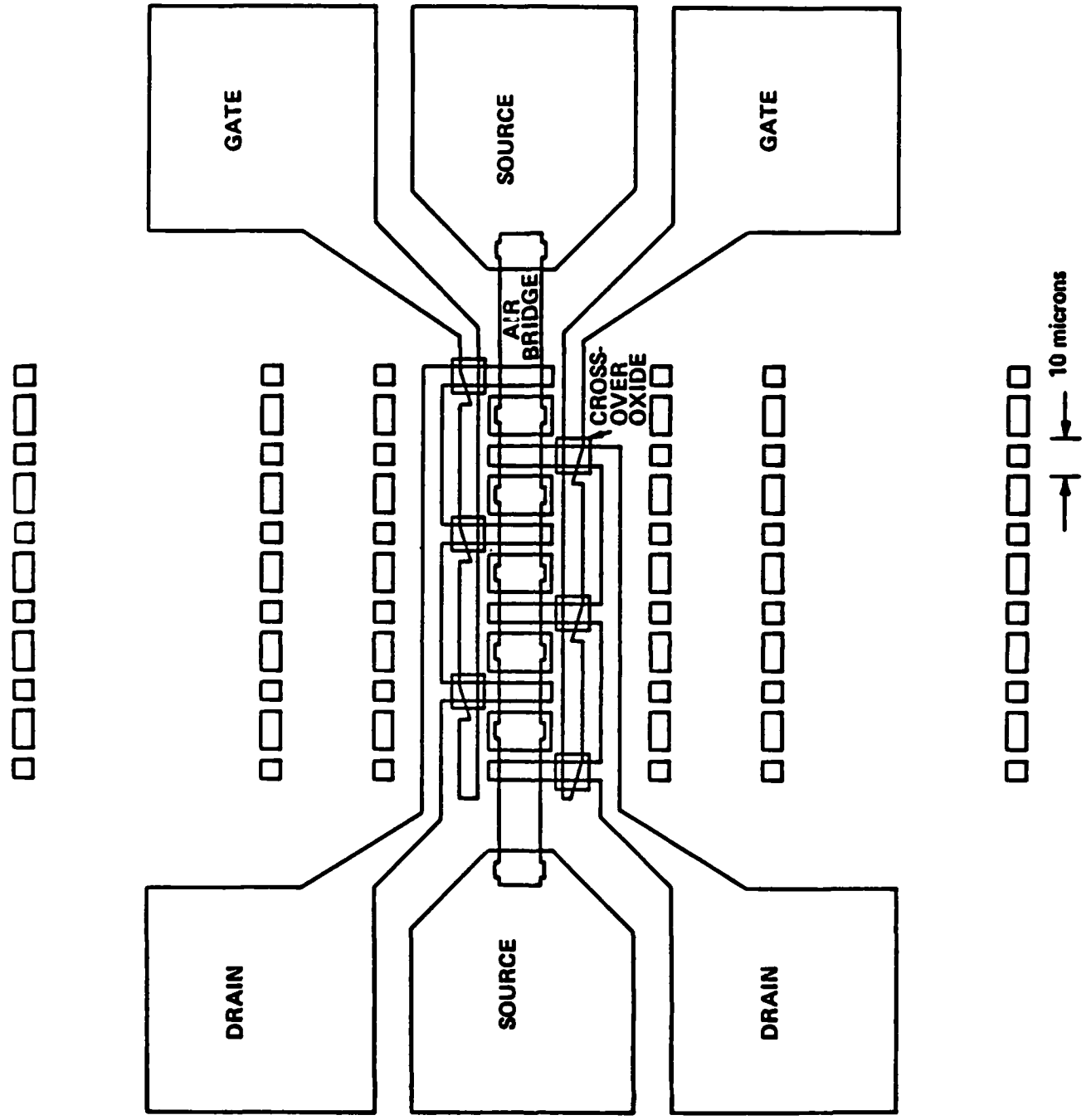


Fig. 2 Design for balanced FET.

II. CONVENTIONAL LOW-NOISE STRUCTURE (FIG. 1)

A. Comparisons with Photolithographic Gates

This work had two main objectives: (1) to determine if electron-beam damage is occurring in the channel region during gate exposure, and (2) to evaluate FET performance with MBE material, using longer gate lengths, exposed photolithographically, together with the self-aligned n^+ technology developed for electron-beam-exposed FETs.

Two runs were made using the same material as had been used for the electron-beam-exposed FETs, but with the gate exposed using photolithography. The first run was done using the Varian "NOM" mask set. Its gate length is nominally one micron and the device width is Z = 300 μm. The results are shown in Table I. The device gate lengths were on the order of 1.2 μm. The origin of the substantial difference in noise figures for the two devices measured was not investigated in detail.

TABLE I

NOM Device Results at 8 GHz

Device	NF_m (dB)	G_a (dB)
NOM 1	2.82	8.8
NOM 2	1.87	10.2

The second run was done using the Varian "LNX-100" mask set. This mask set has a nominal gate length of 0.5 micron and a device width, Z, of 240 μm. The results of this run are shown in Table II. Because of contact problems in the photolithography, the gate lengths were 0.9-1.0 micron. It had been hoped to achieve 0.5 micron in order to afford a closer comparison with the electron-beam-exposed devices. Ideally, one would want the same gate lengths as for the electron-beam-exposed devices

in order to determine directly whether electron-beam damage is a problem. These results are to be compared with 1.1 dB at 8 GHz with 0.3-μm gates using electron lithography.

TABLE II

LNX-100 Device Results

Device	Frequency (GHz)	NF_m (dB)	G_a (dB)
LNX-100-1	8	1.7	9.5
LNX-100-2	10	2.48	10.3
LNX-100-3	10	2.28	8.5

No definitive conclusions were reached concerning the possibility of electron-beam damage in this work. If the noise figures for the photolithographic gates are scaled according to Fukui's noise figure equation[1] from one-micron gate lengths down to a 0.25 value, with all of the other parameters the same (which indeed is a good assumption since the material parameters, pinchoff voltage, source resistance, and gate resistance were measured to be virtually the same), a value of 0.65 dB is obtained at 8 GHz. This value is significantly better than the 1.1-dB values actually measured. However, it is believed that Fukui's equation is valid for an aspect ratio of gate length/channel thickness in the region of 3:1, and hence isn't applicable to the 14:1 ratio of the optically-exposed gates. Hence, the only real way to make a valid comparison is to fabricate devices with long electron-beam-exposed gates.

B. Electron-Beam Damage Study

As mentioned in Annual Report No. 3 of ONR Contract N00014-77-C-0655, because of the degradation observed in the FET drain characteristic when the device is inspected using the 20-keV electron beam of the

scanning electron microscope, it might be expected that some material degradation in the channel would also occur when the gate region is exposed with a 20-keV beam in the lithography process.

An annealing study done by Pons and Mircea of LEP[2] on electron irradiation-induced defects in GaAs indicates that a 210°C anneal for 150 min significantly reduces the concentration of the defect levels E2-E5 produced by a 1-MeV electron beam. Accordingly, a 2.5-hr anneal at 210-220°C in N_2 was done on several completed devices from run EB 29. The result was that the gate leakage increased (went from 10 μA at 4V to 10 μA at 1V) and the minimum noise figure increased rather than decreased, going from 1.1 to 1.63 dB.

A discussion with A. Zylbersztejn of Thompson-CSF at the U.S.-France Workshop on GaAs Microstructures in Boston, June 8-10, 1981, led to the conclusion that there should be little or no electron-beam damage to the channel. Zylbersztejn has investigated the effects of traps induced by 1-MeV electron irradiation upon FET properties and concluded that the threshold for damage to GaAs in terms of generation of deep level traps E1-E5 is 200-250 keV. A paper is soon to be published concerning this. It appears unlikely therefore that the 20-keV level used to expose the gate patterns could damage the material in the channel region.

C. More Device Runs

Typical gate lengths for mushroom gate geometries appear to be larger than obtained previously on nonmushroom structures. Values for run EB 29, for example, appeared to lie on the 0.3 to 0.4-micron ranges. This may be an artifact, due to the difficulty of measurement caused by the mushroom overhang on top of the gate stripe. In order to achieve shorter gates than this, several runs were made during this period without the mushroom structure. The idea was to rely on a baffled gate

evaporation to transform the triangular gates into a thicker, more rectangular structure to reduce the gate resistance from its values for runs prior to EB 29. Even though the gate resistance might not be as low as for the mushroom structure, the gate lengths should be shorter and more easily measured.

Table III gives the results of several runs not employing the mushroom gate structure.

TABLE III

Non-Mushroom Gate Performance at 8 GHz

Run	NF_m (dB)	G_a (dB)	Estimated Gate Length (μm)	r_g (Ω)	R_s (Ω)
EB 30	1.17	12.6	~0.35		
EB 31-1	1.13	13.2	~0.35	1.17-1.5	
EB 31-2	1.2	14.1	~0.35	1.17-1.5	
EB-32			0.25-0.3	0.945	
EB 34			0.27	1.04-1.25	
EB 35-1	1.05	14.0	~0.25	1.38	4.2
EB 35-2	1.13	13.0	~0.25	1.38	
EB 35-3	1.13	13.0	~0.25	1.38	
EB 36	1.12	13.0	~0.3		4.3

The main yield killers for these runs were (1) missing gate sections, due presumably to the PMMA resist being too thin to give a clean break between the gate metal and the metal to be lifted off, coupled with the poor adhesion of Au to GaAs, and (2) the loss of devices during the substrate thinning and scribing process (especially runs EB 30-34).

A resist layer was used to protect the front surface of runs EB 35 and 36 during the substrate thinning, which helped the yield considerably. A thicker PMMA layer (0.8 μm vs. 0.6 μm) was used for run EB 33, but

evidently the gate metal thickness was even thicker, and all of the gates lifted off, for zero yield. In addition, the thicker resist gave a longer channel recess (~1 μm), due to the larger overhang caused by electron scattering.

The results in Table III show a consistent uniformity in the rf results for all of the runs, being 1.0-1.2 dB for NF_m and 13-14 dB for G_a. These results are basically the same as those for run EB-29 which employed a mushroom profile for the gate. Note that the gate resistance values are only lsightly higher than the 0.8-0.9 ohm values for EB-29. When compared to the 6 ohms for the unbaffled run EB 26, this confirms the improvement caused by using the baffles to produce a collimated molecular beam for the gate evaporation. Since r_g for the devices in Table I is significantly smaller than R_s, one would not expect much change in the performance for the increase in r_g from that of EB 29, and indeed there appears to be none. Hence it appears that the more difficult technology of using a mushroom gate profile need not be employed, at least at this time, to achieve optimum performance.

One item worth noting is the higher values of g_m observed for run EB 31. As shown in Fig. 3, values of 36 mmhos were achieved, whereas typically values of 28-30 mmhos are measured. It would seem that this would most likely be due to higher active layer doping (MBE wafer #667).

The uniformity of the rf performance of runs EB 29-36 suggests that either some sort of fundamental limit on device performance has been achieved, or that some limit in the measurement technique has been reached. As has been discussed in Sec. A, a much lower value of NF_m is expected, and it may be that the lossy Q of microstrip matching of the input is a limiting factor now that the device input Q has been increased.

For the low-noise measurements at 8 GHz, the input is matched by adjusting a capacitance which is a quarter of a wavelength away from the

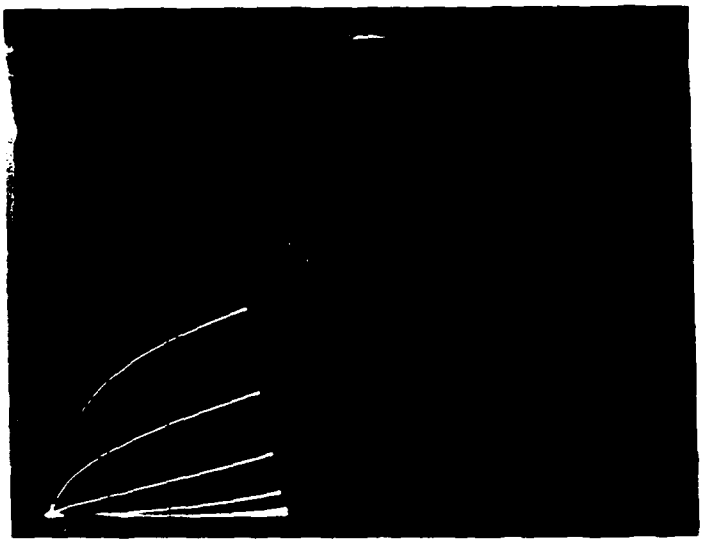


Fig. 3 High g_m for run EB 31.
(5 mA/div; 0.5 V/div; 0.2V/step)

input along a microstrip line, to simulate the required inductance. According to Alan Podell, a Varian consultant, this is a very lossy technique, and it seems probably that with the high Q input of the FETs (the mushroom gate of run EB 29 allowed an improvement in the input resistance of around a factor of 2.6), the low Q of the matching network does not permit an optimum noise match to be achieved at 8 GHz. Since the input Q will go down as the frequency is increased, a 26-GHz noise test setup is now being designed and assembled. At this high frequency, the large reduction in input resistance of these runs from that of EB 26 should manifest itself in a significantly lower noise figure, something very difficult to observe at 8 GHz.

III. BALANCED LOW-NOISE STRUCTURE (FIG. 2)

During this period, devices from runs #2 and #3 were evaluated. Figures 4 and 5 show the drain characteristics for two of the devices from run #2. The g_m's are 28-30 mmhos, and are the same as for the FETs using the structure of Fig. 1, which have the same total active Z = 150 μm device width and are fabricated on identical MBE material. The purpose of this balanced FET design is to match the dc characteristics of the FETs using the Fig. 1 structure, but to outperform them at rf frequencies by virtue of lower gate resistance, source inductance, and feedback capacitance in the balanced mode.

Since we have not yet developed the circuitry to provide balanced signals and balanced matching, rf measurements were made on several of the devices by connecting both drain and gate pads together and operating the FET as a 3-terminal device rather than in the balanced mode. Table IV gives the results of the measurements, made at 8 GHz.

TABLE IV

Balanced FET Performance in Single-Ended Mode at 8 GHz

Device	NF_m (dB)	G_a (dB)
BALFET 2-2	3.5	3.6
BALFET 2-3	3.1	4.5
BALFET 3-1 (common drain)	2.66	10.2
BALFET 3-2	3.6	3.2

These results are rather poor in light of the NF_m = 1-1.5 dB, G_a = 12-14 dB values obtained for the FETs using the Fig. 1 structure. Slightly poorer performance could be expected when operated single-endedly due to the increased feedback capacitance (ideally, it should be double so that

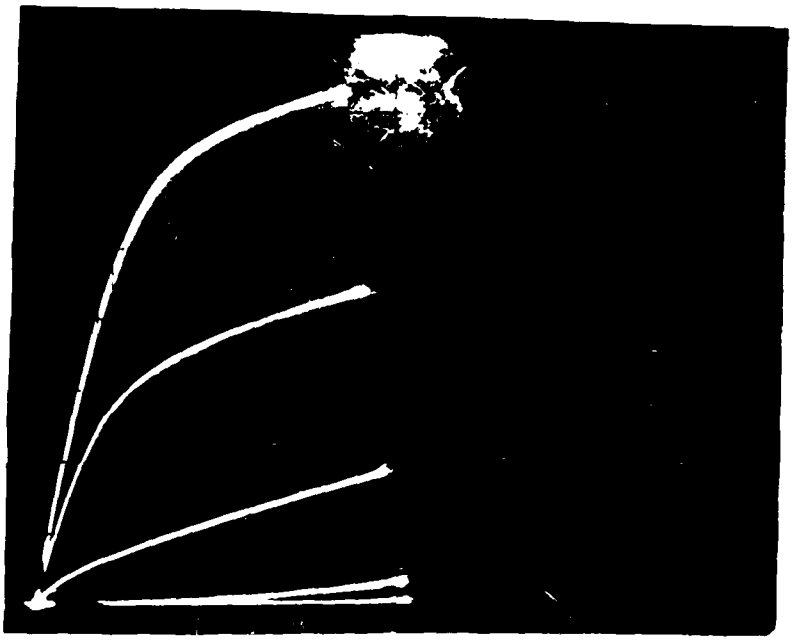


Fig. 4 Typical balanced FET drain characteristic.
(5 mA/div, 0.5 V/div, -0.5V/step)

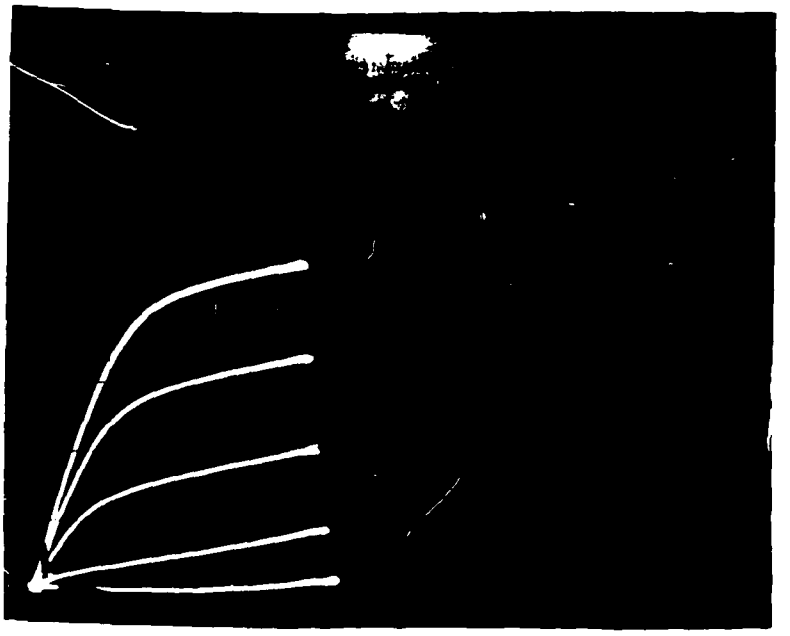


Fig. 5 Typical balanced FET drain characteristic.
(10 mA/div, 0.5V/div, -0.5V/step)

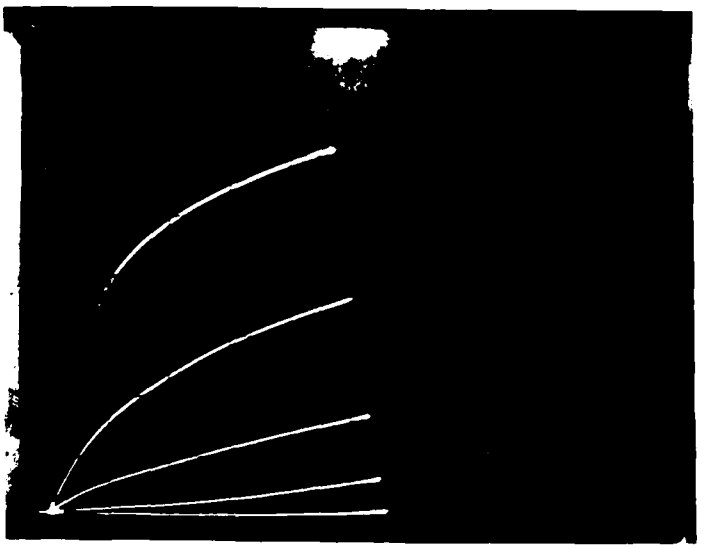
when operated in the balanced mode it will effectively be zero) and higher source inductance (due to the air bridge needed for the paralleling of the ten segments, which also should be effectively zero when operated in the balanced mode). However, the degradation indicated by the data in Table IV is unexpected.

The reason device 3-1 was bonded up in the common drain configuration is shown in Fig. 6, where an abnormal kink appears in the common-source characteristic, but is absent in the common-drain configuration. This phenomenon was typical of run #2 also, and becomes pronounced after bonding. Moving the wire leads to the curve tracer around did not change the drain characteristic, indicating that the phenomenon is an intrinsic property of the device and not simply an oscillation controlled by the lead wires as is often the case for low-noise FETs.

The yield was very low for run #3 because of shorting problems, perhaps because of the air bridge underplating the resist or misalignment of the dielectric squares. Consequently, it is not known whether device 3-1 gave superior results because of being bonded in the common drain configuration or because it was intrinsically a better device than 3-2.

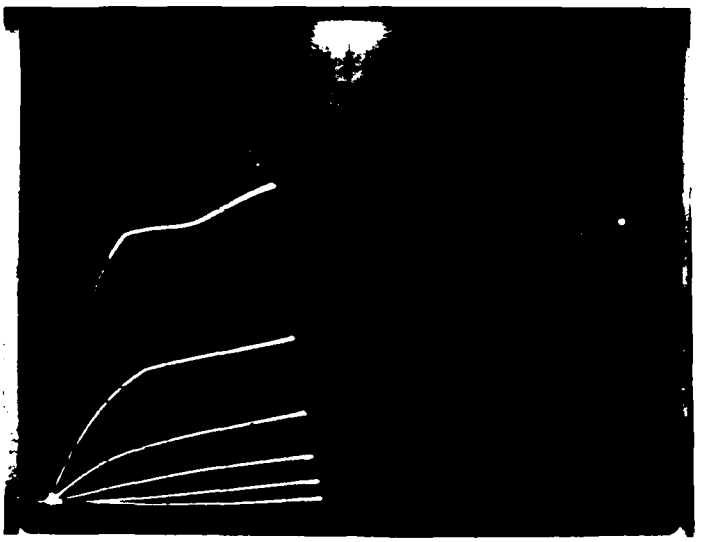
Runs #4 and #5 were also made during this period, but both had g_m compression. Device 5-2 gave NF_m = 3.85 dB and G_a = 4.7 dB at 8 GHz (common source), typical for the common source results for runs #2 and #3. However, although run #5 showed the same differences between common source and common drain configurations (as shown in Fig. 6), when bonded in the common drain configuration the rf results were no better than for the common source connection. This might suggest that device 3-1 would also have had a better performance in the common source connection.

S-parameters were measured on the balanced FETs whose rf performance was given in Table IV. Table V gives the y-parameters at 8 GHz



5 mA/div; 0.5V/div;
-0.5V/step
common drain

(a)



5 mA/div; 0.5V/div
-0.5V/step
common source

(b)

Fig. 6 Assymetry in the balanced FET's drain characteristics.
(a) common drain; (b) common source.

Table V seems to indicate that the low g_m for device 2-3 and the high g_{11} for device 3-2 are the main origins of inferior performance compared to device 3-1. It appears that the low g_m for device 2-3 occurred <u>after</u> the rf data was taken, so the y-parameters for device 2-3 may not be too meaningful, due to deterioration. It also appears that g_{11} and b_{12} are the reasons why device 3-1 does not match the performance of run EB 26. Table VII shows what happens to the maximum available gain MAG as computed from the y-parameters when g_{11} and b_{12} are adjusted for device 3-1 to match those of EB 26. Table VII reveals that both g_{11} <u>and</u> b_{12} are inhibiting performance and that <u>both</u> must be lowered to match the results for EB 26.

TABLE V

<u>BALFET 8-GHz y-Parameters</u>

	EB 26-4 V_d=3.5V V_g=0	EB 26-5	BALFET 3-1 V_d=2.5V V_g=0 Common Drain	BALFET 3-2 V_d=2.5V V_g=0	BALFET 2-3 V_d=2.5V V_g=0
g_{11} (mV)	0.986	1.02	2.58	9.0	0.883
b_{11} (mV)	10.2	11.7	16.3	17.6	8.4
g_{21} (mV)	17.6	20.1	25.8	17.2	7.05
b_{21} (mV)	-5.07	-5.39	-11.5	-22.9	-5.12
g_{12} (mV)	0.247	0.191	0.279	- 0.422	-0.397
b_{12} (mV)	-0.231	-0.212	- 1.76	- 8.05	-2.25
g_{22} (mV)	4.3	4.41	5.88	8.26	10.1
b_{22} (mV)	6.72	6.79	8.4	16.2	11.1
b_{12} @ 8 GHz	-0.166	-0.163	- 0.488	- 2.05	-0.619

for these devices along with the parameters for run EB 26 (using the conventional low-noise structure of Fig. 1) for purposes of comparison. Table VI reviews the rf performance of all these devices.

TABLE VI

8-GHz RF Performance

Device	NF_m	G_a
BALFET 2-3	3.1	4.5
BALFET 3-1	2.66	10.2
BALFET 3-2	3.6	3.2
EB 26-4	1.19	13.1
EB 26-5	1.19	13.2

TABLE VII

Computed MAG Values for BALFET 3-1

g_{11} (mV)	b_{12} (mV)	MAG (dB)
2.58	-1.76	12.0
2.58	-0.22	12.1
1.0	-1.76	12.0
1.0	-0.22	19.0

To allow more general conclusions, it is obvious that more devices need to be fabricated and tested. With device 3-1 common drain, device 3-2 common source, and device 2-3 degraded, it is hard to make any general statements about the y-parameters of the BALFET so far. It is worth noting that, from Table V, with the exception of b_{12} (by reason of the oxide crossovers), all the other y-parameters of run EB 26 can be matched by at least one BALFET, although not simultaneously.

IV. g_m COMPRESSION REVISITED

The reappearance of g_m compression in this reporting period was rather disconcerting. It seems to be more of a problem with the BALFET runs, but its solution will certainly benefit the conventional structure also. This marks the third time that this problem has been addressed on a relatively intensive scale. The first time (~1.5 years ago) it was seen only when easily oxidized metals (Ti or Al) were used. The solution in principle was straightforward -- use a good vacuum and make sure the wafer surface was free of water. However, the small overhung gate aperture and the possibility that the PMMA might outgas water indefinitely might have been at least partially responsible for the small vestige of g_m compression that persisted. With the use of Au gates, g_m compression had never been seen until about 8 months ago. By trial and error, it appeared at that time (and until now) that a BOE (buffered HF oxide etchant) etch prior to evaporation was sufficient to eliminate g_m compression with Au gates. Recently however, apparently spontaneously, even the BOE dip has been found to not be sufficient. Perhaps its disappearance some months ago was coincidental and unrelated to the use of BOE. Possibly a new mechanism for g_m compression has entered the picture.

The following is a brief listing of procedures tried during this period which however failed to solve the problem.

- Long pumpdown (3-4 x 10^{-7} Torr) and a rapid Au evaporation
- H_2O_2 after the citric acid etch
- Ammonia etch in place of the citric acid etch (basic etch rather than acidic etch, and inorganic rather than organic)
- Wafer with no n^+ layer so no citric acid etch needed
- Use of 100 Å of Au-Ge before the Au to aid adhesion in case g_m compression is related to lack of adhesion of the Au
- Elimination of the Triton X-100 wetting solution.

Also, it seemed that some MBE wafers were more prone to g_m compression than others, but no differences could be found from the growth run sheets.

One procedure that appeared to eliminate g_m compression was a plasma descum in oxygen after the channel etch followed by a BOE etch. Both the descum and the BOE were needed. g_m compression has not resulted since this process has been instituted. Since it isn't clear why an O_2 descum is needed after the channel etch, it isn't certain whether the descum is actually needed, or whether some other, unresolved factor(s) are at work.

Another cause for g_m compression was found to be a submicroscopic break in the gate metallization leg that connects the gate to the gate pad at the point where the leg crosses the edge of the gate pad. Evidently, the citric acid undercuts the gate pad metallization to provide an overhang which results in a break in the metallization. For any given device, this cause for g_m compression can be remedied by running a probe tip across the break area. Thicker gate metallization and/or reversal of the gate and gate pad metallizations should remedy this problem in the future.

In summary, three causes for g_m compression have been identified to date: (1) the gettering of O_2 by Al and Ti, (2) breaks in the gate connection to the gate pad, and (3) a cause which occurs even for Au gates and which, for the present, seems to be eliminated by a plasma descum and BOE etch following the channel etch. Some of the frustrations in the past in solving g_m compression may have been due to attributing it to a single cause, when in reality various combinations of the above were occurring.

V. CONCLUSION

For the conventional low-noise structure of Fig. 1, many device runs were made during this period using a baffled gate evaporation in place of the lower-yield mushroom gate profile. Although the gate resistance was slightly higher than with the mushroom profile, it was low enough to maintain the low noise figures of the mushroom profile devices. The uniformity of the rf performance (1.0-1.2 dB noise figure with an associated gain of 13-14 dB at 8 GHz) suggests that either some sort of fundamental limit on device performance has been achieved, or that some limit in the measurement technique has been reached. Since lower values of noise figure were expected, closer investigation of device parameters is indicated, along with increasing the measurement frequency to possibly improve the matching. During this period, evidence was gathered to suggest that electron-beam damage of the channel is not a problem. The intention is to fabricate devices on OM (organometallic) VPE materials to determine what limits on device performance the material might play. Unlike ion-implantation, LPE, or chloride-transport VPE, OM-VPE can reproduce the sharp step transistions in doping, characteristic of MBE material.

During this period, several balanced FETs were evaluated. While yielding analogous dc characteristics to the conventional low-noise-structure device, the rf performance was relatively poor when tested in the single-ended mode. When these devices were s-parameter tested, all of the devices were found to be different, but in general, deficiencies in g_{11} and b_{12} appeared to limit the gain performance. More devices need to be fabricated and tested before problem areas can be identified with confidence. One encouraging feature is that, with the exception of b_{12} (due to oxide crossovers), all the other y-parameters of the single-ended run EB 26 can be matched by at least one BALFET, unfortunately not simultaneously.

The problem of g_m compression recurred in this period, and appears to have been eliminated by instituting both a plasma descum and an HF etch prior to the gate metal deposition. It was also discovered that a break in the metallization connecting the gate to the gate pad can also give g_m compression. This problem can be solved by either thicker metallization or by reversing the gate and gate pad metallizations.

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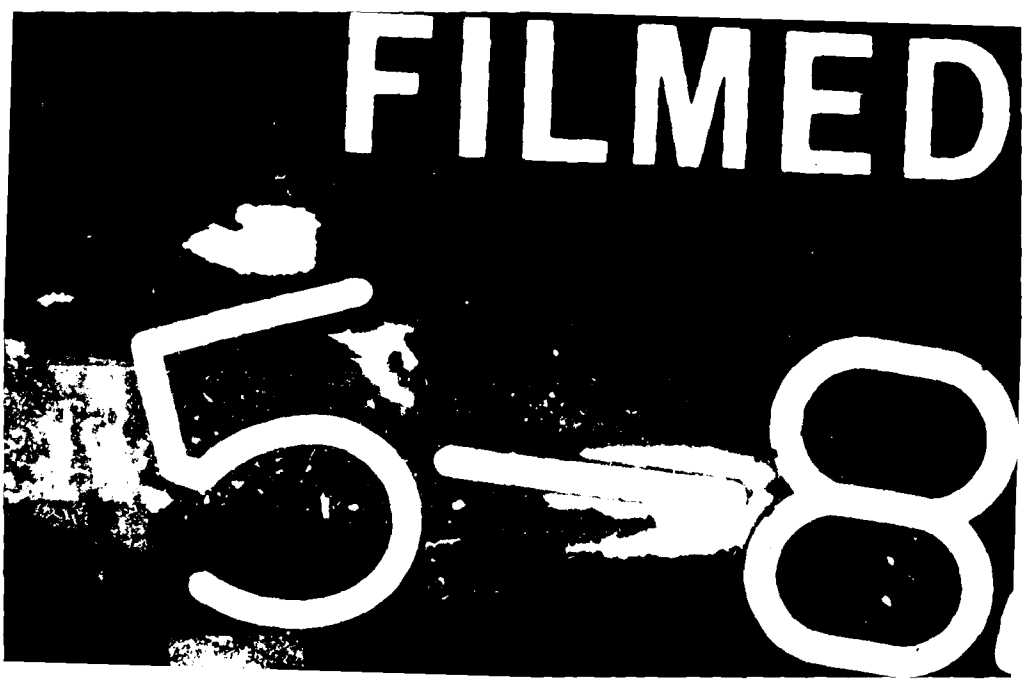
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