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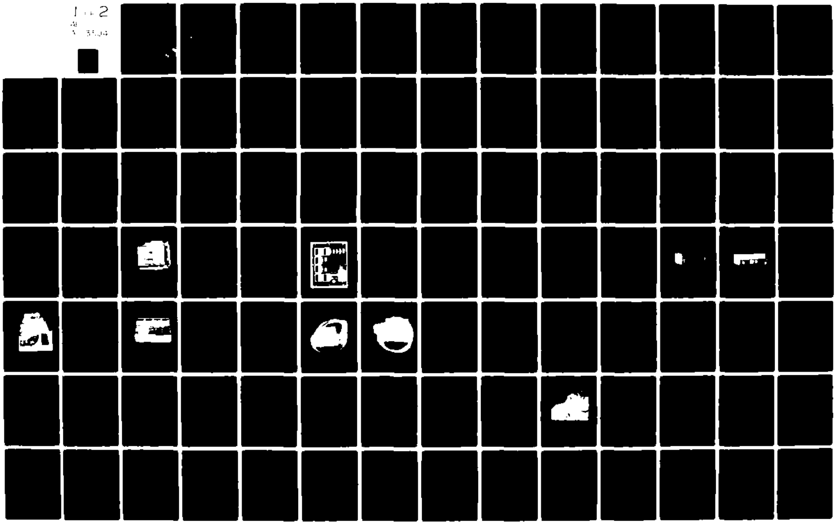

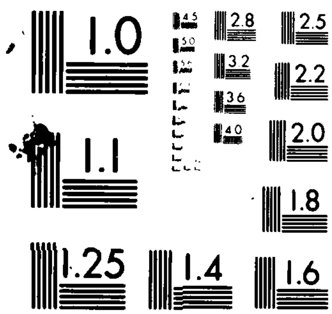
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REPORT SD-TR-81-86

SD/LDEF Technical User's Manual

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El Segundo, Calif. 90245

30 September 1981

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This report has been reviewed by the Public Affairs Office (PAS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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SD 802 Spacecraft Mate. als Experiment
Test Plan

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Aerospace Materials Sciences Laboratory (MSL) has the technical responsibility for the Space Division experiment on the Long Duration Exposure Facility to be flown on the Space Shuttle. MSL's primary function is to mechanically integrate the Space Division subexperiment packages to the satellite vehicle and to provide a flight electronics system to retrieve and store data from the subexperiments.

This report provides a complete review of the flight and ground support electronics with an emphasis on documenting the electronics programming particular to this

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19. KEY WORDS (Continued)

20. ABSTRACT (Continued)

mission. The electronics fabricated by MSL and the test plan for the hardware flight qualification tests from component to system levels are documented. Appendix A gives a breakdown of the transducers used and their locations so that these data can be easily shared among the many experimenters.

PREFACE

Many people within the Materials Sciences Laboratory and other laboratories contributed to this project. Among the most significant contributors were the following.

P. Schall was principal investigator, with specific responsibility for thermal calculations and for the computer hardware and software interface.

A. F. DiGiacomo coordinated the subexperiment arrivals, their mechanical integration into the LDEF trays, and the vibration tests.

W. C. Burns was responsible for the design, fabrication, and test of the Aerospace electronics.

R. P. Giguere was consultant on the electronics design, testing, and documentation.

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FIGURES

FIGURES (Continued)

TABLES

1. INTRODUCTION

This report describes the flight electronics and ground support hardware fabricated by The Aerospace Corporation for the Long Duration Exposure Facility (LDEF) experiment to be flown on Space Shuttle. The report will serve as the test plan for the hardware flight qualification test at the component and subsystem levels. Enough detail is provided so that a competent, though unfamiliar, experimenter can follow the operation of the experiment during the ground support and flight test phases. This report incorporates material from the Experiment Power and Data System (EPDS) users manual (Ref. 1), the LDEF handbook (Ref. 2), and other documents listed in the Reference section to detail the overall experiment without the need for constant referral to the subsystem references.

1.1 MISSION

The data recording network for the LDEF project is designed to collect data from various materials being exposed to the low orbit space environment and to store these data on magnetic tape for future retrieval. Data from the experiments are scanned once every 3.49 min for 32 consecutive scans. This burst cycle is repeated every 93.16 hr throughout the mission. The data recording network is programmed to turn itself off 367 days after startup.

1.2 ELECTRICAL COMPONENTS

The recording network consists of duplicate electronic packages for the leading and trailing edge trays. Each data recording package consists of an EPDS supplied by NASA, an Aerospace-designed signal conditioning unit (SCU), ground support equipment (GSE), batteries for power, and numerous transducers attached to the experimental materials.

1.2.1 Experiment Power and Data System

The EPDS consists of a data processor controller assembly (DPCA), a magnetic tape memory system (MTM), and a primary battery power source. The DPCA is hard-wire programmable to accommodate a variety of data collection needs. The system operates from primary batteries. Designs have been selected to minimize power requirements. Data from the experiment are a mix of high-level analog, low-level analog, and parallel digital signals. The MTM provides storage for about 14 megabits of data.

1.2.2 Transducers and the Signal Conditioning Unit

The transducers (supplied by Aerospace) consist of strain gauges, thermistors, and solar cell power monitor circuits. Data are also obtained from a Boeing fiber optics experiment and Berkeley Controls quartz crystal monitor (QCM). The SCU applies power to the experiments and conditions these data to be compatible with EPDS. In addition, the SCU provides the warm-up and shut-down timing for the experiments.

1.2.3 Ground Support Equipment

The NASA-furnished GSE consists of a Kennedy tape transport to generate a computer compatible tape (CCT), a magnetic tape memory reproducer to manually control the MTM, and a data display box (DDB) to monitor the DPCA data activity. Aerospace is providing the simulated loads, the external power supply for the SCU, the pulse command sequencer to initiate the scanning cycles, and the microcomputer hardware and software to read and transcribe the CCT.

2. DETAILS OF ELECTRONIC COMPONENTS

2.1 EXPERIMENT POWER AND DATA SYSTEM

2.1.1 Magnetic Tape Memory

Normally, EPDS collects, digitizes (if necessary), and stores the experimental data in its buffer memory. At programmed times, the buffer memory is transferred to magnetic tape. The tape recorder is a two track, direct record, hermetically sealed recorder. The recorder starts on track 1 and records serially until the end of the tape is sensed. Internal recorder logic automatically stops the tape, switches to track 2, and reverses the direction of the tape so the recording continues on track 2. During this transfer, from one to three 4K (4096-bit) buffer memory dumps are lost. The recording on track 2 continues until the recorder circuitry senses the beginning of the tape, at which time the recorder stops and accepts no further data.

The recorder tape moves at 2 in./sec and records data at a rate of 4K bits/sec. Since each start-stop cycle requires about 1 in. of tape, each 4K memory dump uses 3 in. of tape. The magnetic tape length is 450 ft, about 1800 dumps per track, or 7×10^6 bits/track of storage for a single buffer memory dump per record cycle. The total possible run time for our recorder is approximately 435 days, which is more than the 367-day limit set by the data processor controller assembly (DPCA) electronic counter.

The tape recorder has record electronics only. Normal recovery of recorded data requires the use of the ground support equipment (GSE) data display box, an MTM controller, and the transcription of the data onto a computer compatible tape (the recorder tape is not removable).

Two techniques for detecting the end of a data block are: (1) use of a unique order of bits that would not be found in the data pattern and (2) counting the number of clock pulses for each data block and gating off data when the required number is reached. Our software uses only the first method with the unique 24-bit sync signal that starts each data set. In addition, the decoding software senses the beginning of tape and end of tape marks.

On initial flight MTMs tested, errors occurred in leading bits (up to 20) of each reproduced memory dump sequence. Appropriate changes have been made to the 4K buffer board to provide precursor leading zeros to the MTM at the start of each memory dump sequence. This change will ensure there are no leading bit errors. The use of the MTM tape capacity is not affected, because the precursor bits occur in a time period allotted for the MTM to come up to speed. The software has provisions for ignoring these leading zeros in the reproduced data.

2.1.2 Data Processor Controller Assembly

The DPCA provides the EPDS signal interface to the signal conditioning unit (SCU), all the EPDS timing and controls, and control of the MTM (Fig. 2-1). The general programming questionnaire (Tables 2-1 and 2-2) summarizes the programming for both the leading and trailing edge EPDS units. A brief explanation of these features follows.

2.1.2.1 Analog Inputs

The DPCA accepts both high-level (±5 V differential) and low-level (±10 mV differential) analog inputs. In this mission, all 64 available analog channels are used. Fifty-seven channels are high level, and seven channels are low level. All signals share a common differential multiplexer. The sum of the common-mode voltage plus the peak-input signal cannot exceed ±5.5 V. All analog inputs are bipolar relative to the signal ground, have a differential impedance greater than 5 megohms, and have fixed gains. The measurement resolution is equivalent to 1 in 1024 (10 bits). This 10-bit resolution is the same for all inputs and sets the EPDS word size to 10 bits for all words.

2.1.2.2 Digital Inputs

The DPCA will accept up to a maximum of 24 parallel discrete digital inputs. However, our word size of 10 bits fixes the maximum number of usable digital inputs at 20, or 2 words. The four remaining bits are not used, although they remain initialized throughout the mission. All inputs are compatible with the EPDS 7.5-V battery powered complementary metal oxide

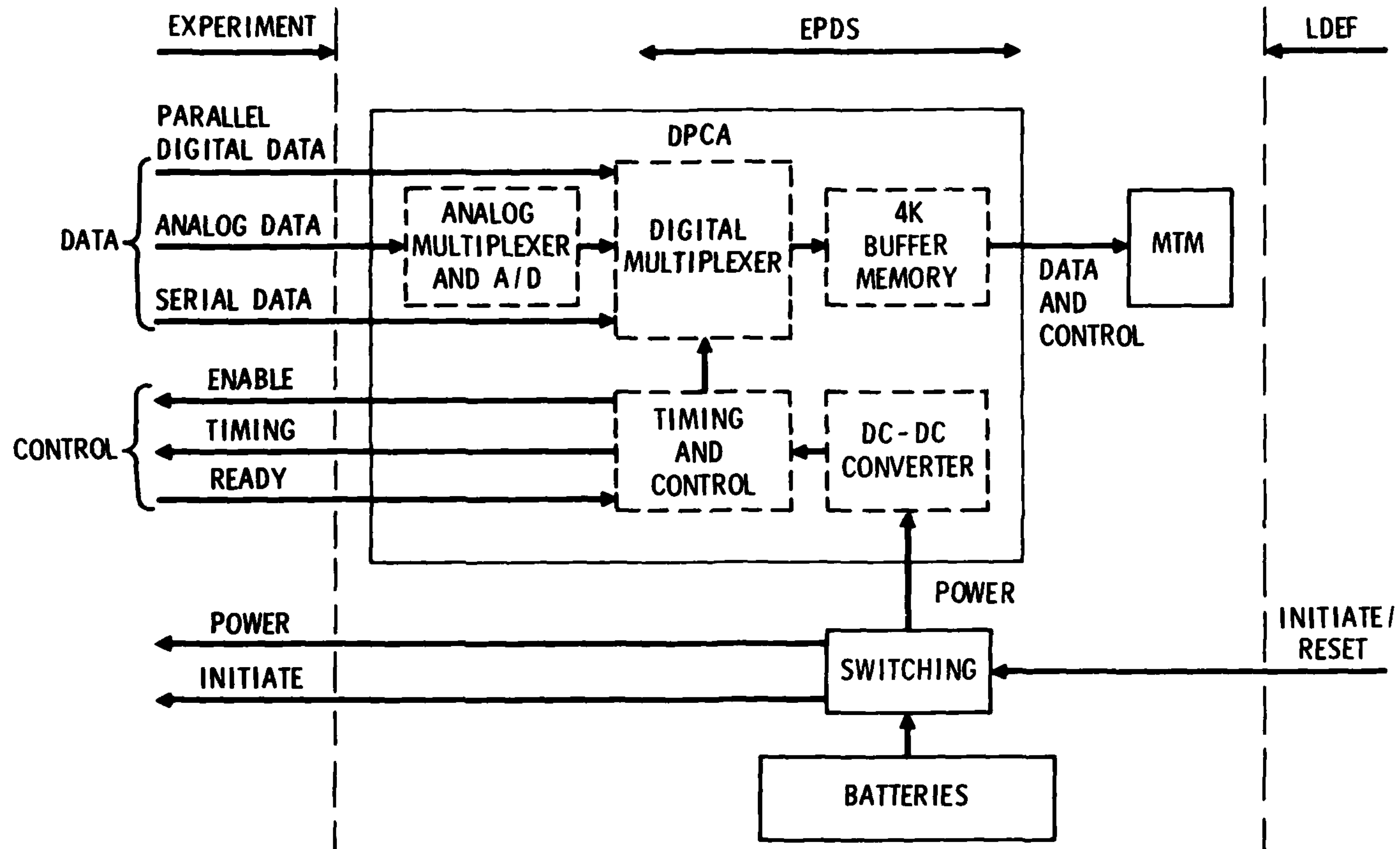


Fig. 2-1. EPDS Block Diagram (From Ref. 1)

Table 2-1. M0003 SD-802 Spacecraft Material Leading Edge Unit

EPDS Programming Questionnaire

E1 = 8807 hours or 9450 counts (0.932 hr/count)

E2 = 8807 hours or 9450 counts (0.932 hr/count)

E3 = 3.49 minutes or 4 counts (52.4 sec/count)

E4 = 174.7 minutes or 200 counts (52.4 sec/count)

CON1 = Logic "0"

Number of Data Scans/Enable = 5 .

Will the DEC Input be:

(a) Hard-wired to Logic "1" or

(b) Will it be driven by Experiment Logic? Yes

Number of Bits/Word = 10. (resolution)

Does the experiment require a start-up delay at the beginning of each scan? Yes How many seconds? 20

How many words of sync code? 3

Desired sync code 1111 1010 1111 0011 0010 0000 (in binary, 24 bits maximum)

How many words of time code? 3

How many words of serial digital data? 0

How many words of low-level analog data? 7

How many words of high-level analog data? 57

How many words of parallel digital data (or post sync)? 2

Desired post sync code = NONE (in binary, 24 bits maximum)

What is the number of bits/scan? 720 (4096 bits maximum)

What is the number of data scans to be loaded into the buffer memory? 5 (data scans/dump)

How many times will the contents of the buffer memory be written in a single block on tape? 1 (memory dumps)

Data Scan Sequence: SYNC, time, parallel digital, low-level analog, and high-level analog data.

Table 2-2. M0003 SD - 802 Spacecraft Material
Trailing Edge Unit

EPDS Programming Questionnaire

E1 = 8807 hours or 9450 counts (0.932 hr/count)

E2 = 8807 hours or 9450 counts (0.932 hr/count)

E3 = 3.49 minutes or 4 counts (52.4 sec/count)

E4 = 174.7 minutes or 200 counts (52.4 sec/count)

CON1 = Logic "0"

Number of Data Scans/Enable = 5 .

Will the DEC Input be:

(a)Hard-wired to Logic "1" or

(b)Will it be driven by Experiment Logic? Yes

Number of Bits/Word = 10. (resolution)

Does the experiment require a start-up delay at the beginning of each scan?

Yes How many seconds? 20

How many words of sync code? 3

Desired sync code = 0000 0101 0000 1100 1101 1111 (in binary, 24 bits maximum)

How many words of time code? 3

How many words of serial digital data? 0

How many words of low-level analog data? 7

How many words of high-level analog data? 57

How many words of parallel digital data (or post sync)? 1

Desired post sync code = None (in binary, 24 bits maximum)

What is the number of bits/scan? 720 (4096 bits maximum)

What is the number of data scans to be loaded into the buffer memory? 5 (data scans/dump)

How many times will the contents of the buffer memory be written in a single block on tape? 1 (memory dumps)

Data Scan Sequence: SYNC, time, parallel digital, low level analog, and high-level analog data.

semiconductor (CMOS) (i. e., V_{DD} = 7.5 V, V_{GG} = ground). Since there are no serial digital data generated by the experiment, the DPCA is programmed to reject all serial digital data.

2.1.2.3 Synchronization Pattern (SYNC)

The DPCA provides a synchronization pattern with each data scan to assist in data recognition. The pattern and number of bits are programmed into the DPCA as three words. Only the first 24 bits of these words are programmable. The patterns for the leading edge and trailing edge DPCAs are listed in Tables 2-1 and 2-2. Leading zeros (up to 20) precede the synchronization pattern for each reproduced memory dump sequence. No postsynchronization code is used for these units.

2.1.2.4 Time

The DPCA has a 24-bit, binary counter driven by a precision oscillator that sets time relative to the "initiate" signal sent by the Shuttle prior to LDEF deployment. The oscillator and counter are continuously powered. The rate at which the counter is incremented is approximately 0.61 Hz ($1.28 \times 10^6 \div 2^{21}$). A period of 318.15 days (the capacity of the 24-bit counter) passes before the counter recycles. The entire contents of the counter requires three words (30 bits) and follows the synchronization code in the data block. The timing accuracy is expected to be ±40 parts per million, when all effects of temperature and aging are considered.

2.1.2.5 Data Scan

A data scan is one sampling of all measurements. EPDS is hard-wire programmed to provide five consecutive data scans during a data enable period. Multiple, consecutive data scans offer a means of statistically reducing noise errors if the data do not change during the sampling interval. The order of data in a scan is SYNC, time, parallel digital data, low-level analog data, and high-level analog data. The low-level data must precede the high-level, and at least one analog measurement must be low level. Through hard-wire programming by NASA, the experimenter determines the data scanned and the number of words in each type of data. It is not necessary to scan all types of data.

2.1.2.6 Buffer Memory

The EPDS provides a 4K bit static CMOS random access memory (RAM) to accumulate data and provide more efficient use of the magnetic tape. On the basis of the number of bits in a data scan, the experimenter determines how many complete data scans can be stored in 4K bits. This number is hard-wire programmed into the buffer memory circuitry by NASA. When the memory has stored this number of data scans, a memory readout cycle is initiated and the entire 4K bits are recorded on magnetic tape. Since the total number of data bits is less than 4K, undefined filler bits will be found on the magnetic tape. Our number of data scans between memory dumps does not permit the memory capacity to be exceeded. For these units, we have a total of 72 words per scan (3 synchronization + 3 timing + 64 analog + 2 parallel digital words = 72 words) and have five data scans per memory dump without overwriting the memory (72 words/scan × 10 bits/word × 5 scans/dump = 3600 bits per dump). After the memory dump sequence has been initiated, all data inputs are ignored until the readout dump cycle is complete. We have chosen to read the buffer memory onto the magnetic tape only once during a single dump cycle.

2.1.2.7 Voltage Reference

During a scan cycle, EPDS provides two stable reference voltages (nominally ±5.0 V) from the internal analog-to-digital (A/D) converter. Circuit current loading by the experimenter is less than 1 mA.

2.1.2.8 Initiate Circuit

Prior to LDEF deployment, the Shuttle sends an electrical "initiate" or "set" signal to LDEF (through an umbilical), which effectively permits the application of primary power to the electrically operating experiments. After LDEF retrieval and reconnection of the umbilical, the Shuttle sends a "reset" signal, which removes power from experiments for the return to earth. To accommodate these signals, a magnetic latching relay is located within EPDS. The previously unused relay contacts are used to make connections to the experiment batteries. Connections to these experimenter contacts are on connector P752. Another set of contacts is reserved for a function monitor circuit in the LDEF data system that records contact closure within the experiment. Pins G and H of the connector are reserved for an LDEF continuity circuit used to ensure positive mating of the connector before flight. These connections to LDEF are through connector P753.

In EPDS, one set of the initiate relay contacts is used to connect the DPCA to the 7.5-V battery. When contacts are closed, 7.5 V are applied to the DPCA and an "initial reset" (IRST) occurs, which forces all logic functions and counters into a known state. All EPDS time measurements are relative to receipt of the "set" signal. The initiate relay results in all time measurements being reset to zero.

2.1.2.9 Data Enable Lines

EPDS provides four 7.5-V CMOS compatible lines to the experimenter to permit the experiment and EPDS to enter into a data collecting mode. The lines are called decision enable (DEC ENA), decision (DEC), enable (EBL), and decision disable (DEC DBL). At each data enable period, determined by the program counters, EPDS provides a 20 to 30 msec wide DEC ENA pulse that instructs the experiment to go into a data scan. The data-taking portion of EPDS is not powered up at this time. After a 20-sec warm-up period, the SCU provides a level signal on DEC notifying EPDS that it is ready to provide data. EPDS concurrently continues to sample the status of DEC every 51.2 msec. If a signal has not been provided by the experiment in 112 min, the data-taking portion of EPDS will be automatically powered up and a normal data scan initiated, thus completing the cycle. EPDS provides an EBL level signal coincident with receiving the DEC pulse that starts the data scan. The EBL level signal remains high until all data scans have been completed. On the trailing edge of the EBL level signal, a 20 to 30 msec wide DEC DBL signal is provided to the experiment to turn off the data recording system until the next DEC ENA pulse.

2.1.2.10 Program Counters

EPDS provides four hard-wire programmable internal counters to establish the data enable periods. These counters have a four-decade capacity and are driven from a precision oscillator. The counters are preset to the programmed count at the initialization of the EPDS and count down to zero.

The counters are identified as E1 through E4. Counters E1 and E2 are one-time event counters, are decremented at a nominal rate of once per 0.932 hr ($2^{32} \div 1.28 \times 10^6$ Hz) and are usable over a count of 3 to 9999 (counts of 0 through 2 are not usable). E3 and E4 are cyclic counters decremented at a nominal rate of once every 52.4 sec ($2^{26} \div 1.28 \times 10^6$ Hz) with a usable range of 3 to 9999. On reaching a zero count, E3 or E4 is automatically preset to the programmed count and the cycle is continuously repeated.

Modification No. 1 to the EPDS permits these units to take 32 equally spaced DEC ENA signals at programmed intervals. The 32 DEC ENA signals are spaced at 3.49-min (E_3) intervals and provide equal sampling over a span of 111.8 min (slightly longer than the LDEF orbital period). These 32 data scans are then repeated at 93.16 hr (E4 x 32) intervals (Fig. 2-2).

The control line (CON1) in the EPDS is hard-wired low, and this mode predetermines when the first data scan starts and when all further EBL pulses are inhibited. In this mode, the cyclic counter E3 controls the DEC ENA pulse, if events E1 (367 days) and E2 (367 days) have not occurred. When event E2 occurs, all further DEC ENA pulses are inhibited. Since in this mode E1 and E2 are equal, counter E1 cannot transfer control of the DEC ENA pulses to the cyclic counter E4, as it would if E1 were less than E2. CMOS signal pulses (7.5 V) are provided from EPDS on the leading edge of the E1 and E2 events to facilitate experiment control. This modification No. 1 is designed to initiate a burst of 32 data scans immediately after EPDS initialization by LDEF and on the falling edge of every thirty-second E4 pulse that follows. The elapsed time from initialization to the first DEC ENA is 3-1/2 counts (E3), or 3.06 min. The full E3 count (3.49 min) is the time period between data scans within a burst. The options available with these counters are described in Ref. 1.

2.1.2.11 Programmed Inputs

All digital inputs to EPDS are wired to either a logic 1 or 0 (+7.5 V or ground), even though the inputs might not be used by the experiment. This requirement is applicable to parallel and serial digital data, programming connectors on the DPCA printed circuit cards, word counter flip-flops,

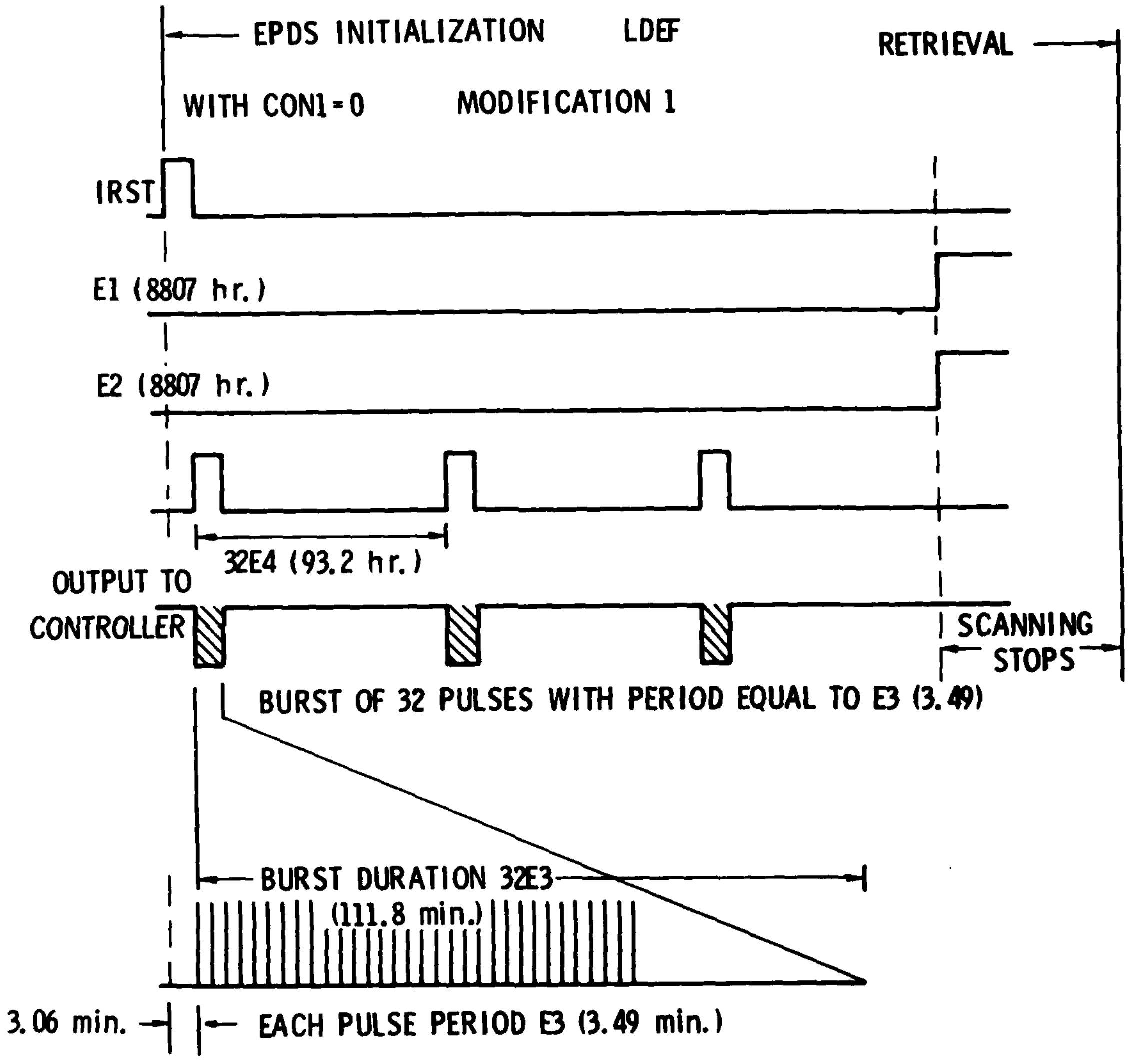


Fig. 2-2. Program Counters Commands

and certain externally programmed inputs such as CON1, CON2, and $\overline{C_T}$. All unused analog inputs are connected to analog ground. Unconnected (floating) inputs on CMOS circuit devices tend to put the device in a linear conduction region, causing excessive and damaging electrical stresses and heating to the CMOS devices.

2.2 BATTERIES

The batteries for EPDS and the experiment are of the lithium/sulfur dioxide (Li/SO_2) type. For EPDS a nominal 7.5-V battery (6.0 to 9.0 V) provides power for the data processor controller electronics, and a nominal 12-V (10.5 to 15 V) battery provides power for the EPDS magnetic tape module. Two additional 12-V batteries power the experiments and the SCU. Regulators within the SCU stabilize the actual voltages used as the battery voltage varies over time.

Battery capacities are a function of temperature and discharge rate. The curves in Fig. 2-3 illustrate the way in which the capacity of one cell is affected by both the rate of discharge and the temperature. The 7.5- and 12-V batteries have internal paralleling of four and two cells, respectively. The point at which cell voltage drops to 2.0 V (Fig. 2-4) determines the cell capacity for a steady-state discharge at constant temperature. For the NASA safety factor, it is assumed that the battery system does not exceed 75% of its rated capacity during the combined requirements of testing and experiment lifetime. Using NASA criteria, the safety limit is calculated to be 12 A hr. The calculations of Table 2-3 estimate that only 6.67 and 2.32 A hr will be required for a 400-day mission from experiment batteries No. 1 and 2. If the EPDS power-down signal fails, the power estimates increase to 10.75 and 4.64 A hr. All estimates are within NASA safety limits.

A phenomenon associated with the lithium battery is that of low initial voltage after storage or very light duty. Battery voltage will drop to a relatively low level and then recover. The available turn-on voltage is affected by the operating and storage temperatures, past and present battery loading, and the overall duty cycle. Ground test personnel must be aware of this phenomenon during qualification tests and checkouts, especially if the

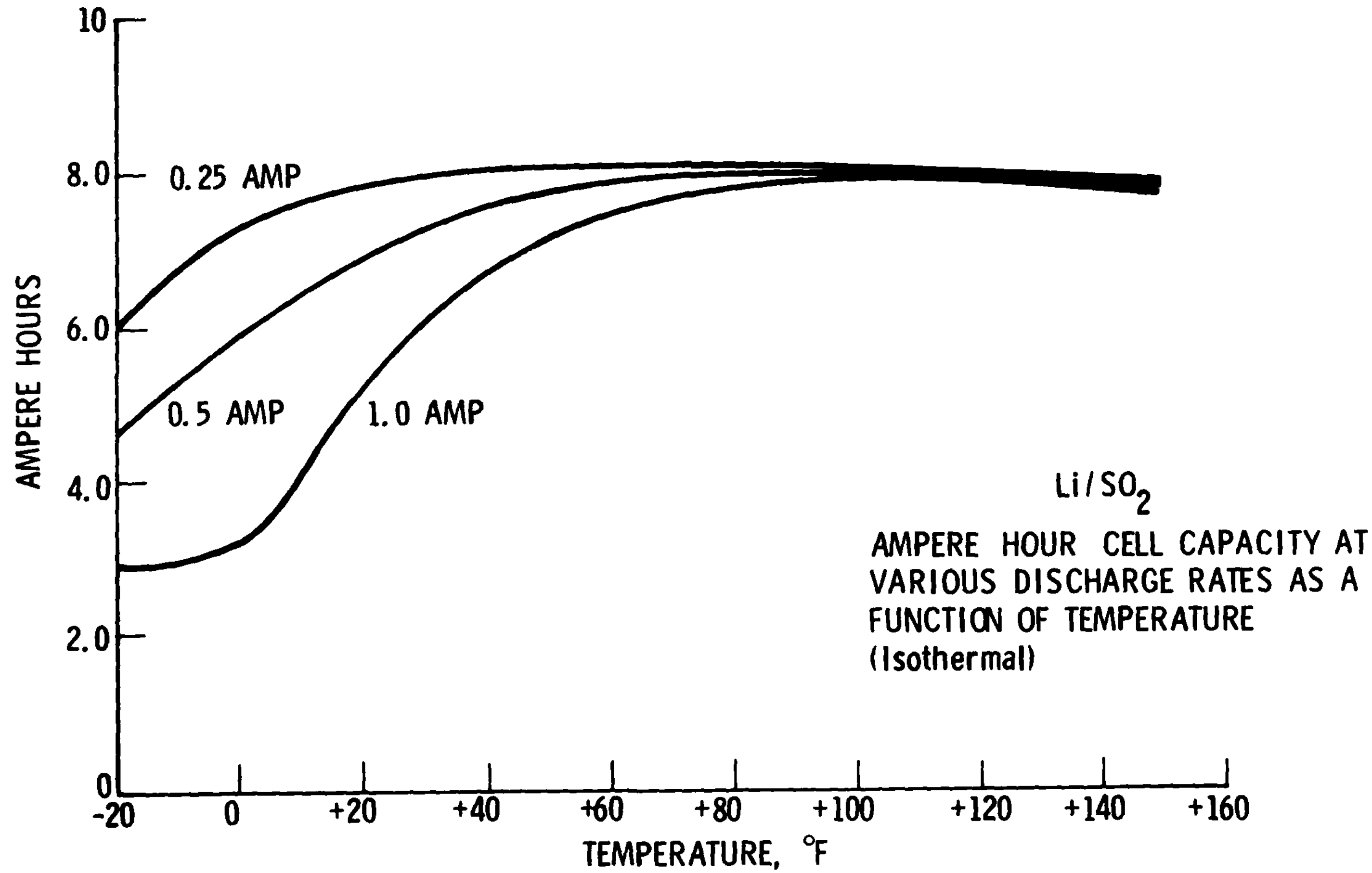


Fig. 2-3. Battery Cell Capacity (From Ref. 1)

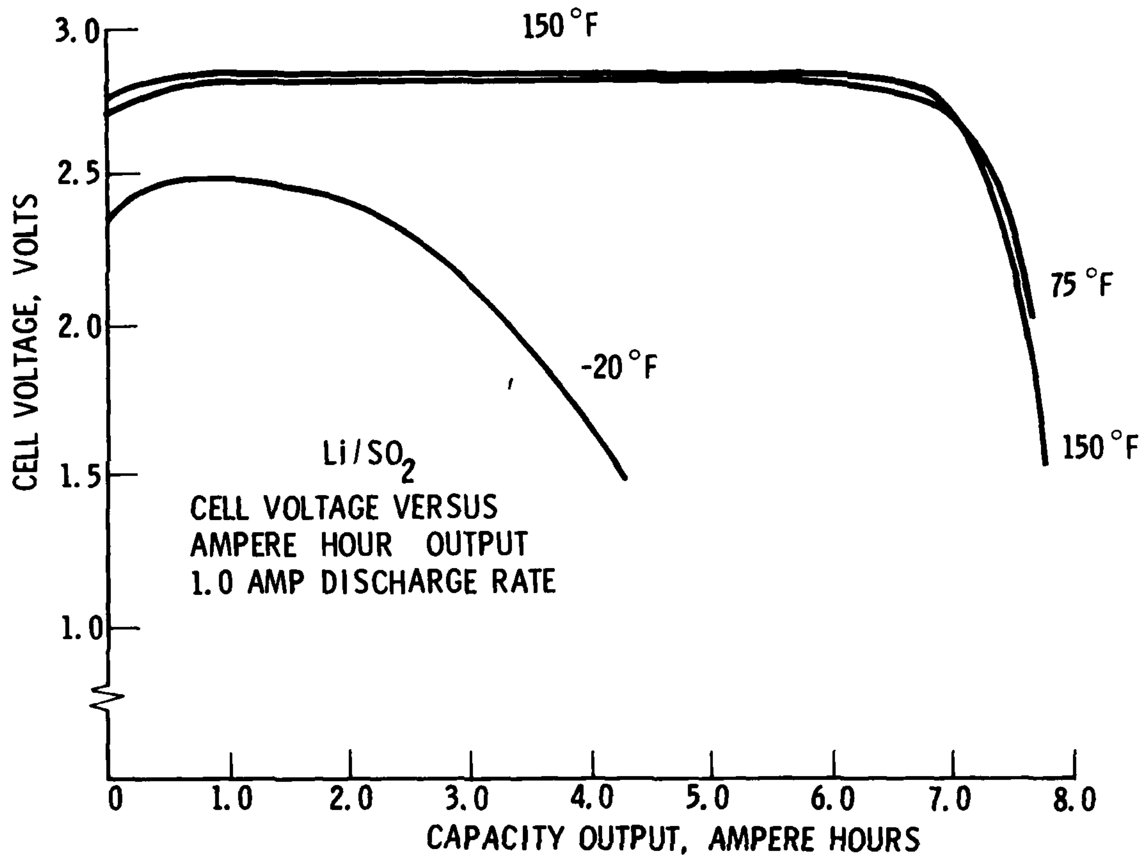


Fig. 2-4. Cell Voltage versus Capacity (From Ref. 1)

Table 2-3. Estimates of Battery Ampere Hours Used During Mision[a]

Battery No. 1, +12 V			
State	Current[b]	On Time	A hr
Standby	270 A	9600 hr	2.59
Power-up[d]	220 mA	18.55 hr	4.08
Power-down	33 mA	9.027 hr	0.00
Total			6.67

Battery No. 2, -12 V			
State	Current[c]	On Time	A hr
Standby	0	0	
Power-up[d]	125 mA	18.55 hr	2.32
Power-down	0	0	
Total			2.32

[a]Estimates are for a 400-day mission.
[b]Test Voltage = +13.139 V
[c]Test Voltage = -13.34 V
[d]If the EPDS power-down signal fails to shut down the SCU and experiments, an internal SCU timer will take over the power-down timing, resulting in an increase up to a factor of 2 of the total on time and power-up ampere-hours for the mission.

warm-up time is short or if the battery is operated after a long storage period. A deep discharge for a brief period will stabilize the battery voltage. Refer to the EPDS manual battery section for further details before attempting this discharge.

2.3 EXPERIMENT INSTRUMENTATION

The signal conditioning system consists of transducers in the experimental trays, batteries for powering the experiments, and a buffer circuity for interfacing the signals from the transducers with EPDS. The batteries are two 12-V Li/SO_2 units of the same type as described in Section 2.2 Details of the types of transducers used and of the SCU follow.

2.3.1 Transducers

The transducers supplied by Aerospace consist of strain gauges, thermistors, and circuits used to monitor solar cell power. The 20 strain gauges in each tray system are Micro-Measurements model ED-DY-125TQ-10C. Their useful temperature range is from -100 to 350°F, and their strain level range is approximately ±2000 microstrains. The characteristic resistance for these gauges is 1000 ohm ±0.5%. Each strain gauge is connected in a simple bridge circuit (Fig. 2-5a), in which the output difference is amplified by a low-noise amplifier (Harris 2730-8). The gain of these amplifiers is set such that a 1-microstrain signal will result in a 1-mV output from the amplifiers to EPDS high-level analog inputs. All 20 of these amplifiers are located within the SCU enclosure. The temperature drift of these amplifiers ranges from -3 mV/°C to +7.5 mV/°C. Each 10 amplifiers share a common heat sink with temperature monitored by thermistors (channels 43 and 44). The drift of each amplifier over the operating temperature range was recorded during SCU thermal-vacuum qualification tests. By compensating for these drifts in the data reduction process, more accurate strain measurements are possible.

The solar cell power monitor circuit (Fig. 2-6) in the SCU measures the voltage developed by the short-circuit current of the cell through a 0.05-ohm resistor. Normally, a flux level of 1 sun incident on one of these cells generates a short circuit current of 160 mA and a corresponding voltage of 8 mV. The voltage data are transmitted to EPDS as low-level analog signals for storage.

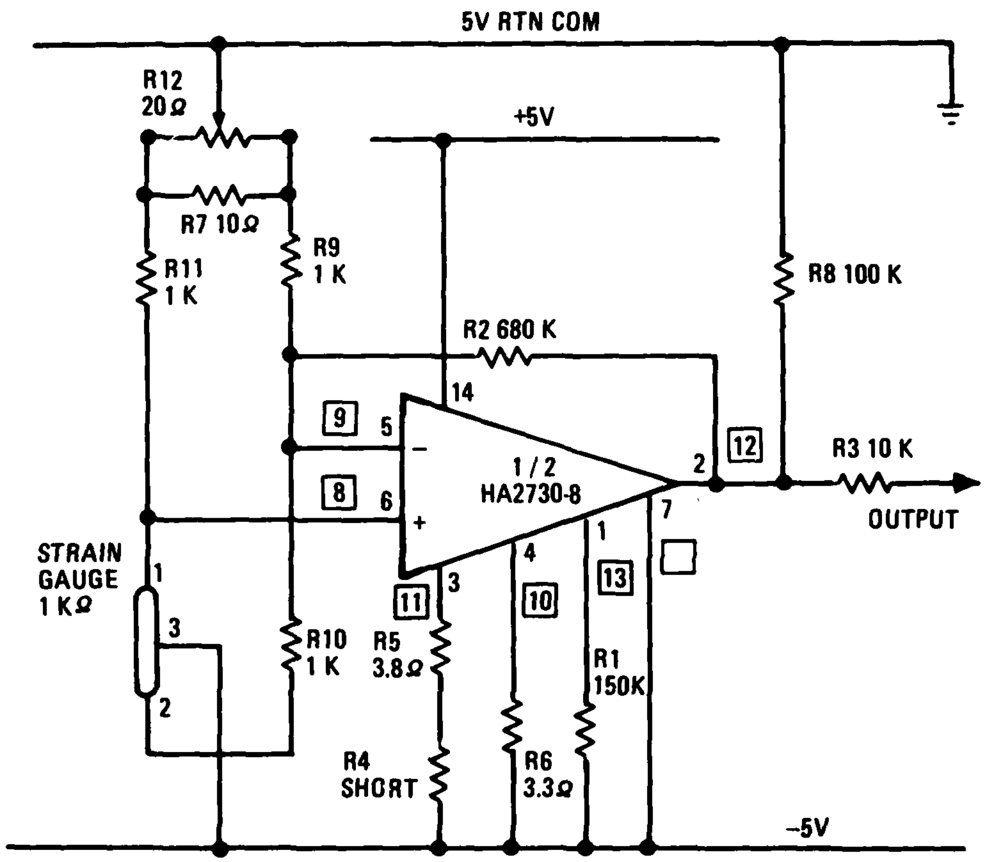


Fig. 2-5a. One of 20 Bridge and Strain
Gauge Amplifier Circuits

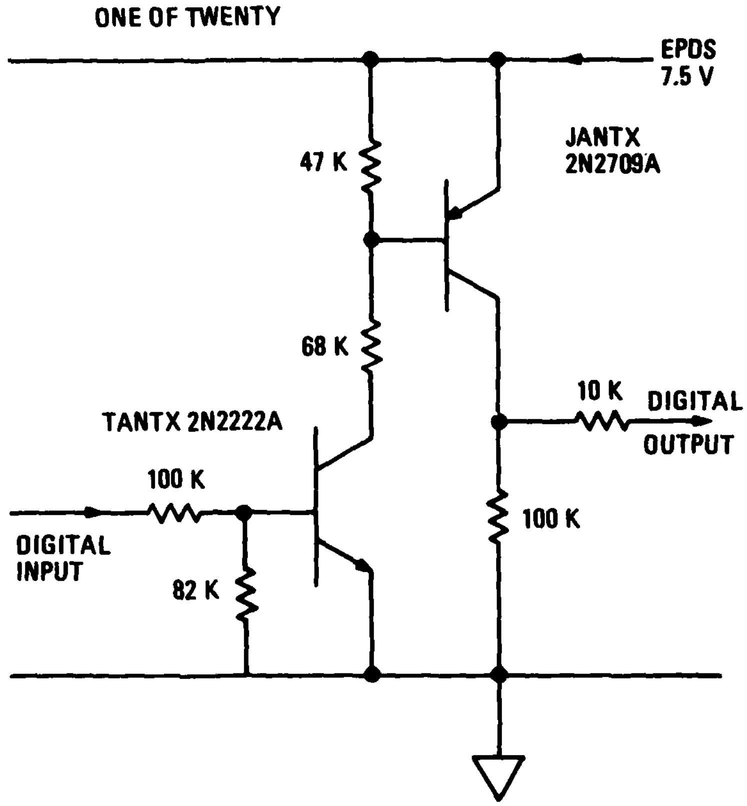


Fig. 2-5b. Interface Voltage Translation Circuit

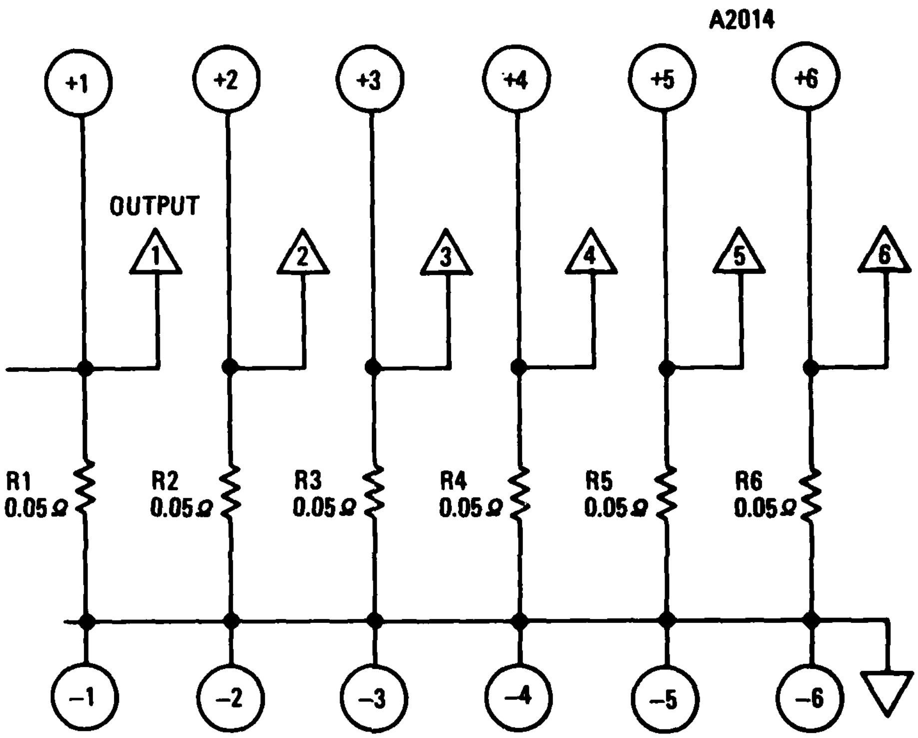


Fig. 2-6. Solar Cell Power Monitor Circuits

The transducers used to sense temperature are thermistors (Appendix A). Three different Yellow Springs Instrument (YSI) thermistor models cover the temperature ranges expected during this experiment. Model 44033 is used for the low temperature circuit; model 44032, for the high temperatures; and model 44031, for the wide range and composite sample temperatures (Fig. 2-7a and 2-7b). The interchangeability among thermistors of the same model is ±0.1°C from 0 to +75°C. The operable temperature range is -55 to +70°C. The time constant is about 1 sec for heat sunk (Torr-sealed to the tray) thermistors, and their dissipation constant is 8 mW/°C. The YSI thermistor resistance versus temperature table is reprinted in Table 2-4. For convenience, the measured output voltage versus temperature for our circuits is reprinted in Tables 2-5 through 2-7b. It is this voltage that is transmitted to EPDS high-level analog inputs.

The data from the Berkeley Controls quartz crystal monitor (QCM) and the Boeing fiber optics experiments are transmitted to EPDS as parallel digital data. Further details of these experiments are given in the documentation supplied by Boeing and Berkeley Controls.

2.3.2 Signal Conditioning Unit

The SCU acts as the interface between the transducers and the EPDS recording networks. All transducer signals are processed in the SCU before they are transmitted to EPDS. The location and primary function of each of the 10 input/output ports of the SCU is indicated in Fig. 2-8. The SCU on command from EPDS powers up the experiments for the data scans and also powers down the experiments after the data scan. The SCU enclosure houses the electronics for the Berkeley Controls QCM, the monitoring circuits for the thermistors, strain gauge amplifiers, solar cell power monitoring circuits, and the interface voltage translation circuits for the parallel digital data.

The 20 translation circuits (Fig. 2-5b) ensure that the digital logic of EPDS has the proper voltage for a true (high) bit even as the EPDS battery voltage drops during the mission. If this translation were not used, the SCU true voltage could either be less than the true threshold level of the EPDS logic or greater than the damage threshold as the two battery supplies (for SCU and EPDS) discharge.

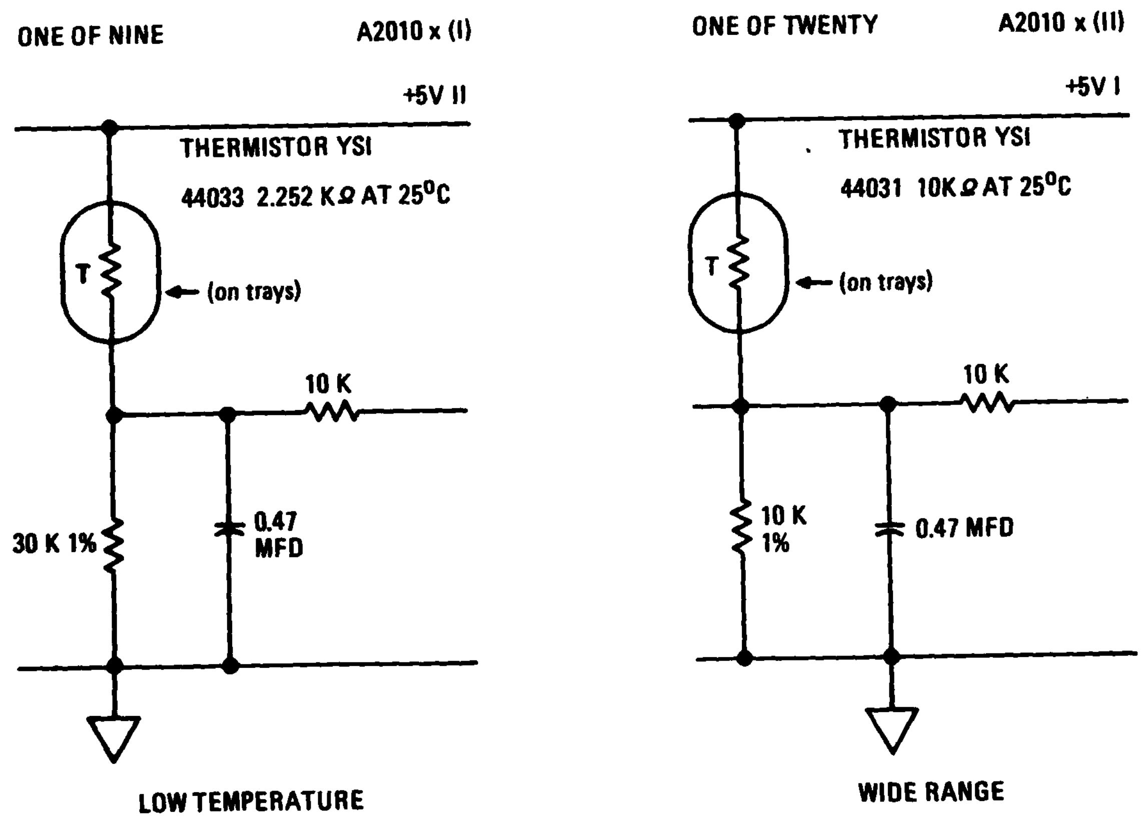


Fig. 2-7a. Low Temperature Thermistor Circuit and Wide Range Thermistor Circuit

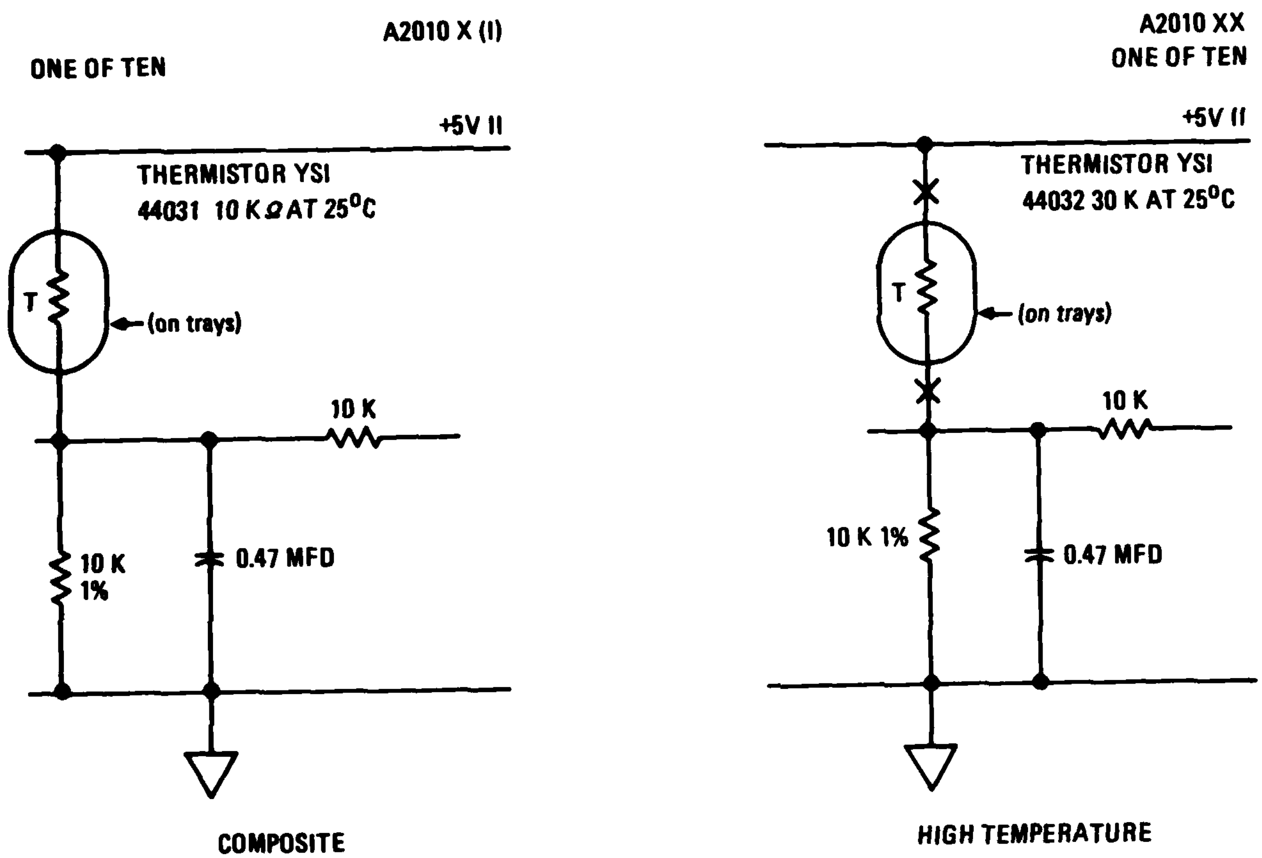


Fig. 2-7b. Composite Thermistor Circuit and High Temperature Thermistor Circuit

Table 2-4. YSI Thermistor Resistance vs. Temperature*

PART NO.	44001	44002	44003	44004 44033	44005 44030	44007 44034	44006 44031	44008 44032	44011	44014	44015
Ω @ 25°C	100	300	1000	2252	3000	5000	10,000	30,000	100,000	300,000	1 MEG.
BODY	BLACK	BLACK	BLACK	BLACK ORANGE	BLACK ORANGE	BLACK ORANGE	BLACK ORANGE	BLACK ORANGE	BROWN	BROWN	BROWN
END	BROWN	RED	ORANGE	YELLOW ORANGE	GREEN BLACK	VIOLET YELLOW	BLUE BROWN	GRAY RED	BROWN	YELLOW	GREEN
TEMP. °C	RESISTANCE Ω										
−80	11.73K	53.50K	229.0K	1660K	2211K	3685K	3558K				
79	10.97K	49.93K	213.1K	1518K	2022K	3371K	3296K				
78	10.30K	46.62K	198.5K	1390K	1851K	3086K	3055K				
77	9656	43.55K	184.9K	1273K	1696K	2827K	2833K				
76	9061	40.70K	172.4K	1167K	1555K	2592K	2629K				
75	8506	38.06K	160.8K	1071K	1426K	2378K	2440K				
74	7990	35.61K	150.0K	982.8K	1309K	2182K	2266K				
73	7509	33.33K	140.0K	902.7K	1202K	2005K	2106K				
72	7060	31.22K	130.8K	829.7K	1105K	1843K	1957K				
71	6642	29.25K	122.2K	763.1K	1016K	1695K	1821K				
−70	6251	27.42K	114.3K	702.3K	935.4K	1560K	1694K				
69	5886	25.71K	106.9K	646.7K	861.4K	1436K	1577K				
68	5545	24.12K	100.0K	595.9K	793.7K	1323K	1469K				
67	5227	22.65K	93.63K	549.4K	731.8K	1220K	1369K				
66	4929	21.27K	87.70K	506.9K	675.2K	1126K	1276K				
65	4650	19.98K	82.18K	467.9K	623.3K	1039K	1190K				
64	4389	18.78K	77.04K	432.2K	575.7K	959.9K	1111K				
63	4144	17.66K	72.25K	399.5K	532.1K	887.2K	1037K				
62	3915	16.62K	67.80K	369.4K	492.1K	820.5K	968.4K				
61	3700	15.64K	63.64K	341.8K	455.3K	759.2K	904.9K				
−60	3499	14.73K	59.77K	316.5K	421.5K	702.9K	845.9K				
59	3310	13.88K	56.16K	293.2K	390.5K	651.1K	791.1K				
58	3132	13.08K	52.78K	271.7K	361.9K	603.5K	740.2K				
57	2965	12.33K	49.63K	252.0K	335.7K	559.7K	692.8K				
56	2809	11.63K	46.69K	233.8K	311.5K	519.4K	648.8K				
55	2661	10.98K	43.94K	217.1K	289.2K	482.2K	607.8K				
54	2523	10.36K	41.37K	201.7K	268.6K	447.9K	569.6K				
53	2392	9785	38.97K	187.4K	249.7K	416.3K	534.1K				
52	2270	9245	36.72K	174.3K	232.2K	387.1K	501.0K				
51	2154	8738	34.62K	162.2K	216.0K	360.2K	470.1K				
−50	2045	8262	32.64K	151.0K	201.1K	335.3K	441.3K				
49	1942	7815	30.80K	140.6K	187.3K	312.3K	414.5K				
48	1846	7395	29.06K	131.0K	174.5K	291.0K	389.4K				
47	1754	7000	27.44K	122.1K	162.7K	271.3K	366.0K				
46	1668	6629	25.92K	113.9K	151.7K	253.0K	344.1K				
45	1587	6280	24.49K	106.3K	141.6K	236.2K	323.7K				
44	1510	5951	23.15K	99.26K	132.2K	220.5K	304.6K				
43	1438	5642	21.89K	92.72K	123.5K	205.9K	286.7K				
42	1369	5351	20.70K	86.65K	115.4K	192.5K	270.0K				
41	1304	5076	19.59K	81.02K	107.9K	180.0K	254.4K				
−40	1243	4818	18.55K	75.79K	101.0K	168.3K	239.8K	884.6K	3356K		
39	1185	4574	17.56K	70.93K	94.48K	157.5K	226.0K	830.9K	3147K		
38	1130	4344	16.64K	66.41K	88.46K	147.5K	213.2K	780.8K	2951K		
37	1078	4127	15.77K	62.21K	82.87K	138.2K	201.1K	733.9K	2769K		
36	1029	3922	14.94K	58.30K	77.66K	129.5K	189.8K	690.2K	2599K		
35	981.8	3729	14.17K	54.66K	72.81K	121.4K	179.2K	649.3K	2440K		
34	937.6	3546	13.44K	51.27K	68.30K	113.9K	169.3K	611.0K	2292K		
33	895.6	3374	12.76K	48.11K	64.09K	106.9K	160.0K	575.2K	2154K		
32	855.8	3211	12.11K	45.17K	60.17K	100.3K	151.2K	541.7K	2025K		
31	818.0	3057	11.50K	42.42K	56.51K	94.22K	143.0K	510.4K	1904K		
−30	782.1	2911	10.92K	39.86K	53.10K	88.53K	135.2K	481.0K	1791K		
29	748.1	2773	10.38K	37.47K	49.91K	83.22K	127.9K	453.5K	1685K		
28	715.7	2642	9866	35.24K	46.94K	78.26K	121.1K	427.7K	1586K		
27	685.0	2519	9381	33.15K	44.16K	73.62K	114.6K	403.5K	1494K		
26	655.7	2402	8922	31.20K	41.56K	69.29K	108.6K	380.9K	1407K		
25	627.9	2291	8489	29.38K	39.13K	65.24K	102.9K	359.6K	1326K		
24	601.5	2185	8079	27.67K	36.86K	61.45K	97.49K	339.6K	1250K		
23	576.4	2086	7692	26.07K	34.73K	57.90K	92.43K	320.9K	1178K		
22	552.4	1991	7325	24.58K	32.74K	54.58K	87.66K	303.3K	1111K		
21	529.6	1901	6978	23.18K	30.87K	51.47K	83.16K	286.7K	1049K		
−20	507.9	1816	6649	21.87K	29.13K	48.56K	78.91K	271.2K	989.8K		
19	487.3	1736	6338	20.64K	27.49K	45.83K	74.91K	256.5K	934.6K		
18	467.6	1659	6043	19.48K	25.95K	43.27K	71.13K	242.8K	882.7K		
17	448.8	1586	5764	18.40K	24.51K	40.86K	67.57K	229.8K	834.0K		
16	430.9	1517	5499	17.38K	23.16K	38.61K	64.20K	217.6K	788.2K		
15	413.8	1451	5248	16.43K	21.89K	36.49K	61.02K	206.2K	745.2K		
14	397.5	1388	5009	15.54K	20.70K	34.50K	58.01K	195.4K	704.7K		
13	382.0	1329	4783	14.70K	19.58K	32.63K	55.17K	185.2K	666.7K		
12	367.1	1272	4569	13.91K	18.52K	30.88K	52.48K	175.6K	630.9K		
11	352.9	1218	4365	13.16K	17.53K	29.23K	49.94K	166.6K	597.2K		
−10	339.4	1167	4172	12.46K	16.60K	27.67K	47.54K	158.0K	565.5K		
9	326.5	1118	3988	11.81K	15.72K	26.21K	45.27K	150.0K	535.6K		
8	314.1	1072	3813	11.19K	14.90K	24.83K	43.11K	142.4K	507.5K		
7	302.3	1028	3647	10.60K	14.12K	23.54K	41.07K	135.2K	481.0K		
6	291.0	985.5	3489	10.05K	13.39K	22.32K	39.14K	128.5K	456.0K		
5	280.2	945.3	3339	9534	12.70K	21.17K	37.31K	122.1K	432.4K		
4	269.8	907.0	3196	9046	12.05K	20.08K	35.57K	116.0K	410.2K		
3	259.9	870.4	3061	8586	11.44K	19.06K	33.93K	110.3K	389.2K		
2	250.5	835.5	2931	8151	10.86K	18.10K	32.37K	104.9K	369.4K		
−1	241.4	802.3	2808	7741	10.31K	17.19K	30.89K	99.80K	350.7K		
0	232.7	770.5	2691	7355	9796	16.33K	29.49K	94.98K	333.1K	1080K	3966K
+1	224.4	739.9	2579	6990	9310	15.52K	28.15K	90.41K	316.4K	1030K	3740K
2	216.4	710.7	2472	6644	8851	14.75K	26.89K	86.08K	300.6K	975.3K	3529K
3	208.7	682.8	2370	6319	8417	14.03K	25.69K	81.98K	285.7K	923.8K	3330K
4	201.4	656.2	2273	6011	8006	13.34K	24.55K	78.11K	271.6K	875.2K	3144K
5	194.3	630.8	2181	5719	7618	12.70K	23.46K	74.44K	258.3K	829.5K	2969K
6	187.6	606.4	2093	5444	7252	12.09K	22.43K	70.96K	245.7K	786.3A	2804K
7	181.1	583.2	2009	5183	6905	11.51K	21.45K	67.66K	233.8K	745.6K	2649K
8	174.9	561.0	1928	4937	6576	10.96K	20.52K	64.53K	222.5K	707.2K	2504K
9	169.0	539.8	1852	4703	6265	10.44K	19.63K	61.56K	211.9K	671.0K	2367K
+10	163.3	519.4	1779	4482	5971	9951	18.79K	58.75K	201.7K	636.8K	2238K
11	157.8	500.0	1709	4273	5692	9486	17.98K	56.07K	192.2K	604.5K	2117K
12	152.5	481.4	1642	4074	5427	9046	17.22K	53.54K	[illegible]	574.0K	2003K
13	147.4	463.6	1578	3886	5177	8628	16.49K	51.13K	174.5K	545.2K	1896K
14	142.6	446.6	1518	3708	4938	8232	15.79K	48.84K	166.3K	518.0K	1795K
15	137.9	430.2	1459	3539	4714	7857	15.13K	46.67K	158.6K	492.3K	1700K
16	133.4	414.6	1404	3378	4500	7500	14.50K	44.60K	151.3K	468.0K	1610K
17	129.1	399.6	1351	3226	4297	7162	13.90K	42.64K	144.3K	444.9K	1525K
18	125.0	385.3	1300	3081	4105	6841	13.33K	40.77K	137.7K	423.2K	1446K
19	121.0	371.5	1251	2944	3922	6536	12.79K	38.99K	131.4K	402.6K	1370K
+20	117.1	358.3	1204	2814	3748	6247	12.26K	37.30K	125.5K	383.1K	1299K
21	113.4	345.6	1160	2690	3583	5972	11.77K	35.70K	119.8K	364.6K	1232K
22	109.9	333.5	1117	2572	3426	5710	11.29K	34.17K	114.5K	347.1K	1168K
23	106.4	321.9	1076	2460	3277	5462	10.84K	32.71K	109.4K	330.6K	1110K
24	103.1	310.7	1037	2354	3135	5225	10.41K	31.32K	104.5K	314.9K	1053K
25	100.0	300.0	1000	2252	3000	5000	10.00K	30.00K	100.0K	300.0K	1000K
26	96.9	289.7	963.4	2156	2872	4787	9605	28.74K	95.51K	285.9K	949.7K
27	94.0	279.8	928.9	2064	2750	4583	9227	27.54K	91.34K	272.5K	902.2K
28	91.1	270.3	895.9	1977	2633	4389	8867	26.40K	87.38K	259.8K	857.2K
29	88.4	261.1	864.1	1894	2523	4204	8523	25.31K	83.60K	247.8K	814.7K
+30	85.7	252.4	833.7	1815	2417	4029	8194	24.27K	80.00K	236.4K	774.5K
31	83.2	244.0	804.5	1739	2317	3861	7880	23.28K	76.58K	225.6K	736.5K
32	80.7	235.9	776.5	1667	2221	3702	7579	22.33K	73.32K	215.3K	700.5K
33	78.4	228.1	749.6	1599	2130	3549	7291	21.43K	70.22K	205.5K	666.4K
34	76.1	220.6	723.8	1533	2042	3404	7016	20.57K	67.28K	196.2K	634.1K
35	73.9	213.4	699.0	1471	1959	3266	6752	19.74K	64.44K	187.4K	603.6K
36	71.7	206.5	675.2	1412	1880	3134	6500	18.96K	61.75K	179.0K	574.6K
37	69.7	199.8	652.4	1355	1805	3008	6258	18.21K	59.19K	171.0K	547.2K
38	67.7	193.4	630.4	1301	1733	2888	6026	17.49K	56.75K	163.5K	521.2K
+39	65.8	187.2	609.3	1249	1664	2773	5806	16.80K	54.42K	156.3K	496.6K

*Taken from Yellow Springs Instruments catalogue.

Table 2-4. YSI Thermistor Resistance vs. Temperature (Continued)

PART NO.	44001	44002	44003	44004 44033	44005 44030	44007 44034	44006 44031	44008 44032	44011	44014	44015
Ω@25°C	100	300	1000	2252	3000	5000	10,000	30,000	100,000	300,000	1 MEG.
BODY	BLACK	BLACK	BLACK	BLACK ORANGE	BLACK ORANGE	BLACK ORANGE	BLACK ORANGE	BLACK ORANGE	BROWN	BROWN	BROWN
END	BROWN	RED	ORANGE	YELLOW ORANGE	GREEN BLACK	VIOLET YELLOW	BLUE BROWN	GRAY RED	BROWN	YELLOW	GREEN
TEMP. °C	RESISTANCE Ω										
+40	63.9	181.2	589.0	1200	1500	2863	5682	16.16K	52.19K	149.4K	473.2K
41	62.1	175.5	569.5	1152	1535	2580	5389	15.52K	50.07K	142.9K	451.0K
42	60.4	170.0	550.7	1107	1475	2458	5193	14.92K	48.04K	136.7K	430.0K
43	58.7	164.7	532.7	1064	1418	2363	5006	14.35K	46.11K	130.8K	410.0K
44	57.1	159.6	515.3	1023	1363	2272	4827	13.80K	44.26K	125.1K	391.1K
45	55.6	154.6	498.6	983.8	1310	2184	4655	13.28K	42.50K	119.8K	373.1K
46	54.1	149.9	482.5	946.2	1260	2101	4489	12.77K	40.81K	114.7K	356.1K
47	52.6	145.3	467.0	910.2	1212	2021	4331	12.29K	39.20K	109.8K	339.8K
48	51.2	140.9	452.1	875.8	1167	1944	4179	11.83K	37.66K	105.2K	324.4K
49	49.8	136.6	437.8	842.8	1123	1871	4033	11.39K	36.19K	100.8K	309.8K
+50	48.5	132.5	423.9	811.3	1081	1801	3893	10.97K	34.70K	96.54K	295.9K
51	47.2	128.5	410.6	781.1	1040	1734	3758	10.57K	33.44K	92.52K	282.7K
52	46.0	124.7	397.8	752.2	1002	1670	3629	10.18K	32.15K	88.69K	270.1K
53	44.8	121.0	385.4	724.5	965.0	1608	3504	9807	30.92K	85.04K	258.1K
54	43.6	117.4	373.5	697.9	929.6	1549	3385	9450	29.74K	81.55K	246.7K
55	42.5	114.0	362.0	672.5	895.8	1493	3270	9109	28.61K	78.22K	235.9K
56	41.4	110.7	351.0	648.1	863.3	1439	3160	8781	27.53K	75.04K	225.6K
57	40.3	107.5	340.3	624.8	832.2	1387	3054	8467	26.50K	72.01K	215.8K
58	39.3	104.4	330.0	602.4	802.3	1337	2952	8166	25.50K	69.11K	206.4K
59	38.3	101.4	320.1	580.9	773.7	1290	2854	7876	24.56K	66.34K	197.5K
+60	37.3	98.5	310.5	560.3	746.3	1244	2760	7599	23.65K	63.70K	189.1K
61	36.4	95.7	301.2	540.5	719.9	1200	2669	7332	22.77K	61.17K	181.0K
62	35.5	93.0	292.3	521.5	694.7	1158	2582	7076	21.94K	58.75K	173.3K
63	34.6	90.3	283.7	503.3	670.4	1117	2497	6830	21.14K	56.44K	166.0K
64	33.8	87.8	275.3	485.8	647.1	1079	2417	6594	20.37K	54.23K	159.0K
65	33.0	85.4	267.3	469.0	624.7	1041	2339	6367	19.63K	52.12K	152.3K
66	32.1	83.0	259.5	452.9	603.3	1006	2264	6149	18.93K	50.10K	146.0K
67	31.4	80.7	252.0	437.4	582.6	971.1	2191	5940	18.25K	48.17K	139.9K
68	30.6	78.5	244.8	422.5	562.8	938.0	2122	5738	17.60K	46.32K	134.1K
69	29.9	76.4	237.8	408.2	543.7	906.3	2055	5545	16.97K	44.54K	128.6K
+70	29.2	74.3	231.0	394.5	525.4	875.7	1990	5359	16.37K	42.85K	123.3K
71	28.5	72.3	224.5	381.2	507.8	846.4	1928	5180	15.80K	41.23K	118.3K
72	27.8	70.3	218.2	368.5	490.9	818.3	1868	5007	15.25K	39.67K	113.5K
73	27.2	68.5	212.0	356.2	474.7	791.2	1810	4842	14.72K	38.18K	108.9K
74	26.5	66.6	206.1	344.5	459.0	765.1	1754	4682	14.21K	36.75K	104.5K
75	25.9	64.9	200.4	333.1	444.0	740.0	1700	4529	13.72K	35.39K	100.3K
76	25.3	63.2	194.9	322.3	429.5	715.9	1648	4381	13.25K	34.08K	96.31K
77	24.7	61.5	189.5	311.8	415.6	692.7	1598	4239	12.79K	32.82K	92.48K
78	24.2	59.9	184.3	301.7	402.2	670.3	1549	4102	12.36K	31.62K	88.82K
79	23.6	58.4	179.3	292.0	389.3	648.8	1503	3970	11.94K	30.46K	85.32K
+80	23.1	56.8	174.5	282.7	376.9	628.1	1458	3843	11.54K	29.35K	81.98K
81	22.6	55.4	169.8	273.7	364.9	608.2	1414	3720	11.15K	28.29K	78.78K
82	22.1	54.0	165.2	265.0	353.4	588.9	1372	3602	10.78K	27.27K	75.71K
83	21.6	52.6	160.8	256.7	342.2	570.4	1332	3489	10.42K	26.29K	72.78K
84	21.1	51.3	156.6	248.6	331.5	552.6	1293	3379	10.08K	25.35K	69.98K
85	20.6	50.0	152.4	240.9	321.2	535.4	1255	3273	9744	24.45K	67.29K
86	20.2	48.7	148.4	233.4	311.3	518.8	1218	3172	9424	23.59K	64.72K
87	19.7	47.5	144.5	226.2	301.7	502.8	1183	3073	9117	22.76K	62.26K
88	19.3	46.3	140.8	219.3	292.4	487.4	1149	2979	8821	21.96K	59.91K
89	18.9	45.2	137.1	212.6	283.5	472.6	1116	2887	8536	21.19K	57.65K
+90	18.5	44.1	133.6	206.1	274.9	458.2	1084	2799	8261	20.45K	55.48K
91	18.1	43.0	130.2	199.9	266.6	444.4	1053	2714	7996	19.75K	53.41K
92	17.7	41.9	126.8	193.9	258.6	431.0	1023	2632	7741	19.07K	51.42K
93	17.3	40.9	123.6	188.1	250.9	418.2	994.2	2552	7496	18.41K	49.52K
94	17.0	39.9	120.5	182.5	243.4	405.7	966.3	2476	7259	17.78K	47.69K
95	16.6	39.0	117.5	177.1	236.2	393.7	939.3	2402	7030	17.18K	45.94K
96	16.3	38.1	114.5	171.9	229.3	382.1	913.2	2331	6810	16.60K	44.26K
97	15.9	37.2	111.7	166.9	222.6	370.9	887.9	2262	6598	16.04K	42.65K
98	15.6	36.3	108.9	162.0	216.1	360.1	863.4	2195	6393	15.50K	41.10K
99	15.3	35.4	106.2	157.3	209.8	349.7	839.7	2131	6195	14.98K	39.62K
+100	15.0	34.6	103.6	152.8	203.8	339.6	816.8	2069	6005	14.48K	38.20K
101	14.7	33.8	101.1	148.4	197.9	329.8	794.6	2009	5821	14.00K	36.84K
102	14.4	33.0	98.6	144.2	192.2	320.4	773.1	1950	5643	13.54K	35.53K
103	14.1	32.2	96.2	140.1	186.8	311.3	752.3	1894	5472	13.09K	34.27K
104	13.8	31.5	93.9	136.1	181.5	302.5	732.1	1840	5307	12.66K	33.06K
105	13.5	30.8	91.6	132.3	176.4	294.0	712.6	1788	5147	12.25K	31.91K
106	13.3	30.1	89.5	128.6	171.4	285.7	693.6	1737	4993	11.86K	30.79K
107	13.0	29.4	87.3	125.0	166.7	277.8	675.3	1688	4844	11.47K	29.72K
108	12.8	28.7	85.3	121.6	162.0	270.1	657.5	1640	4700	11.11K	28.69K
109	12.5	28.1	83.2	118.2	157.6	262.6	640.3	1594	4561	10.75K	27.71K
+110	12.3	27.5	81.3	115.0	153.2	255.4	623.5	1550	4427	10.41K	26.76K
111	12.0	26.8	79.4	111.8	149.0	248.4	607.3	1507	4297	10.08K	25.84K
112	11.8	26.2	77.6	108.8	145.0	241.6	591.6	1465	4172	9763	24.96K
113	11.6	25.7	75.8	105.8	141.1	235.1	576.4	1425	4051	9456	24.12K
114	11.4	25.1	74.0	103.0	137.2	228.7	561.6	1386	3933	9161	23.31K
115	11.1	24.6	72.3	100.2	133.6	222.6	547.3	1348	3820	8876	22.52K
116	10.9	24.0	70.7	97.6	130.0	216.7	533.4	1311	3711	8601	21.77K
117	10.7	23.5	69.1	95.0	126.5	210.9	519.9	1276	3605	8336	21.05K
118	10.5	23.0	67.5	92.5	123.2	205.3	506.8	1241	3502	8080	20.35K
119	10.3	22.5	66.0	90.0	119.9	199.9	494.1	1208	3403	7832	19.68K
+120	10.1	22.0	64.5	87.7	116.8	194.7	481.8	1176	3307	7594	19.03K
121		21.6	63.1	85.4	113.8	189.6	469.8	1145	3214	7364	18.41K
122		21.1	61.7	83.2	110.8	184.7	458.2	1114	3124	7142	17.81K
123		20.6	60.3	71.1	107.9	179.9	446.9	1085	3038	6927	17.23K
124		20.2	59.0	79.0	105.2	175.3	435.9	1057	2953	6720	16.68K
125		19.8	57.7	77.0	102.5	170.8	425.3	1029	2872	6519	16.14K
126		19.4	56.4	75.0	99.9	166.4	414.9	1002	2793	6326	15.62K
127		19.0	55.2	73.1	97.3	162.2	404.9	976.3	2717	6139	15.12K
128		18.6	54.0	71.3	94.9	158.1	395.1	951.1	2643	5958	14.64K
129		18.2	52.9	69.5	92.5	154.1	385.6	926.7	2571	5784	14.18K
+130		17.8	51.7	67.8	90.2	150.3	376.4	903.0	2501	5615	13.74K
131		17.5	50.6	66.1	87.9	146.5	367.4	880.0	2434	5452	13.31K
132		17.1	49.5	64.4	85.7	142.9	358.7	857.7	2369	5294	12.89K
133		16.8	48.5	62.9	83.6	139.4	350.3	836.1	2306	5141	12.49K
134		16.4	47.5	61.3	81.6	136.0	342.0	815.0	2244	4994	12.10K
135		16.1	46.5	59.8	79.6	132.6	334.0	794.6	2185	4851	11.73K
136		15.8	45.5	58.4	77.6	129.4	326.3	774.8	2128	4713	11.37K
137		15.5	44.6	57.0	75.8	126.3	318.7	755.6	2072	4580	11.02K
138		15.2	43.6	55.6	73.9	123.2	311.3	736.9	2018	4450	10.69K
139		14.9	42.7	54.3	72.2	120.3	304.2	718.8	1965	4325	10.36K
+140		14.6	41.9	53.0	70.4	117.4	297.2	701.2	1914	4204	10.05K
141			41.0	51.7	68.8	114.6	290.4	684.1	1865	4087	9746
142			40.2	50.5	67.1	111.9	283.8	667.5	1817	3974	9455
143			39.4	49.3	65.5	109.2	277.4	651.3	1770	3864	9173
144			38.6	48.2	64.0	106.7	271.2	635.6	1725	3757	8901
145			37.8	47.0	62.5	104.2	265.1	620.3	1681	3654	8637
146			37.0	45.9	61.1	101.8	259.2	605.5	1639	3555	8383
147			36.3	44.9	59.6	99.40	253.4	591.1	1598	3458	8137
148			35.6	43.8	58.3	97.10	247.8	577.1	1558	3364	7899
149			34.9	42.8	56.9	94.87	242.3	563.5	1519	3274	7669
+150			34.2	41.9	55.6	92.70	237.0	550.2	1481	3186	7447

Note: Only thermistors with ±0.2°C interchangeability are available encased in Teflon as standard parts. For Part No. of Teflon encased thermistors add 100 to part No. of ±0.2°C interchangeable thermistors. Example: 44001 is a standard thermistor, 44101 is a Teflon encased thermistor with the same resistance values.

Table 2-5. High Temperature Thermistor Voltage vs. Temperature Power Supply Voltage 5.003 Vdc YSI 44032, 44910, 311P18, -10S Resistance 30 KΩ at 25°C

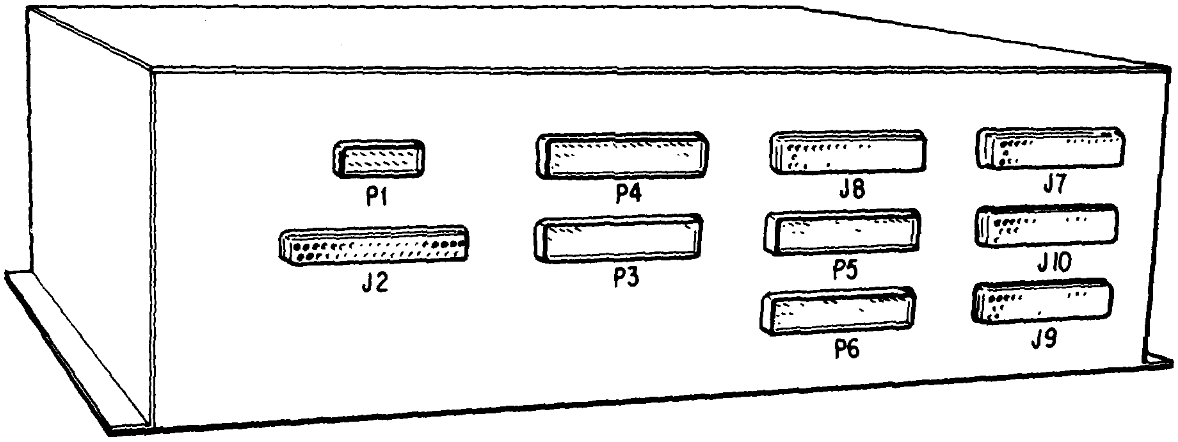
Temperature, °C	Volts	Temperature, °C	Volts	Temperature, °C	Volts	Temperature, °C	Volts	Temperature, °C	Volts
+1	0.497	21	1.093	41	1.957	61	2.883	81	3.643
2	0.519	22	1.130	42	2.004	62	2.927	82	3.675
3	0.542	23	1.169	43	2.051	63	2.969	83	3.705
4	0.566	24	1.208	44	2.099	64	3.012	84	3.736
5	0.591	25	1.249	45	2.145	65	3.054	85	3.766
6	0.616	26	1.289	46	2.193	66	3.095	86	3.795
7	0.643	27	1.330	47	2.240	67	3.135	87	3.823
8	0.670	28	1.372	48	2.288	68	3.176	88	3.851
9	0.697	29	1.414	49	2.335	69	3.195	89	3.879
10	0.726	30	1.457	50	2.381	70	3.254	90	3.905
11	0.756	31	1.500	51	2.428	71	3.292	91	3.932
12	0.786	32	1.545	52	2.475	72	3.331	92	3.957
13	0.817	33	1.589	53	2.510	73	3.368	93	3.982
14	0.848	34	1.633	54	2.569	74	3.404	94	4.007
15	0.881	35	1.679	55	2.615	75	3.440	95	4.031
16	0.915	36	1.724	56	2.661	76	3.475	96	4.054
17	0.948	37	1.770	57	2.706	77	3.510	97	4.077
18	0.983	38	1.817	58	2.751	78	3.544	98	4.099
19	1.019	39	1.864	59	2.796	79	3.578	99	4.121
20	1.056	40	1.910	60	2.840	80	3.611	100	4.142

Table 2-6. Wide Range Thermistor Voltage vs. Temperature Power Supply Voltage + 5.002 Vdc YSI 44031 + 44908 10 K Ω at 25°C

Temperature, °C	Volts	Temperature, °C	Volts	Temperature, °C	Volts	Temperature, °C	Volts	Temperature, °C	Volts	Temperature °C	Volts
-40	0.198										
39	0.209	19	0.593	+1	1.307	21	2.293	41	3.248	61	3.946
38	0.222	18	0.621	2	1.352	22	2.345	42	3.290	62	3.973
37	0.236	17	0.649	3	1.398	23	2.396	43	3.331	63	4.000
36	0.250	16	0.678	4	1.444	24	2.446	44	3.371	64	4.026
35	0.263	15	0.709	5	1.491	25	2.498	45	3.408	65	4.051
34	0.278	14	0.741	6	1.538	26	2.548	46	3.450	66	4.076
33	0.296	13	0.773	7	1.586	27	2.598	47	3.488	67	4.101
32	0.312	12	0.808	8	1.634	28	2.648	48	3.525	68	4.124
31	0.331	11	0.842	9	1.683	29	2.697	49	3.562	69	4.147
30	0.347	10	0.878	10	1.734	30	2.746	50	3.598	70	4.169
29	0.365	9	0.914	11	1.784	31	2.794	51	3.633	71	4.191
28	0.384	8	0.951	12	1.834	32	2.843	52	3.668	72	4.212
27	0.405	7	1.998	13	1.885	33	2.890	53	3.701	73	4.233
26	0.425	6	1.028	14	1.936	34	2.937	54	3.734	74	4.253
25	0.447	5	1.068	15	2.987	35	3.983	55	3.767	75	4.273
24	0.469	4	1.109	16	2.039	36	3.029	56	3.798	76	4.292
23	0.499	3	1.150	17	2.090	37	3.074	57	3.829	77	4.310
22	0.517	2	1.193	18	2.140	38	3.119	58	3.859	78	4.329
21	0.542	1	1.236	19	2.191	39	3.162	59	3.889	79	4.346
20	0.556	0	1.264	20	2.243	40	3.205	60	3.917	80	4.363

Table 2-7. Low Temperature Thermistor Voltage versus Temperature Power Supply Voltage 5.004 Vdc YSI (44902) 311P18-02S and YSI 44033 Resistance 2252 Ω at 25°C

Temperature, °C	Volts	Temperature, °C	Volts	Temperature, °C	Volts	Temperature, °C	Volts	Temperature, °C	Volts
-60	0.434	39	1.486	18	3.032	+1	4.057	22	4.610
59	0.464	38	1.556	17	3.100	2	4.097	23	4.626
58	0.497	37	1.626	16	3.166	3	4.133	24	4.641
57	0.532	36	1.699	15	3.231	4	4.169	25	4.656
56	0.568	35	1.772	14	3.294	5	4.202	26	4.670
55	0.583	34	1.846	13	3.357	6	4.235	27	4.683
54	0.647	33	1.920	12	3.417	7	4.266	28	4.696
53	0.690	32	1.995	11	3.476	8	4.296	29	4.708
52	0.734	31	2.071	10	3.533	9	4.325	30	4.719
51	0.780	30	2.147	9	3.588	10	4.353		
50	0.828	29	2.223	8	3.642	11	4.380		
49	0.879	28	2.299	7	3.747	12	4.405		
48	0.931	27	2.375	6	3.752	13	4.430		
47	0.986	26	2.451	5	3.816	14	4.454		
46	1.042	25	2.526	4	3.844	15	4.476		
45	1.100	24	2.601	3	3.890	16	4.498		
44	1.160	23	2.675	2	3.934	17	4.518		
43	1.222	22	2.748	1	3.977	18	4.538		
42	1.286	21	2.821	0	4.018	19	4.557		
41	1.351	20	2.892			20	4.575		



P1	-	Power Supply Inputs
J2	-	EPDS/SCU Pulse Command Inputs
P3	-	Solar Cells, Composites plus Low Range Thermistor Inputs
P4	-	High Range Thermistors, Parallel Boeing Data Inputs
P5	-	Wide Range Thermistors and Strain Gauge Inputs
P6	-	Strain Gauge Inputs
J7	-	Solar Cells, Composite and Low Range Thermistor Outputs
J8	-	High Range Thermistors, Boeing and QCM Parallel Digital Data Outputs
J9	-	Strain Gauge Outputs
J10	-	Wide Range Thermistor Outputs

Figure 2-8. Input/Output Ports of SCU

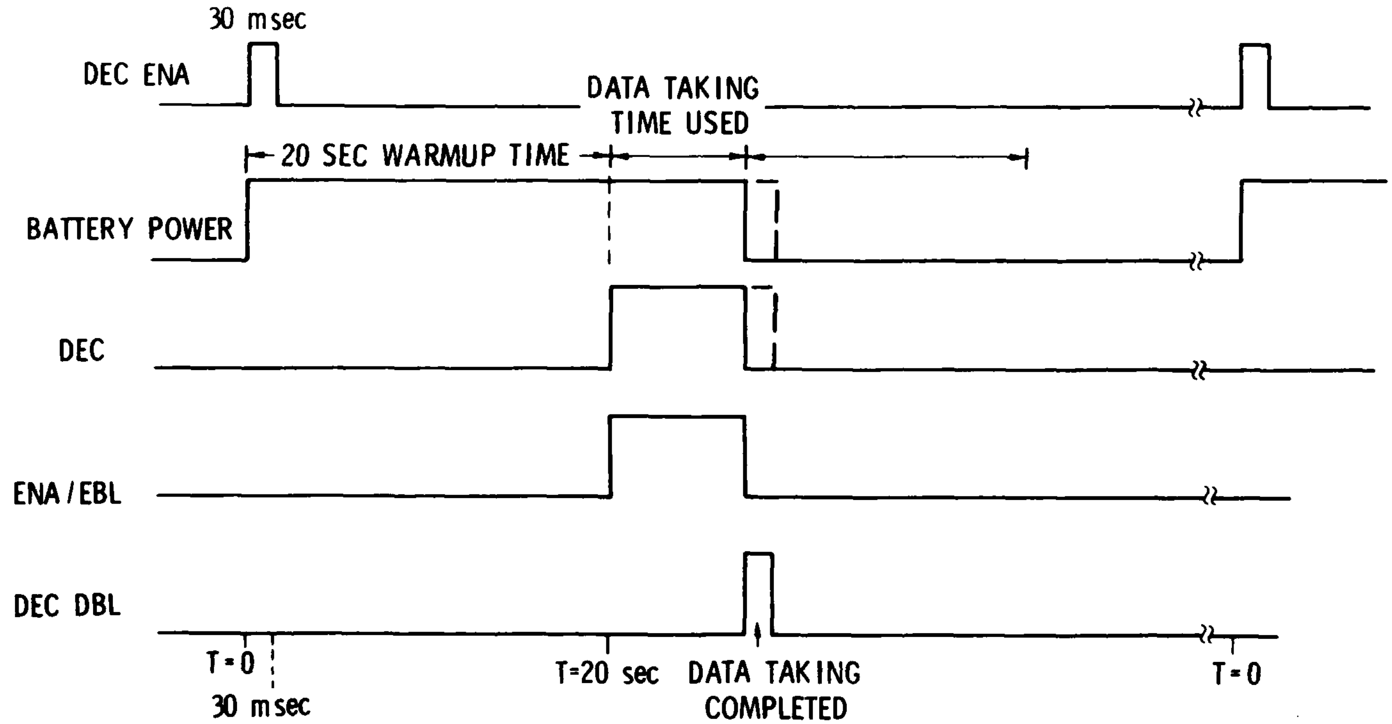


Fig. 2-9. Pulse Command Sequence

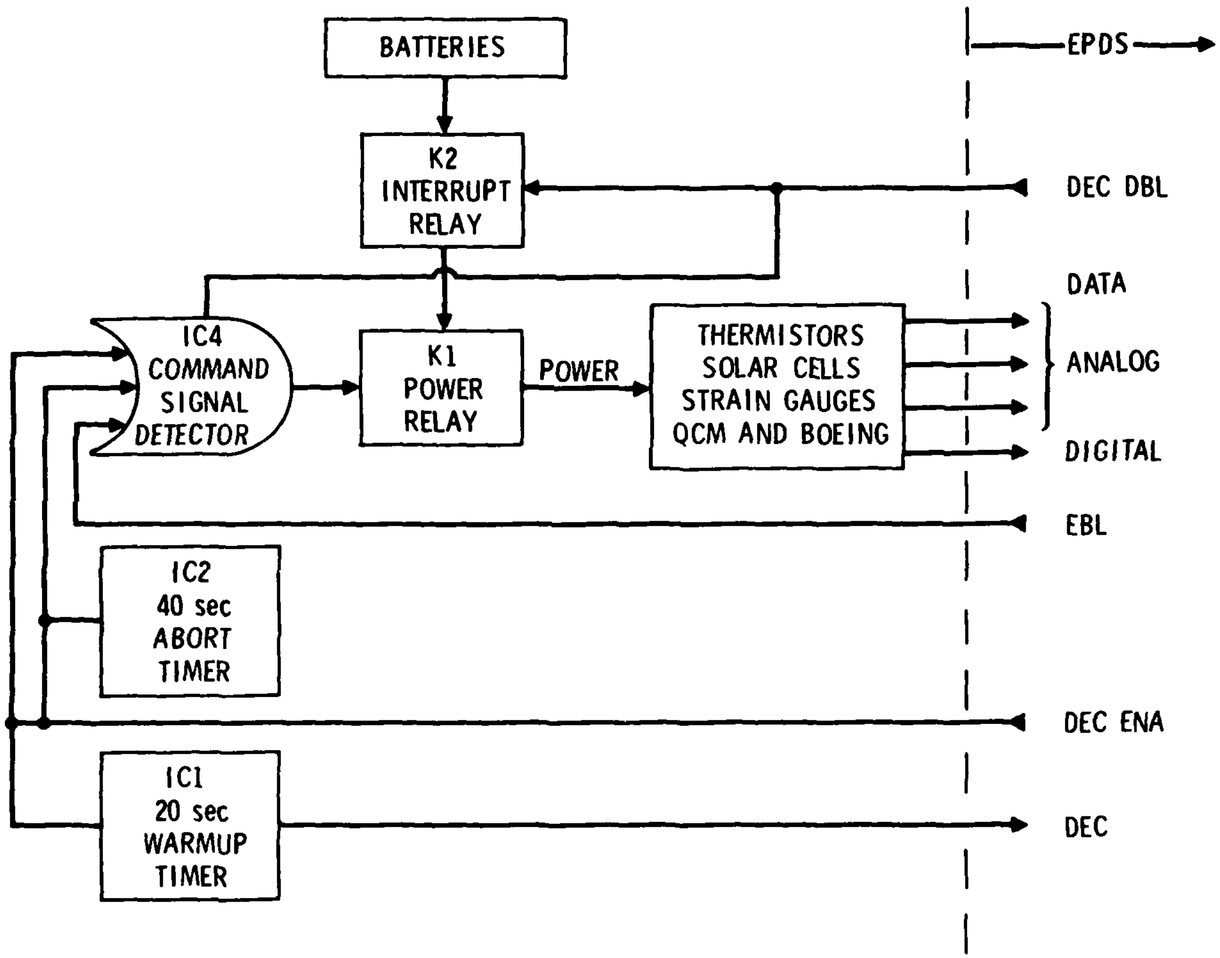
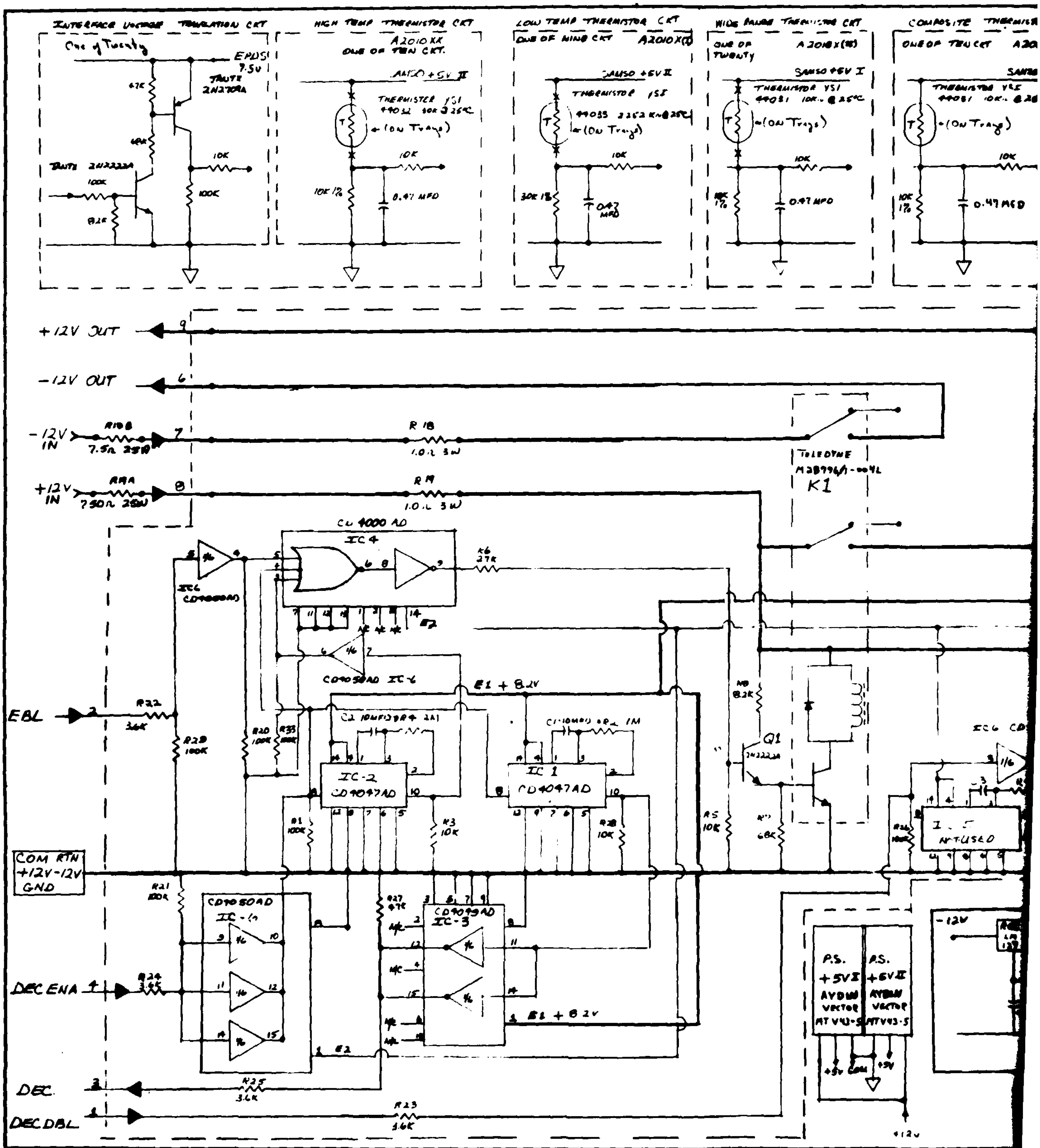


Fig. 2-10. SCU Functional Block Diagram



INTERFACE VOLTAGE TRANSLATION CKT
One of Twenty
HIGH TEMP THERMISTOR CKT
ONE OF TEN CKT.
LOW TEMP THERMISTOR CKT
WIDE RANGE THERMISTOR CKT
COMPOSITE
(On Trays)
0.47 MFD
+12V OUT
-12V OUT
-12V IN
+12V IN
TELEDYNE
K1
EBL
Q1
IC-2
CD4047AD
IC 1
CD4047AD
IC 4
IC-3
E1 + 8.2V
NOT USED
COM RTN
+12V -12V
GND
CD4050AD
CD4049AD
DEC ENA
DEC
DEC DBL
P.S.
+5V I
+5V II
VECTOR

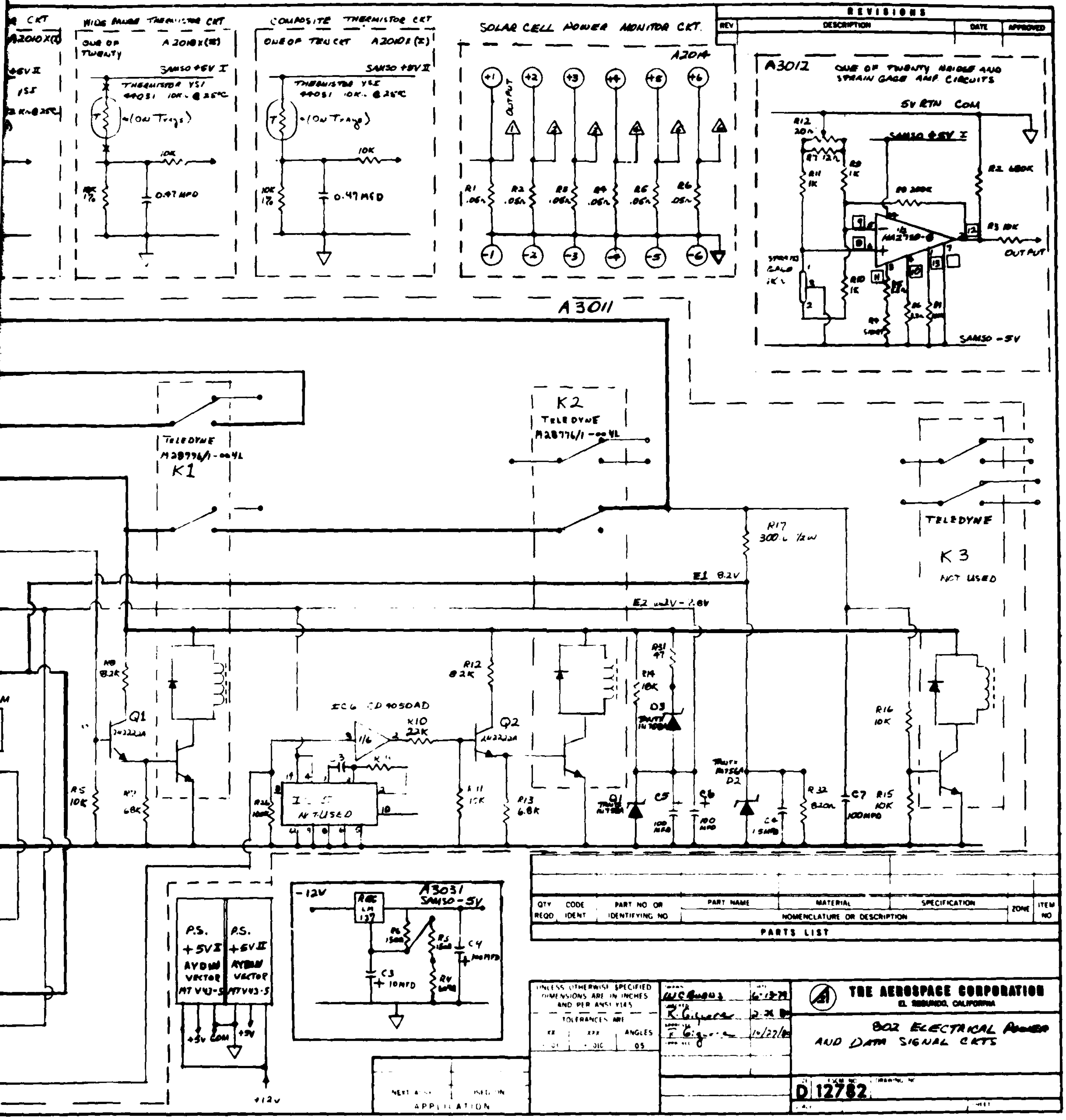


Fig. 2-11. SCU Circuit Schematic

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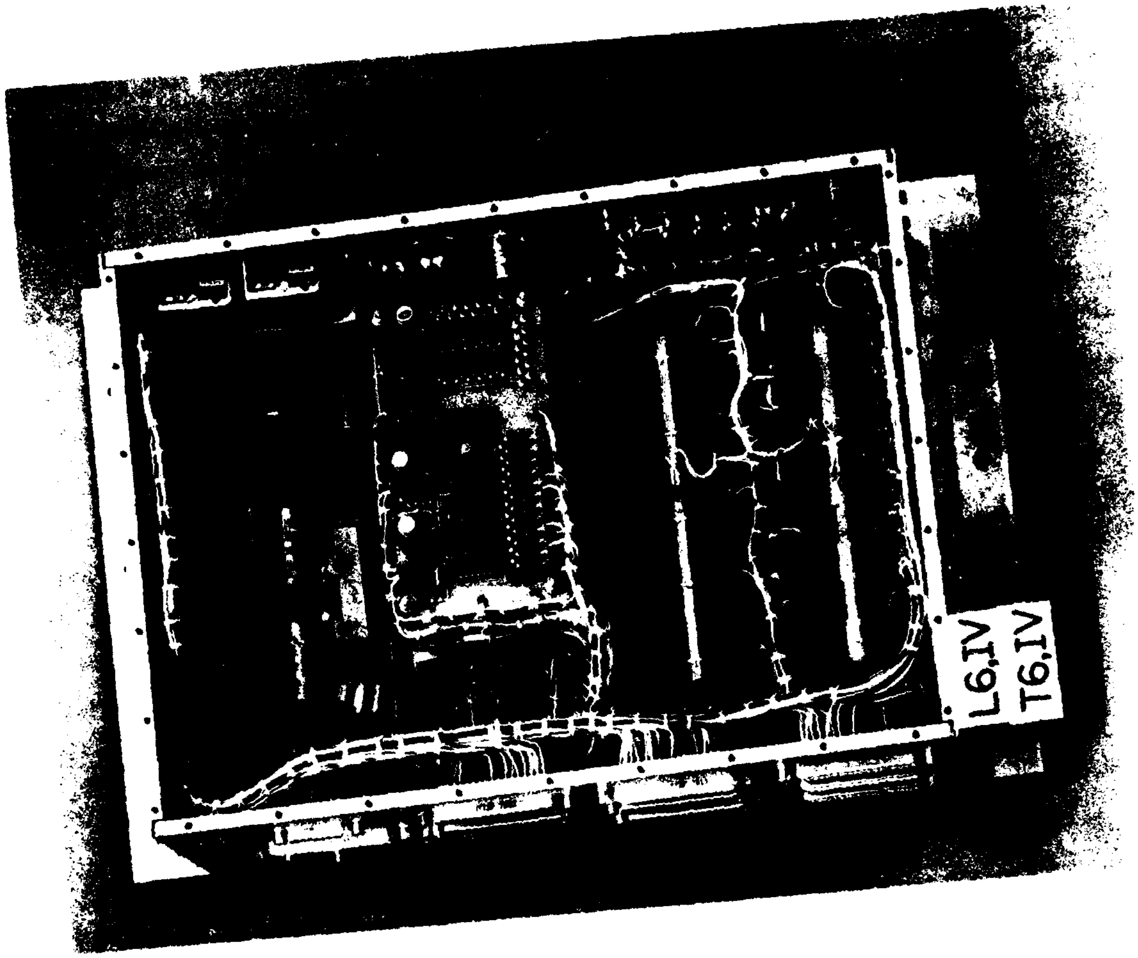

Fig. 2-12. Photograph of SCU

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The pulse command sequence between EPDS and the SCU is shown in Fig. 2-9. These commands interact with the SCU (Figs. 2-10 through 2-12) in the following manner. Initial turn on of the data recording network begins just after deployment of the LDEF satellite. In the SCU, power is applied to the NOR gate of IC4 to activate the DEC ENA command signal detector and to power the automatic shutdown timer, IC5. Only these two circuits in the SCU remain activated throughout the entire mission. The current drain from these components is less than 300 μA. All other circuitry and transducers are slaved to the EPDS data scan cycle. When the NOR gate (IC4) receives the DEC ENA command from EPDS, the power relay K1 is energized and the remaining SCU circuitry and the experiments are powered up. Two internal timers are started. One is a 20-sec timer (IC1), which permits the electronics to come to a steady state after turn on and before IC1 sends EPDS a buffered DEC command to start the data scan. The other timer (IC2) shuts down the SCU 40 sec after starting if no shutdown command is received from EPDS. During the data reading process, both the DEC ENA and the EBL signal lines are kept high to ensure that IC4, the command signal detector, does not accidently shut down the SCU during the data reading process. After EPDS has finished the data scan, it commands the SCU, through its DEC DBL line, to shut down the SCU immediately. The SCU then awaits the next DEC ENA command from EPDS.

3. DETAILS OF GROUND SUPPORT EQUIPMENT

The experiment power and data system (EPDS) ground support equipment consists of a magnetic tape memory (MTM) controller, a data display box (DDB), a computer-compatible tape recorder (CCT) with tapes, and interfacing cables. In addition, the Aerospace ground support equipment (GSE) consists of a command sequencer, an experimental load simulator, and a channel selector probe. These Aerospace units permit the checking out of the signal conditioning unit independently of EPDS.

3.1 EXPERIMENT POWER AND DATA SYSTEM GROUND SUPPORT SYSTEM

3.1.1 Data Display Box

The DDB is designed to aid the user in evaluation of the performance of an EPDS operating in a particular application. To meet this objective, the DDB provides the user with four support functions: (1) a monitor of data processor controller assembly (DPCA) data activity, (2) an interface between the flight tape recorder and CCT, (3) an auxiliary ac line-operated power distribution and control system, and (4) a numeric display and thermal printer that can both display and record the DPCA data. The user can display or print data in either octal or decimal format, display or print a single word within a DPCA data scan, or sequentially display and print every word in a data scan. The display monitors the same data signal that is presented to the 4K buffer memory in the DPCA. Key timing signals from the DPCA are used to slave the operation of the DDB to the DPCA. The printer lists data at less than 3 lines/sec, and, therefore, cannot list data in real time. The data display can not read (list) data directly from the tape but only indirectly through the 4K buffer memory. The EPDS stores large volumes of data during ground and flight operations, and a total analysis of all data will require transcription of the MTM data onto a CCT for computer analysis.

3.1.1.1 DDB Front Panel

The four meters across the top of the DDB front panel (Fig. 3-1) provide for measurement of the 7.5- and 12-V currents. Spring-loaded switches

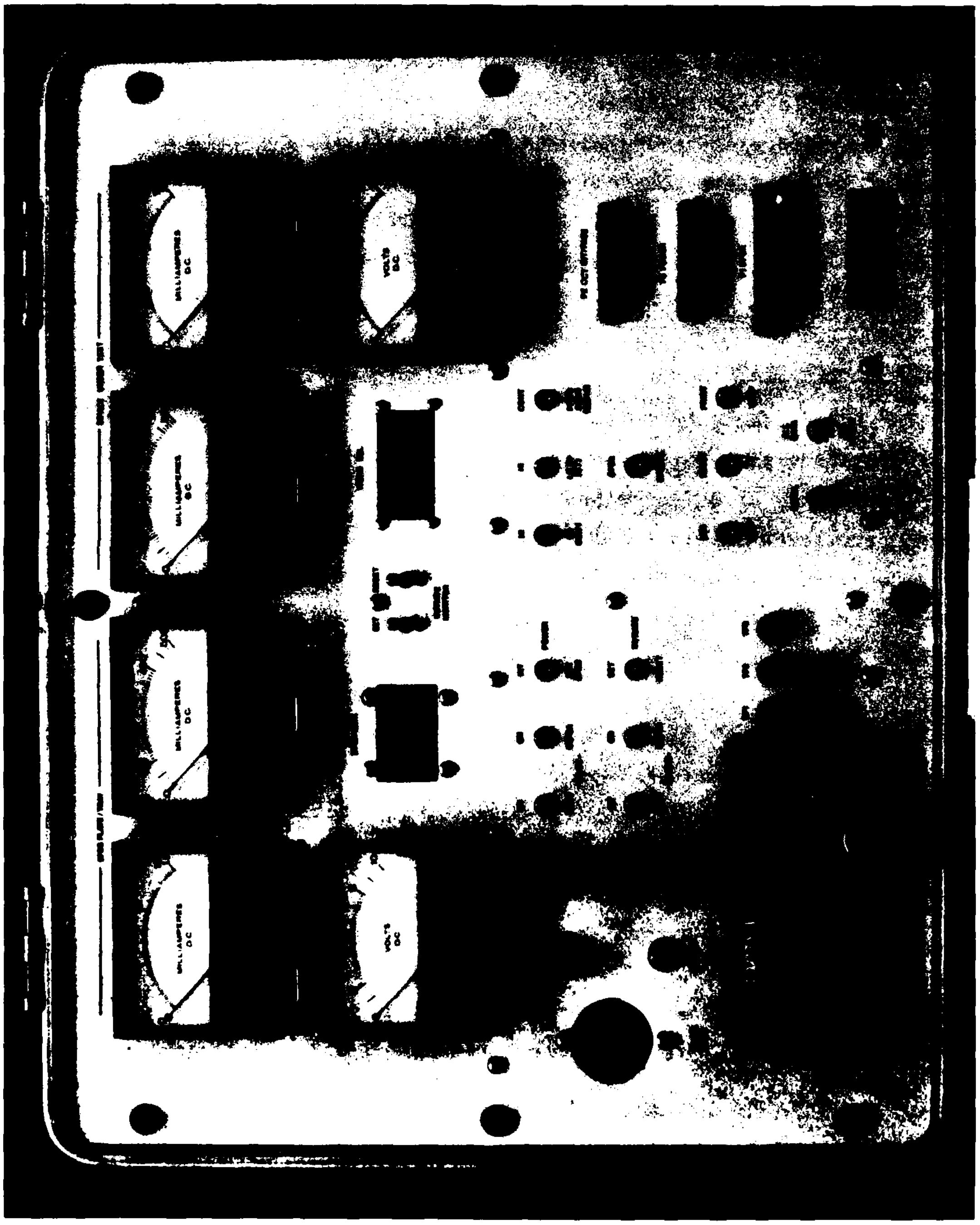

Fig. 3-1. Data Display Box Front Panel

are provided below the 7.5-V current meters to provide a range of 1.5 or 150 mA. Current loops are provided in series with each of the current meters to permit the monitoring of transient currents. The two lower meters monitor the 7.5- and 12-V supplies. A switch is provided below the 12-V current meter to permit the monitoring of a 12-V supply that is used only for the MTM controller. The ac input to each of the internal power supplies is fused. The power switch applies ac power to the power supplies and the printer. The three connectors on the lower right-hand side provide connections to the MTM controller. The top connector (P2CCT INT/FACE) is the output of the CCT circuitry and is to be connected to the computer-compatible tape recorder. The middle connector (P3 POWER) is connected to the EPDS initiate connector (P753) and the EPDS GSE power switching connector (P751). The lower connector (P1 DPCA) is connected to the EPDS DPCA connector (S703A) and to the MTM controller. The five test-point jacks (TP1 through TP5) provide oscilloscope monitoring of the DPCA data, bit clock, word clock, and reset signals.

The OCTAL/DEC switch is used to place the digital display and printed data in either octal or decimal format. The ALL DATA/SEL WORD switch is used to determine whether the digital display and printer data are a single selected word determined by the thumbwheel switches (WORD SEL) or all the data. The LED TEST causes the digital display to display all 8s. The RESET switch is used to ensure that, in the ALL DATA mode, the first word displayed is word 1. The RESET switch (S_2 on LD-DPCA-730) also ensures that no transient has set the counter associated with word selection to an ambiguous count. A good practice is to exercise the RESET switch prior to each printing or displaying of ALL DATA. The DPCA/MANUAL switch placement indicates whether the DPCA or the MTM controller issues controls to the MTM. The CON1 switch permits DDB control of the user program function CON1. The $\overline{C_T}$ switch permits DDB control of the clock inputs to the E1 through E4 counters. In the HI position, a 5-kHz clock is connected to all four E counters to functionally exercise these counters in a reasonable time. User access to the E1 through E4 pulses must be by an extender card and the oscillator-divider printed circuit card or at the DPCA plug S705 (one of the user plugs on the DPCA). The ON/OFF switches, for the EPDS and for the 7.5 and 12 V experiments, switch the dc output of the appropriate power supply. The INT/EXT switch energizes a relay (K2) on the mounting plate and permits EPDS operation on internal batteries or the DDB external supplies. Disconnecting cables from the EPDS or removal of ac power to the DDB will result in the EPDS reverting to internal batteries. Power must be applied to K2 to maintain the external position. The SET/INITIATE switch exercises the initiate function (K1) on the mounting plate. The INITIATE MONITOR lights, between the thumbwheel switches and the digital display, are used to monitor the position of the initiate relay. Storage of the EPDS to prevent battery drain is with the initiate in the RESET position.

The CON2 switch is used to place the DPCA in a normal flight mode or a continuous scanning mode. Our experiment requires this switch to be set in the PROG SCAN position. The key timing signals for operation will be provided by the DPCA flight program. EPDS will scan the input data signals, store the data in the 4K buffer memory, and transfer the data to MTM tape. Only during the time that data are stored in memory can DDB display or print data signals.

In the ALL DATA print mode, the printer will print all data measurements consecutively. However, the first data measurement listed will be separated in time by many data scans from the last measurement listed. In the SEL WORD print mode, the printer may be able to print the selected word on every data scan if the number of words in a data scan is long. The printer's maximum operating speed is 3 lines/sec. The printer format is seven characters wide. The four right-most characters are the data in either octal or decimal format. The two left-most characters represent the number of the data measurements. If the number of data measurements exceeds 99, the numbers will cycle back to zero and continue to increment, and the user will have to infer a leading-hundred digit. In an octal format, there will be a blank space between the data and the word number. In a decimal format, a plus sign will appear between the data and the word number to signify that the data are in a decimal format.

3.1.1.2 Computer Compatible Tape Interface Circuitry

The CCT interface portion of the DDB provides the means to perform end-to-end testing during EPDS integration with an experiment. The CCT interface is designed to transfer the data gathered by the flight recorder during DPCA operation to a 1/2-in., 9-track, 800-bit/in. format, which can be used as input to most large computer installations. After the data are resident in a large computer, there are a number of options for processing and listing the data in the format most meaningful to the user.

The circuit will fill each 8-bit character across the width of the tape with eight successive 1-bit characters from the flight recorder. The ninth track of the CCT recorder is normally used to record the internally-generated parity bit for each character. To prevent possible ground-loop problems, the data and clock are isolated from the MTM controller through optically-coupled isolators.

3.1.1.3 Power Distribution and Control Circuitry

The power distribution and control system permits the user to begin EPDS operation and substitute ac line-operated power supplies in place of the normal battery supplies. Complete metering is provided for the voltage and current of both the 7.5- and 12-V system supplies. Provision is made to allow the user access to the same supplies with independent current metering. Current loops are also provided so the power supply current waveforms can be observed on an oscilloscope.

3.1.2. Computer Compatible Tape Recorder

The CCT recorder is a Kennedy Model 9832 which consists of a Model 9800 synchronous tape transport with a built-in buffered formatter. The recorder operating manual (Ref. 3) includes a complete description of the interface requirements and lists of pin interface connections and command controls. In Table 3-1 is a brief description of each of the command controls and indicators.

Table 3-1. Kennedy Tape Recorder Controls and Indicators

Control	Function
End of File Pushbutton and Indicator	Momentary pushbutton, generates end of the sequence tape rewinds, if commands are not generated from customer interface.
On line Pushbutton and Indicator	Momentary pushbutton that causes alternate actions. First activation places the unit on line, in which condition it can be remotely selected and will be ready if tape is loaded to or past the load point. Next activation takes the unit off line. LED indicator is illuminated when unit is on line. A short time lag between closure and action is provided to guard against accidental operation.
Load Pushbutton and Indicator	Momentary pushbutton, activates reel servos (tension tape) and starts load sequence. LED indicator is illuminated when reel servos are activated and tape is tensioned. Pushbutton is disabled when tape unit is on line.
Rewind and Indicator	Momentary pushbutton, activates rewind operation. Control is enabled when tape is tensioned and unit is off line. LED indicator is illuminated during either local or remote rewind. Pushbutton is disabled when tape unit is on line.
Write Status Indicator	Illuminated when tape unit is on line and write status is selected.
Data In Memory Indicator	Illuminated when there are data in memory that have not been transferred to tape.
Write Enable Indicator	Illuminated when a reel with a write enable ring is mounted on the supply (file) hub.

3.1.3 Magnetic Tape Memory Controller

The MTM controller (Figs. 3-2 and 3-3) contains portions of the MTM recorder electronics and provides for manual control of the MTM. Power (±12 V and 5 V) for operation of the MTM controller is provided by the DDB. The DDB provides a switch for manual or DPCA operation of the MTM. The MTM tape can be erased by using the controller and placing the DDB in a manual mode. The function of each control is explained in Table 3-2.

Several peculiarities occur in the operation of the MTM in the EPDS. It is not possible to fully erase the MTM tape automatically because of the physical mounting of the record and erase heads in the MTM. To erase the leading 12 to 15 in. of tape, the tape must be manually positioned 12 to 15 in. back from the beginning of tape (BOT) into the clear tape area and then the erase mode must be activated.

In the reproduce mode (Ref. 4), the MTM controller provides data, a coherent clock, and a data-present signal to the DDB for formatting to a CCT. At the beginning of a data block, the data present level goes true (high) prior to the first output clock so that it can be used to gate on equipment to receive data. The ground recorder needs a logic zero bit before it can synchronize. The detection of the end of a block is more difficult to achieve. Since the data present status must remain true through tape dropouts, it is delayed from going false approximately 8 msec following the last valid data transition. During this period, noise causes triggering of the data detection comparator and causes spurious clocks and data to appear at the output. The software determines the end of valid data during decoding.

3.2 AEROSPACE GROUND SUPPORT SYSTEM

The Aerospace GSE (Fig. 3-4) consists of a pulse command sequencer, power supply, dummy loads, TRS 80 microcomputer, and a channel selector probe. The command sequencer simulates the EPDS command pulses and timing sequences to the signal conditioning unit (SCU) and is capable of speeding up the normal timing sequences. Each of the dummy loads mimics a transducer signal to the SCU. The channel selector probe is used to sample each of the SCU outputs. By means of this GSE, each SCU can be checked out without tieing

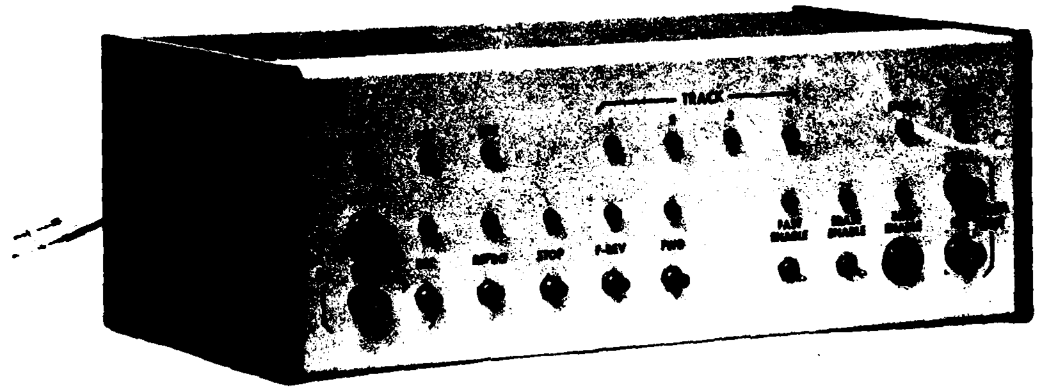

Fig. 3-2. Front Panel of MTM Controller

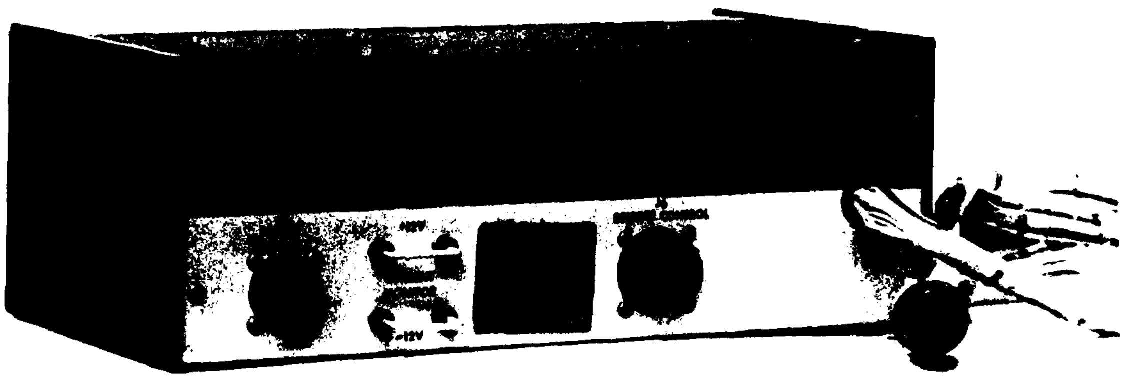

Fig. 3-3. Rear Panel of MTM Controller

Table 3-2. Magnetic Tape Memory Controller:
Controls and Indicators

Control	Function
REC Switch and Indicator	Applies power to record electronics while advancing tape.
REPRO Switch and Indicator	Applies power to reproduce electronics while advancing tape. If data are present, the DATA PRESENT indicator will be illuminated.
F-REV Switch and Indicator	Reverses tape direction while unit is in REPRO mode. DATA PRESENT indicator will be illuminated if there are data on the tape.
STOP Switch and Indicator	Terminates any of the above commands.
FWD Switch and Indicator	Sets the recorder to operate in the forward direction. Read track will be set to track 1, record track will not be changed. A REC or REPRO command is required to initiate tape motion.
FAST ENABLE Switch and Indicator	Causes tape to move at high speed when operating in REC, REPRO, or F-REV modes.
ERASE ENABLE Switch and Indicator	Permits erasure of tape in any mode.
BIAS ENABLE Switch and Indicator	Not functional. Illuminates when recorder is up to speed and ready to accept record data. Valid in REC mode only.
READY Indicator	Illuminates when recorder is up to speed and ready to accept record data. Valid in REC mode only.
BOT Indicator	Illuminates when clear leader at beginning of tape is sensed. Indicator will not light in STOP mode.
EOT Indicator	Illuminates when clear leader at end of tape is sensed.
TRACK Indicator	Designates whether recorder is in track 1 or 2. Tracks 3 and 4 are not functional in this system.
ERROR Indicator	Illuminates when internal real time detector detects an error in the reproduce data.
DATA IN and DATA OUT Ports	Not used

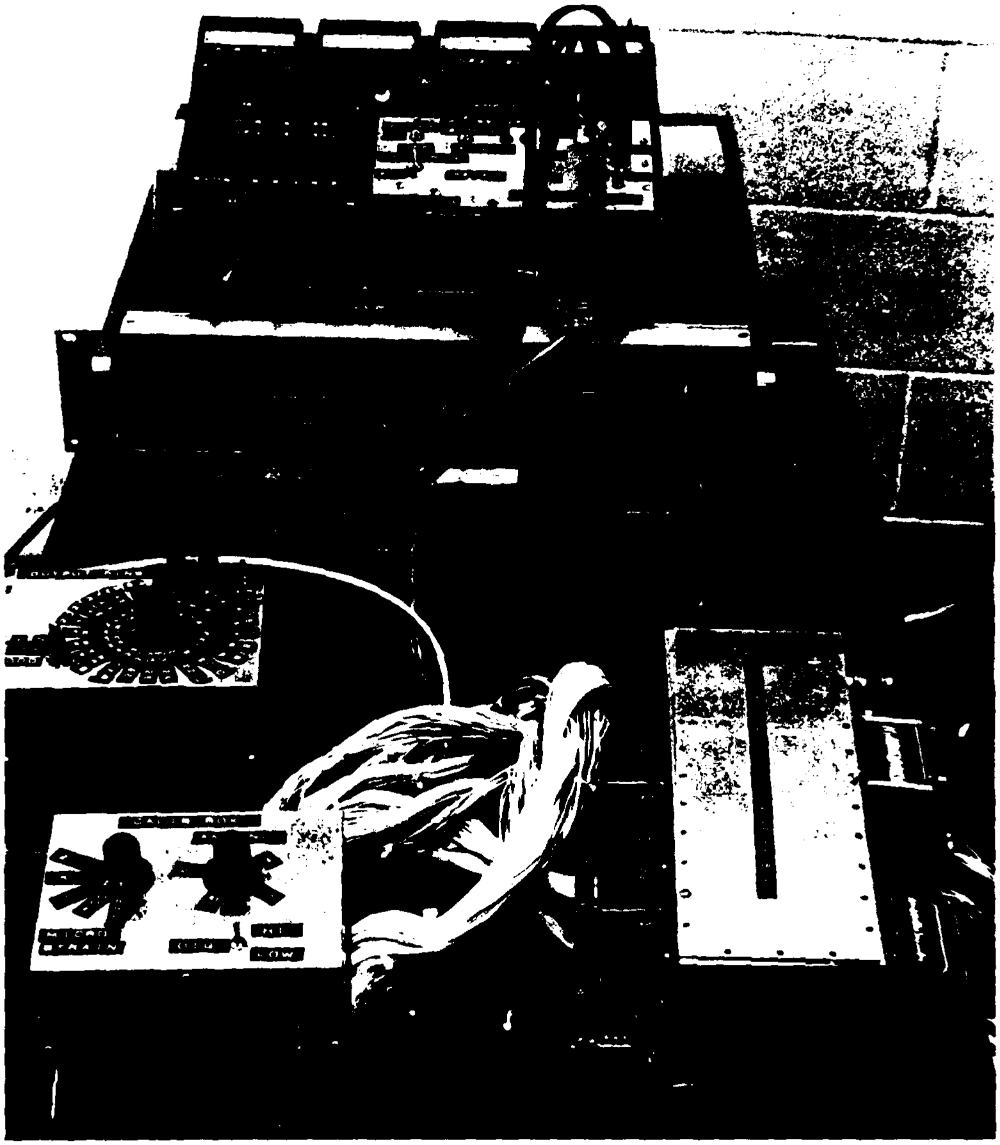

Fig. 3-4. Aerospace GSE

in to EPDS and its ground support equipment. The TRS 80 microcomputer is used for decoding the Kennedy tape during the ground qualification tests.

3.2.1 Pulse Command Sequencer

The pulse command sequencer is located in a separate ground enclosure (Fig. 3-5). Its one output plug connects to the SCU socket J2. The functional block diagram for the pulse command circuitry is shown in Fig. 3-6. The decision enable (DEC ENA) pulse to turn on the SCU is a resettable one-shot, triggered either by the internal 10-Hz oscillator or by an external pushbutton switch. The pulse is 30 msec wide, as is that of the EPDS, and repeats every 3.5 (or 5) min. After the normal 20-sec SCU warmup, the sequencer receives the decision (DEC) pulse from the SCU. In the internal mode, this pulse is fed back to the SCU as an enable (EBL) pulse. After a 5-sec delay, a 30-msec decision disable (DEC DBL) pulse turns the SCU off. In the external mode, no EBL pulse is sent. The SCU is shut down either by the SCU internal 40-sec timer, or by externally triggering the DEC DBL pulse.

3.2.2 Load Simulator

In Table 3-3 are listed the different transducers, the dummy load substituted, and the data simulated. The data points are typical values that would be obtained from the transducers during the mission. These dummy loads, which are located in a separate ground support enclosure (Fig. 3-7), connect to the SCU input ports as detailed in the wire lists for plugs P3, P4, P5, and P6. A current of 160 mA to simulate a 1-sun reading from each solar cell must be provided from an external current supply to each of the six solar cell inputs located on the dummy load box. The strain level from zero to 2000 microstrains is selected by a switch on the box. A dummy load that mimics this level is applied to only one of the 20 strain gauge amplifiers. A separate switch is used to indicate which amplifier is activated. Digital bits 1 to 10 from the Boeing experiment can be placed in either a high or a low state for simulation tests. The EPDS/SCU switch provides the option of using either the EPDS or the SCU for power.

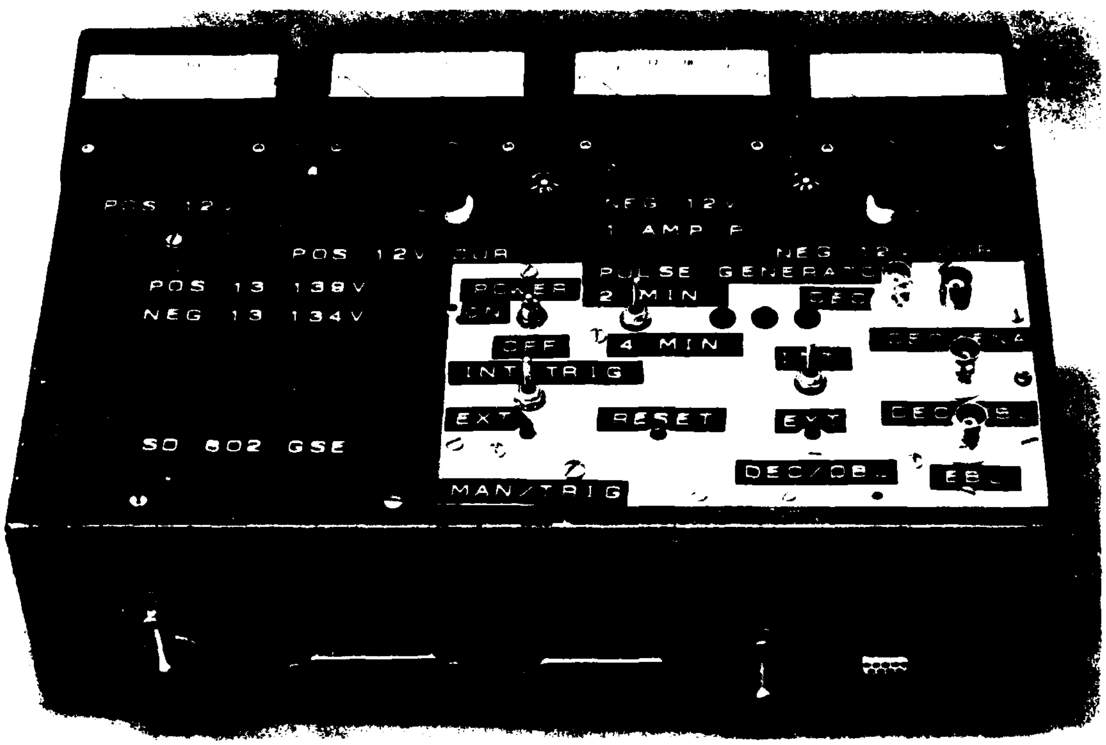

Fig. 3-5. Aerospace Pulse Command Sequencer (GSE)

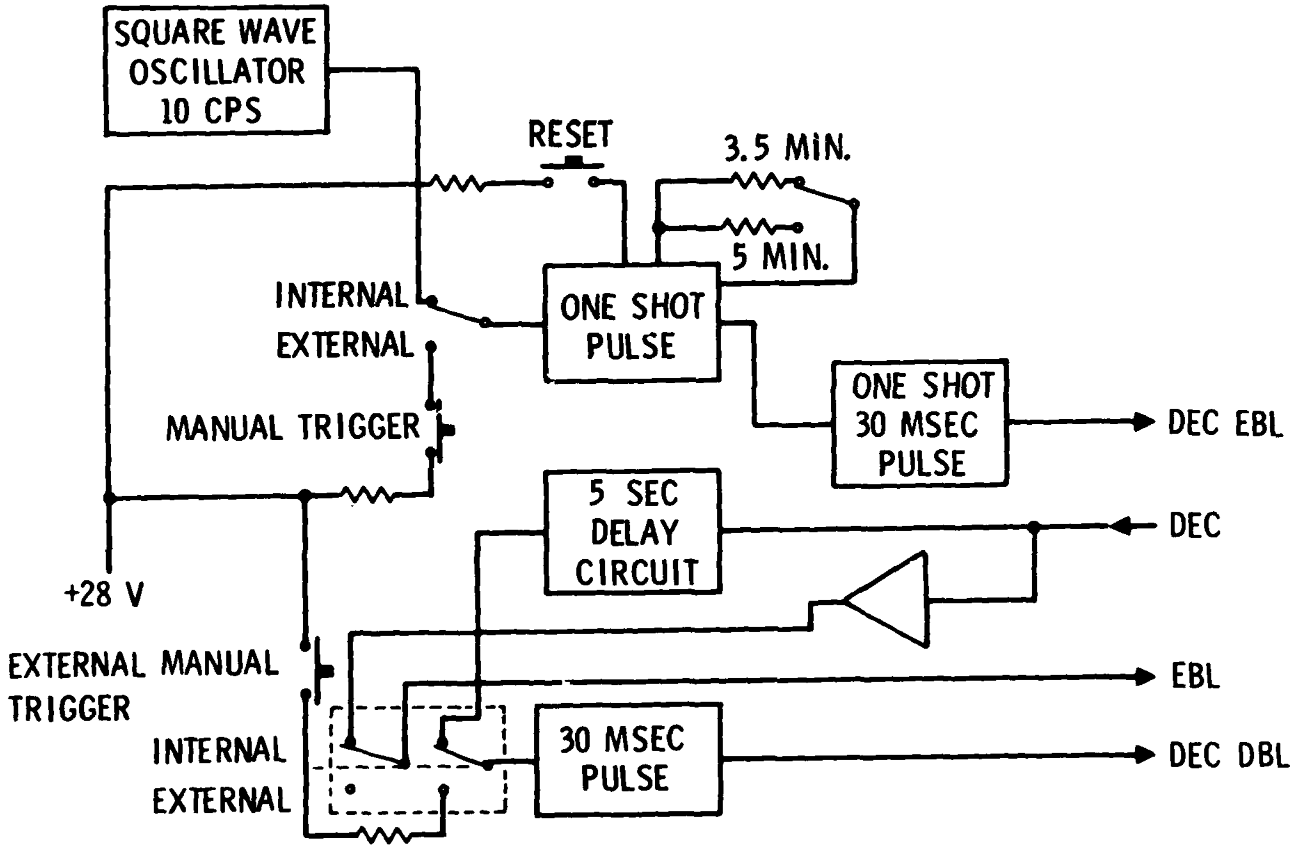

Fig. 3-6. Pulse Command Sequencer Functional Block Diagram

Table 3-3. SCU Loads Simulated

Transducer	Dummy Load	Data Simulated
Wide range thermistors	10 KΩ 1%	25°C
Composite thermistors	15 KΩ	15°C
Low range thermistors	300 KΩ	-59°C
High range thermistors	10 KΩ	+52°C
Strain gauge	1 KΩ (±0.02% at 25°C)	0 μstrain at 25°C
	1 KΩ shunted with 999 KΩ	500 μstrain
	1 KΩ shunted with 499.5 KΩ	1000 μstrain
	1 KΩ shunted with 333 KΩ	1500 μstrain
	1 KΩ shunted with 249 KΩ	2000 μstrain
Solar cell	160 mA	One sun
Fiber optic digital	+ 5 V	Logic high
Quartz crystal monitor	+ 5 V	Logic high

Fig. 5-7. Transducer Load Simulator

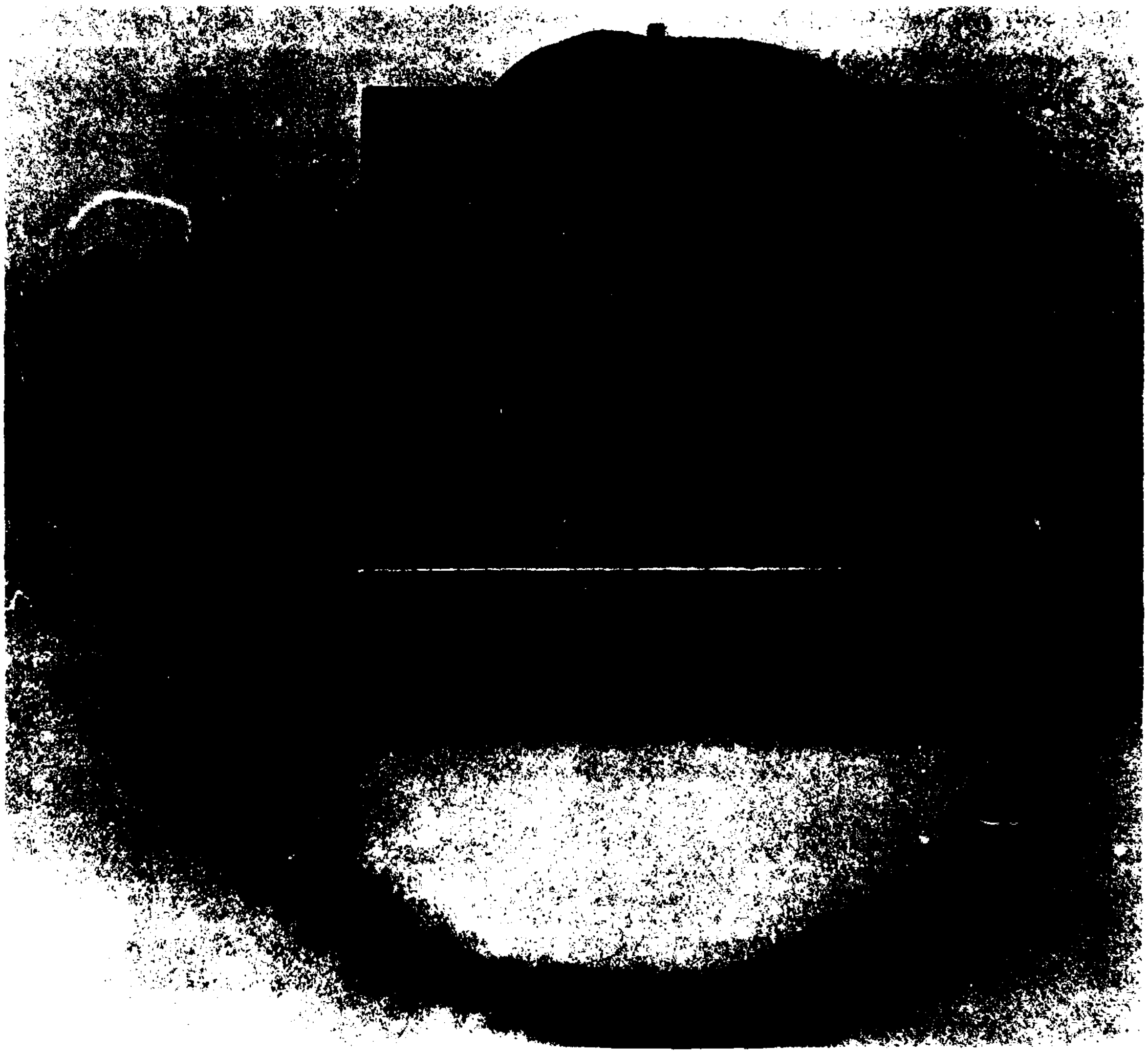

Fig. 3-8. Channel Selector Probe

3.2.3 Channel Selector Probe

The SCU outputs can be read with a channel selector probe (Fig. 3-8) during each DEC ENA cycle of the pulse command sequencer. This probe has only one connector plug and must be inserted in each one of the four output sockets (J7, J8, J9, or J10). Each connector pin pair (signal channel) must be read out separately. A 24 position rotatory switch is used to dictate which of the 24 pairs is to be read. A separate toggle switch must be used to sample the output from the twenty-fifth pair. The output from this probe is fed to a digital voltmeter. The output from each pin and socket is then compared to the output wire lists of J7, J8, J9, and J10.

3.2.4 Power Supply

The power supply shares and powers the same enclosure as the command sequencer. The four meters across the top provide for measuring the ±12-V power supply voltages and currents. Current loops are provided in series with each supply to permit the monitoring of transient currents with an oscilloscope. Each supply is fused separately. When the BYPASS switch on the right front panel is set to the internal position, this supply provides ±12 V power to the SCU. No EPDS GSE or external batteries are needed. In this mode, plug J12 on the power supply connects directly to J1 on the SCU. If the EPDS GSE is used with the SCU, the DDB provides the +12-V power and the Aerospace power supply provides the -12-V power to the SCU. The DDB does not have a -12-V source. In this mode, the BYPASS switch is set to the external or GSE position, the GSE cable from P3 is routed to P751A on the supply, and a cable from S751A with the needed -12 V for the SCU is connected to the EPDS plug 751, which in turn routes power through a different cable to the SCU power input plug P1. Connector J12 on the power supply is not used in this situation.

4. TEST PLANS

Preflight tests of the signal conditioning unit (SCU) at the box level and at the system level will be made to calibrate the units and to verify the reliability of the instrument package for this LDEF flight. The proposed test plan is outlined in Fig. 4-1.

Many of the proposed tests, i.e., the flight level system checkouts, are repeated many times to verify a proper system operation. The vibration flight acceptance test and the thermal-vacuum qualification test, however, need be performed only once. The order and the number of repeated tests may change, whereas the sequence of one-time system checkouts is not likely to change.

The test plan progress is from the box level checkout of the flight instrumentation to a full-up flight system test after installation on the LDEF. System checkouts are proposed before and after each qualifying test, each storage period, and each shipment to NASA facilities. NASA is responsible only for the vibration flight acceptance test; Aerospace is responsible for all other tests. The flight electronics tests will incorporate simulated loads for the preliminary tests until the actual transducers are mounted in the trays. In later electronics tests, the actual flight transducer will be used in the trays.

4.1 BOX LEVEL TESTS, SIGNAL CONDITIONING UNIT

4.1.1 Checkout of SCU Electronic Functions

For these tests, the experimenter connects the Aerospace ground support equipment (GSE) to the SCU as shown in Fig. 4-2. The dummy loads described in Section 3.2.2 simulate signals from the transducers to the four SCU input connectors P3, P4, P5, and P6. The pulse command sequencer and power supply provide the necessary commands and power to connectors J2 and P1. The power supply is operated with the BYPASS switch in the internal position. The output signals from the SCU during each ON cycle are read by inserting the channel selector probe into each output port (J7, J8, J9, and

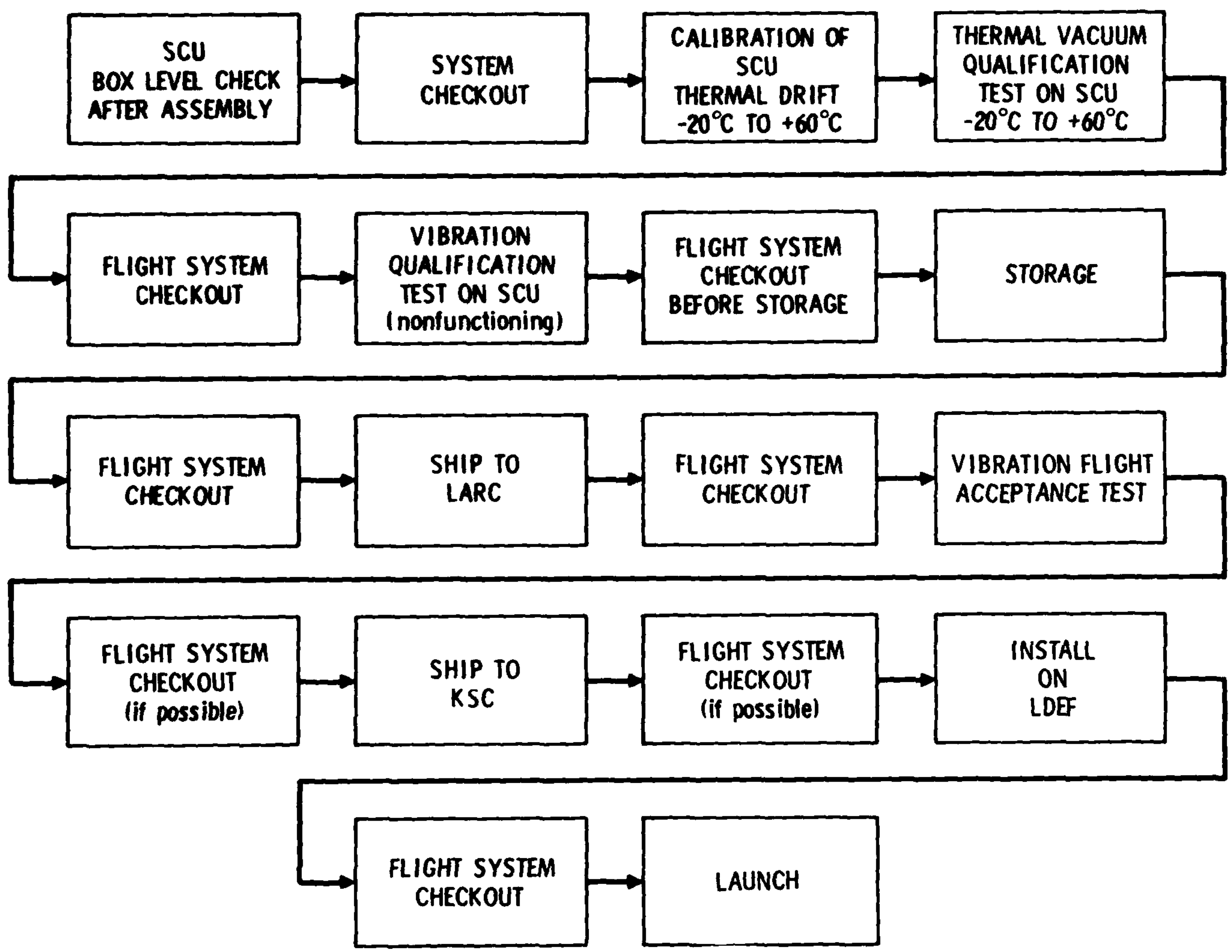

Fig. 4-1. Test Plan

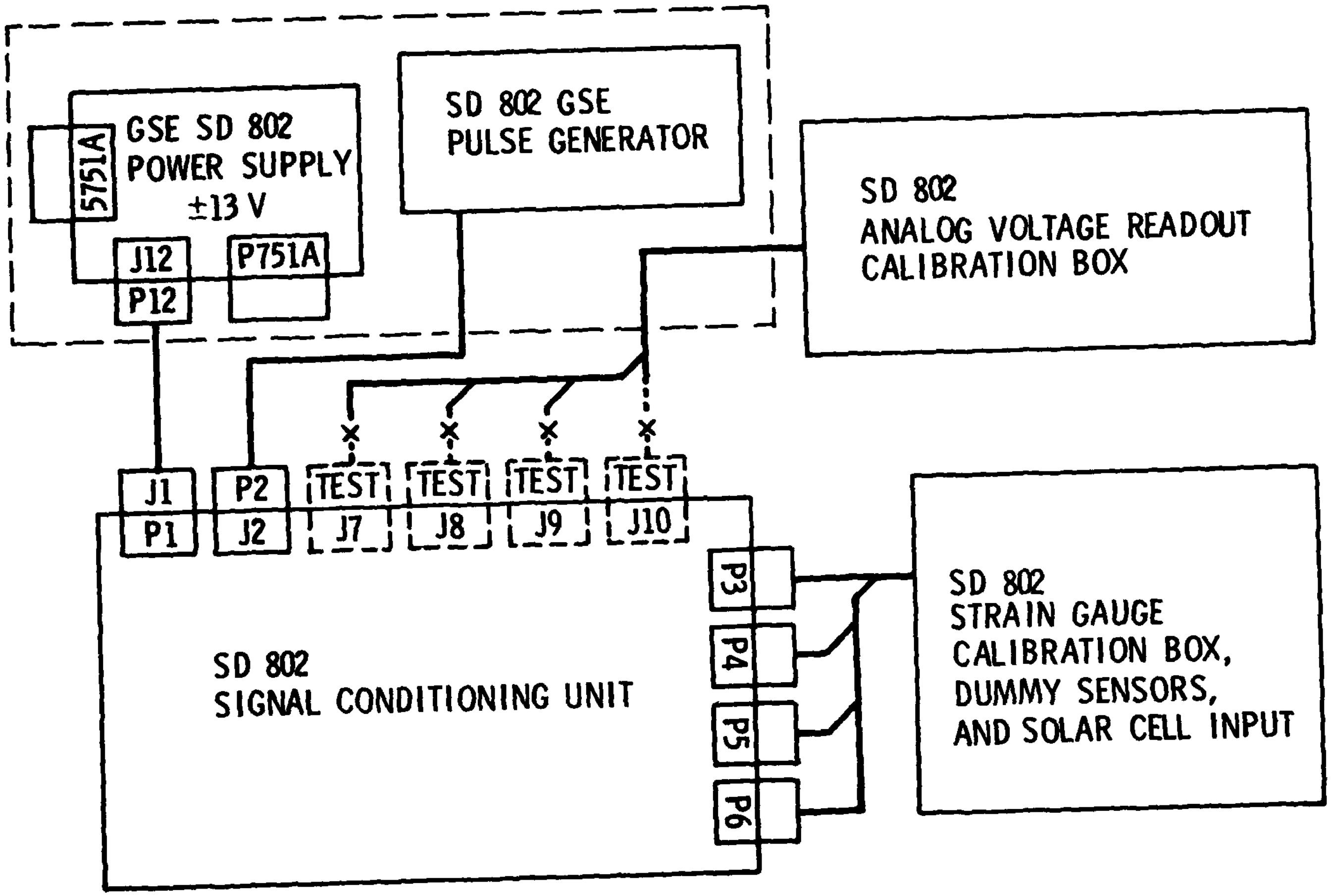

Fig. 4-2. SCU Box Level Test Interconnections

J10) and manually switching the selector position to each of the connector pin pairs that constitutes a signal channel. The digital voltmeters measure the signal voltage across each of these pairs.

The minimum and maximum allowable electrical signals are listed in Table 4-1 for the command signals, SCU regulators, and input power. A 1% accuracy in the analog measurements is desired for this mission. Therefore, the measured analog outputs in the checkouts should not deviate more than 1% from those listed in the output wire lists. The measurement obtained from the strain gauges must compensate for the thermal drift of each amplifier. Thermal drift of each amplifier over the mission temperature range (-20 to 60°C) will be measured at this checkout stage.

4.1.2 Vibration Qualification Test

Vibration tests are performed to identify the response frequency of the SCU and to demonstrate its structural integrity when exposed to a qualification level test environment. The adverse environment tests have already been performed on the experiment power and data system (EPDS). The SCU test will be conducted while it is not activated.

The vibration test will follow a procedure similiar to that for the LDEF experimental trays (Ref.5). The probable order of testing for each of the three orthogonal axes is a sine survey, sine qualification, and random qualification vibration. The sine survey is a low-level sweep from 5 to 2000 Hz at two octaves/min to permit the frequency responses to be identified. The input excitation cannot exceed 0.5 g zero to peak. After the sine survey, the sine qualification test is applied following the specifications of Table 4-2.

The last vibration test per axis is a qualification random vibration with a power spectral density within ±3 dB of the frequency shown in Fig. 4-3. The attenuation below 10 Hz and above 1600 Hz should be greater than 24 dB/octave. The less demanding sine and random flight acceptance tests for each axis will be completed later by NASA.

Table 4-1. Signal Conditioning Electronic Control Unit

Parameter	Requirement Min	Requirement Max	Actual Measurements at +25°C
Input voltage (Pos)	+12.0 V	+15.0 V	13.5 V
Input voltage (Neg)	-12.0 V	-15.0 V	13.5 V
Positive input power	0	200 mA	170 mA
Standby	0	0.3 mA	0.3 mA
Negative input power	0	200 mA	130 mA
Standby	0	0	0
+5 V I regulator	4.95 V	5.05 V	5.005
+5 V II regulator	4.95 V	5.05 V	5.003
-5 V III regulator	4.90 V	5.10 V	5.055
DEC ENA pulse	15 msec	40 msec	
DEC DBL pulse	15 msec	40 msec	
Power up time (+12 V and -12 V) K1 relay ON	40 sec	80 sec	
DEC level high	7.0 V	8.4 V	7.65 V
Delayed time	20 sec	30 sec	22 sec
DEC-DBL shut down Time K2 relay ON	10 msec	30 msec	
EBL level	4.5 V	8.5 V	
EBL pulse delay	20 sec	30 sec	22 sec

Table 4-2. Sine Qualification Testing Specification*

Input Amplitude	Frequency Range (Hz)	Sweep Rate
0.75-in.double amplitude	5-14	2 oct/min
±7.5 g	14-20	2 oct/min
±1.5 g	20-35	2 oct/min

*From Ref. 2.

4.2 FLIGHT SYSTEM LEVEL TESTS

The preliminary flight system checkouts on the ground will require use of simulated loads for the transducers, external power and ground support equipment for controlling the flight electronics (Figs. 4-4 and 4-5). After assembly of the LDEF trays, the flight system will be checked out using the actual flight transducers, powered by internal batteries, with the flight electronics under EPDS control (Fig. 4-6).

Some tests of the flight system need be made only once, i.e., check of EPDS general programming features. Other tests must be performed periodically regardless of the test schedule, i.e., the exercising of the magnetic tape memory (MTM) every 6 months. A preliminary test of the EPDS programming in the first flight system checkout verified that actual EPDS programming matches exactly the programming format (Tables 2-1 and 2-2) we requested from NASA. The Lockheed MTM must be exercised every 6 months to prevent the magnetic tape from taking a set. This procedure entails advancing the tape in the fast mode from beginning to end of tape and then reversing direction, stopping when the beginning of tape is reached.

4.2.1 Flight System Functional Test Procedure

The following procedures are to be followed for the flight system functional test.

4.2.1.1 Component Interconnection

When using the GSE equipment for flight system tests, connect all components as shown in Figs. 4-4 and 4-5 using the same simulated loads as in the SCU box level tests. Battery power is optional. The actual connections of the flight system as the experiment would fly are shown in Fig. 4-6.

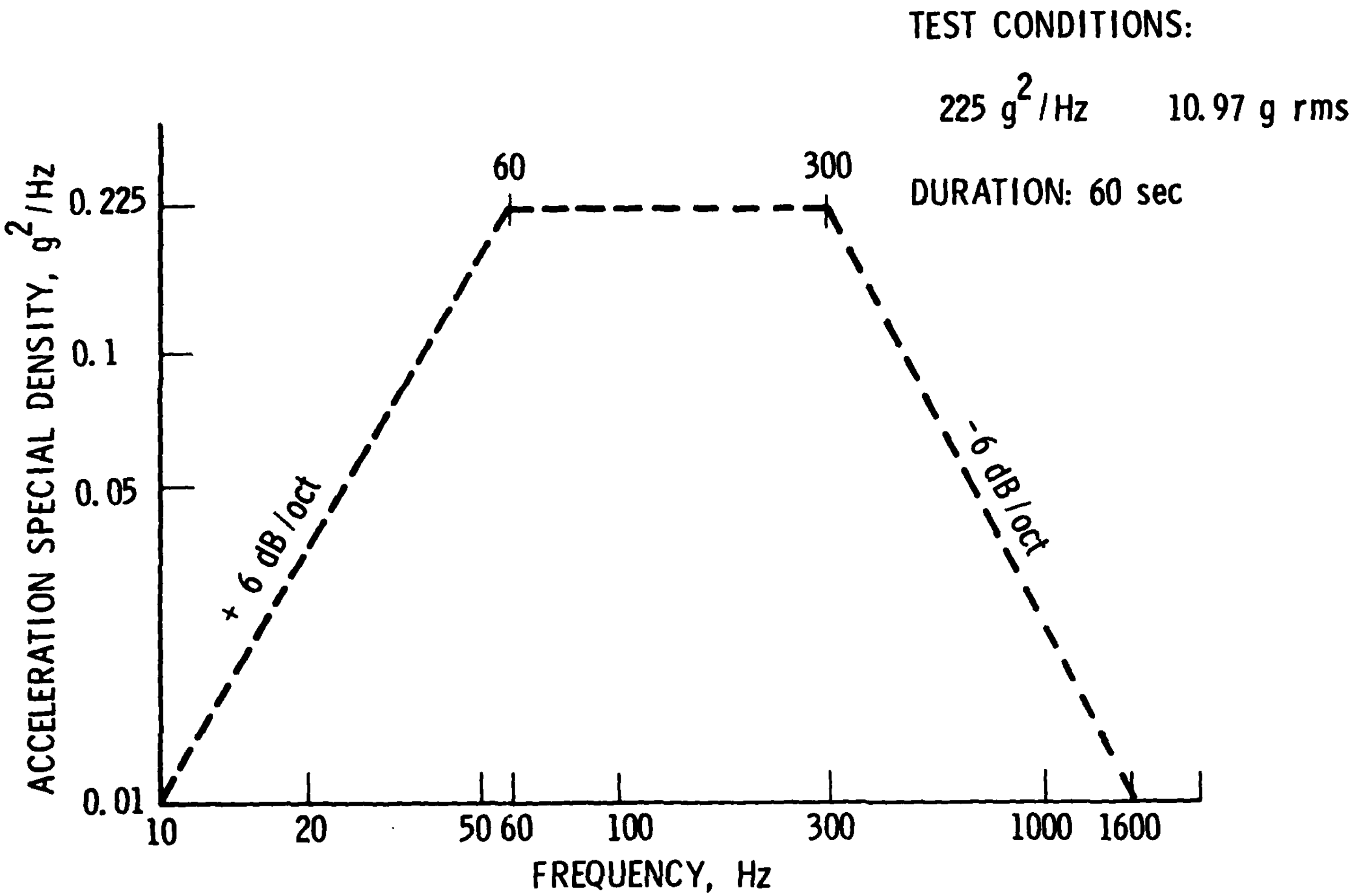

Fig. 4-3. Random Vibration Conditions for Developmental and Qualification Tests (From NASA Flight Qualification Specification, Ref. 2)

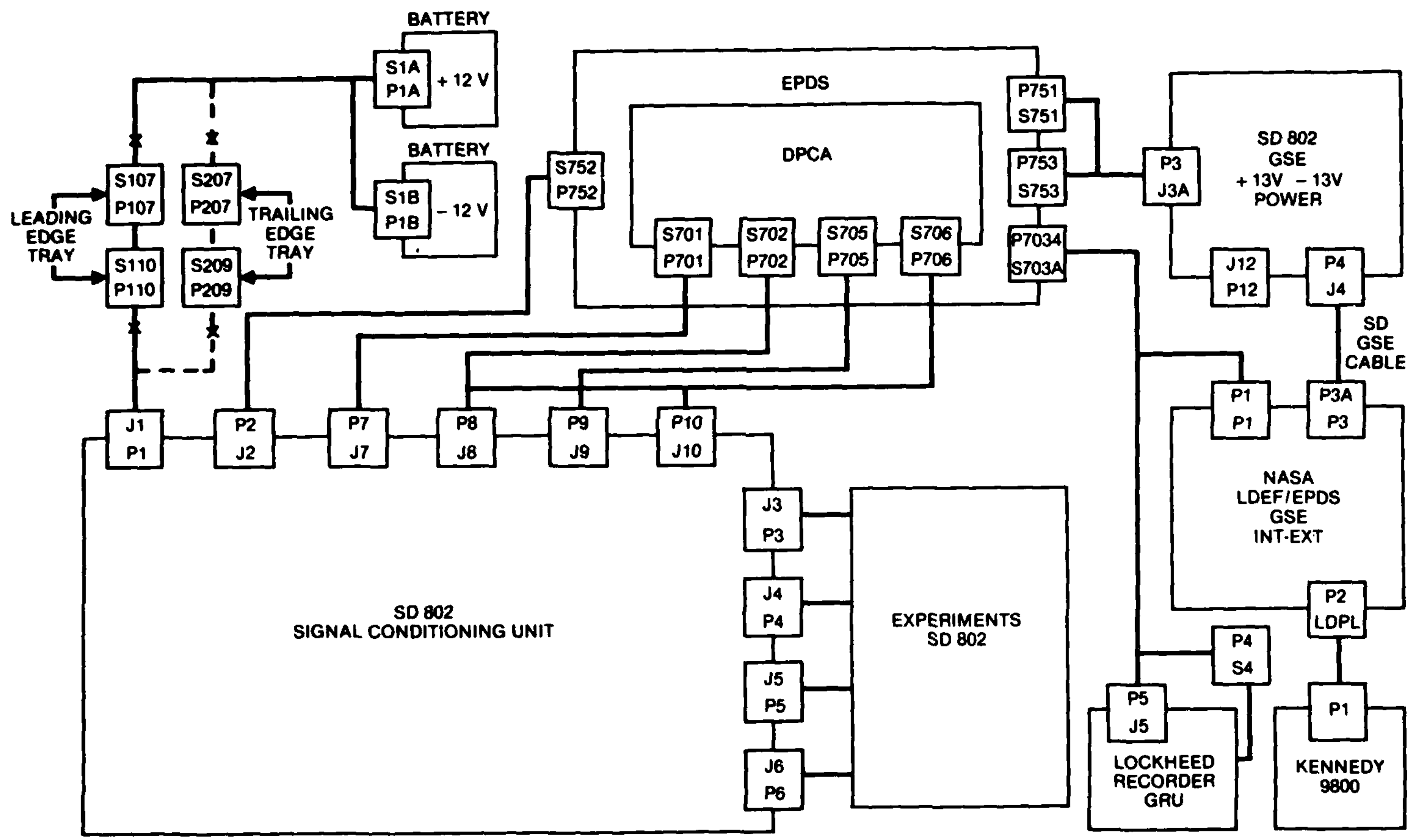

Fig. 4-4. Flight System Interconnections
Simulated Loads/GSE

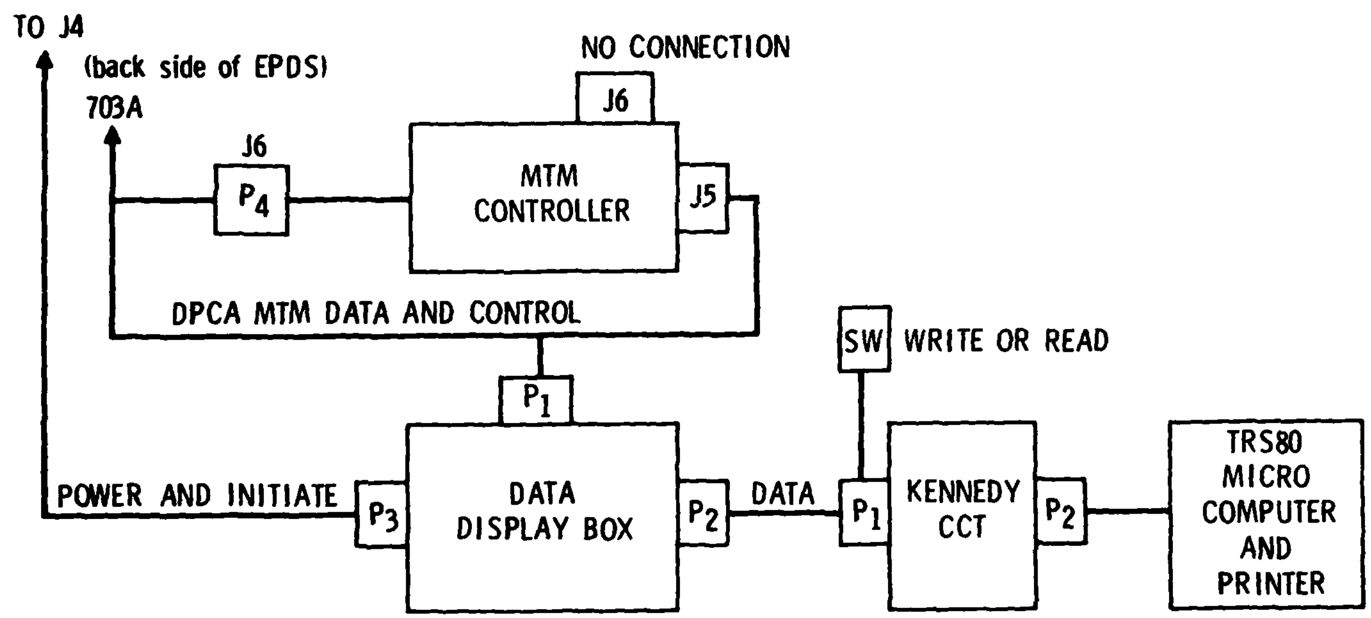

Fig. 4-5. Ground Support Equipment Interconnections

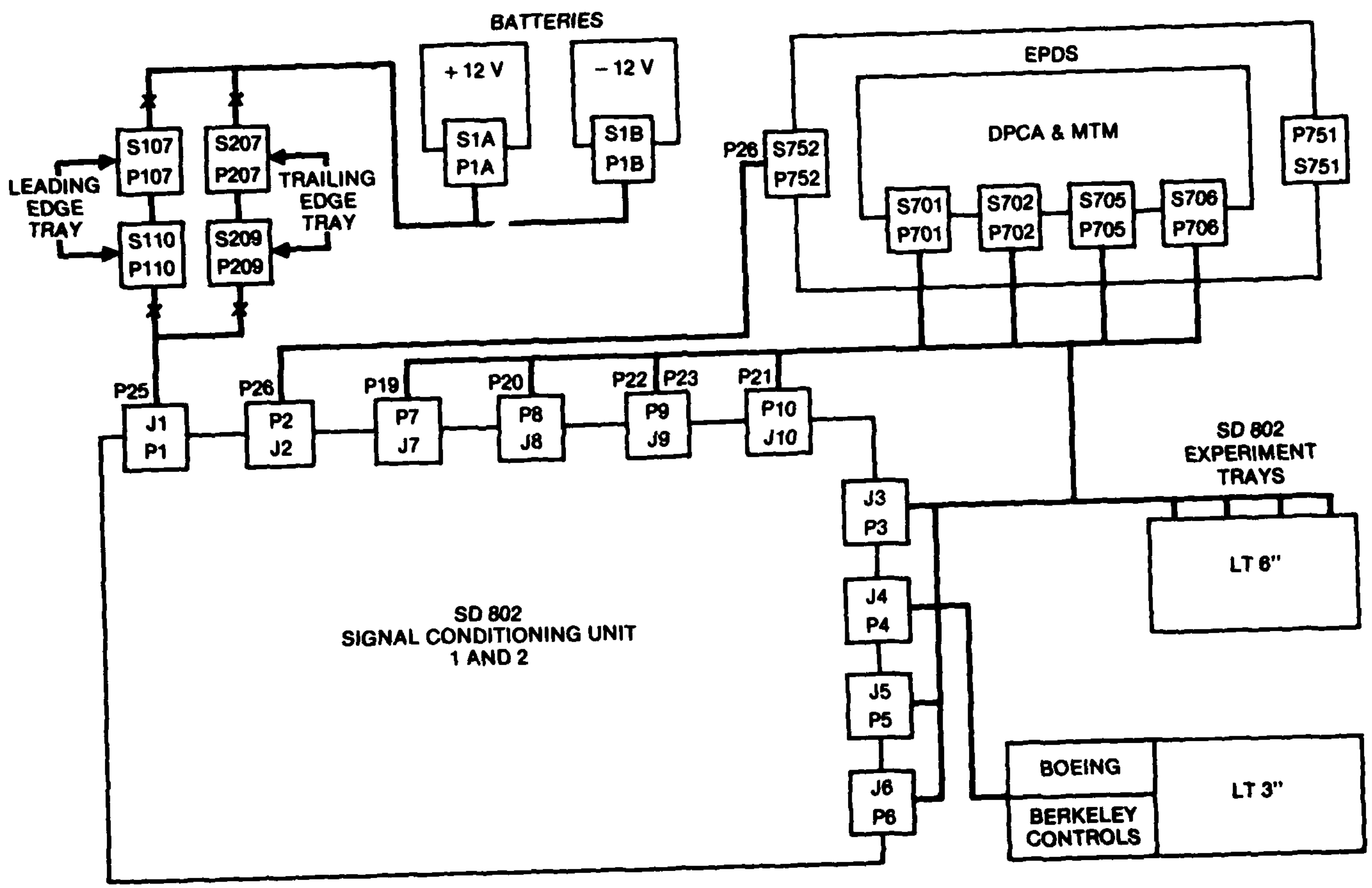

Fig. 4-6. Flight System Interconnections
Transducers/Batteries

4.2.1.2 Standby Mode

A. Initialize Circuits. Initialize all circuits before turning GSE power ON.

DDB

Control	Power
• EPDS ac power	OFF
• ± 12 V EPDS	OFF
• ± 12 V Exper	OFF
• Select EPDS power	Ext. EPDS (no batteries used)
• CON1	HI
• $\overline{\text{CT}}$	LOW
• CON2	PROG
• DPCA	MANUAL (MTM control)
• OCTAL/DEC	DEC
• ALL DATA/SEL WORD	ALL DATA

SD GSE

Control	Position
• ac power	OFF
• BYPASS	EXT

B. <u>GSE Power Turnon</u>. After initializing, turn on the GSE power.

Control	DDB Position	Results
• ac power	ON	Power Bulb ON
		Reset LED ON
		Printer ON
		Random DPCA Data Word
		−7.5 V on 7.5-V meter
		± 12 V on 12-V meter
• −7.5 V EPDS	ON	~ 580 μA of standby current
• −12 V EPDS	ON	~ 300 μA of standby current using current probe
• −7.5 V Exper	ON	
• −12 V Exper	ON	
• RESET printer momentary ON		
	SD GSE	
• ac power	ON	Meter voltage ± 13 V

C. Position MTM Tape. While in the standby mode, reposition a clean MTM tape to the start position with the MTM controller before taking or playing back any data.

- Set in Manual. The DDB DPCA/MANUAL switch must be in the MANUAL position for the MTM controller to operate the tape.

- Rewind Tape. Depress F-REV switch and permit tape to run back to BOT. The F-REV, REPRO, TRACK 1, and possibly DATA PRESENT LEDs will be active while the tape rewinds.

- Tape Advance. Press FWD and REPRO switches to advance the tape for a period 2 min longer than the recording time needed. Push STOP switch. The tape will have advanced on TRACK 1.

- Erase Tape. Set ERASE ENABLE switch to ON. Actuate F-REV switch to erase the tape until the BOT, or stop when the starting point is reached. Turn ERASE ENABLE off.

- Advance to Start Position. Actuate FWD and REC switches to advance tape for 1 min to ensure the tape is not in any worn area near the BOT. Push the STOP switch.

- Ready. An erased tape section is now ready for a data run. The run time must be less than 2 min of the erase time.

4.2.1.3 Operating Modes

The flight system is now ready to operate. The sequences of the three basic operating modes are:

A. Data Acquisition. Acquire data from experiments, store the information on the MTM tape, and monitor data channels with the DDB.

- DPCA. The DDB DPCA/MANUAL switch must be in the DPCA position to transfer data to MTM tape.

- INITIATE SET. Send an INITIATE SET command from the DDB, performed by the shuttle at payload separation, to place EPDS in the programmed, repetitive, accelerated test mode, operating on GSE power. After a wait of 3 min, the DPCA and SCU will power up and place data on the MTM tape every scan. The printer will have time to print only five sequential data channels each scan. Data channels can also be read using the SEL WORD command and thumbwheels to select the data channel to be printed. The READY, FWD, REC, and TRACK 1 LEDs on the MTM controller and the GSE ammeters should indicate activity. When the data run is complete, place the system on standby.

- Standby. Reset the INITIATE switch to place system o· ·andby.

- Rewind MTM TAPE. Place the DPCA/MANUAL switch to MANUAL and rewind the MTM tape until BOT. Run forward in REC mode 50 sec and STOP.

- Ready. An encoded tape section is now ready for transfer to a computer compatible tape.

B. Data Transfer. Transfer the MTM tape contents onto a computer compatible tape.

- Set in MANUAL. The DDB DPCA/MANUAL switch must be in the MANUAL position during the data transfer.

- Mount CCT. Mount on the Kennedy recorder a computer compatible tape with a Write Enable ring.

- ON. Turn the Kennedy recorder power ON. WRITE ENABLE will light.

- Rewind CCT to BOT.

- WRITE. Set READ/WRITE enable switch to WRITE.

- LOAD Tape. LOAD will light.

- ON LINE. Place recorder ON LINE. WRITE STATUS will light.

SYSTEM READY FOR TRANSFER

- Transfer. Press REPRO and FWD switches on MTM controller to start transfer. DATA PRESENT on controller and DATA IN MEMORY on recorder should indicate transfer activity. The recorder will transfer data and stop the CCT only when data are present on the MTM tape. When data transfer is completed, the recorder will stop stepping and the DATA PRESENT LED will extinguish.

- STOP. When transfer is complete, stop the MTM tape from advancing further by using the STOP command on the MTM controller.

- Rewind CCT to BOT.

C. Data Transcription. Computer transcription of the CCT.

- READ. Switch the READ/WRITE switch on the Kennedy recorder to READ.

- LOAD TAPE.

- ON LINE. Place recorder ON LINE. DATA MEMORY will extinguish.
- Transcribe. The system is now ready to be transcribed by the TRS 80 microcomputer. Follow the instructions in Appendix B.

4.2.1.4 Flight Data

The retrieved flight tape will be transcribed by the same procedure as that described in Section 4.2.1.3, except that a full-size computer will replace the TRS 80 and process the data directly from the CCT.

4.2.2 Thermal-Vacuum Qualification Test

Each LDEF data recording network will be evaluated while the SCU is exposed to three cycles of thermal-vacuum stress (Fig. 4-7). The cycle consists of a ramp down from ambient to $-20°C \pm {}^{0}_{5}$, a ramp up to $+60°C \pm {}^{5}_{0}$, and a ramp down to ambient. Functional tests during each cycle will be made during the periodic stabilizations at -20, 0, +20, +40, and +60°C. The ramp $\Delta V/\Delta T$ must not exceed 100°F/hr. The EPDS package has passed a similar thermal stress given test by NASA. The interconnection of the component and test measurements are the same as for the flight system checkout (Section 4.2.1). Two cable adapter fixtures are needed for operating with our test chamber. The only additional parameter to measure will be operating temperature. Care must be taken to stay within the temperature range and rate assigned.

Fig. 4-7. Thermal-Vacuum Qualification Test

5. REFERENCES

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4. Operating Manual for the Mark 5 Type 4200 Magnetic Tape Recorder and Reproduce Unit, Manual No. 3A0177, Lockheed Electronics, Industrial Technology Division (1979).

5. DiGiacomo, A. F., Qualification Vibration Test Report for SD 802 Materials Experiment, TR-0081(6950-05)-1, The Aerospace Corporation (to be published).

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SYMBOLS

A	Aerospace
A/D	analog-to-digital
AFAL	Air Force Avionics Laboratory
AFAPL	Air Force Aero-Propulsion Laboratory
AFFDL	Air Force Flight Dynamics Laboratory
AFML	Air Force Materials Laboratory
BOT	beginning of tape
CCT	computer compatible tape
CMOS	complementary metal oxide semiconductor
CON1	control line no. 1
DDB	data display box
DEC	decision pulse
DEC DBL	decision disable pulse
DEC ENA	decision enable pulse
DPCA	data processor controller assembly
EBL	enable pulse
EPDS	equipment power and data system
GSE	ground support equipment
HTT	high-temperature thermistor
IRST	initial reset
LDEF	Long Duration Exposure Facility
LTT	low-temperature thermistor
MDAC	McDonnell Douglas Astronautics Co.

PRECEDING PAGE BLANK-NOT FILMED

MTM	magnetic tape memory
NASA	National Aeronautics and Space Administration
QCM	quartz crystal monitor
RAM	random access memory
SCPM	solar cell package module
SCU	signal conditioning unit
SD	Space Division
WRT	wide range thermistor
YSI	Yellow Springs Instrument

APPENDIX A

SAMPLES, TRANSDUCERS, AND TRAYS

Various locations within each tray are instrumented for temperature monitoring, because there are not enough analog channels to permit the temperature of each experimenter's sample to be monitored directly. In this appendix, the locations of the transducers within the trays and the analog channels that record their data are identified. This list permits rapid identification of the data channel of the temperature monitoring point nearest to a given sample.

LEADING EDGE

Analog Channel	Agency	Tray	Module + Position No	Transducer Type	Experimenter's Number	Description of Monitored Item
1	AFAPL	L3	IV-23	SCPM	X3	Solar Module
2	AFAPL	L3	IV-22	SCPM	B	Solar Module
3	AFAPL	L3	IV-21	SCPM	VJ1	Solar Module
4	AFAPL	L3	IV-20	SCPM	GA1	Solar Module
5	AFAPL	L3	IV-19	SCPM	A	Solar Module
6	AFAPL	L6	VI-21	SCPM	1	Solar Module
7	NASA	L6	I	SHUNT	-	Current Sensor, DPCA/EPDS
8	NASA	L6	I	Voltage	-	5 V Sensor, DPCA/EPDS
9	NASA	L6	I	Voltage	-	12 V Sensor, DPCA/EPDS
10	A/AFFDL	L6	III	#1 WRT	?	Test Sample?
11	A/AFFDL	L6	III	#2 WRT	?	Test Sample?
12	A/AFFDL	L6	III	#3 WRT	?	Test Sample?
13	A/AFFDL	L6	III	#4 WRT	?	Test Sample?
14	A	L3	I	#1 LTT		Shield Plate, Quadrant 1
15	A	L3	III	#2 LTT		Sample Tray, Bottom Surface
16	A	L3	II	#3 LTT		Sample Tray, Bottom Surface
17	A	L3	IV	#4 LTT		Sample Tray, Bottom Surface
18	A	L6	III	#5 LTT		Bottom Surface, Separation Plate
19	A	L6	VI	#6 LTT		Sample Tray, Bottom Surface
20	A	L3	I	#1 HTT		Quadrant 4, Shield Plate
21	A	L3	III	#2 HTT		Sample Tray, Bottom Surface
22	A	L3	II	#3 HTT		Sample Tray, Bottom Surface
23	A	L3	IV	#4 HTT		Sample Tray, Bottom Surface
24	A	L6	III	#5 HTT		Bottom Surface, Separation Plate
25	A	L6	VI	#6 HTT		Sample Tray, Bottom Surface
26	AFAL	L3	I-1	#1 WRT	c	Resonant Reflector
27	AFAL	L3	I-2	#2 WRT	d	Circuit Analog Sheet
28	AFAL	L3	I-3	#3 WRT	a	Capacitive Grid
29	AFAL	L3	I-4	#4 WRT	b	Resonant Window
30	A	L3	III	#5 WRT		Test Sample Mounting Tray
31	A	L3	II	#6 WRT		Sample Tray, Bottom Surface
32	SD/MDAC	L3	II-51	#7 WRT		Sample Package

LEADING EDGE (Continued)

Analog Channel	Agency	Tray	Module + Position No	Transducer Type	Experimenter's Number	Description of Monitored Item
33	Berkeley Controls	L3	II-45	#8 WRT	12	QCM
34	A	L3	IV	#9 WRT		Sample Tray Base, Side Wall
35	A	L3	IV	#10 WRT		Sample Tray, Bottom Surface, Beneath Solar Cells
36	Boeing	L3	V	#11 WRT	8	Sample Package, Preassembled
37	Boeing	L3	V	#12 WRT	8	Sample Package, Preassembled
38	A	L6	III	#13 WRT		Vertical Surface, Mirror Holder
39	SD/MDAC	L6	VI-14	#14 WRT	IV	Sample Package
40	A	L6	VI	#15 WRT		Sample Tray, Bottom Surface
41	NASA	L6	I	Voltage	-	V. Temp., DPCA/EPDS
42	Boeing	L3	V	Voltage	-	Test Sample Monitor
43	A	L6	IV	#18 WRT	18	Signal Conditioning Unit
44	A	L6	IV	#19 WRT	19	Signal Conditioning Unit
45	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
46	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
47	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
48	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
49	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
50	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
51	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
52	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
53	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
54	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
55	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
56	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
57	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
58	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
59	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
60	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
61	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
62	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
63	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure
64	A/AFFDL	L6	III	Strain Gauge		Test Sample, Strain Measure

TRAILING EDGE

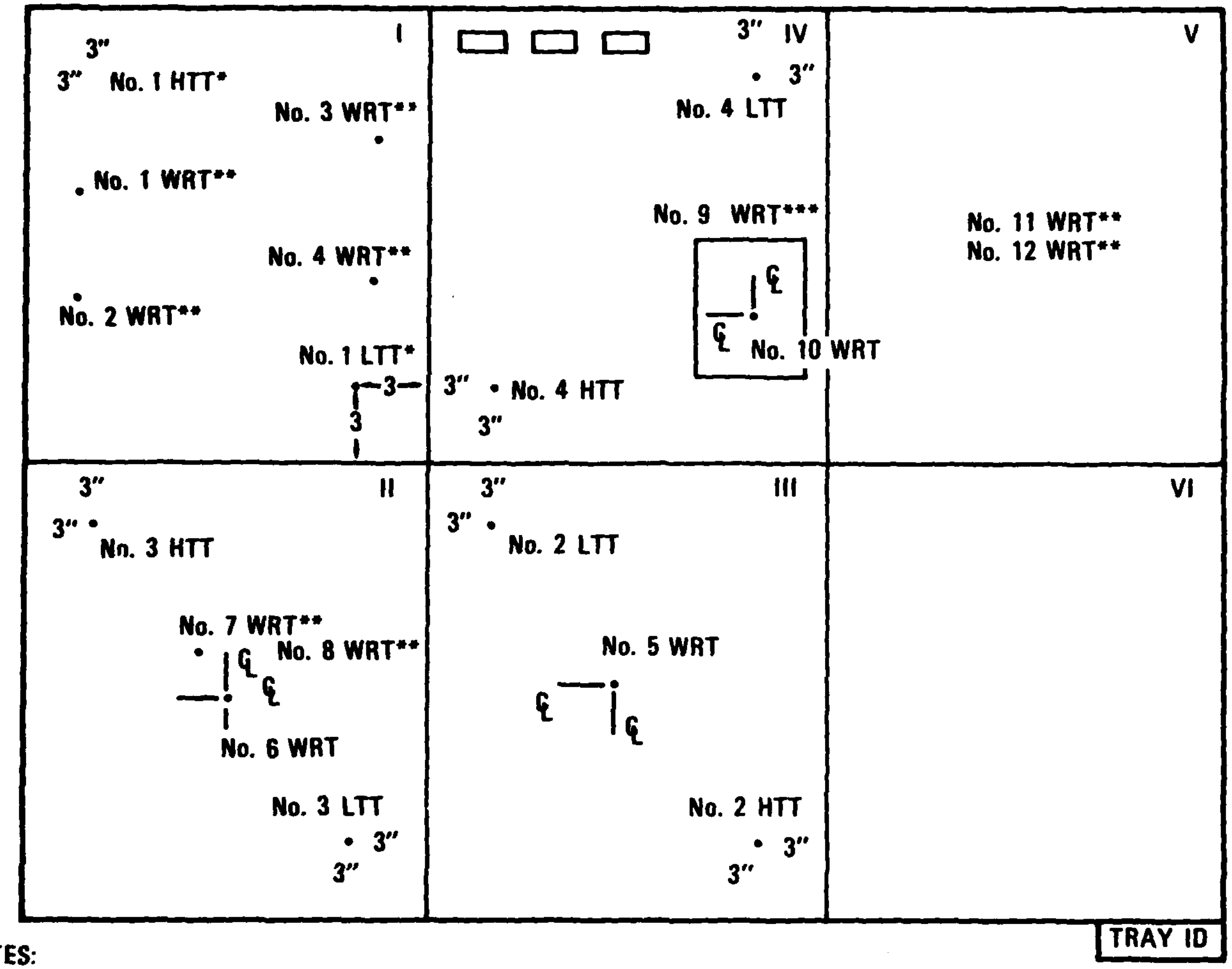
Analog Channel	Agency	Tray	Module + Position No	Transducer Type	Experimenter's Number	Description of Monitored Item
1	AFAPL	T3	IV-19	SCPM	c	Solar Module
2	AFAPL	T3	IV-20	SCPM	GA2	Solar Module
3	AFAPL	T3	IV-21	SCPM	VJ2	Solar Module
4	AFAPL	T3	IV-22	SCPM	D	Solar Module
5	AFAPL	T3	IV-23	SCPM	X4	Solar Module
6	AFAPL	T6	IV-22	SCPM	X2	Solar Module
7	NASA	T6	I	SHUNT		Current Sensor, DPCA/EPDS
8	NASA	T6	I	Voltage		5 V Sensor, DPCA/EPDS
9	NASA	T6	I	Voltage		12 V Sensor, DPCA/EPDS
10	A/AFFDL	T6	III	#1 WRT		Test Sample
11	A/AFFDL	T6	III	#2 WRT		Test Sample
12	A/AFFDL	T6	III	#3 WRT		Test Sample
13	A/AFFDL	T6	III	#4 WRT		Test Sample
14	A	T3	I	#1 LTT		Quadrant 1, Shield Plate
15	A	T3	III	#2 LTT		Sample Tray, Bottom Surface
16	A	T3	II	#3 LTT		Sample Tray, Bottom Surface
17	A	T3	IV	#4 LTT		Sample Tray, Bottom Surface
18	A	T6	III	#5 LTT		Bottom Surface, Separation Plate
19	A	T6	VI	#6 LTT		Sample Tray, Bottom Surface,
20	A	T3	I	#1 HTT		Quadrant 4, Shield Plate
21	A	T3	III	#2 HTT		Sample Tray, Bottom Surface
22	A	T3	II	#3 HTT		Sample Tray, Bottom Surface
23	A	T3	IV	#4 HTT		Sample Tray, Bottom Surface
24	A	T6	III	#5 HTT		Bottom Surface, Separation Plate
25	A	T6	VI	#6 HTT		Sample Tray, Bottom Surface
26	AFAL	T3	I-1	#1 WRT	c	Resonant Reflector
27	AFAL	T3	I-2	#2 WRT	d	Circuit Analog Sheet
28	AFAL	T3	I-3	#3 WRT	a	Capacitive Grid
29	AFAL	T3	I-4	#4 WRT	b	Resonant Window
30	A	T3	I	#5 WRT		Side Wall of Base
31	A	T3	III	#6 WRT		Sample Tray, Bottom Surface
32	SD/MDAC	T3	II-52	#7 WRT	A & B	Coating & Materials Package T3-11-6-52-1A & 3

TRAILING EDGE (Continued)

Analog Channel	Agency	Tray	Module + Position No	Transducer Type	Experimenter's Number	Description of Monitored Item
33	SD/MDAC	T3	II-51	#8 WRT	III	SPL Coatings. T3-11-6-51-111
34	Berkeley Controls	T3	II-45	#9 WRT	03	QCM, T3, -11-14-45-03
35	A	T3	IV	#10 WRT		Side Wall of Base
36	A	T3	IV	#11 WRT		Sample Tray, Bottom Surface, Beneath Solar Module
37	Boeing	T3	V	#12 WRT		Sample Package, Preassembled
38	Boeing	T3	V	#13 WRT		Sample Package, Preassembled
39	AFML/MDAC	T6	VI-20	#14 WRT	A	SMATH Materials
40	SD/MDAC	T6	VI-21	#15 WRT	2	SPL Coating-Solar
41	NASA	T6	I	Voltage		V. Temp. DPCA
42	A	T6	VI	#16 WRT		Sample, Tray, Bottom Surface, Beneath Solar Module
43	A	T6	IV	#18 WRT		Signal Conditioning Unit
44	A	T6	IV	#19 WRT		Signal Conditioning Unit
45	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
46	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
47	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
48	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
49	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
50	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
51	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
52	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
53	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
54	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
55	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
56	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
57	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
58	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
59	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
60	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
61	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
62	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
63	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure
64	A/AFFDL	T6	III	Strain Gauge		Test Sample, Strain Measure

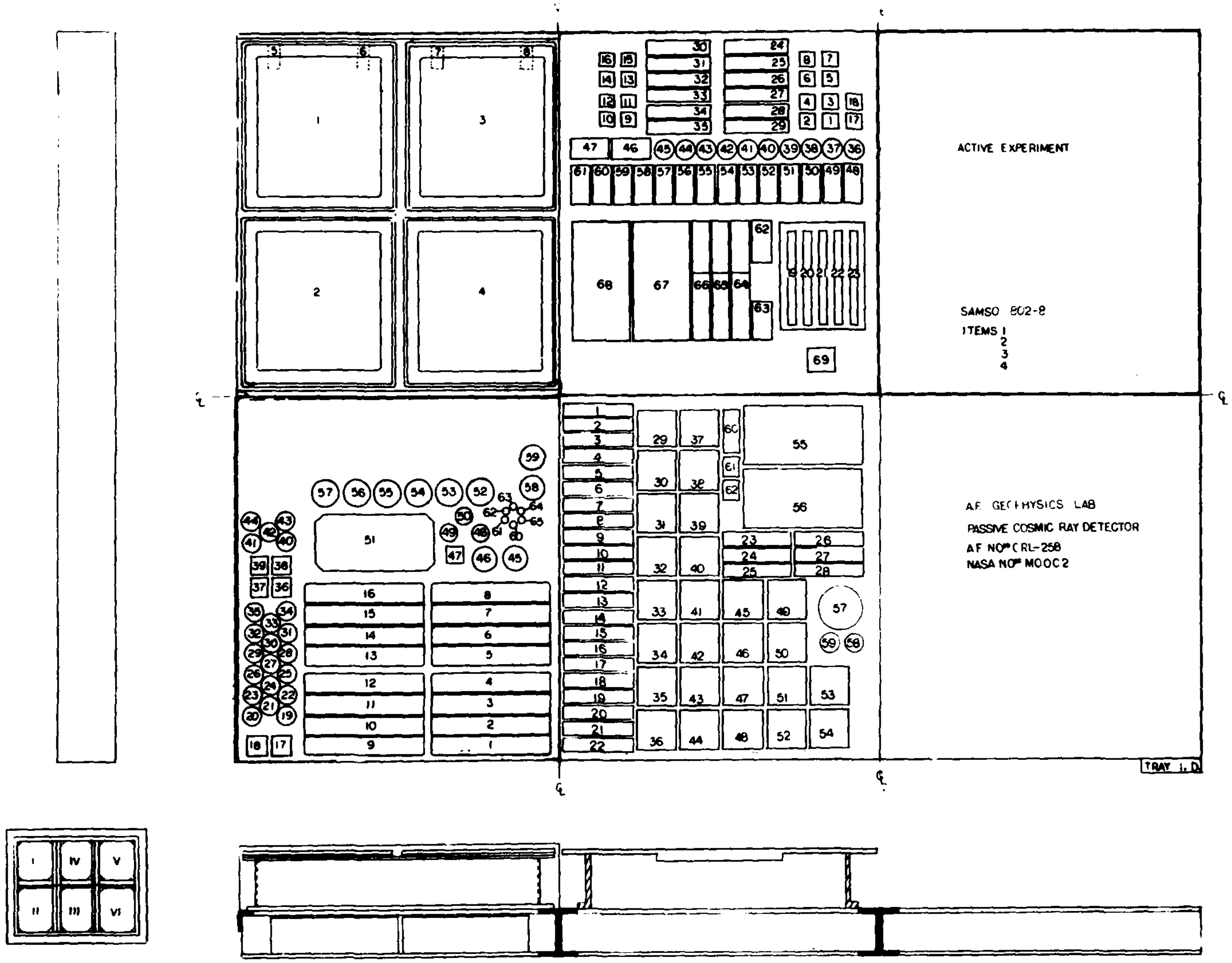
AFAPL = Air Force Aero-Propulsion Laboratory
NASA = National Aeronautics and Space Administration
A = Aerospace
AFFDL = Air Force Flight Dynamics Laboratory
AFAL = Air Force Avionics Laboratory
SD = Space Division
MDAC = McDonnell Douglas Astronautics Corp.
AFML = Air Force Materials Laboratory

3 in. Tray, Leading Edge



NOTES:

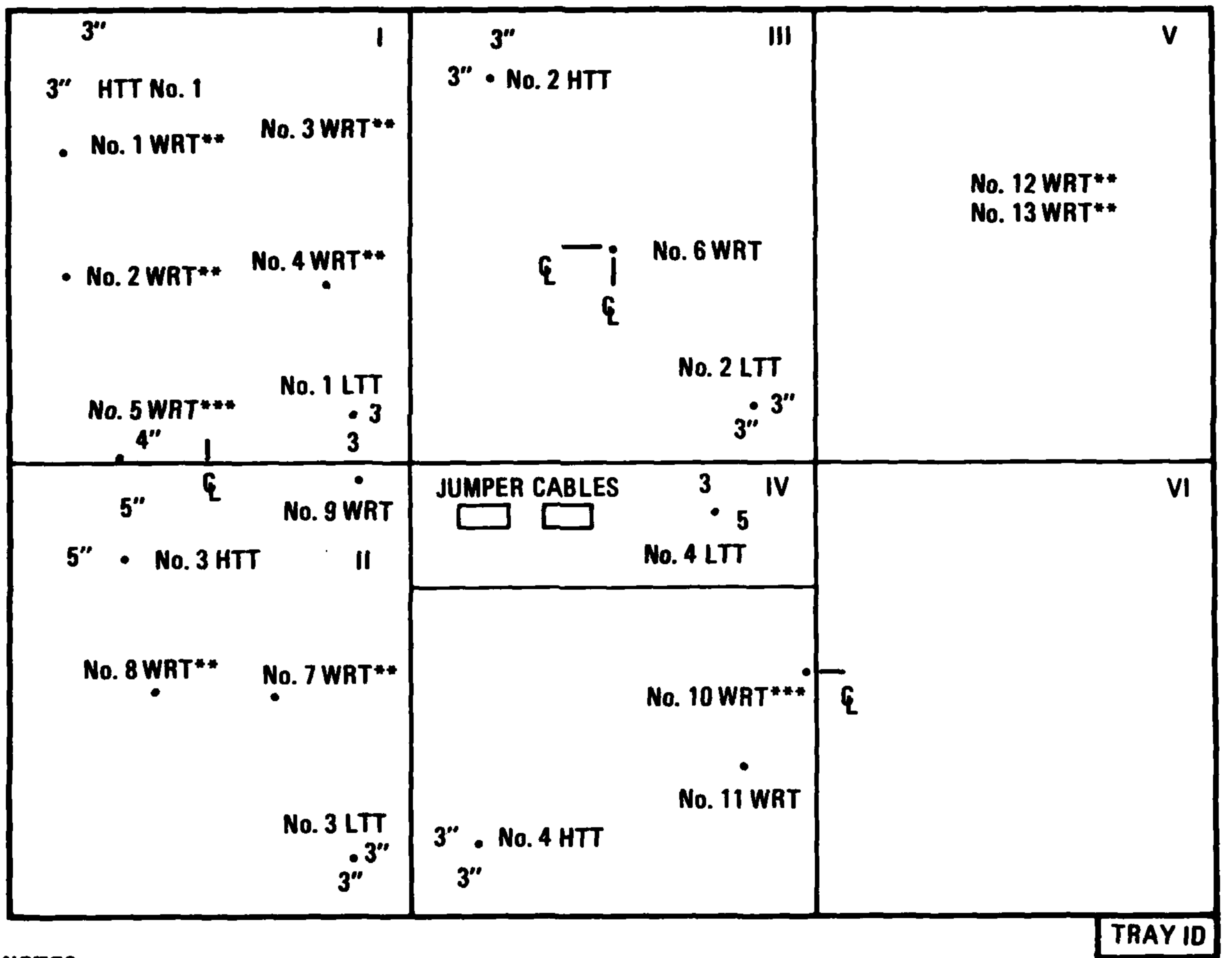
* Bottom surface of cover plate
** On sample
*** Mid-vertical surface of base
• All location not noted have thermistor bonded to the bottom surface of the sample plate



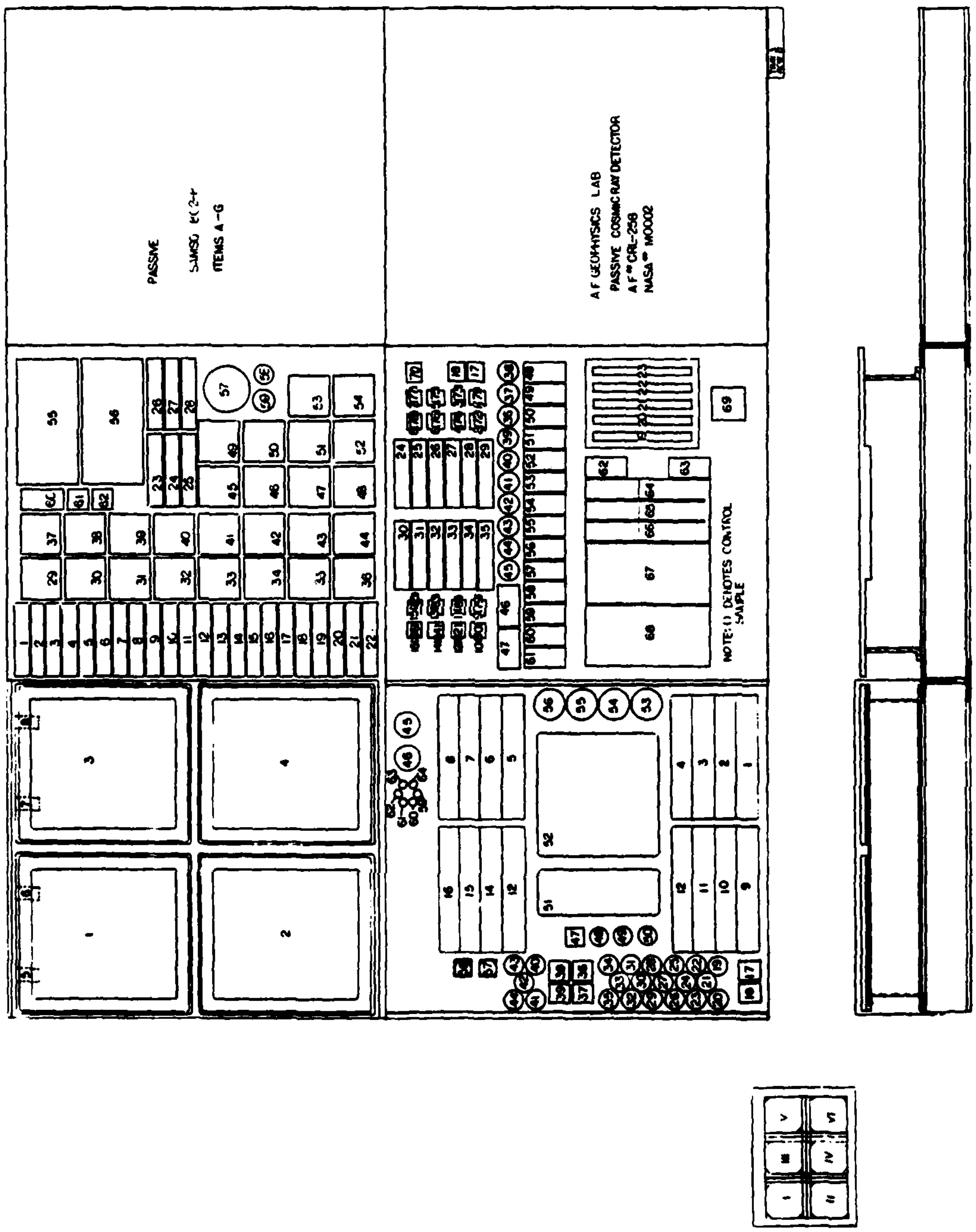
THREE INCH TRAY LEADING EDGE
SAMSO 8C2

LF 12 80

3 in. Tray, Trailing Edge

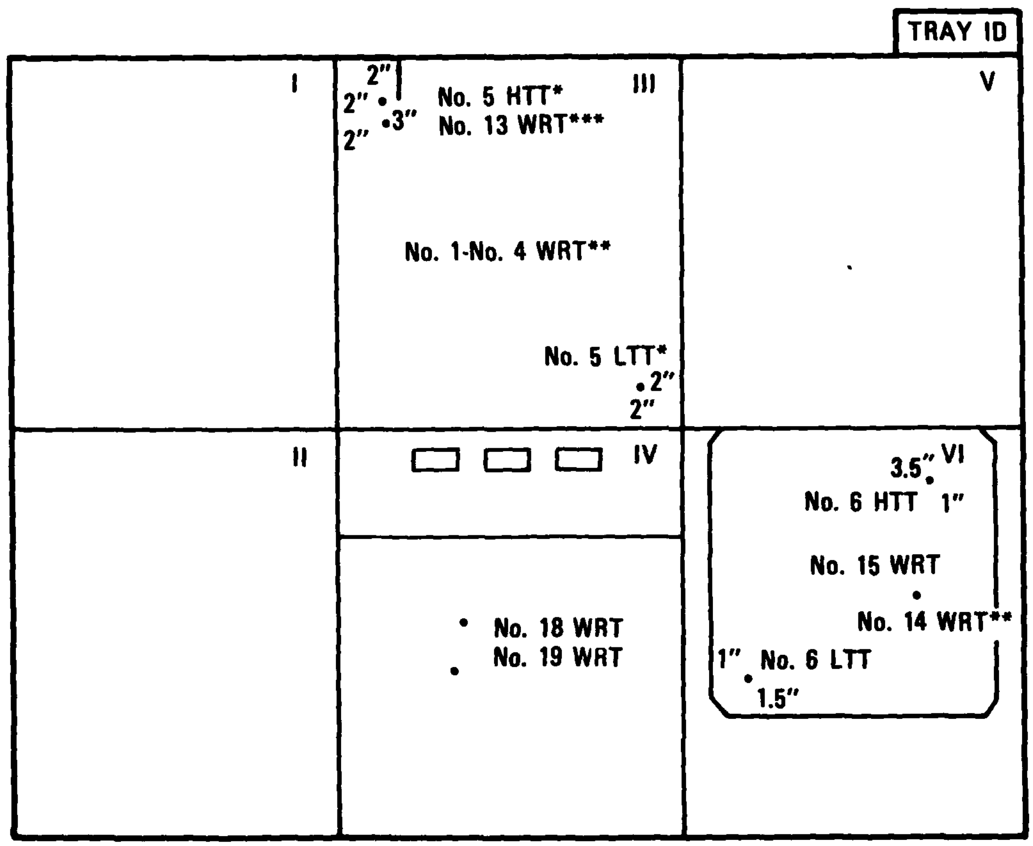


NOTES:
* Bottom surface of cover plate
** On sample
*** Mid-vertical surface of base
All locations not noted have thermistor bonded to the bottom surface of the sample plate



THREE INCH TRAY, TRAILING EDGE
SAMSO EC2

6 in. Tray, Leading Edge



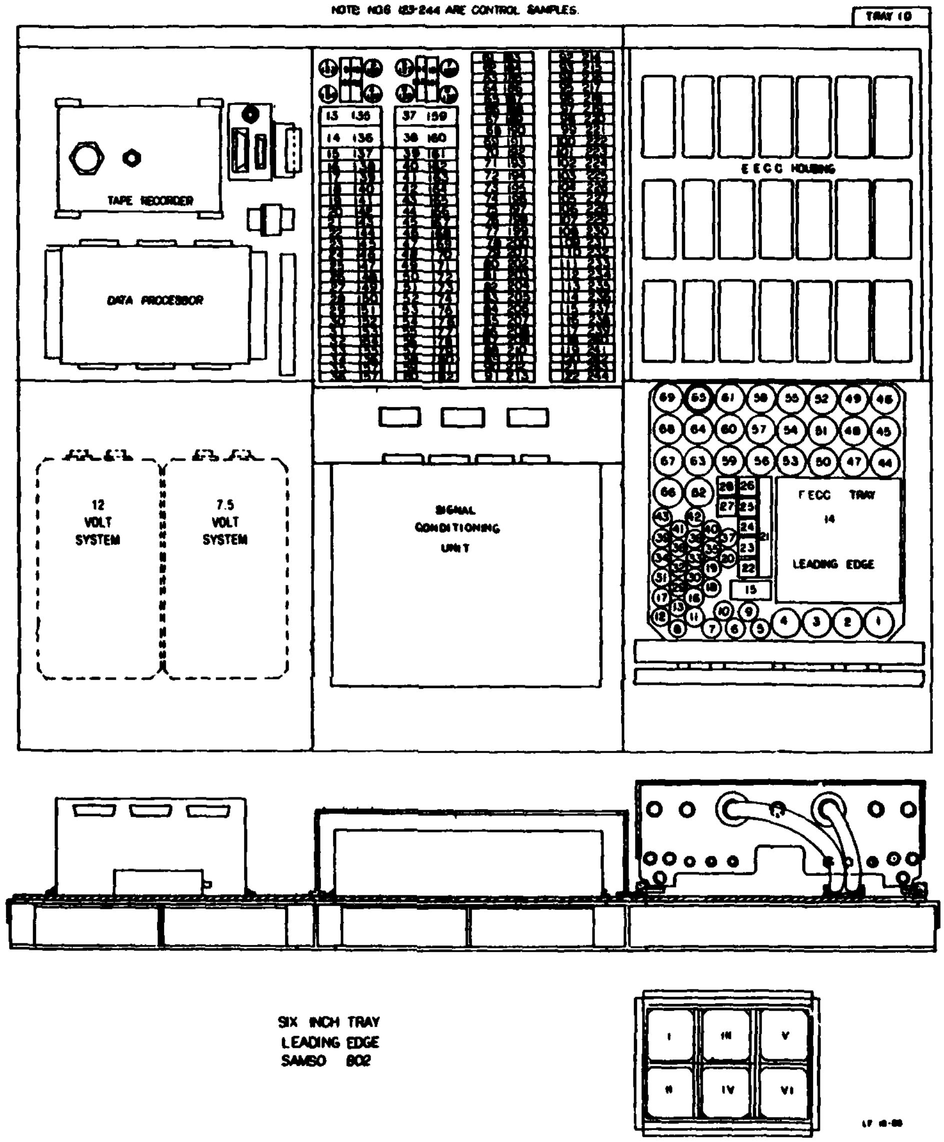
NOTES:

* Bottom surface of cover plate

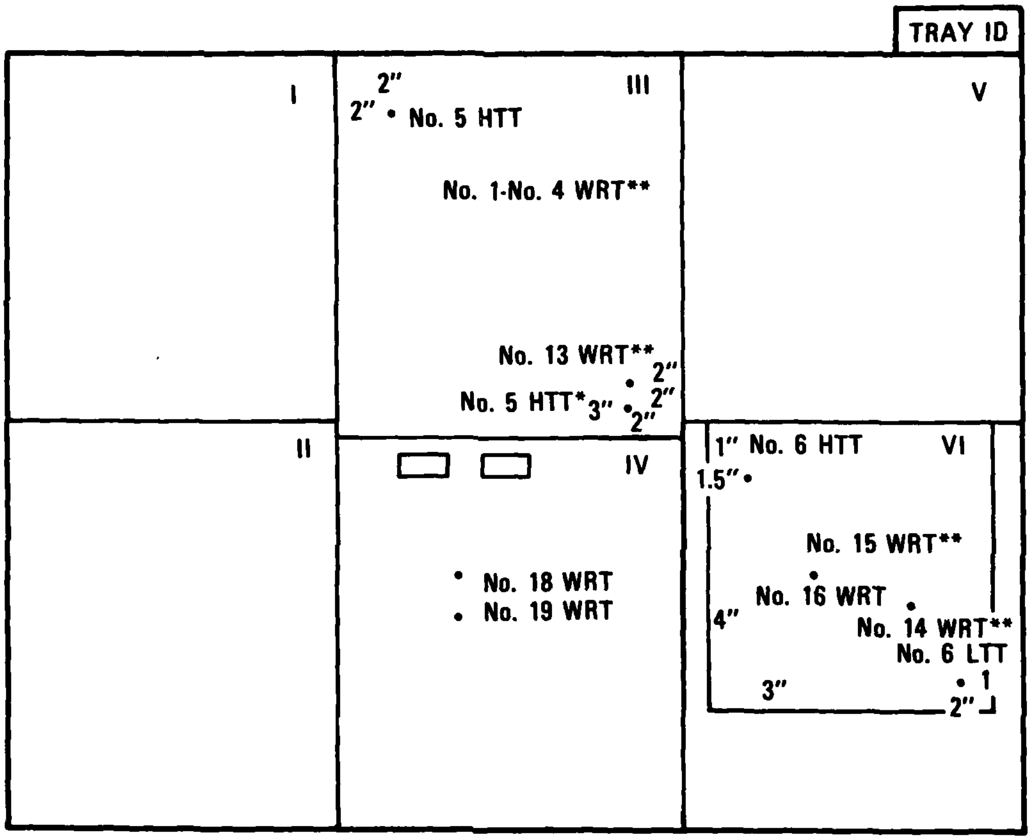
** On sample

*** Mid-vertical surface of base

• All locations not noted have thermistor bonded to the bottom surface of the sample plate


NOTE: NOS 183-244 ARE CONTROL SAMPLES.
TRAY 10
TAPE RECORDER
DATA PROCESSOR
EECC HOUSING
12 VOLT SYSTEM
7.5 VOLT SYSTEM
SIGNAL CONDITIONING UNIT
EECC TRAY 14 LEADING EDGE
SIX INCH TRAY
LEADING EDGE
SAMSO 802

6 in. Tray, Trailing Edge



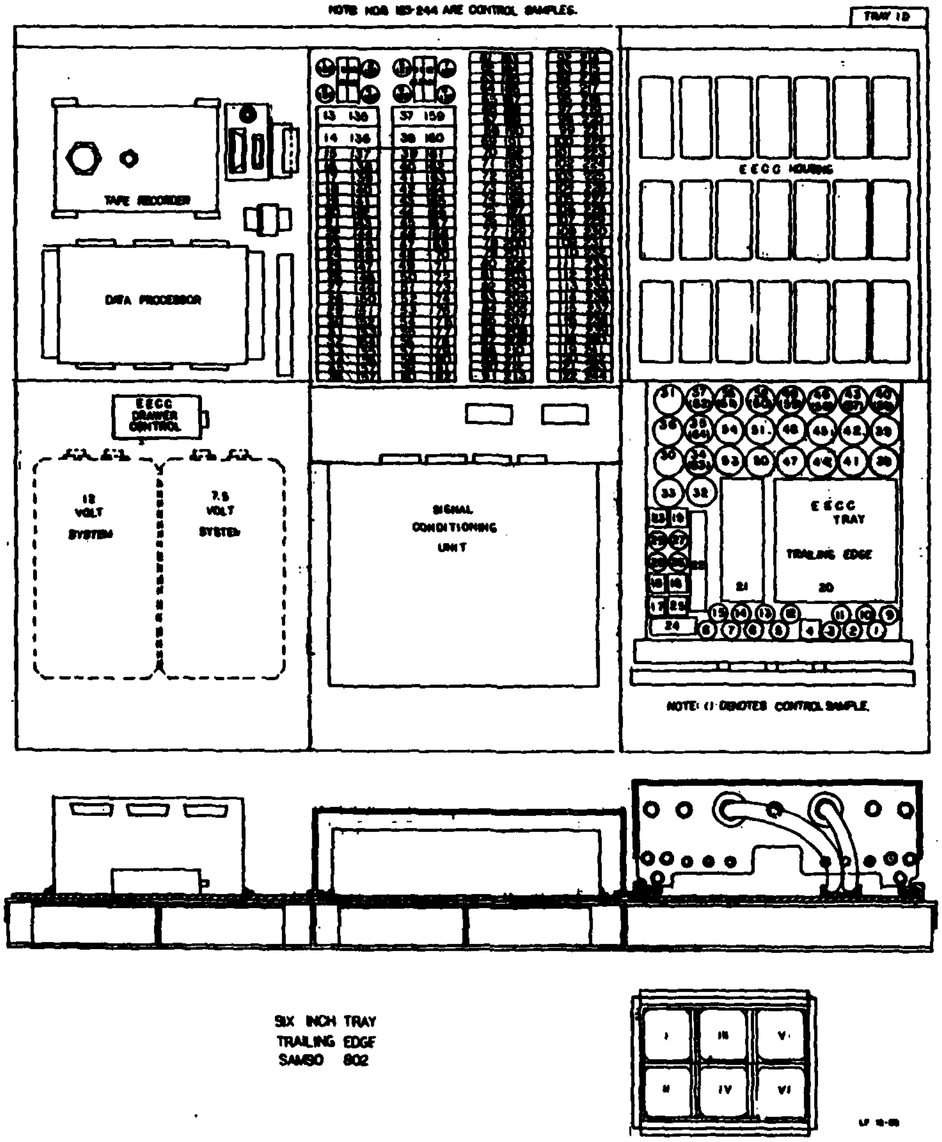
NOTES:

* Bottom surface of cover plate

** On sample

*** Mid-vertical surface of base

• All locations not noted have thermistor bonded to the bottom surface of the sample plate



SIX INCH TRAY
TRAILING EDGE
SAMSO 802

APPENDIX B

HARDWARE AND SOFTWARE FOR CHECKOUT OF LDEF DATA RECORDING SYSTEM

Prepared by

P. Schall and W. C. Burns
Materials Sciences Laboratory

The in-flight data collected for the LDEF Spacecraft Materials Experiment will be processed and stored in the EPDS, purchased from NASA. For these data to be retrieved, the tape record stored in EPDS must be transcribed onto a CCT by means of NASA-furnished GSE. Portable equipment for reading out the CCT record is needed to facilitate preflight checkout of the data recording system; therefore, a Radio Shack TRS-80 microcomputer was interfaced with the CCT recorder and a computer program was written to process the data. The hardware and software developed for this program are described herein.

INTRODUCTION AND BACKGROUND

The in-flight data collection system for the Spacecraft Materials Experiment to be flown in the Long Duration Exposure Facility, LDEF, is comprised of various data sensors (thermistors, strain gauges, etc.), a Signal Conditioning Unit, SCU, and an Experiment Power and Data System. Two such systems will be used; one on the leading edge and one on the trailing edge segments of the experiment.

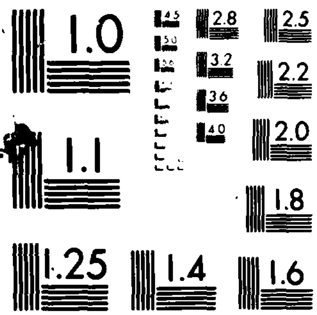
The EPDS has a capacity of processing and recording information from 20 digital and 64 analog data channels. The system can be user programmed to provide the desired timing for data collection and the binary word length to be used in the A to D conversion of the analog data. The selected word length is also applied to the formatting of the Synch code and time signal which procedes each scan of the data channels. The following description applies to the specific user programming of the EPDS units for this experiment. The Synch code, comprised of 24 bits of code, plus 6 filler bits is treated as three 10-bit words. The Synch code identifies the onset of a data scan, the specific experiment and the location of the data system (leading or trailing edge). This is followed by a 24-bit binary time code plus 6 filler bits formatted as three 10-bit words. The data follows in sequence as two 10-bit words corresponding to the 20 parallel digital data channels and 64 words of digitized analog data. Each scan therefore consists of 72 words. Data is collected in a burst of 5 consecutive scans totaling 3600 bits which are stored in a 4 K buffer memory. At the conclusion of a 5 scan burst the buffer memory is dumped to a Lockheed Mark V Type 4200 single-track tape recorder. A total of 32 buffer dumps, equally spaced in time over a total time slightly longer than one orbital period, and are recorded at approximately 4 day intervals during the flight. The flight recorder track consists of blocks of 3600 bits of real information interspersed with noise bits recorded when the tape comes up to speed before each buffer dump and filler bits corresponding to the buffer memory capacity less 3600.

Information is retrieved from the EPDS recorder by transcribing, using Ground Support Equipment, GSE, to a Kennedy Model 9800 Computer

AD-A113 504 AEROSPACE CORP EL SEGUNDO CA LAB OPERATIONS F/G 9/3
SD/LDEF TECHNICAL USER'S MANUAL.(U)
SEP 81 R P GIGUERE F04701-80-C-0081
UNCLASSIFIED TR-0081(6950-05)-2 SD-TR-81-86 NL

2 of 2

END
DATE
FILMED
5 82
DTIC


1.0
2.8
2.5
3.2
2.2
3.6
4.0
2.0
1.1
1.8
1.25
1.4
1.6

Compatible Tape (CCT) recorder. The CCT stores the information as 8-bit characters that bear no fixed phase relationship to the original 10-bit data words. The CCT record must be searched for the Synch code and the time and data words must be reconstructed and converted to useful form. The actual flight tapes will be processed on a large computer to analyze and massage the data and present results in appropriate formats. However, during the preflight phase of the experiment there is a need for portable hardware that can be used to check out system performance at Aerospace during assembly, at LaRC before and after flight acceptance tests, and at KSC during prelaunch testing. This report describes the hardware and software assembled to fill this requirement.

HARDWARE DESCRIPTION

A TRS-80 Model I, Level II microcomputer was interfaced with the CCT recorder via a S100 bus. The interface wiring diagram is shown in Figure 1. Communication between the TRS-80 and the CCT requires only a rather straight forward handshake procedure. The read data available, RDA, line from the CCT, when in the true state, indicates that data is available in the CCT buffer memory. The state of RDA is ascertained by latching the state into the S100 bus by a software pulse from the TRS-80 out of Port 2 and examining the input from Port 1 (RDA true = Port 1 level of 253). A CCT character is made available for extraction by sending a readout one character, ROOC, pulse to the CCT. The character may be latched at the S100 bus using either a software strobe or the read data strobe, RDS, pulse generated by the CCT following receipt of an ROOC pulse. The circuit shown in Figure 1 has provisions for both methods of strobing but the RDS is actually used for normal operation. However, the software strobe line is used at the start of the readout to initialize the line in a high state since the RDS is a downward going pulse. The CCT 8-bit characters are latched at Port 0 of the S100 from which they are retrieved by the TRS-80 for processing.

Initial attempts at operating the system resulted in loss of either the first or last character from each CCT buffer (512-character) load depending on the specific handshake sequence used. After expenditure of considerable effort the source of the problem was finally identified, with the assistance of Kennedy Service Personnel. The ROOC pulse, as produced by the TRS-80, was about 3 msec long. During a change of CCT buffer loads the RDA changes

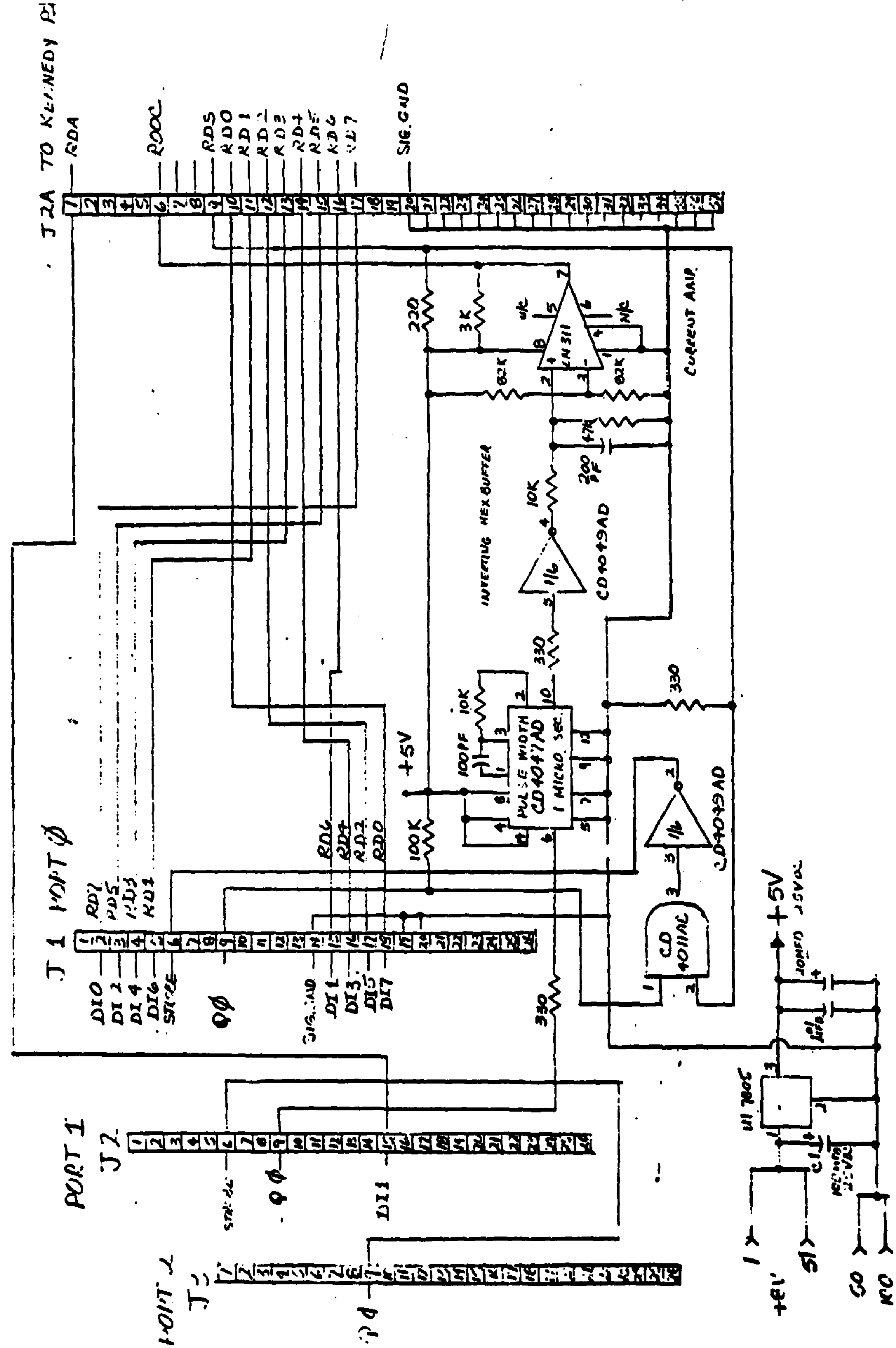

J2A
J 1
PORT Ø
PORT 1
J 2
+5V
SIG. GND
CURRENT AMP
INVERTING HEX BUFFER
CD4049AD
PULSE WIDTH
CD4047AD
1 MICRO. SEC.
LM 311
100K
220
3K
330
10K
100PF
200 PF

FIGURE 1

from true to false and back to true. Due to peculiarities of the CCT circuit, if RDA pulse occurs during an ROOC pulse the buffer pointer is indexed one extra position resulitng in loss of a character. The problem was solved by shortening the ROOC pulse with an monostable multivibrator circuit installed in the line between the S100 bus and the CCT. This reduced the ROOC pulse length to ~ 1 μ sec and prevented overlap with the RDA pulse. Other components in the ROOC line, shown in Figure 1, increase the available current drain on the line. Without these components the available current was marginal in meeting the CCT operation requirements.

SOFTWARE DESCRIPTION

Computer programs to read the CCT tape were written in Radio Shack Level II basic. The initial program contained many diagnostic features to aid in debugging and inspection of intermediate results. This program was called "LDEF Conversion", LC. Later a faster running version called "LDEF Tape Read", LTR, was written to take advantage of the fact the EPDS buffer filler bits were generally all "1" and the noise bits recorded during EPDS tape startup were generally all"O". Since this garbage comprised about one-half of the information on the tape processing time could be reduced by about 50% by not searching through it for the Synch code. Instead the garbage was rejected quickly on the basis of its own characteristics. Also the diagnostic features contained in LC were deleted in LTR.

In the following paragraphs the final program, LTR, will be described first. Then the additional features available in LC will be discussed.

General Approach

The LTR program sequentially searches for the Synch code, locates the time code and converts to days, hours, minutes and seconds, reconstructs the 10-bit data words and converts these words, which are data [illegible]tization numbers to appropriate data values for each data channel. The [illegible] is repeated until all data blocks on the CCT are processed or until terminated manually. In the present version quantitization numbers for analog data channels are converted to the original signal voltages. Conversion to the basic data such as temperature, strain, etc. could be provided by addition of appropriate subroutines if desired. However the present format is considered adequate for preflight experiment checkout. The additional capabilities for massaging the data will be incorporated into programs for analysis of the actual flight data.

The LTR program functions by constructing a string variable from the CCT 8-bit characters. This string is maintained at a minimum length of 40-bits during Synch code search and processing of the time code, and a minimum of 11-bits during processing of data words. This is implemented by discarding bits from the left end that have been processed and adding CCT characters to the right end. The initial string is constructed of the first 5 characters of the CCT record. This string is searched to determine whether it contains the Synch code. If not the string is regenerated by calling additional CCT characters and re-examined until the Synch code is found. At this point the Synch code and trailing 6 filler bits are discarded and the time code is identified and converted. Then the data channels are processed and search for the next Synch code is resumed.

Computer output to both a line printer and CRT is provided and connection to both are required for the program to run. The hard copy format is (1) time at which data set was recorded and cumulative number of 8-bit bytes retrieved from the CCT at that time and (2) tabulation of data channel numbers and corresponding data values. Data channel numbers are 7 through 72 inclusive; numbers 1 through 6 having been assigned to the 6 words containing the Synch and time codes. The cumulative count printed after each time output serves as a benchmark to check that no CCT bytes have been missed in each sequence of 5 data scans. The byte count should increment by 90 (90 x 8 = 720 bits = 72 ten bit words) between consecutive data scans in the sequence. In addition, "BUFFER CHANGE TOTAL BYTES = XXX" is printed at each point at which the software byte counter indicates that a CCT buffer reload should have occurred. Visual confirmation that this printout coincides with an actual buffer reload (tape movement) provides additional evidence that all bytes have indeed been retrieved. As mentioned earlier, the program can be run in a time only mode, in which case the data channel signal values are not processed or printed out.

Outputs to the CRT are as follows: Prompts for location (leading or trailing edge) and time only mode are displayed. Once the program is running and in the Synch code search mode the current string variable being examined and the cumulative total bytes retrieved from the CCT are displayed. This serves no useful purpose other than a visual indication that the program is running. At each point that a Synch code is located "FOUND" will be displayed and START point = XX and END point = YY, indicating the location of the Synch code within the current string. This will be followed shortly by printer output of time and data. Thus a combination of CRT and printer activity provide indication of the operation currently being performed by the computer.

In the event that the RDA is false at the time of interogation the message "RDA FALSE INP (1) = XXX" will be displayed on the CRT and the program will stop running. The probability of this occurrence is remote and would most likely indicate an electronic malfunction. Although it has never occurred as of this writing, RDA could conceivably have been momentarily false at the time of interogation and shortly returned to the true state, due to a temporary delay in reloading of the CCT buffer. To check for this possibility enter, from the keyboard, "OUT 2,0: OUT 2,1: PRINT INP (1)". If the response is 253 RDA has returned to the "TRUE" state and the program can be resumed by entering "CONT".

Detailed Program Description

A listing of the string and numeric variables used, in the order of their first appearance in the program is given in Table 1. The program listing is given in Table 2.

Program steps 10 through 100 initialize the operation by prompting for the location (leading or trailing edge) of the EPDS and mode of operation (time only or full output) and selecting the appropriate Synch code (SC) and conversion constants (H1, H2, L1 and L2) for converting quantitization numbers to analog signal voltages. This is followed by initializing the counters to count the location of the current CCT byte in the buffer (CC) and the total byte count (TB), setting the two strobe lines high (Step 92) and identifying the characteristics of the filler bits in the EPDS buffer memory (CK$) and finally, setting up the initial 40-bit string variable S$ from the first 5 bytes of the CCT buffer.

Steps 110-114 maintain a minimum string variable length of 40 bits during Synch code search and display the current string being searched on the CRT. Step 120 determines whether the current string is composed of noise or buffer filler bits and, if so, bypasses the search for the Synch code. Steps 125 to 160 implement the search for the Synch code in the current string and generate a new string if the Synch code is not found. Steps 170-192 output to the CRT that the Synch code has been found, discard the Synch code from the current string and generate a new string of appropri-

TABLE 1. STRING AND NUMERIC VARIABLES

L$ =	Location of EPDS.
T$ =	Designator for Time only mode.
SC$ =	Synch Code.
H1, H2 =	Conversion constants for high level analog channels.
L1, L2 =	Conversion constants for low level analog channels.
CC =	CCT buffer byte count.
TB =	Total byte counts.
CK$ -	String characteristics of 3 CCT filler bytes.
S$ -	Dynamic string for Synch code search and extraction of time and data.
NB =	Number of bytes to be retrieved from CCT during next branch to subroutine 1400.
Y$ =	Left 24 bits of S$, used to test for presence of noise or filler bits.
I% =	Loop counter.
SP%, EP% =	Starting and ending location of Synch Code in S$.
T$ =	24 bit time code.
CH$ =	10 bit data string.
V =	Decimal data channel word.
J% =	Loop counter.
TI#, C#, X#, Z#, Y# =	Double precision variables used to convert 24 bit time code to real time.
D, H, M, S =	Days, hours, min, sec of real time.
QN =	Decimal number corresponding to 8-bit CCT byte.
G% =	Loop counter.
X, X$, A$ =	Used in regenerating S$

TABLE 2. LDEF TAPE READ

-PROGRAM LISTING-

```
10 CLEAR 800:CLS
20 PRINT TAB(20)"LDEF TAPE READ":PRINT TAB(15)"WITH CCT AND LINE PRINTER ONLY":P
RINT
30 INPUT"LEADING OR TRAILING EDGE (L OR T)";L$
40 INPUT"IF YOU WANT TO PRINT TIME ONLY ENTER YES";TP$
55 SC$="111110101111001100100000"
60 IF L$="T" THEN SC$="000001010000110011011111"
65 IF L$="L" THEN H1=4.988:H2=2.44E-3:L1=10.188:L2=4.993E-3:ELSE H1=4.991:H2=2.4
35E-3:L1=10.136:L2=4.962E-3
70 CC=1:TB=0
75 LPRINT"LDEF TAPE READ"
80 LPRINT"":IF L$="L" THEN LPRINT"LEADING EDGE" ELSE LPRINT"TRAILING EDGE"
90 IF TP$="YES" THEN LPRINT"TIME READOUT ONLY"
92 OUT 0,1:OUT 2,1
95 CX$="111111111111111111111111"
100 S$="":NB=5:GOSUB 1400
110 N=LEN(S$):IF N>=40 THEN 120
111 R=(40-N)/8:NB=INT(R):R=R-NB:IF R>0 THEN NB=NB+1
114 GOSUB 1400:PRINTS$,TB
120 Y$=LEFT$(S$,24):IF VAL(Y$)=0 OR Y$=CX$ THEN NB=2:GOTO 155
125 FOR I%=1 TO LEN(S$)
130 IF SC$=MID$(S$,I%,24) THEN 170
140 NEXT:I%=0
150 IF I%=0 THEN NB=2
155 GOSUB 1400
160 R%=LEN(S$)-16:S$=RIGHT$(S$,R%):PRINTS$,TB:GOTO 120
170 SP%=I%:EP%=I%+23:PRINT"FOUND","START POINT=";SP%,"END POINT=";EP%
180 N%=LEN(S$)-EP%:S$=RIGHT$(S$,N%):NB=INT((40-N%)/8):GOSUB 1400
190 N%=LEN(S$)-6:S$=RIGHT$(S$,N%)
192 IF LEN(S$)<40 THEN NB=1:GOSUB 1400
210 T$=LEFT$(S$,24):GOSUB 800
230 N%=LEN(S$)-30:S$=RIGHT$(S$,N%):NB=5:GOSUB 1400
250 FOR I%=7 TO 72
260 IF LEN(S$)<=10 THEN NB=5:GOSUB 1400
270 CH$=LEFT$(S$,10):S$=RIGHT$(S$,LEN(S$)-10)
280 IF I%<>8 THEN 320 ELSE GOSUB 1500
300 V=(4*V)+1:LPRINT"CHANNEL-8=";V
310 NEXT
320 IF I%<>7 THEN 360
350 LPRINT"CHANNEL-7=";CH$:NEXT
360 GOSUB 1500
```

```
380 IF I%>15 THEN 400
390 V=(4*L2*V)-L1:GOTO410
400 V=(4*H2*V)-H1
410 LPRINT"CHANNEL-";I%;"=";V
420 NEXT:GOTO 110
800 C#=0
805 FOR J%=1 TO 24
820 TI$=RIGHT$(T$,1)
830 TI#=VAL(TI$):K%=J%-1
840 M=TI#*(2^K%):C#=C#+M
850 T$=LEFT$(T$,24-J%):NEXT
860 X#=.61*24*3600
870 D=INT(C#/X#)
880 Z#=(C#/X#-D)*24:H=INT(Z#)
890 Y#=(Z#-H)*60:M=INT(Y#)
900 Z#=(Y#-M)*60:S=INT(Z#)
930 LPRINT D;"DAYS,";H;"HRS,";M;"MIN,";S;"SEC":LPRINT TAB(8)"TOTAL BYTES=";TB
950 IF TP$="YES" THEN 1000 ELSE RETURN
1000 NB=78:GOSUB 1400:GOTO 110
1400 FOR J%=1 TO NB
1410 OUT 2,0:OUT 2,1:IF INP(1)<>253 THEN PRINT"RDA FALSE","INP(1)=";INP(1):STOP
1420 OUT 1,0:OUT 1,1
1425 OUT 2,0:OUT 2,1:IF INP(1)<>253 THEN PRINT"RDA FALSE","INP(1)=";INP(1):STOP
1430 TB=TB+1
1440 IF TP$="YES" AND NB=78 THEN 1450 ELSE GOSUB 1600
1450 IF CC=512 THEN 1480
1460 CC=CC+1:NEXT:RETURN
1480 LPRINT TAB(4)"BUFFER CHANGE","TOTAL BYTES=";TB
1490 CC=1:NEXT:RETURN
1500 V=0
1510 FOR J%=1 TO 10
1520 DE$=RIGHT$(CH$,1):DE=VAL(DE$)
1530 K%=J%-1:V=V+(DE*(2^K%))
1540 CH$=LEFT$(CH$,10-J%):NEXT:RETURN
1600 QN=INP(0):QN=255-QN:A$=""
1620 FOR G%=1 TO 8
1630 X=((QN/2)-INT(QN/2))*2:X$=STR$(X)
1640 X$=RIGHT$(X$,1):A$=X$+A$:QN=INT(QN/2):NEXT
1660 S$=S$+A$:RETURN
```

ate length. Steps 210 and 230 extract the time code and generate the appropriate string for the start of retrieval of data words. Steps 250-420 extract the 10-bit data quantitization numbers and convert to signal values for channels 7 through 72.

The following subroutines support the program steps described above. Subroutine 800 (Steps 800-1000) converts the time code to real time and outputs to the printer. When operating the program in the time only made this subroutine controls the rapid retrieval and discard of the data words.

Subroutine 1400 (steps 1400-1490) provides the handshake with the CCT, maintains the buffer byte and total byte count and latches bytes at the S100 bus. Since the TRS-80 internally converts the binary bytes to decimal numbers these must be reconverted to the binary form for the string operations used in the main program. Except when data bytes are to be discarded (time only mode) subroutine 1400 calls upon subroutine 1600 (steps 1600-1660) for the decimal to binary conversion and addition of the binary byte to the right end of the working string, S$. It should be noted that the CCT record is the complement of the EPDS record, hence the second operation in step 1600 to generate the correct byte format.

Subroutine 1500 performs the binary to-decimal conversion for the 10-bit data words, (quantitization numbers) which are returned to the main program as the variable V. The V values are converted to the original analog signals (voltages) for the low level channels (9 through 15) in step 390 and for the high level channels (16 through 72) in step 400. Channel 7 is a 10-bit binary word and does not require binary to decimal conversion (step 350). Channel 8 is a special case. This channel is the data from the QCM monitor. The experimenter provided his own A to D converter that produces 12 bit words. Since the EPDS were hard wired for 10-bit words, only the 10 highest order bits of the QCM data are recorded. The decimal value of the 12-bit word is estimated by assuming that the two lowest order bits were 01. This is performed by the first operation in Step 300. Inability to record the entire 12-bits results in an uncertainty of +1, -2 Hz in the QCM frequency data. This is the equivalent of less than a monolayer of contaminant.

LC Program Description

The additional features of the LC program include: (a) provisions for internal generation of simulated CCT bytes to permit program checkout without the presence of a CCT, (b) Option of operating without a line printer, in which case all outputs are displayed on the CRT and (c) provides a listing and description of key variables and subroutines on request. The program contains prompting for inputs to identify the options selected.

When operated in the internal data generation mode the program provides a program check option which, if selected, provides intermediate results that can be used to diagnose the source of any problem in running the program. The internally generated data consists of the equivalent of one data scan including Synch and time codes. It has provisions for inserting any number of leading bits, up to 190, ahead of the Synch code.

The LC program listing is shown in Table 3.

TABLE 3. LDEF CONVERSION

-PROGRAM LISTING-

```
10 CLEAR 800:CLS
20 PRINT TAB(20)"LDEF CONVERSION":PRINT""
22 INPUT"DO YOU WANT TO SEE DESCRIPTION OF KEY VARIABLES, STRINGS AND SUBROUTINE
S,IF SO ENTER YES";Q$
24 IF Q$="YES" THEN CLS:GOSUB 2000
30 INPUT"LeADING OR TRAILING EDGE (L OR T)";L$
40 INPUT"DATA INPUT IS (CCT OR IN)";DI$
45 IF DI$="IN" THEN INPUT"PROGRAM CHECK, IF SO ENTER YES";PC$
50 INPUT"LINE PRINTER (ON OR OFF)";P$
52 INPUT"IF YOU WANT TO PRINT TIME ONLY ENTER YES";TP$
55 SC$="111110101111001100100000"
60 IF L$="T" THEN SC$="000001010000110011011111"
65 IF DI$="CCT" THEN OUT 0,1:OUT 2,1:CC=1:TB=0
70 IF DI$="IN" THEN INPUT"NUMBER OF LEADING BITS (<190)";LB
80 B$=STRING$(LB,"0"):T$=STRING$(24,"1"):C$=STRING$(6,"0")
90 B$=B$+SC$+C$+T$+C$
100 C$=STRING$(9,"1"):E$="0":C$=C$+E$:S$=""
110 N=LEN(S$):IF N>=40 THEN 120
111 R=(40-N)/8:NB=INT(R):R=R-NB
112 IF R>0 THEN NB=NB+1
113 GOSUB 1300
114 PRINT S$
115 IF PC$="YES" THEN PRINT "STRING ` 90=";S$
120 FOR I=1 TO LEN(S$)
130 IF SC$=MID$(S$,I,24) THEN 170
140 NEXT:I=0
150 IF I=0 THEN NB=2:GOSUB 1300
155 R=LEN(S$)-16
160 S$=RIGHT$(S$,R):PRINTS$,TB:GOTO 120
170 SP=I:EP=I+23:PRINT"FOUND","START POINT=";SP,"END POINT=";EP
180 N=LEN(S$)-EP:S$=RIGHT$(S$,N):NB=INT((40-N)/8):GOSUB 1300
190 N=LEN(S$)-6:S$=RIGHT$(S$,N)
192 IF LEN(S$)<40 THEN NB=1:GOSUB 1300
195 IF PC$="YES" THEN PRINT"STRING ` 190=";S$
200 PRINT"LENGTH OF STRING @ 190=";LEN(S$)
210 T$=LEFT$(S$,24)
212 PRINT"T$=";T$
215 IF PC$="YES" THEN PRINT"TIME COUNT=";T$;"——SHOULD READ 24 ONES":GOTO 220:EL
SE 225
220 PRINT"IF OK, ENTER CONT":STOP
```

```
225 GOSUB 800
230 N=LEN(S$)-30:S$=RIGHT$(S$,N):NB=5:GOSUB 1300
240 N=LEN(S$):PRINT"LENGTH OF STRING @ 240=";N
250 FOR I=7 TO 72
260 IF LEN(S$)<=10 THEN NB=5:GOSUB 1300
270 CH$=LEFT$(S$,10):S$=RIGHT$(S$,LEN(S$)-10)
275 IF PC$="YES" THEN PRINT "CHANNEL-";I;"STRING=";CH$:PRINT" SHOULD READ 111111
1110"
280 IF I<>8 THEN 320
290 GOSUB 1500
300 V=(4*V)+1:GOSUB 500
310 NEXT
320 IF I<>7 THEN 360
330 IF P$="ON" THEN 350
340 PRINT"CHANNEL-7=";CH$:NEXT
350 LPRINT"CHANNEL-7=";CH$:NEXT
360 GOSUB 1500
370 IF L$="L" THEN H1=4.988:H2=2.44E-3:L1=10.188:L2=4.993E-3:ELSE H1=4.981:H2=2
435E-3:L1=10.136:L2=4.962E-3
380 IF I>15 THEN 400
390 V=(4*L2*V)-L1:GOTO410
400 V=(4*H2*V)-H1
410 GOSUB 500
420 NEXT
430 IF D1$="CCT" THEN 110
440 PRINT"":PRINT"END OF INTERNAL DATA CONVERSION":END
500 IF P$="ON" THEN 520
510 PRINT"CHANNEL-";I;"=";V:RETURN
520 LPRINT"CHANNEL-";I;"=";V:RETURN
800 C#=0
805 FOR J=1 TO 24
820 TI$=RIGHT$(T$,1)
830 TI#=VAL(TI$):K=J-1
840 M=TI#*(2^K):C#=C#+M
850 T$=LEFT$(T$,24-J):NEXT
860 X#=.61*24*3600
870 D=INT(C#/X#)
880 Z#=(C#/X#-D)*24:H=INT(Z#)
890 Y#=(Z#-H)*60:M=INT(Y#)
900 Z#=(Y#-M)*60:S=INT(Z#)
910 IF P$="ON" THEN 930
920 PRINT"TIME=";D;"DAYS,";H;"HRS,";M;"MIN,";S;"SEC":GOTO 940
930 LPRINT D;"DAYS,";H;"HRS,";M;"MIN,";S;"SEC":LPRINT TAB(8)"TOTAL BYTES=";TB:GO
TO 945
```

```
940 IF PC$="YES" THEN PRINT"TIME SHOULD BE 318 DAYS, 7 HRS, 53 MIN, 57 SEC
945 IF TP$="YES" THEN 1000
950 RETURN
1000 FOR W=1 TO 7S
1010 GOSUB 1600
1020 NEXT
1030 GOTO 110
1300 IF DI$="CCT" THEN 1400
1310 FOR J=1 TO NB
1320 IF LEN(B$)<=40 THEN B$=B$+C$
1330 A$=LEFT$(B$,8):B$=RIGHT$(B$,LEN(B$)-8)
1340 S$=S$+A$:NEXT:RETURN
1400 FOR J=1 TO NB
1410 GOSUB 1600
1420 S$=S$+A$:NEXT: RETURN
1500 V=0
1510 FOR J=1 TO 10
1520 DE$=RIGHT$(CH$,1):DE=VAL(DE$)
1530 K=J-1:V=V+(DE*(2[K))
1540 CH$=LEFT$(CH$,10-J):NEXT:RETURN
1600 OUT 2,0:OUT 2,1:IF INP(1)<>253 THEN PRINT"RDA FALSE","INP(1)=";INP(1):STOP
1602 OUT 1,0:OUT 1,1
1604 OUT 2,0:OUT 2,1:IF INP(1)<>253 THEN PRINT"RDA FALSE","INP(1)=";INP(1):STOP
1606 QN=INP(0):QN=255-QN:TB=TB+1
1610 A$=""
1620 FOR G=1 TO 8
1630 X=((QN/2)-INT(QN/2))*2:X$=STR$(X)
1640 X$=RIGHT$(X$,1):A$=X$+A$
1650 QN=INT(QN/2)
1660 NEXT
1670 IF CC=512 THEN 1705
1680 CC=CC+1:RETURN
1705 LPRINT TAB(4) "BUFFER CHANGE";"  TOTAL BYTES=";TB
1710 CC=1:RETURN
2000 PRINT TAB(20)"STRINGS AND VARIABLES":PRINT""
2010 PRINT"L$=LOCATION ON LDEF, LEADING OR TRAILING EDGE"
2020 PRINT"DI$=DATA INPUT MODE, CCT OR INTERNAL"
2030 PRINT"P$=LINE PRINTER ON OR OFF"
2040 PRINT"LB=NUMBER OF LEADING BITS AHEAD OF SYNC CODE"
2045 PRINT"NB=NUMBER OF CCT BYTES TO BE INPUT"
2050 PRINT"SC$=SYNC CODE"
2060 PRINT"B$=INTERNALLY GENERATED STRING  SIMULATES  BYTES FROM CCT"
```

```
2070 PRINT"A$=INDIVIDUAL BYTES FROM B$ OR CCT"
2080 PRINT"S$=ACTIVE STRING FOR SYNC CODE, TIME AND DATA"
2090 PRINT"N=LENGTH OF ACTIVE STRING":PRINT"TO SEE THE REST ENTER CONT":STOP
2100 CLS:PRINT"T$=BINARY TIME COUNT"
2110 PRINT"CH$=BINARY CODE NUMBER FROM DATA CHANNEL"
2120 PRINT"V=DECIMAL CODE &/ANALOG SIGNAL"
2130 PRINT"":PRINT TAB(25)"SUBROUTINES"
2140 PRINT"500-CRT OR LINE PRINTER COMMANDS"
2150 PRINT"800-CONVERTS TIME COUNT TO DAYS,HRS,MIN,SEC"
2160 PRINT"1300-INPUTS BYTES FROM CCT OR INTERNAL SIMULATOR"
2170 PRINT"1500-CONVERTS 10-BIT BINARY TO DECIMAL"
2180 PRINT"1600-CONVERTS CCT BYTE BACK TO BINARY"
2190 PRINT"":PRINT"TO RESUME PROGRAM-ENTER CONT":STOP:CLS:RETURN
```

LABORATORY OPERATIONS

The Laboratory Operations of The Aerospace Corporation is conducting experimental and theoretical investigations necessary for the evaluation and application of scientific advances to new military concepts and systems. Versatility and flexibility have been developed to a high degree by the laboratory personnel in dealing with the many problems encountered in the nation's rapidly developing space and missile systems. Expertise in the latest scientific developments is vital to the accomplishment of tasks related to these problems. The laboratories that contribute to this research are:

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