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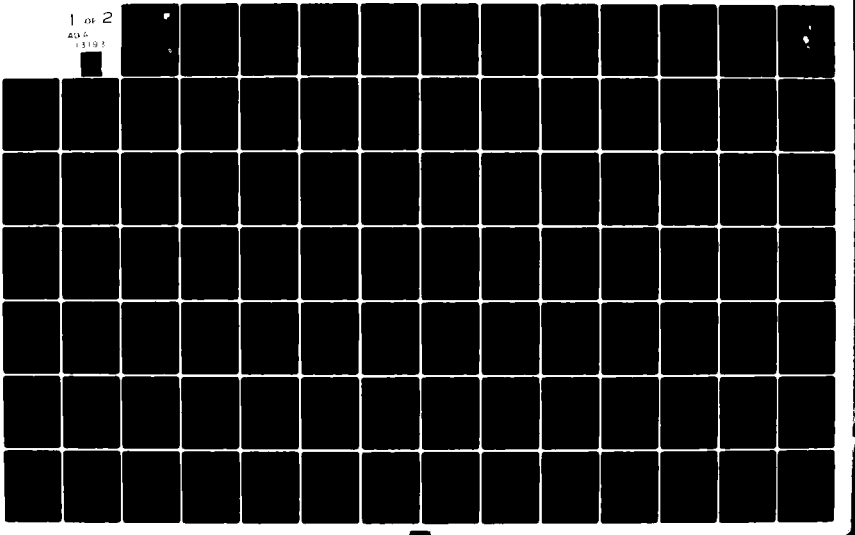

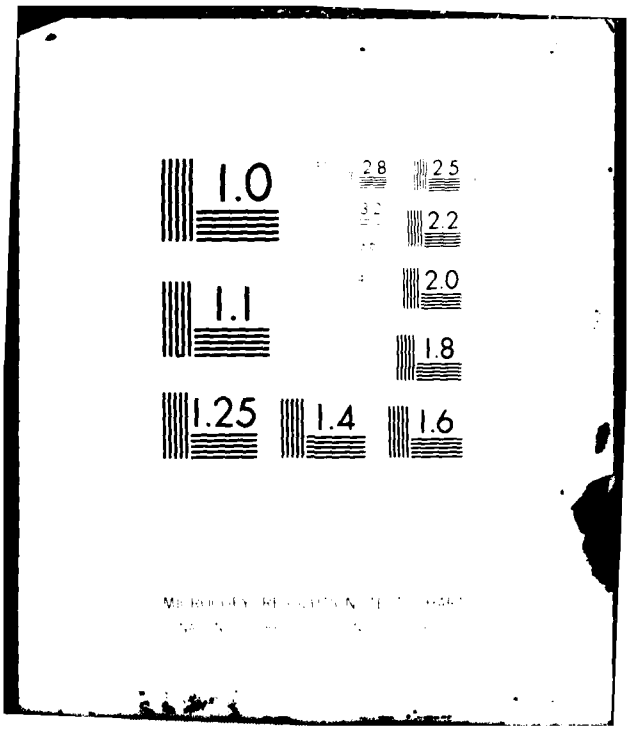
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RADC-TR-81-375
Final Technical Report
January 1982

ELECTRONICALLY TUNABLE AMPLIFIER TECHNOLOGY

E-Systems, Inc.

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Electromagnetic Compatibility (EMC)	PIN Diode Switched Capacitors

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)
The development and design of an electronically tunable frequency stacked filter pair based on a combination of classical microwave filter cavity designs and an electronically tuned resonator design technique is described in this technical report. The filters, consisting of a 100 watt two pole filter and a 1000 watt single pole resonator, are intended to be placed at the input and output of a frequency hopping UHF power amplifier to reduce the broadband noise and spurious signal outputs of the resulting electronically tunable amplifier. The improvement in EMC (electromagnetic

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compatibility) performance allows the amplifier to be used in colocation environments with other equipment.

The design of each of the electronically tuned filters is based on a previously developed method of tuning a high power resonator with PIN diode switched capacitors. The correlation of the design of both the combline input filter and the coaxial resonator output filter to the electronically tuned resonator with the susceptance slope parameters required is developed with the mathematical models presented in the report.

The primary result of the research effort is the development of an experimental model filter pair which demonstrates the feasibility of operating at power levels compatible with a 1000 watt power amplifier and tuning within the 350 to 400 MHz band in less than 60 microseconds. The model tracking filter pair includes the RF cavities, electronic tuning networks, driver networks to interface between the RF circuits and control circuits, and frequency control interface between circuits to convert a parallel encoded frequency input to the control code required to tune the filter to the commanded frequency. The two filters are implemented such that they may be operated individually or as a tracked set.

The performance of the experimental model verifies the basic feasibility of the design concepts used to implement the tracking filter set. Although problems with component losses caused tradeoffs to be required in the design goals resulting in a slightly higher insertion loss and wider bandwidth in the input filter and a doubling of the desired bandwidth in the putput filter, the basic filter performance, power handling, and tuning capability were demonstrated. Significant improvement in the EMC performance of a solid state power amplifier was achieved with the filters installed.

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1.0 INTRODUCTION

Present designs of solid state transmitters and power amplifiers typically incorporate broadband device matching networks to achieve wide operating frequency ranges without requiring tuning. Although this design technique simplifies the application of the transmitter by minimizing interface and tuning requirements (particularly useful in frequency agile systems) and significantly reduces the design complexity compared to cavity tuned designs, the electromagnetic compatibility (EMC) performance of the amplifier is degraded. Broadband noise and spurious signals from the transmitter and power amplifier are not reduced by internal frequency selective networks, and the highly nonlinear power output stages are directly exposed to external interfering signals, resulting in antenna conducted intermodulation distortion problems.

Applications requiring the use of multiple high level transmitters colocated with high sensitivity receivers are severely affected by the EMC performance of the equipment used. A typical response to the EMC problems described includes the use of transmitter output bandpass filtering, receiver filtering, and frequency management techniques in addition to improving the characteristics of the sources and receivers and their operational environment. However, the use of fast tuning frequency agile sources eliminates the option of using fixed or electromechanical servo-tuned filters, requiring new design methods to allow non-interfering operation of colocated equipment.

The subject of this contract is to address the EMC problems of fast tuning frequency agile communications systems using transmitters and power amplifiers operating at power levels to

1000 watts in the military UHF band. The objective of the effort is to develop frequency hopping filtering techniques to reduce transmitted broadband noise and spurious outputs from present solid state transmitters and power amplifiers. This report documents the development of an electronically tuned frequency tracked filter pair (Figure 1.1) intended for use with a separate transmitter and power amplifier to form an electronically tunable amplifier.

1.1 Description of the Problem

Specifically, this contract is directed toward improving the EMC performance of a 100 watt frequency agile transmitter and 1000 watt external solid state power amplifier set operating over the 350 to 400 MHz band. The EMC improvement desired is to be obtained by reducing the level of input broadband noise and spurious signals to the power amplifier with a two pole bandpass input filter and by further reducing the amplified residual input noise and internally generated undesired signals from the power amplifier with a single pole output resonator. The output resonator also serves to isolate the power amplifier output stages from external interfering signals to reduce antenna conducted intermodulation distortion products. Both filters are to be electronically tuned to allow up to 200 frequency changes per second and are to be frequency tracked. The overall desired system configuration is shown in Figure 1.2.

1.2 Program Requirements and Goals

The effort undertaken on this program is directed toward developing, constructing, and testing an experimental model electronically tuned, frequency tracked filter pair for use with a 1000 watt solid state amplifier. This experimental model is intended to demonstrate the feasibility of the design concept

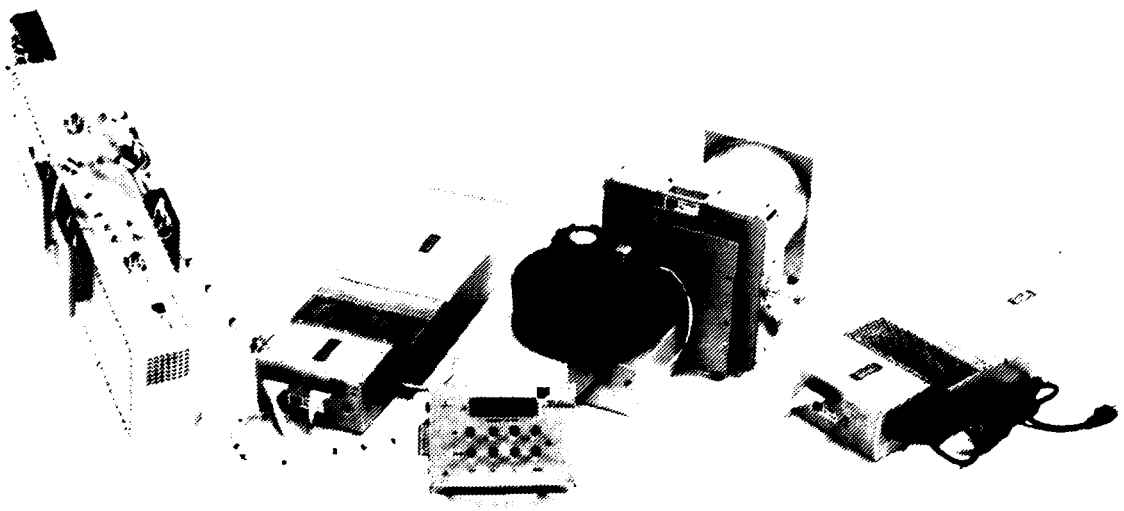

Figure 1.1 Electronically Tuned Filter Pair Experimental Model

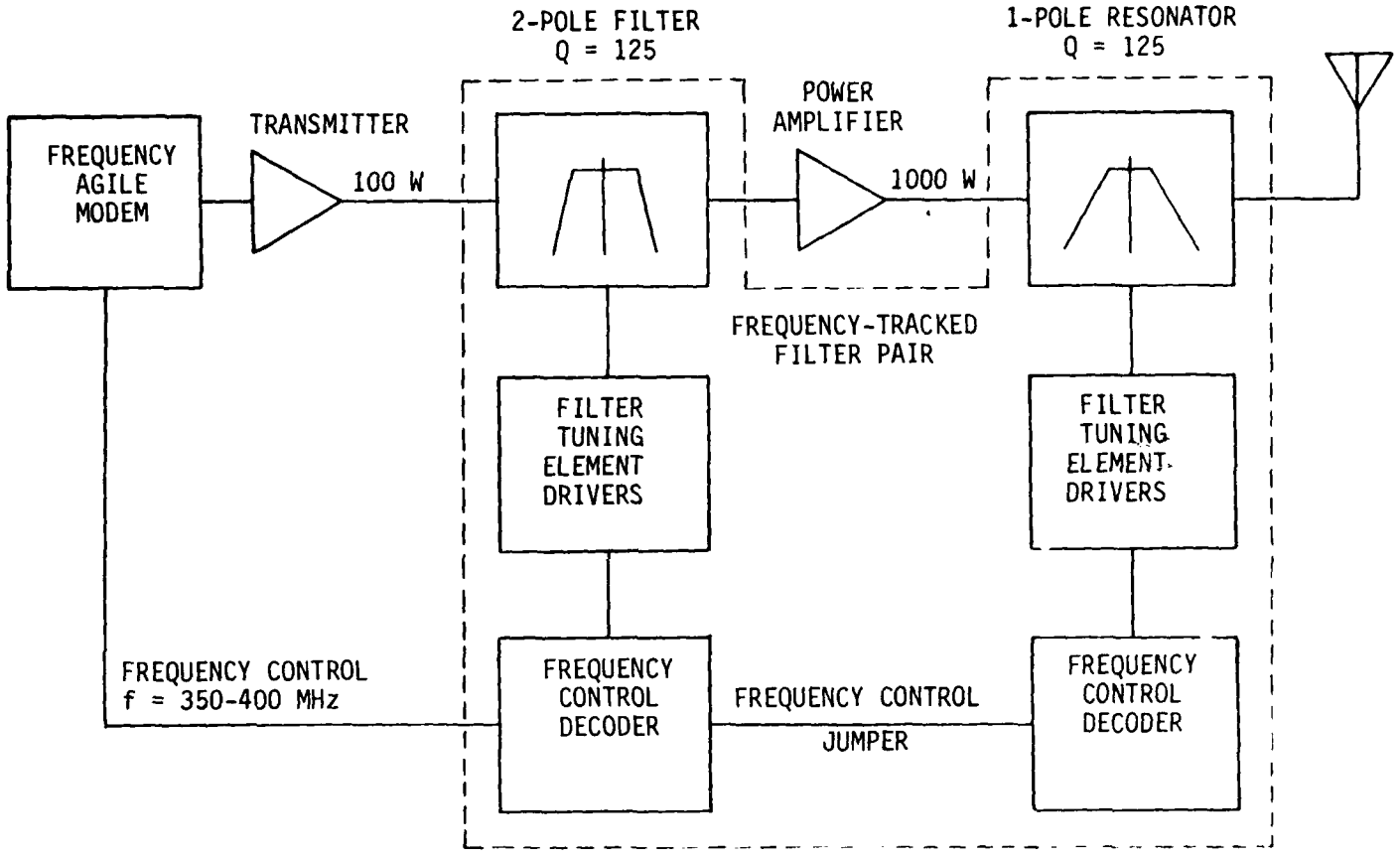

Figure 1.2 Electronically Tuned Amplifier Block Diagram

and to evaluate the improvement in EMC performance of the power amplifier as described in Paragraph 1.1. A complete list of requirements and goals of the filter development effort as described in statement of work N-0-5012 dated 20 June 1979 and Amendment No. 1 dated 07 November 1979 is presented in Tables 1.1 and 1.2.

1.3 Program Summary

The primary result of this effort is the development of an experimental model electronically tuned, frequency tracked filter pair which demonstrates the feasibility of operating at power levels compatible with a 1000 watt power amplifier and tuning within the 350 to 400 MHz band in less than 60 microseconds. The model tracking filter pair includes the RF cavities, electronic tuning networks, driver networks to interface between the RF circuits and control circuits, and frequency control interface circuits to convert a parallel BCD (binary coded decimal) encoded frequency input to the control code required to tune the filter to the commanded frequency. The two filters are implemented such that they may be operated individually or as a tracked set.

The designs of the input and output filters are based on a technique of varying the center frequency of a transmission line resonator by switching high Q (quality factor) ceramic capacitors with high power PIN diodes into the cavity circuit. This tuning method is particularly suited to high RF power levels and the high RF voltages and currents as are present in the high Q resonators required for the filters. Further, the basic concept used provides the flexibility required to implement the desired tuning function with widely varying design parameters such as impedance levels, loaded Q's, power handling requirements, and cavity implementation. These variations are present between the

Table 1.1 Electronically Tuned Filter Pair
Design Requirements

SOW PARAGRAPH	ITEM	REQUIREMENT
4.1.1.1	Input Resonator	Two pole electronically tuned
4.1.1.2	Output Resonator	Single pole electronically tuned
4.1.1.3	Tuning Range	350 to 400 MHz
4.1.1.4	Tuning Interval	2 MHz maximum
4.1.1.5	Tuning Time	Up to 200 hops/second
4.1.1.6	Power Capability	
4.1.1.6.1	Input Resonator	100 Watts CW/FSK
4.1.1.6.2	Output Resonator	1000 Watts CW/FSK
4.1.1.7	Impedance	50 ohms nominal input/output for each resonator
4.1.1.8	Connectors	
4.1.1.8.1	Input	Type N
4.1.1.8.2	Output	Type N or HN
4.1.1.9	Cooling	As required

Table 1.2 Electronically Tuned Filter Pair
Design Goals

SOW PARAGRAPH	ITEM	DESIGN GOAL
4.1.2.1	Intermodulation Products	Minimize forward and reverse
4.1.2.2	Resonator loaded Q	125 minimum
4.1.2.3	Duty Cycle	Compatible with RF power requirement and hopping rate
4.1.2.4	Bandwidth	3 MHz maximum 3 dB bandwidth
4.1.2.5	Insertion Loss	2 dB/resonator
4.1.2.6	Resonator Tracking	Both resonators tracked to within $\pm$200 kHz

input and output filters of the resonator set to optimize the electrical performance of each filter to its operating requirements.

The performance of the experimental model verifies the basic feasibility of the design concepts used to implement the tracking filter set. All of the design requirements of Table 1.1 were demonstrated with the experimental model. However, although the output filter can be operated at its 1000 watt rating at the band edges, a problem with the current handling capabilitiy of the tuning capacitors limits the power capability at many of the center frequencies across the band. This unexpected component limited effect is discussed further in Paragraph 3.2.3.2. Of the design goals as listed in Table 1.2, several trade-offs were made in the performance of the filters because of an unexplained limitation in the unloaded Q achieved relative to the initial design projections. For the input filter, the narrow bandwidth desired was basically maintained and insertion loss allowed to exceed the 2 dB goal to maximize the rejection of transmitter noise. The bandwidth of the output filter was increased to reduce insertion loss to the 1 dB region to obtain the power handling capability desired. Additional details concerning these changes are included in Paragraph 3.1. In spite of the reduced selectivity from the initial design goals, substantial improvements were made in the EMC performance of a driver-power amplifier set as described in Paragraph 3.2.5. Further, recommendations of means of improving the filter designs to obtain additional EMC performance enhancements and to resolve the unloaded Q limitations of the present designs are described in Section 5.0 of this report.

1.4 Program Accomplishments

Although the designs of the input filter and output resonator of the tracking filter set are based primarily on an electronically tuned resonator previously developed and modeled, several new accomplishments were made reflecting directly on this program and on electronically tuned filters in general. These accomplishments include:

- The capability of operating an electronically tuned filter at the 1000 watt level was demonstrated.
- Concepts used to increase the power handling capability of electronically tuned resonators such as RF current splitting through multiple tuning bit sets and selection of the resonator configuration to optimize performance to the capability of the tuning components were verified.
- Methods previously used to implement the electronically tuned resonator were extended to include a coaxial cylindrical RF cavity.
- A potential capacitor dielectric loss contribution to unexpected unloaded Q degradation of the filters was discovered.
- The PIN diode driver circuit was improved by increasing switching speed and modifying the forward bias circuit to incorporate a constant current source, resulting in improved regulation of the bias supply and improved power dissipation handling capability.

2.0 TRACKING FILTER PAIR DESIGN

The design of each filter for the electronically tuned filter pair is concerned with translating the overall filter performance requirements to corresponding requirements for the electronically tuned resonators. Because each filter is intended for a high power application with high selectivity, high levels of circulating RF currents and large RF voltages must be withstood in the filter structure. Low losses are also required to minimize dissipation and maintain the filter response close to the ideal expected response. These factors, coupled with the 350-400 MHz tuning range, indicate that a transmission line cavity-type filter structure is well suited for both filters. The high unloaded Q achievable in an air dielectric cavity and the substantial mechanical structure of the cavity both are particularly important to this application. Further, the desired filter bandpass is directly correlated to the cavity filter response.

2.1 Input Filter Design

The input filter of the electronically tuned filter pair is a two pole design intended to tune across the 350 to 400 MHz band with the capability to handle RF power input levels up to 100 watts continuously. Design objectives of 2 dB maximum insertion loss and a loaded Q of 125 dictate a filter structure capable of a narrow bandwidth response and low filter loss contribution. In addition, the individual requirements of the RF cavity design, the electronically tuned resonators, and the integration of the two into a completed filter must all be considered in the selection of a design approach.

Because of the advantages of a transmission line cavity and because of previous successful results in applying electronic

tuning to similar filters, an air dielectric combline[1] structure was selected for the input filter. The basic combline filter is a low loss transmission line implementation of a standard bandpass filter response. The RF cavity structure provides advantages in its mechanical stability, ease of implementation, and minimal sensitivity of electrical performance parameters to mechanical dimensions. Further, the filter resonators are isolated, grounded transmission lines which easily adapt to electronic tuning.

2.1.1 RF Cavity Development

A simple derivation of the combline filter structure is presented in the following paragraphs. This derivation is directed toward defining the characteristics of the individual resonators in the combline filter such that an electronically tuned resonator with the identical response is designed to be included in the electronically tuned input filter. In addition, the proper correlation of the designed resonator to the resonator as it is applied in the filter structure permits an accurate characterization of the filter power handling capability, loss, and other electrical parameters.

The basic lumped element, generalized bandpass circuit shown in Figure 2.1 is the starting point for a two pole filter design. The bandpass circuit as shown results from a standard lowpass to bandpass mapping function and includes the dissipative losses of the resonant elements.

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[1] G.L.Matthaei, L. Young and E.M.T. Jones, Microwave Filters, Impedance Matching Networks, and Coupling Structures, McGraw-Hill Book Co., N.Y., 1964.

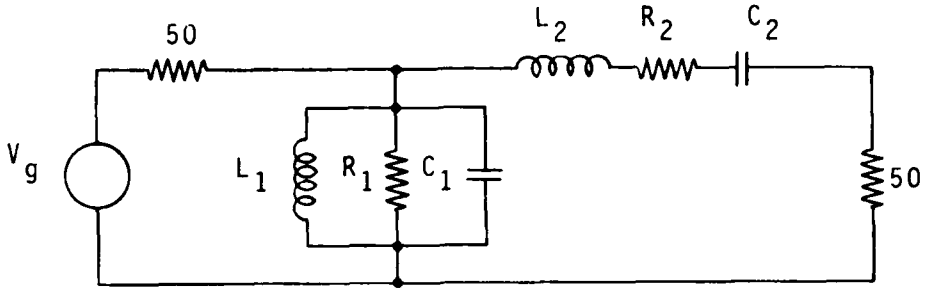


Figure 2.1 Two Pole Lumped Element Bandpass Filter

The series resonant circuit composed of L_2, C_2, and R_2 can be converted to a parallel resonant equivalent by imbedding a parallel resonant circuit between two admittance inverters. The admittance inverter acts as a quarter wavelength of transmission line of impedance J at all frequencies. Therefore, at the terminals of the inverters, the shunt inductance appears as a series capacitance, etc., as in the original model. The inverter in the final filter configuration between the new parallel resonant circuit and the 50 ohm termination can be removed since it has no effect on the amplitude response of the filter. This situation is analogous to terminating a transmission line in its characteristic impedance. The two pole filter model modified to obtain two parallel resonant circuits is shown (minus the output inverter) in Figure 2.2.

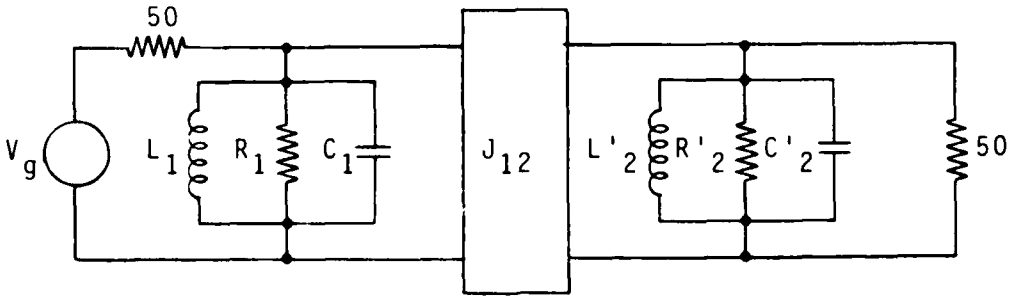


Figure 2.2 Modified Two Pole Bandpass Filter

The next step in the development of the combline filter is the correlation of the parallel resonant circuits to a transmission line equivalent circuit. At frequencies near resonance, the rate of change of input susceptance is described by the resonator susceptance slope parameter, β, which is defined as:

$$\beta = \frac{\omega_o}{2} \left. \frac{dB}{d\omega} \right|_{\omega_o}$$

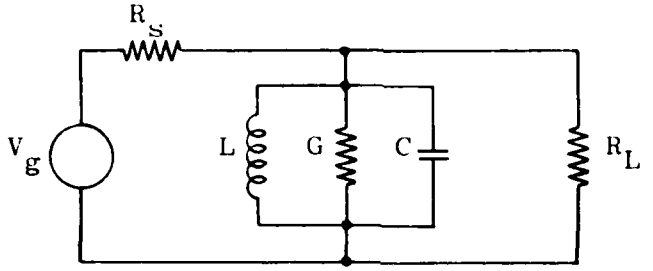
Where: B = Susceptance component of circuit input admittance

ω_o = Circuit resonant frequency

This parameter is directly related to the bandwidth, or loaded Q (center frequency to bandwidth ratio) as shown in Figure 2.3. Also shown in Figure 2.3 is an expression directly relating the lowpass prototype filter values to the resonator susceptance slope values required for a given filter.

For a given parallel lumped element circuit, a transmission line circuit with an identical response near resonance is defined by the susceptance slope parameter. As shown in Figure 2.4, the transmission line equivalent can be a quarter wave shorted stub of a specified characteristic admittance or a foreshortened capacitively loaded shorted stub. Substituting the transmission line resonator in the model of Figure 2.2, and adding ideal input and output transformers to modify the resonator impedance level as desired yields the model of Figure 2.5.

The final translation of the filter to the equivalent combline structure is made by replacing the open-wire transmission line equivalent model of Figure 2.5 with its parallel coupled line equivalent as shown in Figure 2.6. Essentially,



$$\beta = \omega_o C = \frac{1}{\omega_o L}$$

$$Q_L = \beta/(1/R_S + 1/R_L + G)$$

$$Q_U = \beta/G$$

CORRELATING TO A LOWPASS PROTOTYPE:

$$\beta_j = \frac{g_j \, \omega'_1}{W}$$

WHERE:

β_j = SUSCEPTANCE SLOPE PARAMETER FOR jTH RESONATOR

G_j = LOWPASS PROTOTYPE FILTER VALUES

ω'_1 = 3 DB BANDWIDTH OF LOWPASS PROTOTYPE = 1

W = FRACTIONAL BANDWIDTH OF BANDPASS FILTER

Figure 2.3 Resonant Circuit Susceptance Slope Parameter

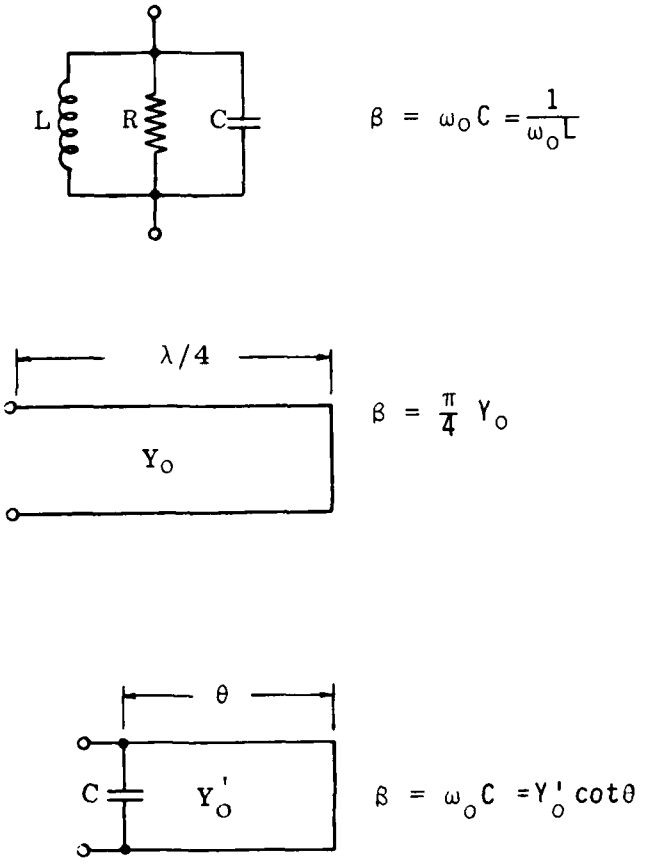


Figure 2.4 Transmission Line Resonator Equivalences

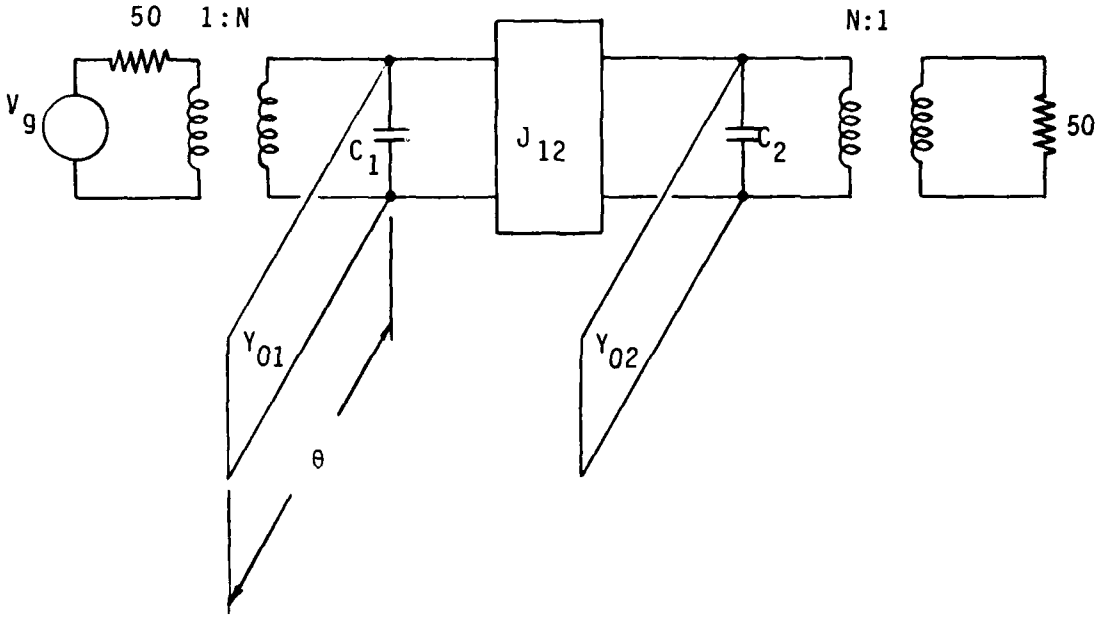


Figure 2.5 Open-Wire Two Pole Transmission-Line Filter Model

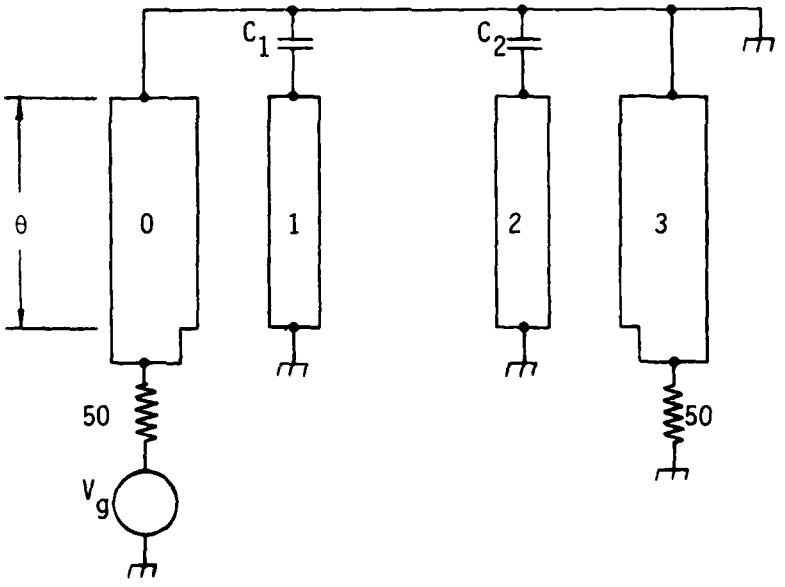


Figure 2.6 Combline Two Pole Bandpass Filter

lines 0 and 3 are the input and output transformers, with the RF signals coupled to resonators 1 and 2 through the gaps between the lines. The admittance inverter is realized through the coupling gap between the resonators. The combline circuit yields a structure with totally isolated tuned resonators and has the mechanical characteristics desirable for high power use.

Each of the resonators in the final combline structure has a susceptance slope parameter directly related to the initial lumped element model as was listed in Figure 2.3. If the isolated resonators of the combline are removed and replaced with similar electronically tuned resonators with the appropriate susceptance slope parameter, the desired filter is achieved in an electronically tuned form. This factor is the basis of correlation between the electronically tuned resonators and the basic combline filter bandpass desired.

One final consideration to be made in the design of the filter is the effect of the admittance inverter on the overall filter response. As described by Matthaei[2], the admittance inverter has the effect of sharpening the response (or reducing the bandwidth) compared to not using the quarterwave coupling technique. The effect is accounted for in the definition of the doubly loaded Q for each resonator in the filter. Doubly loaded Q is defined as the loaded Q resulting from removing the resonator and its effective coupling from the filter and placing a source and load on the resulting single pole filter. Then, the doubly loaded Q is defined as

$$Q_{DL} = \left(\beta j - \frac{\pi}{4}\right)\Big/2 \quad \text{for } j = 1 \text{ or } N$$

$$= \left(\beta j - \frac{\pi}{2}\right)\Big/2 \quad \text{for } j = 2 \text{ to } N-1$$

where N is the number of filter poles.

---

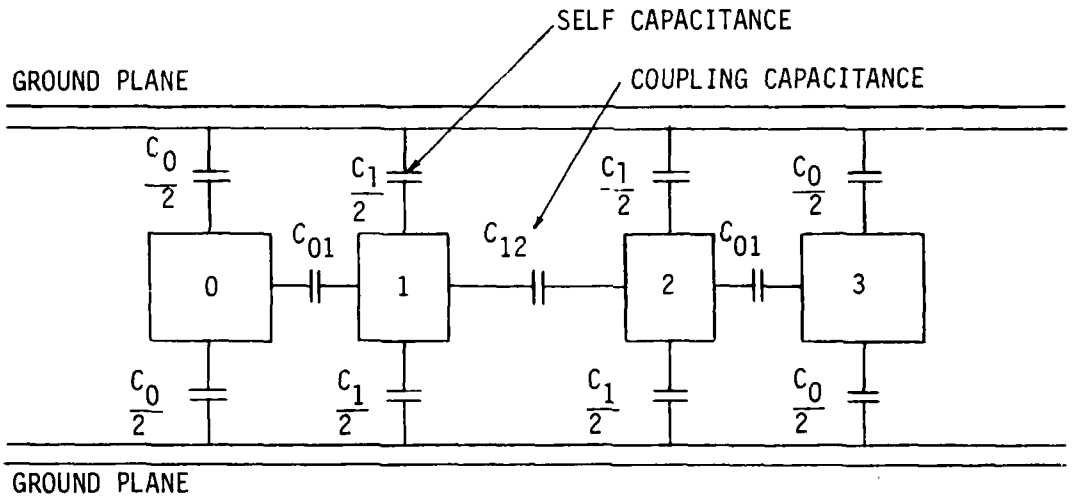
[2]Matthaei, op. cit., Section 8.10

Therefore, for the two pole input filter, a nominal loaded Q of 125 is desired. To maximize passband flatness and minimize VSWR ripples across the band, a Butterworth response characteristic is chosen. A susceptance slope parameter of 177 for each resonator is therefore implied. Finally, a doubly loaded Q of 88 for each resonator is required. The design of the electronically tuned resonators for the filter is based on achieving a loaded Q of 88 to obtain the overall filter response desired. Under this condition, both resonators are identical, and voltage stresses and other electrical parameters projected for the electronically tuned resonator are equivalent to the actual levels present in the two pole filter.

Completing the electrical design of the combline structure for the input filter, a nominal input/output impedance of 50 ohms is desired. To maximize the unloaded Q (minimize cavity losses), a characteristic impedance of 65 ohms is selected for the filter resonators. The selection of 65 ohms is also based on the electrical trade-offs of resonator tuning network voltage and tuning reactance range required to cover the frequency band and on the slight mechanical advantage of increased transmission line width with lower impedance lines. (Recall that the insertion of the ideal input and output transformers in the filter model permits the intermediate impedance level to be arbitrarily selected). Finally, the resonator electrical line length is selected such that the line is a quarterwave long at 635 MHz. Selection of this factor is based on achieving the tuning range maximum limit taking into consideration the minimum reactance of the electronic tuning network to be installed.

Using the resonator parameters listed in the preceding paragraph and the overall selectivity requirements for the filter, the self- and coupling capacitances for the transformer lines

and resonators of the combline structure are calculated. These capacitances are defined as shown in Figure 2.7, and the corresponding values for the input filter are listed in Table 2.1. The values of self- and coupling capacitance are used later in the mechanical design of the input filter cavity.



0 & 3 ARE INPUT/OUTPUT TRANSFORMERS
1 & 2 ARE RESONATORS
BY SYMMETRY, 0 = 3, 1 = 2

Figure 2.7 Filter Self- and Coupling Capacitances

Table 2.1 Two Pole Input Filter Distributed Capacitance

Normalized Self-Capacitance Per Unit Length

$$\frac{C_0}{\varepsilon} = 6.7462$$

$$\frac{C_1}{\varepsilon} = 6.28597$$

Normalized Coupling Capacitance Per Unit Length

$$\frac{C_{01}}{\varepsilon} = 0.49797$$

$$\frac{C_{12}}{\varepsilon} = 0.04567$$

All values normalized to ε (permittivity),
In air dielectric:

$$\varepsilon = 0.225 \text{ pF/inch}$$

2.1.2 Electronically Tuned Resonator

The electronically tuned resonators used in the two pole input filter must have high unloaded Q and be capable of operating at power levels up to 100 watts. As described in Paragraph 2.1.1, each resonator must have a doubly loaded Q of 88 as defined by the susceptance slope parameter for the overall two pole filter with a loaded Q of 125. The two resonators are synchronously tuned and cover the 350 to 400 MHz band in 2 MHz maximum steps at a switching rate compatible with 200 hops per second.

As mentioned previously, the electronically tuned resonators are based on a proprietary design technique previously developed. Briefly, the resonators use a transmission-line section and a fixed lumped capacitor as a primary resonant circuit. Fixed high Q ceramic capacitors connected through high power PIN diodes are also coupled to the resonant circuit to tune the filter. By properly selecting and weighting the fixed capacitor values, the tuning range desired can be uniformly covered with a tuning resolution determined by the number of capacitor-diode tuning elements used.

A set of computer analysis and design programs describe the electronically tuned resonator and the stray elements existing in the RF tuning networks. Each resonator is individually designed on the basis of obtaining the doubly loaded Q required so that projections of withstanding voltages, circulating currents, and other operating parameters correctly describe the performance in the completed filter. The software describing the resonators permits the tuning elements to be coupled to the resonator such that a specified RF voltage is not exceeded for a given input power. This property allows intermodulation distortion products generated within the tuning networks to be minimized.

For the two pole input filter, a 65 ohm transmission line section one quarter wavelength long at 635 MHz is used as the resonator element. This resonator is tuned to approximately 400 MHz with a 1.9 pF fixed capacitor and the stray reactance of the electronic tuning network. Finally, PIN diode switched capacitors from 0.80 to 3.00 pF, with the most significant tuning bit split into two sections to improve RF current handling capability, are used to tune the resonator from 350 to 400 MHz.

An eight bit tuning code providing 2^8 or 256 center frequencies with approximately 200 kHz resolution is used for the input filter. The high resolution resulting from the additional tuning codes is used to allow the two resonators to be easily tracked to each other electronically by using separate bias controls to each RF tuning network and also permits frequency tracking to the output filter. To optimize the tuning network unloaded Q while minimizing DC power dissipation, graduated diode bias currents from 0.25 to 1.0 amps are used, and a reverse bias voltage of 900 volts is used to maximize diode OFF resistance and maximize power handling capability. Tuning speed is set essentially by the speed at which the PIN diode bias circuit can make the transition between forward and reverse bias.

The final major factor analyzed for the electronically tunable resonators is the unloaded Q achievable and the effects of component losses on the insertion loss of the overall filter. Since air dielectric RF cavities are typically used for high power filters, losses in the tuning networks tend to be the limiting factor in the unloaded Q achievable. For the two pole Butterworth response input filter, insertion loss can be projected from the equation:

$$\text{Loss (dB)} = 20 \log (C_n d_k + 1)$$

Where $C_n = a_1/a_0$ = First term of the transfer function polynomial

$C_n = 1.41$ for a two pole Butterworth filter

$d_k = Q_{LTOT}/(Q_{unl}/\text{pole})$

Q_{LTOT} = Overall filter loaded Q

Q_{unl}/pole = Unloaded resonator Q per resonator

To achieve a 2 dB filter insertion loss with a loaded Q of 125, an unloaded Q per resonator of 680 is required. Initial projections of 1200 minimum for unloaded Q (including the RF cavity) yields a filter loss of 1.2 dB. However, as discussed in Paragraph 3.1, the projections were not met for unexplained reasons, and a nominal unloaded Q of only 450 was achieved.

2.1.3 Input Filter Implementation

The mechanical design of the input filter is based on the combline structure selected and the physical requirements of the electronic tuning networks. The primary combline design model was shown in Figure 2.6, and the parameters controlling the mechanical layout and design of the cavity structure were presented in Figure 2.7 and Table 2.1. Based on these values, an air dielectric stripline cavity with rectangular bars between parallel ground planes was designed using standard methods[3]. The mechanical structure resulting from the design is shown in Figure 2.8 and at the extreme left in Figure 1.1.

A large plate spacing (3 inches) was selected for the input filter to maximize the unloaded Q of the resonators. Because the lateral dimensions of the filter are proportional to the cavity height, the overall width and sizes of the rectangular bars are also increased compared with resonators previously constructed. The increased spacing between tuning networks within the cavity results in a beneficial reduction in undesired coupling between the tuning elements of the two resonators.

The two pole filter cavity is constructed of 0.25 inch aluminum presurfaced jig-plate sheet stock and is fastened together with screws and welded joints. The transformers and

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[3] W.J.Getsinger, "Coupled Rectangular Bars Between Parallel Ground Planes", IEEE Transactions on Microwave Theory and Techniques, Volume MTT-10, No. 11, November 1962.

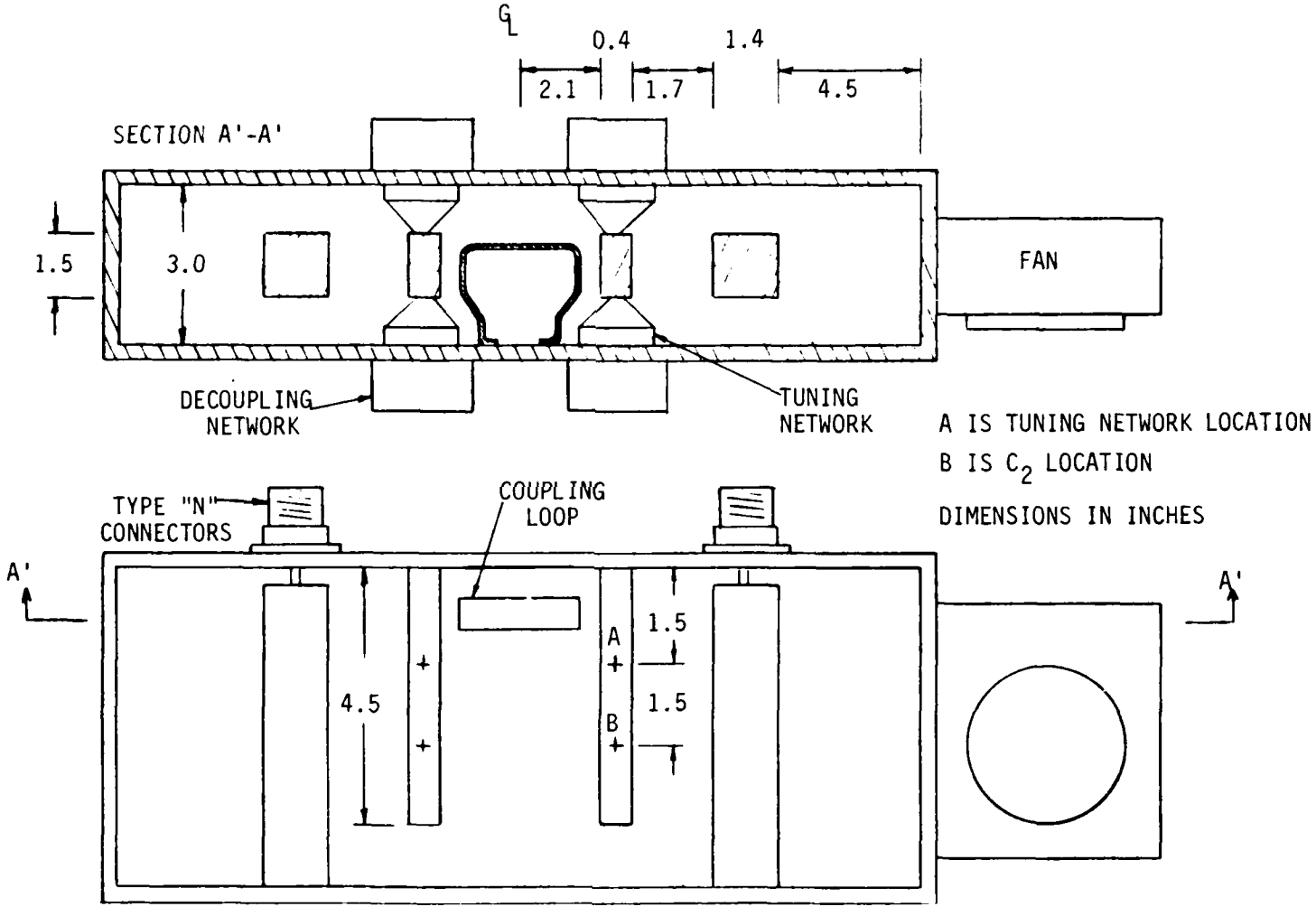


Figure 2.8 Input Filter Layout

resonator bars are machined aluminum stock and are silver plated to maximize the resonator unloaded Q. Type "N" input and output connectors are used on the coupling transformers. A small blower is attached to the RF cavity sidewall to circulate air through the cavity interior and across the tuning networks. The air circulation keeps temperatures in the tuning network below a problem range by minimizing hot spots. All tuning element components are also mounted directly to the cavity walls to provide heatsinking in addition to maximum RF grounding.

Initial tests on the RF cavity with the tuning networks installed showed that the resonators were slightly overcoupled and that the input match was slightly beyond the desired VSWR limit of 1.5:1. Two modifications were experimentally determined to improve the coupling. First, a coupling loop was added between the resonators near the grounded end to increase the magnetic coupling between resonators. The second change was to increase the transformer width and narrow the gap between the transformers and the resonators. These changes, shown in Figure 2.8, resulted in improved coupling and input match for the filter. The deviation between the original coupling design and the revised coupling finally used is the result of the effect of introducing the electronically tuned resonators into the cavity. Because the circulating currents within the resonator are altered by the tuning network as opposed to the normal combline filter, slight adjustments are required to establish proper coupling.

2.2 Output Resonator Design

The output filter of the electronically tuned filter pair is a single pole resonator design which tunes and is tracked by the input filter over the 350 to 400 MHz band. The output filter

RF power handling capability is required to be 1000 watts. As with the input filter, design objectives of 2 dB maximum insertion loss and a loaded Q of 125 dictate a high unloaded Q filter structure with high power handling and dissipation capabilities.

A circular cylindrical coaxial RF cavity with input and output coupling loops was chosen for the output resonator. To maximize unloaded Q and power handling capability, a large (6 inch diameter) cavity with a low characteristic impedance is used. Electronic tuning is directly incorporated into the output filter design with a one-to-one correspondence between the electronically tuned resonator model and the filter as implemented.

2.2.1 RF Cavity Design

The requirement for a single pole passband response in the output filter greatly simplifies the design of the output filter structure. The filter response of the output resonator is that of a single parallel resonant circuit with a loaded Q (and doubly loaded Q) of 125. The resonant circuit is implemented as a single transmission line resonator with a susceptance slope parameter equivalent to the parallel resonant circuit as shown in Figure 2.4. The input and output signals are transformer coupled to the resonator using two simple loops. Since only one resonator is used, equivalent input and output loops will provide a good impedance match at resonance, and the loop size serves to set the coupling factor to obtain the desired bandwidth with an arbitrarily selected resonator impedance level.

A coaxial circular RF cavity forms the transmission line section of the output filter. The design objective is to use a 17.2 ohm characteristic impedance line with a nominal 4.5 inch

inside diameter and 6 inch outer diameter. The low characteristic impedance selected is based on a number of factors. First, a relatively large cavity is desired to maximize surface area and spread the circulating RF current over a large area because of the high power level. At the same time, IMD minimization requires that the RF voltage within the tuning network is minimized. For the very high currents resulting in the tuning network, parallel tuning paths are required with a corresponding increased stray tuning network capacitance. The low impedance resonator is compatible with all these characteristics. Further, mechanical advantages of improved stability for the resonator center conductor, large mating surface area between the center conductor and cavity base, and optimal spacing between the inner and outer surfaces of the cavity for the tuning network are all achieved with standard size tubing. The low impedance resonator also provides isolation between the input and output coupling loops to minimize direct coupling from input to output.

2.2.2 Electronically Tuned Resonator

The implementation of electronic tuning in the output filter resonator follows the same basic concept as used in the input filter (Paragraph 2.1.2). The resonator must have a high unloaded Q and be capable of operating at power levels up to 1000 watts. The bandwidth of the resonator is set by the loaded Q of 125, and the tuning range of 350 to 400 MHz with 2 MHz maximum steps at a switching rate compatible with 200 hops per second matches the input resonator requirements.

For the output filter, a 17.26 ohm transmission line characteristic impedance was the initial design value for the resonator. Final machining on the material to obtain true surfaces resulted in a 17.6 ohm resonator. At 160 MHz, the transmission

line is one quarter wavelength long, and a fixed 4.2 pF capacitor and the total stray reactance of the tuning network is used to tune the filter to approximately 400 MHz. Finally, PIN diode switched capacitor sets control total capacitance values of from 4.2 to 52.7 pF to tune the filter from 350 to 400 MHz.

A five bit tuning code was selected to cover the tuning range in 32 increments for the output filter. The original design projection for the tuning elements and stray reactances present indicated a maximum tuning increment of 1.8 MHz. Because the total series inductance of interconnecting leads was slightly higher than originally anticipated, a final resolution of 2 MHz was obtained. The five bit tuning code is realized as thirteen separate diode capacitor sets, with the individual capacitor values ranging from 4.2 to 8.8 pF. Because the tuning bits are paralleled, a more uniform RF current split is obtained around the resonator circumference for the tuning codes where the circulating current is highest, and the tuning elements are operated within their projected ratings. As described in Paragraph 3.2.3.2, the current handling capability of the tuning capacitors was overestimated, resulting in component failure during testing at rated power.

Each diode-capacitor set is controlled with a 1 amp forward bias or 900 volt reverse bias level. Although the tuning network position combined with the low impedance of the resonator tends to emphasize the ON resistance characteristics of the tuning elements, the high reverse bias voltage is still required to maximize power handling capability and minimize generation of IMD products.

Because of the extremely high operating power level and high loaded Q of the output filter, the unloaded Q requirements have particular importance. For a single pole filter, the loaded Q and unloaded Q versus loss is projected from the equation:

$$\text{Loss (dB)} = 20 \log \frac{Q_{unl}}{Q_{unl} - Q_L}$$

Therefore, a 2 dB insertion loss corresponds to a minimum unloaded Q requirement of 608 for the output filter. The initial projection of total resonator losses yielded an unloaded Q of over 1100 (loss of 1.1 dB), and no problems were anticipated. Note that at a 1000 watt input, a 1 dB loss corresponds to 200 watts dissipation and a 2 dB loss corresponds to 370 watts dissipated. Since most of the losses are present within the tuning network, the tuning components will be subjected to the total heat load of this loss. As described in Paragraph 3.1, since the total unloaded Q actually achieved was low (as in the input filter), the bandwidth was degraded to obtain a final insertion loss of nominally 1 dB because of the heating conditions.

The computer analysis and optimization of the output resonator reveals that because of the extremes taken to optimize high loaded Q, high power, and low IMD in the design, the resonator design parameters have relatively high sensitivities. Thus, small variations in the various design parameters can cause significant changes in the overall results. For a sample of one, this factor is not a problem since corrective action can be taken to obtain the performance desired. However, this is not a desirable feature for a unit to be exposed to wide ranging environments or for a production design.

2.2.3 Output Filter Implementation

The output filter is a single pole cylindrical coaxial transmission line resonator with a design characteristic impedance of 17.26 ohms and using input and output loops for coupling. A basic sketch of the cavity design is shown in Figure 2.9. As previously described, the basic cavity diameters are selected based on the power handling requirement, a desire to maximize the cavity surface area, and the resonator gap spacing with respect to the tuning element dimensions and layout.

The primary cavity resonator is constructed of aluminum tubing stock with a nominal inside diameter of 6 inches and a nominal outside diameter of 4.5 inches. The tubing is welded to flat plate stock and assembled with close-machined interlocking joints to maximize surface contact and minimize RF losses. Since the basic stock material used throughout the filter is 0.25 inches thick, the resulting structure is mechanically rigid and not prone to vibration effects. Final machining was performed after the unit was welded and partially assembled to provide a smooth surface finish throughout the cavity interior surfaces. The operation to remove scratches and true the cavity results in a slight increase in the resonator impedance to 17.6 ohms. All cavity materials are treated with a chromate finish - no silver plating was used.

Cooling air is circulated through a tube to the end of the resonator center conductor, then along the center conductor inside surface, and finally exhausting along the grounded end of the resonator. Because of the high RF current at the resonator ground, maximum cavity heating is expected along this area. Aluminum pins are pressed into the cavity base between the inner and outer conductors to conduct heat into the air stream. Cooling of the cavity outer walls is by convection and all tuning

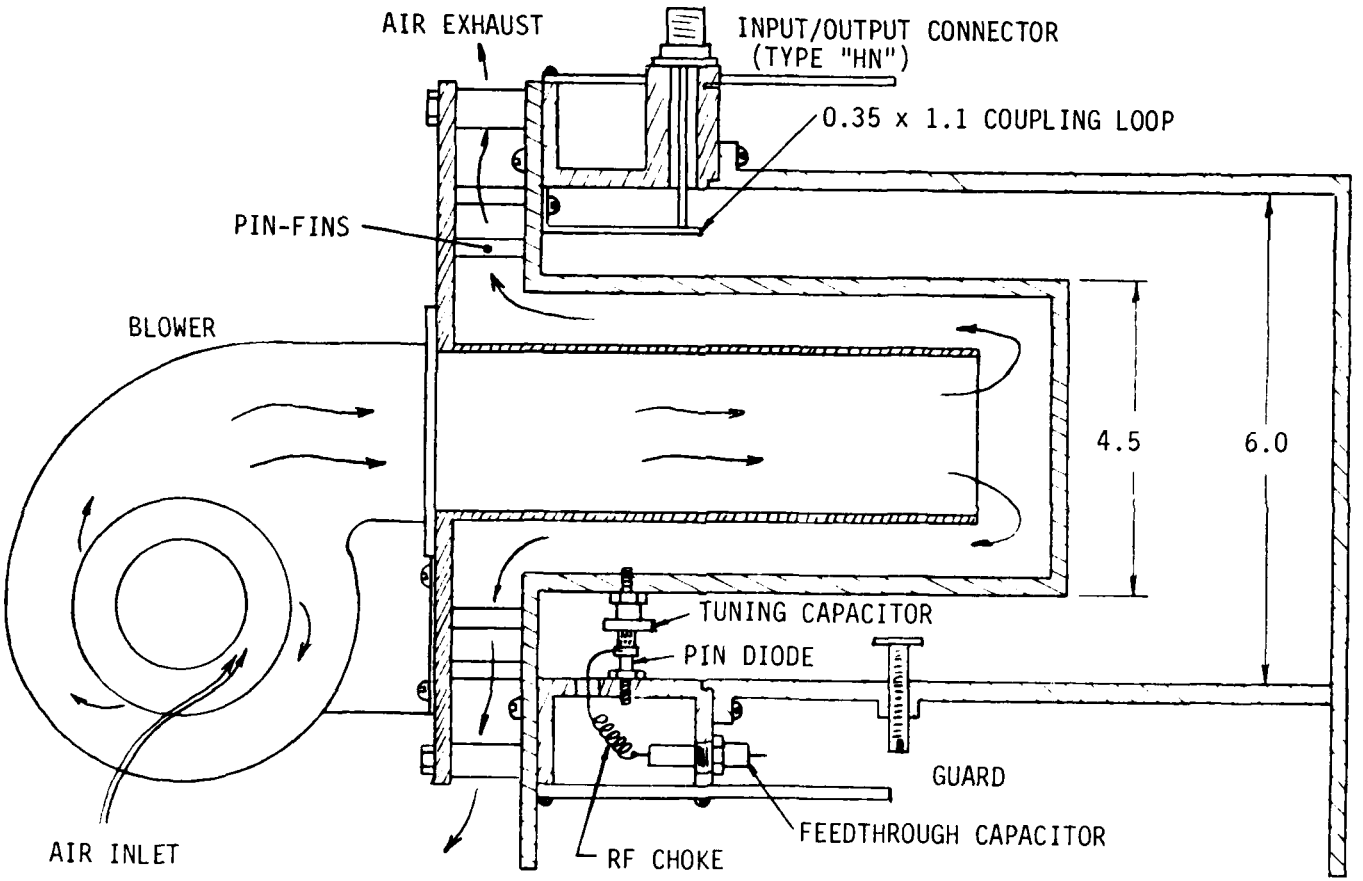


Figure 2.9 Output Filter Implementation

element components are mounted to the cavity walls to provide maximum heatsinking of the PIN diodes and tuning capacitors.

The coupling loops are designed to obtain a loaded Q of 125 at the center of the filter tuning range. Because the presence of the tuning network effectively shunts a portion of the RF cavity circulating current at the lower end of the resonator, the electric field at the open end of the cavity is lower than for an untuned resonator. Therefore, a magnetically coupled cavity with loops inside the tuning network area is more closely related to a standard single frequency resonator. The large diameter of the resonator inner conductor also shields the input and output loops from each other to maximize the ultimate rejection of the output filter.

The size and location of the coupling loops are determined from the equation[4]:

$$\Delta f = \frac{8\ A^2 \mu_0\ f^3 \cos^2\ \theta}{\pi Z_0\ n\ r^2 R_g}$$

Where:

Δf = Resonator 3 dB bandwidth

A = Area of the coupling loop

μ_0 = Permeability of the coupling medium
$= 4\pi \times 10^{-7}$ in air

f = Resonator tuned frequency

Z_0 = Resonator characteristic impedance

n = Number of quarter wavelengths used for resonance

R_g = Generator and load impedance

r = Radius to center of coupling loop

θ = Electrical length from cavity ground to center of coupling loop

[4] Harvard University Radio Research Laboratory Staff, Very High-Frequency Techniques, McGraw-Hill Book Co., Inc., New York 1947, pp 769-795.

As shown in Figure 2.9, the loop size and position are arranged to permit the cavity interior to serve as a portion of the loop. This arrangement plus the use of a wide strap for the loop serve to minimize the self-inductance of the loop circuit. Type "HN" connectors are mated to the coupling loops through a 50 ohm transmission line section integrated into the cavity sidewall.

2.3 Support Electronics

The previous discussions of this section have been concerned with the development of the RF-handling portions of the electronically tuned filter pair. However, to complete the filter, several support circuits are required to perform the PIN diode bias control switching and input interface control functions. The circuits used to control the filter are described in this section.

2.3.1 Filter Frequency Control Interface

The overall frequency control interface for the electronically tuned filter pair is shown in Figure 2.10. A $\overline{\text{BCD}}$ (binary coded decimal) encoded TTL logic compatible input signal is buffered and used as the address for three 2716 EPROM's (ultraviolet-erasable electronically programmable read-only memory). Of the typical 15 line BCD code used for military UHF equipment, only the four 10's MHz, four 1's MHz and the 8, 4, and 2 weighted 0.1's MHz lines are used. This combination of eleven lines provides the capability to address the filter pair with 200 kHz resolution. Since this resolution is similar to that of the input filter, and since the filters are always tuned in the 300 MHz range, additional control lines are not necessary.

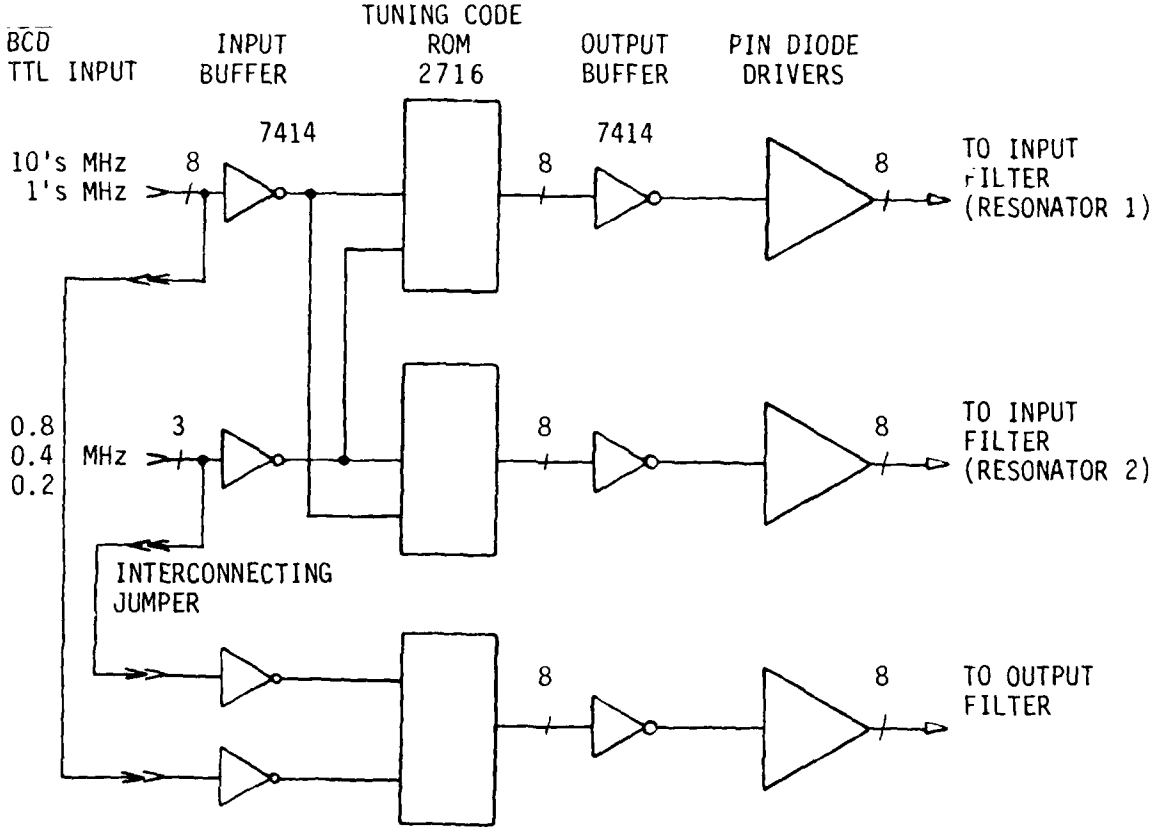


Figure 2.10 Filter Pair Tuning Control Circuit

The 2716 programmable memory IC's contain a binary tuning code for the resonator tuning networks corresponding to each addressed frequency. Of course, only 32 different tuned frequencies exist for the output filter while 250 different frequencies can be addressed by the control system. For both filters, sufficient tuning information is stored to tune the filters to the closest appropriate frequency within the 2 MHz tuning step and 200 kHz tracking objectives. Illegal codes are set to tune to the lowest power dissipation point (400 MHz).

Three eight bit outputs from the control memory are used to control the two filters. One memory IC controls the output filter only. The six paralleled tuning elements used for the most significant bit are split three ways and individually controlled, using the full eight bit IC output. This arrangement allows slightly improved tuning resolution because of the slightly differing stray reactances from code to code. Each of the remaining memory IC's individually controls each resonator of the two pole input filter. The use of individual control codes permits resonator tracking to be performed electronically, rather than having to match capacitors and stray reactances in the tuning networks.

2.3.2 PIN Diode Driver Circuit

The PIN diode driver circuits interface the TTL compatible control signal from the frequency control interface to the reverse bias-forward bias requirements of the RF tuning circuit PIN diodes. As previously described, each PIN diode requires a reverse bias of 900 volts and a forward bias of 0.25 to 1.0 amps, depending on the type diode used and the binary weight of the bit in the tuning code. Because of the hopping

application intended for the filters, the driver circuits must be capable of switching between the levels mentioned within 100 microseconds. The PIN diode driver circuit is a modified version of the circuit previously developed for another RADC project[5].

The tuning speed for the electronically tuned filter pair is set by the rate that the PIN diode bias state can be switched. Two primary factors control the ultimate switching speed achievable and impact the design of the driver networks. First, a large signal swing at the driver output (-1 volt to +900 volts) is required. Since the bias control lines are decoupled within the RF filter cavity with RF chokes and 1500 pF feedthrough capacitors, and paralleling of tuning elements on a single driver circuit results in even greater load capacitance, the driver must have a low source impedance to change the output voltage within a short time. Note that the filter changes frequencies as soon as the bias voltage changes, but the transition from +1 volt to +900 volts is required to obtain full rated power operation and optimum IMD performance. Therefore, actual filter center frequency switching occurs before full settling because of the charging time for the feedthrough capacitors.

A second factor limiting the attainable switching speed of the filter is the minority carrier lifetime of the PIN diodes used. Because of the operating physics of the PIN diodes related to charge storage within the diode intrinsic region, a delay occurs in switching from the forward bias condition to the reverse biased state. The charge storage phenomena causes the diode to continue conducting after the reverse bias is applied until the minority carriers are stripped from the

[5]M.A.Harris, "Transmitter Hopping Notch Filter", Final Technical Report, Contract F30602-79-C-0015, March 1980.

intrinsic region. This delay is characterized by the lifetime, which is approximately 20 microseconds for the diodes used in the electronically tuned filter pair. The PIN diode driver circuit must be capable of driving current into essentially a short circuit when applying reverse bias to switch the diode at the lifetime rating of the diode. The use of shorter lifetime diodes to improve switching speed is not feasible because the lifetime also effects the RF power handling and RF ON resistance of the diode.

The PIN diode driver is essentially an active pull-up, active pull-down circuit to drive the diodes from a low impedance source. Sequential logic circuits control and time the switching transitions to provide compatibility with the PIN diode and drive circuit charge storage characteristics. The change made to the original circuit involves the pull-down (forward-bias) transistors. The new circuit uses a constant current pull-down circuit to set the diode current. Previously, external power resistors were used with a saturated transistor switch. The modified circuit transfers the dissipation of the excess bias source voltage from the resistors in series with the PIN diodes to the pull-down transistors. This change allows the transistor heat sink to dissipate the excess power, permits the bias to be accurately controlled, provides some regulation of the forward bias source (which can reduce power supply contributed spurious signals present in the filter output), and increases the voltage range of the forward bias supply.

A schematic of the modified PIN diode driver circuit is shown in Figure 2.11. Bias for the pull-up transistor (Q1) to reverse bias the diodes is developed by transformer coupling

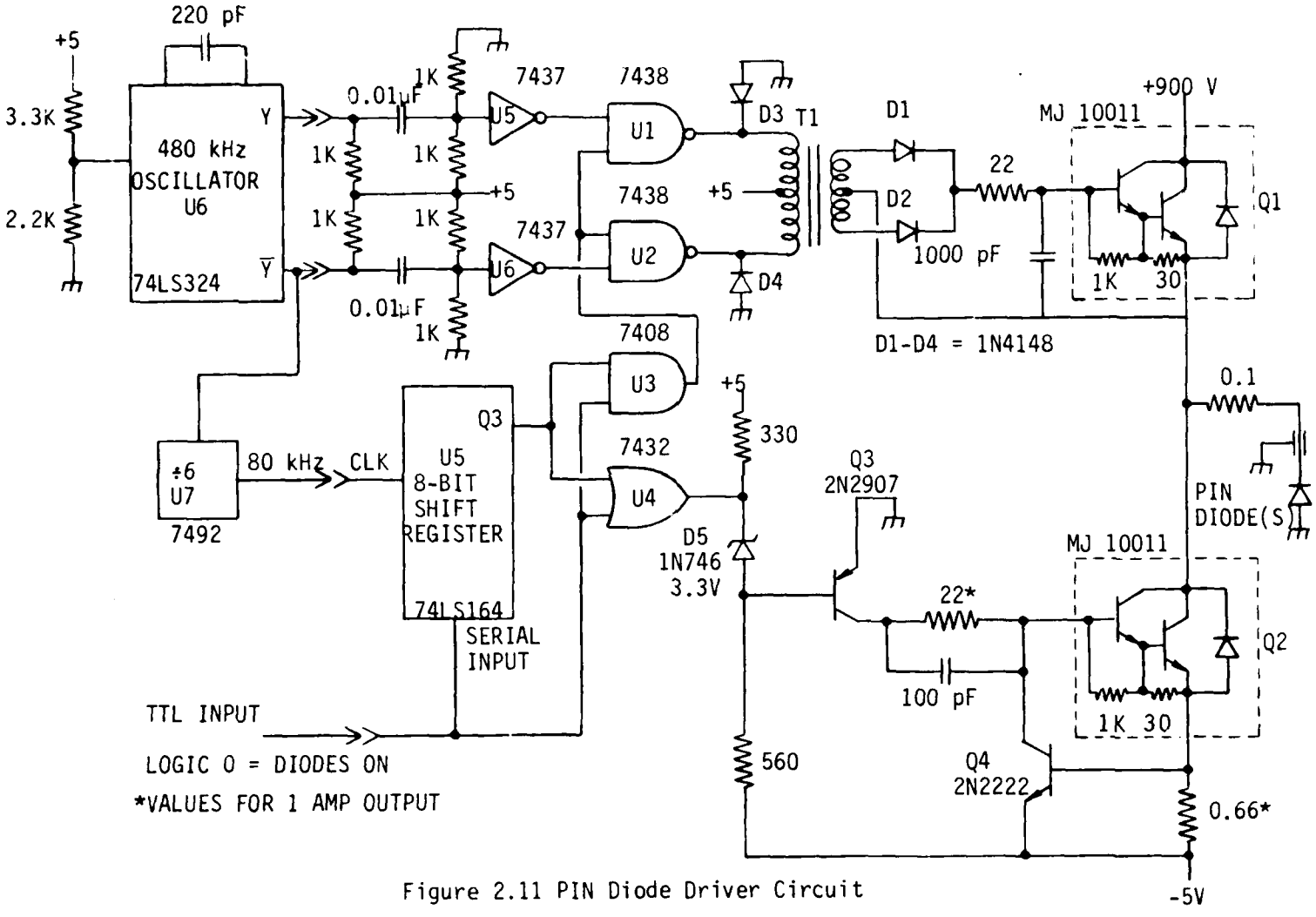


Figure 2.11 PIN Diode Driver Circuit

a 480 kHz signal through gates U1 and U2 when enabled by the output of U3. Diode forward bias is enabled via U4, Q2, Q3, and Q4. To avoid problems of power supplies being shorted together because of simultaneous conduction of the output transistors, Q1 and Q2, a sequential control circuit is used to operate the PIN diode driver. Each driver circuit contains a timing shift register, U5, and control/driver gates U3 and U4.

The circuit operates as follows for an OFF to ON transition. Before the input changes, the Q3 output of U5 and the outputs of U3 and U4 are high. Therefore, Q1 is enabled and Q2 and Q3 are disabled, biasing the PIN diode OFF. When the input changes from a logic high to a logic low, the output of U3 immediately changes states, disabling the base drive and turning OFF Q1. After four complete clock periods of U5 output, the Q3 output of U5 changes to a logic low, and the output of U4 also now changes to a logic low. The four clock periods (at 12.5 microseconds each) permits the high voltage transistor to turn completely OFF before bias is applied to Q2. The high voltage transistors (Q1 and Q2) are Darlington devices (DC beta of 50) with BV_{CEX} ratings of 1400 volts and have relatively high charge storage and thus slow switching times, necessitating the delay.

As the output of U4 changes to a logic low, Q3 is biased ON through a level translator formed from D5 and the 330 and 560 ohm resistors. This results in Q2 being turned ON, forward biasing the PIN diode load. Transistors Q2 and Q4 are connected in a current regulator configuration to set the output current at the desired value. As the load current increases, the voltage across the emitter resistance of Q2 increases until Q3 is forward biased, resulting in the reduction of the base drive of Q2 and regulation of the output current at this point.

An ON to OFF transition occurs as follows. Before the input changes from low to high, the Q3 output of U5, and the outputs of U3 and U4 are logic lows. This results in Q1 being biased OFF, and Q2 is biased ON. At the receipt of the input change, U4 immediately changes state, turning Q2 OFF. After four clock periods, the output of U3 goes high, enabling the 480 kHz oscillator to drive T1. The detected output quickly turns ON Q1 because of the short time constant filter (22 ohms and 1000 pF) and the small base current required (total output static OFF current is less than 50 microamps, worst case).

A common buffered, 480 kHz TTL oscillator and divide-by-six counter are mounted on the control circuit board for the PIN diode driver oscillator and timing signals. The resistor-capacitor oscillator coupling network as shown in Figure 2.11 is used to insure that the transformer drivers U1 and U2 return to a protected state (outputs high) if the oscillator fails. The divide-by-six counter (U7) provides the clock signal to the PIN diode driver timing shift register (U5).

Each PIN driver circuit is repeated four times on a 3.2 by 12 inch printed circuit board. The output transistors are mounted to a heat sink plate and connected to sockets soldered in the PCB to form a sandwich. For the input filter, four of the PCB's are mounted in parallel within a blower cooled enclosure which also contains the frequency control interface and the common components for the driver circuits. The output filter uses the same basic hardware, but only two PCB's are used. Common circuits to the driver boards are repeated in each filter control unit so that each filter may be operated separately.

2.3.3 Filter Primary Power Requirements

As described, the filters require DC primary power sources to provide bias for the PIN diodes in the filter tuning networks and to power the diode driver control circuits and frequency control circuits. The total maximum forward bias current required for both filters is 26 amps. Since the PIN diodes have approximately a 1 volt drop, the control power is 26 watts. Reverse bias current in a static condition is less than 310 microamps from the 900 volt supply. However, a 5 volt supply is required for diode forward bias to allow for switch losses and to improve the supply regulation and efficiency. This increases the total worst case (all diodes ON) power requirement to 130 watts. Also, the reverse bias current increases when switching the filter because the feedthrough capacitors must be charged over a 900 volt swing. Total average reverse bias current is approximately 25 milliamps when hopping at 200 hops per second, resulting in a power requirement of 22.5 watts. A 5 volt logic supply at 3 amps is required for the control logic circuits. Finally, a 115 VAC, 60 Hz supply is required to operate the four cooling blowers (one for each filter cavity and two for the PIN diode driver circuits). The power requirements are summarized in Table 2.2. Standard binding posts are proviced for the DC inputs, and separate grounds are used for each voltage. A standard three prong grounded line cord is used on each filter to provide the blower power.

Table 2.2 Filter Power Requirements

Voltage (Volts)	Current (Amps) (Max.)	Power (Watts)(Max.)
+5.0 $\pm$0.25	3.0	15
+900 $\pm$25	0.025	22.5
-5.0 $\pm$0.5	30	150
115 VAC, 60 Hz	1.35	155

Protection circuits are used on the primary supply inputs to avoid damage from incorrect application of the supply voltages. The two 5-volt supplies are clamped with 6.8 V zener diodes and protected with input fuses, and a series diode is used in the 900 volt line to prevent damage from reverse polarity sources. Testing has shown that the PIN diode driver circuits are especially sensitive to variations in the +5 volt logic supply. The power source must contain sufficient capacitance to permit the peak currents required during switching to be supplied without causing the voltage to drop out-of-range. If the logic supply is not within the 0.25 volt tolerance, intermittent operation and conditions where both the pull-up and pull-down transistors are conducting simultaneously have been noted.

3.0 TEST RESULTS

Testing of the electronically tuned filter pair has fallen into two major categories. First, during the assembly and initial alignment of each filter, tests were made to verify performance and check design parameters. As mentioned previously in this report, the projected unloaded Q was not obtained in the initial filter tests. The results of these initial tests and the additional studies made to determine the cause of the loss problem are described in this section. Finally, performance verification tests on each of the completed filters to measure the operation with respect to the performance goals and requirements was performed.

3.1 Filter Cavity Loss Investigation

The key parameter describing the performance of the electronically tuned filter with respect to the design objectives is unloaded Q. In general, tuning range, speed, and resolution and mechanically oriented parameters are easily achieved. However, the unloaded Q obtained at various stages of the completion of the filter directly impacts the bandwidth, passband shape, insertion loss, and power handling capability. Projections of unloaded Q are made during the initial design of each filter based on similar filter results and measurements previously made on tuning network components. Because many minor implementation factors can have a significant effect on the actual unloaded Q obtained, tests are made on each filter to check the results against the projections made.

The initial test performed on each filter was to measure the unloaded Q of the cavity without tuning networks or other components installed. The only added component is a tuning slug air dielectric capacitor used to tune the resonant frequency of

the filter to approximately 400 MHz. Therefore, the Q measurements contain two loss elements, the cavity itself and the tuning slug. For the input filter, an unloaded Q of 2600 was measured compared with an initial projection of 3000. Considering the capacitor loss, agreement with the projection is reasonable. However, the input filter was deliberately designed to obtain a high unloaded Q by using a large cavity volume compared with previously designed filters, while doubling the volume resulted in essentially no improvement. Although the smaller, previously designed filter was totally silver plated and the input filter used in this effort only contained silver plated resonators, a significant increase in unloaded Q was expected from the volume change. The measured unloaded Q for the output resonator was 2200 compared with a projection of 2800. Again, the effect of the tuning slug may cause some of the degradation measured, and the use of silver plating in the output resonator could raise the measured unloaded Q. Since the cavity-only unloaded Q measurements were significantly greater than the projected unloaded Q with the tuning elements installed, construction of the filters was completed without additional plating or surface-finish operations.

In the initial implementation of the filter tuning networks, toroidal chokes set to be parallel resonant at mid-band were used to decouple the PIN diodes from the bias source. Since the loss of the choke is directly in parallel with the diode OFF resistance, a high Q decoupling network is required. At initial turn-on of the input filter, an insertion loss of over 10 dB was noted, with tuning codes at the high end of the band having greater loss than codes tuning to the 350 MHz region. This loss component was immediately isolated to the decoupling coils, which were replaced with standard molded RF chokes. Losses for

the input filter then dropped to the 3 to 4 dB range. An attempt was made to then replace the molded chokes with air-wound coils, but the increased stray capacitance caused the upper end of the tuning range to not be obtained, even by re-tuning the fixed capacitor, in the input filter. The air-wound coils were used in the output resonator, and they resulted in an additional 0.5 to 1 dB reduction in insertion loss compared with the molded chokes.

After resolving the problems with the bias decoupling networks, initial data was taken on each of the completed filters at several frequencies across the 350 to 400 MHz band to check tuning range, coupling factors, and insertion loss performance. The input filter tuned the full frequency range with the high resolution expected from the tuning bits added to obtain tracking capability. Loaded Q ranged from 110 to 150 as expected, but the response was overcoupled as evidenced by a just noticeable to 0.5 dB passband ripple and a 3:1 peak input VSWR. Insertion loss was also high, ranging from 3.7 to 4.5 dB corresponding to an unloaded Q of approximately 450. The performance of the output resonator was similar to the input filter. The full tuning range was covered with approximately 1.8 MHz resolution as expected. The loaded Q ranged from 80 to 104 with the coupling loops as originally installed. Insertion loss ranged from 1.6 dB at 400 MHz to 3.1 dB at 350 MHz, which is much greater than expected. The corresponding unloaded Q ranged from 350 to 475, compared with original projections of over 1100. As expected from the "blocking" effect of the large diameter center conductor preventing cross-talk between the input and output coupling loops, an ultimate rejection of over 30 dB was obtained.

Because the basic loss characteristics of both the input filter and output resonator were the same, the output resonator was used for additional tests to isolate the problem since modifications were simpler on the one pole filter. Both filters had an equivalent characteristic of having greater losses at the low frequency end of the tuning range, when the tuning code has PIN diodes primarily turned ON. Although the position of the tuning network in the output filter causes the series equivalent resistance of ON bits to have greater effect on losses than OFF bits, the duplication of the loss curve in the input filter indicates a basic problem with the ON resistance of the tuning network. The first change attempted was to halve the diode ON resistance by doubling the bias current. This change had no measurable effect on filter loss indicating that the loss was significant compared to the diode ON resistance, estimated to be approximately 0.03 ohms.

Since the PIN diode losses apparently were not limiting the tuning network unloaded Q, the only remaining lumped element affecting ON resistance is the tuning capacitors. Separate tests were made on several capacitor values in a notch filter cavity to measure the unloaded Q of the ceramic dielectric capacitor. In all cases, the measured unloaded Q exceeded the value used when the filters were designed. The only difference between the measurement technique and the actual capacitor mounting technique used in the filter is that the capacitors are mechanically secured between two plates and pressure applied in the notch filter test fixture, while the capacitor is soldered into the bandpass filters of the electronically tunable amplifier. Therefore, the solder used could be increasing the capacitor plate surface resistivity and degrading unloaded Q.

Since no other method was easily available to mount the capacitors, and since the only remaining elements which could contribute to the problem are silver ribbon leads, solder connections, and contact surface resistance, modifications to the filter bandwidths were made to reduce losses.

For the EMC problem as identified in Section 1, the primary reduction in amplifier noise takes place in the narrow bandwidth two pole input filter. Therefore, the input filter coupling was modified to improve the overcoupled response and minimize the increase in bandwidth while reducing the insertion loss to below 3 dB to insure that the power handling requirement of 100 watts would be met.

As previously mentioned, the input filter was modified from the original design by changing the input transformer width and the coupling to the resonators, and by adding a coupling loop between resonators to widen the bandwidth slightly. Loaded Q was decreased to between approximately 100 and 125, and the coupling and input match were significantly improved.

The primary objective in modifying the output resonator was to insure the capability of handling a 1000 watt input. Although it is desirable to minimize the bandwidth of the output filter to improve antenna conducted intermodulation distortion performance, the problems of handling the power losses in the narrow bandwidth filter as initially achieved were addressed by reducing the loaded Q until an insertion loss of 1 dB maximum was obtained at the high frequency end of the band. This modification, made by reducing the area of the coupling loops, resulted in a final loaded Q ranging from approximately 40 to 55.

During the final testing of the output filter, one final factor impacting the unloaded Q problems noted during the initial testing was discovered. At full rated input power, the dielectric in certain tuning capacitors failed at RF current levels much below the expected capability of the parts. Dielectric losses in the capacitors at UHF frequencies were believed to be negligable. However, failure of the capacitors from RF current (not voltage breakdown) indicates that the capacitors are a significant contributor to the filter loss and that dielectric losses are not an insignificant element of the capacitor unloaded Q.

3.2 Final Filter Performance Testing

The final testing program performed on the electronically tuned filter pair consisted of an overall performance test to measure the characteristics of each filter against the requirements and goals of the statement of work. In general, each test performed is described and the results presented in graphs and Tables in the following sections. Testing was performed using low level signal sources and detectors, with high power testing performed to verify that the results were applicable at full rated power. EMC performance related tests were also performed at high RF power levels.

Through the remainder of this section, the test procedures described will refer to a unit-under-test (UUT). This description is intended to refer to either the input or output filter and the support equipment necessary for operation as shown in Figure 3.1. For tests where both filters are used, the power supply inputs are paralleled and a frequency control jumper cable added between filters. All tests are performed under room ambient conditions.

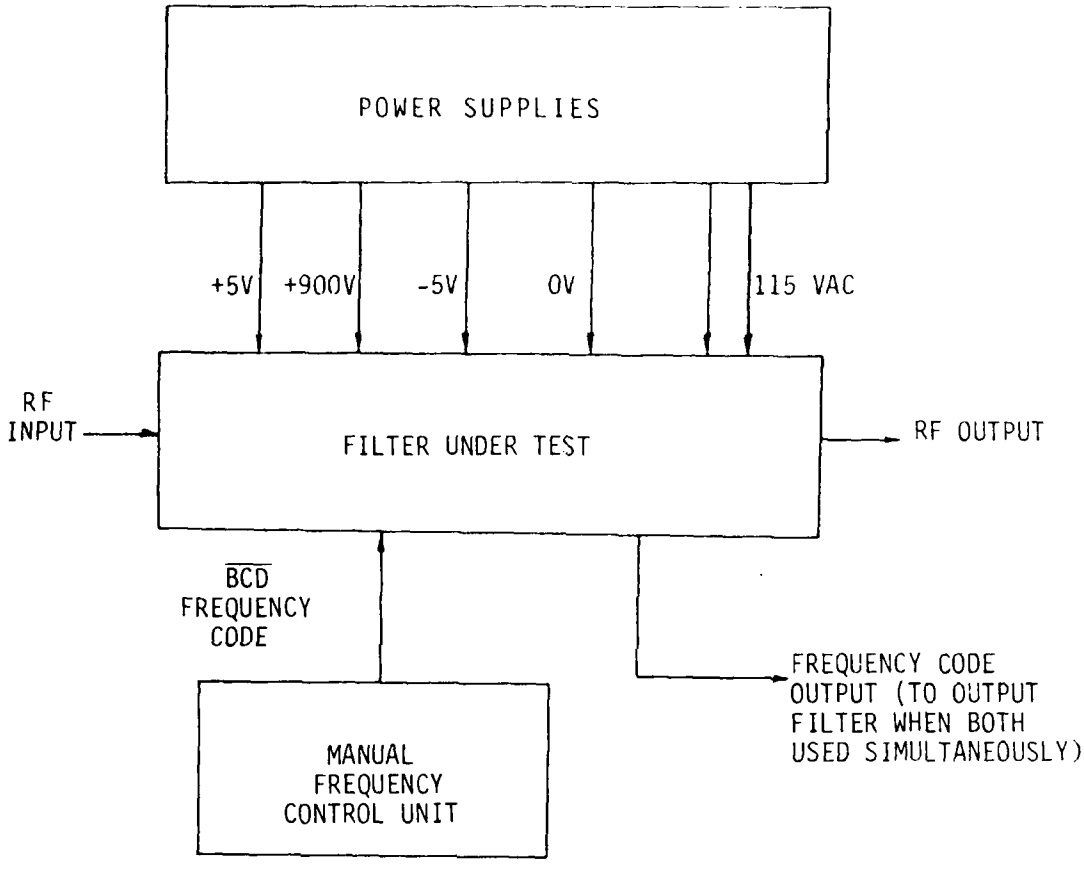


Figure 3.1 Basic Unit-Under Test

3.2.1 Filter Bandpass Response Characteristics.

The primary characterization of the response of both the input filter and output resonator of the electronically tuned filter pair was determined by a complete set of bandpass response plots. The bandpass shape and frequency response of each filter was measured using the test equipment as shown in Figure 3.2. The frequency response was determined on a point-by-point basis using a network analyzer phase-locked to a frequency synthesizer. The actual network transmission or reflection loss measured by the analyzer was transferred to the calculator, then plotted over specified frequency ranges with arbitrary plotting resolutions.

Four basic response plots were made for each tested center frequency. These plots include a high resolution plot of the operating passband of the input filter covering the center frequency (f_o) $\pm$2.5 MHz, a plot of the filter rejection generally covering f_o $\pm$25 MHz, a plot of the filter ultimate rejection over the f_o $\pm$100 MHz range, and a plot of return loss within the f_o $\pm$2.5 MHz filter passband. For the output filter similar plots were made except that the passband was plotted over a f_o $\pm$5 MHz range because of the wider filter bandwidth.

From the resulting frequency plots, tuning range, input impedance (VSWR), loaded Q, bandwidth, and insertion loss were determined using the frequency response definitions shown in Figure 3.3. Tuning interval was determined by tuning the filter under test to its highest frequency, then decreasing the frequency control input until the filter frequency actually changed. The difference between the actual measured center frequencies was recorded as the tuning interval. This procedure was used because the design of the tuning networks

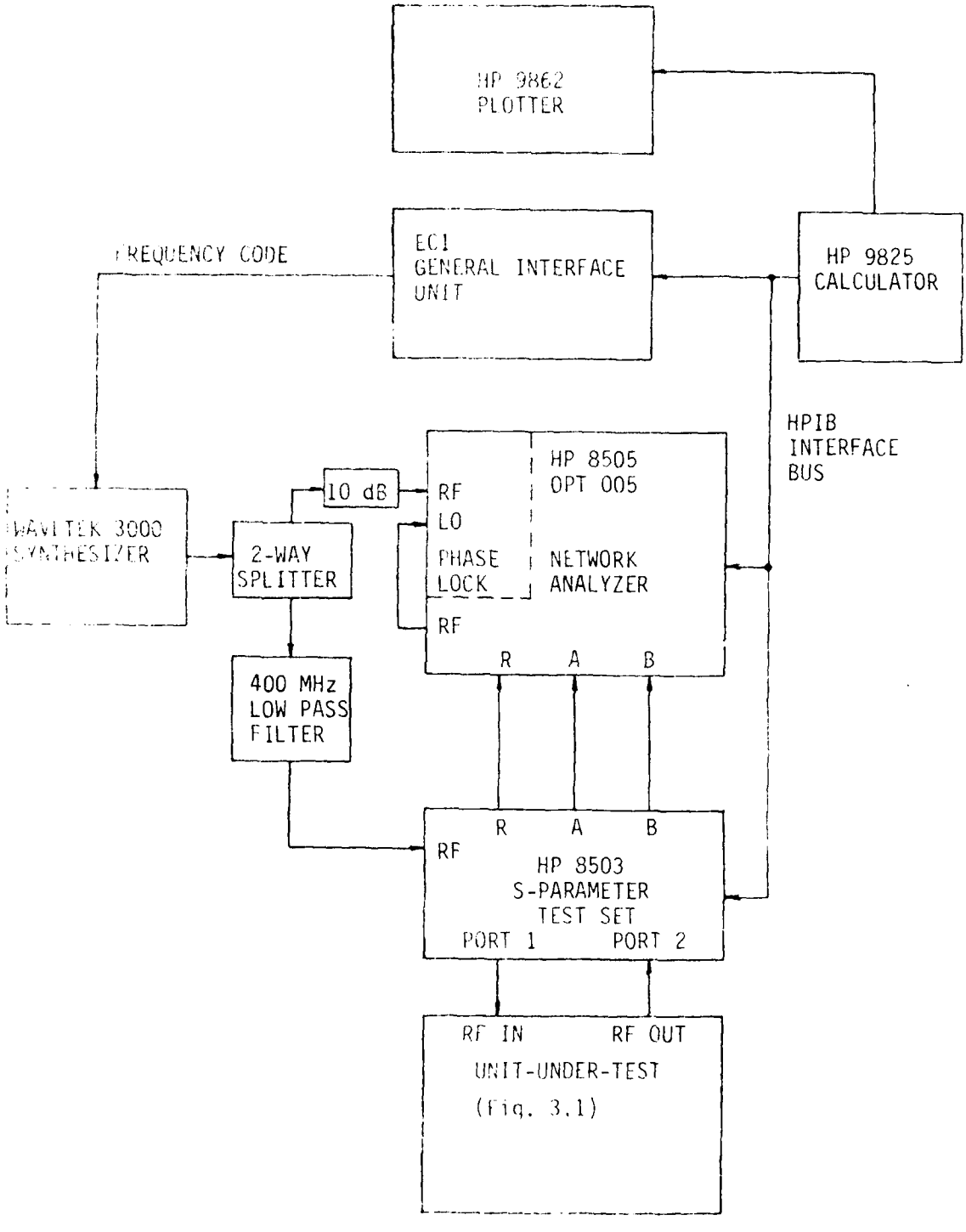
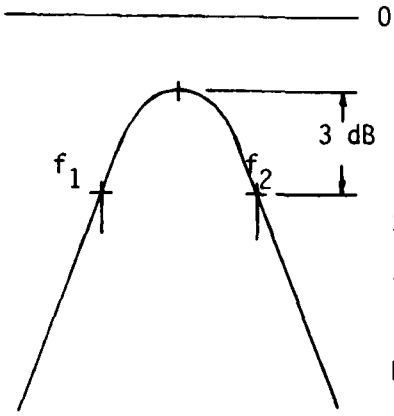


Figure 3.2 Low-Level Frequency Response Test Configuration



3 dB Bandwidth = $f_2 - f_1$

$$f_o = \frac{f_1 + f_2}{2}$$

$$\text{Loaded Q} = \frac{f_o}{f_2 - f_1}$$

VSWR - measured at f_o

$$\text{REFLECTION COEFFICIENT} = 10^{\frac{\text{RETURN LOSS (dB)}}{20}} = P$$

$$\text{VSWR} = \frac{1 + P}{1 - P}$$

Figure 3.3 Filter Bandpass Shape

results in the largest tuning increment being at the highest tuned frequency. Frequency tracking between the input and output filters was also determined by comparing the actual tuned frequencies of each filter for equivalent input codes.

3.2.1.1 Input Filter Results

The input filter response was determined at 10 MHz intervals across the 350 to 399.975 MHz tuning range and at 355 MHz. An additional test was made at the next-to-highest tuned frequency to determine tuning interval as described in Paragraph 3.2.1. The tabulated results of the low-level input filter tests are listed in Table 3.1. Although response plots were made at each tuned frequency, the curves obtained at 350 MHz and 399.975 MHz are representative of the filter response across the frequency band and are included in this report. Figures 3.4 through 3.7 show the input filter response at a desired frequency of 350 MHz, and Figures 3.8 through 3.11 repeat the data at 399.975 MHz.

The tuning interval as indicated in Table 3.1 is 0.470 MHz. From the data in the Table, the accuracy of center frequency tuning resulting from the added tuning bits is evident. The passband plots also show the accuracy of the frequency tracking between the resonators in the input filter by the absence of amplitude ripple in the filter passband. The filter bandwidth is higher than the design goal as set to obtain a 3 dB maximum insertion loss for power handling as was described in Paragraph 3.1. The effect of retuning the input transformers is also seen in the relatively low input VSWR achieved.

A second passband for the input filter at just above 450 MHz when the filter is tuned to 350 MHz is evident from the overall response curve of Figure 3.6. This second response is the result of interaction between the tuning network and the RF

Table 3.1 Input Filter Bandpass Characteristics

	DESIRED CENTER FREQUENCY (MHz) F_1	ACTUAL CENTER FREQUENCY (MHz) F_2	LOADED Q	BANDWIDTH (MHz)	INSERTION LOSS @ F_1 (dB)	INSERTION LOSS @ F_2 (dB)	RETURN LOSS (dB)	INPUT VSWR
1.	350	349.96	124.99	2.80	2.93	2.92	19.2	1.25
2.	360	360.05	116.15	3.10	2.60	2.60	19.5	1.24
3.	370	369.71	103.27	3.58	2.35	2.31	18.8	1.26
4.	380	380.07	102.72	3.70	2.40	2.40	20.7	1.20
5.	390	389.74	97.44	4.00	2.37	2.33	13.9	1.51
6.	399.975	400.14	106.42	3.76	2.56	2.55	14.8	1.44
7.	355	354.95	104.09	3.41	2.52	2.52	19.0	1.25
8.	f_A 399.6	399.67	105.18	3.80	2.70	2.70	12.6	1.61

Note: 1. f_A is first tuning step below 399.975 MHz

2. Refer to Figure 3.3 for definitions of data points

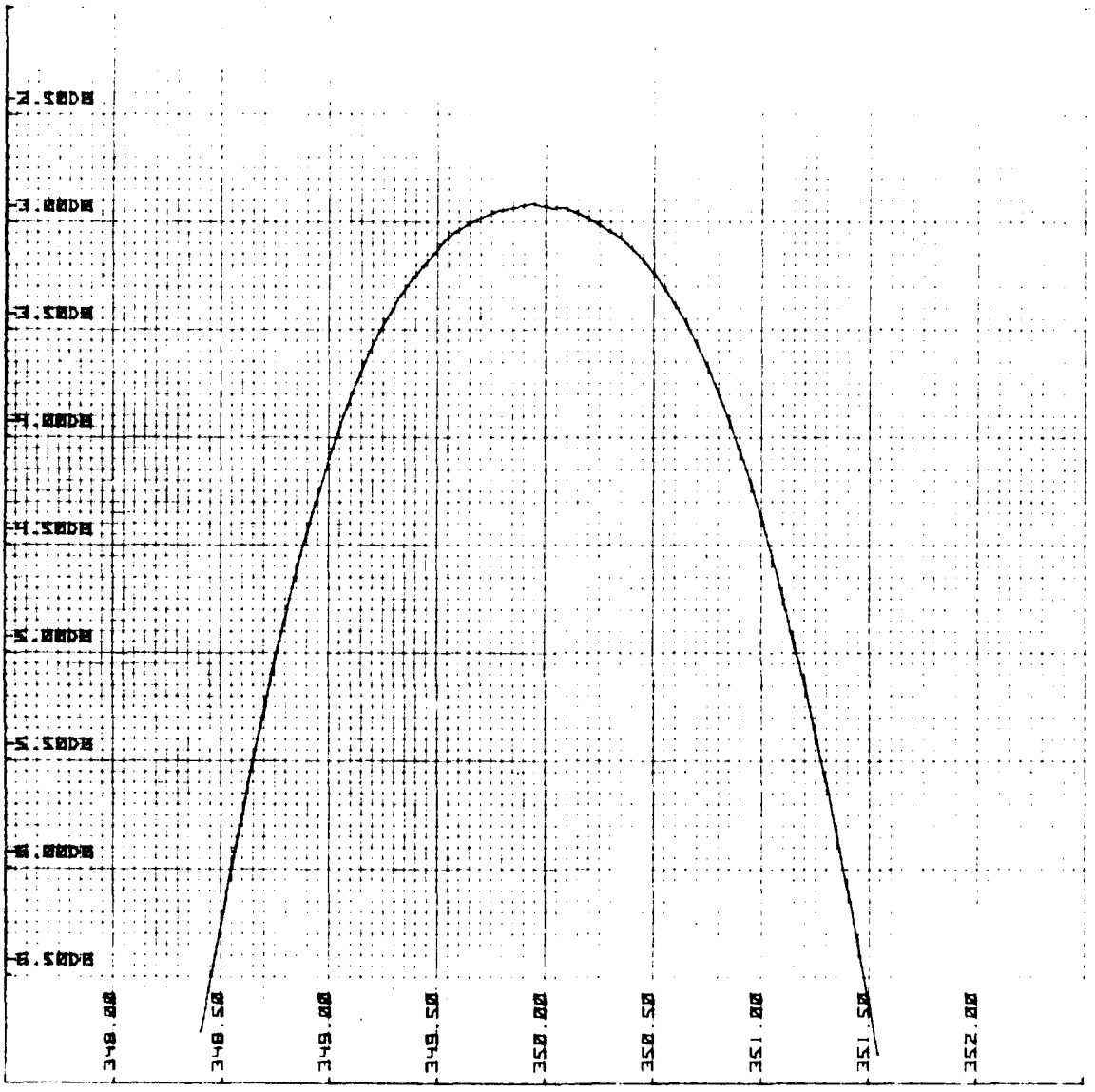


Figure 3.4 Input Filter High Resolution Bandpass Response - 350 MHz

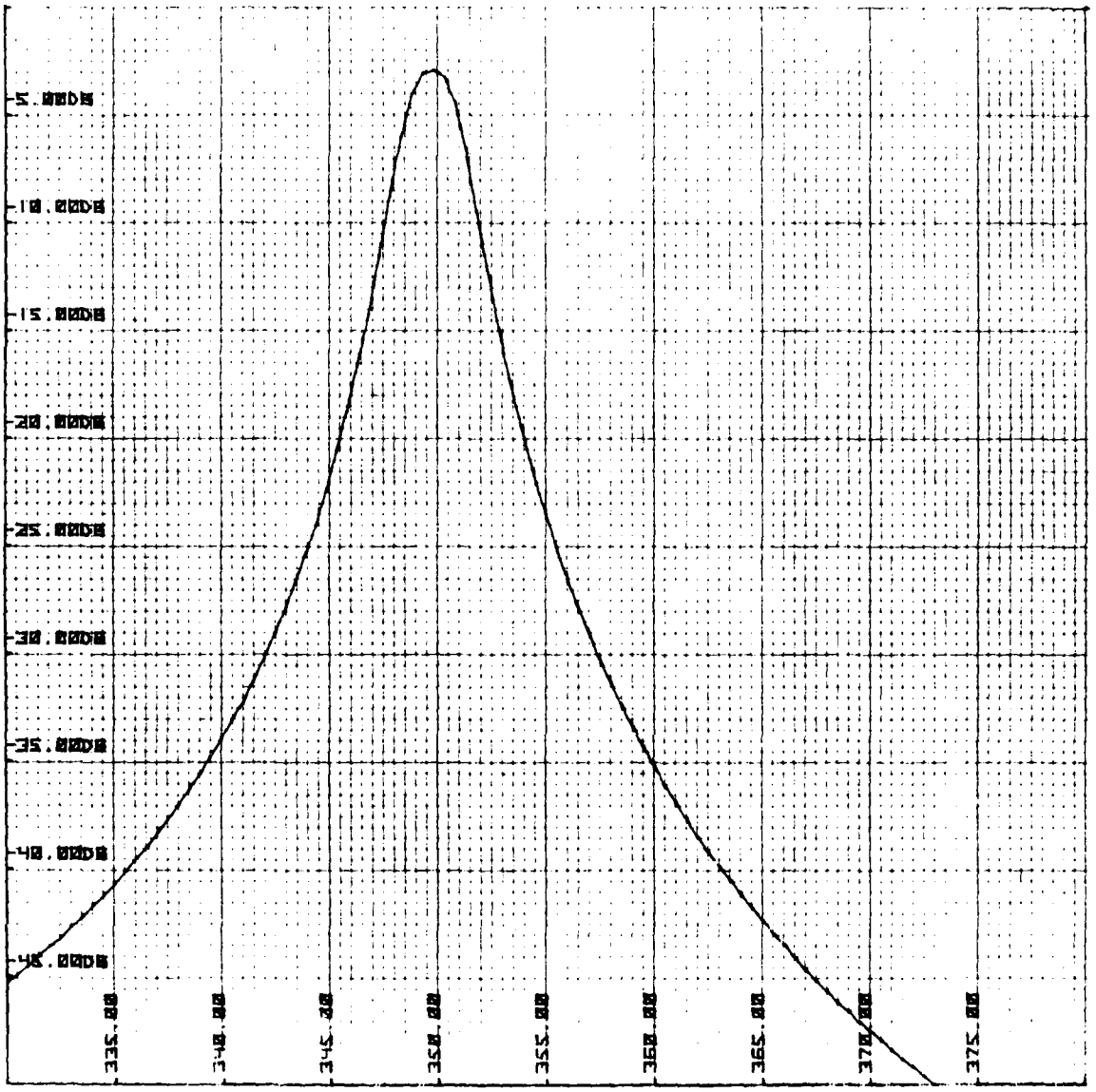


Figure 3.5 Input Filter Selectivity - 350 MHz

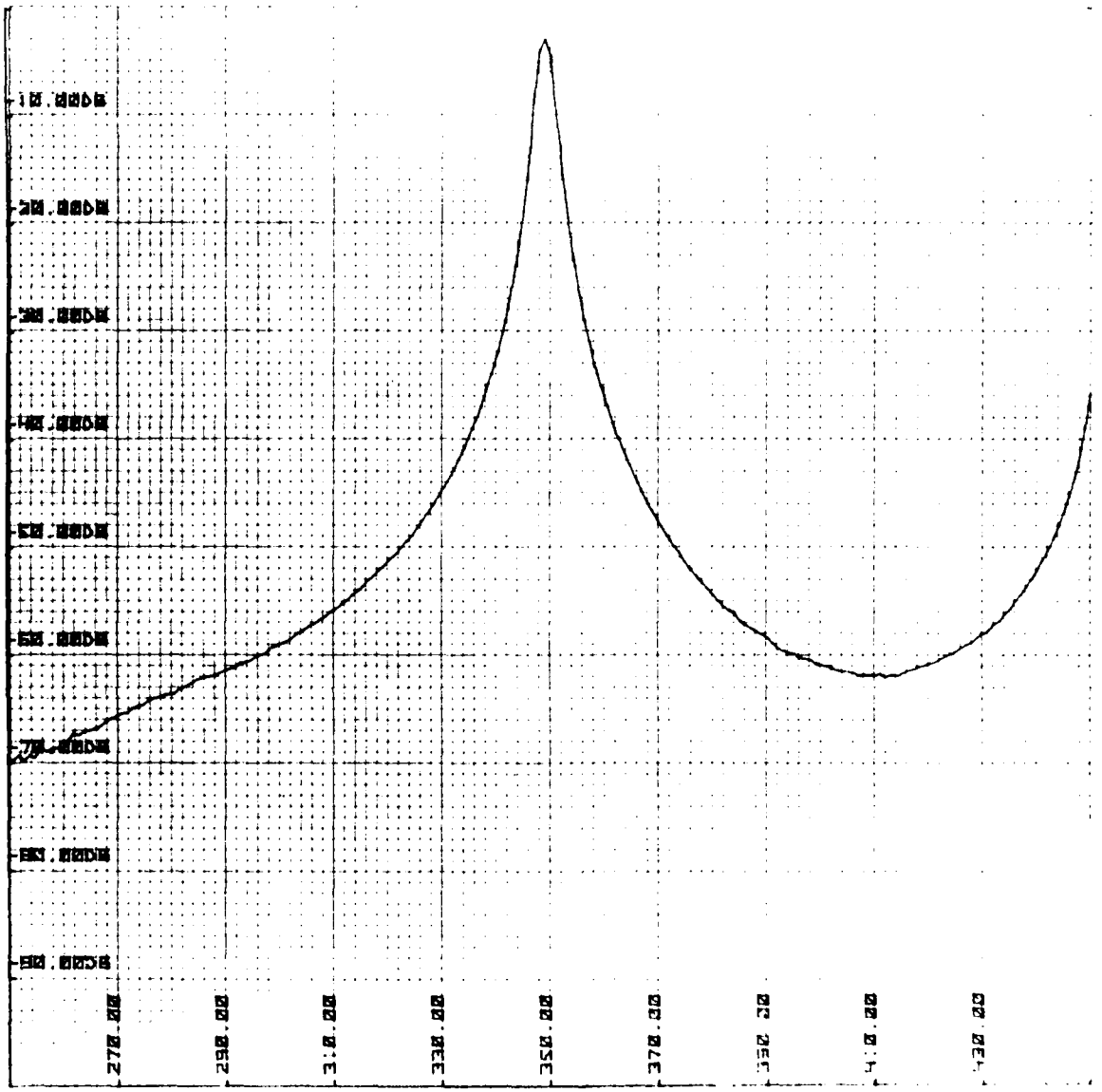


Figure 3.6 Overall Input Filter Response - 350 MHz

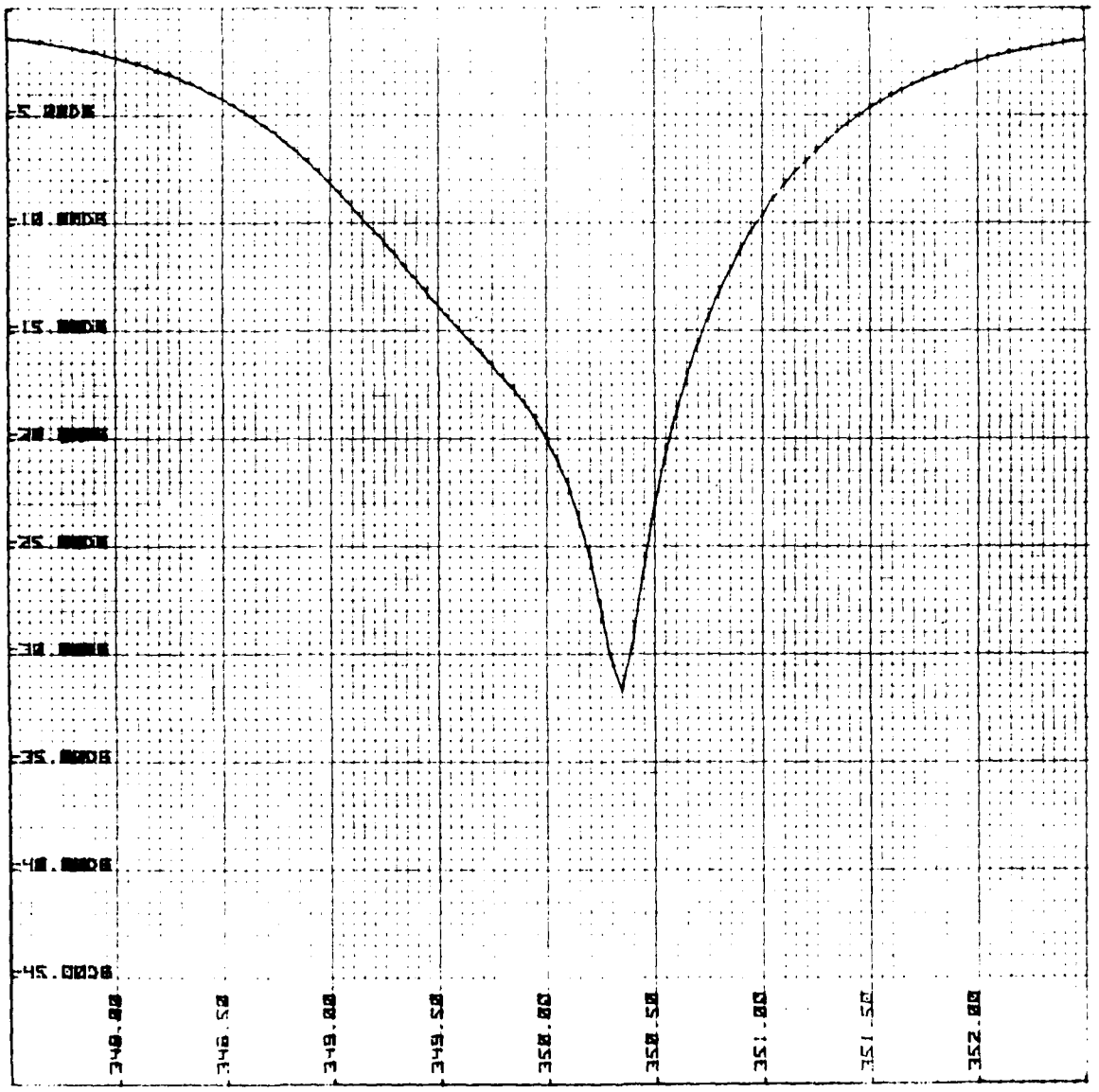


Figure 3.7 Input Filter Return Loss - 350 MHz

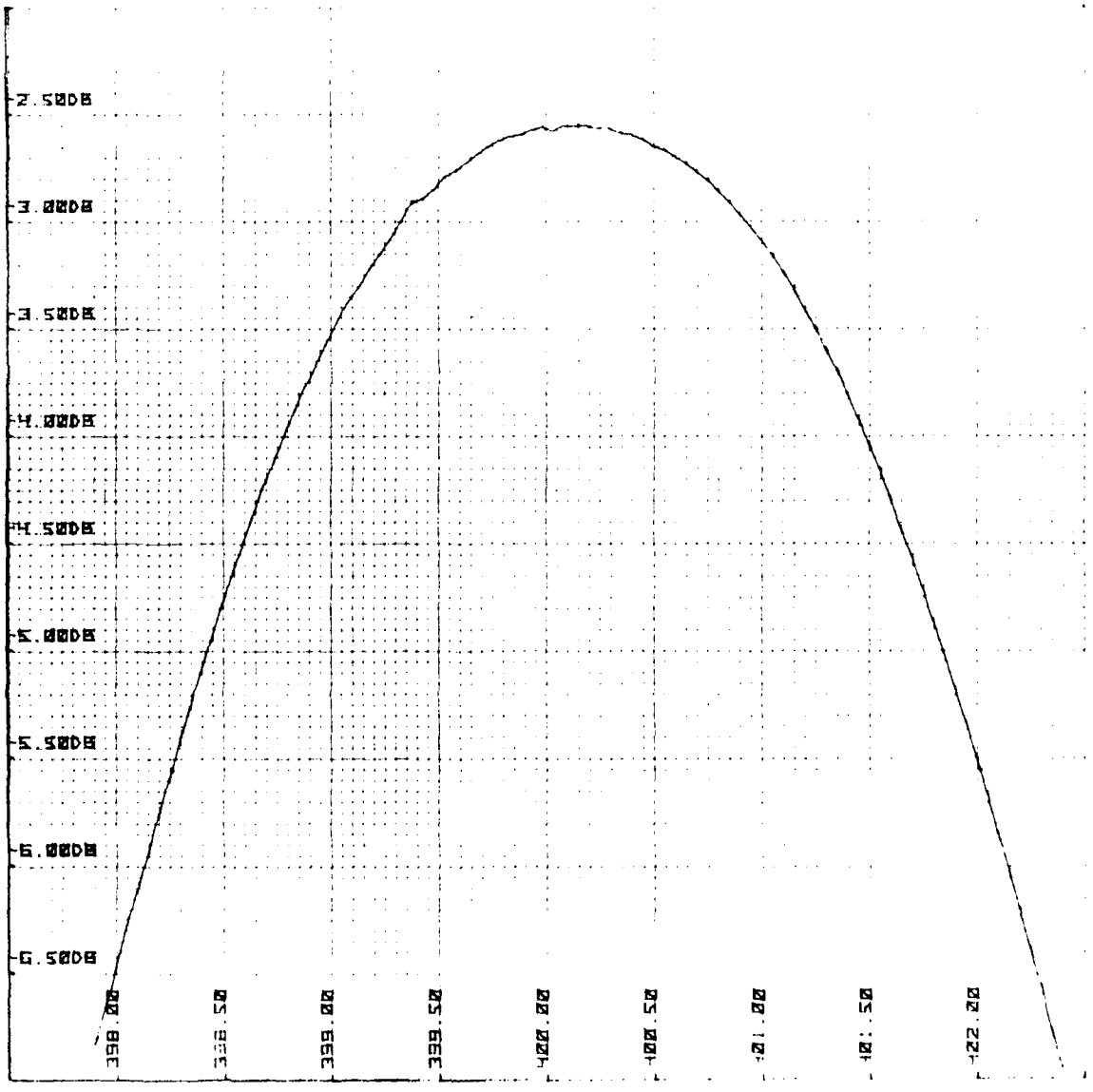


Figure 3.8 Input Filter High Resolution Bandpass Response - 399.975 MHz

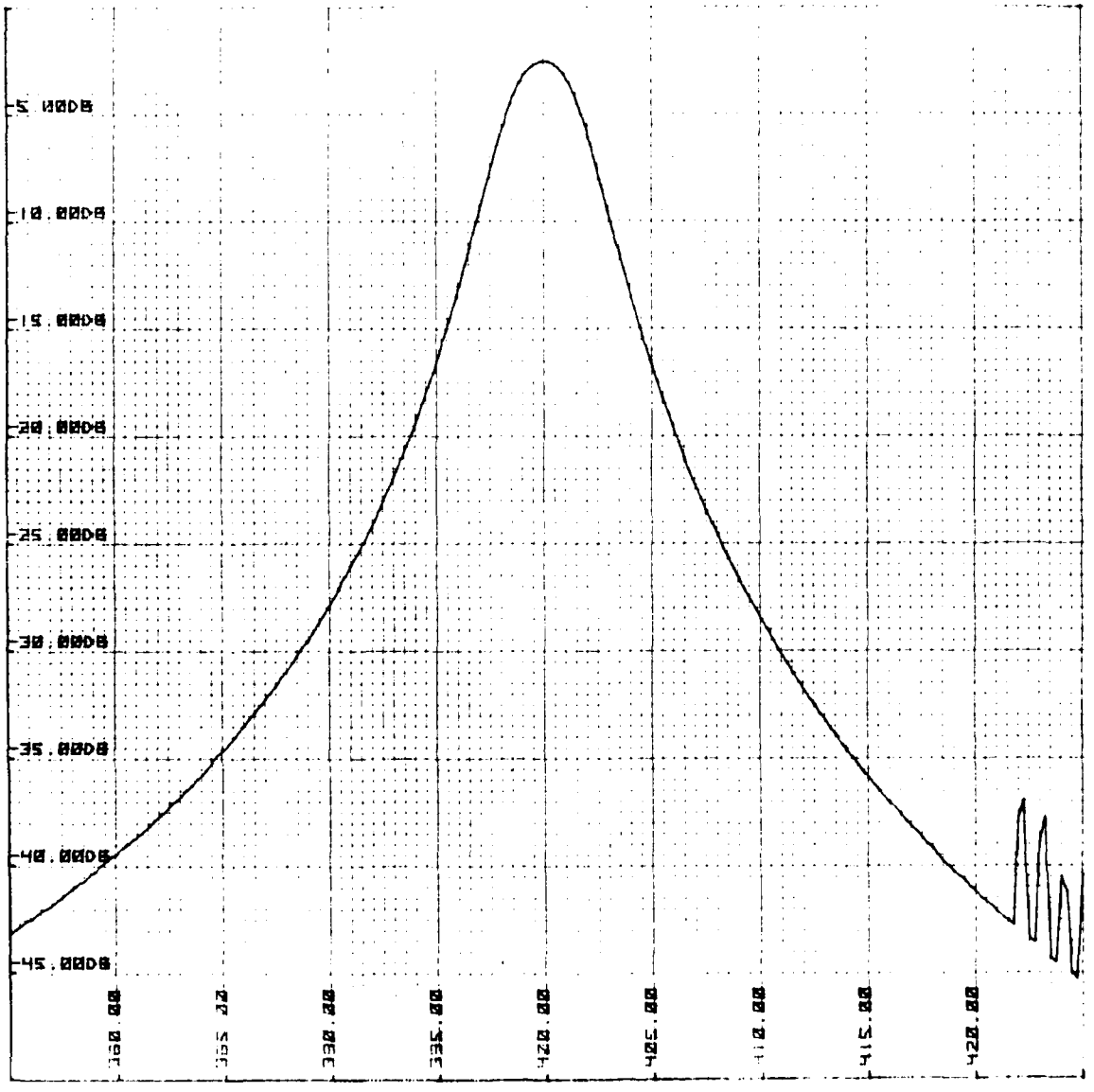


Figure 3.9 Input Filter Selectivity - 399.975 MHz

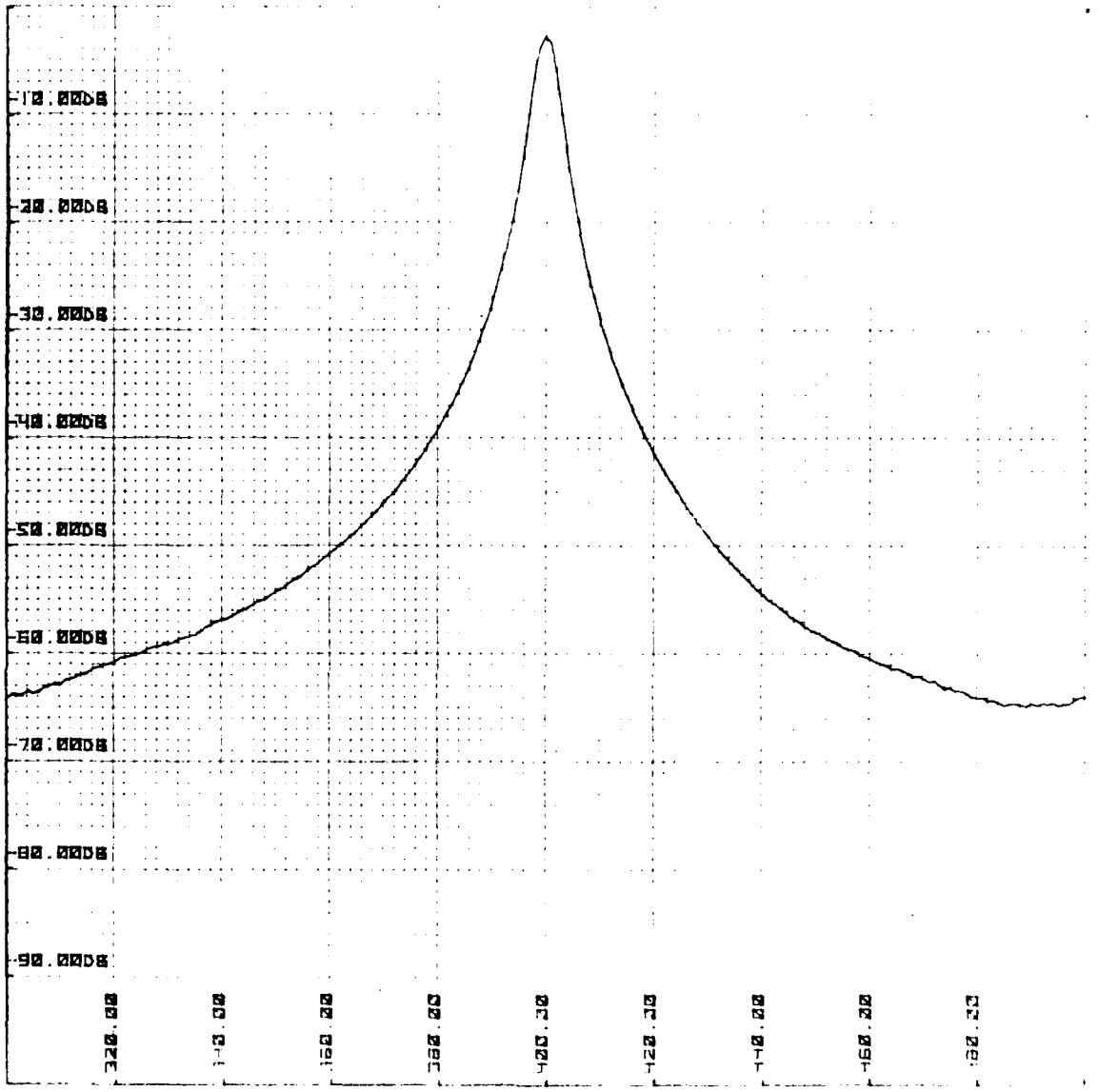


Figure 3.10 Overall Input Filter Response - 399.975 MHz

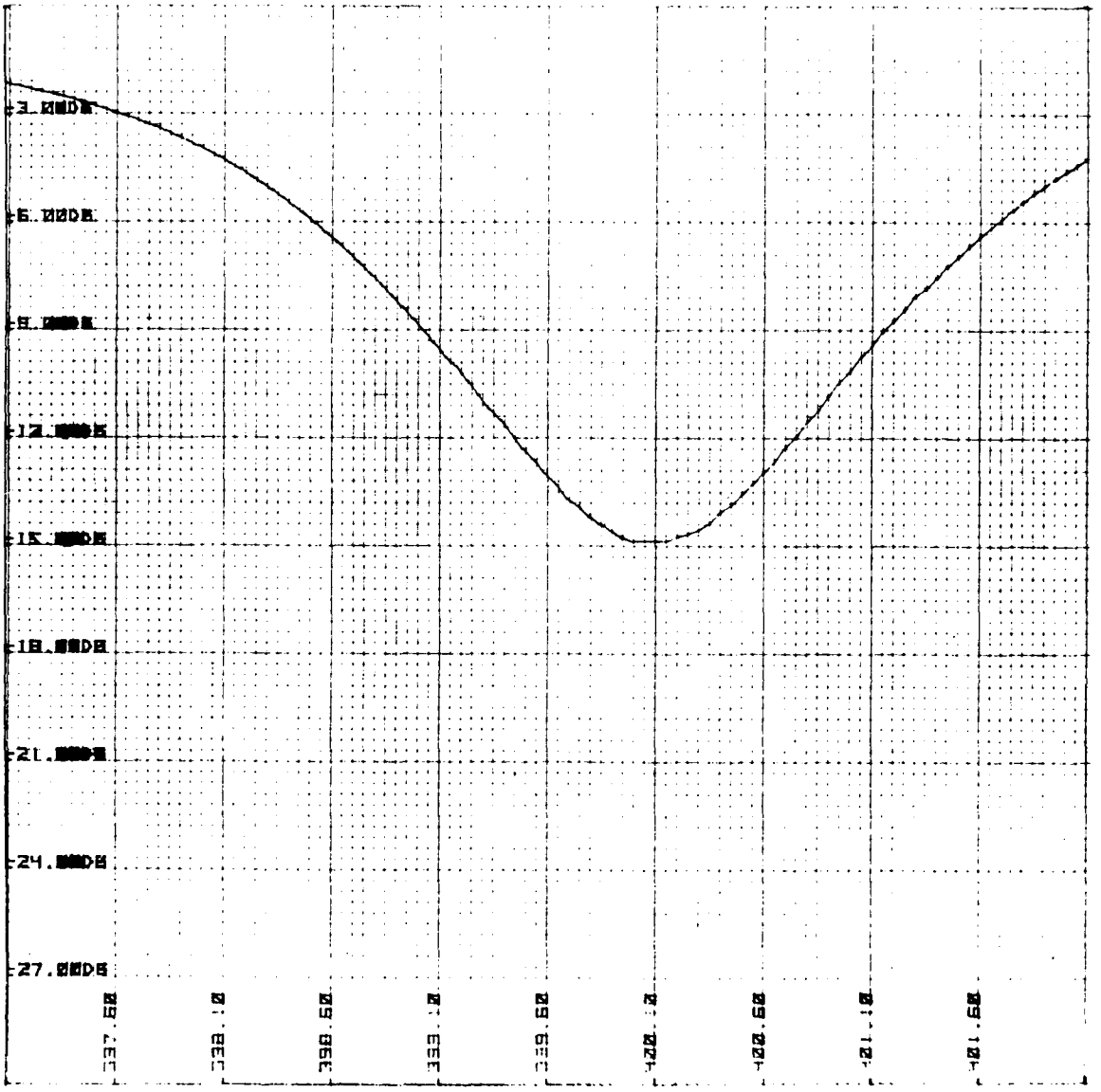


Figure 3.11 Input Filter Return Loss - 399.975 MHz

cavity. For all the frequencies tested, no second response was present within the operating frequency range of the filter. An ultimate rejection of 60 dB was typical for the input filter. Also, the spurious responses shown in Figure 3.9 are the result of the network analyzer dropping out-of-lock and are not filter responses.

3.2.1.2 Output Filter Results

The response of the output filter was measured under the same conditions as the input filter. The tabulated results of the low-level tests on the output filter are listed in Table 3.2. The response plots taken at 350 MHz and 399.975 MHz are presented in Figure 3.12 through 3.15 and 3.16 through 3.19, respectively. These plots are representative of the full sets of plots taken.

The tuning interval as indicated by the data of Table 3.2 is 0.01 MHz. However, the high apparent resolution of the tuning network is a result of using multiple individually tuned capacitor sets with equivalent capacitance values. The tuning curve is set up such that at least one tuning network path must be turned ON to reach 400 MHz. For the output filter, a sufficient difference in stray reactance was present between two equivalent value tuning elements to result in the second set being selected at 399.6 MHz. However, the true maximum tuning interval for the output filter is just under 2 MHz.

The much wider bandwidth obtained compared with the design goal of 3 MHz is shown in Table 3.2. As described in Paragraph 3.1, the bandwidth was deliberately increased to reduce insertion loss to approximately 1 dB. The final bandwidth was set to obtain the insertion loss target at the high end of the tuning range, with an increase in loss permitted at the low end

Table 3.2 Output Filter Bandpass Characteristics

	DESIRED CENTER FREQUENCY (MHz) F_1	ACTUAL CENTER FREQUENCY (MHz) F_2	LOADED Q	BANDWIDTH (MHz)	INSERTION LOSS @ F_1 (dB)	INSERTION LOSS @ F_2 (dB)	RETURN LOSS (dB)	INPUT VSWR
1.	350	350.34	38.16	9.18	1.43	1.44	20.5	1.21
2.	360	360.81	39.13	9.22	1.28	1.23	17.9	1.29
3.	370	370.10	43.54	8.50	1.29	1.30	11.5	1.73
4.	380	380.38	43.72	8.70	1.08	1.07	24.3	1.13
5.	390	389.84	49.16	7.93	1.01	0.98	14.7	1.45
5.	399.975	400.00	56.58	7.07	0.91	0.91	>30	<1.07
7.	355	355.16	43.10	8.24	1.40	1.41	14.8	1.44
8.	f_A 399.4	399.99	55.02	7.27	0.95	0.87	>30	<1.07

Note: 1. f_A is first tuning step below 399.975 MHz

2. Refer to Figure 3.3 for definitions of data points.

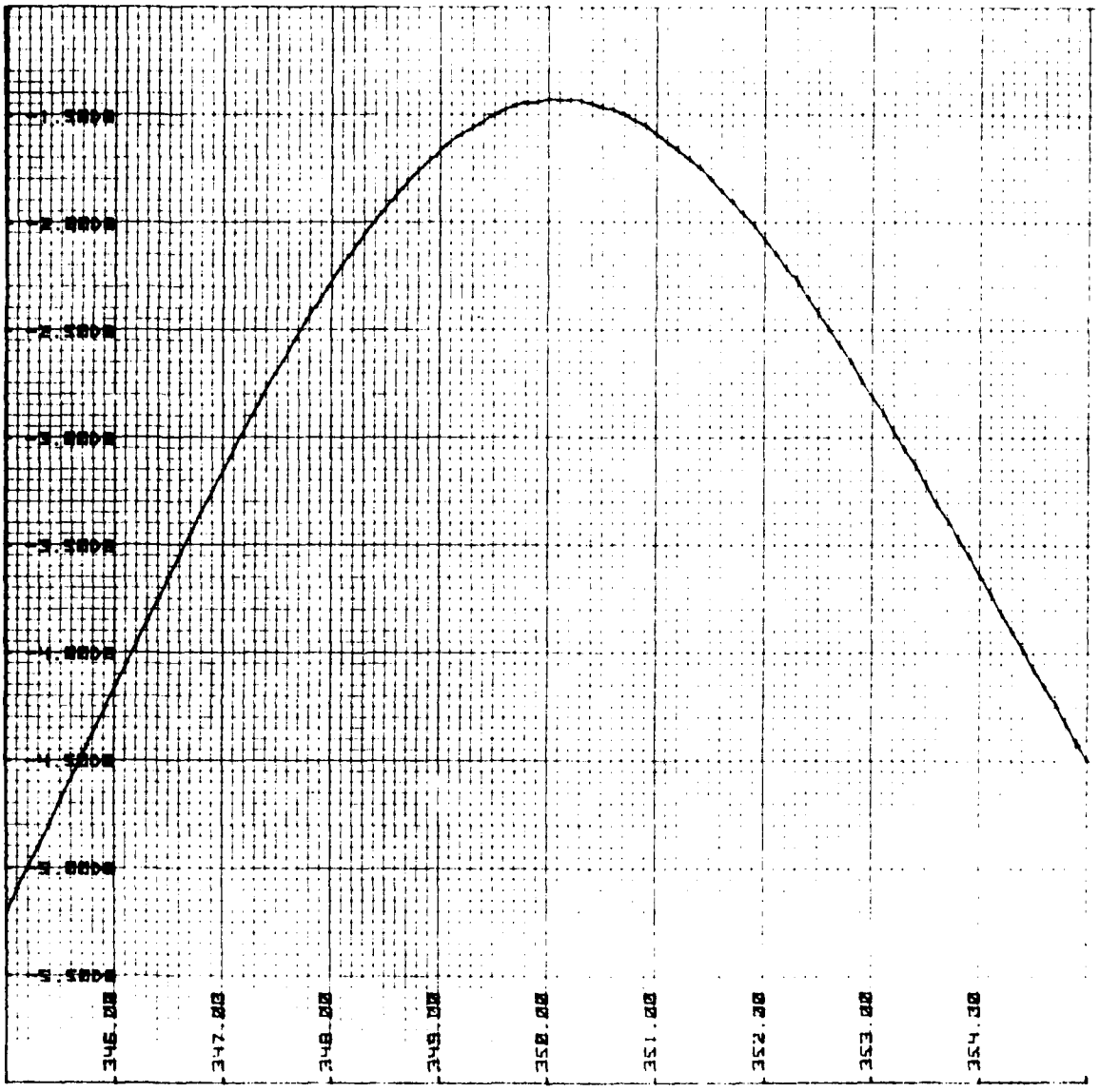


Figure 3.12 Output Filter High Resolution Bandpass Response - 350 MHz

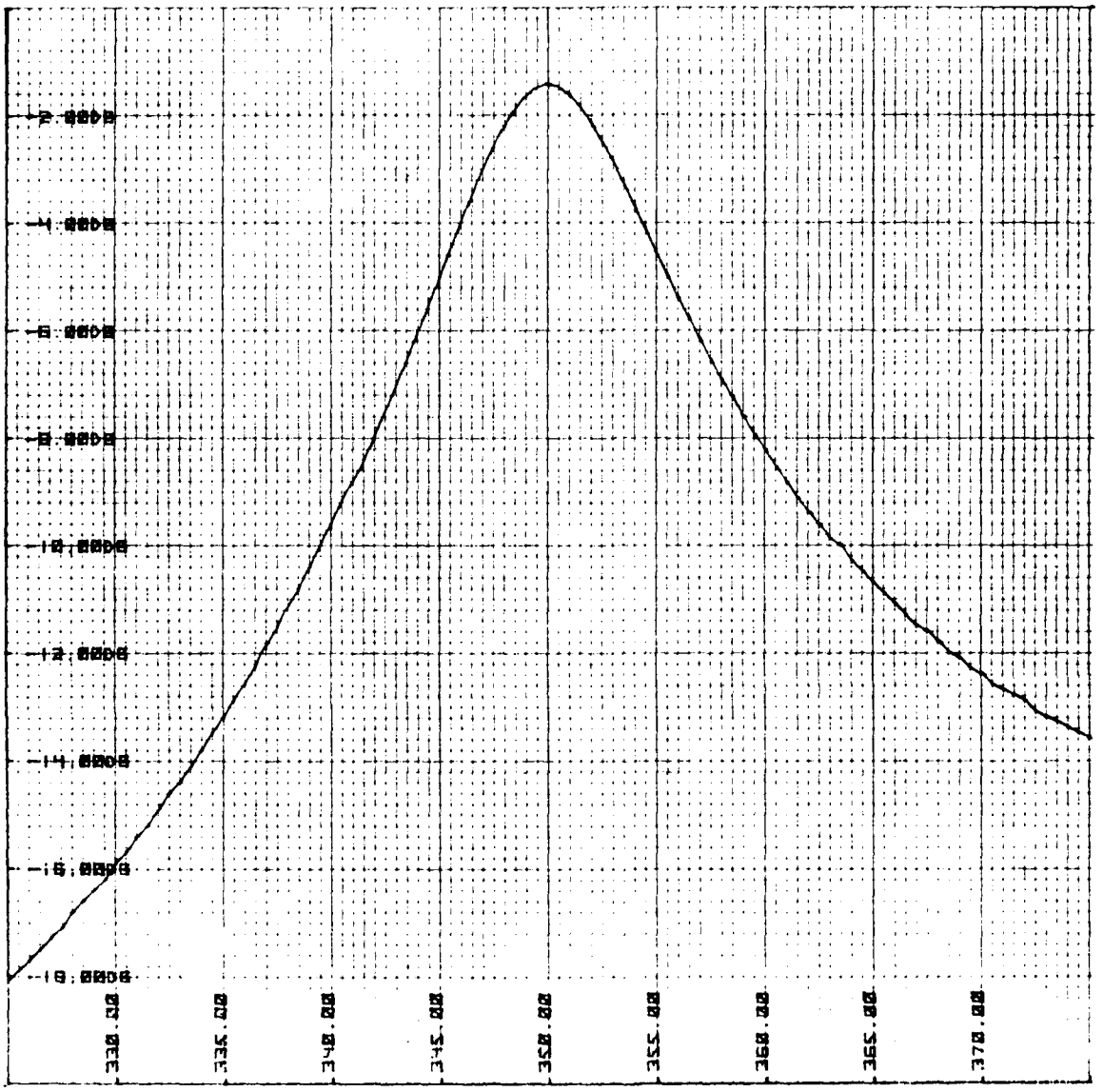


Figure 3.13 Output Filter Selectivity - 350 MHz

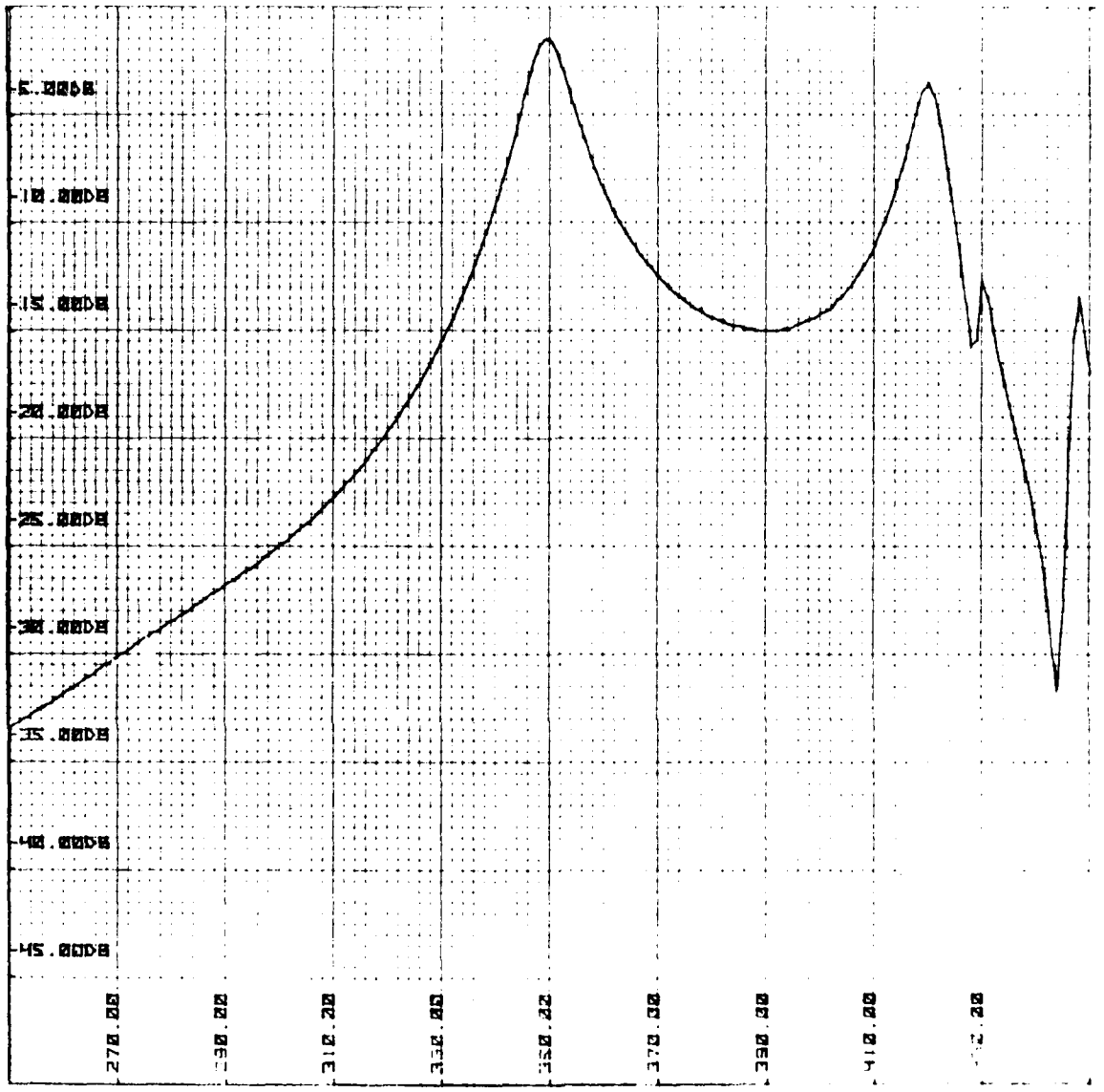


Figure 3.14 Overall Output Filter Response - 350 MHz

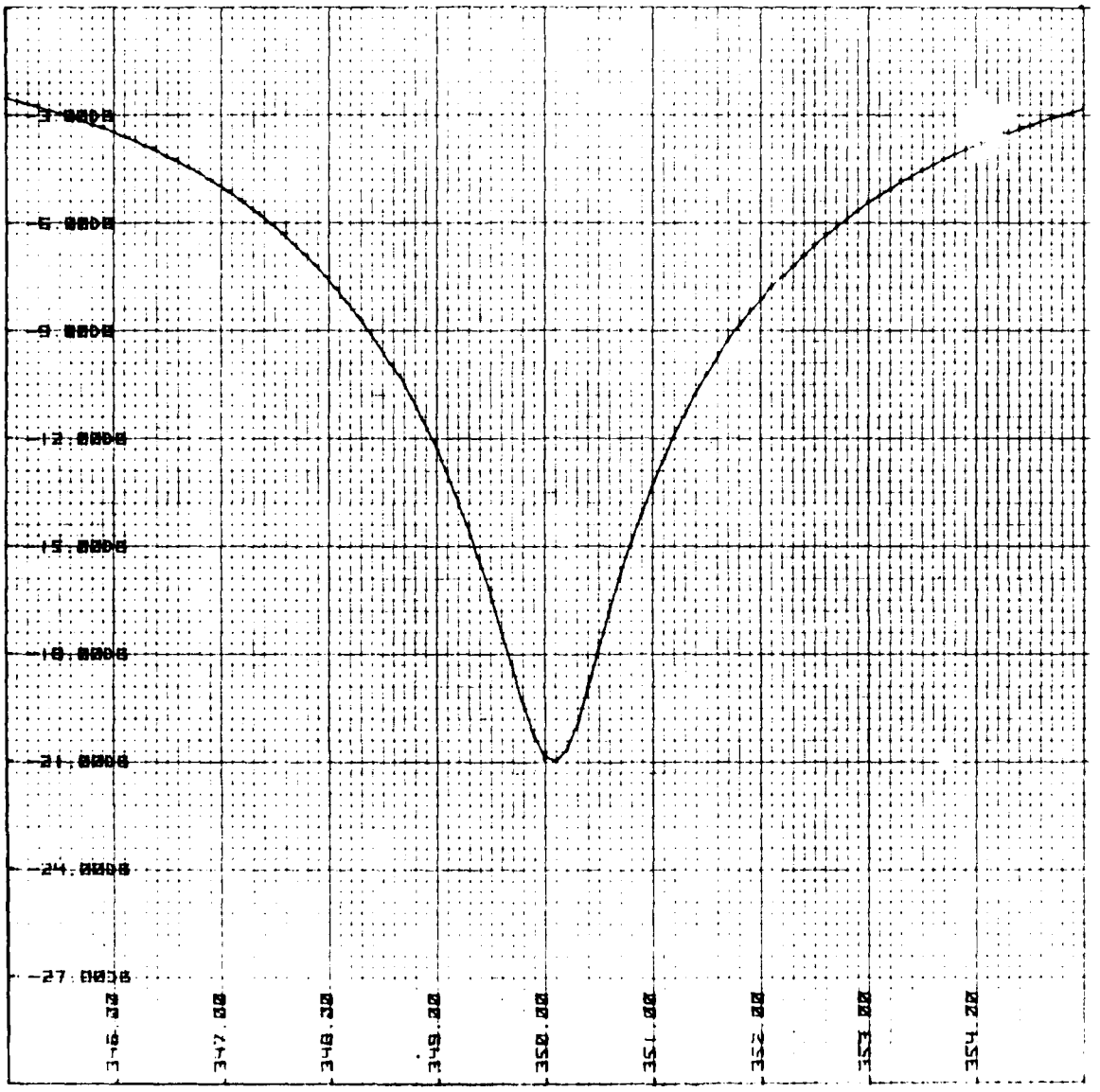


Figure 3.15 Output Filter Return Loss - 350 MHz

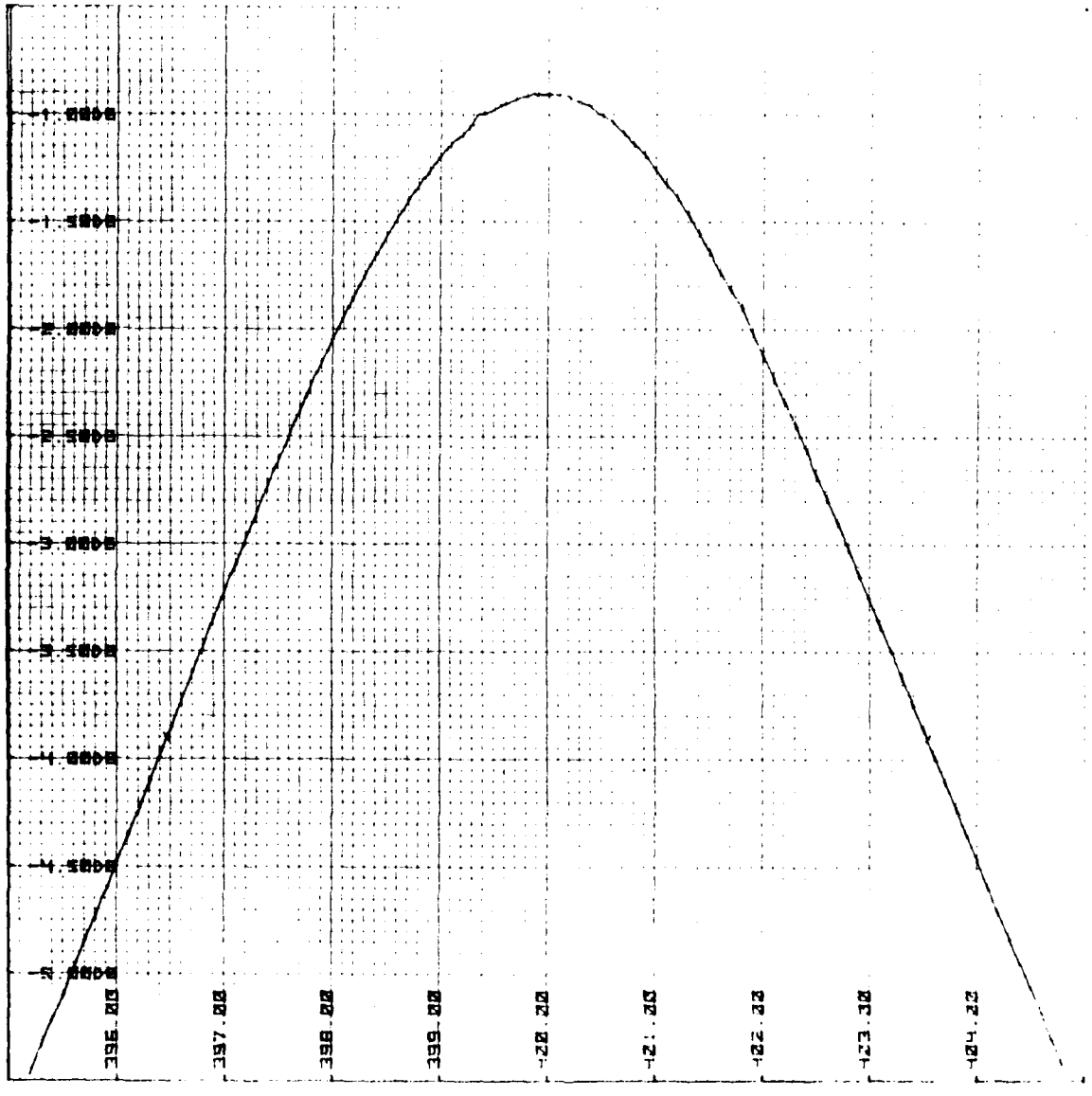


Figure 3.16 Output Filter High Resolution
Bandpass Response - 399.975 MHz

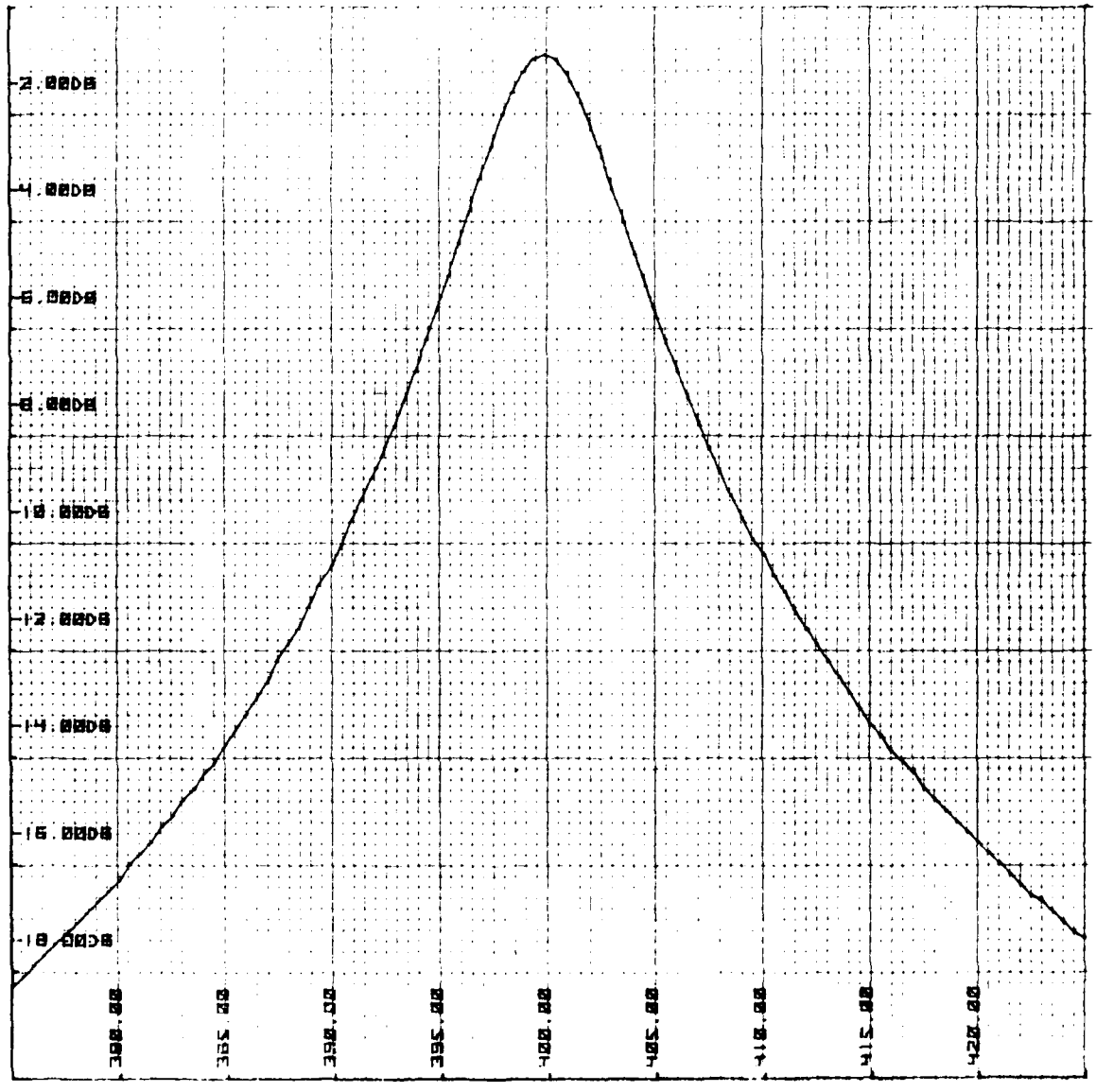


Figure 3.17 Output Filter Selectivity - 399.975 MHz

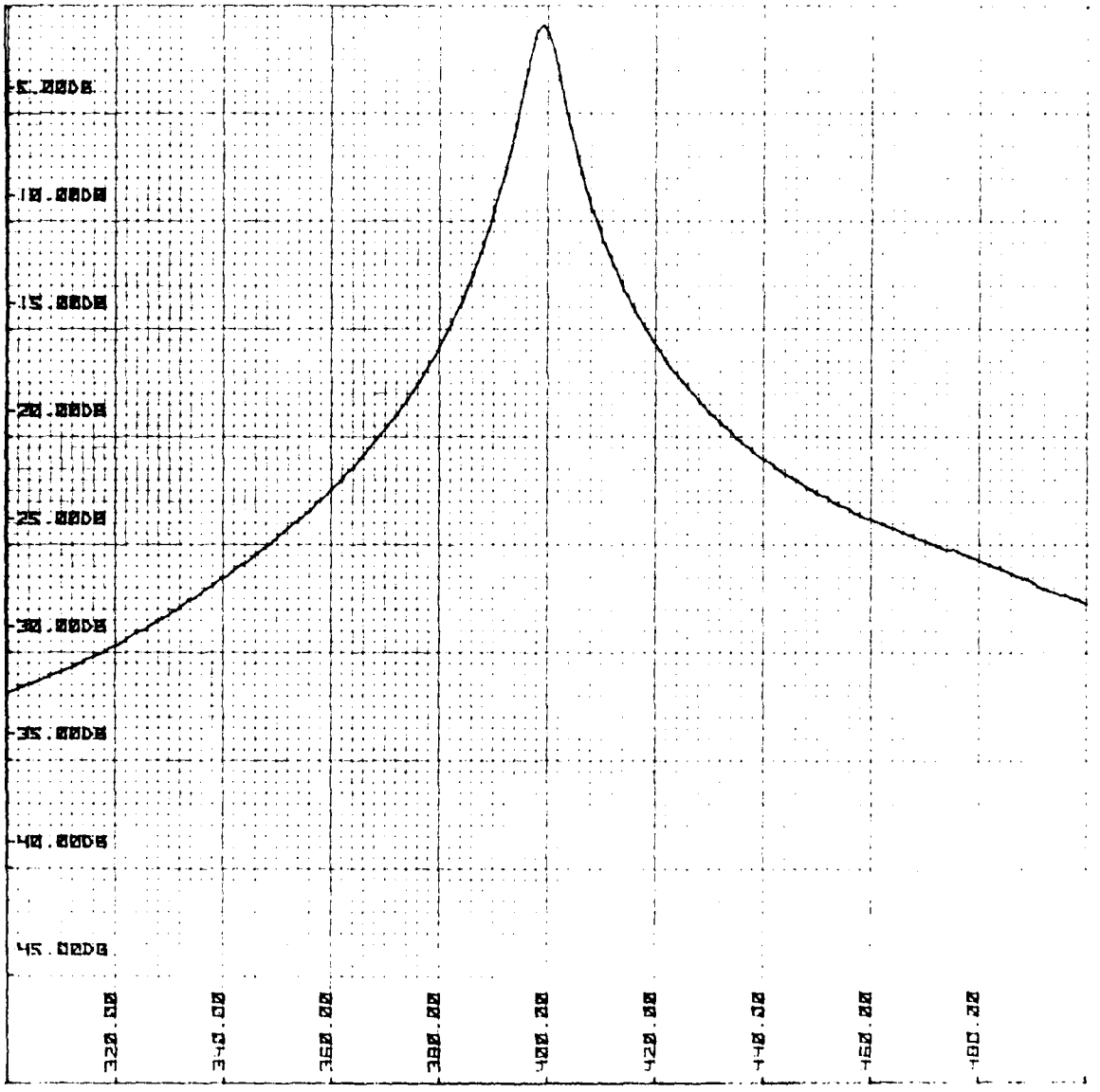


Figure 3.18 Overall Output Filter Response - 399.975 MHz

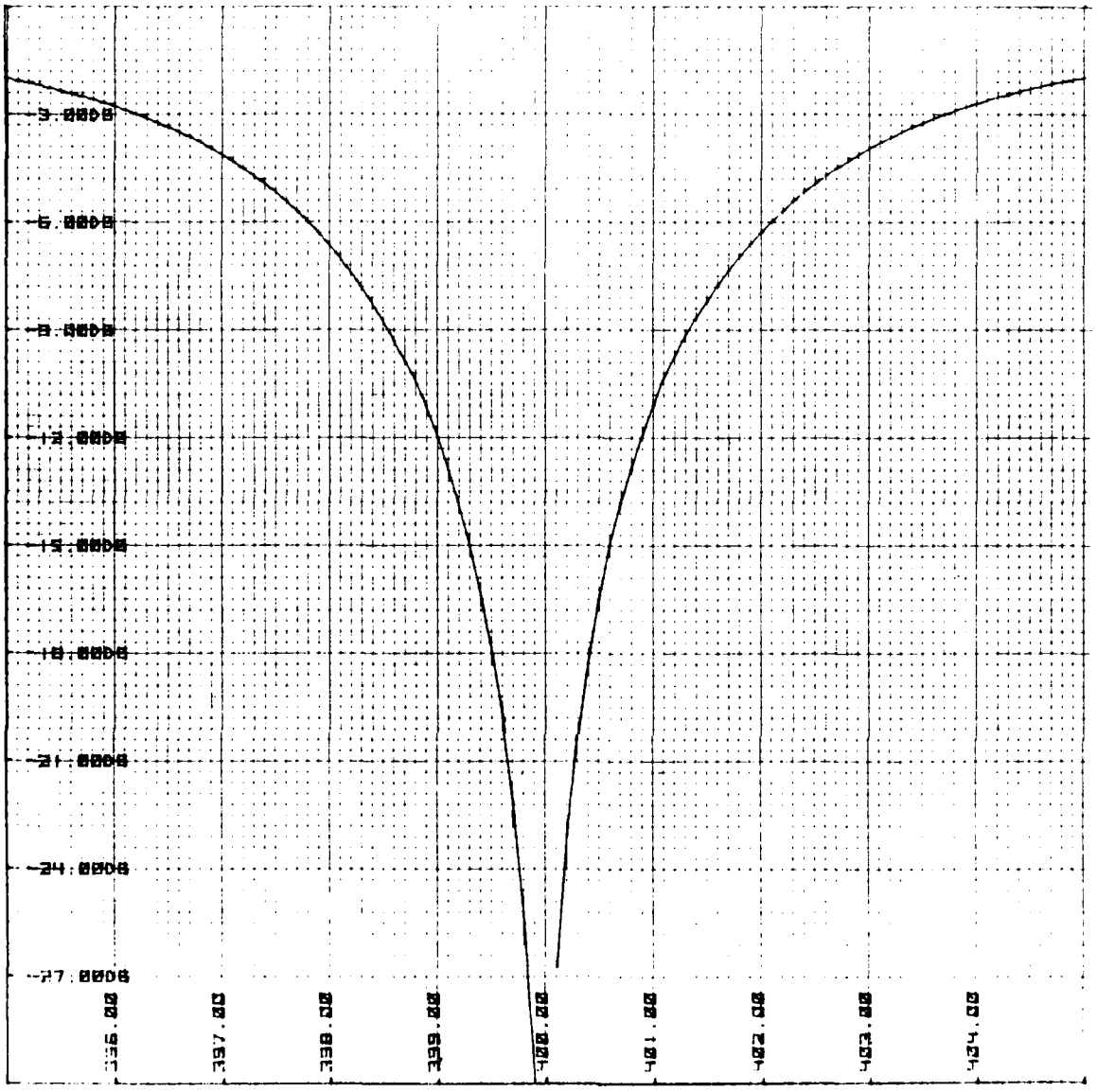


Figure 3.19 Output Filter Return Loss - 399.975 MHz

of the band because of the greater number of ON tuning elements resulting in a more uniform current distribution (and power dissipation) through the filter cavity.

The passband response plots for the output filter show the basic single pole selectivity curves as expected. A number of secondary filter responses present when the filter is tuned to 350 MHz are shown in Figure 3.14. These undesired responses, which are closer to the desired passband in the output filter than the input filter because of the location of the tuning networks, are present for all the tuned frequencies of the output filter. As with the input filter, these responses are the result of interaction between the tuning networks and the resonator and coupling structures. Because the secondary responses fall above 400 MHz, a low pass filter could be used to reject harmonic and spurious output signals from the filter drive source.

3.2.1.3 Filter Frequency Tracking

The only filter response characteristic interacting between the two filters is the frequency tracking accuracy of the tuning networks. The tracking errors obtained for the frequencies tested are listed in Table 3.3. The error shown is greater than the 200 kHz design target because of the method used to set the filter turning codes. As previously described, the input filter resonator tuning resolution is finer than required to obtain tracking between the resonators in the input filter and to track the input filter to the output filter frequency. When the filter tuning codes were determined, all possible codes for the output filter were examined and codes tuning the filter closest to the desired frequency were programmed into the control code ROM (Paragraph 2.3.1). Instead of tuning the

input filter to the output filter and discarding the tuning resolution available, the input filter was also tuned to the closest frequency to reduce losses. While the filter is capable of tuning to the tracking error desired, the system response of the filter pair as tuned has a lower total loss and presents a lower input VSWR to the driver transmitter.

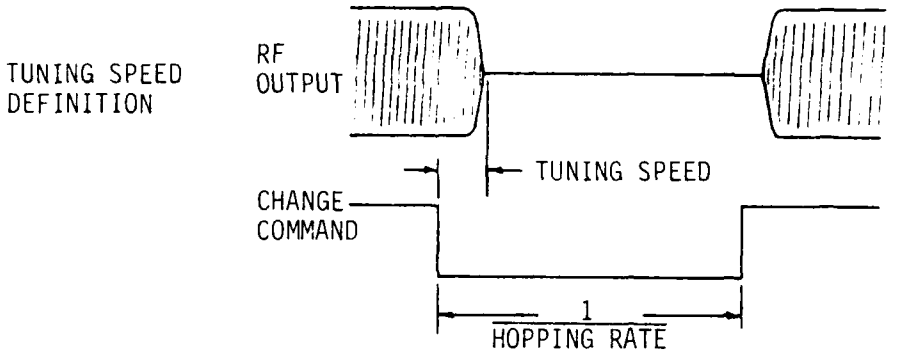
An example of the tracking error achieved would be to obtain a desired frequency of 360 MHz. Since the output filter only has a 2 MHz resolution, it may tune to 361 MHz, while the higher resolution input filter tuned exactly to 360 MHz, resulting in a 1 MHz tracking error. Although the input filter could exactly track the output filter at a desired frequency of 361 MHz, the programming scheme utilizing the added capability of the input filter results in the tracking error desired being exceeded.

Table 3.3 Frequency Tracking Performance

DESIRED FREQUENCY (MHz)	TRACKING ERROR (kHz)
350	380
360	760
370	390
380	310
390	100
399.975	140
355	210

3.2.2 Tuning Speed Tests

To demonstrate compatibility with a tuning time requirement of up to 200 hops per second, the tuning speed test shown in Figure 3.20 was performed. This test relies on the rejection



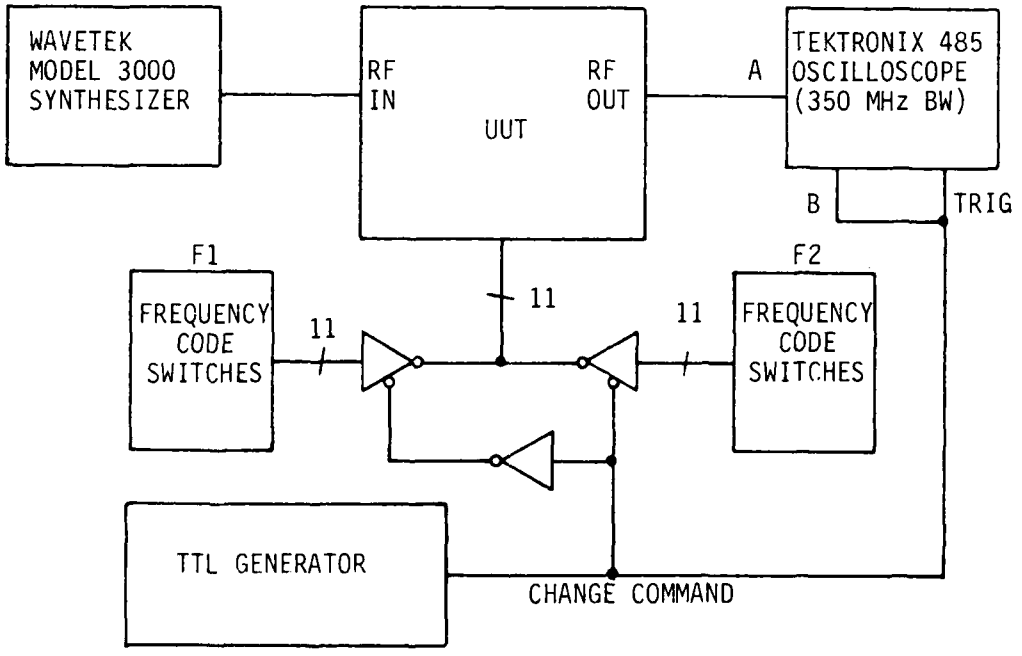


Figure 3.20 Tuning Speed Measurement

of the filter skirt when the filter is tuned away from a CW signal to effectively act as a switch to the input signal. A CW signal is placed at the filter center frequency (the "end" frequency) and the filter tuning control is changed at a 100 Hz rate (200 hops/second) between a "start" frequency and the "end" frequency. The filter tuning speed is then measured by monitoring the RF output of the filter directly on a high frequency oscilloscope. The filter center frequency is controlled by alternately applying one of two fixed TTL logic frequency commands to the control input through two sets of tri-state gates as shown in Figure 3.20. The relationship between the change command and the actual frequency transition is shown in the Figure.

After some initial problems in making the measurement because of system ground loops, the tuning times for each filter individually and for the combined set were measured. The results of these tests for two sets of center frequencies are listed in Table 3.4. All listed times are the maximum noted (to include the timing jitter resulting from the PIN diode driver design), and the tuning speeds are more than adequate for typical 200 hops per second systems. Full settling of the reverse bias voltage occurs within 70 microseconds for both filters.

Table 3.4 Filter Tuning Speed

FREQUENCY (MHz)		TUNING TIME (MICROSECONDS)		
START	END	INPUT FILTER	OUTPUT FILTER	CASCADED FILTERS
350	399.975	40	40	35
399.975	350	44	35	55
370	350	55	40	55
350	370	40	45	45

3.2.3 Power Handling Tests

A simple test consisting of operating each filter at its rated power at three frequencies across the tuning range was performed to demonstrate the power handling capability of the filter pair. A CW signal was applied at the selected filter center frequency, and forward, reflected, and output power levels were measured and recorded using the basic test configuration shown in Figure 3.21.

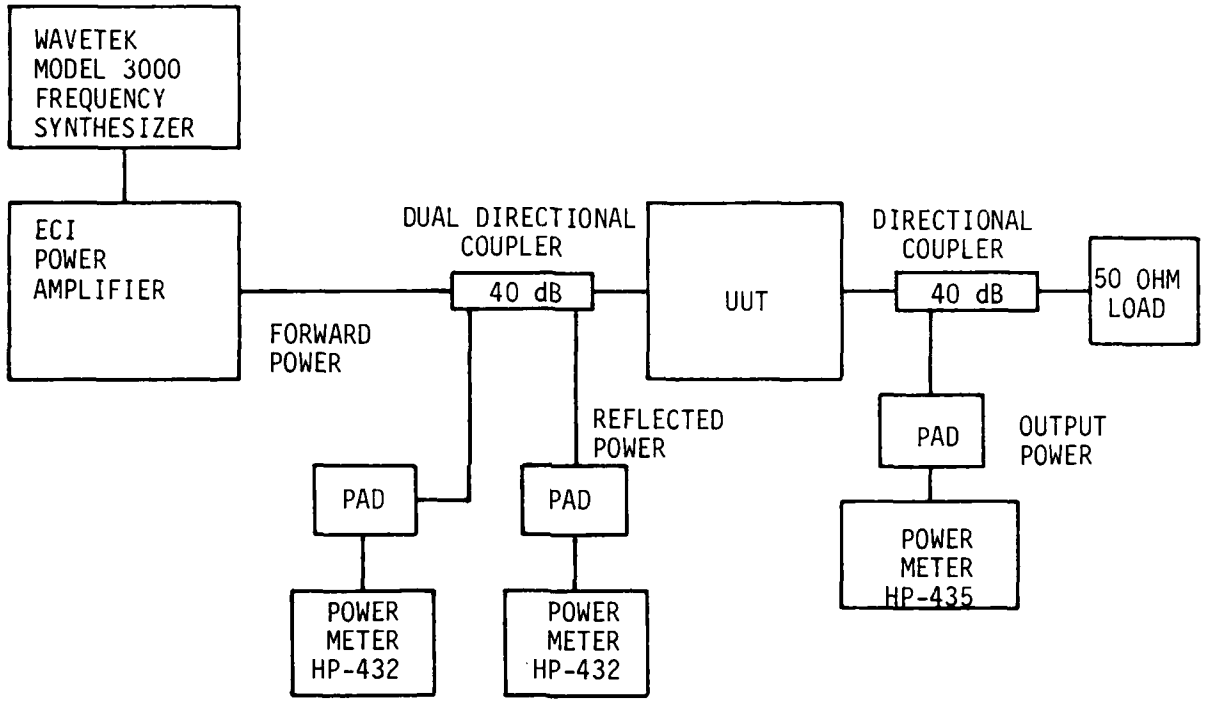
The filter design is intended to be capable of continuous operation. By monitoring the apparent loss and input VSWR as power was applied and noting heating or detuning effects, the capability of handling the rated power continuously and the effectiveness of the cooling systems implemented was noted.

3.2.3.1 Input Filter

The power handling tests performed on the input filter are summarized in Table 3.5. A 100 watt forward power level was applied to the filter and the filter response watched for heating effects. At 399.975 MHz, an approximate 0.05 dB increase in insertion loss was noted between the application of full power and one minute. After this increase, the loss stabilized and no further changes were noted. This result was repeated several times to verify that the filter, and not the monitoring equipment, was changing. No drift or heating effects were noted at other test frequencies.

Table 3.5 Input Filter Power Handling Tests

FREQUENCY (MHz)	POWER LEVEL (WATTS) FORWARD	REFLECTED	OUTPUT	LOSS (dB)	INPUT VSWR
350	100	0.830	50	2.99	1.20
375	100	0.246	56	2.50	1.10
399.975	100	2.3	52	2.80	1.36



NOTE: PADS SET AS REQUIRED FOR POWER LEVELS USED.

Figure 3.21 Power Capability Test Configuration

At the high frequency end of the tuning range, only a few tuning capacitors are directly applied to the tuning circuit. Although NPO ceramic capacitors are used, it is possible that a single part, because of the high RF circulating current, could be heated and cause a slight shift in the center frequency of one resonator to cause the loss increase. The change noted was very slight and did not limit the operation of the filter. The insertion losses noted also compare closely with the values measured using the low level network analysis.

3.2.3.2 Output Filter

The power handling test results for the output filter are summarized in Table 3.6. During testing of the output filter, several failures occurred in the tuning element capacitors before the 1000 watt input power level was reached. The original test concept was to apply a 250 watt carrier signal, then fully modulate the carrier with a 1 kHz tone to obtain a 1000 watt peak power input while watching for arcing or other signs of failure. Then a CW power input of 1000 watts was to be applied and the filter checked for drift and heating effects.

Table 3.6 Output Filter Power Handling Tests

FREQUENCY (MHz)	POWER LEVEL (WATTS) FORWARD	REFLECTED	OUTPUT	LOSS (dB)	INPUT VSWR
350	1000	8	800	1.0	1.20
375	600	-	500	0.79	-
375	500	7	420	0.76	1.27
399.975	1000	15	880	0.56	1.28

Initial testing of the output filter was attempted at 399.975 MHz. At this frequency, only one tuning bit is turned ON, and this bit must handle approximately 10 amps rms of RF circulating current. Because of a test equipment failure, the initial power level applied was well in excess of 1500 watts, and the single ON tuning capacitor failed. This failure resulted in the capacitor being destroyed and was noted in the filter response as a shift to a new center frequency and a corresponding high input VSWR. After replacing the capacitor, the RF power was slowly increased in FM mode until the same capacitor failed again at approximately 250 watts input. This failure indicated a power handling problem in the tuning component. However, similar components have been operated continuously at 20 amps without problem and the filter design was based on this capability.

The defective capacitor was again replaced and the filter retuned to 350 MHz. The full rated 1000 watt power input was applied without incident at this frequency, and no heating or drift affects were noted. Testing next moved to 375 MHz, where one capacitor again failed at between 700 and 750 watts of RF drive. (This was a different part than the piece that failed at 399.975 MHz). This defective part was replaced, and testing once again attempted at 399.975 MHz. During this test, failure occurred at approximately 300 watts.

Since the tuning capacitors were failing repeatedly under high current conditions (the tuning network design maintains nearly constant RF voltage across the band and no failures occurred at 350 MHz), the single ON tuning capacitor was replaced with three paralleled capacitors to obtain an equivalent total capacitance. With this configuration, the 1000 watt input level

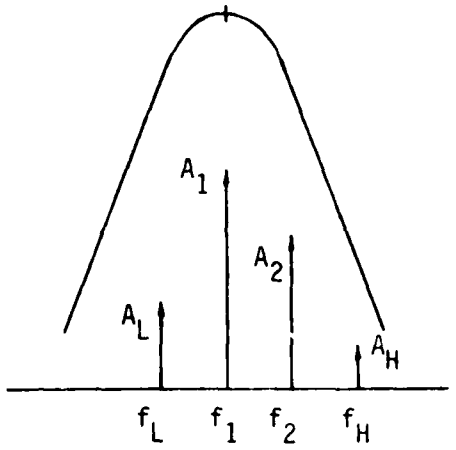
was achieved and no drift or heating effects were noted. Because of the high air flow rate of the output filter blower and mass of the output filter, no thermal heating of the cavity was evident on any exterior surface checked.

Although the capability of the design concept to handle a 1000 watt input was demonstrated with the output filter, the output filter is not capable of withstanding the full input at any frequency within the tuning range. Only the one tuning element was replaced with a paralleled capacitor set, and a power capability of only 200 watts is evident without the change. The cause of the component failure experienced is unknown and is a candidate for further study.

A final effect noted as the result of changing the single capacitor to a parallel set of three pieces was a reduction in insertion loss from 0.91 dB to 0.56 dB (as measured on different equipment). This reduction in loss and the failure of the parts under rated power tend to implicate the capacitors as a cause of the unexpected high unloaded Q obtained for the filters (Paragraph 3.1).

3.2.4 Intermodulation Distortion Products

The measurement of intermodulation distortion products created within each filter of the electronically tuned filter pair provides both a measure of the linearity of the filter and a basis of performance of the filter in a colocation environment. The basic test objective is to inject two CW input signals to the filter with minimal frequency spacing and to measure the level of any third or higher order mixing products. The resulting intercept point, defined in Figure 3.22 along with the relationship between the filter bandpass and the input signals, is a measure of the linearity of the unit under test.



f_1 and f_2 are test signals

$f_H = 2f_2 - f_1 \quad f_L = 2f_1 - f_2$

All levels in dBm (dB referred to 1 milliwatt)

$IP_1 = A_2 + 0.5\ (A_1 - A_H)$

$IP_2 = A_1 + 0.5\ (A_2 - A_L)$

Figure 3.22 Intercept Point Definitions

The two test signals applied to the filter were combined in a multicoupler using the multicoupler filters to isolate the signal sources. This configuration is shown in Figure 3.23. The multicoupler used limits the frequency spacing to approximately 5 MHz. The applied signals at the multicoupler output were 100 watts forward power at the filter center frequency (the "desired" signal) and 10 watts forward power at the second (or "interfering") frequency. The resulting signal at the third order product frequencies was measured, then corrected for the filter rejection to obtain an equivalent level at the filter input. The resulting intercept point referred to the filter input is listed in Table 3.7 for the input filter, the output filter, and the measurement system.

The intermodulation distortion (IMD) tests performed characterize the response of the filters to forward signals. The resulting intercept point measurements may be used to project the performance of the filter with various power levels applied

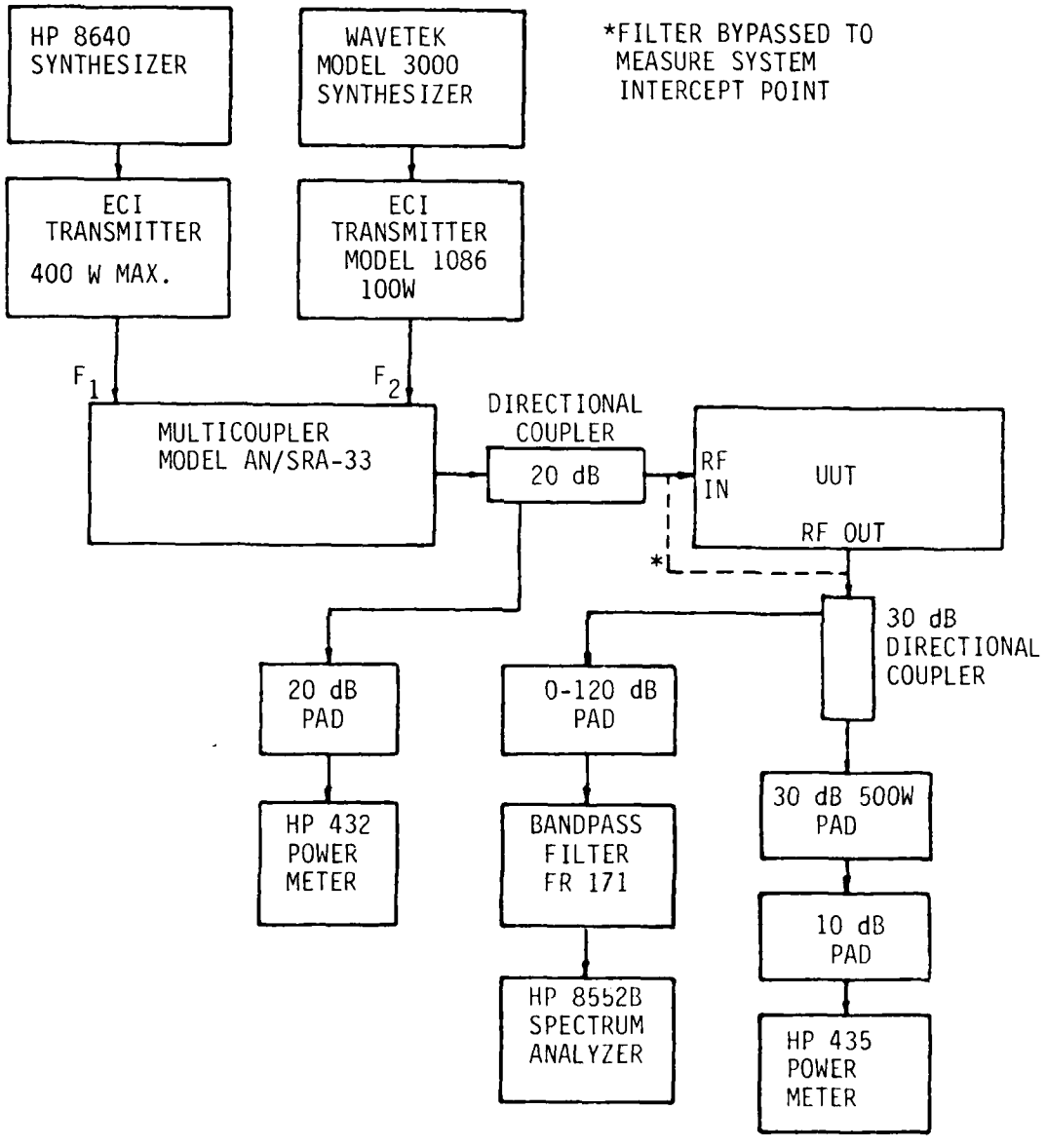


Figure 3.23 Intercept Point Measurement

Table 3.7 Filter Intercept Point Measurement

f_1 (MHz)	f_2 (MHz)	a_L[1] (dBm)	a_H[1] (dBm)	A_L[2] (dBm)	A_H[2] (dBm)	INTERCEPT POINT[3] (dBm) IP_1	IP_2
SYSTEM ONLY							
350	355	<-60	<-60	<-60	<-60	>95	>100
395	400	<-60	-	<-60	-	-	>100
375	370	<-60	<-60	<-60	<-60	>95	>100
INPUT FILTER							
350	355	-32	-58	-10	-23	76.5	75
395	400	-26	-	- 9	-	-	74.5
375	370	-48	-26	-18	-7	73.5	74
OUTPUT FILTER							
350	355	-11	-41	-6	-33	81.5	73
395	400	-20	-	-15	-	-	82.5
37:	370	-37	-19	-27	-14	72	78.5

NOTES:
1. Level measured at filter output.
2. Level corrected for filter rejection.
3. Referred to filter input
4. All frequencies and levels refer to Figure 3.22.
5. Filter center frequency set to f_1, 100 watts applied (+50 dBm).
6. 10 watts (+40 dBm) applied at f_2.

according to the equations listed in Figure 3.22. However, these results are slightly misleading for projections of performance with reverse signals applied such as are present in antenna-conducted IMD tests.

In an antenna-conducted test, the "desired" signal is applied at the filter input, and the "interfering" signal at the filter output. Because of the rejection of the filter (especially in a multiple pole filter), the "interfering" signal level is reduced at the point of non-linearity, resulting in a lower product level. In addition, the filter rejection as the product passes back through the filter to the output further improves the apparent filter performance. The antenna-conducted type test was not performed with the electronically tuned filter pair. However, since the output filter is a single pole resonator the effects of the filter rejection on antenna-conducted IMD performance are minimal for the electronically tuned amplifier.

3.2.5 Amplifier Noise Reduction Tests

The final test performed with the electronically tuned filter pair was a simulation of the electronically tuned amplifier to determine the degree of improvement obtained in the broadband noise performance of the amplifier. A 100 watt transmitter and 400 watt power amplifier were cascaded as shown in Figure 3.24. To increase the noise output of the amplifier without the filters in place, the driver transmitter was operated at a low level (increasing the loss of the input attenuator) and the output power amplifier operated at maximum gain. To maintain the noise output of the transmitter, the input filter was substituted for a 3 dB pad. The noise level was examined with a spectrum analyzer following a notch filter (at 375 MHz) at the system output.

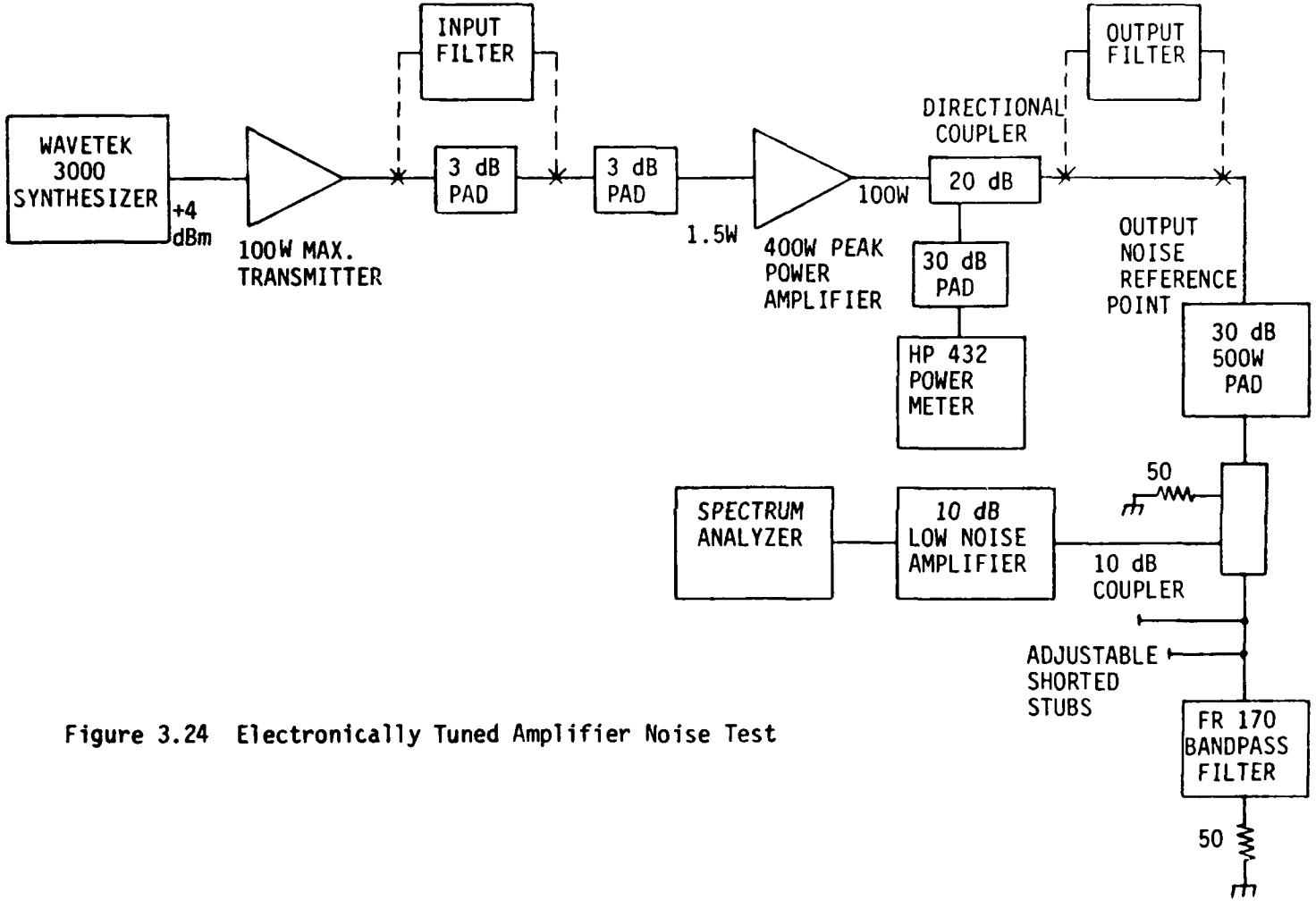
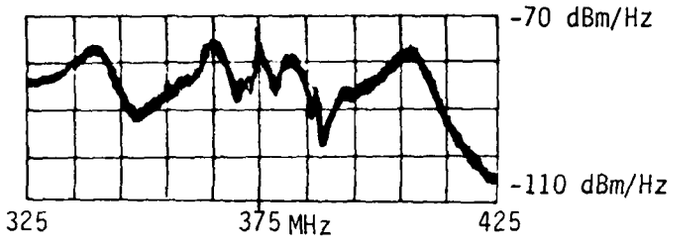
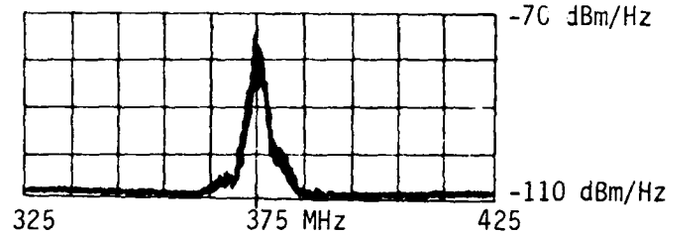


Figure 3.24 Electronically Tuned Amplifier Noise Test

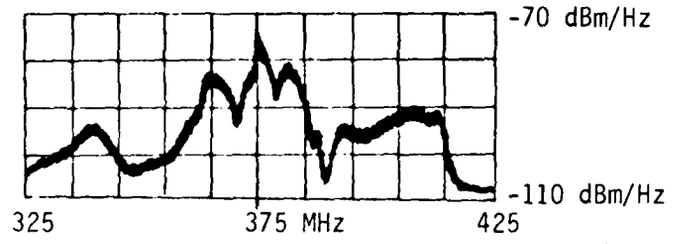
The results of the noise improvement obtained by various combinations of test amplifier configurations over a 100 MHz range are shown in Figure 3.25. The first graph shows the broadband noise output of the amplifiers with no filters installed. The effect of internal amplifier low pass harmonic filtering can be seen in the noise performance above 400 MHz. The second graph shows the substantial improvement obtained with both electronically tuned filters installed in the amplifier. Except for a 20 MHz band centered at the carrier, the noise level shown is the instrumentation noise floor of -110 dBm/Hz. Finally, the response of the amplifier with only the output filter installed is shown. Although some improvement compared with the amplifier-only response is shown, the low ultimate rejection and wide bandwidth of the output filter significantly limits the improvement obtained. Figure 3.26 shows two expanded plots of the amplifier noise over a 20 MHz band. First, the response of the unit with both filters installed is presented. This graph is equivalent to the second plot of Figure 3.25 expanded to provide additional close-in detail. The second graph of Figure 3.26 shows the noise performance of the amplifier set with only the input filter installed. The input filter provides most of the noise improvement obtained on the amplifier, with the major difference between one filter and both filters installed being the gain of the output amplifier.



AMPLIFIER-ONLY
NO FILTERS INSTALLED



AMPLIFIER WITH
INPUT FILTER AND
OUTPUT FILTER INSTALLED



AMPLIFIER WITH
OUTPUT FILTER ONLY
INSTALLED

Figure 3.25 Electronically Tuned Amplifier Noise Performance

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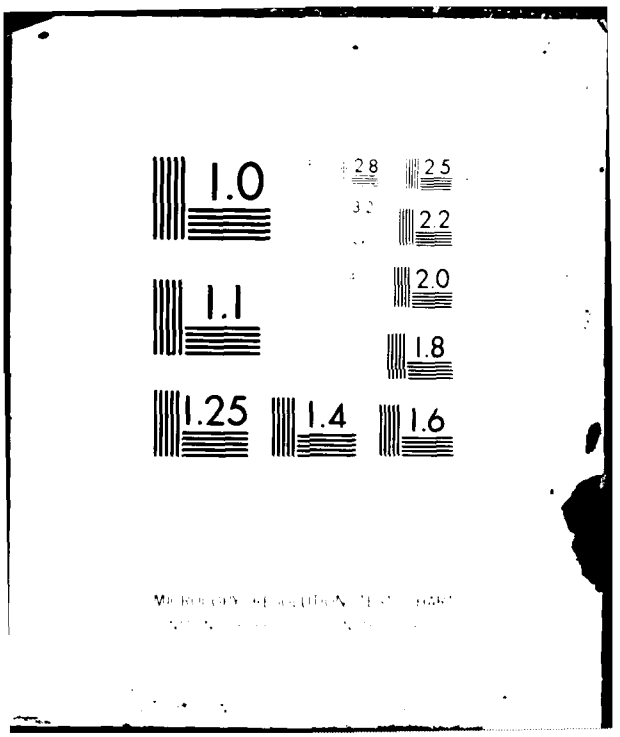
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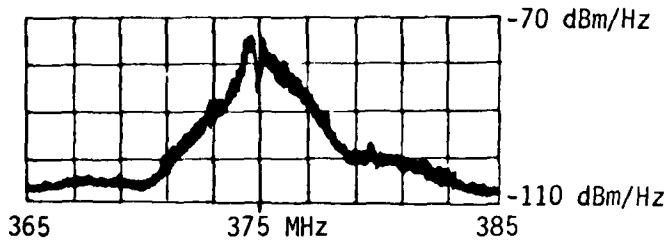
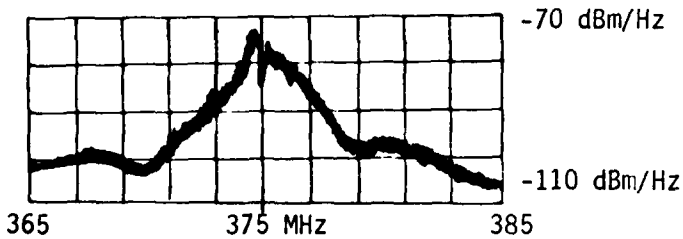


AMPLIFIER WITH INPUT FILTER AND OUTPUT FILTER INSTALLED



AMPLIFIER WITH INPUT FILTER ONLY INSTALLED

Figure 3.26 Expanded Amplifier Noise Performance Plots

4.0 CONCLUSIONS

The development and design of an electronically tuned frequency tracked filter pair based on a combination of classical microwave filter cavity designs and an electronically tuned resonator design technique has been described in this final technical report. The filters, consisting of a two pole 100 watt filter and a single pole 1000 watt resonator, are intended to be placed at the input and output of a frequency hopping UHF power amplifier to reduce the broadband noise and spurious signal outputs of the resulting electronically tunable amplifier. The improvement achieved in EMC (electromagnetic compatibility) performance allows the amplifier to be used in colocation environments with other equipment.

The design of each of the electronically tuned filters is based on a previously developed method of tuning a high power resonator with PIN diode switched capacitors. The correlation of the design of both the combline input filter and the coaxial resonator required is developed in the mathematical models presented in this report.

Experimental brassboard models of the electronically tuned filters were constructed to comply with the design requirements and goals of the statement of work. Advantages and limitations of the filter structures and electronic tuning networks were balanced against the design objectives to obtain the final design concepts used. Because the filters were only intended as brassboard models, primary emphasis was placed on the electrical performance and cooling requirements, while mechanical structure and packaging were secondary considerations in the hardware developed. In addition to the RF cavity structures, each filter includes the support electronics required to interface a BCD-encoded TTL-compatible frequency code to the bias levels needed to tune the filter.

The results of the testing phase of the development program demonstrated the capability of the concepts used to realize the desired filtering and amplifier noise improvement while maintaining the frequency agility required for hopping applications. Two significant problems noted during testing relate to deviations of the final hardware from the initial design projections. First, a problem with higher than expected series resistive losses in the tuning networks resulted in increased filter insertion loss and a trade-off between bandwidth and loss to optimize the filter to the EMC problem. Second, component failures in the output filter limited the power handling capability for certain tuned frequencies. The first problem was resolved by the design trade-off mentioned, while a solution to the second problem was demonstrated by paralleling components to obtain the power handling required. These problems are discussed in Paragraphs 3.1 and 3.2.2, and recommendations for additional effort are listed in Section 5.0. Testing of the experimental model filter pair with a power amplifier demonstrated a significant improvement in the EMC performance of the amplifier beyond ± 5 MHz from the tuned frequency. Combined with the 60 microsecond tuning times, the filters show a good potential for resolving the colocation problems present in frequency hopping systems.

5.0 RECOMMENDATIONS

Although the development of the electronically tuned filter pair is based on previously developed concepts of incorporating electronic tuning into classical microwave filter structures, and the performance of the experimental model demonstrates the basic characteristics desired, several areas of improvement have been noted to enhance the performance of an electronically tuned amplifier. These improvements are concerned with the amplifier configuration, filter implementation, and reduction of filter losses.

Because the experimental model filters are intended only to show the feasibility of the design concept, additional changes not listed are also required to package the filters, provide interface features such as a key interlock, error detection, BITE, and manual local control, and improve the tuning resolution. These enhancements would normally be considered during the development of more advanced hardware.

5.1 Output Filter Configuration

The selection of a single pole output filter for the application described in Paragraph 1.1 causes particular problems in design and limits the amplifier performance obtained. A two pole filter as was used for the input filter of the filter pair would provide significantly improved filter characteristics at the expense of the added complexity of the additional filter pole and supporting electronics required.

The key advantage of using a two pole filter is the reduction in the doubly loaded Q of each resonator required to obtain a fixed bandwidth compared with a single pole filter. For the filter designs of this effort, the single pole output

filter required a doubly loaded Q of 125 while only 88 is required for a two pole filter with the same overall loaded Q of 125. Because of the high power handling requirement of the output filter, the reduction in the electrical stresses in each resonator resulting from the reduced doubly loaded Q significantly eases the requirements on the tuning network design. Also, the reduced circulating voltages and currents in each resonator would permit the tuning network position to be re-optimized such that the network sensitivities would be reduced (Paragraph 2.2.2). As implemented in the experimental model filter because of insertion loss considerations, the final loaded Q of 50 would result in a two pole filter loaded Q of approximately 70 with no increase in electrical stresses.

In addition to the design related factors of implementing the filter, performance related improvements related to the electronically tuned amplifier are also possible with a two pole output filter. A two pole filter has increased rejection to adjacent signals and a greater ultimate rejection than a single pole filter. The antenna conducted intermodulation distortion performance of the amplifier would therefore be improved by allowing closer-spaced signals with equivalent performance and by reducing the level of distortion products for signals outside the filter 3 dB bandwidth. The system noise performance is also improved, although the tests of Paragraph 3.2.5 demonstrated that the primary improvement in noise performance is achieved by the input filter.

5.2 Input Filter Cavity Implementation

The cavity structure for the input two pole combline filter was deliberately made physically large as an experiment to examine the unloaded Q obtained compared with previous

designs. As described in Paragraph 3.1, the improvement obtained by doubling the cavity volume resulted in no measurable increase in the cavity unloaded Q. The single advantage of the very large cavity used is a reduction in the capacitive coupling between tuning network elements of the two resonators. However, a much smaller cavity with internal partitions is appropriate for future designs to reduce the size and weight of the filter structure. Implementation of schemes to further decrease the size by designing the coupling mechanism to interact with the cavity housing[6] have also been used and may be appropriate for the input filter. Should the output filter also change to a two pole design, similar schemes within the power handling requirements are also applicable.

5.3 Tuning Capacitor Losses

A substantial effort was made during the design and testing of the electronically tuned filter pair to determine the source of resonator losses above the levels initially projected (Paragraph 3.1). As finally determined by indirect means through performance characteristics and by component failure during high power testing, the primary cause of the degraded unloaded Q obtained is the high Q capacitors used in the resonator tuning networks.

The requirements of high loaded Q and high power capability result in high circulating RF currents in the tuning networks. The effect of series resistance present in the tuning elements is multiplied by the circulating currents, resulting in a need to significantly reduce losses of all types. The initial design projection of the total equivalent series resistance in

[6] T. Swanson, "Electronically Tuned UHF Receiver Preselector", Final Technical Report, Contract F30602-77-C-0200, August 1979. RADC-TR-79-210

the output filter tuning network was a maximum of 0.020 ohms. Therefore, all factors involved in the construction of the filter, including contact resistances, solder joints, interconnecting lead material and lead length can have major effects on the total resistance, and thus the filter losses.

Because of the failure of the capacitor dielectric during high power testing, dielectric losses appear to be the primary limiting factor in the performance of the filter set experimental model. However, under similar conditions in other filters, these effects have not been noted. Additional study of the exact nature of the losses noted is required, and research and development of capacitors with even lower losses than the parts used could provide a major advance in the performance of other electronically tuned filters. In particular, the cause of the component failures experienced should be investigated further so that component limitations can be accounted for in future designs.

5.4 PIN Diode Bias Decoupling

Once again, losses in the PIN diode bias decoupling networks have been a significant factor in the overall resonator unloaded Q obtainable. Although the optimum decoupling system in terms of size, ease of implementation, and predictable response is a standard molded choke, lower losses are achieved with air-wound coils. The increased stray capacitance, size, and insufficient decoupling of the air-wound choke causes tuning interaction and makes implementation difficult, but reduced losses are required in all areas of the filter design. Additional effort is required to either determine more elaborate decoupling schemes with reduced losses or to improve the predictability of the simple air-wound choke scheme so that compensation methods for its detuning effects can be determined.

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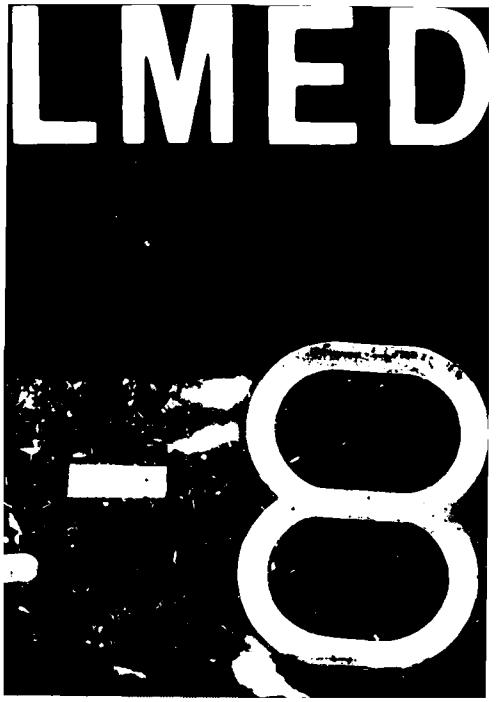
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