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WIDEBAND MONOLITHIC MICROWAVE AMPLIFIER STUDY.(U)
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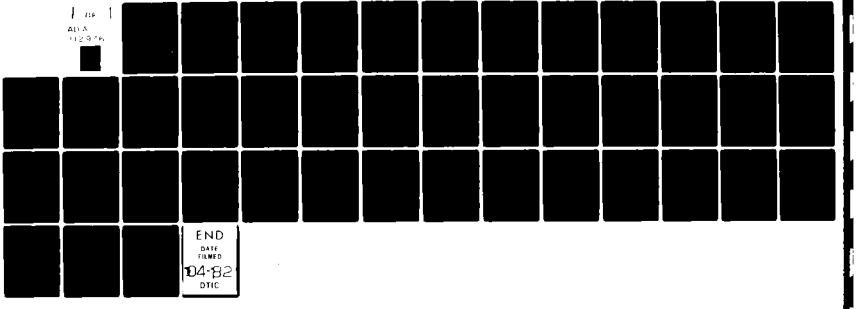

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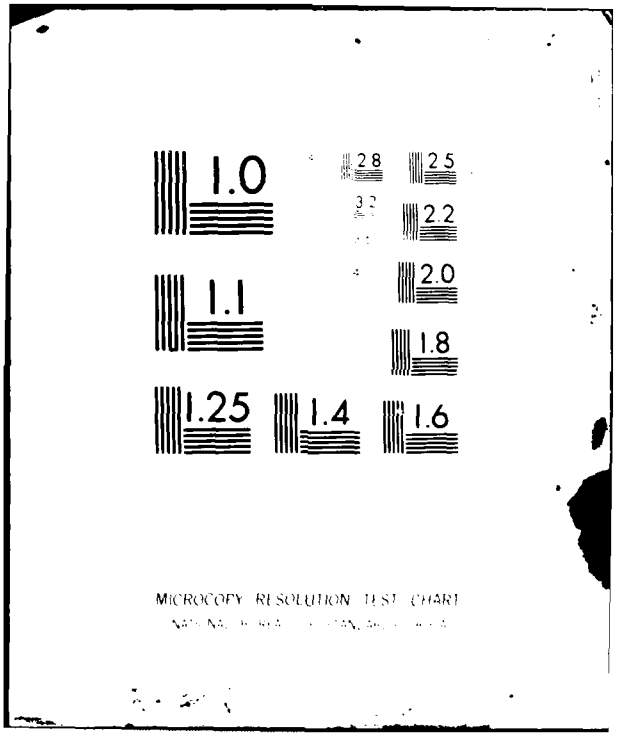
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Electrical

Computer

Engineering

DEPARTMENT OF ELECTRICAL
AND COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN-MADISON

AD A112976

Wideband Monolithic Microwave Amplifier Study

August 1981

Contract N00014-80-C-0923
Contract Authority NR 243-033

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ENGINEERING EXPERIMENT STATION
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SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: NR 243-033-1	2. GOVT ACCESSION NO.: AD-A112 976
3. RECIPIENT'S CATALOG NUMBER:	
4. TITLE (and Subtitle): Wideband Monolithic Microwave Amplifier Study	5. TYPE OF REPORT & PERIOD COVERED: Annual Technical Jul 80 - Aug 81
	6. PERFORMING ORG. REPORT NUMBER: ECE-81-11
7. AUTHOR(s): J. B. Beyer, R. C. Becker, J. E. Nordman	8. CONTRACT OR GRANT NUMBER(s): N00014-80-C-0923
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Dept. of Electrical and Computer Engineering, University of Wisconsin	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: PE 61153N, RR 021-02-03, NR 243-033
11. CONTROLLING OFFICE NAME AND ADDRESS: ONR-414, Arlington, VA 22217	12. REPORT DATE: Aug 81
	13. NUMBER OF PAGES: 38
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report): unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

ONR Scientific Officer (202) 696-4218

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Distributed Amplifier

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report discusses distributed amplifier theory in the context of the microwave monolithic GaAs circuit. It is shown that GaAs FET devices dictate that both the input and output transmission lines become lossy which places fundamental limitations on the distributed amplifier concept and results in different constraints than are found in lossless distributed amplifier design. First order theory indicates that gain asymptotically approaches an upper bound and little benefit results from increasing the number of devices beyond certain limits.

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Enclosure (3)

ECE-81-11 August 1981

Wideband Monolithic Microwave Amplifier Study

J. B. Beyer

R. C. Becker

J. E. Nordman

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I. INTRODUCTION

This report summarizes our efforts from 1 September 1980 to 31 July 1981 of a three-year program to study the feasibility of applying the distributed amplifier concept to GaAs MMIC's. This section will serve as an introduction to the distributed amplifier concept by comparing some of its salient points with those of the cascade amplifier.

Distributed amplification is an old concept[1] that seems to have definite advantage when applied to FET microwave amplifiers. The designs appear to offer potential for improved impedance and gain characteristics over broad bandwidth when compared to conventional cascade amplifiers. In the distributed amplifier, device input and output reactances are incorporated into input and output transmission lines which are periodically loaded by the devices. As a result, the ideally frequency independent characteristic resistance lines tend to provide a constant input and output resistance.

Consider the general problem of impedance matching to a reactively constrained MESFET. In the cascade amplifier approach, it is possible to match[2] but not possible to exactly match at more than one frequency[3]. For broadband operation, a finite mismatch is required in order to compensate for the reactive elements. The distributed amplifier with its almost constant impedance transmission lines represents a different matching problem. Since all reactances are incorporated in the transmission lines, resistive

matching over broad bandwidths becomes a standard low pass filter problem[4].

The distributed amplifier would appear to have an inherently more "flat" gain characteristic than the cascade amplifier. Since the transistors do have gain falloff with frequency, the cascade amplifier must compensate for this with the input and output matching networks. For a MESFET, S_{12} is very small and can be set to zero. Doing so, Ku and Peterson[5] showed that the equation to solve for transducer gain, $G_t(\omega)$ is

$$G_t(\omega) = |S_{21}|^2 \cdot \frac{(1 - |S_g|^2)}{|1 - S_g S_{11}|} \cdot \frac{(1 - |S_L|^2)}{|1 - S_L S_{22}|} \qquad (1)$$

where S_g and S_L are the reflection coefficients of the generator and load respectively, and S_{11} and S_{22} are FET gate and drain reflection coefficients. Solving this for constant G_t in the passband when $|S_{21}|$ is frequency dependent is the objective.

The distributed amplifier is subject to the same variations in $|S_{21}|$ as is the cascade amplifier. The typical case encountered is that $|S_{21}|$ is a decreasing function of frequency. It is this case which we will consider. It can be shown that the impedance of a constant-k transmission line is

$$Z_o = \frac{R_o}{\sqrt{1 - f^2/f_c^2}} \qquad (2)$$

where $R_o = \sqrt{L/C}$ and f/f_c is the frequency normalized to the cutoff frequency of the line. From Ginzton[6], one finds the gain of a distributed amplifier to be

$$A = \frac{n\, g_m}{2} \sqrt{|Z_{01} Z_{02}|} \tag{3}$$

where Z_{01} is the impedance of the input transmission line and Z_{02} is the impedance of the output line. In order to add the transistor drain currents constructively, the cutoff frequency of both input and output lines must be equal. Therefore,

$$A = \frac{n\, g_m}{2} \frac{\sqrt{R_{01} R_{02}}}{(1 - f^2/f_c^{\,2})^{1/2}} \tag{4}$$

which causes a gain peak near f_c, and compensates for transistor gain taper to some extent.

Compensation of gain taper in the distributed amplifier can also be accomplished by use of an equalizer at the input (also possible at the output). Since the input of the distributed amplfier is reasonably constant impedance, we can use the results of Carlin[7] who has shown, for lossless equalizers, that

$$|S_{21}(j\omega)|^2 = 1 - |S_{11}(j\omega)|^2 \tag{5}$$

where S_{21} is the equalizer power shaping function and S_{11} is the reflection function of the equalizer input. Solutions to this problem are simpler than the solutions to Eq. (1), and only need to be applied to the total amplifier, rather than implemented at each stage as in the cascade amplifier. From this, we see that it is potentially easier to obtain a flat gain characteristic from the distributed

amplifier (there are no interstage matching networks to "tweak"). This amplifier could also be physically smaller due to the decreased use of die area for matching sections.

It is interesting to note that matching to a transistor in a cascade amplifier involves absorbing input and output reactances, and then transforming the remaining resistances to the desired level while the distributed amplifier is degraded by the input and output resistances. These degradations are significant and will be discussed in detail later in this report.

Regarding reliability, it should be pointed out that a single device failure in a cascade amplifier chain will result in failure of the entire amplifier chain. The failure of a device in a multiple device distributed amplifier may not result in a complete failure. For example, an open gate on one device in the distributed amplifier will degrade the amplifier performance (i.e., bandwidth, gain, and gain flatness). Similarly, a gate to source short in a later device in one stage will cause the subsequent devices to become non-contributory, with the same results mentioned previously.

A special feature of the distributed amplifier is its ability to provide gain at frequencies above which the transistors have less than unity gain. This is a fundamental property of the amplifier which arises from the isolation of the active device input and output impedances. This isolation permits adding the output currents of the

devices in-phase such that a growing amplitude wave becomes excited on the output transmission line.

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II. GENERAL DISTRIBUTED AMPLIFIER THEORY

Consider the distributed MESFET amplifier stage shown in Fig. 1. The input transmission line connecting the gates is an artificial line consisting of series inductance and shunt capacitance. The series inductance is that of a section of microstrip line short with respect to the wavelength, while the shunt capacitance is that of the transistor gates. The output line connecting the drains is a similar artificial line except here the capacitors represent the capacitance of the transistor drains. Although the true equivalent circuit for a MESFET at microwave frequencies is more complicated than this simple model, it will suffice to demonstrate the principle. A more realistic transistor model will be used shortly when computer modeling is considered.

The characteristic resistance of the input line is $R_{01} = \sqrt{L_i/C_g}$, while that for the output line is $R_{02} = \sqrt{L_0/C_D}$. A forward traveling wave on the input line excites the transistor gates in turn. In order that drain currents produced by each transistor add constructively in the drain line and contribute to a growing wave toward the output termination, it is necessary that the traveling waves on input and output lines have the same propagation velocity. Since

$$v_\phi = \frac{K}{\sqrt{LC}} \text{ m/sec} \tag{6}$$

where K is a proportionality constant, it is required that

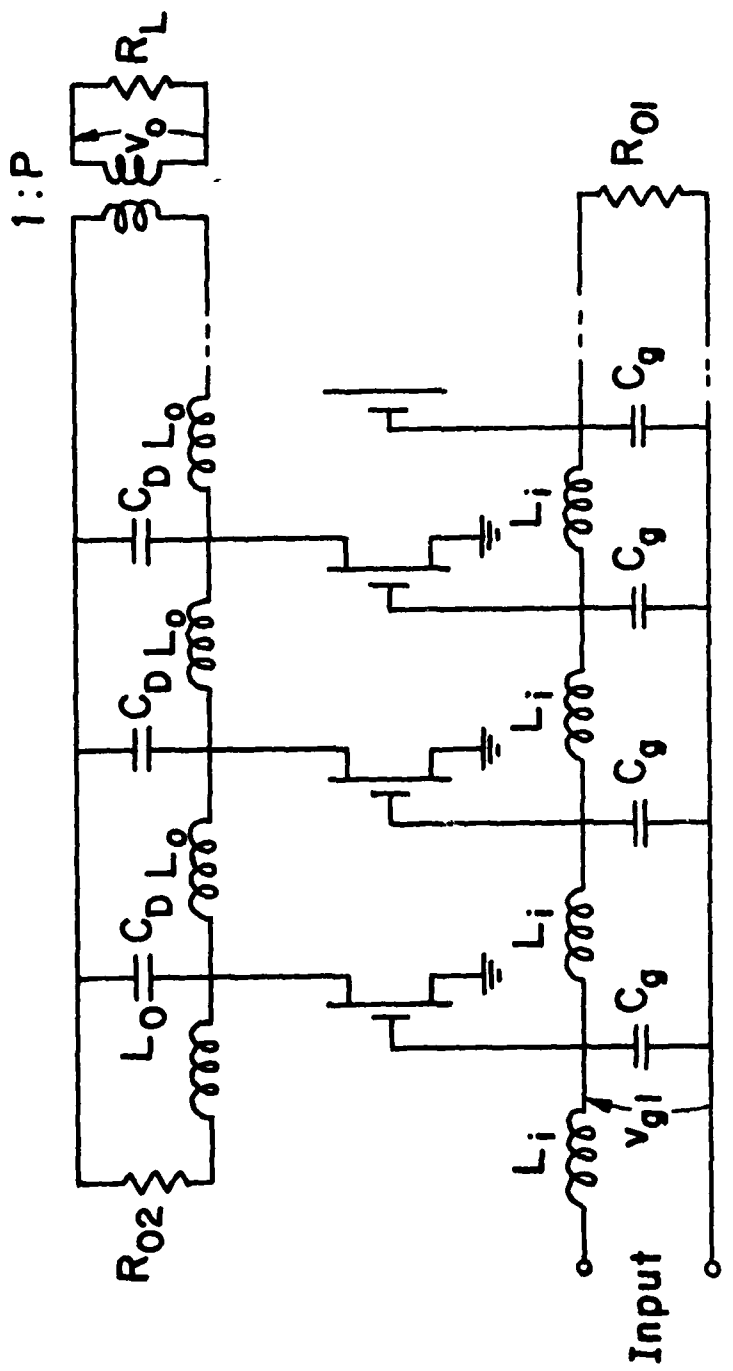

Fig. 1. Distributed Amplifier

$$\frac{L_i}{L_0} = \frac{C_D}{C_g} \tag{7}$$

These equations define important design relations, and, in addition, depending on how certain constraints are imposed, gain and bandwidth are also related. Since wideband operation is the sought-after goal, it is important to understand how the gain-bandwith relationship is developed.

(a) Lossless Case

In the classical loss free case studied by Ginzton, a reasonable constraint to impose dictated by the economics of lumped element circuits was to minimize the number of active devices. He considered a cascade of m such stages as the one in Fig. 1. Each stage contained n active devices, hence a total of N = mn, and N is to be minimized.

When stages such as shown in Fig. 1 are cascaded, the transformer turns ratio must obviously be

$$P = \sqrt{\frac{R_{01}}{R_{02}}} \tag{8}$$

and then the gate-to-gate gain per stage will be

$$A = \frac{ng_m}{2}\sqrt{R_{01}R_{02}} \quad . \tag{9}$$

Since the artificial lines have a cutoff frequency given by

$$f_c = \frac{1}{\pi\sqrt{LC}} \quad , \tag{10}$$

the gain can be written as

$$A = \frac{ng_m}{2 f_c \sqrt{C_g C_D}} \quad . \tag{11}$$

Wheeler[8] defines the device gain for maximum bandwidth operation of the artificial lines as

$$A_t = \frac{g_m}{f \sqrt{C_D C_g}} \quad . \tag{12}$$

Hence, by definition, the frequency for which the device gain goes to one is

$$f_o = \frac{g_m}{\sqrt{C_D C_g}} \quad . \tag{13}$$

This allows the stage gain to be written as

$$A = \frac{nf_0}{2f_c} \quad . \tag{14}$$

For m stages, the amplifier gain is

$$G = \left[\frac{nf_0}{2f_c}\right]^m \quad . \tag{15}$$

Finally, minimizing the number of active devices yields

$$m = \ell nG \tag{16}$$

Equations (13, (15) and (16) constitute the design equations for the loss free amplifier. For a given device, Eq. (13) yields f_0, Eq. (16) gives the number of stages for a desired gain, and finally, Eq. (15) determines the number of active devices per stage for a given bandwidth.

(b) Lossy Case

We have considered the classical case of part (a) in detail and have concluded that it is unrealistic for MMIC application. First of all, in the context of integrated

circuits, it is no longer an economic imperative to minimize the number of active devices, and certain definite benefits accure when this restriction is no longer imposed. Secondly, the dissipative loading included in the input and output of a realistic MESFET model cannot be ignored. Its effect is not only to alter the bandwidth of the artificial lines but in addition to cause attentuation in the lines. As will be shown in the next section, this attenuation is a critical factor and demands the imposition of a different criterion in determining the gain-bandwidth relationship.

Let us examine the simplest case first wherein to first order, the losses may be ignored, but we no longer minimize the number of transistors. Consider as a typical example, Texas Instrument 300 μ gate transistors, which have according to Eq. (13), an f_0 = 54 GHz. For 17 dB of gain and a 20 GHz cutoff frequency, Eq. (14) indicates that a single stage of 6 transistors will be required. For the same gain and bandwidth, but under the constraint of part (a) which minimized the number of devices, Eqs. (14) and (15) dictate 2 stages of 2 transistors each. Hence, the addition of two transistors results in the elimination of a broadband interstage transformer; clearly, this is the preferred choice for MMIC realization.

Consider now the effect of losses to further illustrate that device minimization is not always the best condition. Suppose that each section of input artificial line has an attenuation factor of α_1/section and each section of the

output line has α_1/section. For this case, we rewrite Eq. (9) as

$$A = \sum_{p=1}^{n} \frac{g_m \sqrt{|Z_{01}Z_{02}|}}{2} (\alpha_1)^p (\alpha_2)^{n-p+1} \tag{17}$$

where n = number of transistors in the stage, and p = summation index. To simplify Eq. (17) somewhat for the purpose of illustrating the principle, suppose the attenuation on the input and output lines is the same. Then Eq. (17) becomes

$$A = \frac{ng_m \sqrt{|Z_{01}Z_{02}|}}{2\ 2} (\alpha)^{n+1} \tag{18}$$

where $\alpha_1 = \alpha_2 = \alpha$. The gain in Eq. (18) is maximized when

$$n = -\frac{1}{\ell n|\alpha|} \tag{19}$$

Hence, if the attenuation is of the order of 1 dB per section of line, then the maximum gain will occur with $-1/\ell n(0.89) \cong 8$ devices. Furthermore, Eq. (18) indicates that the maximum gain will only be 2.8 times the gain of one device. Clearly, to achieve high gain, one must cascade stages, each of which has its transistors constrained by Eq. (19).

When input line and output line attenuations are not equal, the expression corresponding to Eq. (19) is somewhat more comlicated, viz:

$$n = \left(\frac{1}{\ell n|x|}\right)\left\{\ell n|\ell n(\alpha_2)| - \ell n|\ell n(\alpha_1)\right\} \tag{20}$$

where $x = \frac{\alpha_1}{\alpha_2}$. The conclusion, however, is clear; the number of devices per stage is controlled by the attenuation of the lines. This attenuation is caused by MESFET dissipative loading, and this loading must be minimized if high gain wideband amplifiers are to be realized.

When the loss is small but non-negligible, Eq. (17) may be written as

$$A = \sum_{p=1}^{n} \frac{g_m\sqrt{R_{01}R_{02}}}{2} (\alpha_1)^p (\alpha_2)^{n-p+1} \tag{21}$$

and with the same manipulations as in section (a), Eq. (21) becomes

$$A = \sum_{p=1}^{n} \frac{f_0}{2f_c} (\alpha_1)^p (\alpha_2)^{n-p+1} \tag{22}$$

For m stages, the amplifier gain will, of course, be

$$G = A^m \tag{23}$$

Now, Eqs. (20), (22), and (23) become the proper design equations. For a given loss, Eq. (20) determines the number of devices per stage; then, for a given device and desired bandwidth, Eq. (22) yields the stage gain. Finally, Eq. (23) determines the number of stages which must be cascaded to yield a desired amplifier gain.

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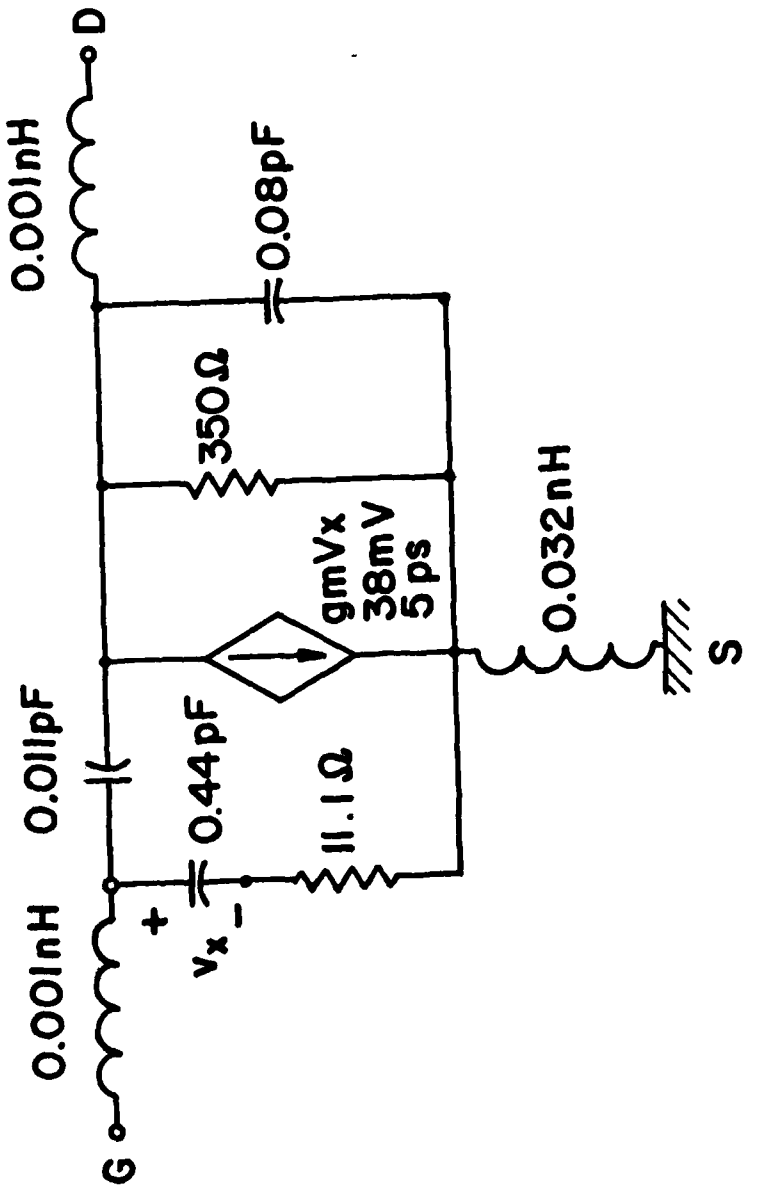
III. COMPACT COMPUTER ANALYSIS

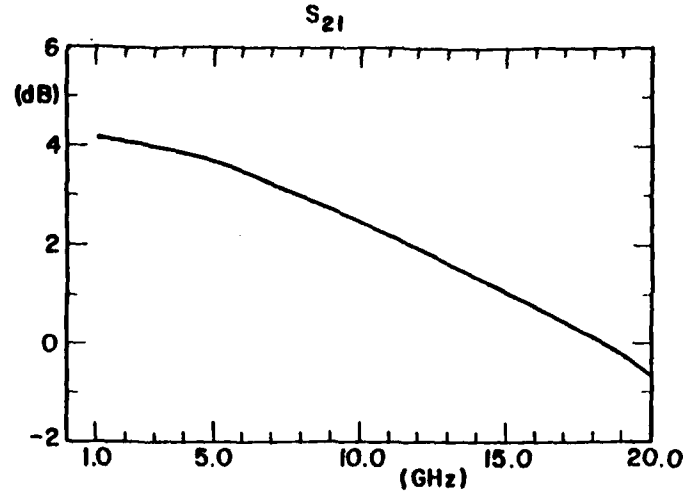
In order to determine the effect of using realistic transistor models, it was decided to design two amplifiers following the idealized analysis of Section II(a), and to observe the results using a COMPACT computer program with the optimized Texas Instrument 300 μ MESFET shown in Fig. 2, inserted in place of the idealized transistors. The two circuit designs which were analyzed were designed to provide overall gains of 8 dB for the two-stage, 4-transistor amplifier and 15 dB for the 6-transistor, two-stage amplifier. The design was intended to provide gain to at least 30 GHz; however, the transistor model probably is not valid above 20 GHz so the analysis was limited to below 20 GHz for this reason. The results are shown in Figs. 3 and 4.

It is of interest in these plots to note the slow gain decrease with frequency as well as the low gain. It is of particular interest to see the fit of these curves to the predicted performance when the line attenuation is considered. The plot in Fig. 5 is the transmission loss of the drain line alone as used in one stage of the two-stage transistor amplifier. Using these results and assuming the losses to be equally distributed among the transistors, the overall predicted gain of one stage now becomes 2.5 dB at 2 GHz or ≈5 dB for the complete amplifier. This is in reasonable agreement with the computer model. At 20 GHz, the gain should be 4.28 dB per stage or ≈9 dB overall, which disagrees with the model. When the losses in the input line



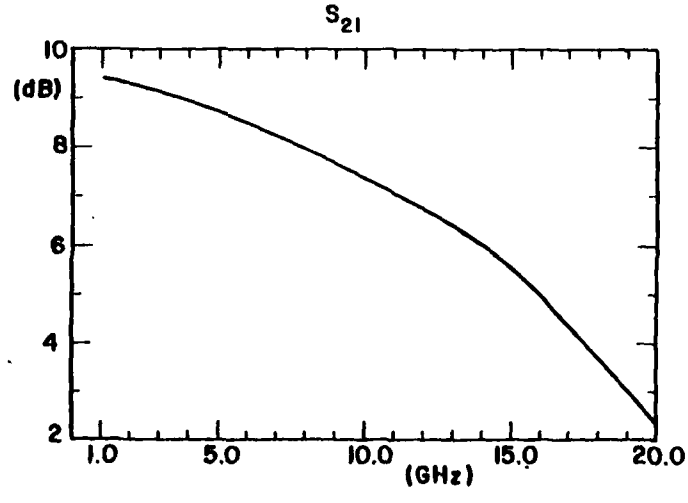
OPTIMIZED MODEL FOR TI - 300μ GaAs MESFET.

Fig. 2



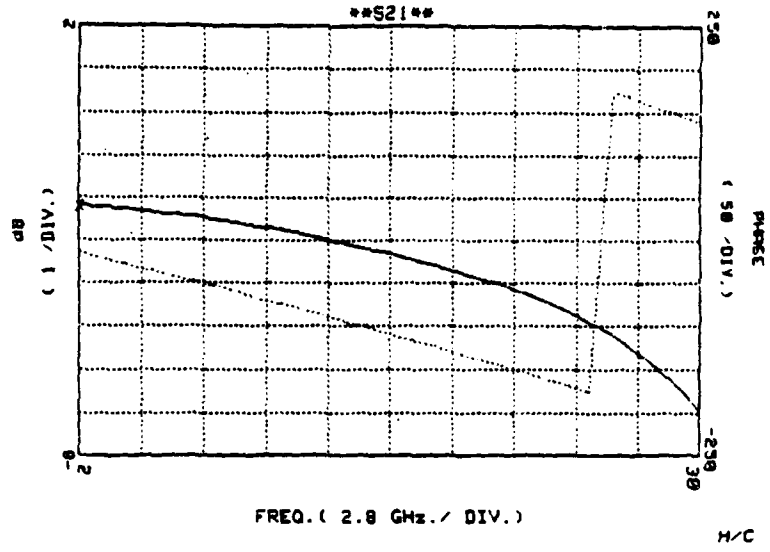
S_{21} FOR TWO CASCADED AMPLIFIERS OF 2 TRANSISTORS EACH

Fig. 3.



S_{21} FOR TWO CASCADED AMPLIFIERS OF 3 TRANSISTORS EACH

Fig. 4.

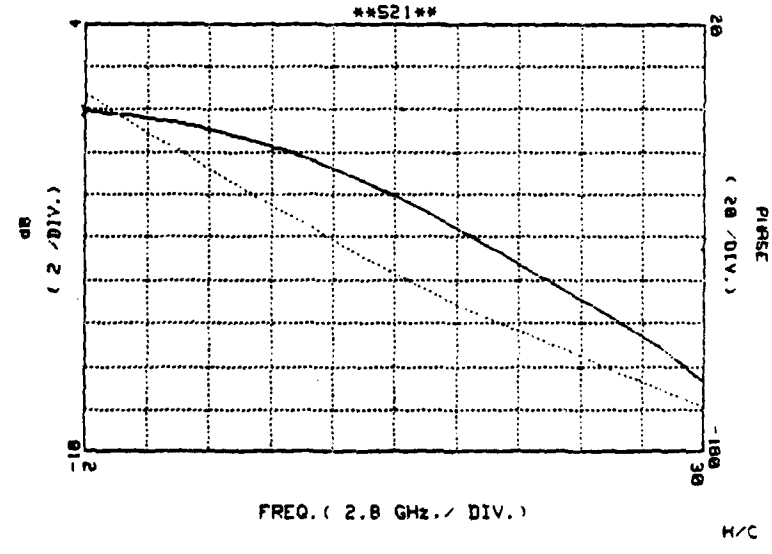


••• Phase

___ Amplitude

Drain line transmission loss (3 sections; T-section)

Fig. 5.



••• Phase

___ Amplitude

Gate line transmission loss (3-sections; T-section)

Fig. 6.

shown in Fig. 6 are taken into account, the amplifier shows a 20 GHz gain of ≈0.84 per stage compared to a 0.3 dB loss per stage shown by the model. This is in reasonable agreement and indicates the importance of line loss considerations.

Considering only drain line losses for the 6-transistor amplifier, at 2 GHz, the gain equation predicts 10.5 dB (versus 9.4 dB for the model) and at 20 GHz, it predicts a gain of 9.8 dB (versus 2.3 dB for the model). From this, it is apparent that gate line losses are indeed as significant as first anticipated, and additional investigation into the behavior of the input and output transmission lines is in order. In the next two sections, a report on the preliminary consideration of these problems will be given. In the follow-section, transmission line effects for a given transistor will be analyzed, and following that, the problem of choosing the optimum transistor will be addressed.

IV. ADDITIONAL DEVICE EFFECTS

The presence of dissipative elements in the MESFET device model not only causes attenuation, as has been discussed at some length in preceding sections, but in fact also dictates a preferred line topology. By examining Zobel's equations[9] for constant-k filters with parallel R-C shunt elements, one sees that the T-section line exhibits a resonant behavior, while no such behavior is present in the π-section line. These results are shown in Figs. 7 and 8 for the frequency range 20 to 30 GHz. Also shown are the results for three sections of line in tandem. It is clear that the T-configuration is the preferred topology for amplifier layout when losses are present, as the impedance is more nearly constant over wide bandwidths.

For the cases under consideration, the Texas Instrument 300 μ gate width device has been selected. Typical drain parameters put R_{ds} = 380Ω, C_{ds} = 0.08pF. For a 100Ω transmission line, L = .910 nH, which may present fabrication problems, but is adequate for study. Computer simulation of three sections of this line indicate a total loss of 3.1 dB at 2 GHz, rising to 4.5 dB loss at 20 GHz. Unlike the impedance analysis for this line, the analytical expressions for drain line losses do not fit computer simulation data very well.

Reducing the drain line impedance will reduce losses, but the gain decreases faster than the losses. Tapering the drain line impedance, as suggested by Ginzton, should

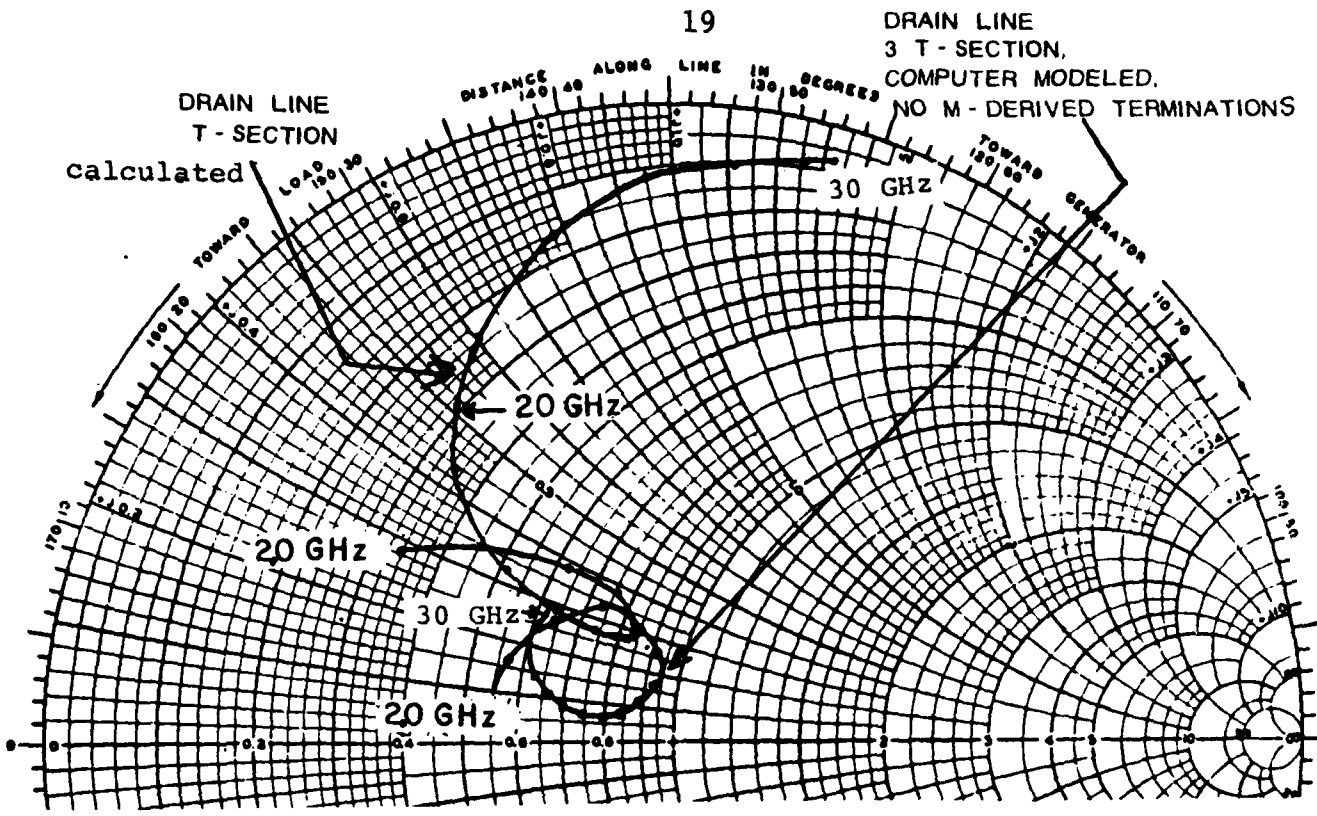


Fig. 7 Drain Line Impedance

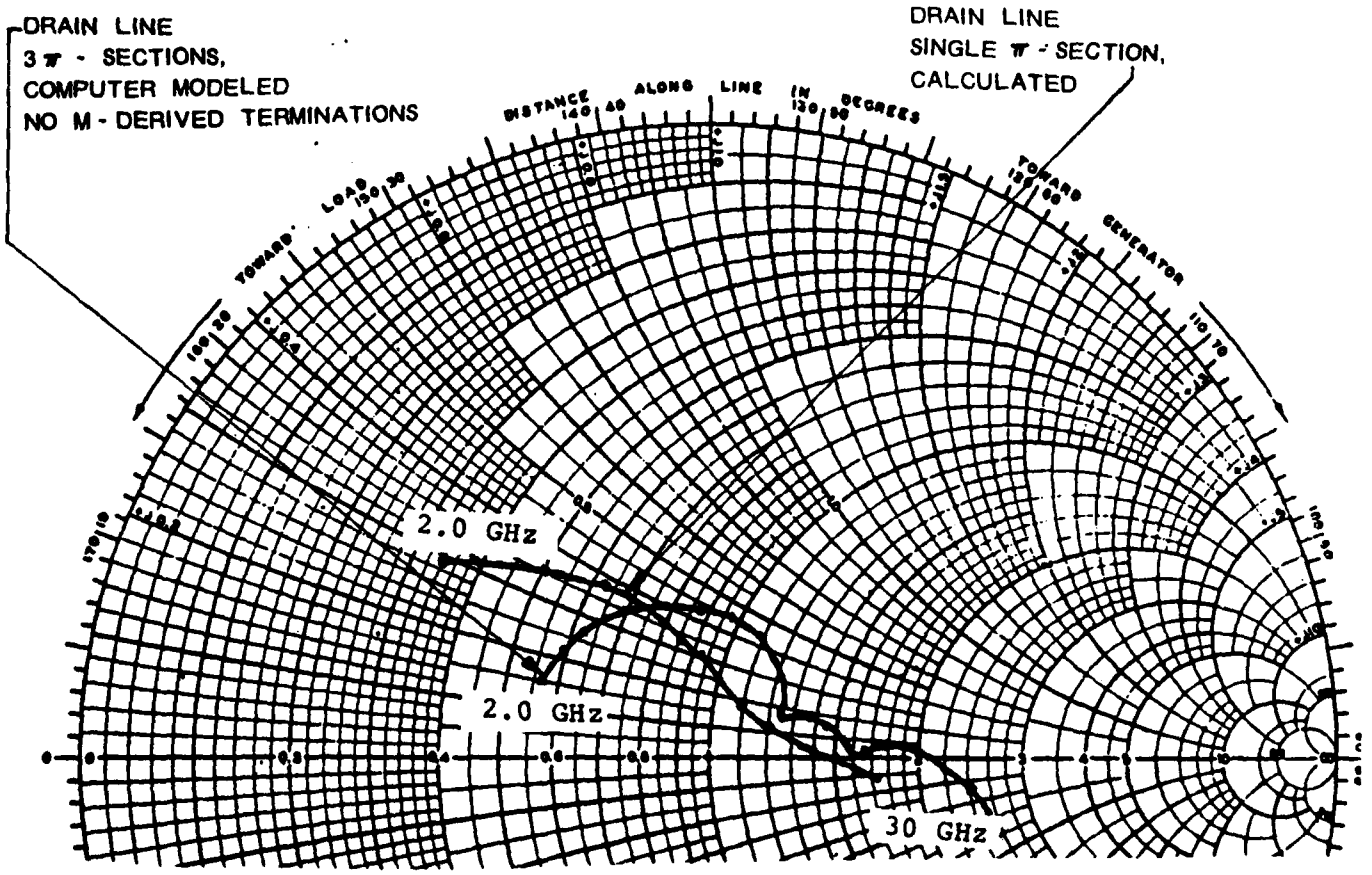


Fig. 8 Drain Line Impedance

result in a 3 dB improvement in overall gain, although the tapered impedance reduces the gain compared to an untapered, lossless line.

Similar significant losses occur in the gate line. Examining Zobel's equation for constant-k transmission line dispersion, one finds for the line section model with $L_1/2$ Henrys of inductance for the series elements and a shunt branch consisting of R_2 and C_2 in series that

$$\gamma = \alpha_s + j\beta = \cosh^{-1}\left[1 + \frac{j\omega L_1}{2\left(R_2 + \frac{1}{j\omega C_2}\right)}\right] \tag{24}$$

as the defining equation. In the absence of losses,

$$\gamma = \cos^{-1}\left[1 - \frac{\omega^2 LC}{2}\right], \tag{25}$$

which is purely imaginary for $f \geq \frac{1}{\pi\sqrt{LC}}$, the cutoff frequency of the line. For the 300 μ Texas Instrument MESFET, using an 18Ω gate transmission line (i.e., L = 0.168nH, C = 0.42pF, and R = 11.1Ω), this equation predicts a loss of .66 dB/section at 10 GHz, and 5.08 dB/section at 30 GHz. This is an excellent agreement with computer simulated data, and shows the significance of the FET input resistance in attenuating the signal on the line.

As has been shown previously, the presence of such severe losses as 5 dB/section of line constitute a major stumbling block for distributed amplifiers by placing definite limits on the number of active devices one may use. The gate line losses can be minimized by shunting with a capacitor. However, significant reductions in loss are

again exceeded by a greater reduction of gain, precluding any hope of improving performance using this technique.

Another factor of importance in distributed amplifier design which results from consideration of a more realistic transistor model is the Miller effect capacitance resulting from C_{gd}. The first device in a stage will experience an input capacitance of

$$C_{IN} = C_{gs} + C_{gd}\left(1 + \frac{g_m R_{02}}{2}\right) \tag{26}$$

where $\frac{g_m R_{02}}{2}$ is the "forward wave gain" of the device. This forward wave, however, grows as it progresses down the line, and hence subsequent devices experience a greater potential difference betweeen gate and drain, and hence an enhanced Miller effect. The greatest effect would occur for lossless lines, and the resulting input capacitance of the n^{th} device would be

$$C_{IN} = C_{gs} + C_{gd}\left(1 + \frac{n g_m R_{02}}{2}\right) \tag{27}$$

Since typically C_{gd} is an order of magnitude smaller than C_{gs}, the effect is rather small; However, depending on the device g_m and the number of devices per stage, it may have to be compensated for by adding capacitance to earlier devices in order to keep the characteristic resistance of the gate line constant.

The effect of C_{gd} on output capacitance is more pronounced due to the similarity of the magnitude of C_{gd} and C_{ds}. It is also more complex, as the effect is frequency dependent. Here,

$$Y_o = j\left[C_{ds} + C_{gd} - C_{gd}\frac{\omega^2}{\omega + \omega_p^2} + g_m\frac{\omega_p}{\omega^2 + \omega_p^2}\right]$$

$$+ g_m\frac{\omega^2}{\omega^2 + \omega_p^2} + \frac{^2pC_{gd}}{\omega^2 + \omega_p^2};\ \omega_p = \frac{1}{R_oC_{gd}} \tag{28}$$

which makes

$$C_D = C_{ds} + C_{gd} - C_{gd}\frac{\omega^2}{\omega + \omega_p^2} + g_m\frac{\omega_p}{\omega^2 + \omega_p^2} \tag{29}$$

and

$$G_D = g_m\frac{\omega^2}{\omega^2\omega_p^2} + \omega^2\frac{\omega_pC_{gd}}{\omega^2 + \omega_p^2} \tag{30}$$

where R_0 is the input line impedance (assumed to be pure real), C_D is the FET effective output capacitance for the common source configuration, and G_D is the effective conductance of the drain for the same configuration. For most cases, ω_p is one order of magnitude greater than ω, and thus, the frequency dependence of C_D may be insignificant; However, C_{gd} cannot be ignored when considering the output line shunting capacitance.

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V. DEVICE MODELING AND OPTIMIZATION OF DEVICE CONFIGURATIONS

In the preceding sections we have looked at the problem of optimization of amplifier performance using a given active device by varying circuit parameters such as line impedance and topology. We now consider the problem of finding the best device for given circuit constraints.

Any contemplated wide band distributed amplifier configuration is sufficiently complex to require a computer aided design. This, then, requires suitable circuit models for MESFET's and interconnections. Some effort was made to investigate existing GaAs FET models. It became evident that although models created from an analysis of device physics are very valuable in establishing a circuit configuration and a relation between circuit parameters and physical structure, reasonably accurate parameter values are obtained only through direct measurement on finished devices. In order to design a monolithic circuit, it then becomes necessary to begin with measurements on discrete devices. This, of course, is also difficult because of the probable differences in parasitic elements in the two cases. These differences are particularly important for a wideband design because the form of the circuit as well as parameter values may be different.

The modeling problem for devices in the distributed amplifier, then, has two main parts—selection of a suitable circuit configuration and selection of suitable parameter values. One way to minimize the labor on the first part

is to choose a very complicated circuit such as that of Fig. 9. Because of the large number of nodes which would appear in a distributed circuit using these device "elements" and because of the uncertainty and difficulty in selection of parameter values, this approach to the design amounts to a very expensive, time consuming way to show possible feasibility of a particular amplifier configuration. Since we are initially interested in understanding the limitations posed by real devices on the behavior of distributed amplifiers, we have decided to approach the problem using as simple a model as possible. The distributed circuit of Fig. 10, with suitable selection of parameters, allows the study of the effect on gain and frequency response of input circuit loss, output circuit loss, mismatch of phase velocities between lines, mismatch of load resistances, and combinations of these imperfections. Two parallel efforts have been started using this basic circuit configuration. The first, which is described in Sec. III, involves a computer solution of previously proposed multistaged amplifiers using typical parameters of devices made by Texas Instruments. The second effort is an attempt to ascertain the relative importance of the above mentioned imperfections, and from these results try to specify ideal device dimensions, device numbers and layout.

To date we have considered only the effects of loss in the transistors. As is evident from Eq. (17), loss on input and output lines have very similar effects. However, if the input line loss dominates, the devices on the signal end of the lines contribute most to the gain, while if the output line loss dominates, the devices near the load contribute

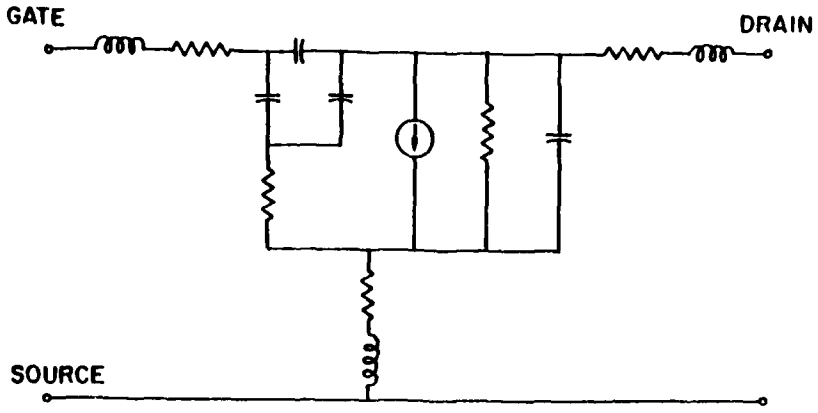

Fig. 9.

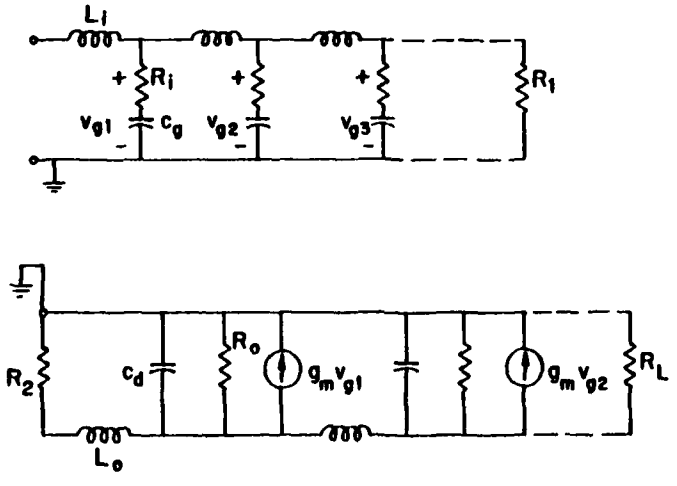

Fig. 10.

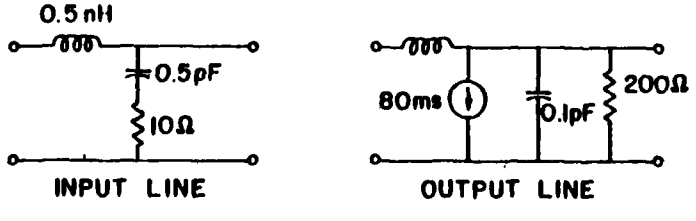

Fig. 11.

more heavily. Another significant difference is that because a series RC branch is involved, the value for α_1 tends to be more frequency dependent than α_2.

For example, consider the circuit values shown in Fig. 11. These are reasonable values for a 300 μm GaAs FET. The damping constant on the input line is

$$\alpha_{s1} = \omega^2 \sqrt{L_1 C_1}\, R_i C_i (4 + \omega^2 R_1^2 C_1^2)^{-1/4} \approx 0.048 \text{ nepers/section} \qquad (31)$$

at 10 GHz. The damping on the output line is about

$$\alpha_{s2} \approx \omega\left(1 + \frac{G_2^2}{\omega^2 C_L^2}\right)^{1/4} \sqrt{L_2 C_2}\, \frac{1}{\sqrt{1 + \dfrac{4\omega^2 C_2^2}{G_2^2}}}$$

$$\approx .063 \text{ nepers/section} \qquad (32)$$

at 10 GHz. Therefore, the transistors on the load end contribute slightly more heavily to the gain. At 20 GHz, $\alpha_{s1} \approx 0.17$ nepers/section and $\alpha_{s2} \approx .062$ nepers/section. The input α_s increases fairly rapidly and the relative contributions of the transistors change.

The above example suggests that loss in the drain circuit line may be a significant contribution to gain limitation in a distributed amplifier. This loss is controlled by the drain-source saturation resistance. There appear to be at least two ways to increase this resistance. The first is to use transistors with longer gates. This also increases C and decreases g_m, but because we can match C with the correct external L, and because it is not necessary to maximize

the gain per device, this possibility deserves further study. A second technique is to decrease the bias to a flatter portion of the output volt-ampere characteristic. This reduces g_m somewhat and also reduces the available voltage swing per device. Again, this may be acceptable. In fact, a bias variation along the line might be in order. The devices at the load end must handle a larger voltage swing but are less affected by the loss in the output line. Some volt-ampere curves published by Texas Instruments exhibit an apparent horizontal and even negative sloped portion. This may be only a heating effect but it will be investigated further as a possible bias region.

Loss in the gate line is perhaps more important. It is particularly troublesome because of its strong frequency dependence. This loss is due primarily to the gate metallization, the parasitic source resistance in series with the channel, and a difficult to calculate, channel resistance. They are all of comparable magnitude in microwave FET's. It may again be advantageous to use longer gate devices. This will reduce the gate metallization resistance. However, the other two resistances may, in fact, increase. Another possibility is to use different transistors on the signal and load ends. This could be used to compensate the total gain for the change in α_{sl} with frequency. Different gain devices could be automatically selected at different frequencies as α_{sl} changed.

TABLE I

TRANSMISSION LINE LOSS PER SECTION FOR SELECTED MICROWAVE MESFET's

	C_2(pF)	C_1(pF)	R_1(Ω)	α_{s1}	f	R_2(Ω)	α_{s2}	g_m(MS)
TI (300 μ)	.1	.5	10	.0476	(10GHz)	400	.0636	40
				.103	(15GHz)		.0630	
				.173	(20GHz)		.0628	
HP (500 μ)	.16	.5	10.3	.078	(10GHz)	192	.134	43
				.168	(15GHz)		.131	
				.283	(20GHz)		.131	
IBM (400 μ Si)	.05	.47	29.5	.054	(10GHz)	667	.0384	17
				.100	(15GHz)		.0379	
				.145	(20GHz)		.0377	
Avantek (500 μ)	.06	.4	17.2	.038	(10GHz)	500	.0514	32
				.0798	(15GHz)		.0507	
				.130	(20GHz)		.0504	
Fairchild (300 μ)	.04	.25	18.3	.0175	(10GHz)	400	.0664	20
				.038	(15GHz)		.0650	
				.0646	(20GHz)		.0641	
Nippon Electric (300 μ)	.16	.35	10.3	.0558	(10GHz)	600	.0417	18
				.123	(15GHz)		.0417	
				.212	(20GHz)		.0417	
Varian (600 μ)	.2	1	7.6	.138	(10GHz)	450	.0558	42
				.286	(15GHz)		.0557	
				.460	(20GHz)		.0556	
TI (300 μ)	.09	.41	11	.039	(10GHz)	350	.0733	38
				.0845	(15GHz)		.0723	
				.143	(20GHz)		.0720	
TI-75, extrapolate (scale) from 78Bi-55I$_c$	.0225	.103	44	.00976	(10GHz)	1400	.0183	9.5
				.0212	(15GHz)		.0181	
				.0361	(20GHz)		.0180	

Using published equivalent circuit data, the values for α_{s1} and α_{s2} were calculated for a number of transistors fabricated by different manufacturers. The results are shown in Table I. The calculation was made after fixing the characteristic impedance of the output line at 50Ω and requiring that $\sqrt{L_1C_1} = \sqrt{L_2C_2}$. No attention was paid to the practical problem of obtaining the necessary values for L_1 and L_2 in the real circuit. The device with a 75 μm wide gate is not real. It was merely presumed that the multi-fingered 300 μm device from Texas Instrument could be scaled.

In all the devices, α_{s1} increases by a factor somewhat less than ω^2 between 10 GHz and 20 GHz. The value of α_{s2} remains almost constant with frequency. In most cases, α_{s1} dominates at 20 GHz and it is a major limitation at higher frequencies.

We have in Sec. II(b) found the optimum number of transistors of a given type for a given line loss for maximum gain. (This loss, in fact, depends strongly on the transistor type.) Consider now the question of how many transistors should one use for maximum stage gain if the devices are allowed to each become smaller so as to reduce the loss. From Eqs. (31) and (32), one sees that for fixed line impedance level, the attenuation constants decrease with decreased transistor gate width, since C_1 and C_2 will both decrease, and the R_1C_1 and C_2/G_2 products will remain constant to first order. Hence, as the transistor is scaled down, so is α_s but, of course, g_m is likewise reduced. For the Texas Instruments transistors shown in Table I, the assumed relationship is

$$g_m = K\alpha_s = -K \ln|\alpha| \tag{33}$$

when K is of the order of unity or less. Equation (17) can be used with typical device parameters to calculate expected maximum gain values with the number of transistors constrained by Eq. (19). To date we have done this only for the special case of $\alpha_{s1} = \alpha_{s2}$, (Eq. (18)), and the output line impedance held at 50Ω. Under these conditions, Eq. (18) constrained by Eq. (19) becomes

$$A_{max} = 25e^{-(\frac{n+1}{n})} \tag{34}$$

Figure 12 shows Eq. (34) for the maximum stage gain as well as Eq. (19) which relates n and α. One notes that as the gate width is reduced, g_m decreases and the number of transistors for maximum gain increases through Eq. (19). In addition, one also sees that as the number of transistors increases the maximum stage gain approaches an asymptote, and there is little benefit in gain of using more than 5 to 10 transistors per stage. The bandwidth, however, will continue to increase as the devices get smaller and more numerous, since C_1 and C_2 will both continue to decrease. For fixed R_0, then L_1 and L_2 must also decrease, and hence, the cutoff frequency increases as seen from

$$f_c = \frac{1}{\pi\sqrt{LC}}.$$

In terms of bandwidth, the limit, of course, is a completely distributed transistor with a theoretical cutoff frequency of infinity. The practical limitations of this approach include not only problems with fabrication of correct inductances but the frequency dependence of α.

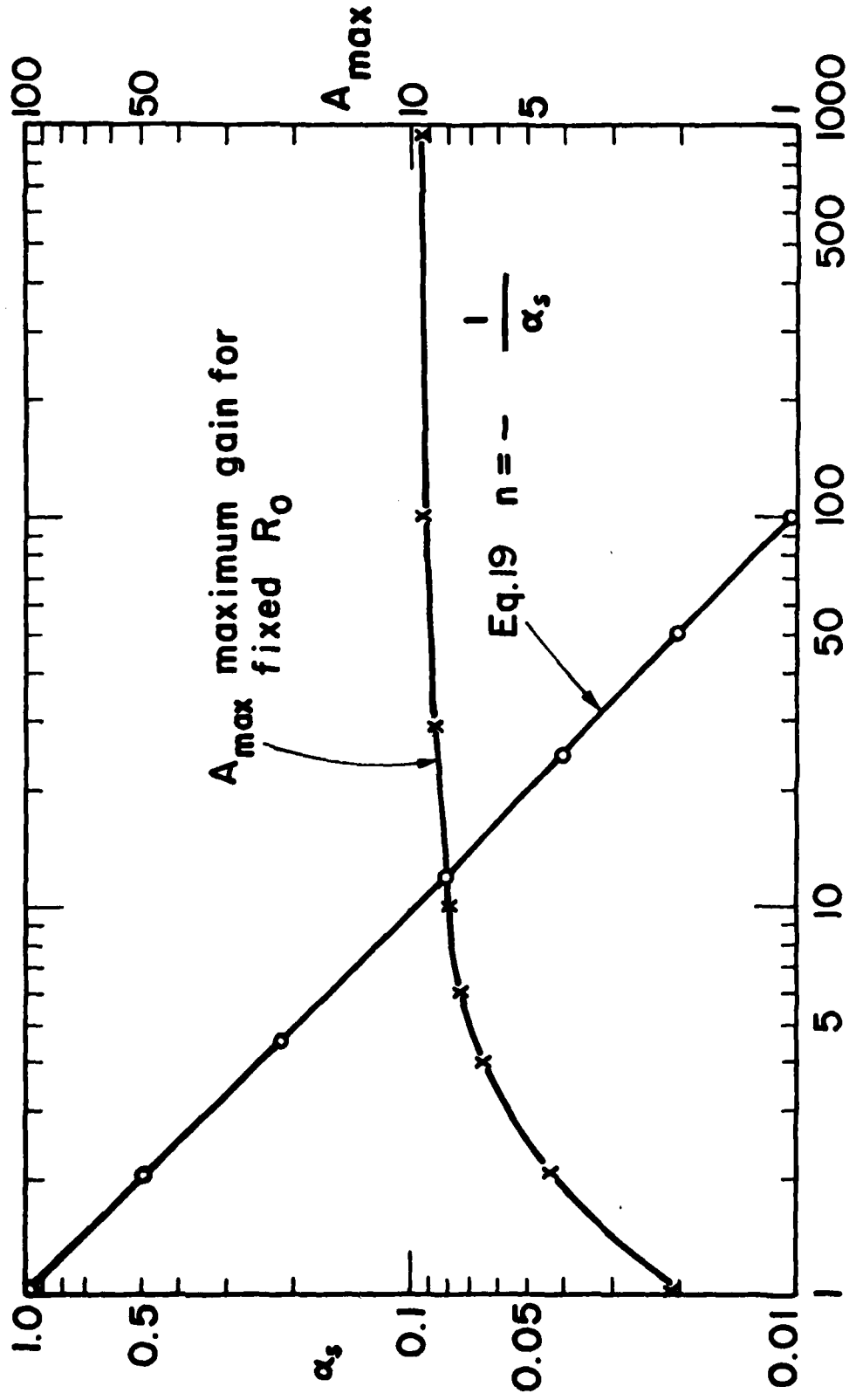
100
50
A_{max}
10
5
1
1000
500
100
50
10
5
1
n
1.0
0.5
0.1
0.05
0.01
α_s
A_{max} maximum gain for fixed R_o
Eq.19 $n = -\frac{1}{\alpha_s}$

Fig. 12

One can also determine from the plot of Eq. (19) the approximate device size. For example, if m = 10, $\alpha_s \approx$ 0.1 and the device must be larger than 300 μm. For n = 100, $\alpha_s \approx$ 0.01 and the device is now smaller than 75 μm.

VI. AIR BRIDGE MEASUREMENTS

MMIC topology demands the use of air bridge lines especially if balanced devices are used. Since it is essential to know the phase velocity on, and characteristic impedance of, such lines in order to design interdevice inductors, we have recently begun an experimental measurement program to obtain such information. Measurements are being made using an HP8410 network analyzer which has an upper frequency capability of 18 GHz.

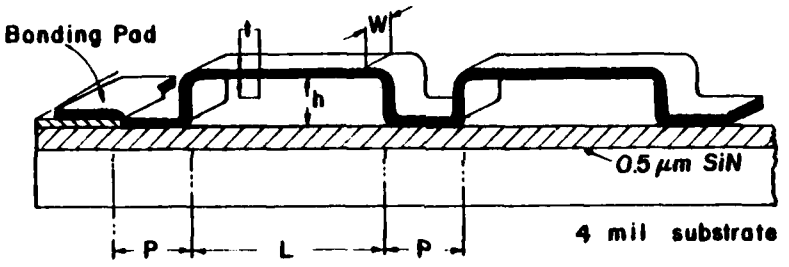

Fig. 13

Figure 13 shows a typical section of air bridge line as fabricated for us by Texas Instruments. Values for the "island" length, P, range from 12 to 24 μm, with span length, L, ranging from 50 to 125 μm. The height of the bridge is 1 μm. Because of this close proximity, the impedance of the air sections is very near to the impedance of a microstrip of the same size, which results in nearly uniform transmission lines with negligibly small added capacity due to these islands. Thus, one expects the periodic loading effect of the capacitive islands to

be negligible. This would not be true if the bridge height were more nearly equal to the substrate thickness.

Initial measurements of these lines have been inconclusive. Consider a line of L = 50 μm, P = 12 μm, thickness t = 2 μm and width 10 μm. Calculating the microstrip inpedance of a 10 μ wide strip over a dielectric equivalent to the air-GaAs combination, we find Z_o = 107Ω. For the microstrip on GaAs, the impedance is 101Ω. Measurements on a 2400 μm length sample of this air bridge line indicate a reflection minima at 16 GHz which indicates either λ/2 resonance or strong absorption. Transmission loss at 16 GHz is ≈ -.6 dB, ruling out absorption. Using Court's equations[10] for transmission loss and line impedance, α = 0.935 and $|\rho|$ = 0.123, indicating a 64Ω line. This is a rather serious discrepancy. Clearly, a transmission maxima would have been a preferred point to choose, but for lines near 50Ω, these maxima are not always significant.

Currently, efforts are being made to improve the accuracy of our measuring system, with particular emphasis on enhancing the accuracy of line impedance measurements near 50Ω. This is particularly important for calculating α, as it currently is calculated as a small difference between two large numbers.

REFERENCE

10. Court, R.A., "Determination of the Parameters of Microwave Transmission Lines from Transmission and Reflection Measurements," IEEE Trans. on Instrumentation and Measurement, IM-26(4), 419, 420, December (1977).

VII. SUMMARY, CONCLUSIONS, AND PRESENT EFFORTS

For the sake of clarity and future reference, the material in preceding sections has not been presented in chronological order. In fact, our original computer model investigations of distributed amplifiers using realistic transistor models led us to examine the cause of gain taper, and reduced gain and bandwidth, over that predicted by our simplified theory. While we have investigated many aspects of this problem, we feel that our most significant finding is the relationship of line loss to the expected gain and number of devices. Of particular interest are the results of scaling in Section V. Data available to us from Texas Instrument on their 1200, 900, 600, and 300 micron transistors indicate that, in fact, the input and output time constants do not scale and may change to our advantage if the gate width is reduced. If this turns out to be true, the predictions of Fig. 12 are somewhat pessimistic, and we should be able to achieve the desired gain and bandwidth with fewer active devices. As mentioned previously, Fig. 12 represents an idealized case with input and output line attenuation equal and $R_o = 50\Omega$ for both lines. These conditions were used to show the trend as device size was reduced. In a realistic case, the attenuation cannot be the same on both lines except at one frequency and holding $R_o = 50\Omega$ for both lines may require unrealistic inductor sizes or the addition of capacitance

to keep the phase velocities equal. The main effect of relaxing these restrictions will be on the value of absolute gain obtainable, and the nature of the curve in Fig. 12 should change very little. We now intend to look at these effects in detail as they affect broadband amplifier performance.

Our immediate goal is to design and have fabricated for testing a series of multi-device stages. However, since working computer models are essential first, we will continue to solve the problems we have identified so far. Hence, we plan to make computer studies with narrower gate width devices to test the theory of Section V. We will also look at the effect of longer gate length and choice of bias point to increase drain resistance as well as fabrication techniques to reduce series gate resistance. We will study the use of different devices within a stage to compensate for gain taper and Miller effect. We also plan to examine the distortionless line concept versus an equalizer in the drain line to compensate for gain taper. In addition, we will also investigate the use of m-derived terminations for increasing the useful bandwidth. We will also continue to make measurements on air bridge lines both because the data itself is needed and because the perfection of measurement technique is needed so that we will be able to measure the amplifiers when they are available.

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