QUARTERLY TECHNICAL REPORT 4

ON THE

EARTH STATION INTERFACE

FOR

DEMAND ASSIGNMENT APPLICATIONS

FOR THE PERIOD 10/01 THROUGH 12/31

Sponsored by:

Defense Advanced Research Projects Agency

ARPA Order Number 3674/5

and

Defense Communications Agency

Contracting Agency: DSSW

Contract Number MDA903-81-C-0638

Effective Date of Contract: 81 SEP 08

Expiration Date of Contract: 82 DEC 31

JOHN E. McCORMICK
Program Manager
(714) 457-2340 x644

"The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the U.S. Government."

LINKABIT Corporation
A M/A-COM Company
3033 Science Park Rd.
San Diego, CA 92121

The principal effort during the fourth quarter of calander year 1981 was scheduled rework, updates and system integration of the ESI Advanced Development Models. During this time, very few technical developments were made; however, one step taken late in the quarter was to define the approach for test fixtures used with the digital circuit boards. This report presents a technical overview of the design philosophy.

Technical Overview of the ESI Test Fixtures

An early objective of the ESI follow on program is to create a series of test fixtures suitable for testing the circuit card assemblies (CCA's) undergoing redesign on the same project. The problem then is to create a test fixture which can be designed and constructed while the CCA design itself is being brought to maturity. One advantage the ESI program enjoys is the fact that previously built ADM versions of the CCA's have defined the generic requirements so the redesign efforts on them represent enhancements and improvements rather than total restructuring of input and output characteristics.

The method decided upon utilizes a signature analysis technique. The architecture of the test fixtures is shown in Figure 1.

The tester architecture uses a 2K x M PROM to generate M input signals driving the CCA under test. A 2K x N PROM generates signals which would be expected from a properly operating CCA. The signals which actually return from the CCA under test, when it is driven by the M input signal lines, are compared to those

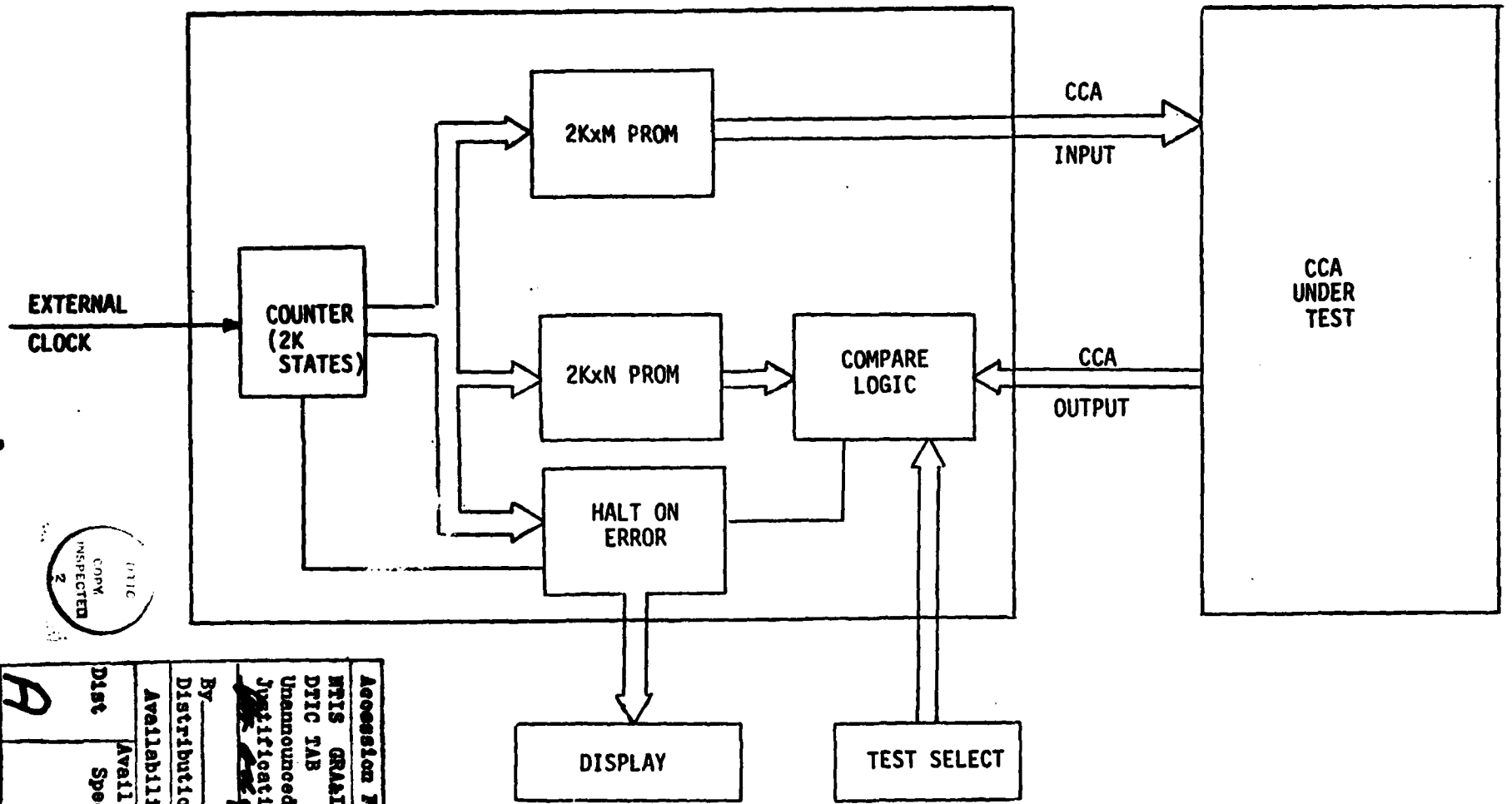

Figure 1. Test Fixture Block Diagram

stored in the 2K x N PROM and any errors are displayed. The sequence halts on an error to display the incorrect response.

The 2K x M input signals are grouped into separate sequences which allow major subsystems of the CCA to be tested in order to isolate any faults.

Several advantages can be cited for this approach. One is the fact that the majority of the circuit boards in the ESI (9 of 11) are digital in nature so the technique is widely applicable and provides a common design base. Since the detailed functional requirements reside within the PROM's, revisions can be accommodated with code changes rather than hardware changes. This allows the test fixtures and CCA's to be developed in parallel. The approach should go a long way to prevent test fixture obsolescence as the ESI matures in response to future network needs.

Summary

The signature analysis approach to the test fixtures should provide a good common design base along with excellent flexibility for accommodating future changes resulting from system level maturity.

The follow-on ESI program contains a number of enhancements such as Downline Loading capability, Upline Frequency Tracking, and Built-In Test, which will be incorporated as the Circuit Card Assembly designs progress. Future quarterly reports will discuss technical details and philosophy of those designs.