SPONTANEOUS OSCILLATIONS IN GALLIUM ARSENIDE FIELD EFFECT TRANSISTORS

H. L. Grubin

United Technologies Research Center, East Hartford, CT 06108, U.S.A.

D. K. Ferry

Colorado State University, Fort Collins, CO 80521, U.S.A.

and

K. R. Gleason†

Naval Research Laboratory, Washington, DC 20375, U.S.A.

Abstract—We present results of experiments and numerical simulations designed to reveal the presence of spontaneous oscillations arising from negative differential mobility effects in gallium arsenide field effect transistors. The measurements include d.c. and pulsed current/voltage vs temperature characterization, sampling scope measurements, spectral analysis to 40 GHz and observation of light emission. The simulation is a time dependent large signal transient analysis arising from a fully two-dimensional solution of the self-consistent potential and charge within the device.

1. INTRODUCTION

The gallium arsenide field effect transistor has been around a long time[1, 2] showing promise of delivering high power while sustaining low noise levels. GaAs is, however, subject to hot electron effects that manifest themselves in the presence of highly nonuniform charge layers or "domains". And depending on device size and bias values, these domains are either trapped near the gate or drain contacts[3], or propagate between them.

The presence of trapped high field domains is expected to profoundly affect FET performance and is currently subject to much study[4–6]. However, with the exception of early empirical studies[2, 7] and recent numerical studies[3, 8, 10], the dynamic properties of the propagating domain, the conditions for their existence, and their influence on device performance has until recently[11–14] been largely ignored. The renewed interest arises from a need to determine the extent to which the occurrence of spontaneous oscillations in GaAs FETs[11–14] are a consequence of negative differential mobility (NDM). In the following we discuss the influence of trapped and propagating domains on FET operation. We also present evidence for the *highly probable* conclusion that the propagating domain is the origin of our observation of spontaneous oscillations in GaAs FETs.

The study reported here is in two parts: (i) numerical simulation and (ii) experiment. The numerical studies reveal the presence of *two qualitatively different trapped domains and one traveling domain*. The first trapped domain forms within the conducting channel and at the drain edge of the gate contact.[4–6] Its formation is a direct consequence of velocity limitation in GaAs and its presence is responsible for current *saturation at values of drain voltage significantly below that predicted by*

Shockley[15]. The second trapped domain is qualitatively different and *forms in FETs capable of sustaining a current instability arising from (NDM).* This domain forms *near the drain contact, at high drain and low gate bias levels and is coincident with the cessation of oscillatory activity* in GaAs FETs. (The extent to which it is removed from the gate region depends on the gate to drain spacing and the doping concentration of the epitaxial region.) The domain is qualitatively similar to the *high anode field* configuration in two terminal devices, where it is also responsible, in many cases, for the cessation of oscillation[16]. Each of the low and high drain bias trapped domains may pulsate in time and so enhance the noise existent in the FET. In the case of the traveling domain, it, as for some transferred electron logic devices (TELD) is launched at the drain aide of the gate contact, propagates to the drain contact and then recycles successively. While the traveling domain need not be "stable" in the sense of two terminal NDM devices[16], its threshold and quenching conditions are similar to that for two terminal devices[3, 8].

The experimental studies reported below consist of pulsed and d.c. measurements performed as a function of temperature and under different circuit conditions. We have determined the spectral content of the oscillations when they occurred, and for pulsed measurements have sampled the current and voltage at different points within the pulse. The devices studied were empirically separated into two groups as determined by the ratio

$$K = \frac{\text{Gate voltage at cutoff } (= V_{co})}{\text{Drain voltage at the onset of current saturation } (= V_{ds})}.$$

(1)

Devices with K greater than unity sustained current

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†Present address: Textronix, Inc., Beaverton, Oregon.

oscillations; those with K approximately equal to or less than unity were electrically quiet. For those cases with K greater than unity oscillations began beyond the knee of current saturation. In each case the oscillations ceased at high values of drain and gate bias. In most of the electrically unstable devices the onset of the oscillation is marked by a drop in current. In all cases the instability appears to be initiated when the average field under the gate contact first reaches the NDM threshold field value. This result holds true under different ambient temperature conditions. An estimate of the carrier velocity in the channel between the gate and drain contacts indicates that prior to the oscillation the electrons are usually drifting at speeds in excess of the saturation drift velocity. When the oscillations ceased with increasing gate bias the carrier velocity dropped to values significantly below the saturation drift velocity. Each of the above results are consistent with an instability arising from the presence of negative differential mobility.

2. DEVICE CLASSIFICATION

The classification parameter K (see eqn 1) emphasizes differences between the GaAs and classical FET, where for the latter[15] V_{cc} and V_d are equal. For GaAs, the very earliest experiments[1, 2, 7] showed K varying from unity to values significantly higher than unity. (Current devices[17] have not altered this situation). In those experiments[1, 2] when $K \approx 1$, no instability was reported. When K was at the high end of the scale, the studies in Refs.[2] and [7] showed that the device no longer exhibited the classical characteristics, but instead sustained spontaneous oscillations for a range of bias values.

The results of the computer simulation corroborate the empirical classification. But, in addition relate stability to the material parameter v_s, the electron saturated drift velocity. Specifically, the simulations show that a necessary condition for a current instability is that the current at saturation either exceed or be within a narrow band about the value

$$I_s = G_0 E_s L. \qquad (2)$$

In eqn (2), G_0 is the open channel conductance (= Area/($L \times$ Resistivity)). $E_s = v_s/\mu$. L is the source to drain separation, and μ the low field mobility of the semiconductor. In two terminal device language, E_s is the sustaining field[16]. Summarizing: If IDDS denotes the zero gate bias current at saturation then

IDSS < I_s : Stable current-voltage characteristics
IDSS > I_s : Unstable current-voltage characteristics.   (3)

The above conclusion is essentially similar to that of Yamaguchi et al.[8].

The results discussed above summarize the general features of the GaAs FET. The space charge distribution within the FET is responsible for these properties and will be discussed in the next section.

3. LARGE SIGNAL DYNAMIC MODELLING OF THE GaAs FIELD EFFECT TRANSISTOR

3(a). Introduction

The following analysis is for devices in the configuration of Fig. 1(a) where the source and drain contacts are at parallel ends of the device. This configuration eliminates geometrical effects due to coplanar placement of the source and drain contacts. Coplanar contact calculations have been performed for the configuration shown in Fig. 1(b), which also include the presence of a substrate. And the results of these studies show injection into the substrate, with the instabilities still remaining. All of the calculations reported below are for elements with doping levels nominally equal to $10^{15}/cm^3$, a value approx. 1.5 to 2 orders of magnitude below that of presently fabricated devices. This choice was made because the cost of computing the contributions of transiting domains increases monotonically with increased doping level[18]. However, a number of representative calculations have been performed at higher doping levels with similar results. We note that the results of Yamaguchi et al.[8] were at $3 \times 10^{16}/cm^3$ and where there is overlap with our studies there is agreement. Also, the main results of the experiment confirm the conclusion developed at these lower doping levels.

3(b). Current voltage characteristics and space charge distribution for FET with $K \approx 1$

The space charge distributions for a $K \approx 1$ device are displaced in Figs. 2-4. The inset of each figure shows its current-voltage characteristic with the lower case letters keyed to the space charge distribution. The current is normalized to the value
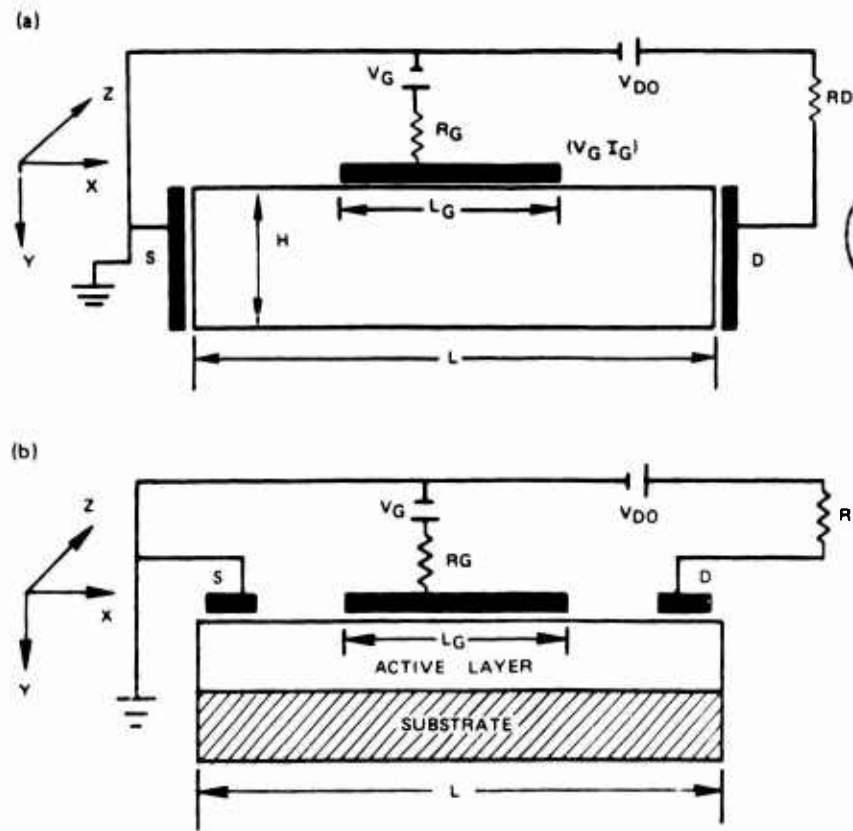
$$I_p = G_0 E_p L. \qquad (4)$$

where E_p is the electric field at peak velocity. And the voltage is normalized to

$$V_p = E_p L. \qquad (5)$$

The bold curve is the electron drift velocity electric field relation scaled to current and voltage. The closed circles denote computed points and each point is a stable time independent point.

For the space charge distribution the x-axis represents the longitudinal spatial dependence. The vertical charge distribution is along the y-axis. The source contact is in the y-z plane at $x = 0$; the drain contact is at $x = L$. The gate contact is in the x-z plane at the indicated points.

At low values of drain bias and zero gate bias (Fig. 2a), there is a region of charge depletion under the gate contact. The charge region spreads somewhat beyond the gate contact boundaries (enclosed rectangular parallelepiped), but pretty much the space charge distribution is what one would expect from classical arguments[15]. An increase in drain voltage to the knee of the current voltage relation (Fig. 2b) leads to a domain, representing the first significant departure from the classical analysis. The domain consists of an accumulation layer, which

Fig. 1. Device-circuit configuration used in the FET simulations. (a) Parallel source and drain contacts. (b) Coplanar source and drain contacts. Substrate is included.

forms within the boundaries of the gate region and is followed downstream by a depletion layer. Domain formation is a consequence of current continuity and velocity limitation and occurs when the current density under the gate exceeds

$$J_p = N_0 e v_p \qquad (6)$$

where v_p is the maximum carrier velocity. Further increases in drain bias result in an increase in the amount of charge accumulated and a broadening of the domain (Fig. 2c). We point out that while the presence of a domain is necessary for a current instability, it is not sufficient. By analogy with two terminal devices the current density downstream from the dipole must exceed the sustaining current, J_s, where

$$J_s = N_0 e v_s \qquad (7)$$

(see also eqn 2). This criteria is approximately satisfied for the FET but is not as stringent. It suffices to state that the current density for the $K \approx 1$ devices is generally too low to sustain an instability.

The calculations of Fig. 3 are for finite values of gate bias. At low drain bias levels the depletion layer extends well beyond the gate boundaries. We see a region of local charge accumulation, although clearly there is a net depletion of carriers. However, increasing the drain bias results in a strong region of charge accumulation, fol-

lowed by significant depletion until the drain contact is reached where the boundary conditions require a significant increase in the charge density.

Two extreme conditions are displayed in Fig. 4. Here at low values of drain bias and a value of gate bias near cutoff we see the presence of a depletion layer broadly surrounding the gate region. At zero gate bias levels but very high drain bias levels we see the presence of a region of charge accumulation extending from the gate region to the drain contact.

We summarize the above results by stating that for a collection of ostensibly classical current-voltage curves the space charge distribution is far different in many circumstances from that developed originally for the FET[15]. Thus while the current-voltage relation does not provide us with detailed information about the distribution of space charge for the $K \approx 1$ device, we expect that the form of the distribution will affect the equivalent circuit element representations of the device[4,5].

3(c). *Current voltage characteristics and space charge distributions for* FETs *with* $K > 1$

For a given doping level and source drain spacing, the principle difference between devices with $K > 1$ and $K \approx 1$ is that the former have wider channels, therefore, lower open channel resistances, and for a given bias draw more current. For these devices the current density is usually high enough to sustain an instability. *In our simulations the onset of the instability marked the onset*
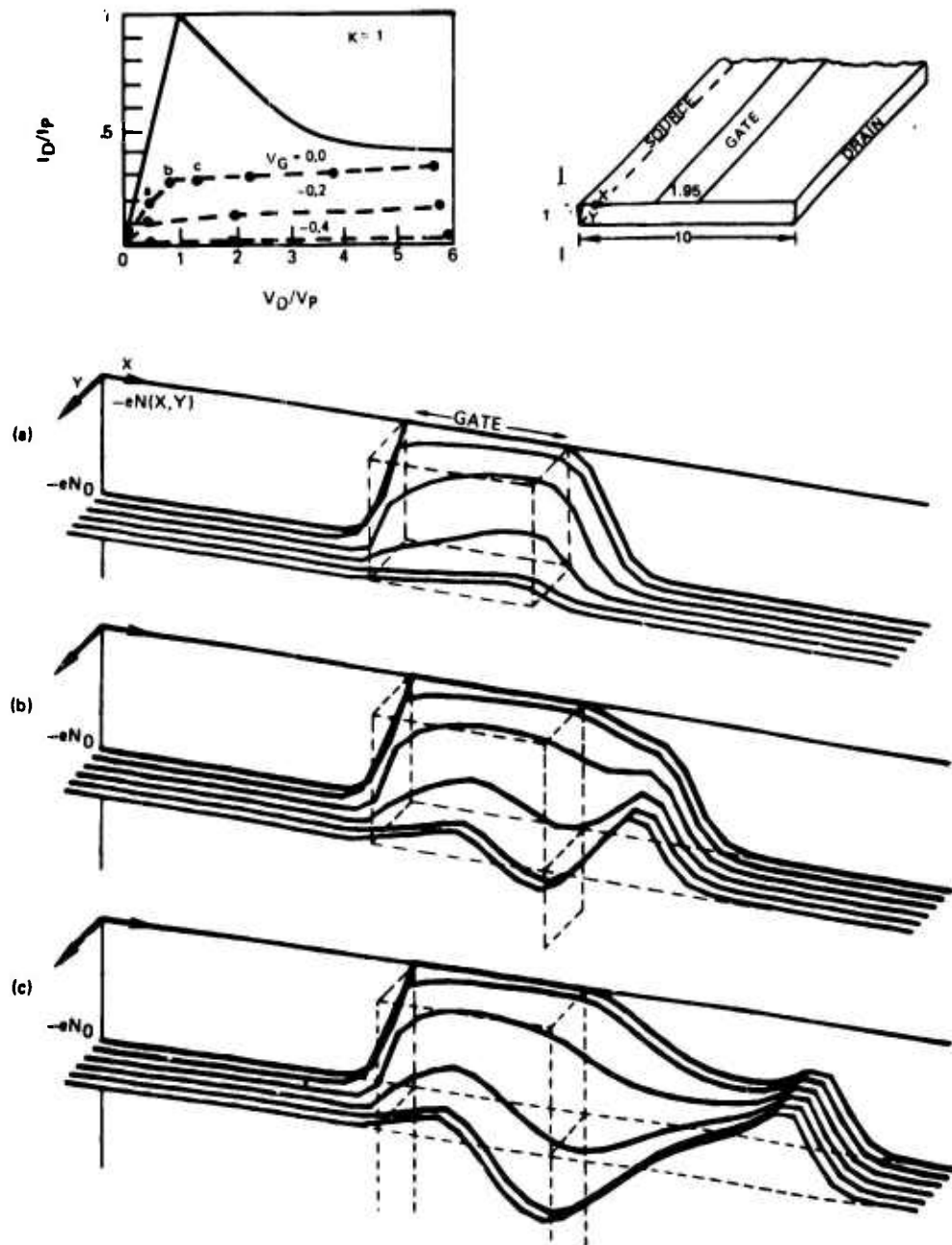
Fig. 2. Space charge configuration as a function of bias. Profiles correspond to indicated points on the current voltage characteristics. Solid line represents GaAs velocity vs electric field relation scaled to current and voltage. Device configuration is also shown, with dimensions in microns.

of current saturation. In our experiments, the instability occurs *after* the device enters saturation. The simulations for the wider channel device are displayed in Figs. 5 and 6.

Figure 5(a) shows the charge distribution at a bias level just below that necessary to launch a traveling domain. Within the gate boundaries there is charge depletion. But towards the bottom of the channel and just before the boundary there is a trace of an accumulation layer—implying that the current density is highest there. Coupling this result to the current value in the inset to Fig. 5, we have the result that within the gate boundary the current density is approximately equal to J_p, while within the gate-to-drain region the current density exceeds J_s.

The above conditions are sufficient to launch a domain in two-terminal devices, and indeed here a slight increase in drain bias results in the launching of a domain (Fig. 5b). In this case further increases in bias result in the charge accumulation layer spreading toward the bottom of the channel (within the gate boundaries) and also toward the drain contact. The domain detaches from the gate region and periodic transit time oscillations occur. Figure 5(b) shows a "snapshot" of the domain at one instant of time during propagation. (Recycling domains
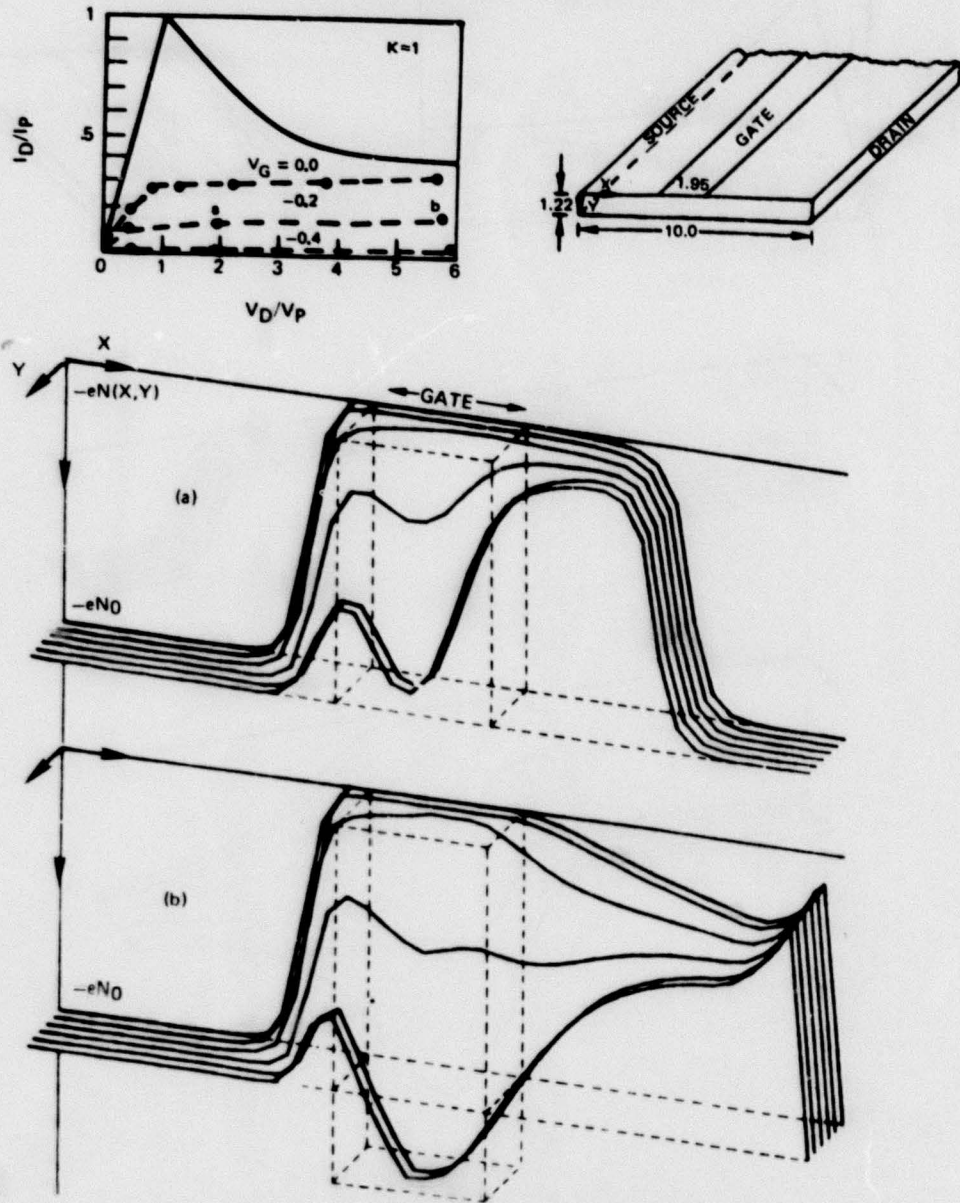
Fig. 3. As in Fig. 2, but for different bias values.

are illustrated in Fig. 5. Ref.[3].) The propagating and recycling domain can persist for a rather wide range of drain bias values. The amplitude of these resulting transit time oscillations are bias dependent as illustrated in Fig. 7.

Figure 7 contains plots of drain and source current vs drain potential at different times, with time eliminated between these. In Fig. 7(a) we plot drain current vs drain voltage for four different values of drain bias. The bold lines denote calculated results; the dashed lines are an estimate of the current vs voltage; the skew lines are the drain d.c. load lines. In each calculation displacement current contributions result in transient drain current values in excess of their steady state values. This is apparent for the bias levels of 1.4 and 1.6 V_p, where after steady state has been reached the displacement current

goes to zero and the system relaxes to the value denoted by the closed circle. When the domain is propagating the current oscillates along the load line. At a bias of 1.6 V_p the current oscillation amplitude is somewhere around 20% of its d.c. value. Further increases in drain bias result in an increase in the amplitude of the oscillation. The average current associated with these oscillations is denoted by the x's. *We note that the average-current-voltage relation for the range in which there are transit time oscillations, exhibits a region of negative differential conductivity* (NDC). *The NDC is, for these calculations dynamic in origin.* The second part of Fig. 7 shows the source current vs drain voltage for the same calculation as that of 7(a). Here, in Fig. 7(b) we see the presence of superlinear current-voltage relations at low drain bias levels, followed by looping when domains are present.
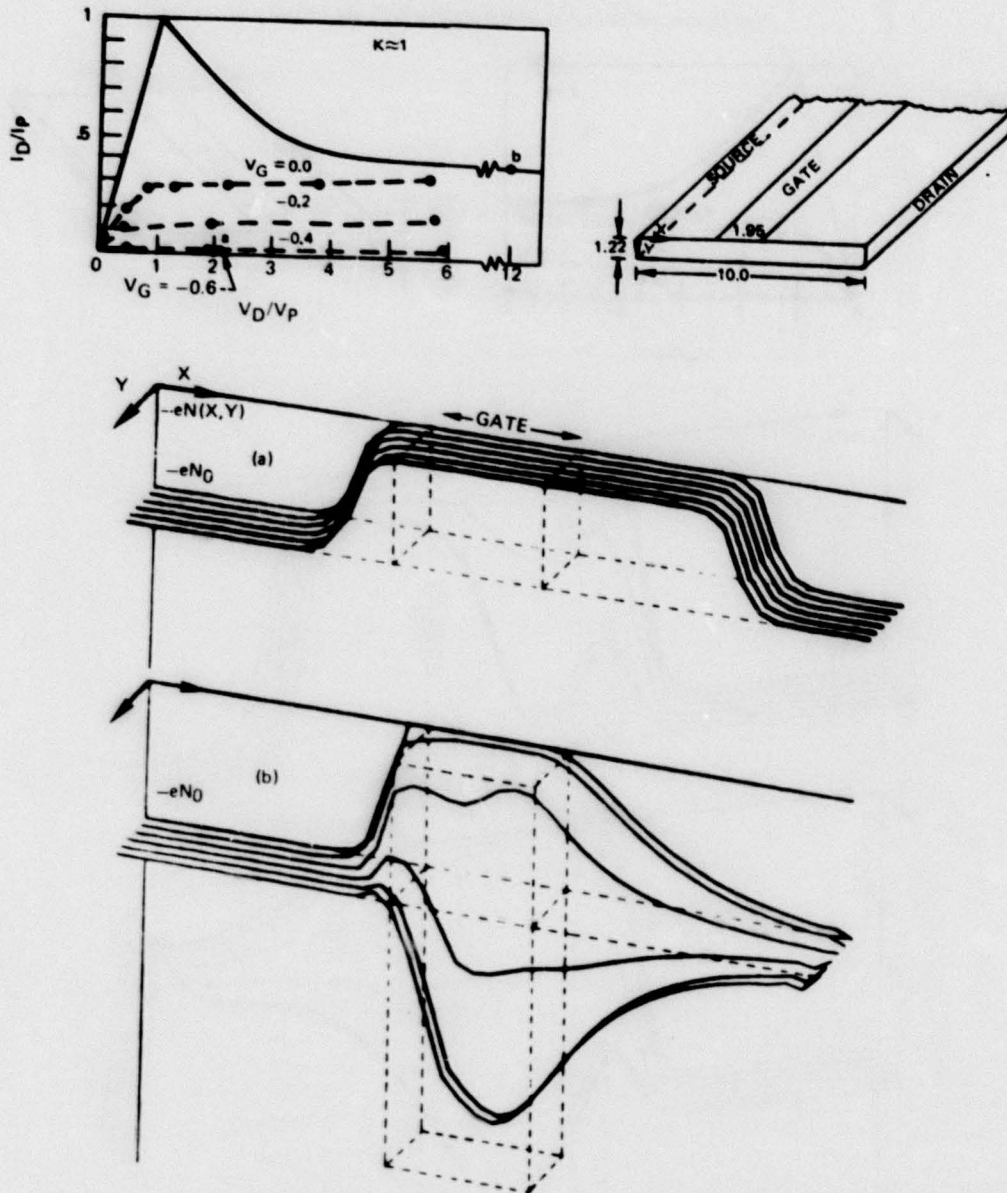
Fig. 4. As in Fig. 2. but for different bias values.

Both of these effects occur because of large transients through the gate contact.

With respect to transit time oscillations we point out that no experiment has yet been designed that provides unequivocal evidence for their existence in commonly fabricated GaAs FET'. In most common designs the gate to drain separation is somewhere between one-half and five microns, and for these values it is not clear that conditions exist for the propagation of "stable" domains[16]. The result is that the properties of these propagating domains are readily influenced by the external circuit and can in some cases be controlled by it. An example of this complex dipole-circuit interaction exists in two terminal devices (e.g. the quenched multiple dipole mode[16]). There is also the possibility that in place of the negative differential mobility induced oscil-

lations in GaAs FETs there are feedback circuit oscillations that are independent of any hot electron effects. However, in the experiments reported below we show that the evidence points to the oscillations as being negative differential mobility induced. Two additional space charge profiles are important in this regard and are discussed below.

The two profiles of interest are coincident with the suppression of transit time oscillations. In one case a significant increase in drain bias alone suppresses the instability. In the second case an increase in the magnitude of the gate bias is sufficient to suppress it. The space charge profile associated with the high drain bias suppression of the instability is displayed in Fig. 6(a). We see that an accumulation of charge forms downstream from the gate boundaries and extends towards the drain
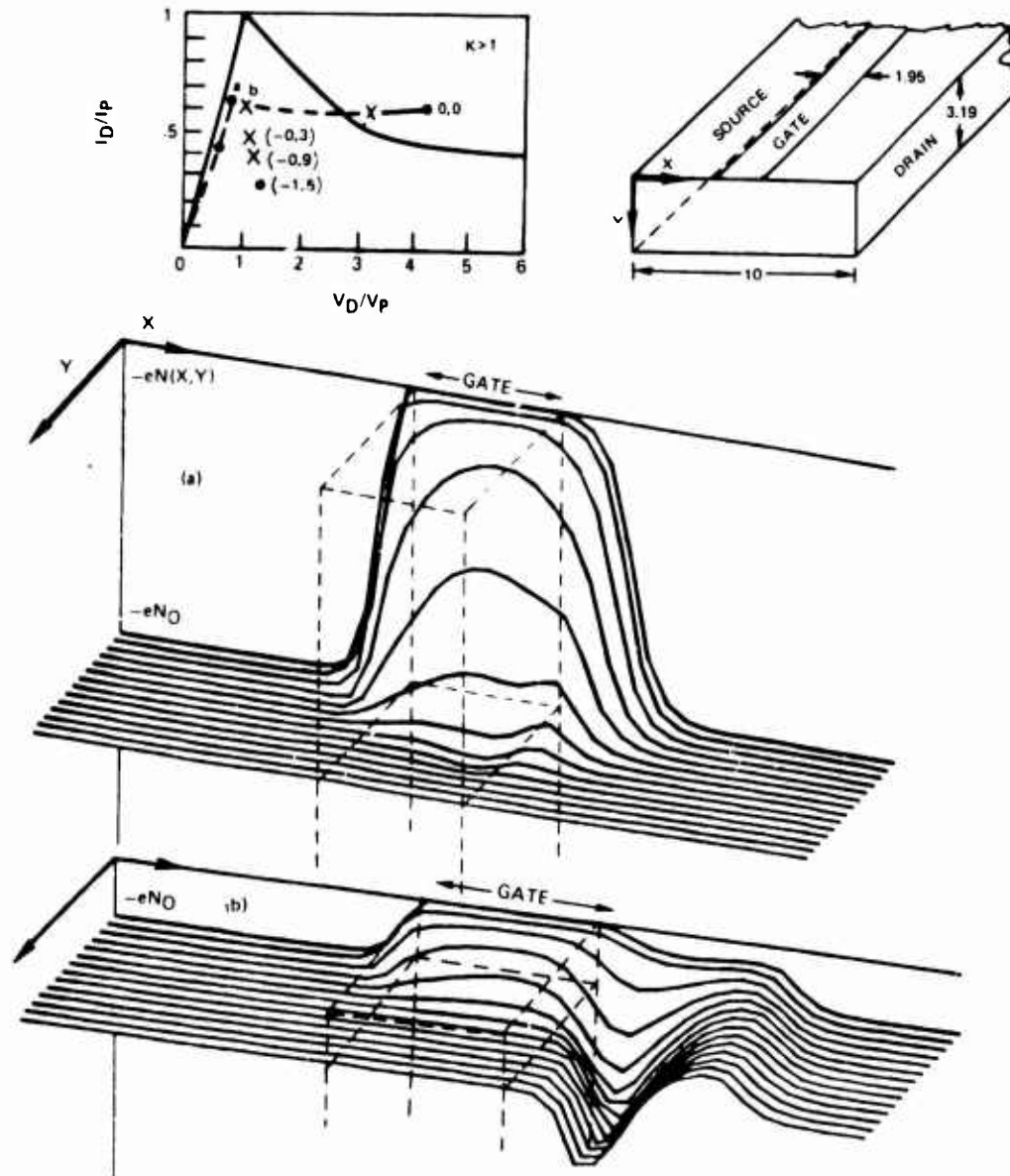
Fig. 5. As in Fig. 2, but for a different size device. X's denote transit time oscillations

contact. While this layer generally is not a static one but instead pulsates in time there are some broad features associated with it. For example, *the profile forms at values of current density in excess of J, and at high values of drain potential.* Most of the potential drop is across the gate-to-drain region (Ref.[3], Fig. 7), where we may expect the electric fields to be well within the saturated drift velocity region. Thus the carriers within the gate-to-drain region are traveling at their saturated drift velocity values. This fact and current continuity with the current density exceeding J, are responsible for the region of charge accumulation. By way of analogy this solution is qualitatively similar to two terminal device solutions which show the presence of anode adjacent domains[16]. Further, in three terminal devices with long gate-to-drain spacings and high doping con-

centrations the anode adjacent domain has been experimentally probed[19].

The space charge profile associated with the high gate bias suppression of the instability is displayed in Fig. 6(b). This shows a snapshot of the space charge layer while undergoing a damped oscillation. This layer of charge also pulsates in time, but in contrast to the space charge layer of Fig. 6(a), this one *forms at current density values that are less than J.* Indeed for this case most of the potential drop falls under the gate contact and extends some distance downstream from the edge of the gate boundaries[3] (Fig. 8). As long as the space charge layer does not reach the drain contact the electric field downstream from the edge of the nonuniform space charge region will be less than the "two-terminal sustaining field"[16] $E_S = v_s/\mu$. This situation is analogous
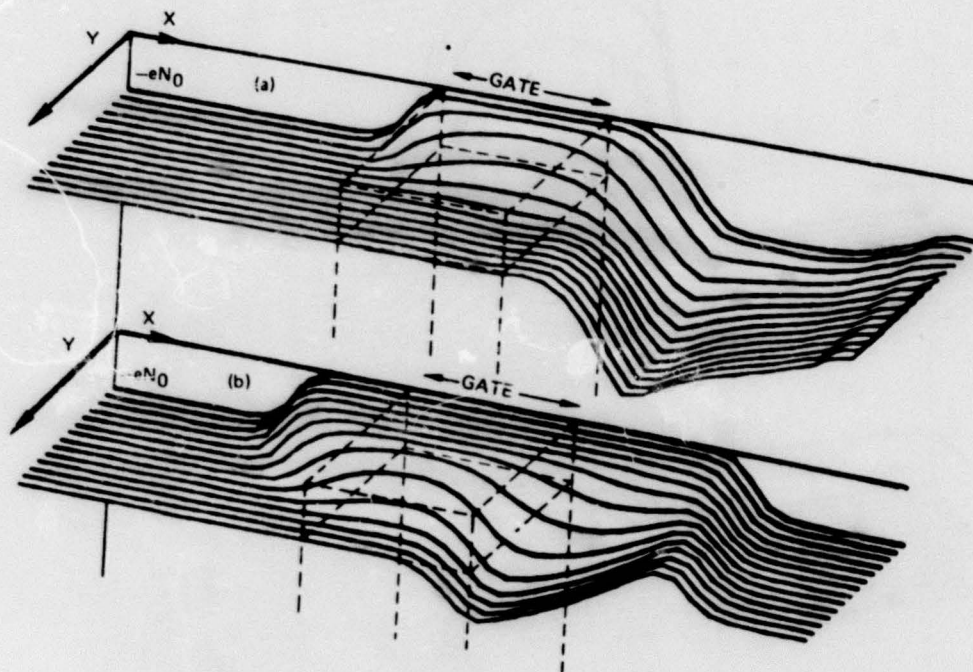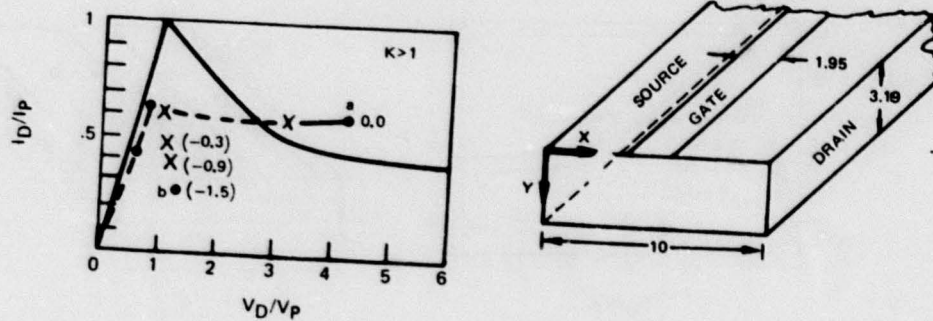
Fig. 6. As in Fig. 5, but for different bias values.

to the two terminal high cathode boundary field profiles[16].

3(d). *Summary*

To summarize, there are several key features associated with negative differential mobility induced instabilities in field effect transistors. These are:

(1) The instability occurs in devices with K greater than unity.

(2) The instability occurs at or beyond the "knee" of the current-voltage relation.

(3) A necessary condition for an instability is that the current density downstream from the gate boundary be greater than or approximately equal to J_s, or equivalently, that the drift velocity either exceeds v_s, or is approximately equal to v_s.

(4) Saturation in current occurs when the average field within the conducting channel under the gate contact is approximately equal to the threshold field for negative differential mobility.

(5) The instability can be suppressed by imposing a gate bias sufficiently high to reduce the current density downstream from the gate boundary to a value significantly less than J_s.

(6) The instability can be suppressed by imposing a sufficiently high value of drain bias.

Let us now turn our attention to how these instabilities manifest themselves in actual devices.

5. EXPERIMENTS WITH GALLIUM ARSENIDE FIELD EFFECT TRANSISTORS

5(a). *Experiments with* $K > 1$

Figures 8 and 9 display, respectively, temperature dependent, d.c. and pulsed drain current vs drain voltage characteristics for a GaAs FET. The source, drain and

LOAD LINES

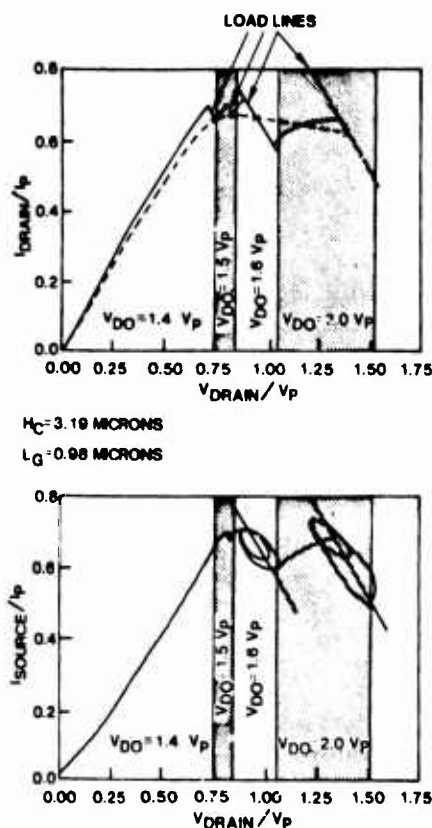$H_C = 3.19$ MICRONS
$L_G = 0.98$ MICRONS

Fig. 7. Instantaneous current vs voltage for the device of Figs. 5 and 6. (a) Drain current vs drain voltage. (b) Source current vs drain voltage.

gate contacts are coplanar with the source and drain contacts separated by approx. $8.5\,\mu$m. The gate is more or less centrally placed with a length, L_g, equal to $3.0\,\mu$m. The gate width, L_z, is $250\,\mu$m. The epitaxial layer thickness, H, was $3000 \pm 500°$ Å with a nominal doping level of $10^{17}/cm^3$. The mobility measured from adjacent samples varied from 3000 to 4000 cm²/V-s. The cutoff voltage for this device was 8.9 V. *This device sustained current oscillations as detected by a spectrum analyzer.* All six criteria listed in the last section for NDM induced instabilities were satisfied. We discuss each separately below. Oscillation characteristics

(1) $K = V_{co}/V_{ds} \cong (8.9 + 0.8\,V)/2.5 = 3.9$, where the cutoff voltage includes as assumed built in potential of approx. 0.8 V.

(2) At each value of ambient temperature, the instability occurred beyond the knee of the current voltage characteristic.

(3) The velocity was computed from the relation

$$v = I/(N_0 eHL_z).\qquad(8)$$

And the values prior to an instability are displayed as a function of *ambient* temperature in Fig. 10(a) where the error bars represent uncertainties in the value of H. In Fig. 10(a) the solid line corresponds to an estimate of the saturated drift velocity from Ruch and Fawcett[20] and Freeman and Hobson[21]. This data is available only to

12 kV/cm, and we have reduced these results by approx. 10% for higher fields. The closed circles in Fig. 10(a) are for the d.c. measurements; the x's represent pulsed measurements (1 μ sec pulse lengths, 1% duty cycle). The pulsed results generally surround the solid line and are higher than the d.c. results. In general over the temperature range exceeding 150 K the pulsed measurements yield a velocity exceeding v_s.

(4) The average field under the gate boundary is estimated from the relation

$$E_g = V_{tg}/L_g\qquad(9)$$

where V_{tg} is the longitudinal potential drop under the gate contact and is obtained from an equation that ignores contact resistance contributions:

$$V_{tg} = V_{ds} - IR_0(L - L_g)/L\qquad(10)$$

where V_{ds} is the drain voltage and I the drain current. $R_0(= 1/G_o)$ is the open channel resistance and may be obtained from the measured drain current voltage characteristics of the device via the relation

$$R_0 = R_d(V_g)(1 - [(V_{bi} + V_g)/V_{co}]^{1/2}) \Big/ \Big(1 - \Big[1 - \frac{L_g}{L}\Big](V_{bi}$$
$$+ V_g)/V_{co})^{1/2}\Big)\qquad(11)$$

where we have adopted the viewpoint of eqns (2) and (3) of Grehene[22]. V_{co} in eqn (11) includes the built in potential. The above expression for R_0 is expected to be valid at low values of drain bias. Assuming a built in potential of 0.8 V and reading R_d at $V_g = 0$ from the d.c. characteristics we compute R_0. The values are listed in Table 1, where we have ignored the temperature variations in V_{bi} and V_{co}. We see that the average field under the gate is relatively insensitive to temperature, as is the threshold field for negative differential mobility[20]. An average field of 4.2 kV/cm is consistent with a mobility for $10^{17}/cm^3$ material of 4200 cm²/V-s.

(5) As shown in Fig. 10(b) the carrier drift velocity at the cessation of oscillations is below v_s.

(6) All oscillations cease at high drain bias levels.

The next set of data are displayed in Fig. 11 where we show d.c. and sampling scope data (taken 25 nsec into a 50 nsec pulse, with low duty cycle). The GaAs FET had a source to drain spacing of $3.5\,\mu$m and a gate length of $1\,\mu$m. The cutoff voltage for this device was 3.0 V and the mobility was quoted at around 4500 cm²/V-s. With regard to the first two oscillatory criteria, $K \approx 4.8$ and the instability occurs just beyond the knee of the current vs voltage characteristic. The peak velocity just prior to the instability at 57 ma is computed from the equation

$$v = \mu IR_0 L\qquad(12)$$

with $R_0 = 9.7\,\Omega$ (from pulsed data) and $\mu = 4500$ cm²/V-s. The result is $v = 0.68 \times 10^7$ cm/sec. which falls approximately within the range of values of Fig. 10. An average threshold field of 4 kV/cm for a one micron gate

Table 1. d.c. Data.

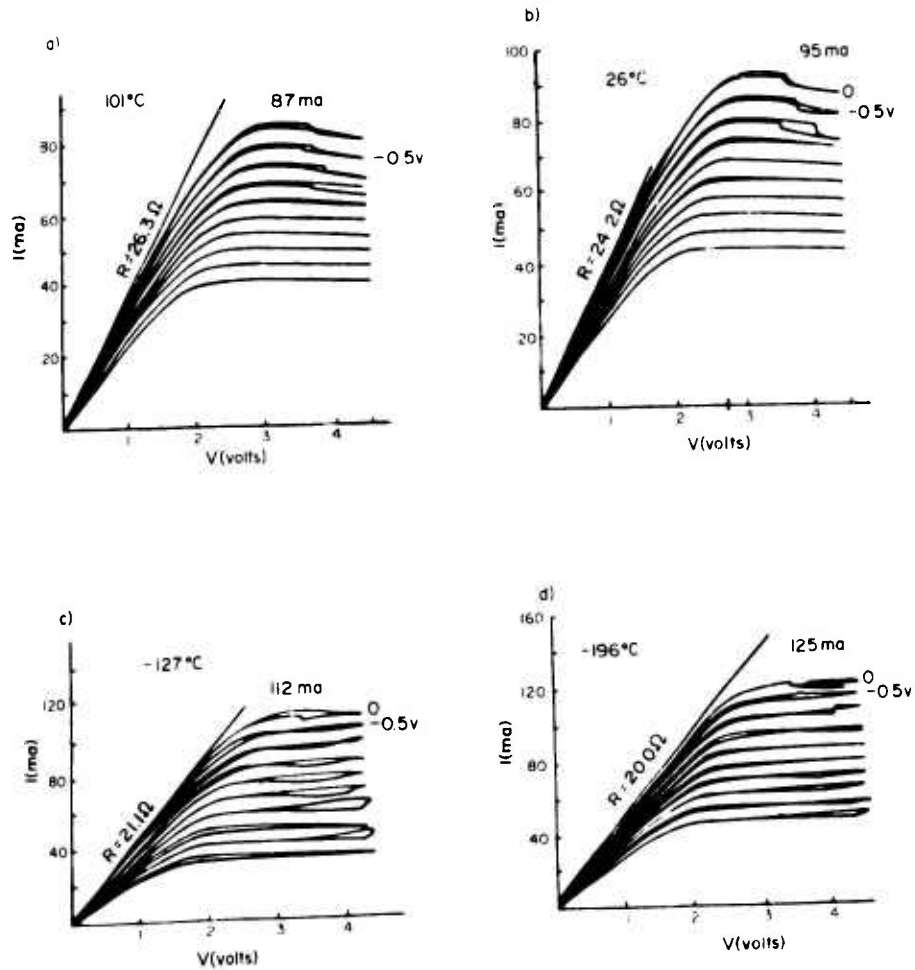| T CASE	V_{DS} (v)	$I_0 \times 10^{-3}$(a)	Rd (OHMS)	Ro (OHMS)	Eav (Kv/cm)
383°K	2.5	82	26.3	23.0	4.26
299°K	2.5	90	24.2	21."	4.22
166°K	2.5	105	21.1	18.4	4.17
77°K	2.5	115	20.0	17.5	4.00

Fig. 8. Temperature dependent d.c. current voltage data for a long gate FET. Device parameters are discussed in text.

is reached at a drain voltage of approx. 0.8 V; and it is here that we see substantial preinstability current broadening. The oscillations which are initiated at about 1.2 V are not suppressed until a sufficiently low value of current density is attained. The characteristic of the instability is suggestive of hot electron contributions richer than that discussed in the last section (see also Ref. [13]). However, consistent with the sixth criteria the oscillations are suppressed at high values of drain bias. This is displayed in Fig. 12 where we show sampling scope measurements at increasing drain bias for the device subjected a 1.5 μsec pulse. We see the initiation

of oscillations at low drain bias levels with subsequent suppression at high drain bias levels.

4(c). *Experiment with* $K \approx 1$

The final set of measurements is for a device with K approximately equal to unity. These are pulsed measurements. The device has a cutoff voltage of approx. 1.8 V and no oscillations were detected on a spectrum analyzer over a range of 40 GHz. The device had a quoted doping concentration of 5×10^{16}/cm³ and an epitaxial thickness of 0.5 μm. These values were not
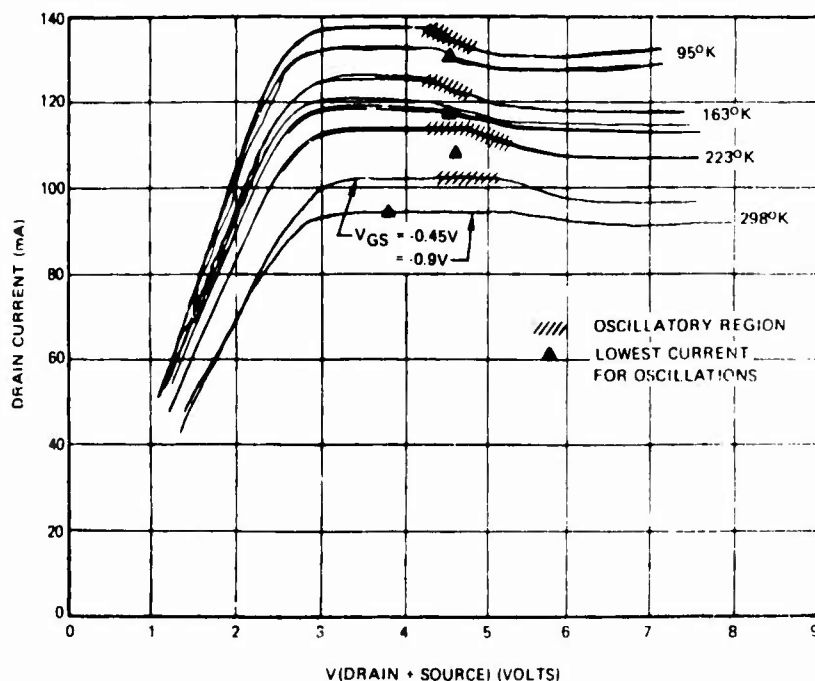
Fig. 9. Temperature dependent pulsed data for the device of Fig. 8. For these measurements a 5 Ω resistor separated the source from ground.

consistent with pinchoff values using the equation

$$V_{co} = eN_0H^2/(2\epsilon). \tag{13}$$

With a quoted value of $L_g = 360 \mu m$, eqn (8) yields a room temperature range of values of v, associated with the product N_0H.

$$v = 4.7 \times 10^{18}/N_0H. \tag{14}$$

From eqn (14) with N_0H varying from $10^{12}/cm^2$ to $1.5 \times 10^{12}/cm^2$, v varies from about 0.5×10^7 cm/sec to 0.3×10^7 cm/sec. All values are too low for an instability to occur.

4(c). *Discussion*

The experiments discussed above provide evidence that the GaAs FET is capable of sustaining negative differential mobility induced current instabilities. These instabilities occur when the average field under the gate contact exceeds the NDM threshold field and when the current density at the onset of saturation is approximately equal to or exceeds the saturation drift current density for GaAs. There are several additional experimental aspects that should be highlighted. The d.c. measurements of Fig. 8 were characterized by a drop in current at the instability threshold; the pulsed measurements also show a drop in current. The d.c. measurements of Fig. 11 do not show a dropback in current; the sampling scope measurements do. There is hysteresis in the d.c. measurements of Fig. 8 with the instability persisting for increasing and decreasing values of drain bias. However on the decrease the instability persisted at drain bias levels somewhat below the instability threshold. This is a

characteristic of two terminal transit time devices[16]. With regard to the sampling scope measurements of Fig. 11, we see some spreading of the current vs voltage prior to the instability. This may correspond in part to a pulsating trapped domain near the gate contact, as discussed in the earlier sections.

The oscillation properties reported here were detected using sampling oscilloscopes and spectrum analyzers. Spectral analysis was used on the devices of Figs. 8, 9 and 13. Sampling scope measurements were for the device shown in Figs. 11 and 12 and other devices not reported here. At first the spectrum analyzer was set up to detect frequencies to 18 GHz. In this set up, frequencies of 1.2, 1.6, 2.5 and 4.2 GHz were detected. These oscillations were bias dependent but ceased at drain bias levels in excess of 6 V. The oscillations ceased at substantially higher gate bias levels. Under the assumption that there were additional frequencies in excess of 18 GHz that were going undetected, and that by analogy to two terminal devices where the introduction of a inductor reduces the circuit frequency, we introduced a ½ nH inductor in series with the source loop. The low frequency oscillations disappeared and in their place were instabilities at 13, 13.6 and 14.2 GHz. More detailed spectral analysis measurements were subsequently made with the spectrum analyzer open to frequencies to 40 GHz. The pulsed measurements were then analyzed, with the following details. Oscillations began at 3.5 V and persisted to just below 4.25 V. Oscillations were observed at 6.5, 13, 23, 30, 36 and 40 GHz. Higher frequencies could not be detected. The oscillations were strongest at 4.1 V where the 6.5 and 40 GHz signals dominated. At 4.25 V on the drain the oscillations ceased, at least up to 40 GHz. In the same measuring circuit and with the gate
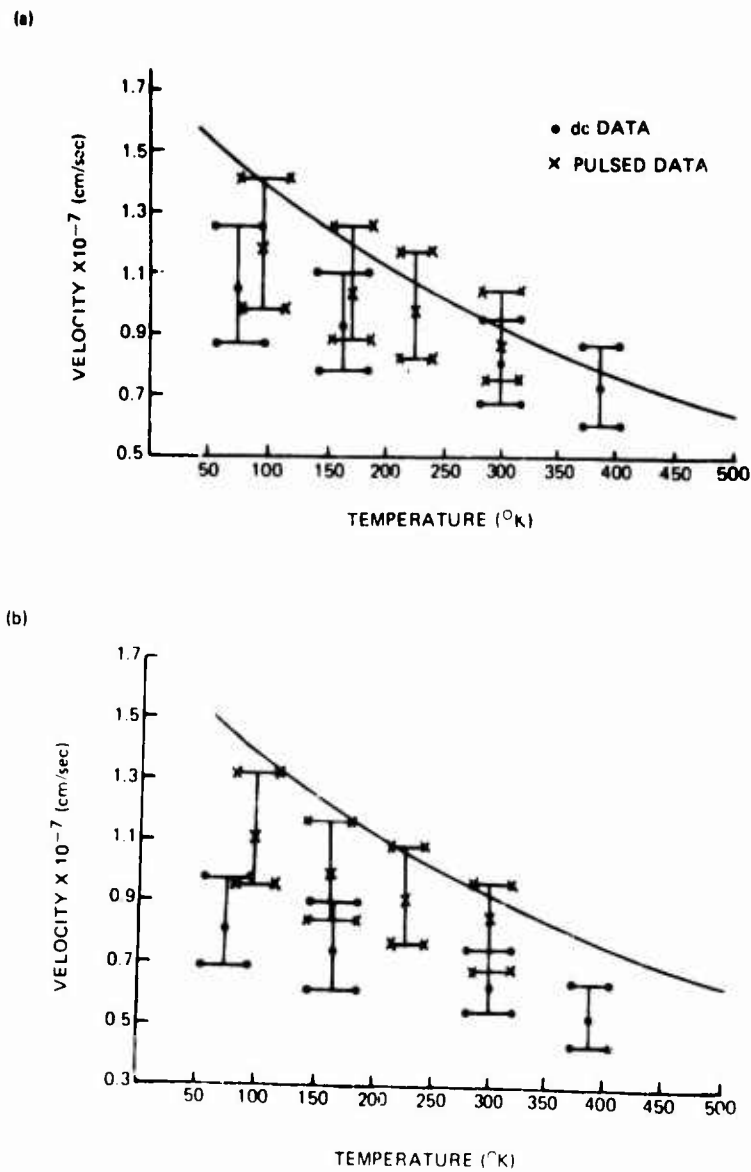
(a)

(b)

Fig. 10. Solid curve is an estimate of high field saturated velocity vs ambient temperature (a) Velocity, from eqn 8, vs ambient temperature, prior to oscillations. (b) Velocity, from eqn 8, vs ambient temperature, at cessation of oscillations with application of a high gate bias.

wide open visible light was detected at 6.4 V on the drain. This was not accompanied by any oscillations whose frequency was below 40 GHz. An initial reduction in potential on the gate contact resulted in similar behavior but at −0.8 V on the gate, all oscillatory activity ceased, including the appearance of light. The electrical behavior of this device was measured at a variety of temperatures, with qualitatively similar behavior.

The oscillation frequencies reported above bear no clear relation to the transit-time oscillation frequency. As indicated in Section 3, the gate drain separation may be too short to guarantee stable domain propagation and so the oscillatory properties, including the frequency are likely to be determined by a complex device-circuit interaction. There is also the possibility that the oscillations we are observing are a consequence of feedback

between the gate and drain loop. While this situation cannot be ignored the evidence in terms of the six instability criteria given in the last section, including the suppression of oscillations at high drain bias levels, make this possibility small.

In the above paragraphs we reported the observation of light. Light was also observed under d.c. conditions. The details are as follows. Under d.c. conditions light was seen at the beginning of the current instability, became dimmer as the drain bias increased but remained while the device oscillated. The light was stronger at drain bias levels sufficient to eliminate the oscillations. At moderate gate bias levels faint light remained, but at sufficiently high gate bias levels large enough to eliminate the oscillations, all light activity ceased. The light, for all practical purposes was white. The observations of light is
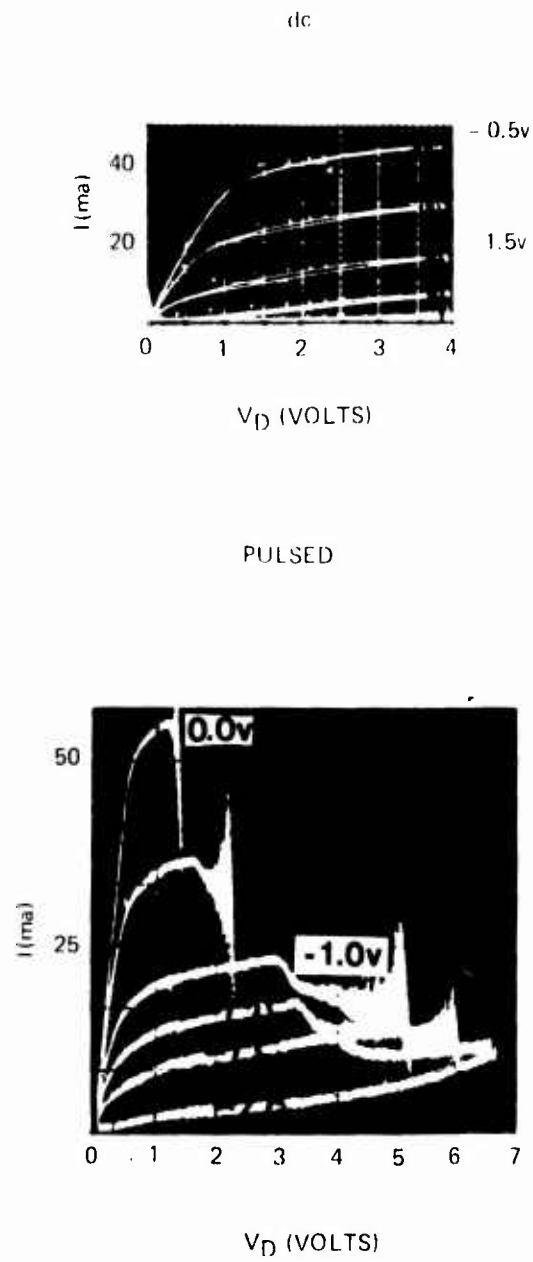
dc

PULSED

Fig. 11. (a) d.c. and; (b) pulsed sampling scope measurements of the current voltage characteristics for a short gate FET.
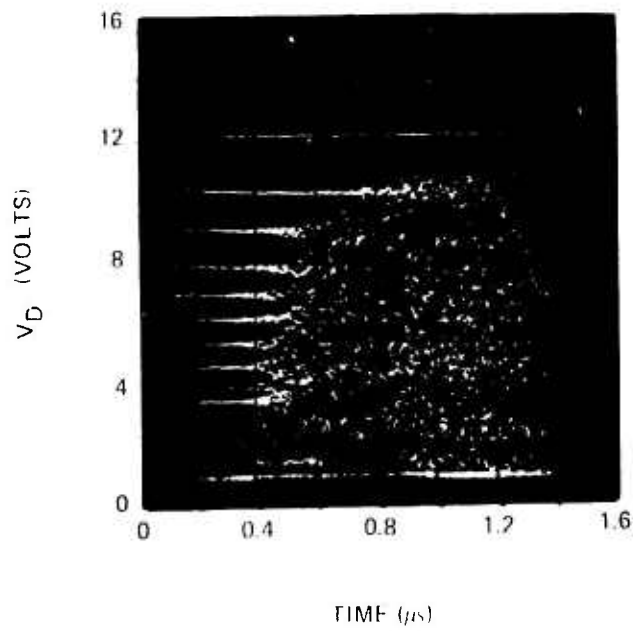
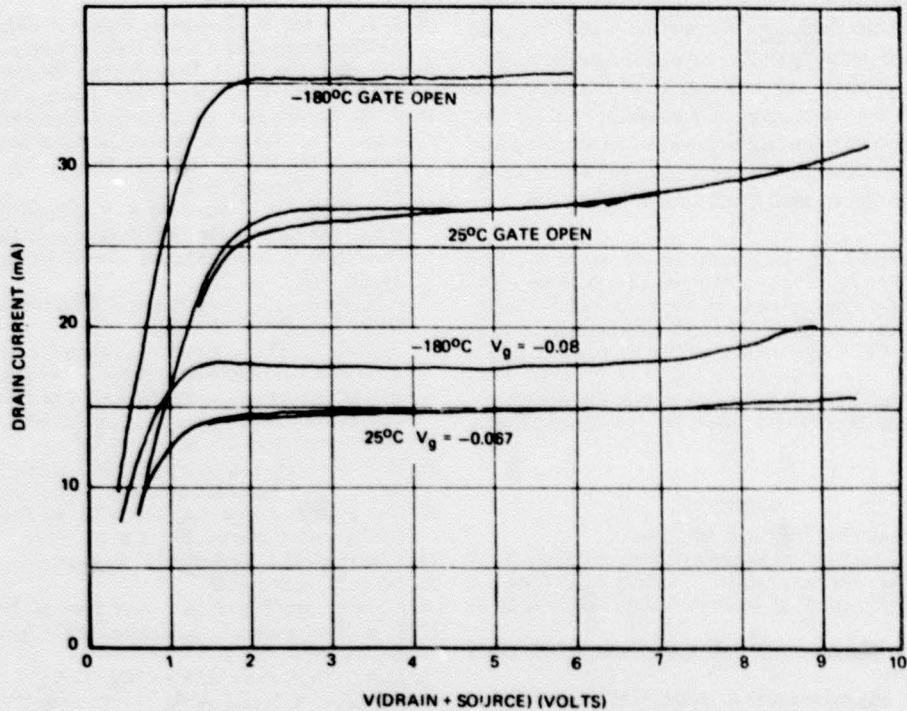Fig. 12. Sampling scope pulsed drain voltage vs time as a function of drain bias for the short gate FET.

Fig. 13. Pulsed current vs voltage data for a device that did not exhibit any oscillations.

compelling evidence for the presence of regions of high electric field and excess carriers. At low drain bias levels, the dimness of the light may be accounted for by the fact that the time averaged electric field at a given point within the sample is less for propagating domains then for the trapped domains. The latter occurs at high drain bias levels. The absence of light at high gate bias levels may possibly be due to the broad region of charge *depletion* in the vicinity of the gate boundary. The arguments for white light are somewhat uncertain. We recall, however, that the separation between the central portion of the conduction band and the valence band is within the infrared, while the separation between the satellite conduction and valence bands is within the ultraviolet. The entire visible spectra is within these two bounds.

We note that Mimura *et al.*[23] on $10^{17}/cm^3$ GaAs FETs also observed visible white light at high drain bias levels. For devices with highly doped n^+ drain contacts light was observed at the $n^+ n$ interface; for devices without an n^+ drain contact radiation was observed at the drain metalization edge. Mimura *et al.*[23], attribute the radiation to impact ionization within a domain trapped at the drain contact. The intensity of this light was observed to increase with drain bias and decrease as the gate voltage was made negative. These results are consistent with our findings.

5. SOME MODELLING CONSIDERATIONS

The results of our analysis are consistent with the identity

$$IDSS \times R_0 = E_{out}L \qquad (15)$$

where E_{out} is the longitudinal electric field in the source to gate region. In devices with K greater than unity, E_{out} will generally be at least equal to E_s; and so for this case a lower bound for *IDSS* exists:

$$IDSS \times R_0 \geqq E_s L. \qquad (16)$$

For example, with the device reported in Figs. 8 and 9, the room temperature values of the l.h.s. of eqn (16) (from Table 1) is equal to 1.9 V. The r.h.s. side with $E_s = 2.2$ kV/cm is equal to 1.87 V. For the device whose properties are displayed in Figs. 11 and 12, $IDSS \times R_0 = 0.52$ V, while $E_s L = 0.77$ V. By way of comparison Shockley's study[24] teaches that

$$IDSS \times R_0 = V_{co}/3 \qquad (17)$$

while more recently Shur[25] have concluded that

$$IDSS \times R_0 = E_s L_g. \qquad (18)$$

Equation (18) yields results significantly lower than observations, and less than eqn (16).

6. CONCLUSIONS

In conclusion, through analysis and experiment we have presented evidence for the presence of negative differential mobility induced current instabilities in GaAs FETs. We have listed six criteria that identify these NDM instabilities, paramount among these is the fact that the longitudinal electric field under the gate must be greater than the threshold field for negative differential mobility while the current density must exceed the sus-

taining current. The fact that the instabilities in some cases are delayed until higher values of bias are reached implies that the field must exceed the NDM threshold field for the instability. We have also presented corroborating experimental and theoretical evidence, consistent with the conclusions of Yamaguchi *et al.*[8], that devices whose current densities, within the source to gate region, are less than J_s will not go unstable. Those whose current densities exceed J_s will sustain instabilities.

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