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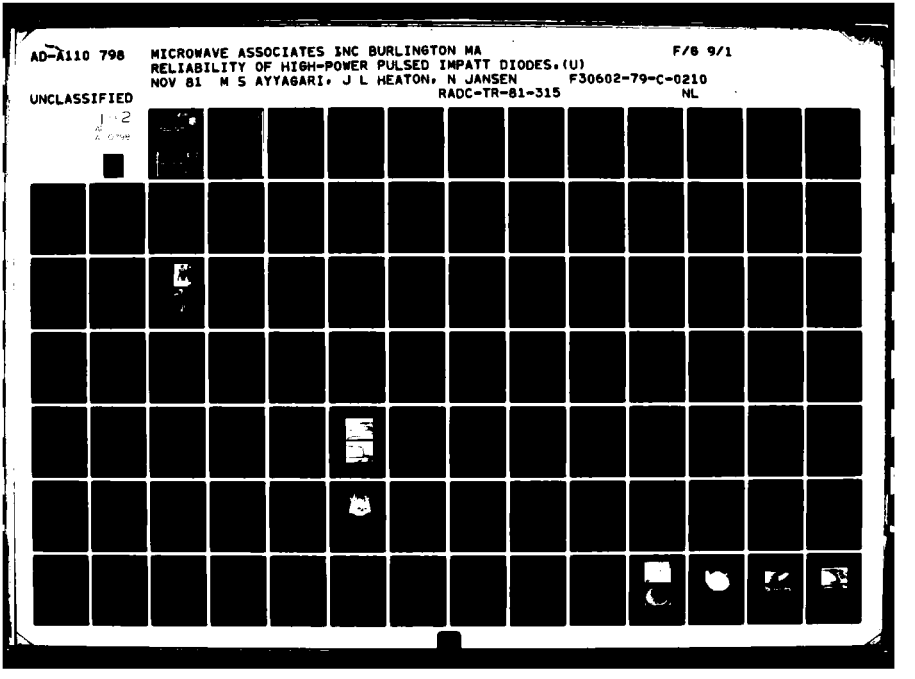

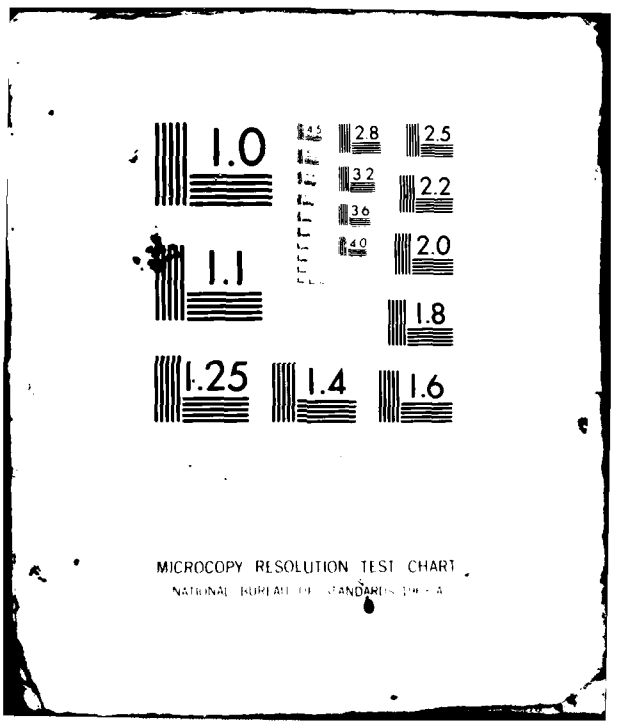
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RELIABILITY OF HIGH-POWER PULSED IMPATT DIODES

Microwave Associates, Inc.

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Because of their present and future use in military systems, particularly missile seekers, high power pulsed IMPATT reliability is of considerable interest. This report is concerned with a reliability study of gallium arsenide double-drift pulsed IMPATTs of the Read doping profile type, that is both n and p active regions and contains avalanche confining doping structures. Both short-term (freak failure region) and long-term reliability testing have been carried out, comparing performance and

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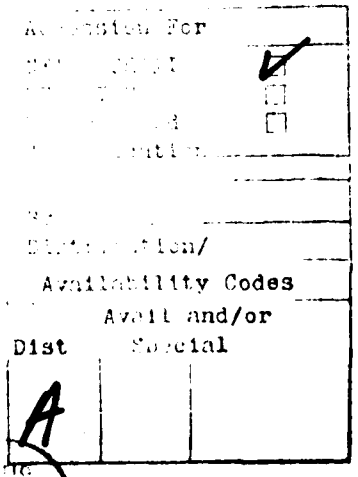
failure mechanisms of the gallium arsenide devices with a smaller number of silicon flat profile double-drift devices, and Schottky-barrier, single-drift, low-high-low doping profile gallium arsenide devices.

The double-drift gallium arsenide devices were fabricated using sequential vapor phase epitaxy, at Microwave Associates, and were capable of 17 watts of peak output power at 10 GHz under one microsecond, 30% duty operation. The reliability testing was divided into three areas. First, various screening tests were evaluated for effectiveness in removing defective devices from a newly manufactured lot. DC burn-in, pulsed DC burn-in (non-oscillating), and pulsed oscillating burn-in were compared, with equivalent average device junction temperature (235°). In each case, 168 hour tests at maximum recommended average input power were conducted. In the case of gallium arsenide double-drift devices, pulsed burn-in, with or without RF oscillations, were equally effective. However, for GaAs single-drift diodes, only oscillating burn-in was adequate.

In the second phase of testing, devices were stressed under oscillating conditions, with a set of increasing bias current values, until failure occurred. The test was repeated at 16 different pulse widths and duty cycle combinations allowing determination of the most stringent operating conditions, and evaluation of failure mechanisms characteristic of such overstress. In nearly every case, failure at the mesa surface was seen for the gallium arsenide devices.

The third phase of testing was directed at examination of long-term reliability and wear-out failure mechanisms. Both a high temperature storage step-stress test and a long-term operation constant stress test were carried out. In the step stress test, following 335°C bake for 168 hours, irreversible changes in diode breakdown behavior involving an increase in leakage current and general rounding of the breakdown characteristics were seen.



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1.0 INTRODUCTION

1.1 Program Summary

High power pulsed IMPATTs represent an attractive solid state replacement for small and medium power magnetrons and travelling-wave tubes. When used in power combiners, the IMPATTs have provided pulsed solid state sources with average output powers in excess of 100 watts and peak power near 500 watts. The principal applications for pulsed solid state microwave sources are military, particularly for the seeker radar in missile systems. Such use provides a unique reliability problem, in that, during operation pulsed IMPATTs are stressed more heavily by electric field, current density and junction temperature than other solid state devices. One of the reasons for seeking solid state replacements for tube-type systems is increased reliability, as has been demonstrated in the case of low power transmitters.

It was the purpose of this study to determine the reliability characteristics of high power pulsed IMPATT diodes, including development of appropriate burn-in schedules for early failure elimination, determination of operating parameter limits for safe operations, and identification of long-term failure mechanisms under actual use conditions. Devices studied under the program include gallium arsenide single-drift Schottky junction low-high-low (L-H-L) profile devices, double-drift hybrid devices (flat profile p-side, L-H-L n-side) and full Read [L-H-L or high-low (H-L) profile on both sides] devices fabricated at Microwave Associates, as well as silicon flat profile double-drift devices purchased commercially (from Hewlett-Packard). All devices were capable of 12 to 15 watts of peak output power at high duty cycle (25 to 33,1/3%), and 10 to 20% efficiency. Emphasis was

placed on the gallium arsenide double-drift devices, with the silicon devices being included for comparison purposes. Single-drift gallium arsenide devices were also included, because devices of this type are presently being used in missile system applications. Preliminary tests were also carried out using gallium arsenide flat profile devices.

Silicon double-drift devices used in this study were pre-screened by the manufacturer (H-P). The GaAs devices used in this study were produced by Microwave Associates and were not screened for early failures.

The testing sequence carried out began with early failure region test evaluation, in order to determine the most cost effective screening method for these devices. DC burn-in, pulsed DC burn-in (devices not oscillating), and pulsed RF burn-in were compared for effectiveness in removing defective devices from the population. These tests represent a set of screening methods involving increasing complexity and cost as one progresses from DC to pulsed DC to pulsed RF burn-in. When applied to single-drift (SD) gallium arsenide or double-drift (DD) silicon devices, pulsed DC and DC burn-in produced comparable failure rates, while pulsed RF burn-in produced a significantly higher rate, and would be the required early failure region screening method for these devices. Double-drift gallium arsenide devices, however, exhibited similar failure rates for pulsed DC and pulsed RF burn-in, while the DC burn-in rate was much lower, indicating pulsed DC burn-in could be substituted for RF burn-in for DD gallium arsenide devices. All early failure region tests were carried out under identical average junction temperature conditions.

Long-term pulsed RF burn-in (1000 hours duration) was carried out on both hybrid and full Read double-drift gallium arsenide devices. Overstress junction temperature was used in order to produce significant failures within the test duration. Failing units were subjected to failure analysis, and mean lifetime determined at the junction temperature used.

A high temperature storage step stress test was carried out using both hybrid and full Read gallium arsenide double-drift devices. The test was repeated using diodes of special construction to avoid possible effects of remelting of the chip bonding preform. Mesa failure temperatures for 168 hour stress periods were established, and failure analyses carried out.

Both silicon and gallium arsenide hybrid and full Read double-drift devices were subjected to a pulse-to-failure burn-out test, establishing useful operating limits for the devices. Contours of maximum allowable pulse current versus pulse width and duty cycle were constructed.

Additional special tests conducted included a thermal cycling test and a switching transient test. In the switching transient test, ten full Read double-drift gallium arsenide double-drift devices were operated under pulsed RF burn-in conditions as had been previously done. In addition, the pulsed bias was switched ON and OFF every two minutes. The failure rate seen was not significantly different from that recorded previously for these devices without ON - OFF switching.

In total, the following devices were manufactured (or in the case of silicon devices, purchased) and tested during this program:

(1)	50	-	Single-Drift L-H-L Schottky GaAs devices
(2)	50	-	Silicon Flat-Profile Double-Drift devices (H-P 5082-0710)
(3)	25	-	Double-Drift Flat-Profile GaAs devices

(4)	100	-	Double-Drift Hybrid Profile GaAs devices
(5)	75	-	Double-Drift Read Profile GaAs devices

Figure 1-1 presents a summary of the overall testing sequence used. As shown, all devices entering long-term or overstress testing had been prescreened with DC, pulsed DC, or pulsed RF burn-in. All failing devices were subjected to failure analysis. In cases where electrical and visual examination indicated the same failure mechanism, only representation sample devices were further analysed.

The study reported here has revealed the potential reliability performance of presently available pulsed IMPATT devices, and has uncovered some potential reliability problems that indicate necessary changes in fabrication methods. This information will be of great value to diode users as well as manufacturers, allowing eventual development of higher reliability systems employing pulsed IMPATT devices.

1.2 Reliability Physics Theory - General

The typical failure rate versus time curve for a component population is composed of three regions (Figure 1-2). These regions are the infant mortality or freak failure region, the useful life region and wear-out failure region. This type of behavior is typical for all semiconductor devices. An additional failure mode can occur during the useful life and is catastrophic in nature. This failure mode is not related to the inherent processes involved in the device manufacture, but to the effects of transient phenomena on a high field device. These failures are a result of diode - circuit interactions and cannot be studied by the conventional approaches used for reliability studies.

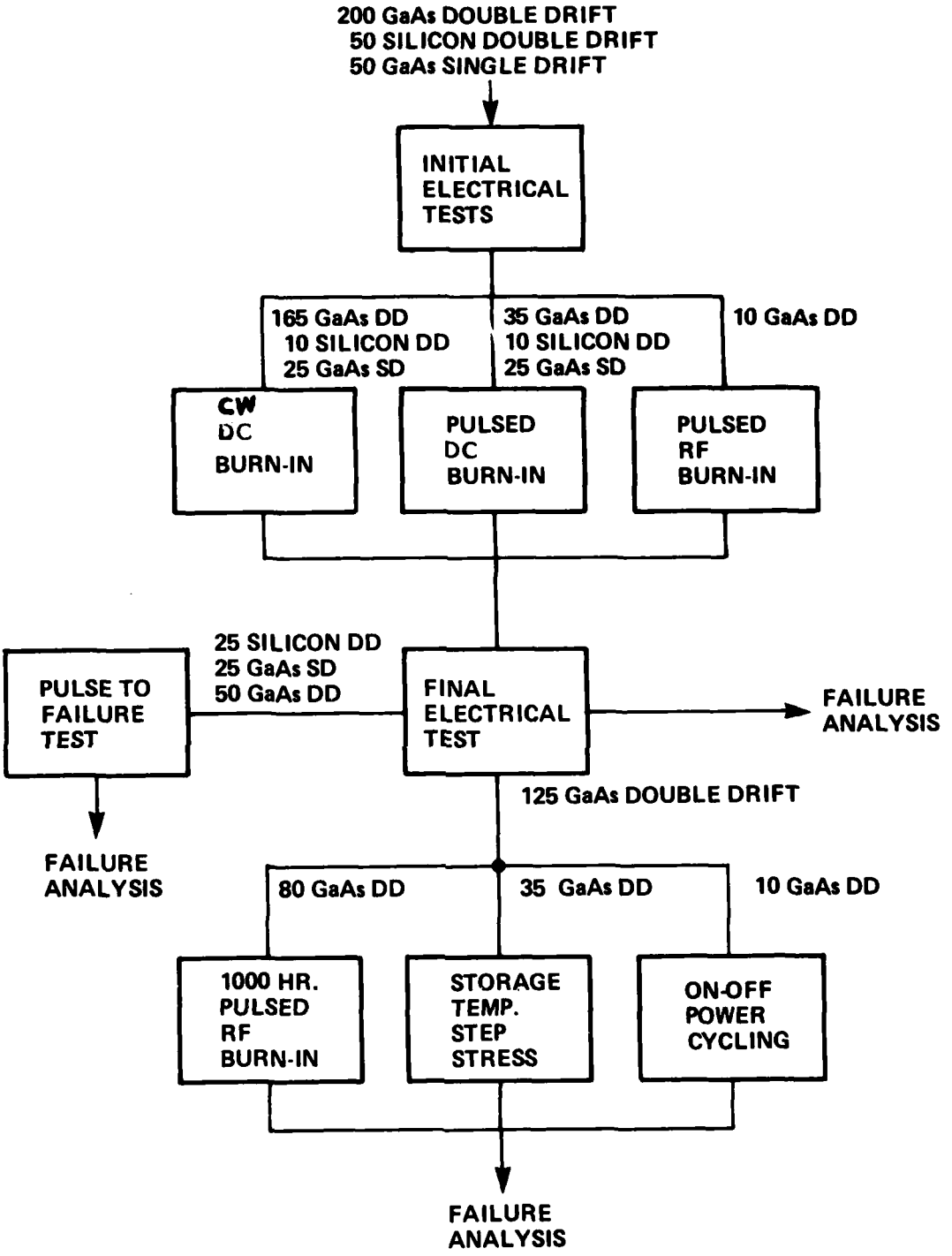

FIGURE 1-1 A SUMMARY OF THE OVERALL TESTING SEQUENCE

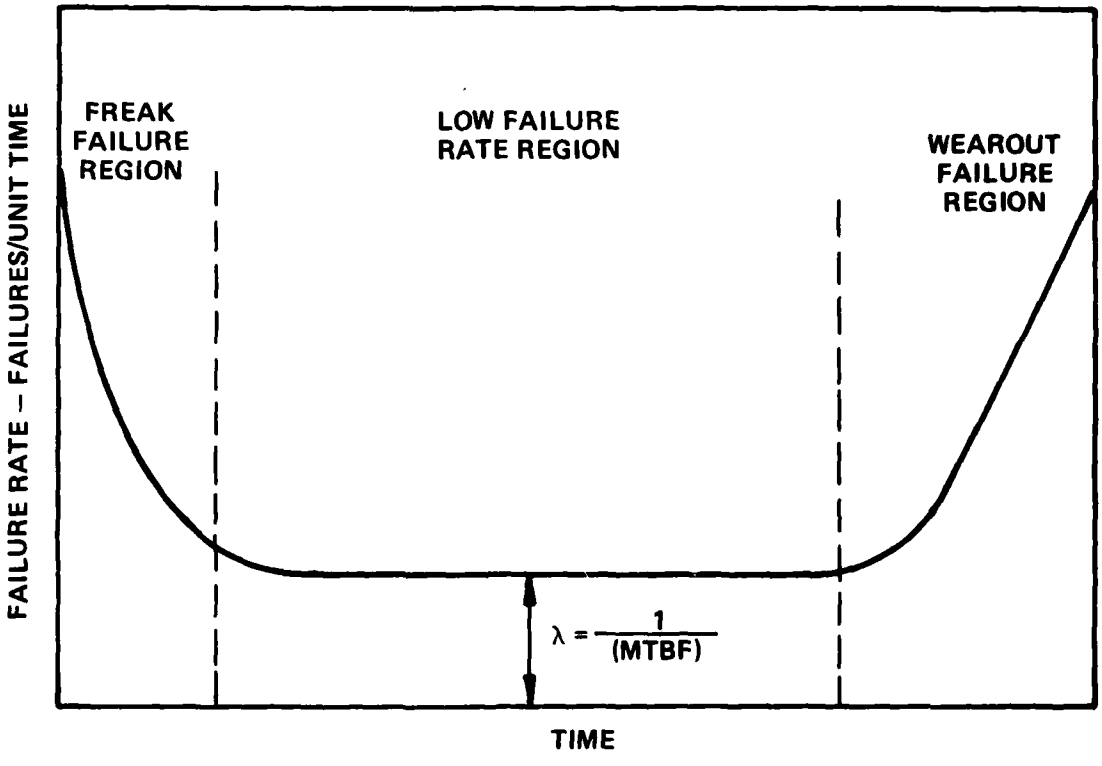

FIGURE 1-2 GENERALIZED FAILURE RATE vs. TIME CHARACTERISTICS

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For the typical failure rate - time distribution for semiconductor devices (Figure 1-2), it is instructive to inquire as to what is to be accomplished in reliability testing and procedures developed for the different areas of the failure rate curve. The freak failure or infant mortality region is characterized by a failure rate that decreases with time as faulty devices are removed from the population. It is the purpose of this period to remove sufficient defective devices to reduce the failure rate to an acceptable level during the useful-life region. The procedures which are utilized must therefore enhance the infant mortality rate so as to minimize the useful-life failure rate by eliminating any defective devices during this infant mortality period.

Some sort of burn-in screening process is normally used to remove weak devices from the population, and reduce the failure rate to an acceptable level. Generally, operation of devices under increased stress conditions (RF burn-in) is employed as a screening test. However, as a production technique, RF burn-in is costly because of the equipment involved and the loading time required. In this program, various alternatives to RF burn-in were considered, including pulsed DC burn-in and DC burn-in under non-oscillating conditions.

The second region or useful-life region of the generalized failure rate versus time curve is characterized by a small, time independent failure rate, λ. The MTBF (mean-time-between-failures) is the reciprocal of the failure rate, and is of importance to system designers because it allows prediction of failure rates in systems employing many diodes. The MTBF was investigated by long-term RF burn-in tests (greater than 5000 hours) conducted under worst case RF output power and junction temperature conditions.

After many thousands of hours of operation, components enter the wearout failure region of the failure rate versus time characteristics, where the failure rate is no longer constant but begins to increase with time. This region is normally investigated by using accelerated aging life tests of the step stress or constant stress type.

1.2.1 MTBF Determination

Diode MTBF determination is concerned with measurement of the failure rate of units surviving early failure screening. This portion of the failure rates versus time curve is characterized by a constant failure rate, λ , where:

$$MTBF = 1/\lambda \qquad [1.1]$$

The rate of failure is time independent in this region, leading to an exponential probability of survival given by [1]:

$$P_s = e^{-\lambda t} \qquad [1.2]$$

where:

P_s = probability of component will survive to time, t, (hours)

λ = the failure rate (failures per hour)

Causes of failure in this region are not due to wearout mechanisms such as contact metallization movement, but are of the "freak" variety, such as loosening of the contact wire or failure of the chip bond. Such failures are most difficult to identify because of the normally low observed failure rates.

MTBF is determined by operating a group of units under normal conditions and measuring the observed failure rate. Then

$$MTBF = \frac{\text{Number of Unit Hours of Operation}}{\text{Number of Failures}} \qquad [1.3]$$

The lower confidence limit estimate for the MTBF is computed as follows:

$$L = \frac{2R\overline{m}}{\chi^2_{2R,\ (\alpha/2)}} \qquad [1.4]$$

where:

- L = lowest value that the MTBF could assume with confidence level α
- R = number of devices which have failed
- α = the confidence level
- $\overline{m}$ = estimate of the MTBF from Equation [1.3]
- $\chi^2_{2R,\ (\alpha/2)}$ = value of Chi square statistic for 2R degrees of freedom, and probability level $\alpha/2$

It should be noted that those failure mechanisms responsible for determining the MTBF may not be accelerated by temperature increase. Hence, to be completey valid, MTBF measurements are normally conducted under normal operation conditions,

and may require several years of test time to produce a significant number of failures. Only in tests involving very large samples can meaningful MTBF data be developed in short times.

1.2.2 Wearout Failure

In the wearout failure region of the failure rate versus time curve, the failure rate is no longer constant, but begins to increase as failure due to long-term degradation mechanisms become more likely than the random failures of the middle-life region. The average time to wearout failure is often described by the Eyring-Arrhenius rate law:

$$t_m = \exp\left\{\left[\frac{\Delta H}{kT} + C\right]\right\} \qquad [1.5]$$

or

$$\log t_m = \frac{\Delta H}{kT} + C$$

where

- ΔH = the activation energy for the process
- k = Boltzmann's constant
- C = design constant factor
- T = device active region temperature, °K

The factor, C, reflects variation from unit-to-unit in device manufacture or the effect of stress other than temperature. If, for a large number of units, temperature is held constant, and C is assumed to be normally distributed among units, then the

time to failure is log normally distributed. Such a condition has been found to empirically describe most semiconductor failure distributions[2,3].

In order to determine the activation energy for a process, t_m must be determined experimentally for several different average active region temperatures. This technique is the so called "constant stress" method, (see Figure 1-3), and involves operating a set of devices at a fixed temperature and recording the time to failure for each unit. The test must be repeated for at least two stress levels. Alternatively, the step stress method may be used where the devices are subjected to stress which is repeatedly increased in constant increments after a fixed time interval, until all devices fail. Here, the test is repeated using time intervals of at least two different lengths. All devices failing within a given time interval are considered to have failed at the end of the interval in question. As shown in Figure 1-3, either the constant stress or step-stress technique may be used to generate the Arrhenius accelerated failure curve.

One danger associated with the use of the Arrhenius equation concerns the existence of two or more failure mechanisms. In some cases, certain mechanisms such as melting of contact metallization may be effective only at elevated temperature. Attempts to accelerate those mechanisms responsible for wearout failure under normal conditions may initiate failure due to a second mechanism which completely masks operation of the primary cause failure. In order to eliminate this problem, several quick step stress tests can be run initially in order to find the maximum usable temperature before excitation of additional failure mechanisms.

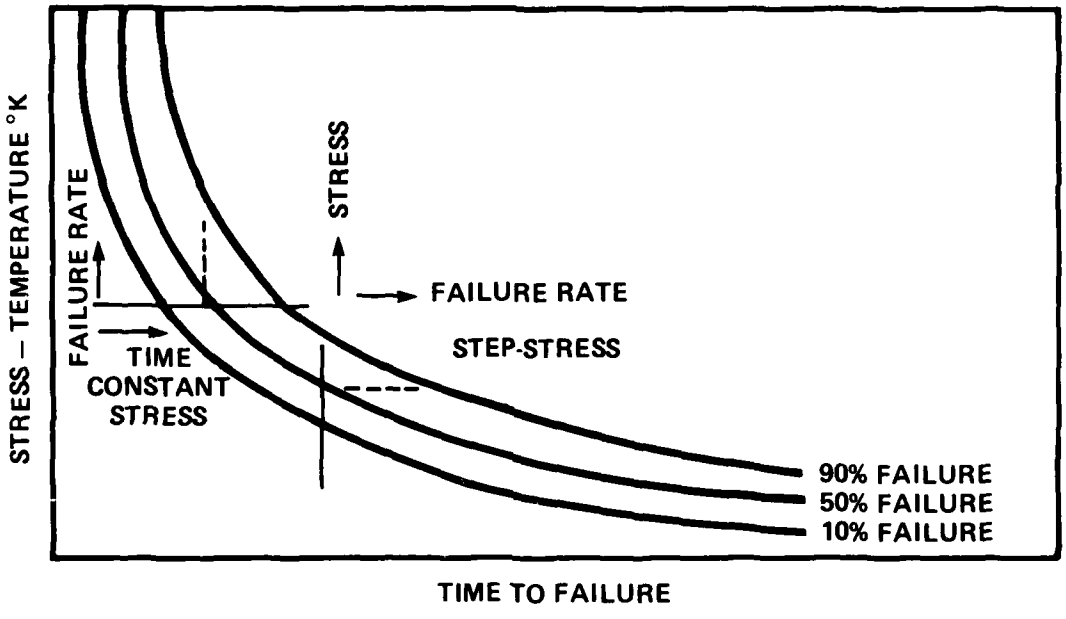

FIGURE 1-3 ACCELERATED FAILURE RATE CURVE SHOWING STEP STRESS AND CONSTANT STRESS TESTS.

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1.3 Failure Mechanisms in Pulsed IMPATT Diodes

Because IMPATT diodes operate under conditions of extremely high electric field and current density compared with other semiconductor devices (5×10^5 V/cm, 2000 A/cm^2), failure mechanisms unique to pulsed IMPATTs may be postulated. Previous investigations [4,5,6] have investigated failure mechanisms in Schottky junction single-drift gallium arsenide IMPATTs. In the case of platinum Schottky Read IMPATT diodes, penetration of platinum Schottky-barrier metallization into the gallium arsenide active region has been cited as a primary cause of long-term diode degradation. Because such motion in effect changes the doping peak location and height, dramatic changes in diode operating performance are expected. If the platinum layer is not excessively thick (less than 200 Å), reaction will stop before much change in diode performance has occurred due to the exhaustion of unreacted platinum.

If thin platinum layers (a few hundred angstroms) are used, a second degradation mechanism can occur. This mechanism involves penetration of gold from the final metallization layer through the platinum by diffusion or surface migration. Such penetration leads to acceptor formation and net donor density reduction in the heavily doped spike region of L-H-L IMPATTs. Single-drift devices tested under this program utilized a four-layer metallization system designed to avoid these failure mechanisms. A 200 Å platinum layer is used and fully reacted with the gallium arsenide to prevent further junction motion during use. A 2000 Å titanium layer prevents further gallium arsenide reaction and is followed by a 1500 Å platinum gold diffusion barrier. A final gold metallization facilitates bonding. The reliability of this Schottky-barrier system as applied to CW L-H-L gallium arsenide IMPATTs has been extensively studied [6].

Failure mechanisms in double-drift IMPATTs generally would not be as contact metallization dependent as single-drift Schottky units because in double-drift devices, contact metallization is isolated from active device areas by intervening n+ or p+ layers. Rather, one might expect a contact related degradation similar to that seen in Gunn devices, [7] where a gradual penetration of gold contact metallization through an n+ buffer layer was identified as the long-term failure mechanism. Figure 1-4 presents in cross-section a Gunn device that failed due to this mechanism following 650 hours at 340°C junction temperature.

Other possible failure mechanisms in double-drift devices include surface breakdown and conduction, conducting channel formation of crystalline defects, and contact electro-migration.

Early failure region failure mechanisms would also include defects common to all semiconductor devices such as loose high thermal resistance bonds, and material damage due to excess bonding pressure.

1.4 Criteria for Failure in GaAs IMPATT Devices

An Impatt device is considered to have failed for this reliability study if one of the following conditions occur:

(i) the device is electrically either short or open,

(ii) any of the following DC characteristics change by more than 10%

- (a) breakdown voltage at 1 mA (V_B)
- (b) forward voltage at 1 mA (V_F)
- (c) leakage current at .8 V_B (I_R)
- (d) capacitance at 0 volts (C_{TO})

(iii) the RF power degrades by more than 2 db for the same RF circuit conditions

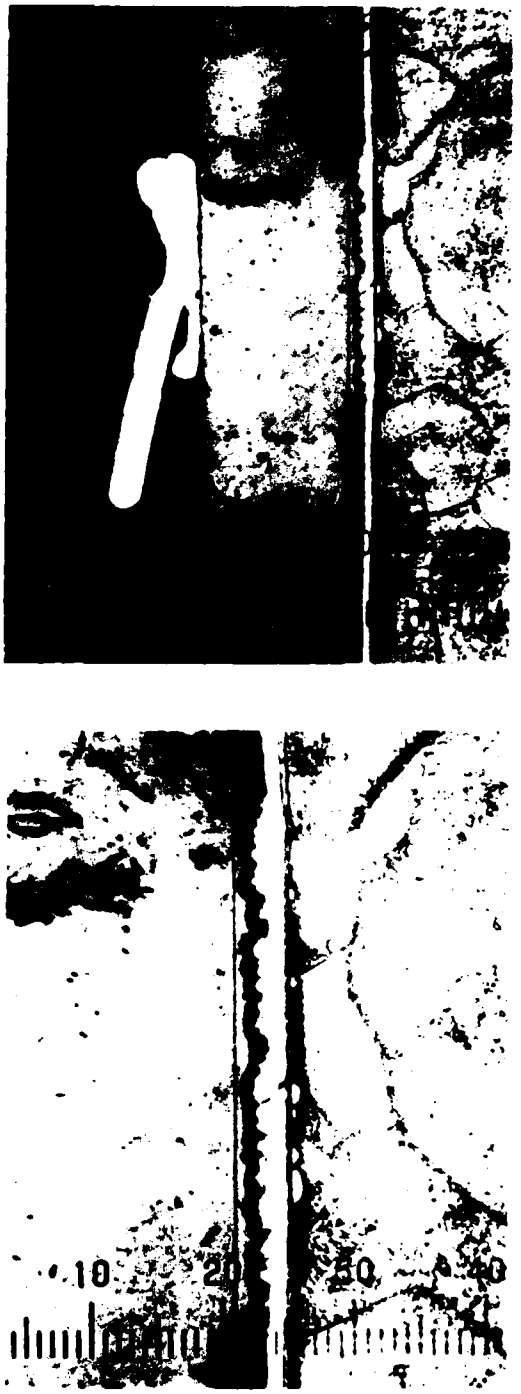

FIGURE 1-4 TWO MICROSCOPIC PHOTOGRAPHS OF A CROSS-SECTIONED GUNN DIODE WHICH EXHIBITED CURRENT DROP DURING CONSTANT STRESS TESTING. EACH SCALE DIVISION IS 0.4 MIL IN THE UPPER PHOTOGRAPH, 0.2 MIL IN THE LOWER. THE DIODE IS FROM STEP STRESS RUN 5, WAFER 6024-1A, IDENTIFICATION NUMBER 16.

2.0 THEORY OF OPERATION, FABRICATION, AND PERFORMANCE OF PULSED IMPATT DIODES

2.1 Device Design

2.1.1 Introduction

In this section, the basic properties of IMPATT devices are described. Important material parameters, doping profiles and how they effect the operating parameters such as efficiency, power output, operating voltage and other important properties will also be described. Approximate design criteria as well as results obtained from highly sophisticated large-signal analysis programs will be presented and estimates concerning device performance and capabilities will be given.

2.1.2 Basic Principles of IMPATT Operation -- Gallium Arsenide Devices

As is well known, IMPATT devices can be reliazed in various forms including single-drift (SD) and double-drift (DD) ones. For each of these types, there are various types of doping profiles which can be employed. The various doping profiles which are most suitable for GaAs devices are shown in Figure 2-1, where the doping density and electric-field profiles at breakdown are shown. In addition to those shown, we can also have hybrid double-drift structures where we have a high-medium or low-high-medium doping profiles on the n-side and uniform doping on the p-side. All of these structures can be represented in terms of an effective avalanche region width (X_a) and a drift region width. For the single-drift structures, there is a one-drift region (for electrons) only (X_{dn}) and for the double-drift structures, there are two-drift regions, X_{dn}, for electrons and X_{dp} for holes

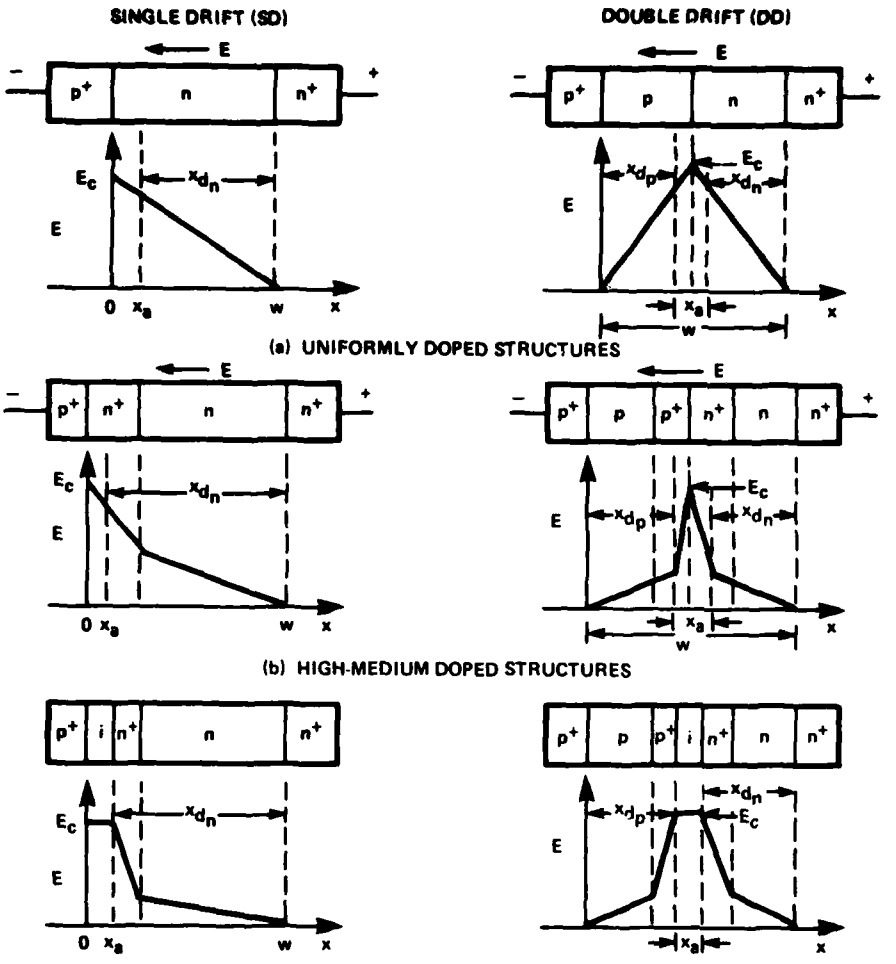

FIGURE 2-1. DOPING AND ELECTRIC FIELD PROFILES FOR VARIOUS SINGLE- AND DOUBLE-DRIFT DIODES

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respectively. The avalanche multiplication and, thus, the particle generation takes place in the avalanche region when the electric field exceeds the critical field (E_c). The carriers are then injected into the drift regions and drift towards the highly-doped end regions and induce a current in the external circuit. The induced current depends on the velocity of the carriers in the drift region as well as the length of the drift region. For a pulse of charge, a drifting between two parallel plates as shown in Figure 2-2, the induced current can be expressed as:

$$J_{ind} = \frac{Q}{W} v_Q - \frac{W_c}{W} \frac{dW}{dt} \qquad [2.1]$$

where:

v_Q = the velocity of the charge clump

W = the width of the depletion layer

W_c = the location of the charge clump

If W is fixed (this would be the case for some punchthrough devices) and v_Q is constant and equal to v_s, (the saturated velocity), then Equation [2.1] becomes:

$$J_{ind} = \frac{Q v_s}{W} \qquad [2.2]$$

It is, therefore, obvious that the induced current waveform will be effected by the velocity - electric field characteristic as well as the doping profile since the doping profile will determine W.

It is very informative to consider an idealized current waveform of the type shown in Figure 2-3, since this will

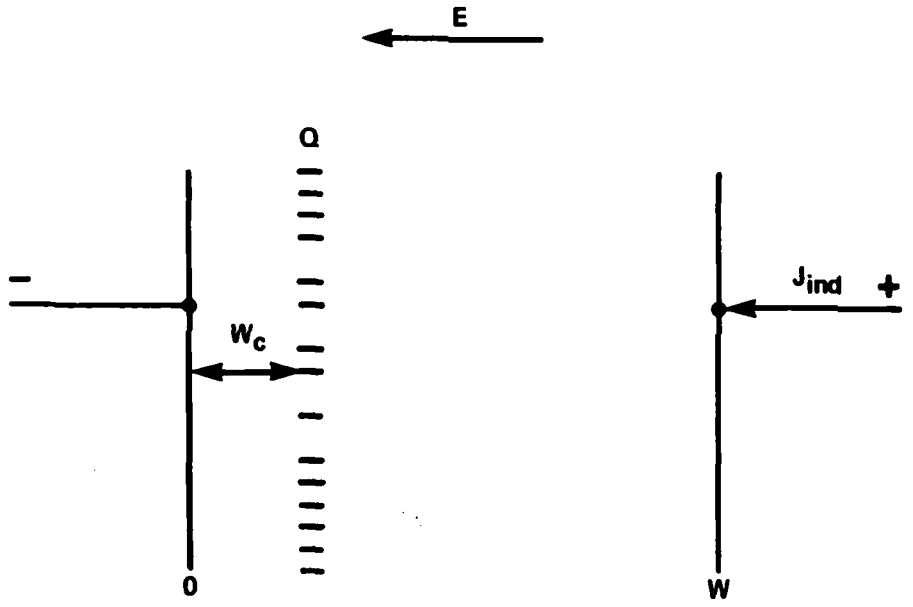

FIGURE 2-2 CHARGE CLUMP Q DRIFTING BETWEEN TWO PARALLEL PLATES

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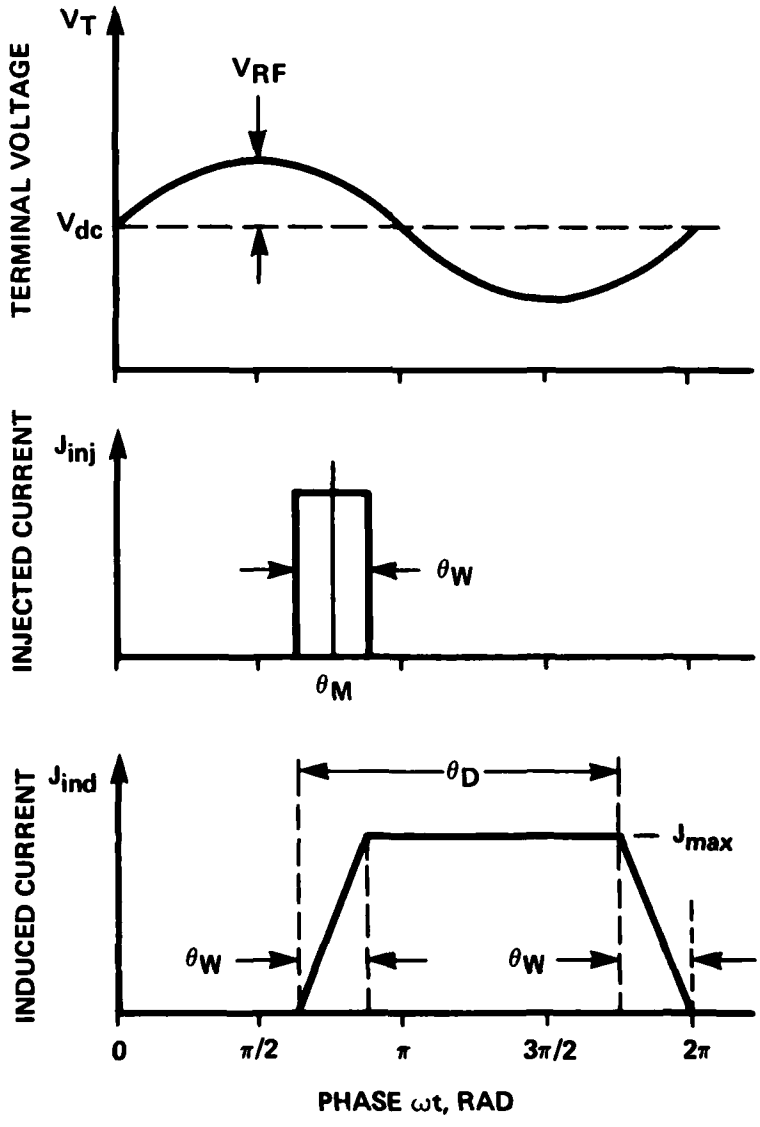

FIGURE 2-3 IDEALIZED VOLTAGE AND CURRENT WAVEFORMS FOR AN IMPATT, MITATT OR TUNNETT DEVICE

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shed a great deal of light on the operation of the IMPATT device and will indicate the various parameters which need to be optimized in order to optimize power output and efficiency. Realistic waveforms which are obtained in realizable structures will be presented later. These types of waveforms can be obtained only from a full-scale, large-signal simulation of the device.

In the idealized waveform shown in Figure 2-3, we assume an applied voltage across the device of the form:

$$v = V_{DC} + V_{RF} \sin \omega t \qquad [2.3]$$

The current pulse generated in the avalanche region, J_{inj}, is shown to be centered at a phase angle θ_M and has a width of θ_W. It is assumed here that the pulse of charge which is injected into the drift region travels in the drift region at a saturated velocity and induces a current in the external circuit J_{ind} as shown in Figure 2-3(c). θ_D is the transit angle through the drift region and is given by:

$$\theta_D = \omega \tau_D = \frac{\omega X_d}{v_s} \qquad [2.4]$$

where:

ω = the radian frequency

τ_D = the drift-time across the drift region

v_s = the saturated velocity

X_d = drift region width

From the voltage and current waveforms shown in Figure 2-3, we can derive simple expressions for the power output and efficiency as follows:

$$J_{DC} = \frac{1}{2\pi} \int_{o}^{2\pi} J_{inj} \, d(\omega t) = \frac{1}{2\pi} \int_{o}^{2\pi} J_{ind} \, d(\omega t) \qquad [2.5]$$

The maximum induced current, J_{max}, can then be expressed as:

$$J_{max} = \left(\frac{2\pi}{\theta_D}\right) J_{DC} \qquad [2.6]$$

The DC power density (per unit area) is given by:

$$P_{DC} = V_{DC} J_{DC} \qquad [2.7]$$

The RF power density (per unit area) is given by:

$$P_{RF} = \frac{1}{2\pi} \int_{o}^{2\pi} J_{ind}(\omega t) V_{RF} \sin \omega t \, d(\omega t) \qquad [2.8]$$

which after algebraic manipulation simplifies to:

$$P_{RF} = V_{RF} J_{DC} \frac{\sin \theta_{W/2}}{\theta_{W/2}} \left[\frac{\cos \theta_M - \cos(\theta_M + \theta_D)}{\theta_D}\right] \qquad [2.9]$$

The efficiency is, therefore, given by:

$$\eta = \frac{P_{RF}}{P_{DC}} = \left(\frac{V_{RF}}{V_{DC}}\right) \frac{\sin \theta_{W/2}}{\theta_{W/2}} \left[\frac{\text{Cos } \theta_M - \text{Cos } (\theta_M + \theta_D)}{\theta_D}\right] \quad [2.10]$$

By proper scrutiny of Equations [2.9] and [2.10], it can be seen that in order to maximize the power output and efficiency, we have to do the following:

(1) maximize $\frac{V_{RF}}{V_{DC}}$

(2) minimize θ_W

(3) make θ_M as close to π as possible

(4) choose the proper value of θ_D

For IMPATT devices, we have the following:

(1) V_{RF}/V_{DC} is determined by the doping profile in the device. This will be discussed in detail when we consider realistic doping profiles.

(2) θ_W is determined mainly by the width of the avalanche region. To minimize θ_W, we minimize the avalanche region width. There is a limit on this, however, since if the avalanche region is made too narrow, tunneling will set in and lower the efficiency. Detailed studies indicate that good performance can be achieved for avalanche region

widths of 0.15 to 0.25 micrometer. These can be readily achieved in practice. The choice of the avalanche region width also depends on the operating current density, the wider we can make the avalanche region and still obtain high-efficiency mode operation.

(3) θ_M is determined by:

(a) The operating current density; the larger the current density, the smaller θ_M becomes.

(b) The operating RF voltage magnitude; the larger the RF voltage magnitude, the larger θ_M becomes.

(c) The reverse saturation current; the larger the reverse saturation current, the smaller θ_M becomes.

(d) Generation of carriers in the drift region; this has the same effect as the saturation current and, thus, avalanche multiplication in the drift region must be avoided.

(4) θ_D is determined by the depletion layer width (i.e., doping profile) and the velocity - electric field of the carriers.

For idealized conditions ($\theta_W = 0$; $\theta_M = \pi$), Equation [2.10] reduces to:

$$\eta = \frac{V_{RF}}{V_{DC}} \quad \frac{\text{Cos } \theta_D - 1}{\theta_D} \qquad [2.11]$$

Therefore, for $\theta_D = \pi$ or $\pi/2$:

$$\eta = -\frac{2}{\pi} \quad \frac{V_{RF}}{V_{DC}} \qquad [2.12]$$

It is interesting to note that under this idealized condition, the efficiency is the same for $\theta_D = \pi$ or $\pi/2$. This is not surprising because, since we are keeping the current density constant, then the induced current maximum will be one-half as large for $\theta_D = \pi$, as that for $\theta_D = \pi/2$.

It is also worth noting that the maximum efficiency for this case occurs for $\theta_D = 0.74\pi$ and is given by:

$$\eta = -\frac{2.27}{\pi} \quad \frac{V_{RF}}{V_{DC}} \qquad [2.13]$$

The negative sign in the efficiency expression implies that the device delivers power. A positive sign implies power absorption.

It is also worth noting that the absolute maximum efficiency occurs for $\theta_M = 0$, $\theta_M = 3\pi/2$ and $\theta_D = 0$. This implies a very sharp pulse of induced current occurring at the minimum of the RF voltage ($\theta = 3\pi/2$). For this case:

$$\eta = -\frac{V_{RF}}{V_{DC}} \qquad [2.14]$$

The induced current waveform, therefore, has a significant effect on the power output and efficiency. Essentially, we want the induced current to be zero between $\theta = 0$ and π and to be as large as possible near the $\theta = 3\pi/2$ point. This is significant because that is essentially what we will strive for in designing the doping profile in such a manner to maximize V_{RF}/V_{DC} and take advantage of the velocity - electric field characteristic in GaAs to maximize the induced current near the $\theta = 3\pi/2$ point. This will become evident when we discuss realistic structures.

2.1.3. Double-Drift Diodes

Double-drift diodes offer cetain advantages over single-drift ones in terms of power output because the impedance level in these devices for the same current density is higher. Therefore, in terms of electrical parameters, the device area can be made approximately twice as large for the same load resistance. This means that the input DC power will be approximately four-times higher (the DC voltage and current will be approximately twice as large) and for the same efficiency, the R.F. power output will be four-times larger. However, the thermal impedance of the device is also higher and for CW operation, this presents a problem.

The various types of double-drift structures were shown in Figure 2-1 and can be classified as follows:

(a) Uniformly-Doped Double-Drift Structure:

Here, the doping concentrations on both sides of the junction are uniform.

(b) Double-Drift Read-Type Structures:

Here, the doping concentrations on both sides of the junction have a high-medium or a low-high-medium doping profile.

(c) Double-Drift Hybrid Structures:

Here, the doping concentration on the p-side is uniform while that on the n-side is a high-medium or a low-high-medium structure.

Because of the properties of p-type material, the efficiency in any of the double-drift structures will be lower than that in the comparable single-drift one. This is because the RF modulation level will always be lower due to losses in the p-type layer if it is exposed during operation.

A typical doping profile and electric-field profile for a hybrid double-drift structure is shown in Figure 2-4(a). The p-side is designed so that it remains punchthrough at the highest RF voltage modulation. A good number for a α which is a measure of the electric field at the p+ edge at DC is 0.25. This insures a reasonable avalanche region width and large RF voltage modulation without exposing

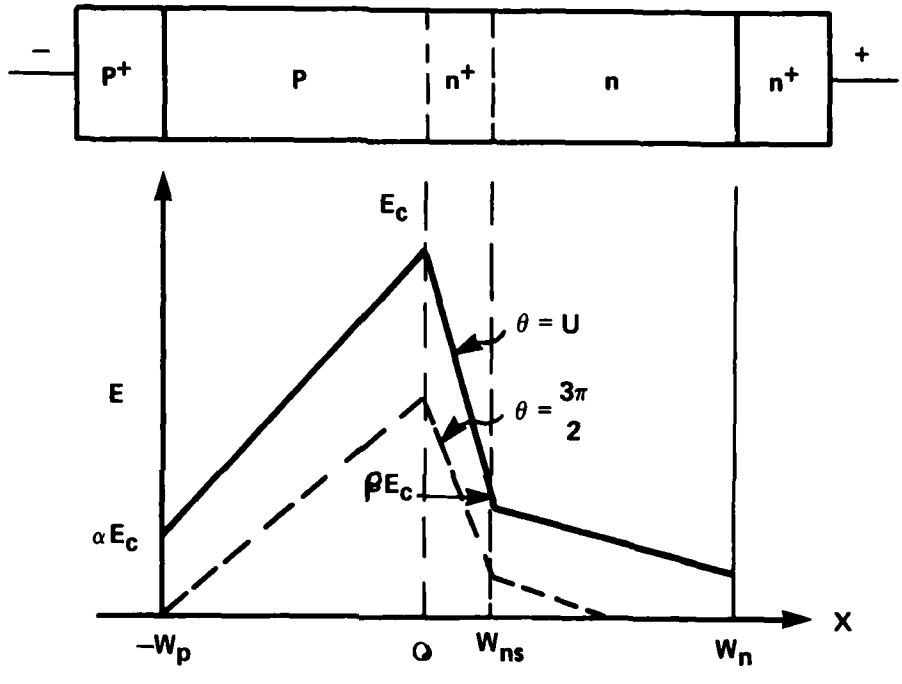


FIGURE 2-4(a) DOPING PROFILE AND ELECTRIC FIELD IN A HYBRID DOUBLE DRIFT STRUCTURE

D-19800

the p-layer. In the n-region, we can use either a high-medium profile or a low-high-medium one. The factor β, which determines the field at the beginning of the drift region, is chosen to be 0.4. The length of the drift region on the n-side is determined from Equation [2.4]. The total transit angle in the drift region on the n-side is made close to π and the doping concentration is chosen so that at the $\theta = 3\pi/2$ phase angle in the RF cycle (where the magnitude of the RF voltage is such that the electric field on the p-side just goes to zero at the p+ edge), the edge of the depletion layer on the n-side moves in to the proper value to meet the pulse of electrons at the proper time. The high-region or low-high-low region on the n-side is made as narrow as possible and concentration is chosen such that the field goes to 0.4 E_c at the beginning of the drift region.

2.1.4(a) Hybrid Double-Drift Device Design Summary

Using the above guidelines, a structure was designed with the following parameters:

p-Side :

Doping on p-Side	=	$8.65 \times 10^{15}/cm^3$
Length of Epi Layer on p-Side	=	3 micrometers

n-Side :

$N_D(p)$	= Doping Peak	=	$4.62 \times 10^{17}/cm^3$
X_p	= Distance to Peak	=	0.15 micrometer
Half Width		=	0.035 micrometer
Doping Concentration in Drift Region		=	$5 \times 10^{15}/cm^3$
Length of Epitaxial Layer		=	3 microns

2.1.4(b) Complete Double-Drift Device Design Summary

Highest predicted efficiencies and output powers are obtainable from structures with H-L or L-H-L profiles on both n and p-sides [8]. This so called full Read double-drift structured is composed of Read-type structures in n and p-type material, sharing a common avalanche zone. Exact design for such devices has been accomplished using computer simulation of device operation. Both a DC simulation developed at Microwave Associates and a large signal simulation developed at the University of Michigan have been used to arrive at the full Read double-drift device design used here. The design is as follows:

p-Side :		
High Region Doping	=	1.4×10^{17} acceptors/cm^3
High Region Thickness	=	0.2 microns
Low Region Doping	=	3.4×10^{15} acceptors/cm^3
Total p-Thickness	=	2.8 microns
n-Side :		
Peak Height	=	5.9×10^{17} donors/cm^3
Peak Half-Width	=	0.035 microns
Peak Position from Junction	=	0.1 microns
Drift Region Doping	=	5×10^{15} donors/cm^3
Total n-Side Thickness	=	2.9 microns

The results of the large-signal simulation appear in Table 2-I. The validity of this design has been investigated through large-signal simulation using a computer program developed at the University of Michigan.

J_{DC} (A/cm^2)	V_{DC} (Volts)	P_{RF} ($Watts/cm^2$)	EFFICIENCY (%)
500	92	14	31.2
750	94	24	34
1000	95	34	36
1500	98	50	34
1850	99	57	31

TABLE 2-1 OPERATING PARAMETERS FOR H-L/L-H-L DOUBLE-DRIFT DIODE AT 10 GHz FROM LARGE SIGNAL SIMULATION: V_{RF} = 75 Volts

Table 2-II presents the results of this simulation. As shown, 24% efficiency is predicted at 1000 A/cm^2 current density, with 24 watts peak RF output power at 10 GHz for a 14 mil diameter device.

2.2 Actual Doping Profiles Realized

Table 2-III presents doping profile data for all double-drift devices used in this program. Also listed in Table 2-III are the results of DC simulation for these wafers, where breakdown voltage, operating frequency, and conversion efficiency are tabulated. Also listed are design goals for each type of double-drift deivce as well as simulated results for the design goals. These design goals differ slightly from those resulting from the large signal simulation, and are included because they were used until the values from the large signal simulation were available.

Examination of Table 2-III highlights some of the problems encountered in growth of double-drift structures, namely, control of p-side doping, and accurate measurment of profile parameters. That parameter measurement was not accurate, can be determined from examination of Table 2-IV, where RF and DC operating parameters for devices made from these wafers are presented. Because the calculation of breakdown voltage given, the doping profile is quite straight forward and considered to be accurate, cases where discrepancies exist between calculated and measured breakdown voltage indicate errors in profile measurement. A detailed discussion of epitaxy and measurement procedures will be published in subsequent reports for ERADCOM. For the purpose of this program, those wafers listed in Table 2-IV met the requirements of 15 W peak output in X-band amd were used in the following reliability studies.

J_{DC} (A/cm^2)	X_A (μm)	E_c (V/cm)	V_{DC} (V)	V_{RF} (V)	G_D (mho/cm^2)	B_D (mho/cm^2)	η (%)
1,500	1.1	4.37×10^5	101	61	-18	106	23
1,700	1.1	4.38×10^5	102	58	-23	100	22
2,000	1.1	4.4×10^5	100	60	-24	105	22
1,250	1.1	4.37×10^5	101	60	-16	108	23
1,000	1.1	4.37×10^5	101	60	-13	110	24

At 1000 A/cm^2: Mesa Diameter = 14 mil

Peak Operating Current = 1 A

Peak Operating Voltage = 100 V

Peak Output Power = 24 W

TABLE 2-II OPERATING PARAMETERS DIODE FOR THE HYBRID DOUBLE-DRIFT DIODE DESIGN AT 10 GHz FROM LARGE-SIGNAL SIMULATION

WAFER NO.	TYPE	p-SIDE					n-SIDE					V_B (V)	f_o (GHz)	EFFICIENCY (%)
		HIGH REGION HEIGHT x 10^{16}	TRANSITION HALF WIDTH, μ	HIGH REGION WIDTH, μ	DRIFT DOPING x 10^{15}	TOTAL THICKNESS μ	PEAK HEIGHT x 10^{17}	PEAK HALF WIDTH, μ	PEAK POSITION μ	DRIFT DOPING x 10^{15}	TOTAL THICKNESS μ			
21118	Flat-Flat	---	---	---	2.9-6.5	6.5	---	---	---	12.0	5.4	57	11	3
21487	Flat-LHL	---	---	---	9.0	2.4	3.5	0.047	0.12	7.0	4.9	49	17	10
21539	Flat-LHL	---	---	---	2.8	2.4	3.0	0.034	0.11	7.0	4.5	80	13	1.7
21613	Flat-LHL	---	---	---	11.0	2.8	3.0	0.039	0.12-0.17	7.3	3.8	65	10.3	19
21624	HL -LHL	3.5	0.025	0.3	12-20	2.9	3.6	0.041	0.12-0.17	6.4	3.9	55	13	15
21693	HL -LHL	3.5	0.025	0.3	6-10	2.5	4.2	0.040	0.12-0.17	7.3	3.5	61	16	19
Design Goal	Flat-Flat	---	---	---	12.0	2.5	---	---	---	13.0	3.5	74	14	17
Design Goal	Flat-LHL	---	---	---	12.0	2.7	3.0	0.040	0.15	6.0	4.0	66	10.3	20
Design Goal	HL -LHL	8.0	0.025	0.19	8.5	2.6	3.85	0.045	0.15	6.7	4.0	54	10.4	24

TABLE 2-III DOPING PROFILE PARAMETERS AND SIMULATED OPERATING PARAMETERS FOR DOUBLE-DRIFT GALLIUM ARSENIDE WAFERS USED FOR RELIABILITY INVESTIGATION (DC Simulation)

WAFER NUMBER	V_B (V)	C_{T0} (pF)	V_{op} (V)	I_{op} (A)	P_o (W)	f_{op} (GHz)	η (%)	COMMENTS
21643-1	60 63	41	126	1.5	20.5	9.9	11	1.2 µsec, 30% Duty
21624-1	60	37	110	1.36	24	9.2	16.3	1.2 µsec, 30% Duty
21613-1	50	31	96	1.1	15.3	9.9	14.5	1.2 µsec, 30% Duty
21539-1	68	18	100	1.25	14.6	8.9	11.7	1.0 µsec, 25% Duty
21487-1	52	15	83	1.25	17.6	10.3	17	1.0 µsec, 25% Duty
21118	72	12	96	2.0	19	9.8	10	1.0 µsec, 10% Duty

TABLE 2-IV BEST MEASURED PERFORMANCE FOR DOUBLE-DRIFT GALLIUM ARSENIDE DEVICES

2.3 Device Fabrication

In this Section, the plated heat sink(PHS) process used at Microwave Associates for gallium arsenide IMPATT fabrication will be described. Both single-drift Schottky and double-drift processes are described separately where procedures differ.

High power GaAs devices incorporate plated heat sink (PHS) die fabrication methods, where a thick gold heat sink pad is plated on the epitaxial layer side of a GaAs wafer. The wafer is then thinned and mesas etched from the substrate side. The process is amendable to extended geometries (where mesa shape is not a single cylinder) particularly when ion milling is used to form the mesas.

2.3.1 Plated Heat Sink Device Fabrication

The plated heat sink (PHS) process steps are summarized in Table 2-V and Figures 2-4(b) and 2-5. In steps where procedures differ, the Schottky-barrier single-drift process as well as the p-n double-drift process is explained. The steps are as follows.

2.3.2 Incoming Wafer Inspection

The surface texture of a GaAs epitaxial wafer is very important in determining the performance of the microwave devices made from it. Uneven surfaces usually correlate with non-uniform active epitaxial layer thickness. Rough surfaces on Read L-H-L wafers are harmful since it causes non-uniform field distributions and result in soft breakdown voltages and poor power output levels.

FLOWCHART

OPERATION

INCOMING WAFER INSPECTION
LOT DOCUMENTATION
WAFER PREPARATION (Pre-Sputter Cleaning)
EPITAXIAL LAYER METALLIZATION
METALLIZATION ADHERENCE TEST
PROTECTIVE PLATING
GaAs FLAT LAP
WAFER CLEANING (Pre-Plating Clean)
HEAT SINK PLATING
WAFER CLEANING
SUBSTRATE THIN LAP
WAFER CLEANING (Pre-Polish Clean)
POLISH ETCH 1
PHOTO STEP #1 (Stress Relief Grid)
ETCH #2 (Grid Etch)
REMOVE RESIST
ETCH #3 (Substrate Tailor Etch)
WAFER CLEAN (Pre-Top Contact Cleaning)
TOP CONTACT METALLIZATION
PHOTO STEP #2
ETCH TOP CONTACT
STRIP RESIST
ETCH #4 (Remove Excess Back Contact Metal)
PHOTO STEP #3 (Mesa Mask)
ETCH STEP #5 (Etch Mesa)
STRIP RESIST
EVALUATION AND TAILOR ELECTRICAL SPECIFICATIONS
MECHANICAL INSPECTION
SEPARATE CHIPS

TABLE 2-V PHS PULSED IMPATT FABRICATION

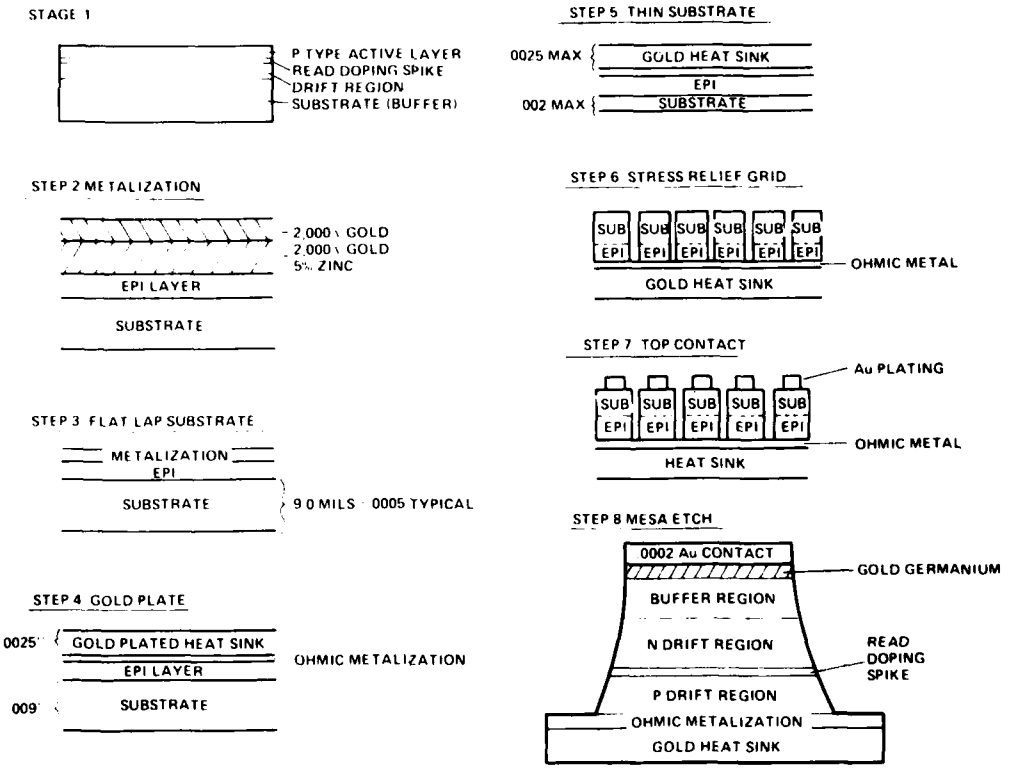


FIGURE 2-4(b) **STEPS IN THE PLATED HEAT SINK PROCESS** D-17299B

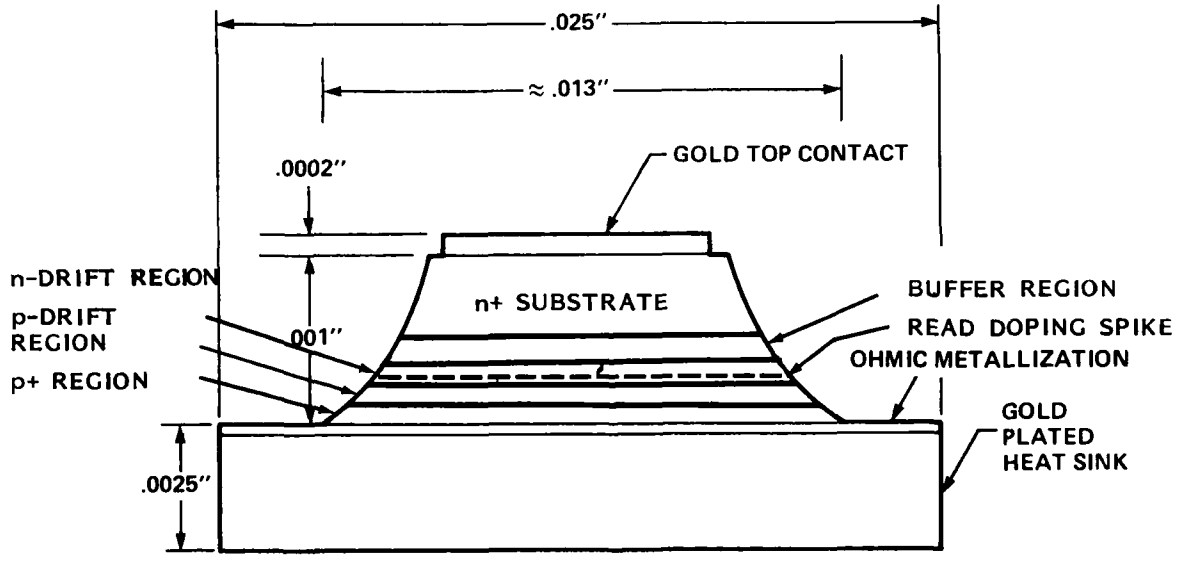


FIGURE 2-5 CROSS-SECTION OF A FINISHED CHIP

D-17298A

The first step is a visual inspection for qualification of size, useable surface, and location of surface hazes and defects. A photograph is taken of the wafer and mounted on a process card which contains all pertinent growth specifications. The types of defects which would cause rejection of wafers are: small or large pits, rough textured surfaces, hazes, scratches, stains or mounts. All of the above information is attached to the final evaluation sheet and filed to ensure lot traceability.

2.3.3 Metallization Procedure

(a) Single-Drift Schottky

One of the most important processing steps from the reliability standpoint is the Schottky metallization. Since junction temperatures of 250°C are not uncommon, intermetallic compound diffusion becomes a serious problem unless a metal layer is sputtered on the wafer which prevents the diffusion of the gold heat sink through the Schottky metal. Microwave Associates has achieved high performance devices and excellent reliability using the following method.

After a thorough cleaning, 200 Å of platinum is sputtered to form a Schottky-barrier metal followed by 1,500 Å of titanium to form a metal diffusion barrier. A second 1,000 Å of Ti is then sputtered onto the titanium layer to ensure reliability and to prevent oxidation of the titanium barrier. Finally, 2,000 Å of gold is sputtered over the wafer to protect the metallization during adherence testing.

(b) Double-Drift

The use of double-drift epitaxial wafers with a grown p+ layer has required a change in the typical method of metallization. Since the junction is not formed by a reaction of the platinum Schottky with the n+ epitaxy a low resistance ohmic contact metallization is necessary to initiate the PHS plating. Microwave Associates had always used gold (95%), zine (5%) metallization for the standard tuning varactor products. This metallization has been adapted for use on double-drift IMPATTs in the following manner.

After a thorough cleaning of the wafer, 2500 Å layer of 95% Au/5% zinc is evaporated on the p+ epitaxial side, followed by 2000 Å of gold. The wafer is then removed and sintered in a pure hydrogen atmosphere at 425°C for 30 seconds. The wafer is then subjected to an adherence test and prepared for the GaAs flat-lap operation.

2.3.4 Gallium Arsenide Flat-Lap

The thickness of each wafer is then measured at several points. A thickness profile map is obtained on the process sheet. Wafers meeting the flatness uniformity specification of ± 0.0001" are moved directly into gold plating. The selected wafers are mounted on a stainless steel block, and lapped and polished until desired parallelism is achieved across the wafer. Good control of flatness, parallelism, and nominal dimensional control is obviously critical in this process. Each surface serves as a reference surface when performing additional thinning operations. The final wafer yield is determined by the measure of control achieved. The final capacitance tolerance is also determined by the quality of each successive lapping operation.

2.3.5 Heat Sink Plating

The thermal resistance of large area pulsed IMPATT diodes is predominantly a spreading resistance. The resistance is inversely related to the conductivity of the heat sink material. Gold is currently used at Microwave Associates on GaAs single and double-drift IMPATTs. In all of the above three cases, it is important that the heat sink metal have a small grain size and high density for optimum thermal conductivity.

It has been established that solution concentration, agitation, temperature, contamination, and constant monitoring are factors which maximize quality and thermoconductivity on heat sinks. Absence of strains, edge build-ups, and variable current densitities also contribute to the best possible heat sink plating conditions.

Edge build-up is minimized by using a silver paste conductive ring. By controlling all of the above parameters, 0.003" stress free, heat sinks are plated consistently with less than ± 0.0001" variation and with no nodules or spikes and edge build-ups of less than 0.0002" in our IMPATT production laboratory.

2.3.6 Gold Lap

A flatness tolerance of ± 0.0001" throughout the lapping steps is necessary to maintain reasonable uniformity in device areas following the mesa etching step. Although gold plating results at Microwave Associates are usually within specification, additional gold lapping is done to standardize heat sink thickness at 0.0024". The operation is described as follows.

The wafers are mounted gold PHS side up on a flat, clean stainless lapping block, using a spray-on adhesive. Using the flatness from the original flat lap operation as a reference plane, the wafers are lapped mechanically using cutting oil and optical abrasive powders. It is important that parallelism be maintained to within 0.0001" since the gold heat sink is used as the reference for a subsequent thinning operation.

2.3.7 Subsequent Thin Lap

The thin lap operation serves to remove all but 0.002" of GaAs material which will be further polished down to less than 0.001". Any errors relating to parallelism will be reflected in the non-uniformity of the gallium arsenide. Thin lap is accomplished by mounting the wafer gold side down on a stainless steel lapping block with a spray-on adhesive. The wafer is then lapped with an optical grade grit mixed with a suspension treated cutting oil. Care must be exercised not to fracture the GaAs material as it is very brittle and thin at this point. The wafer is then dismounted, cleaned, and measured for uniformity.

In order to remove any embedded lapping compound and prepare the surface of the wafer for back metal, the wafer substrate is chemically polished in an agitated solution of 3:1:1 (3 parts sulfuric acid, 1 part hydrogen peroxide, 1 part DI water). At this point, the thickness of the substrate and epitaxial material is less than 0.001". If necessary, it can be thinned down to as little as 0.0005".

2.3.8 Stress Relief Grids

A matrix of 0.002" lines on 0.25" centers are exposed using the standard photo-resist proceudres on the polished GaAs. The GaAs is etched and separated into individual square pads. This relieves any stress due to flexing of the gold heat sink. The wafer is then stripped of photo resist, and cleaned. Now, the pad voltages can be easily measured to determine the approximate breakdown of the slice. If acceptable, the wafer is ready to be cleaned for back contact metallization.

2.3.9 Back Contact Metallization

A gold - germanium eutectic is evaporated to a thickness of 4000 Å and sintered at 375°C for 60 seconds. The wafer is then plated with a 0.0002" of gold to serve as a bonding surface for the top electrical ribbon connection. Back contact definition is accomplished using photo resist and conventional gold stripper.

2.3.10 Mesa Mask and Etch

A photomask which is 0.001" larger than the back contact mask is exposed over the existing dot or ring array. During the subsequent etching in an agitated 3:1:1 (sulfuric, hydrogen peroxide, and DI water) the final mesa structure is achieved. Once each device is etched to size, the wafer is stripped of photo resist and evaluated for voltage breakdown and capacitance. Additional etching may be required to bring the capacitance into a desired range. In doing so, additional undercut of the gold germanium back contact will occur.

Microwave Associates has developed a technique for eliminating excess metal overhang on its finished mesa devices. Photographs of several pulsed IMPATT devices are shown in Figure 2-6. The technique requires that a scanning electron microscope photograph be taken of a representative device from a wafer after tailor etching. Using the micron measuring standards included in the photograph, the exact mesa shape, size and any pertinent information regarding active layer defects can be documented.

At this time, an appropriate contact mask can be chosen and the back contact photo alignment step can be re-defined. When the back contact is etched, the undercut will be minimized and there will be no metal overhang. After packaging, selective etching can be accomplished, thus cleaning up the junction area of the device. Microwave Associates is confident that the additional performance achieved by this process provides our devices with a definite reliability advantage.

2.4 Assembly Methods

2.4.1 Die Bonding

Optimized bonding processes are necessary to insure the lowest possible thermal resistance on all types of IMPATT structures. A major problem in bonding plated heat sink chips is to maintain enough pressure on the chip during heating to insure the thinnest possible solder layer. A second problem involves the creation of an atmosphere which is conducive to optimum solder wetting without the use of flux.

FIGURE 2-6 STRUCTURE OF A SINGLE CHIP PULSED IMPATT DIODE WITH IMPROVED MESA CONSTRUCTION PROCESS

D-19837

In operation, a gold - tin solder preform is first placed into the package which is being held in a heater stage at temperature of 250°C. The PHS chips are then drawn by vacuum into a conventional tungsten - carbide collet and placed directly over the solder. A stream of heated-forming gas (80% nitrogen, 20% hydrogen) is directed at the bond area via a heater nozzle behind the die collet. Pressure is applied and continued until the solder has been melted and displaced by the chip. When the hot gas is shut off, the local temperature immediately decreases to 250°C and the solder is solidified.

Provided that the packages and solder are clean, temperatures are properly controlled, and proper bonding collet pressures are maintained, maximum performance can be expected from this bond. Chip damage is also minimized by the exact choice of bonding tips to insure that undue stress is not applied to the heat sink edges when the chip is held in the collet recess.

Minimum thermal resistance and bond integrity must be controlled by reducing the spreading resistance of both the plated heat sink and the gold - tin solder. These factors are optimized with a heat sink thickness of 0.0025" and a solder thickness of less than 0.005".

2.4.2 Wire Bonding

Following die bonding, the diodes are batch cleaned and prepared for visual inspection. The devices are inspected for several quality criteria which include cracked mesas, metallizaiton voids or defects in geometry, and incomplete solder wetting. Wire connections to the substrate side of the chips are made by thermo-compression bonding to the ohmic contact pads. Two separate gold

ribbons are attached to the die to minimize inductance. The ribbon site obviously depends on the size of the die. In general, 0.00025 x 0.005 gold ribbons are used.

Chip damage is minimized by maintaining a minimum of 0.15" thick top contact as well as monitoring the sharpness of the "wedge" shaped bonding tool.

2.4.3 Device-In-Package Etch

Junction etching of IMPATT devices involves the controlled removal of GaAs material from a packaged chip. Microwave Associates is convinced that top contact overhang is a serious threat to device stability and reliability. Our processes have been perfected to eliminate all forms of metal overhang while minimizing additional in-package etching. This decision requires that we evaluate each wafer while the junction area remains oversized. Sample devices are re-etched until the power and efficiency levels are optimized or the device meets a particular specification. The entire wafer is then etched to the upper limit of the required specification in a solution of 3:1:1. The actual mesa size is determined and the back contact diameter is redefined. The wafer is diced and assembled to the point where ribbon bonding has been completed. At this time, the combined device and package capacitance can be measured as well as breakdown voltage. In the present state, small amounts of junction damage may have occurred during fabrication. In situ etching now becomes a means of selectively etching the active epitaxial area of the device rather than the entire substrate and active area. A 10% solution of potassium hydroxide (KOH) dissolved in DI water is used to etch electrolytically the junction of the device. It is necessary to control this mesa shape to a maximum undercut of 15 microns to insure that small particles are not lodged in the

undercut region. Additional rinsing and neutralizing of the KOH etchant becomes necessary to insure device stability. A prolonged DI water stabilization rinse and isopropyl alcohol boil is carried out prior to a 60 minute bake at 150°C in forming gas (97% N_2 - 3% H_2) before hermetic sealing.

2.5 Device Evaluation

2.5.1 Introduction

IMPATT diodes are characterized by a low value of negative resistance. The RF test fixtures, therefore, have certain requirements for gallium arsenide IMPATT diodes. The test circuit used must transform the waveguide or coaxial line impedance (usually about 300 ohms in waveguide or 50 ohms in coax), to the diode impedance, with a minimum of resistivity loss. The test fixture must be able to resonate the device at the correct frequency. Finally, the test fixture should have the capability of easily adjusting both resistance and reactance to match the appropriate device impedance.

This Section presents an overview of device evaluation using both DC and RF tests. The DC tests include measurement of breakdown voltage, capacitance at zero bias and 80% of breakdown, forward voltage drop, and leakage current at 80% of breakdown.

2.5.2 DC Tests

2.5.2.1 Automated Testing

An automated test system has been designed and constructed, utilizing a Hewlett-Packard 2112 minicomputer as the processor. The computer is capable of operating the

test station while simultaneously controlling other real-time applications including the epitaxial growth reactors.

The system has the capability of measuring breakdown voltage (at 10 μA or 1 mA), forward voltage (at 10 μA, 1 mA, or 100 mA), leakage current (at 0.8 V_B), capacitance voltage characteristic, and capacitance ratios, etc. Again, all data can be stored and processed or sorted as selected. The kit may be connected either to a single diode test station or to an automated probing station (Teledyne Tac Model Number PR100). The probing station accommodates wafers or a 100-position packaged diode array. Software features include open and short detection and automatic polarity determination. The advantages of this system are speed and accuracy. A summary of all diode DC parameters and statisitcs for a typical 1.0 cm x 1.8 cm wafer are printed out in approximately 10 minutes. Capacitance and current measurements have an accuracy of ± 0.5% full scale and voltages can be set with 10 mV resolution. A system block diagram appears in Figure 2-7. Table 2-VI presents a sample of typical output.

2.5.2.2 Thermal Resistance Measurement

(a) Manual Measurement Method

The IMPATT diode thermal resistance measurement used at Microwave Associates is based on the temperature dependence of the diode breakdown voltage, i.e.:

$$V_B(T_J) = K_T (T_J - T_C) + V_{BO} \quad [2.15]$$

where

T_J = junction temperature, °C

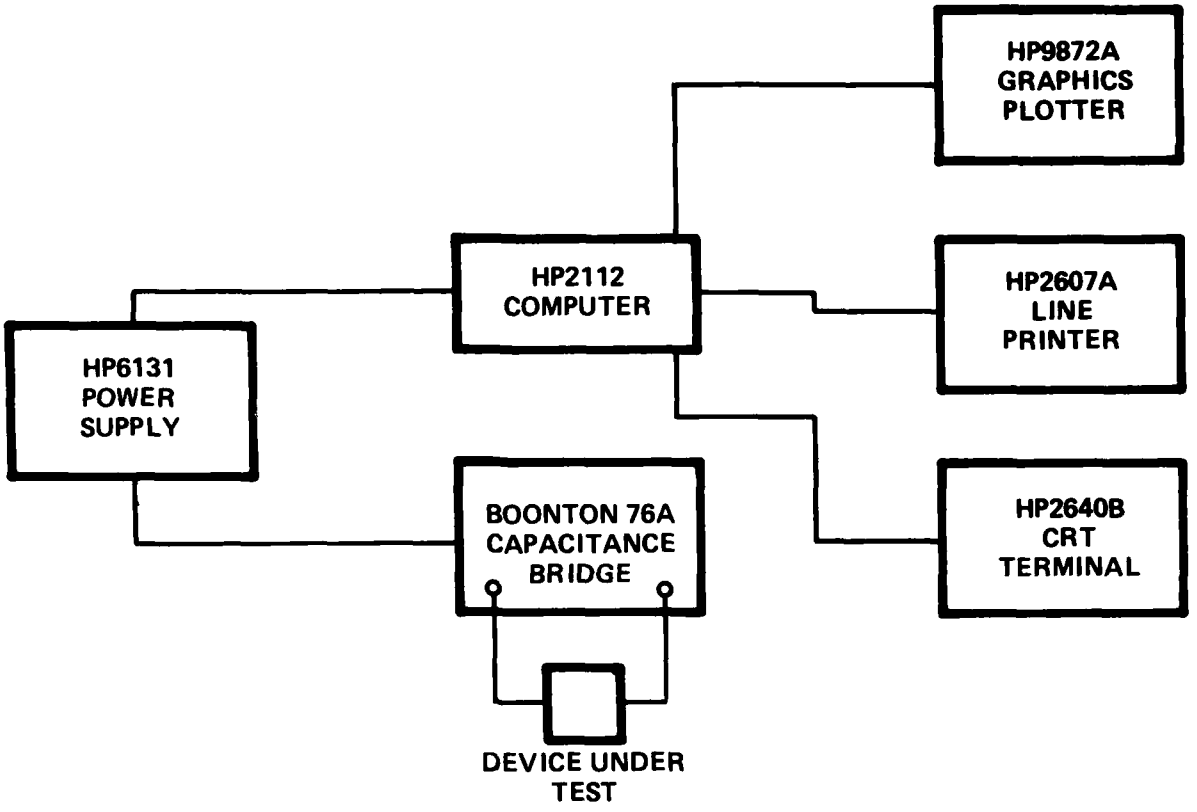


FIGURE 2-7 AUTOMATIC DOPING PROFILE MEASUREMENT SYSTEM

D-17305

7/1981 14: 1:58:89
MEASURED DATA FOR WAFER 21359-1A

(u=MICRO, M=MILLI)

#	VB1 V 10uA	VB2 V 1MA	VF1 V 10uA	VF2 V 1MA	VF3 V 100MA	V* V	C* pF	CTO pF 0V	C.8 pF .8VB	IL uA .8VB	TR 0V .8VB
1	66.89	68.88	-.88	-1.02	-1.49	8352.0	6.65	17.10	4.81	.003	3.6
2	67.18	69.26	-.86	-1.01	-1.48	5.43	7.94	15.91	4.55	.241	3.5
3	66.50	68.73	-.88	-1.03	-1.50	2.84	9.24	15.53	4.41	.063	3.5
4	67.47	69.41	-.87	-1.03	-1.49	8.57	7.11	16.22	4.67	.083	3.5

TABLE 2-VI SAMPLE OUTPUT DATA FROM AUTOMATIC IMPATT DIODE TEST SYSTEM

T_C = initial junction temperature (equal to case temperature, °C)

V_{BO} = breakdown voltage at $T_J = T_C$

K_T = temperature coefficient of the breakdown voltage, V/°C

The circuit of Figure 2-8 has been used. The diode to be measured is placed in a test fixture and biased at the operating point. Oscillations are suppressed by use of graphite load material in the diode mount. A negative-going pulse of 500 nanoseconds duration is introduced across the diode and the amplitude adjusted until the diode peak current equals the DC current. The pulse voltage required at the diode is then subtracted from the applied DC voltage to give a breakdown voltage value, measured with the junction at normal operating temperature. Because the pulse duration is much less than the chip thermal time constant, negligible cooling occurs. Using Equation [2.15], T_J, and thus, θ may be calculated if K_T is known. K_T may be measured by removing DC bias and applying external heat to the diode, while observing the pulsed breakdown voltage. In practice, breakdown voltage V_B is measured as a function of T_C for a few sample diodes from a given wafer and K_T determined from a best fit line drawn on a V_B versus T_C plot. Case temperature of 100, 150 and 200°C are used. The value of K_T obtained is then used to characterize the thermal resistance of other diodes from the wafer.

(b) Automated Thermal Resistance Measurement

Use of the thermal resistance measurement method described in the previous section is fairly time-consuming in that measurement of six parameters and subseuqnet calculations using Equation [2.15] is required. Microwave Associates has

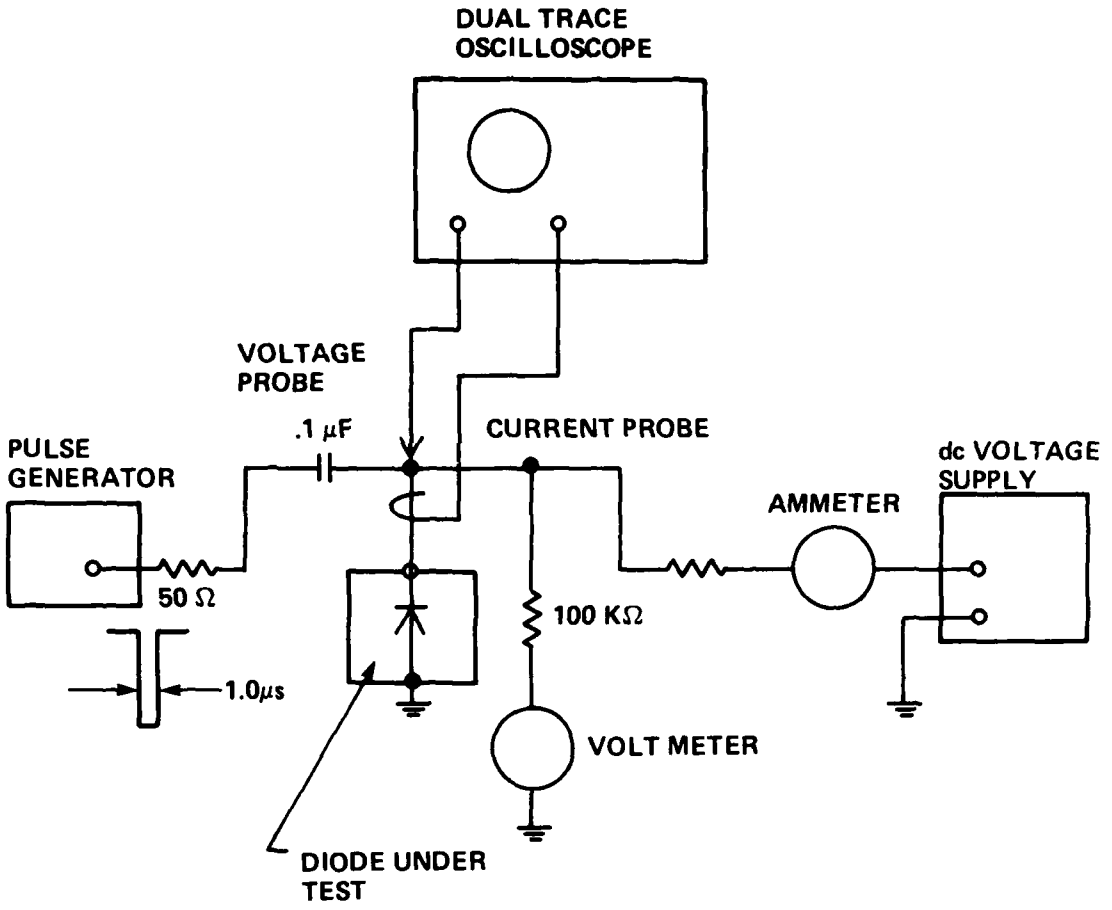


FIGURE 2-8 EQUIPMENT USED IN IMPATT THERMAL RESISTANCE MEASUREMENT

D-14019

purchased a commercially available thermal resistance measurement unit (Sage Enterprises Model Theta 120) that performs the measurement in five seconds and displays the resulting thermal resistance on a digital read-out. When the kit was purchased, the manufacturer was requested to modify the kit to perform measurements under the same conditions as the previously used manual method (i.e., breakdown defined at 4 mA). Agreement between the manual and automatic measurement methods has been excellent.

In addition to the Theta 120, a Sage Enterprises BFC16 breakdown voltage - temperature coefficient calibrator (K_T of Equation [2.15]), has been purchased. This instrument allows calibration of up to 12 devices at a time and incorporates a constant current source, eliminating frequency power supply adjustment as temperature is changed.

2.5.3 RF Tests

RF testing is carried out using the equipment shown in Figure 2-9. The device under test mounted in a coaxial test fixture is connected to a power detector through a tuner, isolator, and precision attenuator. Directional couplers are used to supply s singlas to a spectrum analyzer and diode detector. Pulsed bias is supplied from a Cober Type 604 pulse amplifier driven from a Hewlett-Packard Model 214A pulse generator.

The coaxial test cavity used is shown in Figure 2-10. The circuit uses an eighth wavelength long low impedance (about 12 ohms) transformer section followed by a seciton of 7 mm, 50 ohm air line terminated by a precision 7 mm connector. A sliding teflon slug transformer following the test cavity allows fine tuning of the impedance presented to the diode.

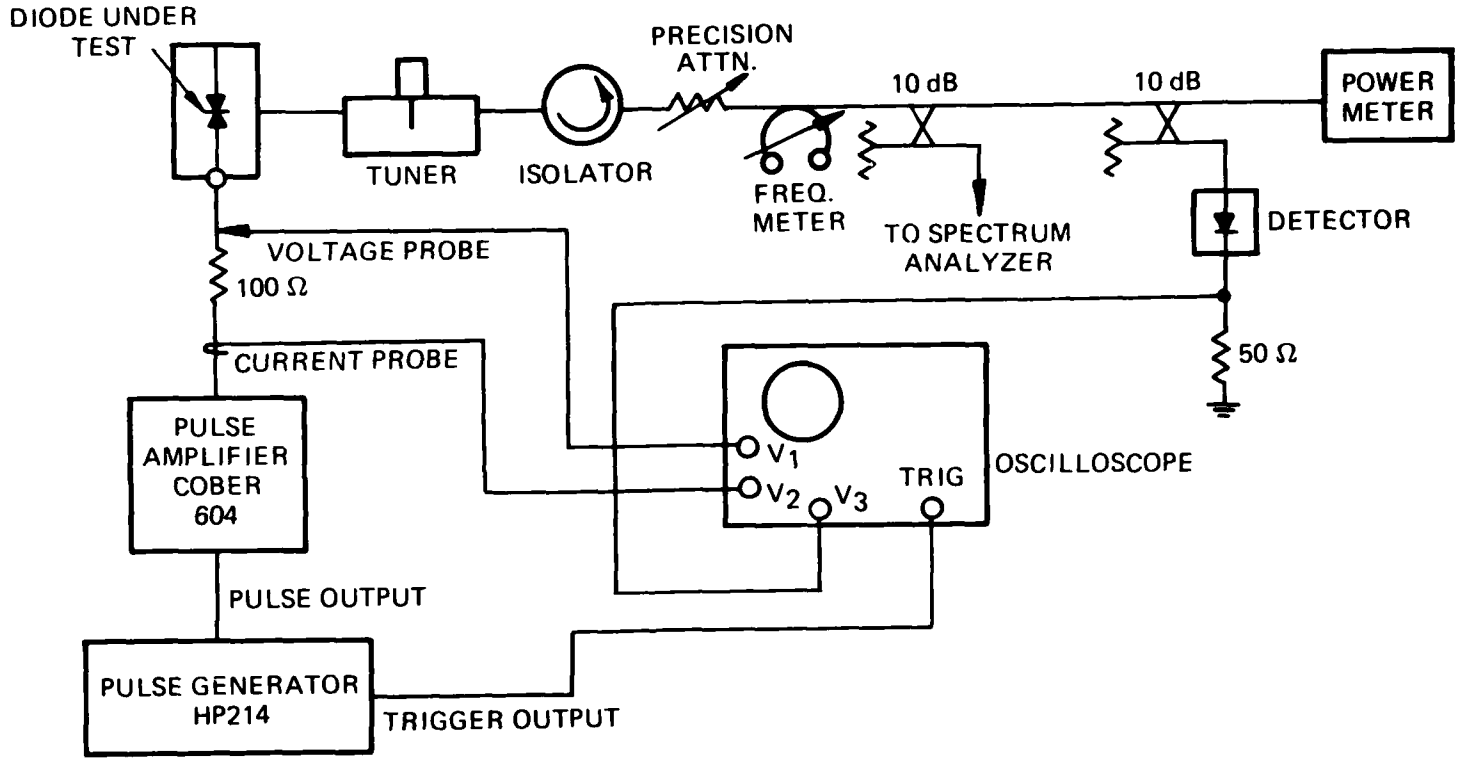


FIGURE 2-9 APPARATUS USED TO DETERMINE IMPATT DIODE DC AND rf PARAMETERS

D-16124

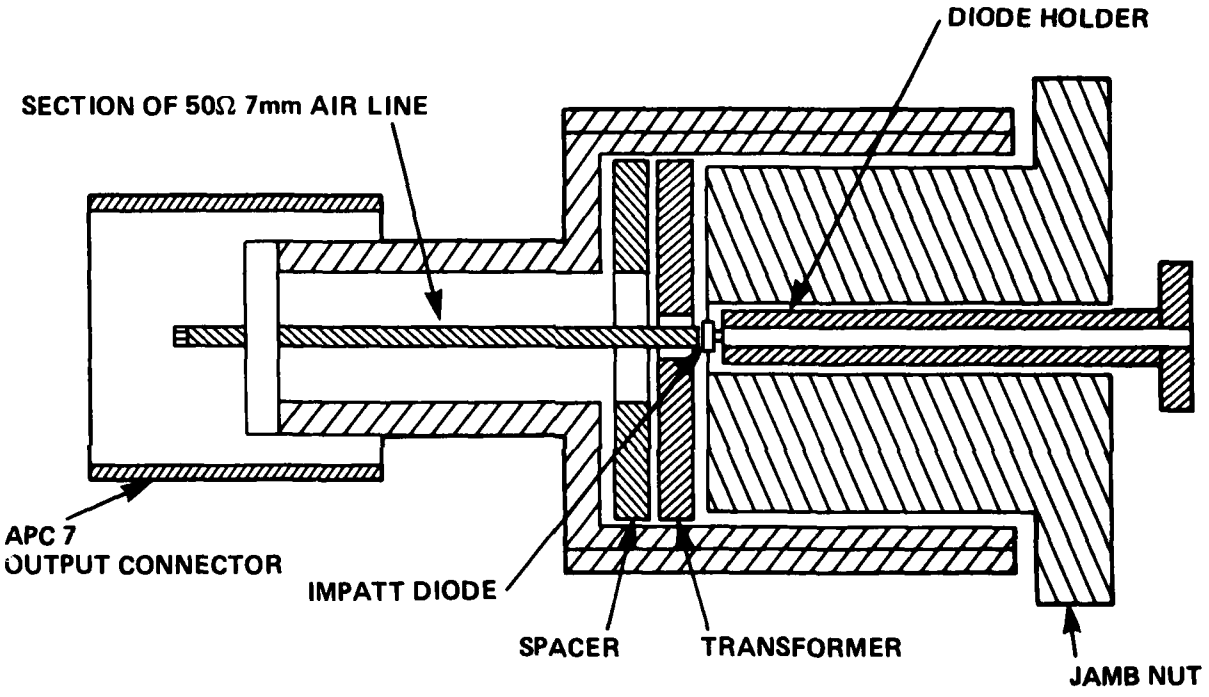


FIGURE 2-10 COAXIAL CAVITY IMPATT TEST FIXTURE

D-20437

The RF test station is used for determination of diode peak output power, efficiency, operating current, operating voltage, operating frequency, and conversion efficiency.

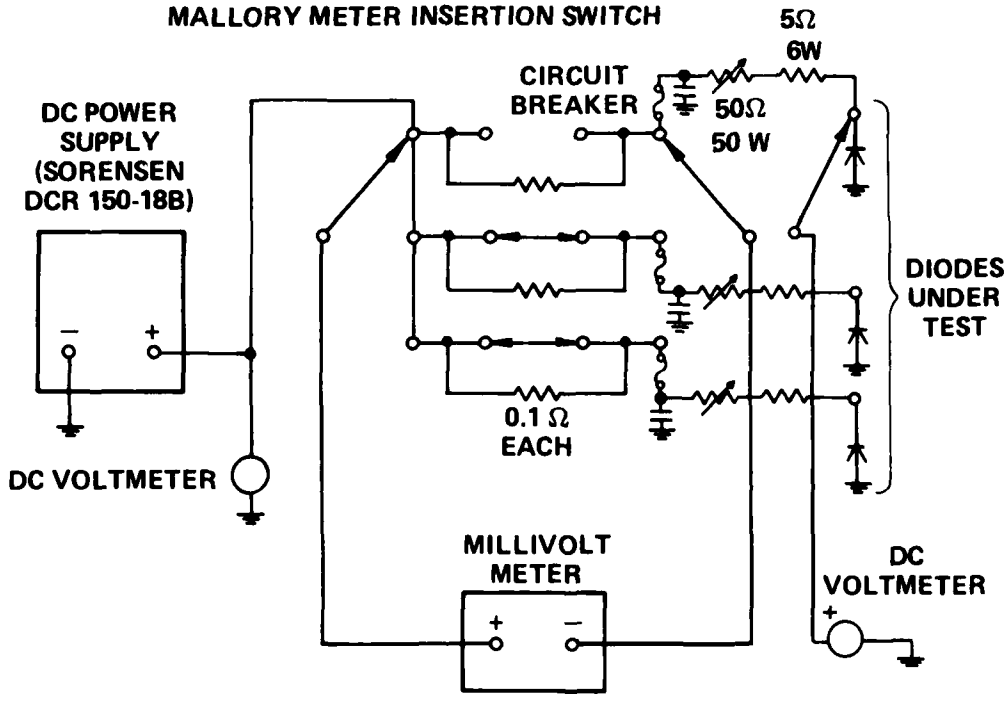
2.5.4 Equipment Used in Reliability Testing

2.5.4.1 DC Burn-In Equipment

Two 50-position IMPATT DC burn-in boards were used to perform the required DC burn-in testing. A schematic diagram of a portion of one board is shown in Figure 2-11. The equipment features controlled temperature circulating coolant, individual diode current adjust, complete metering, and individual circuit-breaker protection. Boards of this type have been in use for over five years, and have proven to be highly reliable. Protective circuitry is used that shuts down the board in case of low coolent level and prevents sudden reapplication of power following line power failure.

2.5.4.2 Pulsed DC Burn-In

A complete pulsed DC burn-in test kit with 30 device capability was loaned to Microwave Associates by Hughes Aircraft Company for use in this program. This unit, shown in Figure 2-12 provides individual pulse modulators for each device with 1.0 A, 143 volt output capability. Duty factors up to 50% can be maintained. A schematic diagram of thie pulse generator used appears in Figure 2-13. This unit also of Hughes design, provides a constant current output pulse and is protected against damage should an IMPATT fail by a shut-down circuit.



NOTE:
ONLY THREE DIODES ARE SHOWN, BUT EACH METER INSERTION SWITCH MAY BE USED TO MONITOR UP TO 12 DIODES, AND A TOTAL OF 50 DIODES MAY BE ACCOMMODATED SIMULTANEOUSLY.

FIGURE 2-11 IMPATT DIODE dc BURN-IN EQUIPMENT

D-11503A

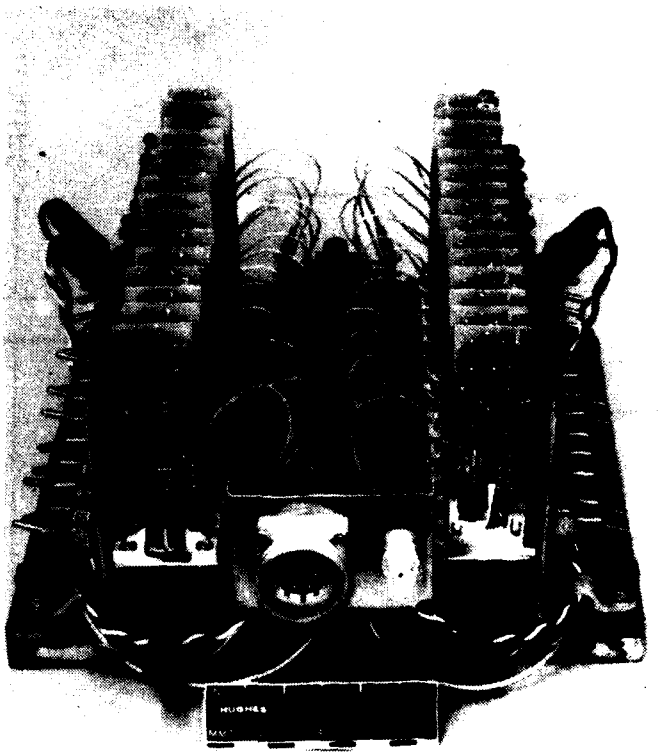


FIGURE 2-12 PHOTOGRAPH OF THE PULSED dc BURN-IN APPARATUS

D-20799

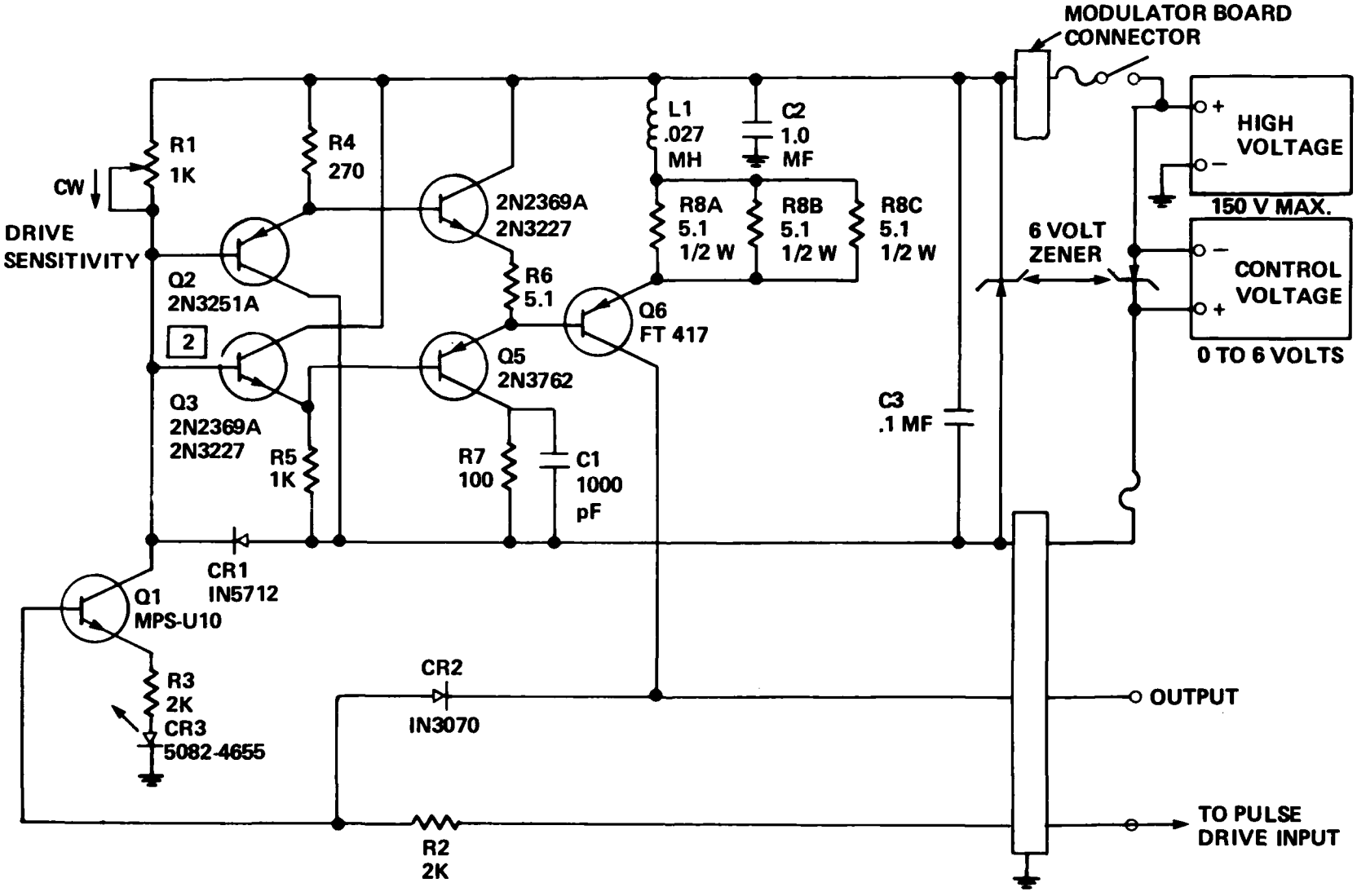


FIGURE 2-13 PULSE MODULATOR USED IN PULSED dc AND RF BURN-IN APPARATUS (COURTESY OF HUGHES AIRCRAFT CO.)

The diode under test are mounted in a water cooled plate and contacted by beryllium - copper fingers. Device case temperature is controlled by varying coolant temperature.

2.5.4.3 Pulsed RF Burn-In Fixture

The pulsed RF burn-in fixture allowed simultaneous testing of 30 devices. The board was divided into three groups of 10 devices with separate power supplies, allowing three types of devices to be tested simultaneously. The same pulse modulation design as used for the pulsed DC burn-in was used (see Figure 2-13). Appropriate fuses and Zener diodes were included to prevent failure of one modulator from effecting other units.

Shown in Figure 2-14 is the simplified version of the coaxial oscillator used in the pulsed RF burn-in apparatus. A single step impedance transformer was used, with compression spring to achieve reliable DC contact to the diode. Oscillator tuning to accommodate various diode types only required changing the transformer slug. The oscillator heat sink was bolted to a temperature controlled plate allowing diode case temperature to be controlled.

The complete RF burn-in assembly consisted of three master pulse generators to provide triggering for each group of 10 oscillators, a low voltage power supply for output amplitude control, and a high voltage supply to provide the pulse output. Each oscillator was connected to a high power coaxial attentuator and diode detector. At weekly intervals during the testing, the diode detector was removed and a thermistor mount attached for output power monitoring. A sketch of the overall RF burn-in assembly appears in Figure 2-15.

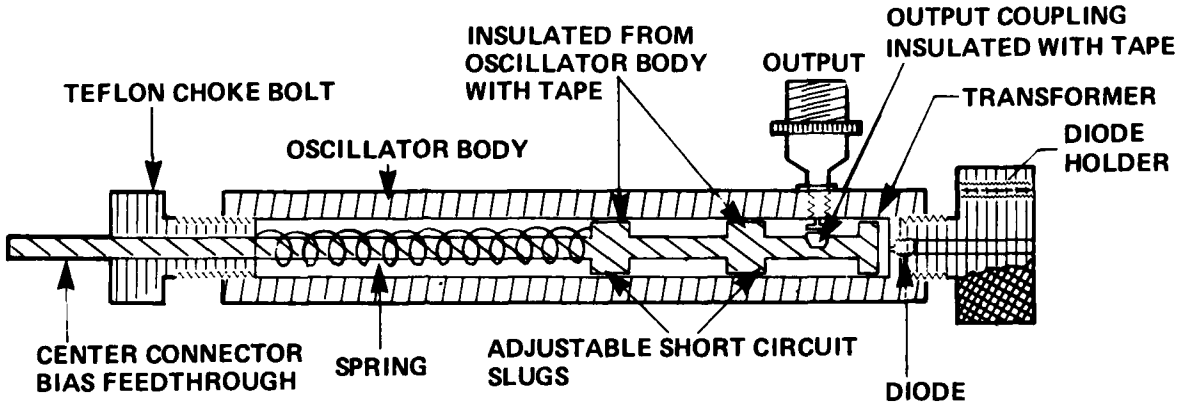


FIGURE 2-14 COAXIAL TYPE IMPATT TEST CAVITY USED IN RF BURN-IN APPARATUS

D-19675

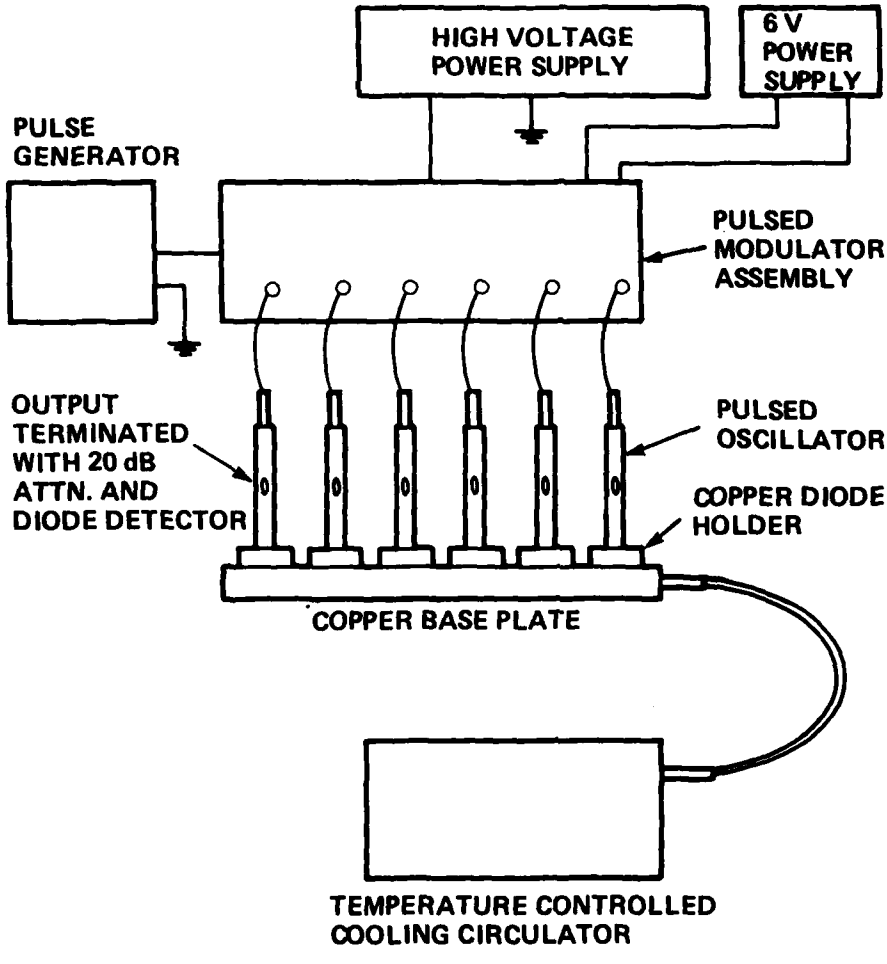


FIGURE 2-15 RF BURN-IN APPARATUS--SIX OF THIRTY POSITIONS SHOWN

D-20828

2.6 Failure Analysis

2.6.1 Microwave Associates' Failure Analysis Lab

The Failure Analysis Laboratory incorporates a scanning electron microscope, X-ray energy analyzer, sample coating sputtering unit, optical microscopes, and an area for mounting and cross-sectioning samples.

The nucleus of the laboratory is the AMR Model 1200A scanning electron microscope (SEM) fitted with EDAX Model 711 X-ray energy analyser. The model 1200A is capable of 70 Å resolution, and has magnification variable from 20X to 30,000X including 5X-zoom. The basic instrument incorporates 2¼ inch diameter sample holder with 40 mm working distance and 90° tilt capability, 4 cubic inch chamber, and 2 minute pump down. Purchased options include gamma non-linear amplification control (provides enhanced contrast for looking into depressions), split screen images with different magnifications, autofocus control (keeps top and bottom of image in focus on tilted specimens), and calibrated micron marker; either backscatter, secondary, or mixed emission modes may be chosen.

The model 711 X-ray analyzer provides elemental X-ray microanalysis capability of elements with atomic number greater than 11. Using a Nova 8K minicomputer, the system is capable of identifying 80 elements using K, L, and M line markers, and atomic number selection from the keyboard. Spatial resolutions of the identification area is 1 micron. Options purchased with the system include a line scan rate meter and map accessory. The line scan rate meter is useful for superimposing on a SEM micrograph, a line scan for concentration of a certain element. The area map accessory produces a SEM

X-ray map search for a chosen element, yielding an image of enhanced brightness where a high concentration of the chosen element exists. The map option also allows bar or outline mode operation.

To facilitate sample coating, a small sputtering system has been purchased for use with the SEM. This system, the Technics Model Hummer II, has capability to deposit either a gold - palladium alloy for SEM work, or a carbon to use with the X-ray analyzer. A five minute cycle time to produce a 200 Å coating is featured.

Additional analytical instrumentation includes the Research Devices, Inc., IR microscope. Using an IR illuminator and image converter, the unit renders semiconductors with bandgap equal to or wider than that of silicon transparent, and allows viewing of contacts, dislocations, metals precipitates, and gross doping fluctuations.

2.6.2 Failure Analysis Procedure

All failing diodes were submitted for failure analysis, however, where the same failure mechanism was indicated by electrical and visual means, only representative samples were investigated in depth.

The following steps were followed in failure analysis. First, the device was visually examined externally for physical damage such as a cracked ceramic. Second, electrical parameters were recorded if the device had not failed to an open or short condition. Changes in breakdown voltage, capacitance at zero bias, leakage current at 25 and 150°C and 80% of breakdown, and RF performance

were recorded. Third, the device cap was removed, and the chip examined optically and recorded photographically. Cap removal was accomplished by cracking away the top portion of the ceramic. In selected cases, the caps were ground away leaving the connection leads intact. Then, experiments such as in-package etching could be performed to see if recovery was observed in RF performance. Fourth, a portion of the ceramic was ground away using a jeweler's abrasive wheel, allowing chip examination with the SEM. Any unusual surface conditions were recorded photographically. Fifth, depending on the conditions observed in previous steps, further investigation was carried out. In some cases, if surface abnormalities were observed, electron microprobe analysis was used. If no apparent cause of failure was found, the gallium arsenide portion of the chip was etched away to reveal any contact abnormalities such as dendrite growth or metal electromigration. In other cases, the device was potted and cross-sectioned for further SEM and microprobe examination.

Each failure analysis step and results were documented in a failure analysis log. Failure analysis steps are summarized in Table 2-VII.

(1) EXTERNAL OPTICAL EXAMINATION

(2) ELECTRICAL TESTS

(3) INTERNAL OPTICAL EXAMINATION

Possible in-package etching for electrical recovery.

(4) SEM EXAMINATION

Possible microprobe analysis of surface.

(5) INTERNAL ANALYSIS:

(a) Etch Removal of GaAs and SEM Examination

(b) Cross-Section and SEM and Microprobe Examination

(6) DOCUMENTATION

TABLE 2-VII FAILURE ANALYSIS PROCEDURE

3.0 EARLY FAILURE REGION TESTING

3.1 Introduction

In the early failure region testing program, various screening methods were evaluated for use in removing defective or damaged units from the population. Such burn-in tests are commonly used in the semiconductor industry to insure that delivered units are of high quality and free of manufacturing defects. Traditionally, for junction devices, high temperature storage, or high temperature reverse bias (HTRB) storage have been used as burn-in procedures. However, in the case of high power dissipation small cross-sectional junction area microwave devices work [6,7] has shown that a burn-in with DC operating voltage and current present is essential. Such operating burn-ins stress devices with their maximum recommended case temperature, for periods varying from 24 to 168 hours. As shown previously for Gunn devices, in such a DC burn-in, most failures occur within the first half hours of operation, with 96% of the failures occurring after 24 hours and 99.5% after 72 hours.

When faced with the choice of an operating dissipation level burn-in, one must consider the trade-off between test complexity and cost (and test kit reliability) versus effectiveness of the burn-in in removing freak failures from the population. In the present study, high power pulsed IMPATT devices were to be tested and the most cost effective burn-in procedure determined. Three test methods were considered, DC burn-in, pulsed DC burn-in, and pulsed RF burn-in. Each method will now be described.

3.1.1 DC Burn-In

In DC burn-in, a constant (DC) voltage is supplied to the device through a 50 Ω series resistor. The voltage is increased until the unit draws avalanche current as required to produce maximum rated power dissipation. The devices under test are mounted in threaded copper holders, and in turn attached to a temperature controlled base-plate. The top of the device contacted with a spring leaded probe. No RF circuit is present, and oscillations do not occur. The plate temperature is controlled by either heating or cooling the flowing coolant as required. Individual diode case temperatures cannot be controlled and may vary slightly due to mechanical integrity of each unit. Each device is protected with an individual circuit breaker (650 mA typical), and the entire rack is equipped with over temperature, low coolant level, and primary power fail safety devices.

3.1.2 Pulsed DC Burn-In

The pulsed DC burn-in test includes the same type of diode mounting and temperature control methods as the DC burn-in with the complication that the bases of the devices are not accessable for case temperature measurement during test. Each device is supplied with pulsed constant current bias from an individual probe amplifier. Diode operating parameters are measured by connecting the current and voltage probes of an oscilloscope to each device in turn. Pulse amplitude is not controlled individually, but is adjusted for all positions at once requiring that the devices tested have nearly identical operating voltages.

Pulse width and duty cycle may be adjusted over a wide range. Because it was desired that increased junction temperature would be the primary stress causing failure a high duty test waveform (1 microsecond, 25% duty) was generally used. At lower duty, the required dissipation could not have been achieved within the current limitation of the pulse generators.

Pulsed DC burn-in increases the stress under which the devices are operated above the level seen during DC burn-in because higher voltages and currents are applied to the device, and due to external heating, the thermal stress is greater. In pulsed burn-in, the chip is actually being temperature cycled at the pulsing frequency causing internal mechanical stress because of the differential expansion coefficient of gallium arsenide and the plated gold (or silver) heat sink (versus $14.2/°C \times 10^6$ for gold). Thermal cycling stress would actually be more severe in wide pulse operation, because the chip temperature excursions would be more extreme. However, the waveform chosen here was selected because it is most commonly encountered in application of these devices.

The level of the stress due to differential expansion can be assessed if the junction temperature rise during the pulse is known. The approximate thermal excursion during pulsed operation for gallium arsenide single-drift Schottky and double-drift devices have been measured and is plotted in Figures 3-1 and 3-2. The measurement was made by calibrating the device operating voltage with junction temperature using a short low duty cycle pulse to avoid self heating. The diode, mounted in a non-oscillating test fixture was externally heated to provide the calibration. The junction temperature was determined as a function of time, also using the non-oscillating test fixture, but with a wide pulse. Operating voltage during the pulse was then translated into junction temperature.

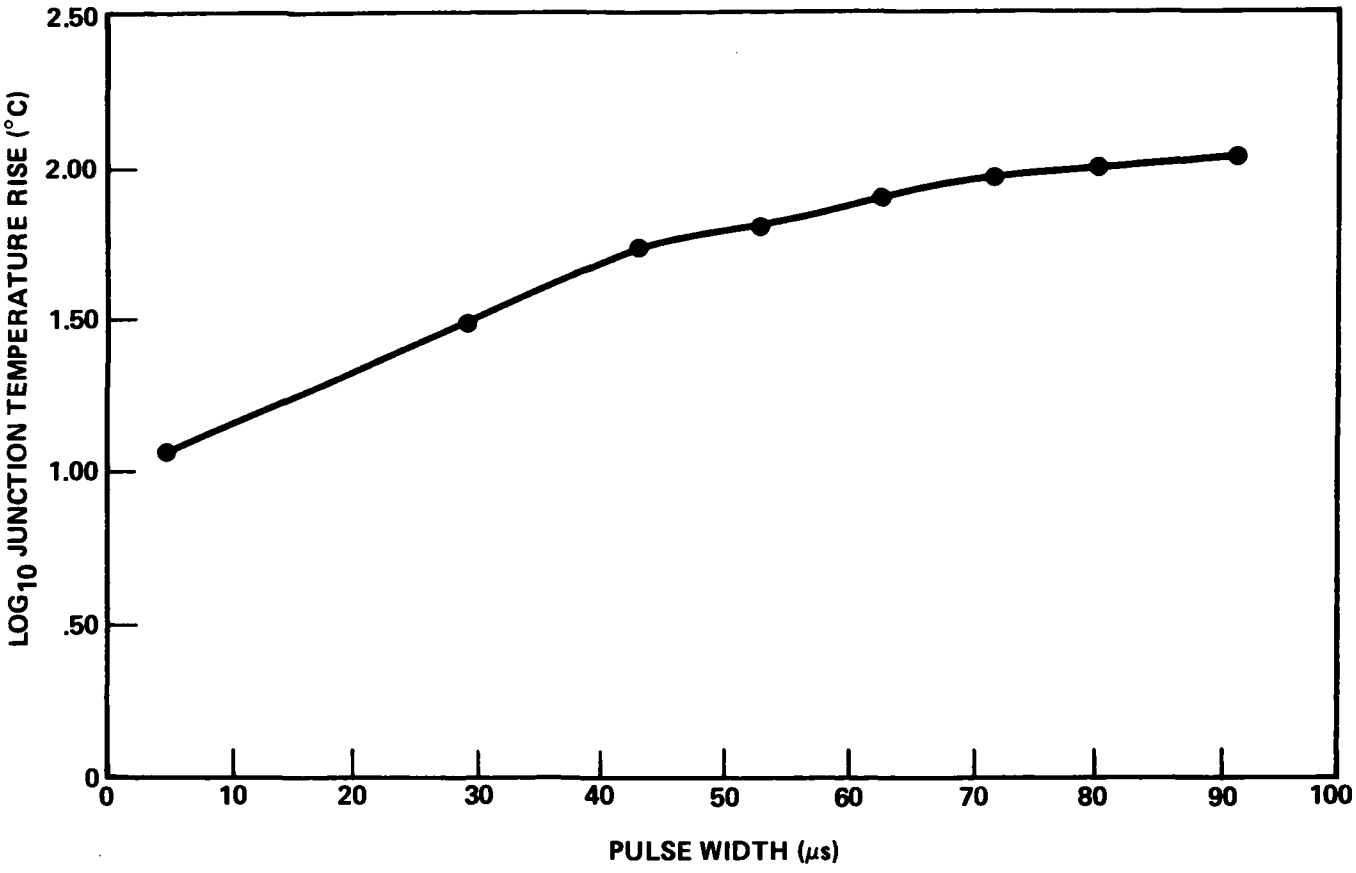


FIGURE 3-1 LOG OF JUNCTION TEMPERATURE RISE ABOVE AMBIENT vs. TIME FOR SINGLE DRIFT GaAs DEVICE (25° C AMBIENT)

D-20827

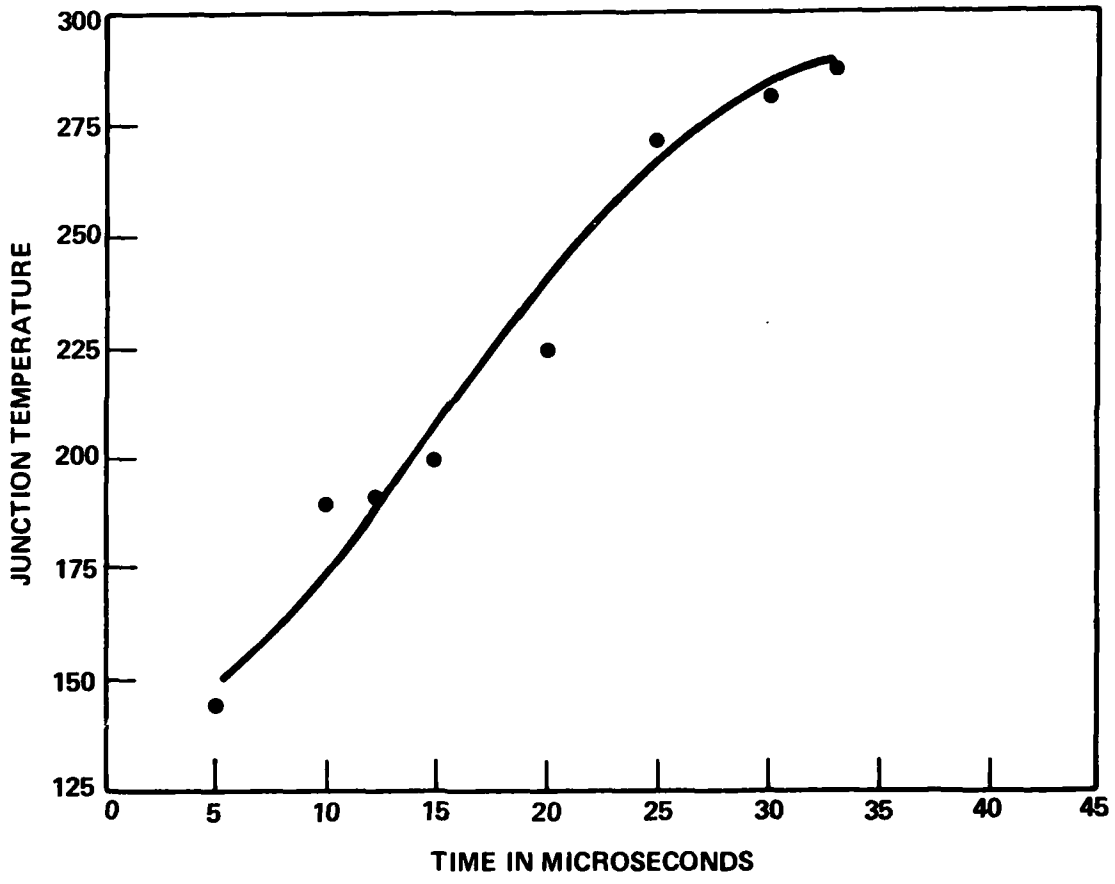


FIGURE 3-2 JUNCTION TEMPERATURE RISE AS A FUNCTION OF TIME FOR DOUBLE DRIFT DEVICES IN THE NON-OSCILLATING CONDITION.

D-20826

As shown, negligible junction temperature rise above average occurs for one microsecond pulse width, allowing average junction temperatures to be used in interpreting pulsed DC and RF test data.

3.1.3 Pulsed RF Burn-in

The most severe screening evaluated here was the pulsed RF burn-in test. In pulsed RF burn-in individual devices were monitored in oscillators to RF attenuators and diode detectors. Again, individual pulse modulators are used, this time with separately adjustable pulse amplitude controls. Each oscillator is attached to a temperature controlled base-plate.

In operation, oscillator tuning is adjusted to obtain operation with a minimum of spectral distortion. Average power dissipation and case temperature are again set to the rated maximum, with a correction being made for output power. During initial set-up, retuning was normally needed after case temperature stabilized. During tuning, a power meter is connected in turn to each oscillator and operating parameters are measured by connecting the current and voltage probes of a monitoring oscilloscope. Indicators LEDs warn of device failure during operation when the power meter is not in place.

Because of increased electric field associated with large signal oscillations, the stress level achieved during pulsed RF burn-in exceeded that of DC or pulsed DC burn-in. That is, the case had been demonstrated through experiences both at Microwave Associates and other laboratories where devices surviving DC burn-in occasionally would fail during subsequent RF testing. Determining if pulsed DC burn-in could replace RF burn-in as a screening method was one of the goals of the Early Failure Region testing sequence.

3.2 Test Results

3.2.1 Single-Drift Schottky Devices

DC and pulsed DC burn-in have been compared for effectiveness in removing defective devices from a population of untested single-drift, Schottky junction, L-H-L profile, gallium arsenide IMPATTs. These devices were nominally capable of 10 watts peak output at 1/3 duty cycle 1 microsecond, pulse width, and 9 GHz.

Twenty-five (25) devices were placed in DC burn-in at 16.9 W dissipation and 95°C case temperature (70°C heat sink). The thermal resistance averaged 7.7°C/W placing the junction at 224°C. Five (5) units failed during the 48 hour test. Thirty (30) units were placed on pulsed DC burn-in at 1/3 duty cycle and 1.0 microsecond pulse width. An 80 volt, 0.64 A peak operating point was chosen placing the input power dissipation at 17.1 watts. A 67°C heat sink temperature was used. The exact diode case temperature could not be measured in the pulsed burn-in apparatus, but a 42°C case temperature was assumed, producing a 224°C junction, as in the DC burn-in. Two (2) diodes failed in the 48 hour test. Tables 3-I and 3-II summarize these results.

Following these burn-in tests, all diodes were RF tested to 1.1 A peak at 1/3 duty cycle and 1 microsecond pulse width. In the past, devices surviving DC burn-in have often failed during RF test, indicating that DC burn-in is not sufficient screening. During RF test at 1.0 A peak, 62 V peak, assuming the diodes are generating 3.3 watts average, power dissipation is about 17.4 watts. Case temperature during RF testing was about 75°C placing the junction at about 209°C.

During these tests, four (4) additional diodes failed from the nineteen (19) surviving DC burn-in, while seven (7) of the twenty-eight (28) surviving pulsed DC burn-in failed. As a tentative conclusion, the pulsed burn-in appeared to be no more effective in removing defective units from the lot than DC burn-in, for single-drift Schottky devices.

TEST	NO. OF STARTS	NO. OF FAILURES	PERCENT FAILURES
DC Burn-In	25	5	20
Pulsed DC Burn-In	30	2	6
RF Test after DC Burn-In	20	4	20
RF Test after Pulsed Burn-In	28	8	28.6

TABLE 3-1 COMPARISON OF DC AND PULSED NON-OSCILLATING BURN-IN TESTS FOR SCHOTTKY JUNCTION SINGLE-DRIFT DEVICES

BURN-IN TEST	V_o (VOLTS)	I_o mA	T Base-Plate °C	T_{CASE} °C	P_D (W)	T_J °C	TIME (Hrs)
DC	75.1	225	70	94.5	16.9	224.5	48
Pulsed	80.1	640	67	92 (est)	17.1	224	48

NOTE: Diode case temperature could not be measured directly in the pulsed burn-in apparatus. The same differential between diode case and base-plate as in the DC case was assumed.

TABLE 3-II BURN-IN CONDITIONS USED FOR EARLY FAILURE REGION TESTING OF SINGLE-DRIFT GaAs DEVICES.

RF burn-in would be required to eliminate early failures and guarantee with high probability that devices would not fail in service.

3.2.1.1 Failure Analysis for Single-Drift Devices Failing in DC or Pulsed DC Burn-In

The defects responsible for failure of these devices in burn-in are those common to other high power semiconductor devices. These defects include cracked chips, poor bonding and chip damage in handling. Some examples of such failures are shown in Figures 3-3 and 3-4. Figure 3-3 shows two views of a chip failing due to a cracked mesa. In the second view, the top contact has been removed revealing clearly the cracked mesa. The cracks have been accentuated by the etch.

In Figure 3-4, a device with a center region failure is shown. Such a failure is probably due to mesa damage at the top bond (ribbon connection) point due to use of excessive pressure.

Figure 3-5 shows a typical edge burn-out failure, The extreme heat generated during failure has vaporized the gallium arsenide in the failure region. Such failures may be due to defects or grain boundaries in the substrate which lead to corresponding defects in the epitaxy (see Figure 3-6) or lot spot formation due to poor bonding. Although the center of the mesa would be expected to experience the higher temperature, edge burn-out would be expected because of the higher electric field in the area of any irregularities in mesa shape.

(a) WITH METALLIZATION

(b) FOLLOWING REMOVAL OF TOP METALLIZATION

FIGURE 3-3 TWO VIEWS OF A DEVICE THAT FAILED IN dc BURN-IN DUE TO A CRACKED CHIP

D-20806

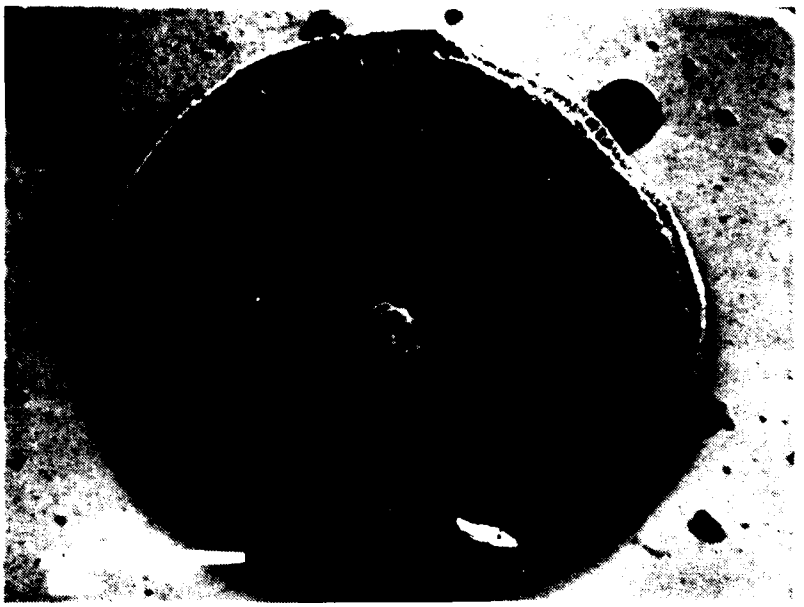


FIGURE 3-4 TOP VIEW OF A DEVICE AFTER FAILURE IN PULSED dc BURN-IN. THE TOP CONTACT METALLIZATION HAS BEEN REMOVED REVEALING THE FAILURE SITE UNDERNEATH THE WIRE-BOND AREA

D-20771

FIGURE 3-5 SIDE VIEW OF A DEVICE FOLLOWING FAILURE IN dc BURN-IN

D-20772

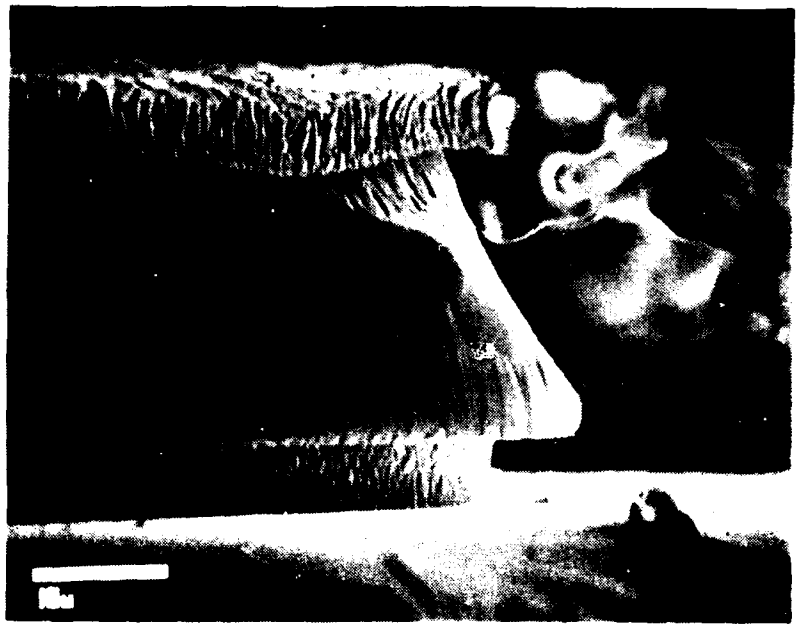
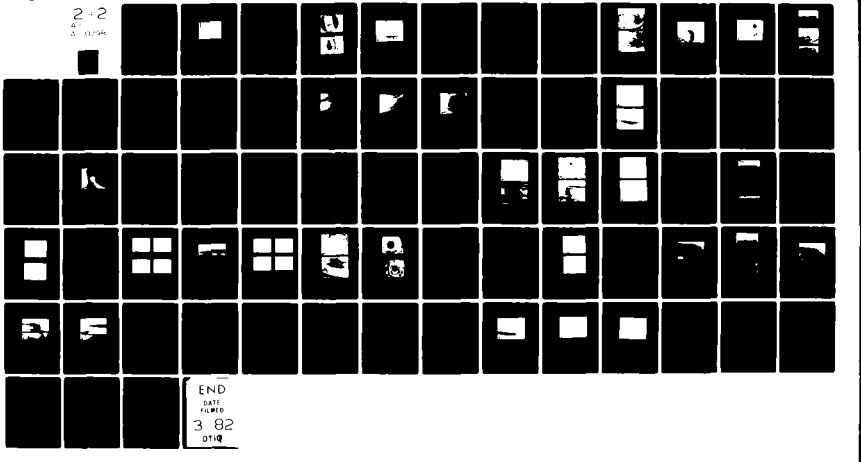


FIGURE 3-6 SIDE VIEW OF A DEVICE EXHIBITING IRREGULAR ETCHING IN THE SUBSTRATE REGION

D-20773

AD-A110 798 MICROWAVE ASSOCIATES INC BURLINGTON MA F/G 9/1
RELIABILITY OF HIGH-POWER PULSED IMPATT DIODES.(U)
NOV 81 M S AYYAGARI, J L HEATON, N JANSEN F30602-79-C-0210
RADC-TR-81-315 NL

UNCLASSIFIED



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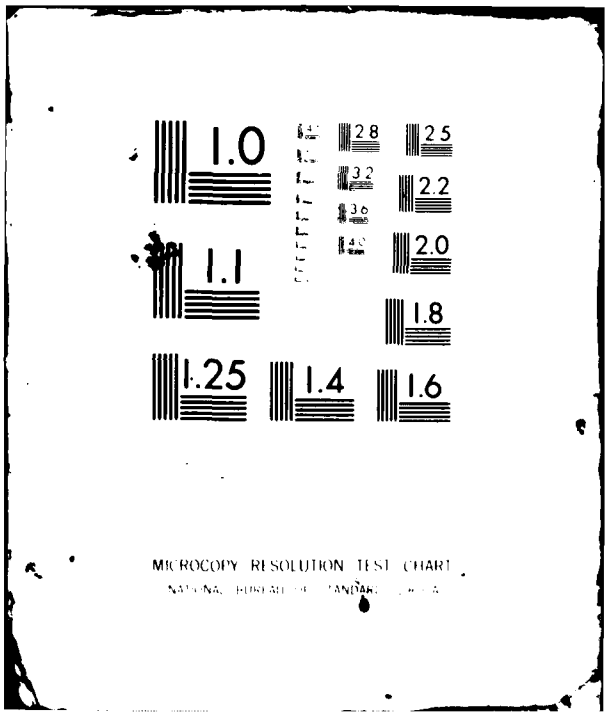

1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART

3.2.2 Silicon Double-Drift Devices

Silicon flat-profile double-drift devices were purchased from Hewlett Packard (part number 5082-0710). These devices were supplied with test data indicating an output power capability of 12.8 W at 10 GHz with 150 volts and 800 mA operating parameters. Efficiency was 10.5 to 11% at one microsecond 25% duty operations. Thermal resistance was quoted as 6.5 to 7.0°C/W.

After some initial difficulty, the quoted performance was verified in the standard coaxial test fixture . A 7 ohm transformer section was used. Because the silicon diodes were supplied in an unthreaded heat sink package, a special diode holder was required. This holder was constructed according to Hewlett Packard specifcations, and contained a collet assembly to securely hold the diode. Although this collet allowed initial RF testing of the device, they could not be installed in any of the reliability test fixtures. All burn-in boards had been made to accept devices with 3-48 threaded bases. To allow installation of the silicon devices in the burn-in boards, threaded adaptors were made from tellerium copper and soldered into the prong bases of the silicon devices. Thermal resistance and output power measurements made before and after soldering indicated no performance degradation. Figure 3-7 shows examples of devices with and without adaptors.

Ten (10) devices were used in each of the burn-in tests conducted. In the DC burn-in test, 14 watts of dissipation and 85°C diode case temperature were used, placing the junctions at approximately 180°C. None of the ten devices failed. The pulsed DC burn-in test was conducted at 350 mA peak pulse current, 150 volts peak, and 90°C diode case temperature. One device failed, indicating that DC and pulsed DC burn-in were of approximately equal effectiveness in producing failures.

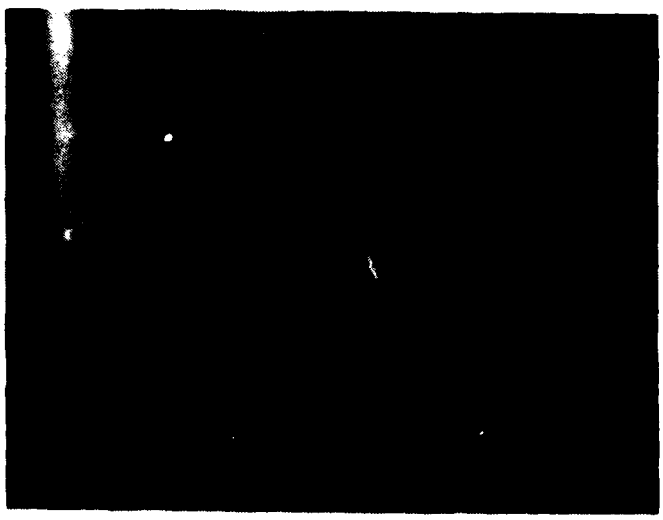


FIGURE 3-7 HEWLETT PACKARD SILICON IMPATT WITH AND WITHOUT THREADED ADAPTOR FOR USE IN BURN-IN APPARATUS

D-20774

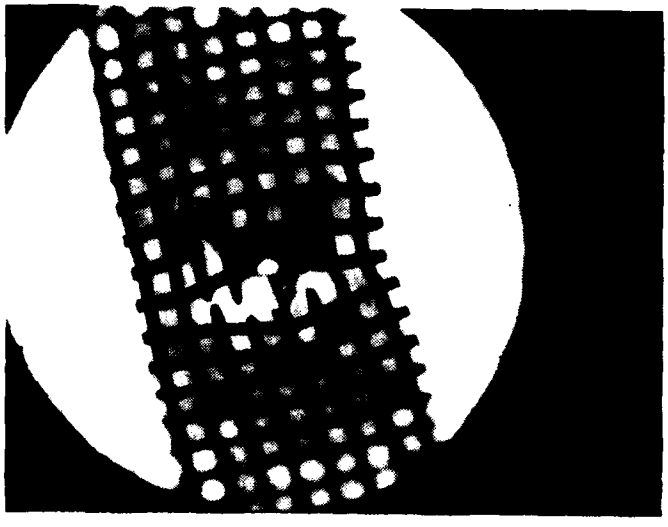
Devices were RF tested following burn-in, and in general, exhibited no change in performance. No additional devices failed, indicating that RF burn-in would not be more effective than DC burn-in for the silicon double-drift units. However, the units were pre-screened at Hewlett-Packard, eliminating other potential RF failures. Test results are summarized in Table 3-III and 3-IV.

3.2.2.1 Failure Analysis of Silicon Double-Drift Devices Failing During Early Failure Region Testing

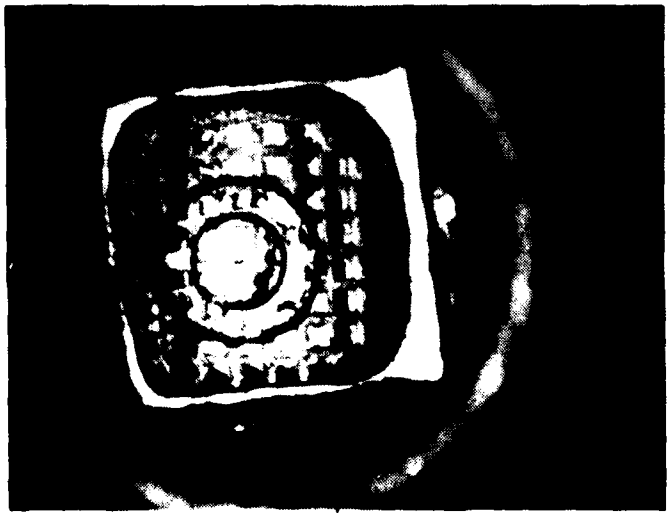
Only one failed silicon double-drift device was available from early failure region testing. Failure analysis for this device was carried out along with analysis of devices failing in the pulsed stress to failure testing, and both are discussed here.

Failure analysis of the Hewlett Packard devices was initially hampered by the fact that a passivating resin had been used and nearly filled the interior of the device (see Figure 3-8). The resin had a jelly like consistency, never completely hardening and contained a mirror image of the mesh used to make a top bond connection to the mesa.

It was discovered that the [illegible] could be removed using a commercial photo-resist stripper. Figure 3-9 presents two views of a silicon device following failure. Annular mesas were used here. Holes are seen in the top contact metallization and in the silicon substrate.



(a) MESH CONNECTING LEAD USED IN HEWLETT- PACKARD SILICON DOUBLE DRIFT DEVICES
50X



(b) TOP VIEW OF HEWLETT- PACKARD SILICON DOUBLE DRIFT DEVICE CONTAINING RESIN

FIGURE 3-8 TWO VIEWS OF A HEWLETT-PACKARD SILICON DOUBLE DRIFT DEVICE

D-20807

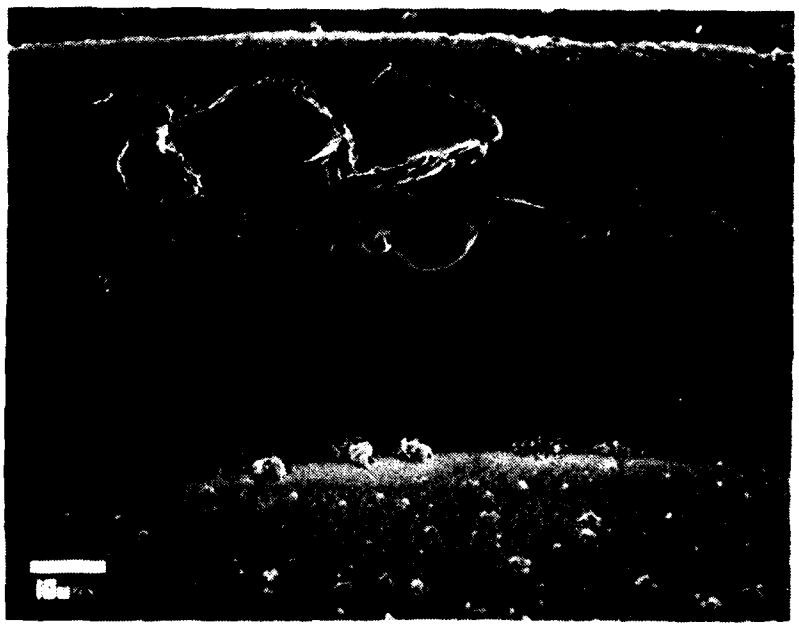


FIGURE 3-9 TWO VIEWS OF A SILICON DOUBLE DRIFT DEVICE FOLLOWING PULSED STRESS TO BURN-OUT TESTING

D-20800

TEST	V_o (VOLTS)	I_O (mA)	T (Base-Plate) (°C)	T_{CASE} (°C)	P_D W (Average)	T_J (°C)	TIME (HOURS)
DC Burn-IN	135	105	60	85	14.2	180	24
Pulsed DC Burn-In (25% Duty)	150	350	65	90	13.1	178	24

TABLE 3-III BURN-IN CONDITIONS USED FOR EARLY FAILURE REGION TESTING OF SILICON DOUBLE-DRIFT IMPATTS

TEST	NO. OF STARTS	NO. OF FAILURES	PERCENT FAILURES
DC Burn-In	10	0	0
Pulsed DC Burn-In	10	1	10
RF Test After DC Burn-In	10	0	0
RF Test After Pulsed DC Burn-In	9	0	0

TABLE 3-IV COMPARISON OF DC AND PULSED DC BURN-IN RESULTS FOR SILICON DOUBLE-DRIFT IMPATTs

Following gold stripping, a layer of metallization remained (see Figure 3-10). Edax analysis of a portion of this metal extending beyond the inner mesa radius on one device (see Figure 3-11) indicated the presence of platinum. Possibly a platinum silicide metallization system was used here. No titanium or chromium were detected, the plated heat sink was determinedto be silver with a platinum overlay.

Failure sites in the silicon devices were not as obvious as in the case of gallium arsenide. Large remelted damage areas were not seen on the mesa periphery, and since top internal failure locations were obscured.

Figure 3-12 shows the location of one failure site. Apparently, a silicon dendrite was formed along a conducting surface channel. In an attempt to locate failure sites, some units were cross-sectioned. Figure 3-13 presents three views of such a device. In view (a), the taper of the heat sink at the edge is seen. View (b), and (c) show each side of the ring mesa at greater magnification. A crack is shown in the left hand view. It is not known whether the crack was caused (or the cause of) failure or the crack was introduced during cross-sectioning. A stain has been applied to the cross-sectioned device, revealing the various epitaxial layers. The p+ to lower contact metallization area appears rough, as if the semi-conductor surface were not smooth or excessive sintering of the contact lead to irregular penetration of the metallization. This condition is partially due to the action of the stain etch. In any case, no direct evidence of burn-out was seen.

In conclusion, it appears that the silicon devices are not damaged to the degree that is seen in gallium arsenide devices when failure occurs. Edge burn-out of over-stressed units does appear to occur in the majority of case.

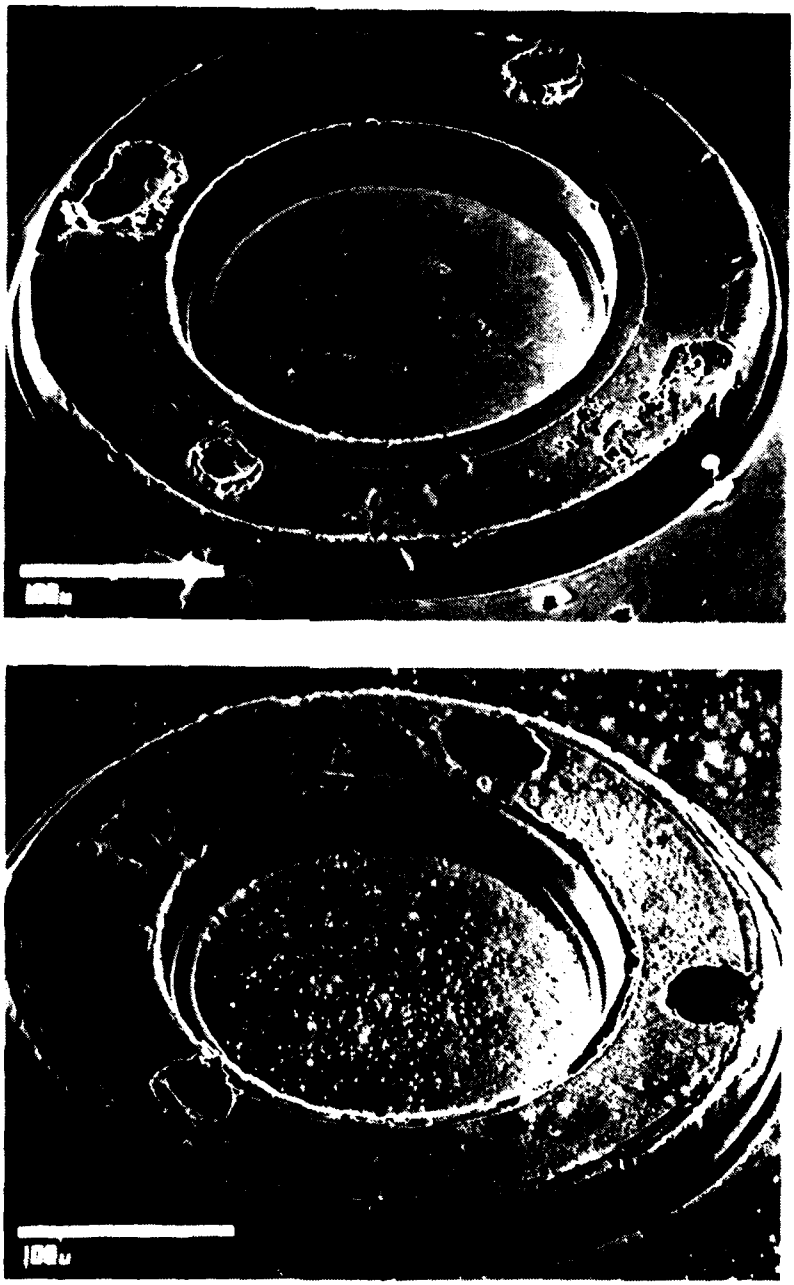


FIGURE 3-10 TWO SILICON DOUBLE DRIFT DEVICES FOLLOWING REMOVAL OF TOP GOLD METALLIZATION

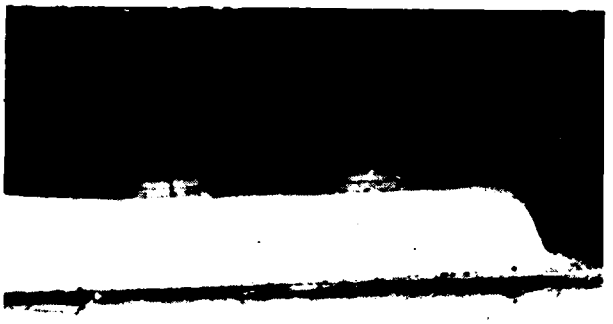
D-20801

FIGURE 3-11 PROTRUDING METALLIZATION IN A SILICON DOUBLE DRIFT DEVICE ANALYZED USING EDAX TO BE PLATINUM

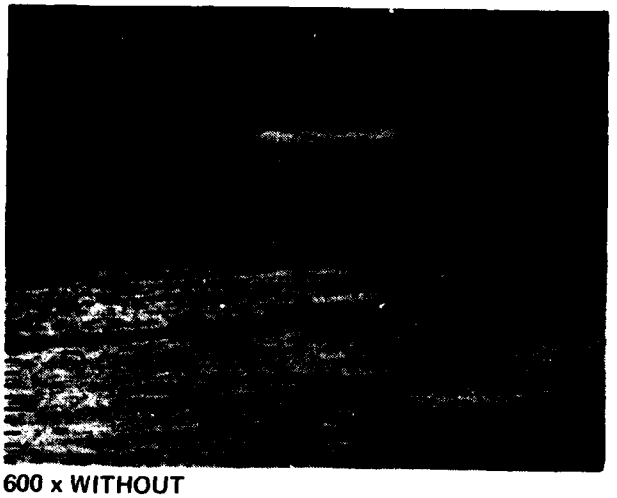
D-20775

FIGURE 3-12 FAILURE SITE LOCATION IN A SILICON DOUBLE DRIFT IMPATT THAT FAILED DURING PULSED STRESS TO FAILURE TESTING

D-20786



(a) 50X



(b) 600 x WITHOUT STAIN ETCH

(c) 1000 x WITH STAIN ETCH

FIGURE 3-13 THREE VIEWS OF A CROSS-SECTIONED SILICON DOUBLE DRIFT DEVICE FOLLOWING FAILURE ON PULSED dc BURN-IN

3.2.3 EARLY FAILURE REGION TESTING OF DOUBLE-DRIFT GALLIUM ARSENIDE DEVICES

Gallium arsenide double-drift devices produced in the assembly area were subjected to the burn-in tests without any pre-screening.

3.2.3.1 Flat Profile Double-Drift Devices

A batch of ten (10) flat-profile double-drift gallium arsenide diodes were subjected to similar DC and pulsed DC burn-in tests. These diodes, from wafer number 21118 were capable of 12 to 19 watts peak at 10% duty, with 11% efficiency. Five (5) diodes were put on the DC burn-in at an average power of 15.6 watts and a case temperature of 100°C, for seven (7) days. One diode failed the test. A pulse width of 1 μsec 10% duty cycle was chosen for non-oscillating pulse burn-in. As in the DC burn-in, an average power of 16.5 watts was applied for seven (7) days with a case temperature of 100°C. There were no failures on this test. Again, there was no statistically significant difference in the failure rate between the two types of burn-in. All the DC parameters (V_B, V_F, C_T at zero bias, C_T at 0.8 V_B, I_L, tuning ratios) were measured before and after the burn-in tests. None of the parameters changed, except for the forward voltage, V_F. Forward voltages were lowered due to the sintering of the back contacts during tests. At the time, these devices were fabricated, palladium, nickel, gold reactive back contacts were in use.

3.2.3.2 Hybrid Double-Drift X-Band Devices

DC and pulsed DC burn-in testing of hybrid double-drift devices from wafer 21487-1A was carried out. Fifty (50) devices were completely RF and DC tested and placed on DC burn-in for 168 hours. Burn-in was carried out at 105°C diode case temperature and 16.5 watts of DC input power, placing the junction at 220° to 225°C. Two devices failed during DC burn-in, 1 additional device failed during subsequent RF testing. No change in breakdown voltage, capacitance, or operating voltage at fixed current was seen. However, output power was generally 0.3 dB lower and operating frequency 500 MHz higher after burn-in.

Circuit conditions were thought to be identified, although the exact position of sliding tuning elements in the tuner section could not be verified. Since 1 MHz capacitance readings for the diodes had not changed, the change in performance seen was probably due to the circuit tuning not being identical.

Pulsed DC burn-in for the devices was performed at 230°C junction temperature. Twenty-nine (29) devices were operated for 168 hours at 25% duty, 1 microsecond pulse width. Each device dissipated approximately 16.5 watts (77 volts and 0.860 A peak), and was maintained at a case temperature of 105°C, as had been done for the DC burn-in. Of the twenty-nine devices, nine (9) failed for a failure percentage of 31%, compared to 6% for non-pulsed DC burn-in at the same junction temperature.

Devices surviving pulsed DC burn-in were RF tested and found to have 0.3 dB lower output power and 500 MHz higher operating frequency as was the case for devices surviving non-pulsed DC burn-in. Again, the change was believed to be due to cavity tuning.

Pulsed RF burn-in was carried out using 10 of the hybrid double-drift devices from wafer 21487-1. The equipment previously described was used.

These devices were operated at 20 watts average input with 1.75 watts average output at 90°C case temperature. A one microsecond 25% duty waveform was maintained. With an average thermal resistance of 7.0°C/watt, the junctions would have been approximately 220°C.

One device failed and was replaced after two days. Subsequently, three (3) additional devices failed for a failure ratio of 36.3%. This percentage is comparable to that seen in pulsed non-oscillating burn-in (31%), but much higher than seen in DC burn-in (6%) at the same average junction temperature for hybrid double-drift devices.

A summary of early failure region testing for hybrid double-drift devices appears in Tables 3-V and 3-VI. When considered in comparison to single-drift gallium arsenide and flat-profile silicon double-drift devices, an unusually large number of failures occurred in pulsed DC burn-in. In fact, for these hybrid devices, pulsed DC burn-in could be substituted for RF burn-in, since failure percentages were nearly equal. A possible explanation for this behavior would involve device bias circuit oscillation during pulsed DC burn-in. This was not detected using a 20 MHz oscilloscope during the test, however. In recommending an appropriate burn-in for double-drift gallium arsenide devices, RF burn-in would still be chosen because the pulsed DC burn-in results are not completely understood.

3.2.3.2 Failure Analysis of Hybrid Double-Drift Devices Failing in Early Failure Region Testing

Devices failing in early failure region tests exhibited edge burn-out in almost all cases, as was seen with single-drift gallium arsenide devices (see Figure 3-14). Cracked mesas also were found as shown in Figure 3-15. Evidence of excess top bonding pressure was also seen (see Figure 3-16). In general, it appeared that no new failure mechanism was active in the hybrid double drift devices that had not been identified in single-drift units.

In summary, the early failure mechanisms in high power pulsed IMPATT diodes can be attributed largely to the manufacturing defects either in processing or in assembly. These defects may be:

(I) chip damage at the top bond (ribbon connection) due to the use of excessive pressure

(II) chip damage in handling

(III) cracked chip due to excessive pressure during the die bonding operation

BURN-IN TEST	V_o (Volts)	I_o (mA)	$T_{base\ plate}$ (°C)	T_{case} (°C)	P_D (W)	T_J (°C)	TIME (Hours)
DC	69	240	85	105	16.5	221	168
PULSED DC (1 μsec, 25%)	77 (Peak)	860 (Peak)	85	105	16.5	221	168
PULSED RF (1 μsec, 25%)	80 (Peak)	1000 (Peak)	65	85	18.25	213	168

P_{out} = 1.75 W

TABLE 3-V BURN-IN CONDITIONS USED FOR EARLY FAILURE REGION TESTING OF HYBRID DOUBLE-DRIFT GALLIUM ARSENIDE DEVICES

TEST	NUMBER OF STARTS	NUMBER OF FAILURES	PERCENT FAILURES
DC Burn-In	50	2	4
Pulsed DC Burn-In	29	9	31
Pulsed RF Burn-In	11	4	36
RF Test after DC Burn-In	48	1	2

TABLE 3-VI COMPARISON OF RESULTS OF EARLY FAILURE REGION SCREENING METHODS FOR HYBRID DOUBLE-DRIFT DEVICES

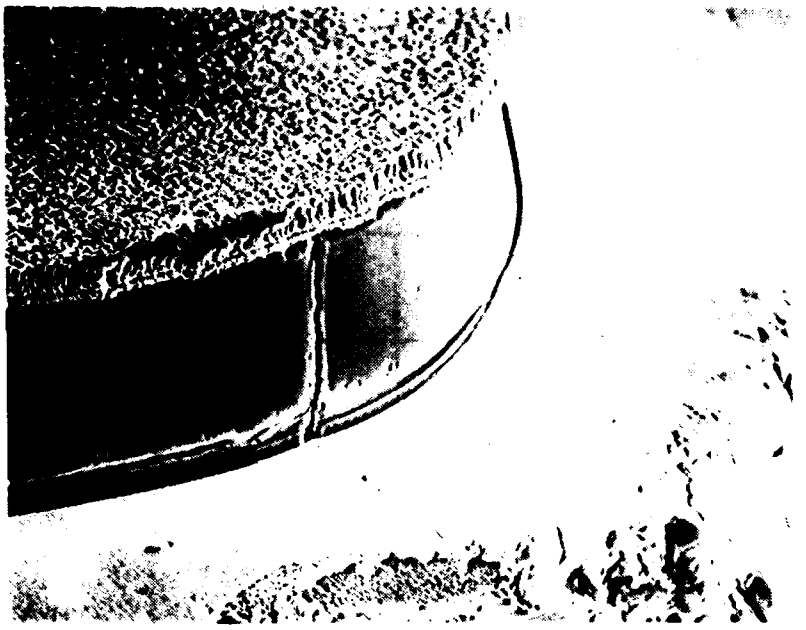


FIGURE 3-14 HYBRID DOUBLE DRIFT DEVICE THAT FAILED DURING PULSED RF BURN-IN DUE TO A CRACKED MESA

D-20787

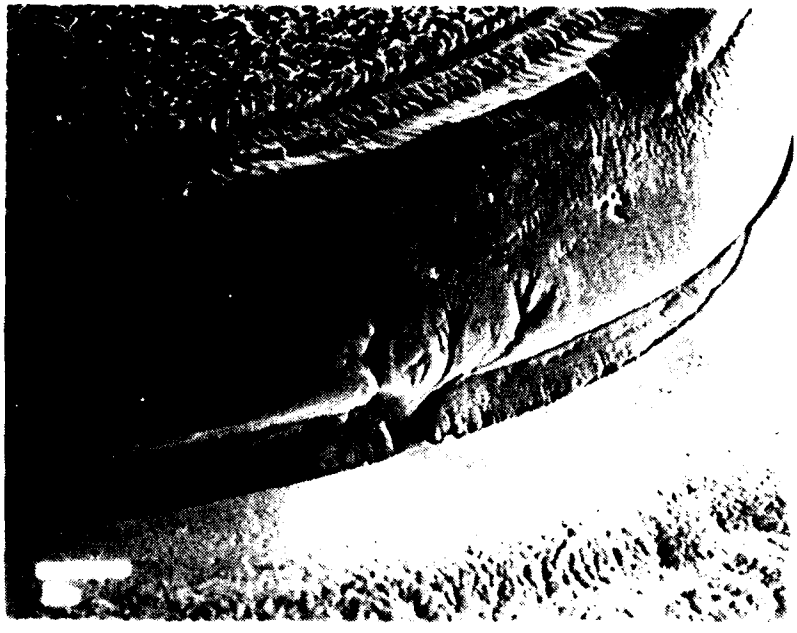


FIGURE 3-15 HYBRID DOUBLE DRIFT DEVICE THAT FAILED DURING INITIAL PULSED RF BURN-IN

D-20788

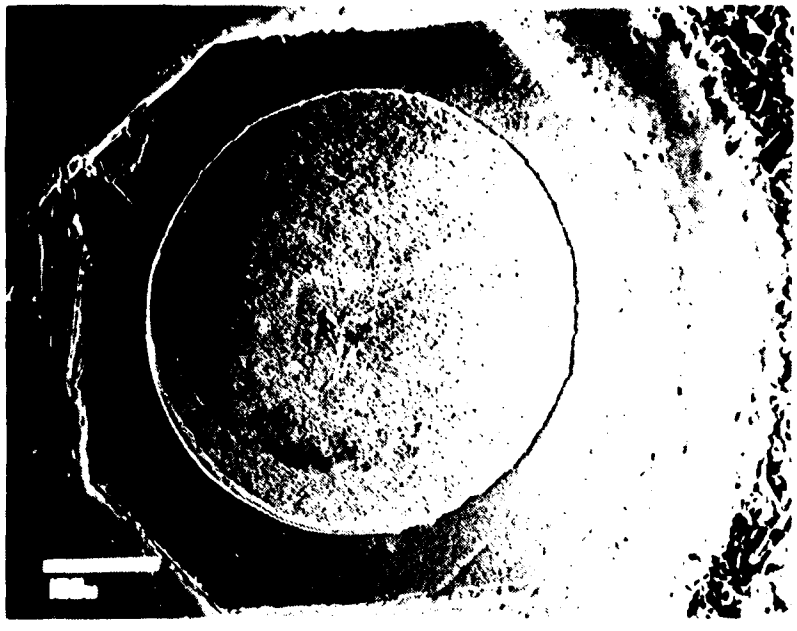


FIGURE 3-16 HYBRID DOUBLE DRIFT DEVICE EXHIBITING DAMAGE FROM EXCESSIVE TOP BONDING PRESSURE

D-20789

(IV) uneven solder flow under the plated heat sink resulting in higher thermal resistance

(V) non uniform in package [illegible] to either forming of a bubble or uneven [illegible] of etch. This kind of defect would lead to [illegible] uniform electric field near the surface and an edge burn-out.

(VI) surface contamination of the junction area either during processing or assembly leading to edge failures.

4.0 LONG-TERM PULSED RF BURN-IN TESTS

4.1 Introduction

Two 1000 hour pulsed RF burn-in tests were conducted, one using hybrid double-drift gallium arsenide X-band devices, the other H-L/L-H-L double-drift gallium arsenide X-band devices. These tests were intended to investigate long-term failure or degradation mechanisms in these devices, and to estimate the mean-time-to-failure for such a lot of units under maximum use stress conditions. The results of such tests allow recommendation of conservative maximum use stress conditions.

In long-term tests, it is desirable to use a population of prescreened devices that hopefully will not exhibit early failures. Analysis of long-term failure test data must include a check for the existance of early failures within the lot. For this reason, all devices used in 1000 hour tests had passed 168 hour DC, or pulsed DC burn-in.

4.2 Hybrid Double-Drift Gallium Arsenide Device Testing

Devices from wafer 21487-1 were tested at 20 watts average input with 1.75 watts average output, one microsecond, 25% duty operation, and 90°C case temperature. With an average thermal resistance of 7.0°C/W, a 220°C junction temperature was maintained. In total, 40 devices were tested because 10 devices failing after less than 100 hours were replaced with fresh devices. Failure analysis of diodes from this test revealed a condition where a surface breakdown and subsequent vaporization of the gallium arsenide had occurred. Determination of the exact cause of failure under these conditions is difficult (see Figure 4-1).

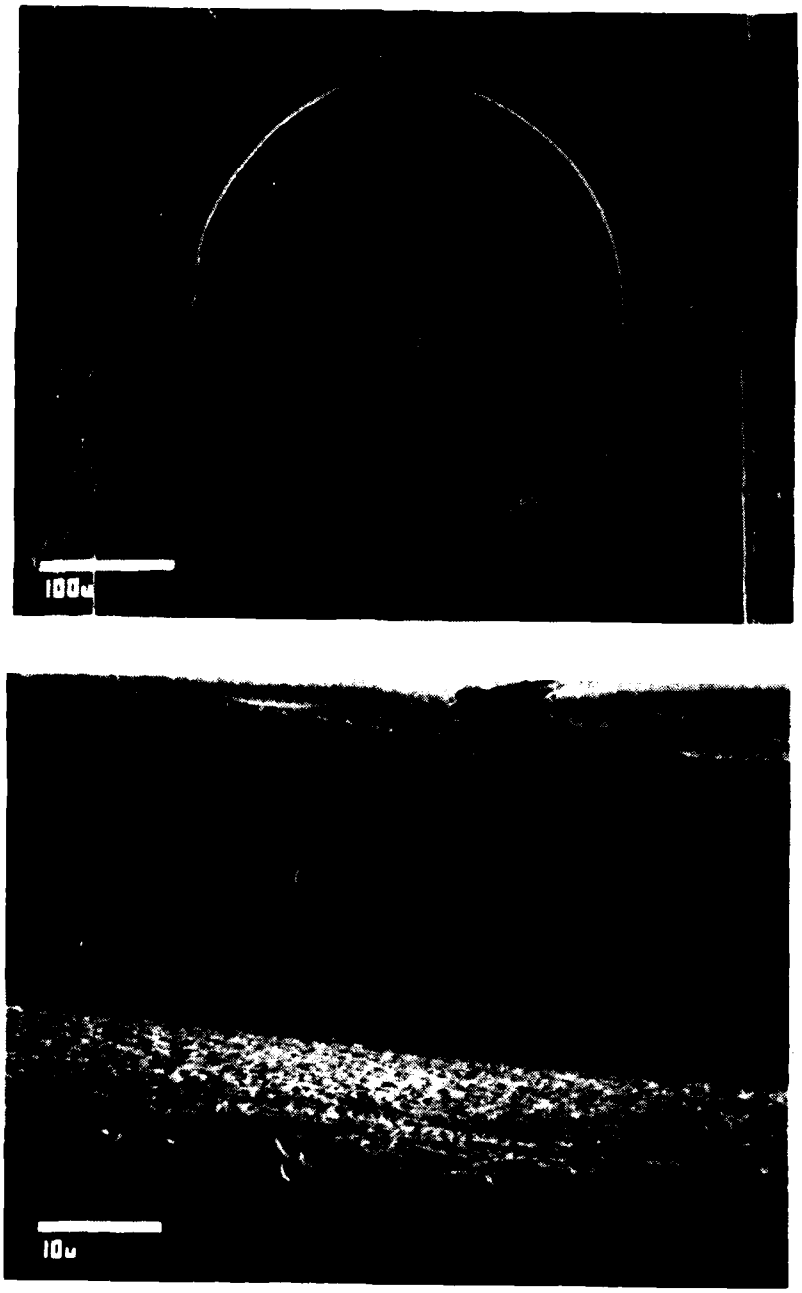


FIGURE 4-1 TWO VIEWS OF A HYBRID DOUBLE DRIFT DEVICE FAILING DURING PULSED RF BURN-IN AFTER 723 HOURS OF OPERATION AT 220°C JUNCTION

D-20802

A plot of time to failure versus cumulative failures, %, (probability scale) has been constructed for the 1000 hour RF burn-in test and appears in Figure 3-17. The points obtained can be fit by a straight line, indicating a log normal distribution in time to failure.

Because of the small standard deviation (steep slope) seen in Figure 4-2, it was suspected that the data might contain early failure units. Figure 4-3 presents number of failures versus hours of operation data for this test. Two distinct regions of different slope (failure rate) are seen. When the units corresponding to the higher slope region are removed and the data replotted on probability paper, Figure 4-4 results. As shown, two failure mechanisms are now indications, but the longer term mechanism still indicates a small standard deviation and predicts a mean-time-to-failure (MTTF) of 2600 hours at 220°C. Figure 4-2 predicted a 1600 hour MTTF.

A closer examination of failed units indicates a problem with potential device shorts from pieces of the top contact metallization (see Figure 4-5). This mechanism probably accounts for the shorter term failures seen. In the next RF burn-in test, this condition was corrected during device processing.

DC and RF testing of devices surviving the 1000 hour pulsed RF burn-in test indicated that no change in parameters had occurred. Table 4-I compares data taken before and after the 1000 hour test.

The seven devices surviving 1000 hour pulsed RF burn-in test were put back on RF burn-in test again to see the long-term failure rates. These seven devices have accumulated over 3000 hours so far without even a single failure. This indicates that once the early failure mechanisms are eliminated, there are no more failures and our initial prediction of MTTF of 2600 hours is on the low side.

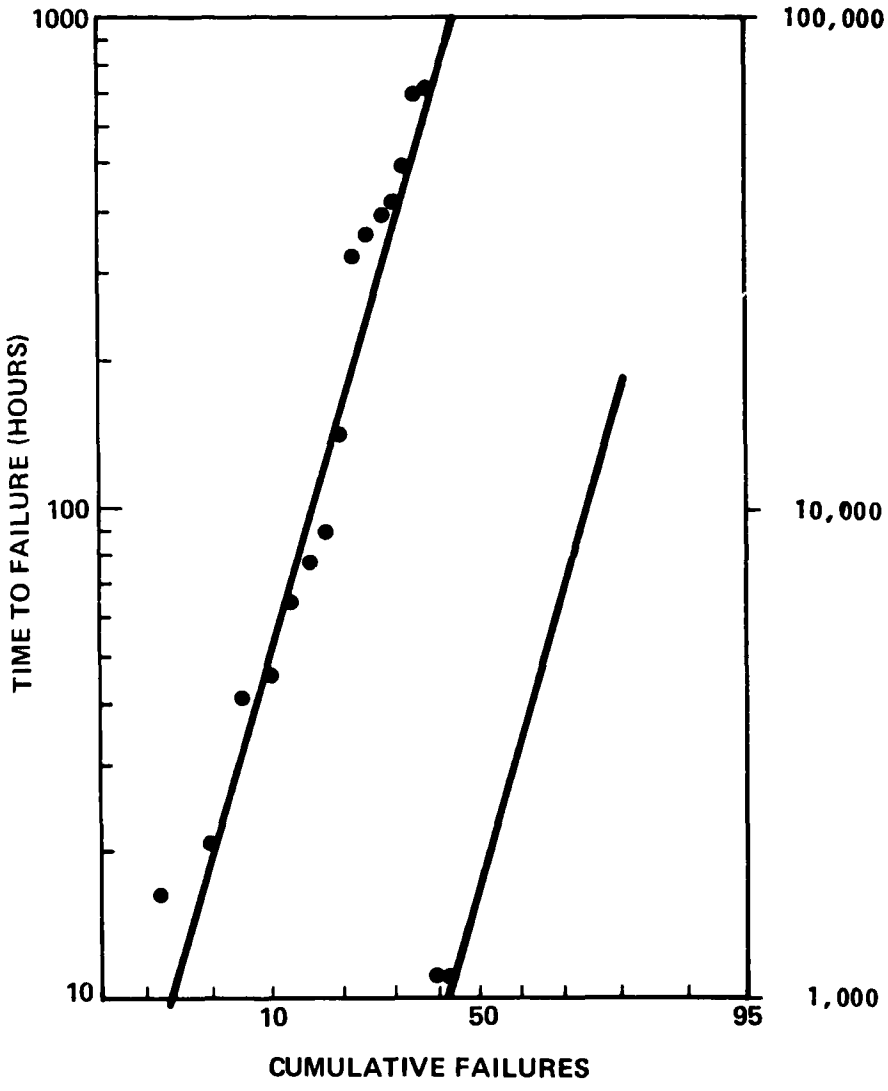


FIGURE 4-2 TIME TO FAILURE vs. CUMULATIVE FAILURES (%) – 1000 HOUR RF PULSED BURN-IN FOR WAFER 21487-1

D-20824

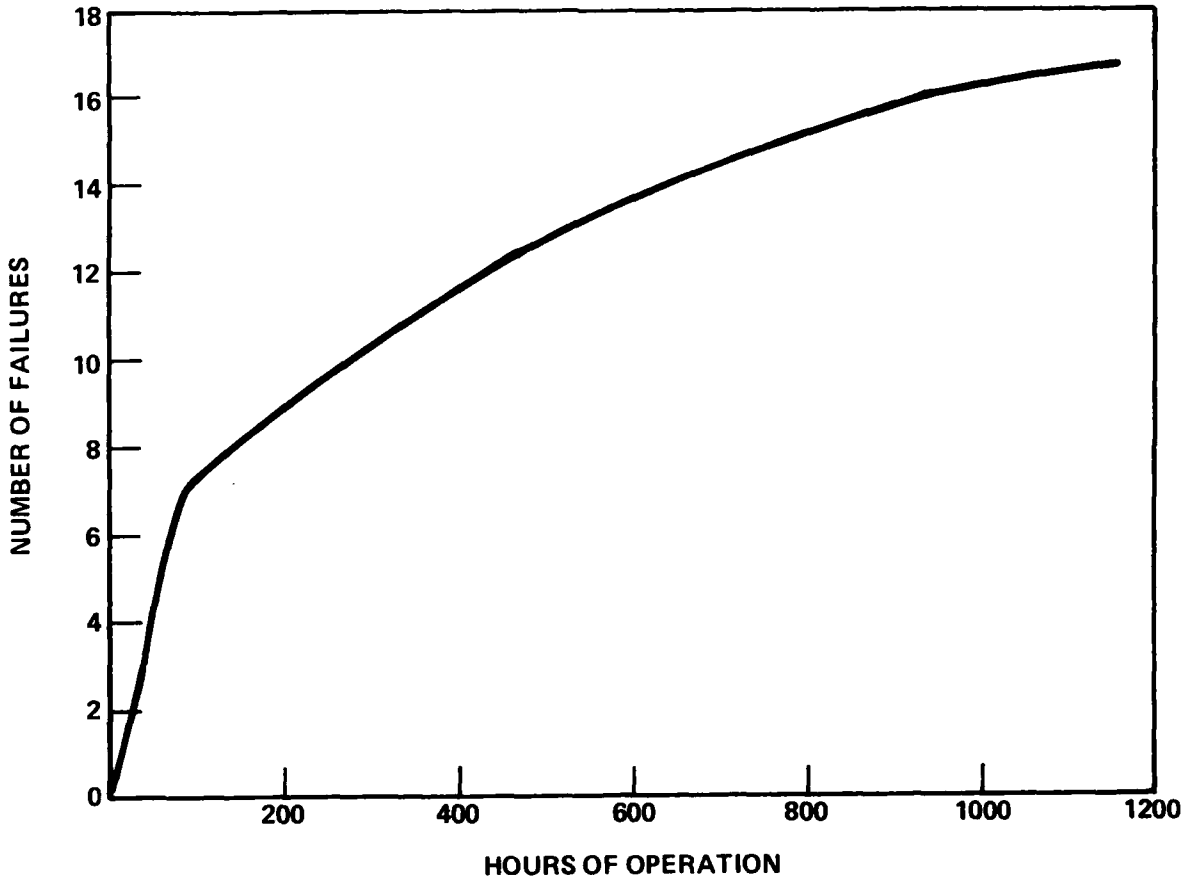


FIGURE 4-3 NUMBER OF FAILURES vs. HOURS OF OPERATION FOR 1000 HR LIFE TEST OF HYBRID DOUBLE DRIFT X-BAND DEVICES

D-20823

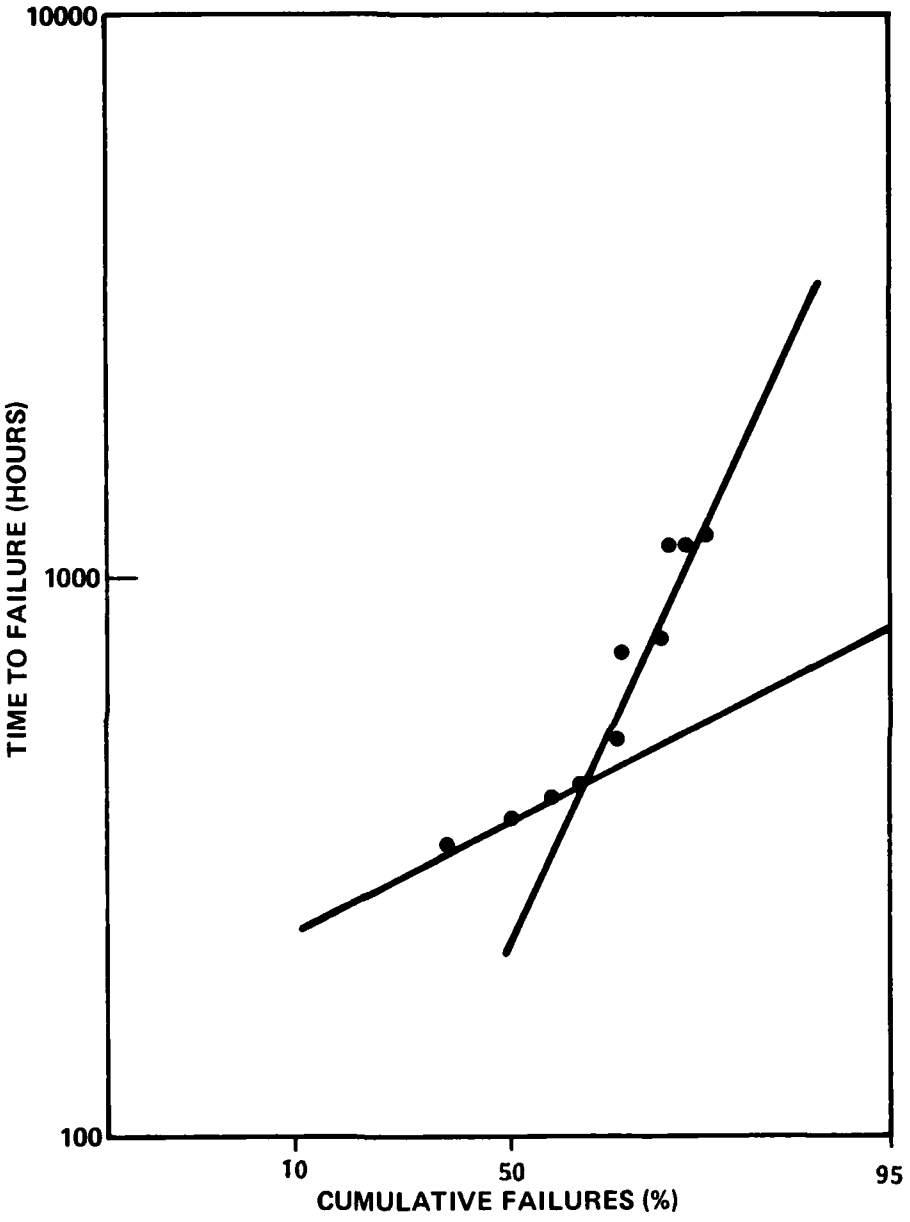


FIGURE 4-4 TIME TO FAILURE vs. CUMULATIVE FAILURES, % FOR 1000 HOUR PULSED RF BURN-IN OF HYBRID DOUBLE DRIFT DEVICES

D-20822

FIGURE 4-5 A HYBRID DOUBLE DRIFT DEVICE THAT FAILED AFTER 67 HOURS OF PULSED RF BURN-IN

D-20790

DIODES ⟶			1	2	3	4	5
V_{op}	Initial	Volts, Peak	84	85	87	86	83
V_{op}	Final	Volts, Peak	83	84	86	86	82
I_{op}	Initial	Amps, Peak	1.3	1.3	1.3	1.3	1.3
I_{op}	Final	Amps, Peak	1.3	1.3	1.3	1.3	1.3
P_o	Initial	Watts, Average	3.3	3.7	3.6	3.4	2.9
P_o	Final	Watts, Average	3.6	3.78	3.7	3.9	3.36
f_o	Initial	GHz	10.012	10.048	9.970	9.911	9.958
f_o	Final	GHz	9.969	10.015	9.973	9.881	9.933
V_B	Initial	Volts (1 mA)	52	52	52	52	52
V_B	Final	Volts (1 mA)	52	52	52	52	52
C_{T0}	Initial	pF	14.5	14.3	14.5	14.5	14.4
C_{T0}	Final	pF	13.6	13.4	13.5	13.6	13.5

Operation at 1.0 microsecond, 25% Duty

TABLE 4-I COMPARISON OF OPERATING PARAMETERS OF DEVICES SURVIVING 1000 HOUR PULSED RF BURN-IN, WAFER NUMBER 21487, HYBRID DOUBLE-DRIFT

4.3 H-L/L-H-L Device 1000 Hour RF Burn-In

Devices from lot number 21693 were used for this test. The device performance capability is as follows:

P_o	=	20 W, Peak
f_o	=	9.94 GHz
V_o	=	126 Volts
I_o	=	1.5 A
Pulse Width	=	1 microsecond
Duty Cycle	=	30%

Initially, the devices were operated at 235°C junction temperature. Operating parameters were as follows:

V_o	=	84 V, Peak
I_o	=	0.8 A
P_o	=	1.25 W, Average
T_{case}	=	85°C
Average Thermal Resistance	=	8°C/W
Pulse Width	=	1.0 microsecond
Duty Cycle	=	30%

After 240 hours of operation at 235°C junction temperature, only one of the twenty-four (24) devices on test had failed. At this point, the diode operating current and case temperature were increased providing a higher stress level. This was necessary in order to obtain a significant number of failures in the time remaining. Operating current was

increased from 0.8 to 0.9 amp, peak and case temperature from 85 to 90°C, placing the junction at approximately 266°C. The new operating parameters were:

V_o = 87 Volts, Peak

I_o = 0.9 Amp, Peak

P_o = 1.5 W, Average

T_{case} = 90°C

As failures occurred, fresh devices were placed in operation. Only devices that accumulated 1000 hours of operation or failed in test have been used in data analysis. Devices with less than 24 hours operation at failure were removed as early failures.

Results of the 1000 hour RF burn-in of Read double-drift devices appears in Figures 4-6 and 4-7. For this test, the failure rate (Figure 4-6) did not indicate the presence of early failures in the lot. Time-to-failure versus cumulative failures may be approximated by a straight line (Figure 4-7) with a predicted MTTF of 2000 hours at 266°C junction temperature.

RF and DC testing of surviving devices again indicated no change in parameters had occurred (see Table 4-2).

4.3.1 Failure Analysis of Read DD Devices Failing on 1000 Hour Pulsed RF Burn-In

Although edge failures were found (see Figure 4-8), more devices, upon initial examination, contained internal failure sites, obvious only when top metallization was removed, or in cross-section. Figure 4-9 and Figure 4-10 present such a case. Here, an internal failure site beneath the top contact metallization is shown.

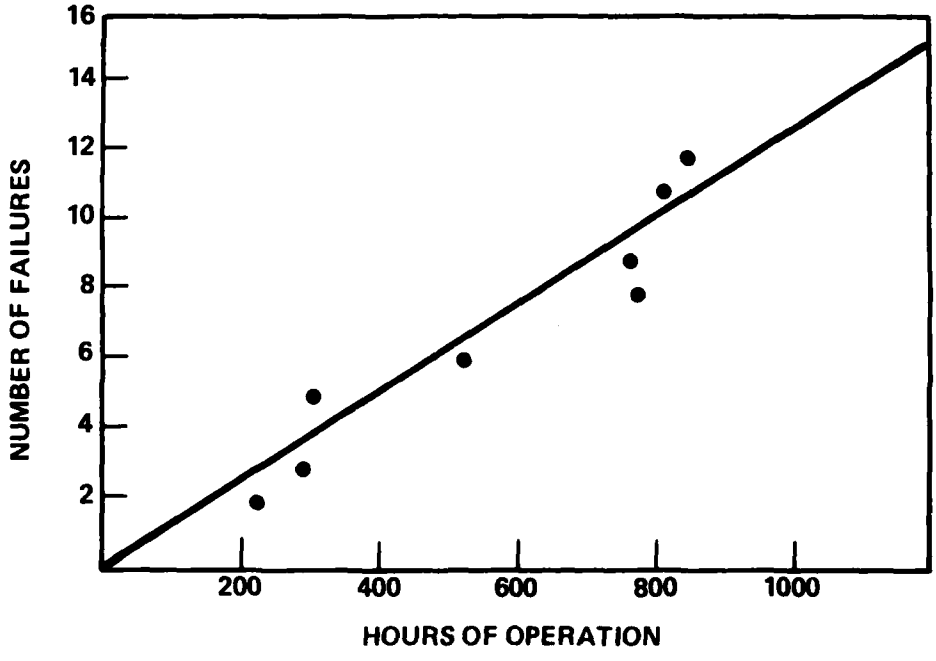


FIGURE 4-6 NUMBER OF FAILURES vs. HOURS OF OPERATION FOR 1000 HOUR LIFE TEST OF HL-LHL DOUBLE DRIFT X-BAND IMPATT's

D-20820

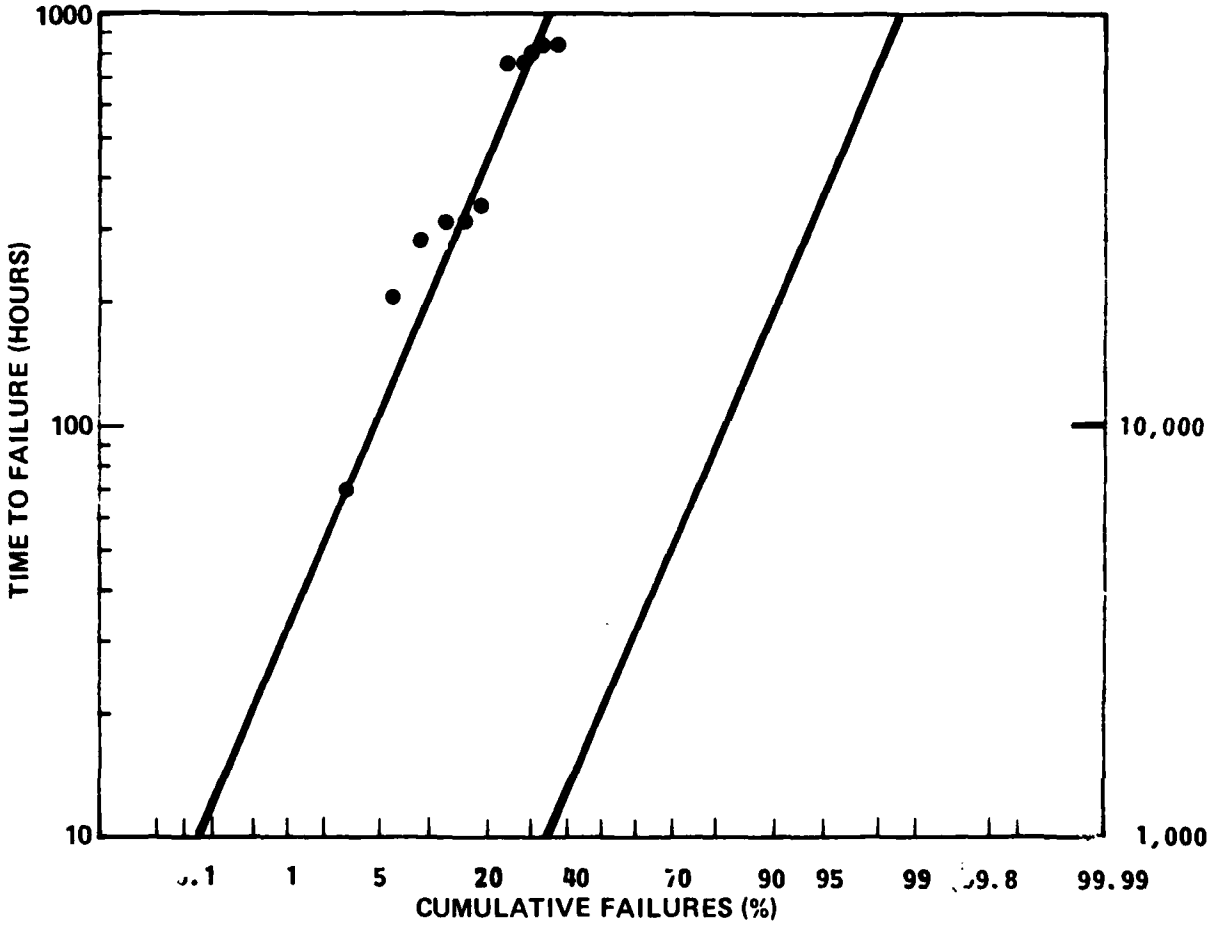


FIGURE 4-7 TIME TO FAILURE vs. CUMULATIVE FAILURES (%) FOR 1000 HOUR PULSED RF BURN-IN TEST OF HL-LHL DEVICES

D-20821

DIODES ⟶			1	2	3
V_{op}	Initial	Volts, Peak	98	98	93
V_{op}	Final	Volts, Peak	102	101	102
I_{op}	Initial	Amps, Peak	1.3	1.3	1.1
I_{op}	Final	Amps, Peak	1.3	1.3	1.3
P_o	Initial	Watts, Average	4.2	4.1	3.8
P_o	Final	Watts, Average	4.5	4.3	4.3
f_o	Initial	GHz	9.444	9.447	9.448
f_o	Final	GHz	9.533	9.435	9.444
V_B	Initial	Volts (1 mA)	62	64	62
V_B	Final	Volts (1 mA)	62	64	62
C_{T0}	Initial	pF	38.7	40.5	39.7
C_{T0}	Final	pF	36.4	38.0	37.2

Operating at 1.0 microsecond, 30% Duty

TABLE 4-II COMPARISON OF OPERATING PARAMETERS OF DEVICES SURVIVING 1000 HOUR PULSED RF BURN-IN, WAFER NUMBER 21693, READ DOUBLE-DRIFT

FIGURE 4-8 TWO VIEWS OF A LH-LHL DOUBLE DRIFT DEVICE FOLLOWING FAILURE AFTER 809 HOURS OF PULSED RF BURN-IN AT 265°C JUNCTION TEMPERATURE

D-20803

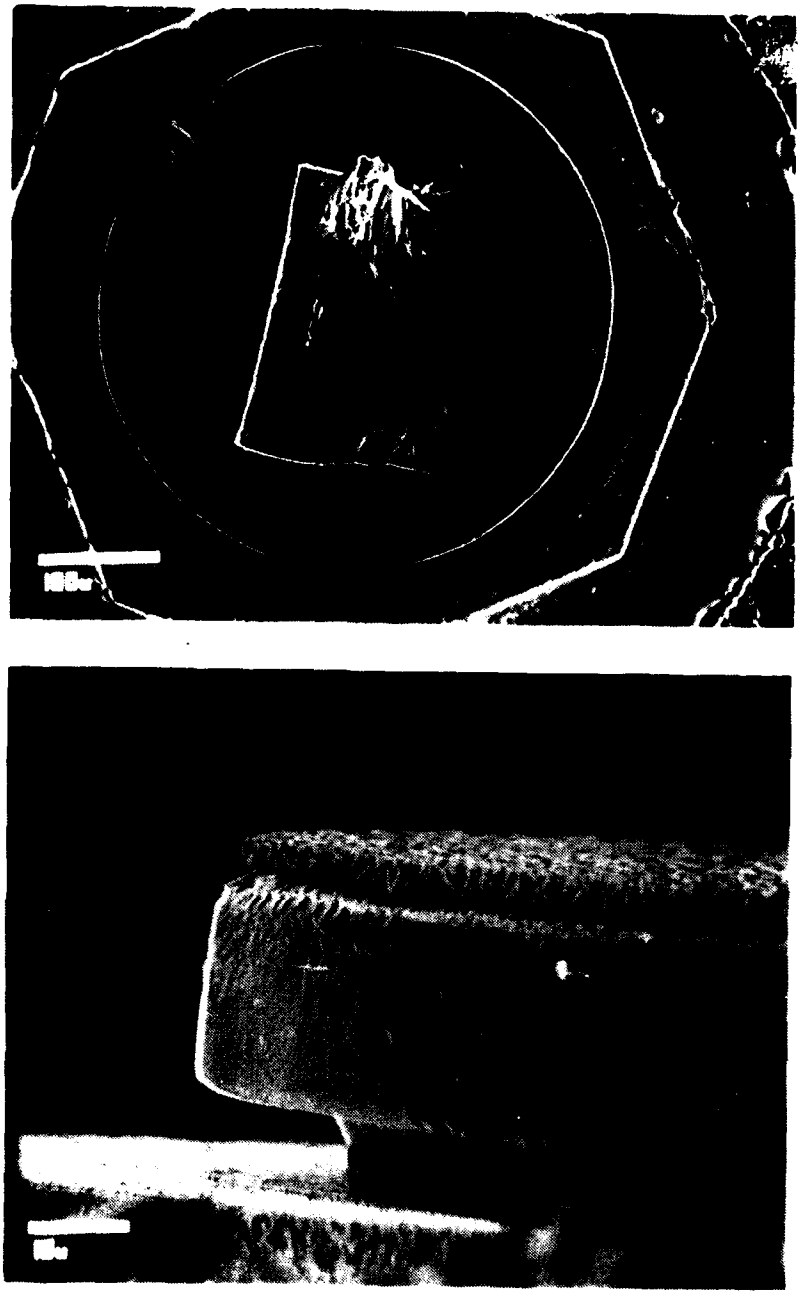


FIGURE 4-9 A HL-LHL GaAs DEVICE FOLLOWING FAILURE AFTER 764 HOURS OF PULSED RF BURN-IN AT 265° C JUNCTION TEMPERATURE. (THE MARK AT THE UPPER LEFT OF THE LOWER VIEW IS A DEFECT CAUSED BY POOR PHOTORESIST DEVELOPMENT)

D-20804

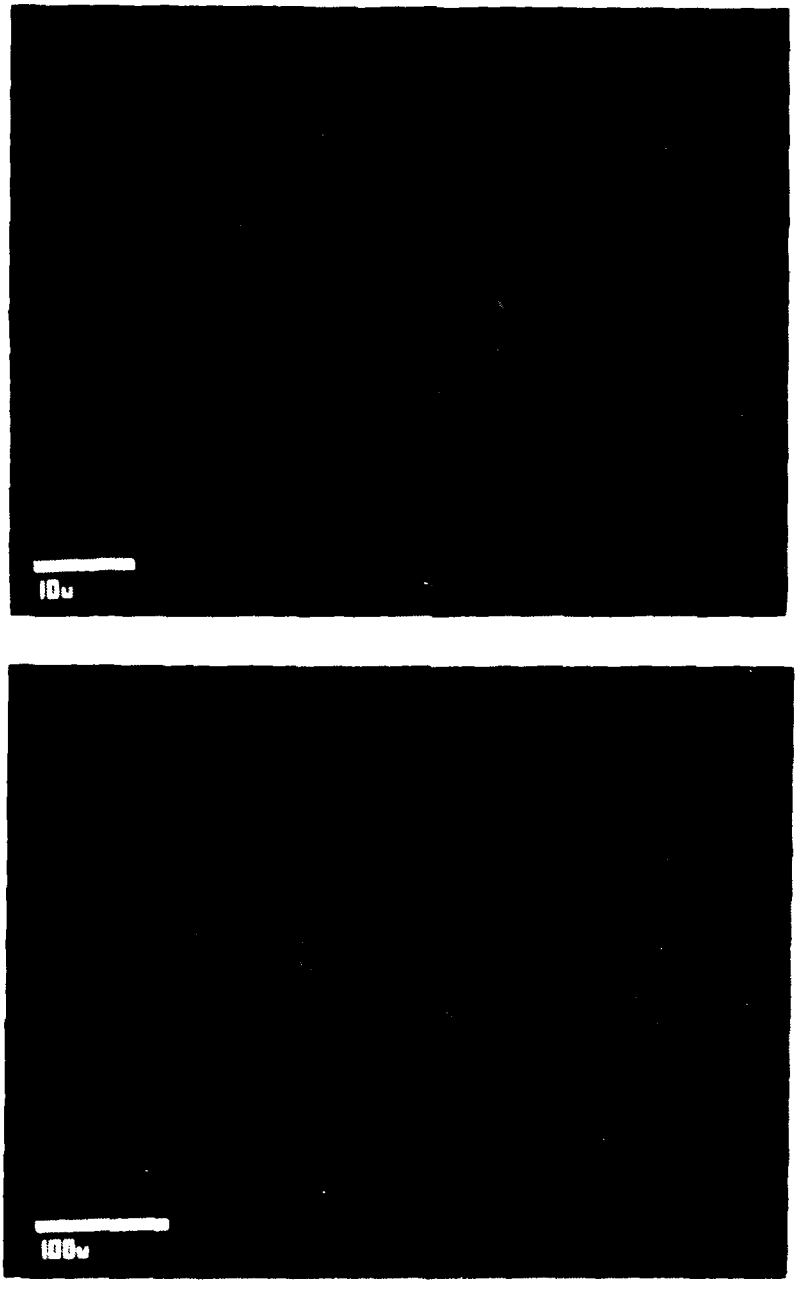


FIGURE 4-10 DIODE FROM THE PREVIOUS FIGURE FOLLOWING REMOVAL OF THE TCP CONTACT METALLIZATION

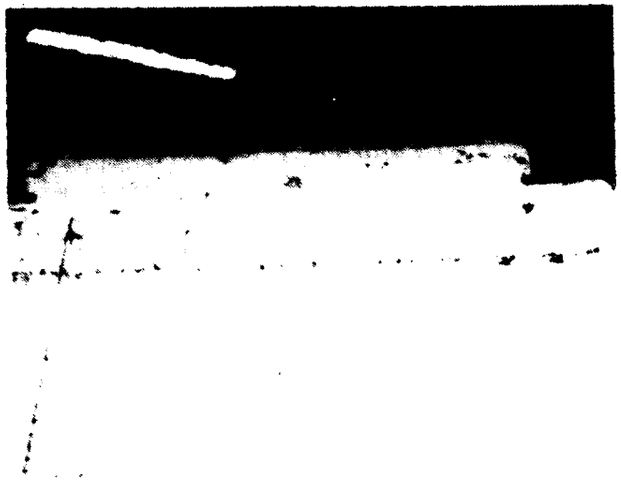
D-20805

Figure 4-11 shows a cross-sectioned device with an internal failure site. The cause of such failures can be attributed to hot spot formation at defect within the epitaxy. No sign of metal migration or contact metallization motion were seen.

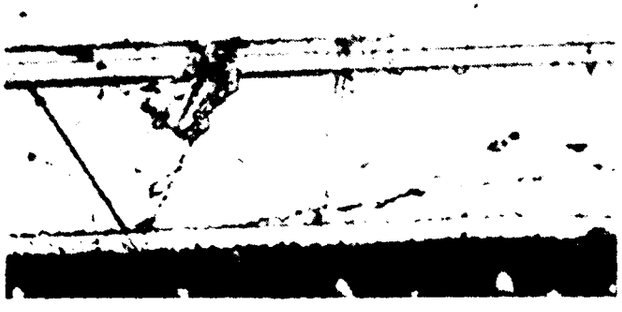
4.4 Conclusions

The pulsed RF burn-in testing has not been definitive in identification of long-term failure mechanisms. It is possible that those failures seen were not of the long-term or wear-out type in that no evidence of parameter drift in surviving units was seen. Rather, then failures could represent random freak failures accountable for MTBF control. That this is likely in the H-L/L-H-L device test follows from the constant failure rate seen. In this case, when interpreted as MTBF data the results of this test indicate an MTBF of 2000 hours at 265°C junction temperature.

Additional long-term tests (perhaps 10,000 hours) would be required to produce detectable long-term failures.



(a) 200X



(b) 600X

FIGURE 4-11 TWO VIEWS OF A CROSS-SECTIONED HL-LHL IMPATT FOLLOWING FAILURE AFTER 768 HOURS OF PULSED RF BURN-IN AT 265°C JUNCTION TEMPERATURE

D-20809

5.0 HIGH TEMPERATURE STEP STRESS TESTS

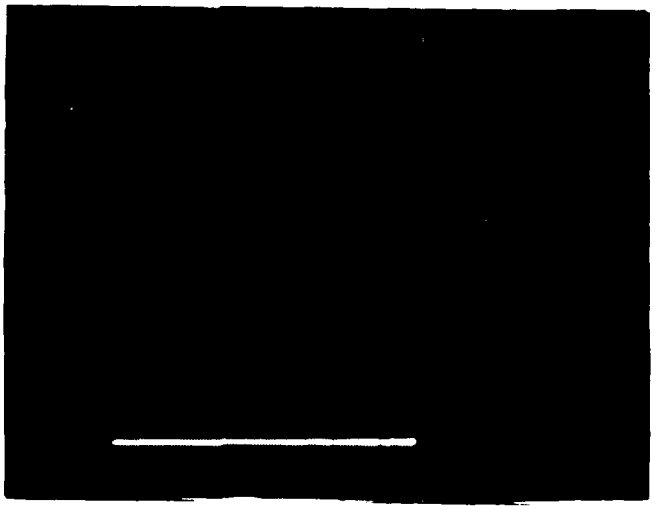
5.1 Introduction

In order to accelerate long-term failure mechanisms allowing analysis in a reasonable time, a high temperature storage step stress test was chosen. It was hoped that increased storage temperature would accelerate operation of those failure mechanisms responsible for wear-out failure. Such acceleration is commonly used in semiconductor testing.

5.2 Test Description and Results

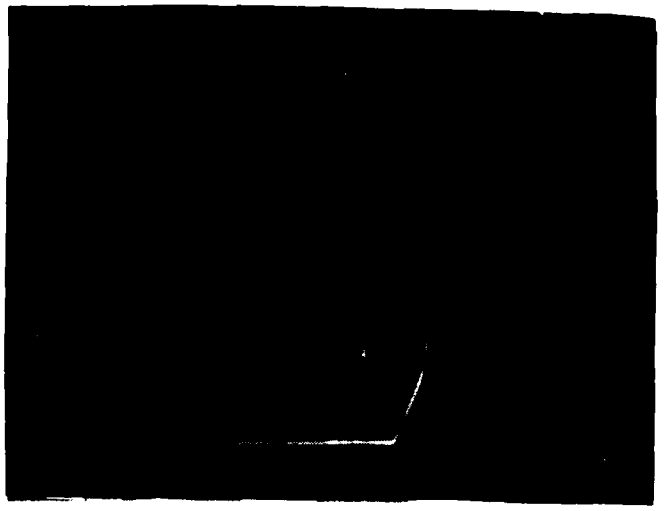
Devices from three different wafers were involved: two gallium arsenide hybrid double-drift devices (21613 and 21359) and one Read double-drift wafer (21693). A 168 hour stress period and stress temperatures of 280, 295, 325 and 335°C were used. After each step, devices were tested for breakdown, forward voltage drop, capacitance (zero bias and 80% of breakdown), and leakage current at 80% of breakdown using automatic equipment. All devices had failed after the 335°C step. Generally, failure showed up as an increase in reverse leakage current at 80% of breakdown by two to three orders of magnitude. Initial leakage currents were in the range of 50 to 100 nanoamperes, while after baking, 20 to 50 microamperes of leakage current were seen. A curve tracer observation of the breakdown characteristic for these devices revealed a soft breakdown or in some cases, a ramping breakdown (see Figure 5-1).

In an attempt to determine the failure mechanism, some devices were opened and etched, removing possible surface contamination. Two etching solutions were used, a 3-1-1 mixture of sulfuric acid, hydrogen peroxide and water, and a 2-1-2 mixture of



(B)

10 V x 0.2 mA/ DIVISION
INITIAL BREAKDOWN CURVE



(A)

10 V x 0.2 mA/DIVISION
FOLLOWING 168 HOURS AT 310°C

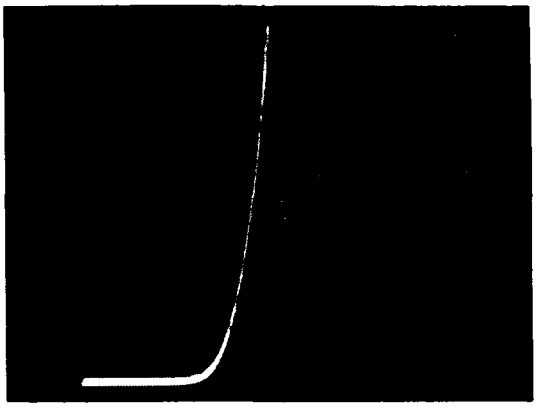
FIGURE 5-1 DEGRADATION IN BREAKDOWN CHARACTERISTIC DUE TO HIGH TEMPERATURE STORAGE STEP STRESS–WAFER 21359-1

D-20810

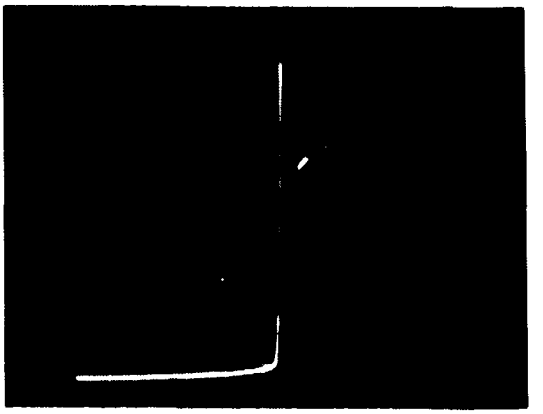
hydrofluoric acid, nitric acid, and phosphoric acid. Some improvement in leakage (about 25%) was obtained by etching, but the original levels could not be obtained nor could the ramping breakdown characteristic be corrected (see Figures 5-2, 5-3, 5-4 and 5-5).

RF re-testing was attempted on some of the devices failing the high temperature storage step stress. Both devices that had been opened for etching and sealed devices were tested. In both cases, no output power was obtained, and burn-out occurred at about 1.0 A peak current. Prior to step stress testing, all devices had been tested at 1.2 A peak. Thermal resistance was measured on a sample of these devices and had increased on the average by 2°C/W from 7.6°C/W to 9.7°C/W. This increase could be attributed to remelting of the solder preform used to attach the chip 80% gold, 20% tin). The initial melting temperature of this preform is 280°C. However, the remelt temperature is higher, probably above 325°C because of a composition change that occurs when some of the chip's plated gold heat sink is dissolved into the molten preform. This remelting could explain the thermal resistance increase seen, but would not explain changes in breakdown characteristics that could not be reversed with etching. Comparison of the solder appearance for a stressed device and non-stressed device appears in Figure 5-6; some change in appearance is shown.

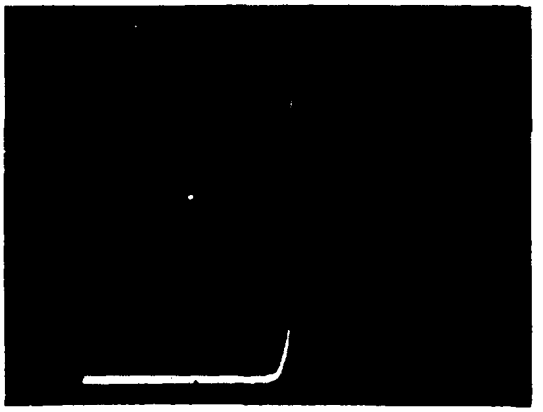
Reciprocal absolute failure temperature versus cumulative failures has been plotted for the storage temperature step stress test in Figure 5-7. All twenty-four (24) devices from the three wafers have been analyzed together in forming this curve. A good straight line fit was obtained, indicating a normal distribution in reciprocal absolute failure temperature exists. If preform melting were responsible for the failures seen, one would expect the last (highest temperature)



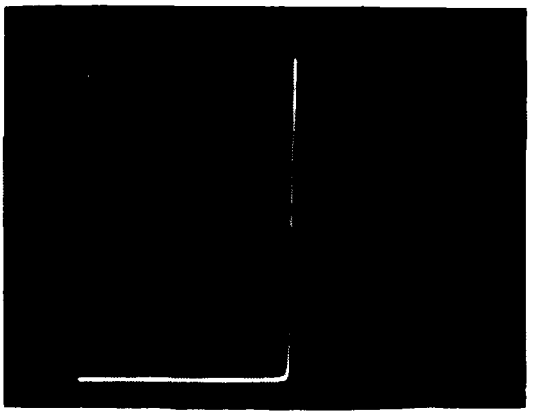
50 μA x 10 V/DIV.
INITIAL



1 mA x 10 V/DIV.
INITIAL



50 μA x 10 V/DIV.
FINAL



1 mA x 10 V/DIV.
FINAL

FIGURE 5-2 IMPROVEMENT IN BREAKDOWN CHARACTERISTIC FOLLOWING 10% AREA REDUCTION USING 311 ETCH.– DEVICE WAS SUBJECTED TO 168 HOURS AT 335°C. WAFER 21613-1A

D-20811

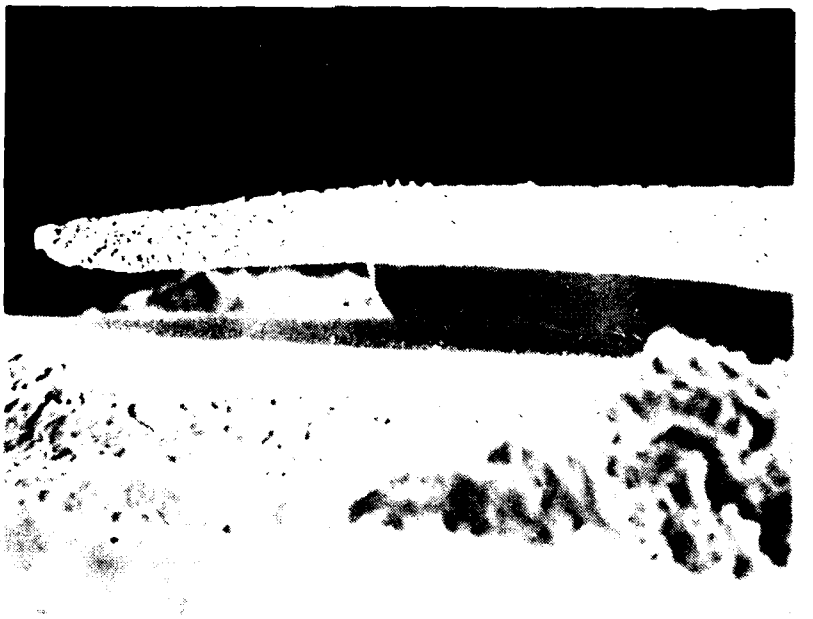
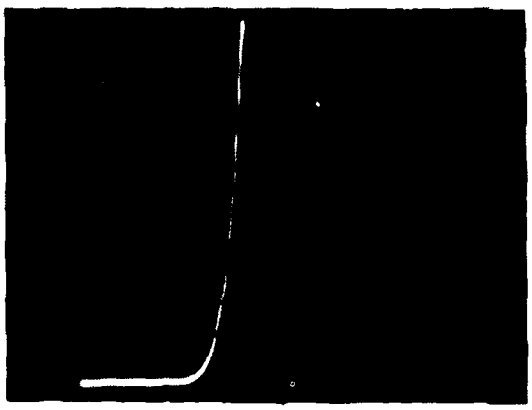


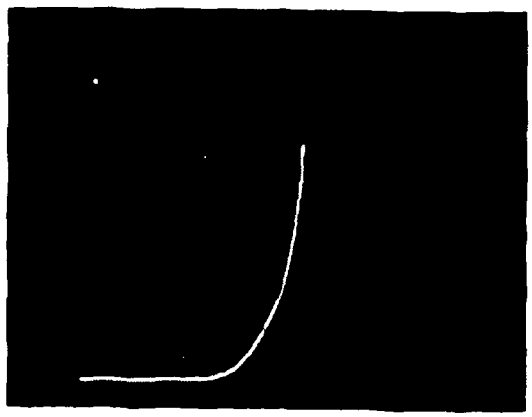
FIGURE 5-3 DEVICE OF PREVIOUS FIGURE FOLLOWING ETCH IN 311

D-20791

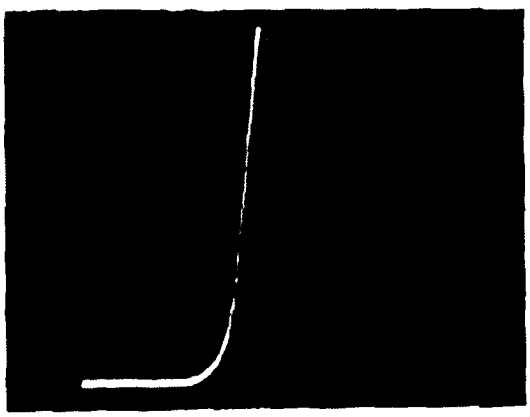
READ DOUBLE DRIFT
DIODE 21693-1A-6



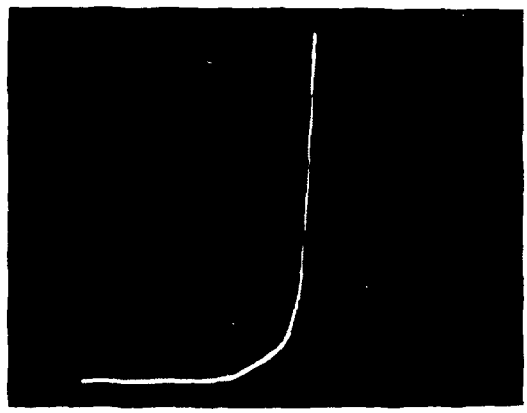
50 μA x 10 V/DIV.
INITIAL



1 mA x 10 V/DIV.
INITIAL



50 μA x 10 V/DIV.
FINAL



1 mA x 10 V/DIV.
FINAL

FIGURE 5.4 A COMPARISON OF BREAKDOWN CHARACTERISTIC BEFORE AND AFTER 10% AREA REDUCTION USING 2-1-2 ETCH—DEVICE SUBJECTED TO 168 HOURS AT 335°C

D-20812

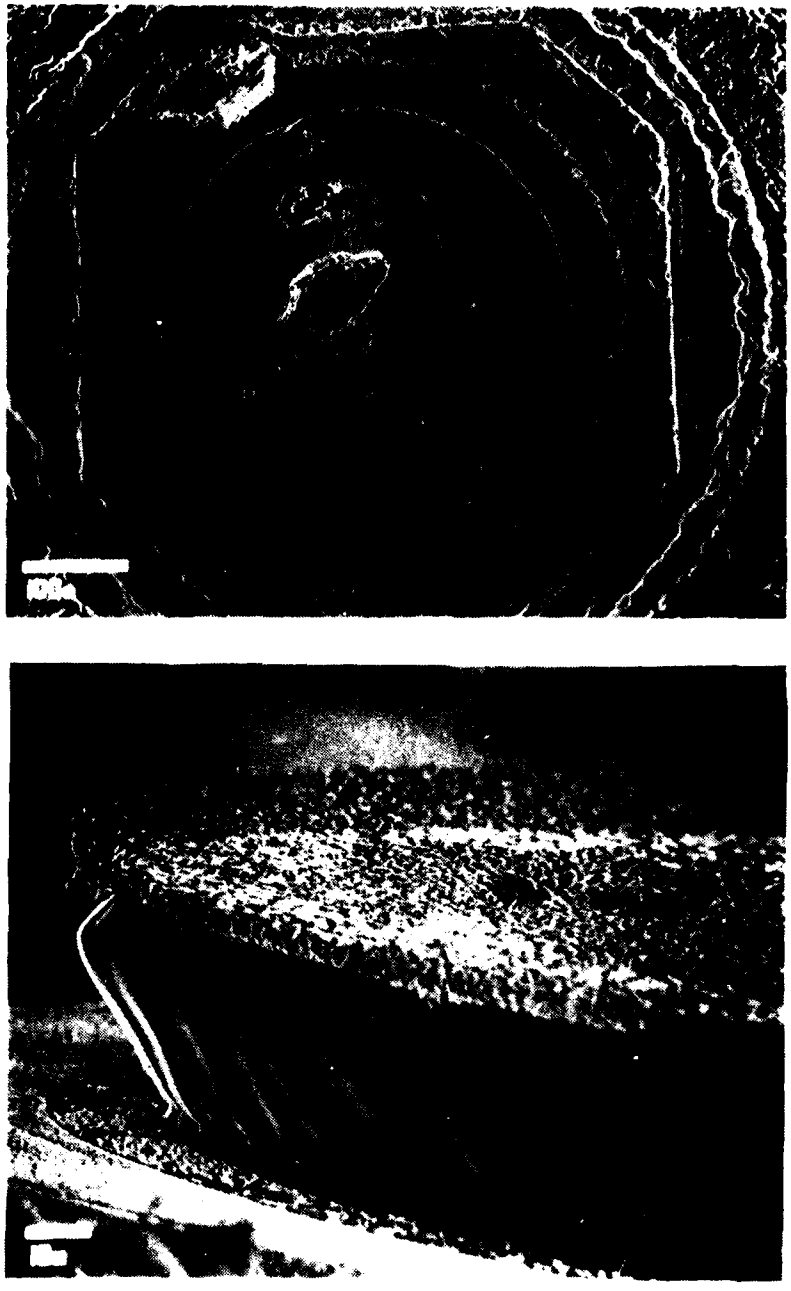
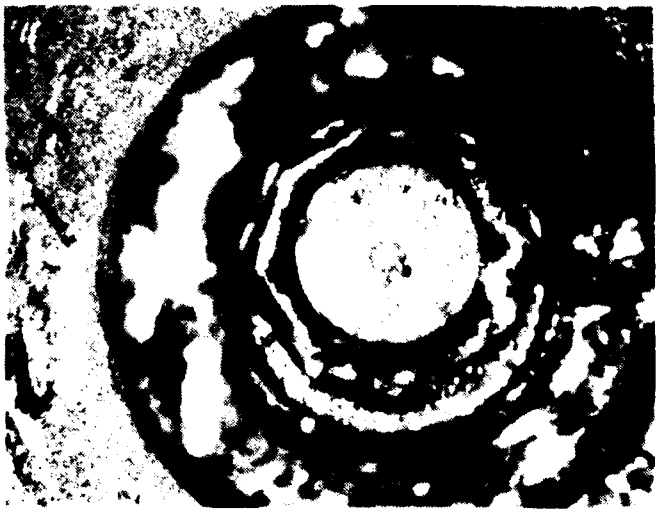


FIGURE 5-5 TWO VIEWS OF THE DEVICE FROM THE PREVIOUS FIGURE FOLLOWING ETCH

D-20813

(a) DEVICE 21359-1A-5
50X
FOLLOWING 168 HOURS
AT 310C



(b) DEVICE 21693-1A #47
NOT HEAT TREATED

FIGURE 5-6 A COMPARISON OF DEVICES SHOWING THE CHANGE IN SOLDER APPEARANCE FOLLOWING HEAT TREATMENT

D-20814

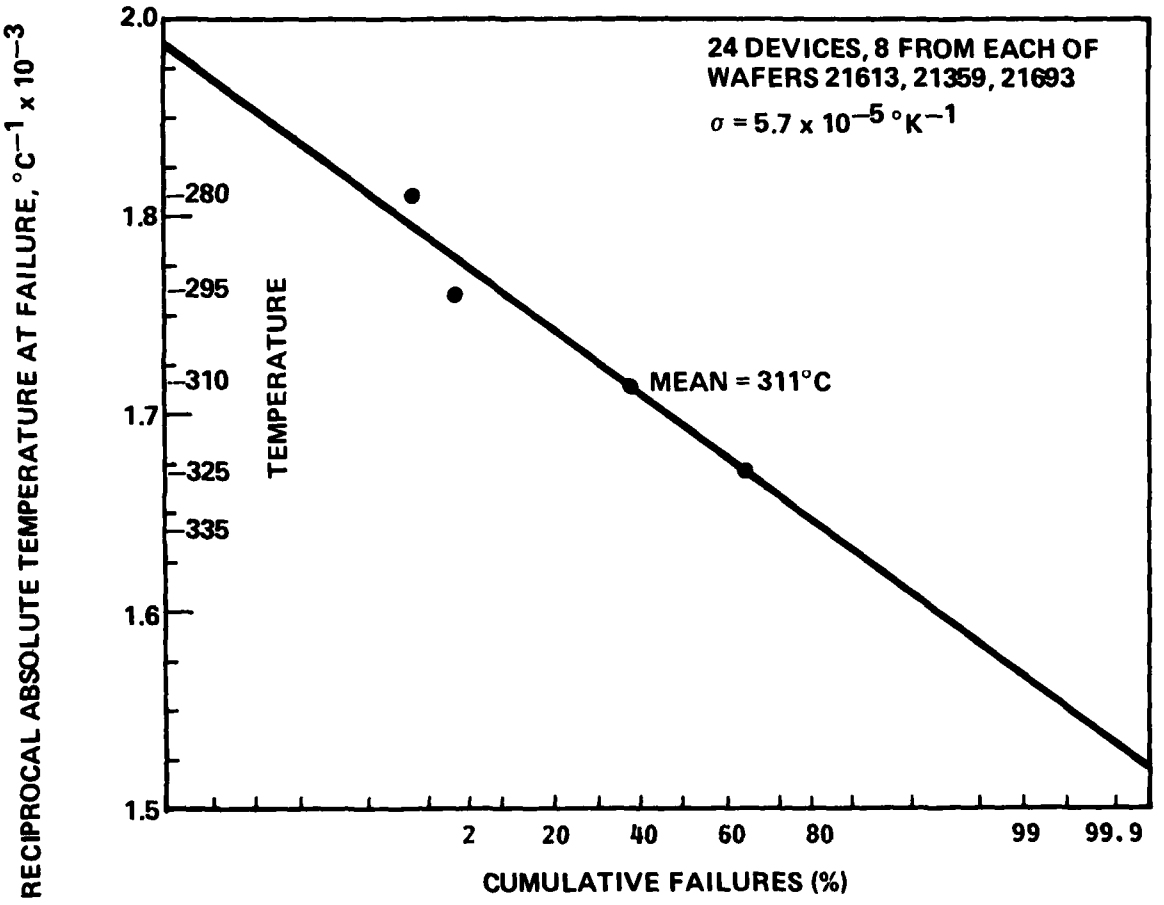


FIGURE 5-7 RECIPROCAL ABSOLUTE FAILURE TEMPERATURE vs. CUMULATIVE FAILURES, % FOR HIGH TEMPERATURE STORAGE TEST--168 HOUR PERIOD--*DOUBLE DRIFT GaAs* IMPATTS

D-20819

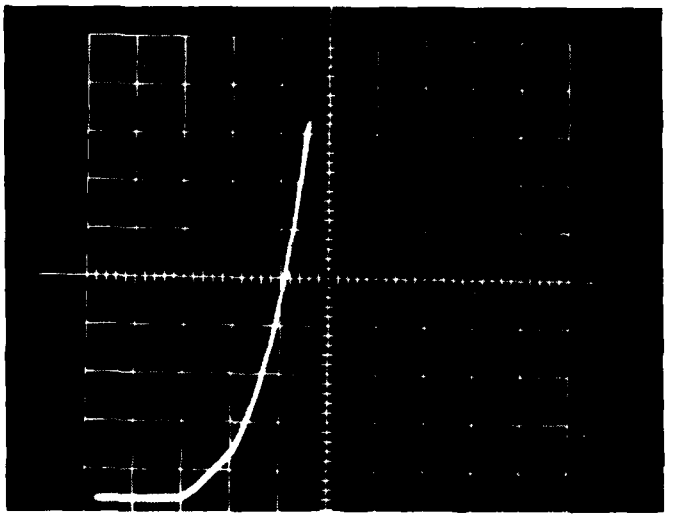
point not to lie on the straight line since two different failure mechanisms would then exist. Analyzing the hybrid and full Read devices together is justified because only one failure mechanism is present.

Because of the possibility that the previous test had been tainted by remelting of the gold - tin solder, the highest temperature step (335°C for 168 hours) was repeated using devices from wafer 21693 (Read double-drift) bonded with 365°C melting point gold germanium solder. Essentially, similar results occurred (see Figure 5-8 and Table 5-1). Here, electrolytic etching in 10% potassium hydroxide in water was used. This etch removes only the p+, p, and active n region leaving the substrate unetched (see Figure 5-9). Any question of the degradation has been eliminated by these tests.

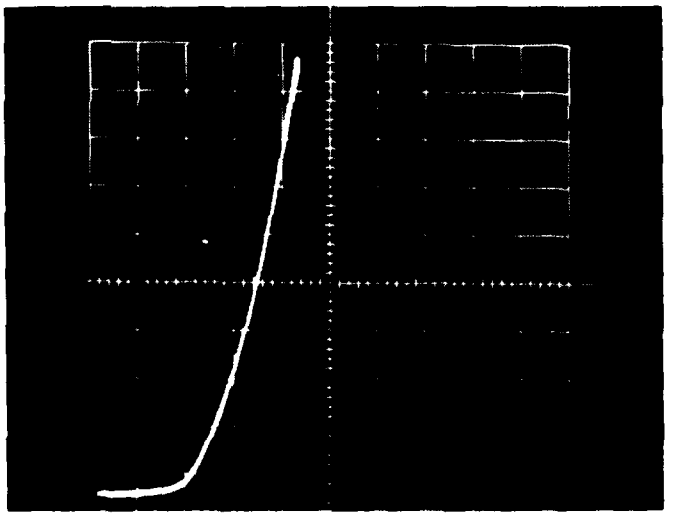
5.3 Failure Analysis

It was felt that contact metallization penetration into the active region could be responsible for the degradation seen, as had been the case in a previous Gunn diode reliability study (discussed in the introduction). Accordingly, several devices were cross-sectioned and examined for metal penetration. No evidence of realloying of the contact was seen (see Figure 5-10).

Examination of mesa side walls with the EDAX did not reveal any detectable contamination. In two cases, pieces of debris were seen in a position so as to short circuit the entire region (see Figures 5-11 and 5-12). Whether this was a coincidence or a cause of failure is not known. The mesas in these photographs reveal the effect of in-package etching in 311 during original assembly. In another case, a pile of debris was seen near the mesa side wall (see Figure 5-13). It was not possible to analyze these materials with the EDAX because of shielding effects caused by the proximity of the mesa.



(a) INITIAL



(b) FOLLOWING 20% CAPACITANCE REDUCTION WITH ETCHING USING POTASSIUM HYDROXIDE

SCALE: X-AXIS 5 VOLTS/Div

Y-AXIS .2 mA/Div

FIGURE 5-8 BREAKDOWN CHARACTERISTICS OF DEVICE 21693-1A (GOLD GERMANIUM BOND) FOLLOWING 168 HOURS AT 335° C

D-20815

WAFER	V_{B-1} (Volts, 10 μA)	V_{B-2} (Volts, 1 mA)	V_{F-1} (Volts, 10 μA)	V_{F-2} (Volts, 1 mA)	V_{F-3} (Volts, 100 mA)	V* (Volts)	C* (pF)	C_{T0} (pF, 0 Volts)	$C_{0.8}$ (pF, 0.8 V_B)	I_L (μA, 0.8 V_B)	T_R (0 V, 0.8 V_B)
2	58.65	63.40	-0.91	-1.05	-1.50	14.00	8.54	35.80	4.48	0.104	8.0
3	61.17	63.16	-0.90	-1.05	-1.49	14.00	8.51	35.65	4.45	0.124	8.0
4	60.64	62.72	-0.90	-1.04	-1.49	14.00	9.09	37.80	4.68	0.256	8.1
5	61.90	64.18	-0.90	-1.05	-1.49	14.00	8.63	35.12	4.36	0.221	8.1
7	58.70	61.75	-0.91	-1.05	-1.49	14.00	8.02	33.38	4.22	0.083	7.9
12	61.12	64.32	-0.91	-1.04	-1.49	14.00	8.77	35.85	4.44	0.256	8.1
14	60.74	62.92	-0.90	-1.05	-1.49	14.00	8.99	37.42	4.62	0.104	8.1
16	57.49	61.75	-0.89	-1.04	-1.48	14.00	9.08	37.97	4.78	0.307	7.9
FINAL DATA											
2	19.02	27.21	-0.82	-0.95	-1.40	14.00	8.61	34.64	6.66	27.962	5.2
3	16.50	27.11	-0.79	-0.93	-1.39	14.00	8.73	34.98	6.76	42.938	5.2
4	15.29	26.29	-0.87	-1.00	-1.43	14.00	8.50	35.57	6.87	49.178	5.2
5	7.49	16.30	-0.87	-0.99	-1.43	7.83	11.19	33.25	8.88	49.074	3.7
7	5.89	19.41	-0.44	-0.91	-1.41	13.11	9.23	34.21	8.48	71.851	4.0
12	4.19	18.15	-0.37	-0.70	-1.38	11.70	10.17	35.49	9.09	73.619	3.9
14	12.14	27.06	-0.86	-0.99	-1.44	7.08	13.18	37.29	7.20	70.031	5.2
16	8.79	20.91	-0.84	-0.97	-1.42	1370.2	9.35	27.86	8.65	61.867	4.4

TABLE 5-I A COMPARISON OF DC TEST DATA FOR READ DOUBLE-DRIFT WAFER 21693-1A, BEFORE AND AFTER 168 HOUR BAKE AT 335°C

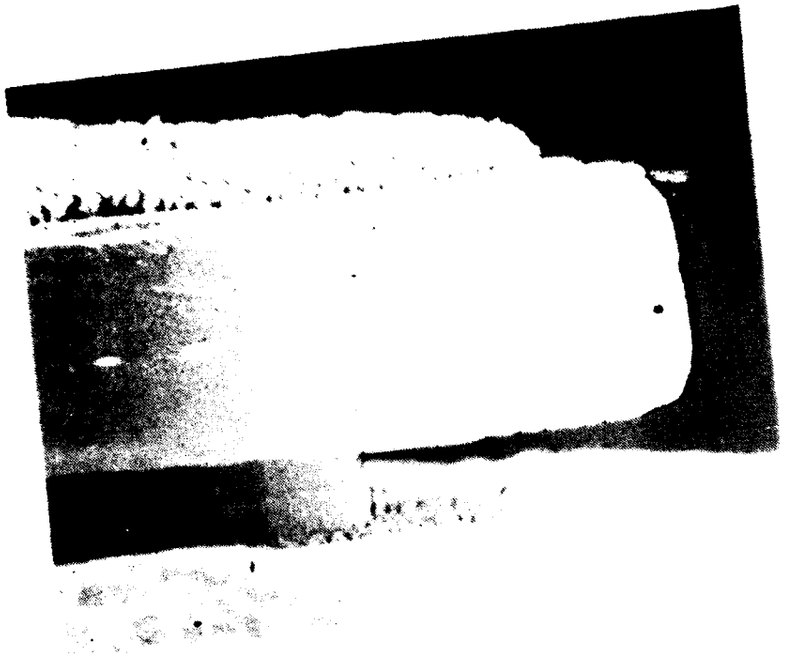
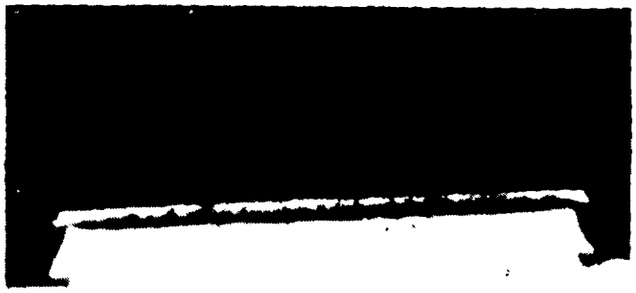


FIGURE 5-9 EFFECT OF POTASSIUM HYDROXIDE ETCH ON A DEVICE FROM WAFER 21693-1A

D-20792

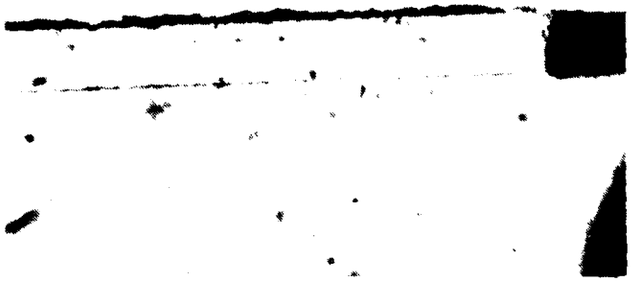


21359-1A #3

FAILED AFTER 168 HR.
310°C BAKE

SOFT

(a) 200X



(b) 1000X FOLLOWING STAIN ETCHING

FIGURE 5-10 TWO CROSS-SECTIONAL VIEWS OF A DEVICE FROM WAFER 21359 THAT EXHIBITED SOFT BREAKDOWN FOLLOWING 168 HOUR STORAGE AT 310°C

D-20816

FIGURE 5-11 READ DOUBLE DRIFT DEVICE FROM WAFER 21693-1 WITH GOLD GERMANIUM SOLDER FOLLOWING DEGRADATION DURING 168 HOUR BAKE AT 335°C

D-20793

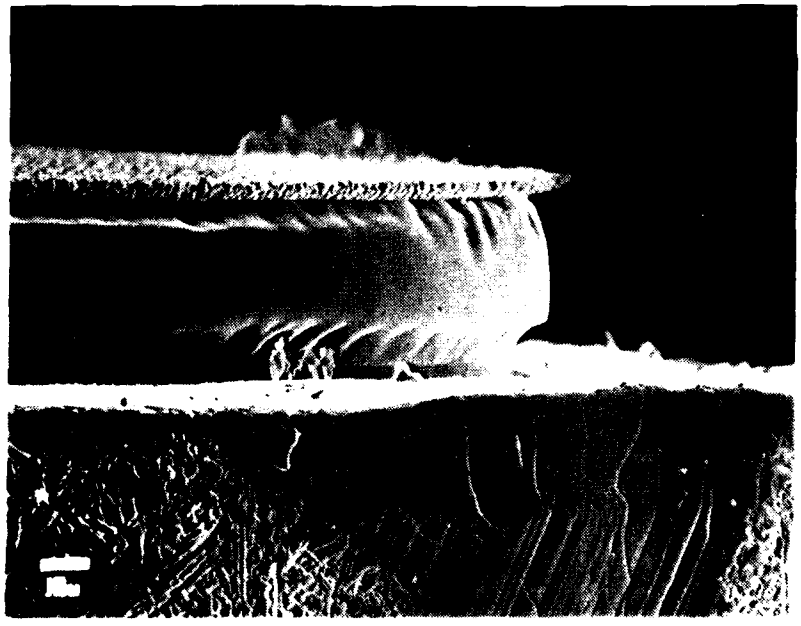


FIGURE 5-12 A SECOND EXAMPLE OF A READ DOUBLE DRIFT DEVICE FOLLOWING 168 HOUR BAKE AT 335°C.

D-20795

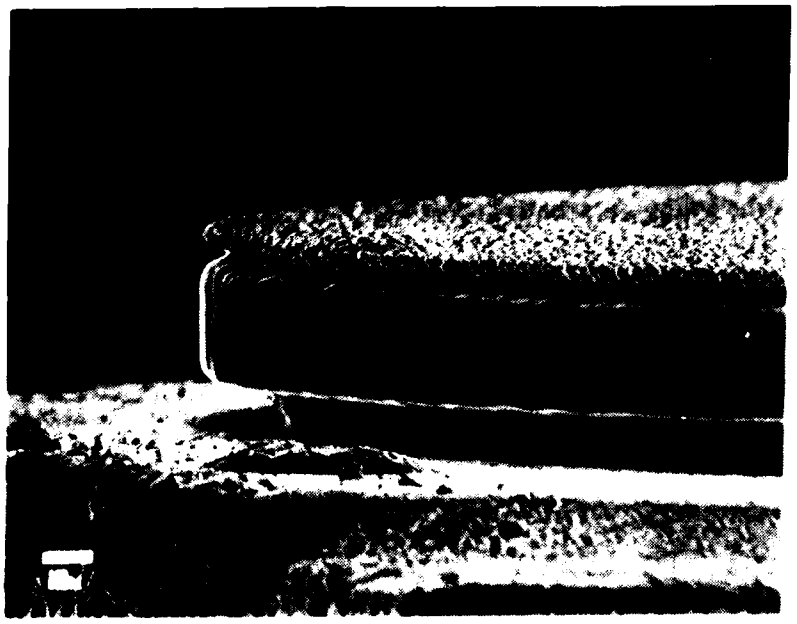


FIGURE 5-13 READ DOUBLE DRIFT DEVICE FROM WAFER 21693-1 FOLLOWING 335°C BAKE FOR 168 HOURS. RESIDUE NEAR THE JUNCTION IS SEEN

D-20794

The exact nature of the degradation has not been established. From the results obtained for Gunn Diode reliability at Microwave Associates, however, gold diffusion from the gold based contact metallization cannot be excluded. This diffusion would occur through the thin (nominal 1 μm) p+ contact into the p-type active layer resulting in a higher p-side doping with subsequent degradation of the breakdown voltage. Diffusion of gold into the junction region would also alter the diode DC characteristics.

This type of failure mechanism would not be operable for operating devices. In the case of operating diodes, the contact layer metallization on the p+ and PHS side is at a temperature only slightly higher than the case temperature and would, therefore, be restricted to temperature less than 125° during operation.

The EDAX results are not conclusive for gold penetration by diffusion. Sensitivity of the EDAX is limited to about 0.1% of the material analyzed which is insufficient to detect gold diffusion at electrically significant levels. Additionally, the presence of gold based metallization and gold heat sinks precludes the possibility of analyzing the gold content of the thin p+ contact layer.

6.0 PULSED STRESS TO FAILURE TESTING

6.1 INTRODUCTION

This test involves increasing the pulse current supplied to an oscillating device until failure occurs. The test is repeated under various pulse widths and duty cycle conditions, allowing determination of a safe operating region for the device. The trade-off between thermally induced failures and high field failures can also be evaluated. Failure analysis of devices from stress to failure tests allows identification of characteristic current overstress failure characteristics. Field failures can then be better analyzed using this information.

Devices were screened for early failures before subjecting them to the long term burn-in, storage temperature step stress, switching transient test, and the pulse to failure tests. Read double-drift profile (H-L/L-H-L) devices which were screened for early failures were used up for the long term pulsed RF burn-in and storage temperature step stress. Due to the excessive failures in storage temperature step stress, the test was repeated to confirm the results. Therefore, adequate number of screened read devices were not available for the pulsed to failure test. However, hybrid double-drift devices with similar early failures, long term RF burn-in, and step stress failure mechanisms were studied for this pulsed test to failure.

The tests were carried out at room temperature ambient in a stress to failure mode. The following 16 combinations of pulse width and duty cycle were used:

Pulse Width: 0.1, 1.0, 10, 20 microseconds

Duty Cycle: 1%, 10%, 25%, 50%

Output Power: (as controlled by bias current) increases from turn-on to power saturation or failure

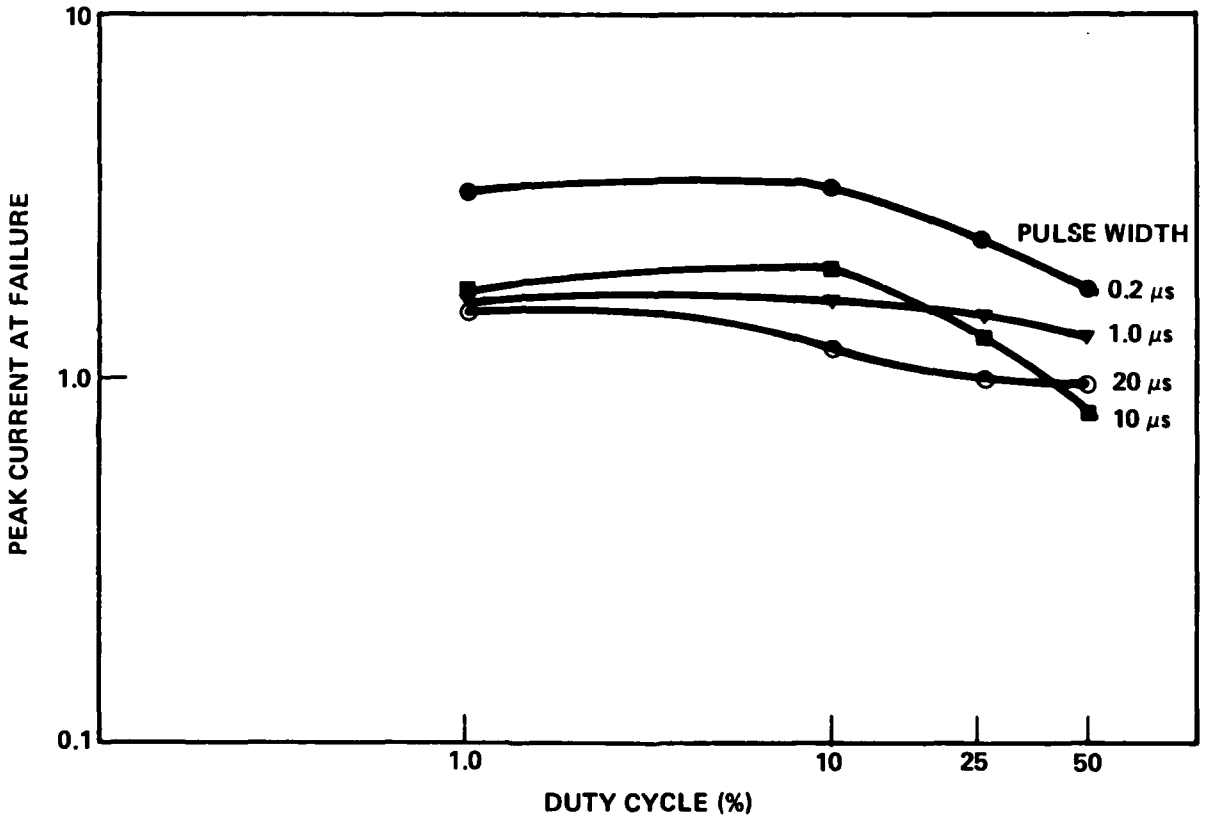
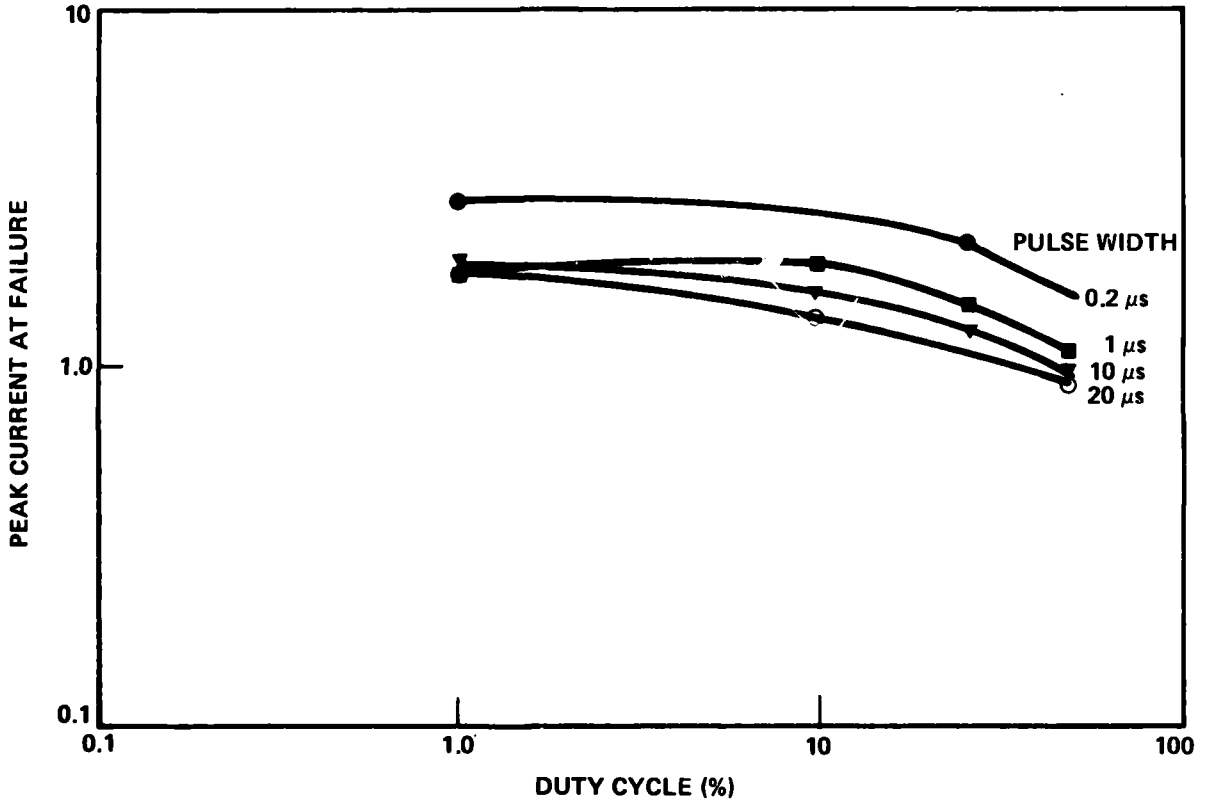


FIGURE 6-1 PULSED BURN-OUT TEST CURRENT AT FAILURE vs. DUTY CYCLE FOR VARIOUS WIDTHS FOR SINGLE DRIFT SCHOTTKY LHL X-BAND GaAs DEVICES

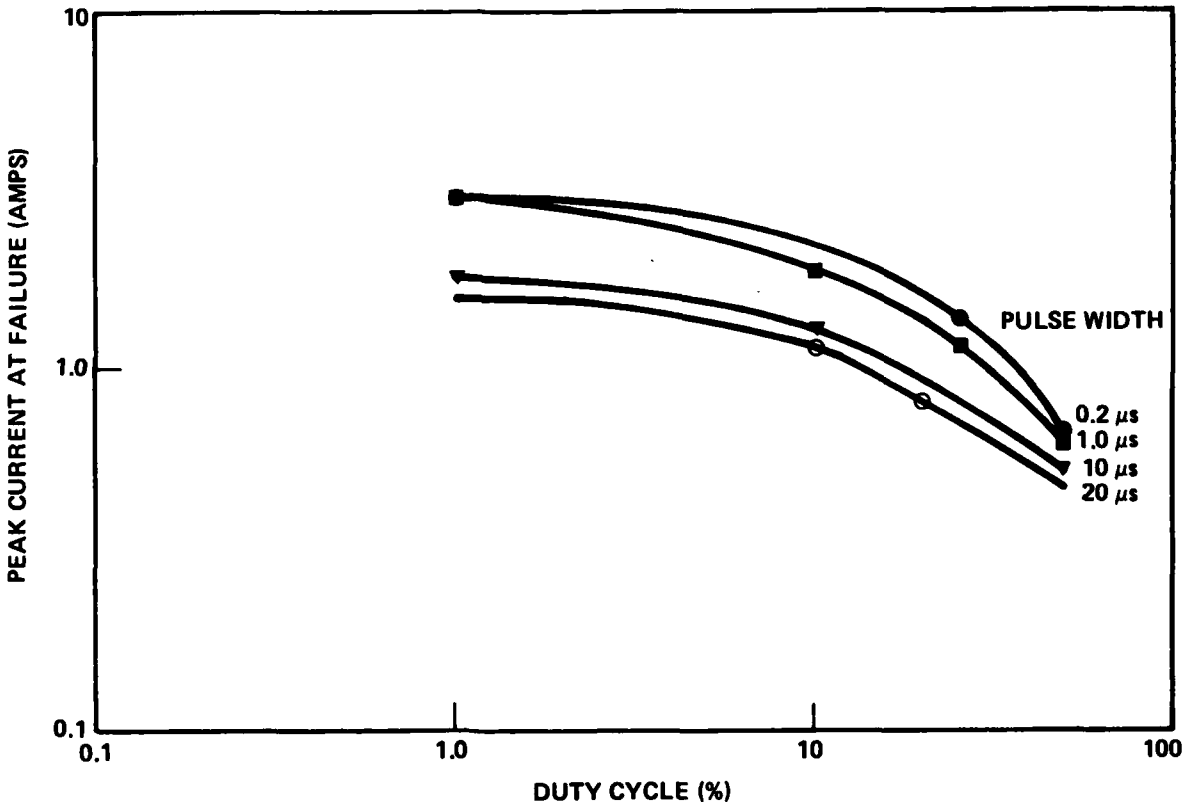
D-20816



WAFER 21359-1A–HYBRID DD

D-20817

FIGURE 6-2 PULSED BURN-OUT TEST CURRENT AT FAILURE vs. DUTY CYCLE FOR VARIOUS WIDTHS FOR HYBRID DOUBLE DRIFT GALLIUM ARSENIDE X-BAND DEVICES



SILICON DOUBLE DRIFT DEVICES 5082-710

FIGURE 6-3 PULSED BURN-OUT TEST CURRENT AT FAILURE vs. DUTY CYCLE FOR VARIOUS PULSE WIDTHS FOR SILICON FLAT PROFILE X-BAND DEVICES

D-20818

Single-drift Schottky L-H-L and double-drift hybrid gallium arsenide devices as well as silicon flat-profile devices were investigated.

6.2 Test Results

Figures 6-1, 6-2, and 6-3 present the results of the pulsed stress to failure test for single-drift Schottky L-H-L double-drift hybrid, and silicon devices, respectively, for a total of thirty-two devices of each type. All devices had survived a DC burn-in except for the silicon devices which had presumably been burned-in by the manufacturer. In general, failure has occurred at lower current when average power input has been increased, either by increasing pulse width or duty cycle. At constant duty cycle, failure current decreases with increasing pulse width in all cases except high duty operation with single-drift Schottky devices.

The gallium arsenide devices did not show much change in failure current for duty cycle variation from 1 to 10%. From 10 to 50%, a 50% reduction in failure current was seen. Silicon devices showed more sensitivity to duty cycle change, and dropped 30% in failure current from 1% to 10% duty cycle change, and 70% additional for 10% to 50% duty cycle change. This behavior indicates a larger sensitivity to average power dissipation than for the gallium arsenide devices. At the same time, the silicon devices appeared to be less sensitive to pulse width variations than the gallium arsenide. This behavior indicates a longer thermal time constant but greater temperature sensitivity.

6.3 Failure Analysis

The silicon devices failing in this test have been discovered previously (see section 3.2.2.1). Edge burn-out was observed in all the gallium arsenide devices examined (see figures 6-4, 6-5, and 6-6). Figure 6-6 is a top view of an edge burn-out failure and is characteristic of pulsed overstress failures. The ceramic need not be removed for identification of this type of failure.

Field service failures involving admitted accidental device overstress have been examined and have also shown edge failure. It may be concluded that edge failure is characteristic of pulsed over-stress operation.

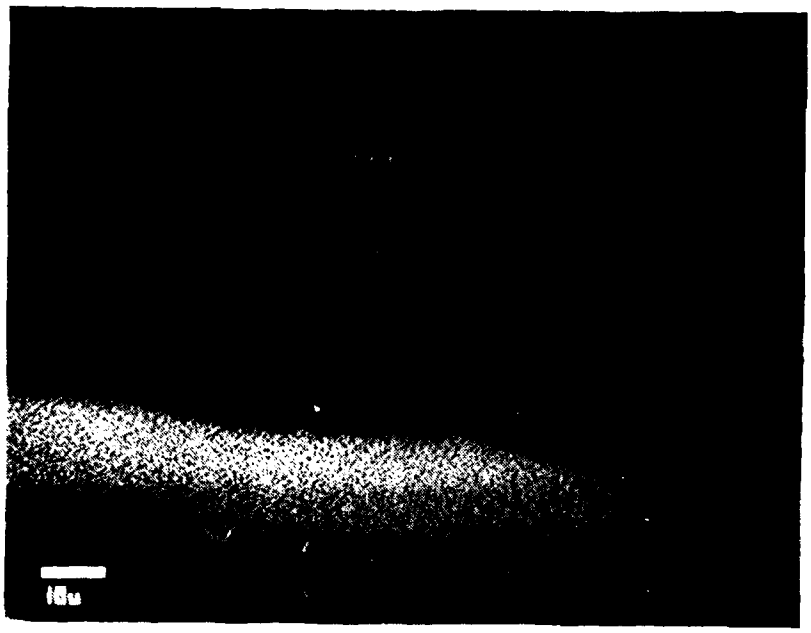


FIGURE 6-4 GALLIUM ARSENIDE HYBRID DOUBLE DRIFT DEVICE EXHIBITING EDGE FAILURE DURING PULSED STRESS TO FAILURE TESTING

D-20798

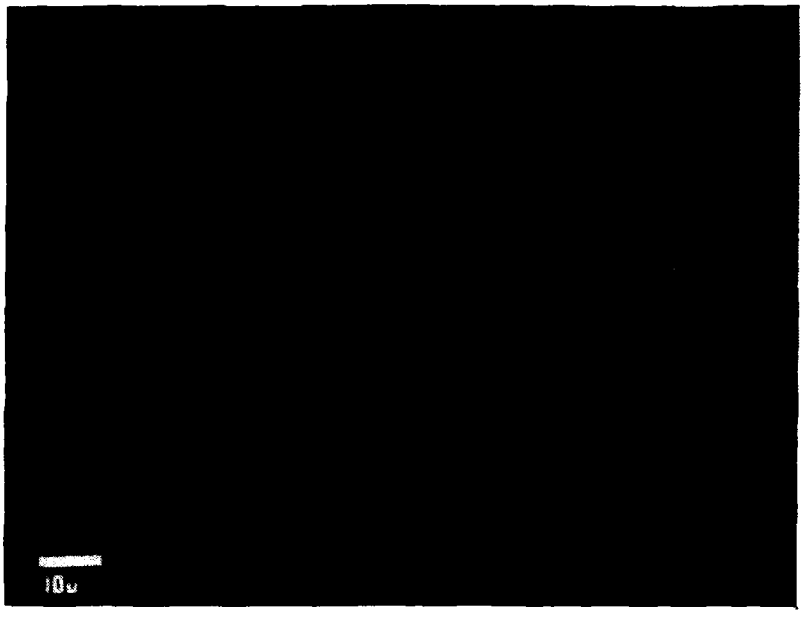


FIGURE 6-5 GALLIUM ARSENIDE HYBRID DOUBLE DRIFT DEVICE EXHIBITING EDGE FAILURES DURING PULSED STRESS TO FAILURE TESTING

D-20797

FIGURE 6-6 SINGLE DRIFT SCHOTTKY DEVICE SHOWING CHARACTERISTIC EDGE BURN-OUT DUE TO PULSED OVER-STRESS

D-20796

7.0 SPECIAL TESTS

7.1 Introduction

Two special tests were conducted to further access the reliability of gallium arsenide pulsed double-drift devices. The first test, a temperature cycling test, involved twenty-five (25) cycles from -65 to +110°C with 15 minutes at extremes. Such a test is useful in evaluating bond integrity, both chip to package and wire bond to chip.

The second special test involved a switching transient test where ten (10) Read double-drift devices were operated under pulsed RF burn-in conditions with the added complication that the pulsed bias was switched on and off every minute. If detremental switching transients should occur, this test would produce a higher failure rate than the normal RF burn-in test.

7.2 Test Results

7.2.1 Temperature Cycling Test

Eight (8) hybrid double-drift devices from wafer number 21613-1 were cycled twenty-five (25) times from -65 to +110°C without bias for this test. No change in device DC or RF parameters were observed in this test, indicating that bond integrity was excellent.

7.2.2 Switching Transient Test

Ten (10) Read Double-drift devices were selected for use in this test, and were placed on pulsed RF burn-in under the following conditions:

V_{op}	=	88 Volts, Peak
I_{op}	=	0.9 A, Peak
P_o	=	1.5 W, Peak
T_{case}	=	80°C
Avg Thermal Resistance	=	8°C/W
T_J	=	258°C

In addition, the pulsed bias was switched on and off every minute. Following 2200 hours of operation, three units had failed (at 24, 81, and 105 hours). These failures do not represent excessive failures above the rate observed without the switching.

8.0 SUMMARY AND CONCLUSIONS

Reliability characteristics of high power pulsed IMPATT diodes were studied. The devices included GaAs single-drift, hybrid double-drift and Read double-drift devices fabricated at Microwave Associates and silicon flat-profile double-drift deivces purchased commercially from Hewlett-Packard.

Various screening tests were evaluated for effectiveness in removing defective devices from a newly manufactured lot. DC burn-in and pulsed RF burn-in were evaluated. For the GaAs double-drift devices, DC burn-in is inadequate and either pulsed DC or pulsed RF burn-in is required. Both techniques appear equally effective. For single-drift GaAs devices, pulsed RF burn-in is the preferred technique. For the silicon double-drift diodes, the results are not sufficiently extensive to draw conclusions between DC and pulsed DC burn-in; both appear acc otable.

The primary failure under RF oscillating conditions for GaAs IMPATT diodes is a failure at the mesa surface. These devices are not passivated and the failure may be due to surface migration of residual impurities on the surface or remaining in the package from the diode fabrication procedure. Since the advent of this program, passivation techniques have been developed which would eliminate those types of problems. This technology was not available during this program, and it is believed that the edge initiated failures have prevented the determination of the wear-out mechanism and the MTTF.

High temperature storage step stress tests were carried out to attempt to study long-term wear-out mechanisms. The devices showed irreversible changes in the DC characteristics. Gold diffusion

from the gold based metallization system may occur and result in the observed behavior. This mechanism would be similar to that observed in the Gunn diode reliability studies. This mechanism would, however, not be expected to be operable in operating devices where the temperature of the contact metallization is appreciable ($\sim$ 200°C) colder than the metallization temperature reached during the high temperature storage tests (> 300°C). It has, therefore, not been possible to determine the wear-out mechanism from these studies.

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