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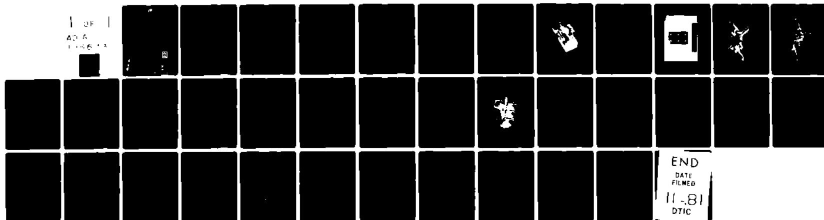

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M.L. Stevens

Characterization of Power MESFETs at 21 GHz

15 September 1981

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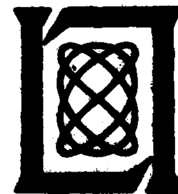
Lincoln Laboratory
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Lexington, Massachusetts



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CHARACTERIZATION OF POWER MESFETS AT 21 GHz

M.L. STEVENS

Group 63

TECHNICAL REPORT 579

15 SEPTEMBER 1981

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LEXINGTON MASSACHUSETTS

ABSTRACT

This report describes the development of GaAs MESFET power amplifiers at 21 GHz. Techniques for making large-signal loadpull and "S" parameter measurements at these frequencies, and the measured device characteristics are presented. A unique method of obtaining accurate gain and power measurements is discussed. Design methods and data are presented on 21 GHz amplifiers with more CW power and higher efficiency than previously achieved.

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I. INTRODUCTION

The MIT Lincoln Laboratory Space Communications Program is currently involved with emerging technology for solid-state EHF communications-satellite systems.

A concept which would provide secure communications to a large number of small mobile users is currently under development [REF. 1]. This concept includes a 44 GHz FDM uplink with multiple narrow beams, antenna nulling and onboard signal processing. The proposed downlink is a 21 GHz beam-hopped, frequency-hopped TDM system.

This report describes the progress in development of components for a solid-state satellite transmitter at 21 GHz, including the results of Lincoln Laboratory sponsored development of GaAs power MESFETs. New large-signal characterization techniques are described, and unique gain and output-power measurement methods are discussed. Finally, data is presented showing the DC-to-RF conversion efficiency (of solid-state amplifiers at 21 GHz) significantly higher than any previously reported [REF. 2, 3, 4].

II. DEVICE DEVELOPMENT

During the past year Lincoln Laboratory has sponsored a development program for GaAs MESFETs at 21 GHz. Table I shows the program goals and the acceptable minimum characteristics of the devices.

TABLE I

POWER GaAs FET SPECIFICATIONS

CHARACTERISTIC	GOAL	MINIMUM
Power Output (W)	1	0.5
Power-added Efficiency (%)	20	15
Gain @ 1 dB Compression (dB)	5	4
Channel Temperature Rise (°C)		<100

The power MESFETs were developed by Microwave Semiconductor Corporation, Somerset, NJ.

Power FETs were constructed with 1.0μm and 0.7μm gate lengths. The gate width was 75μm with a 1200μm gate periphery. The GaAs chips were flip-chip mounted to a gold-plated copper carrier as shown in Fig. 1. The resulting average thermal resistance was reported as approximately 13°C/W [REF. 2].

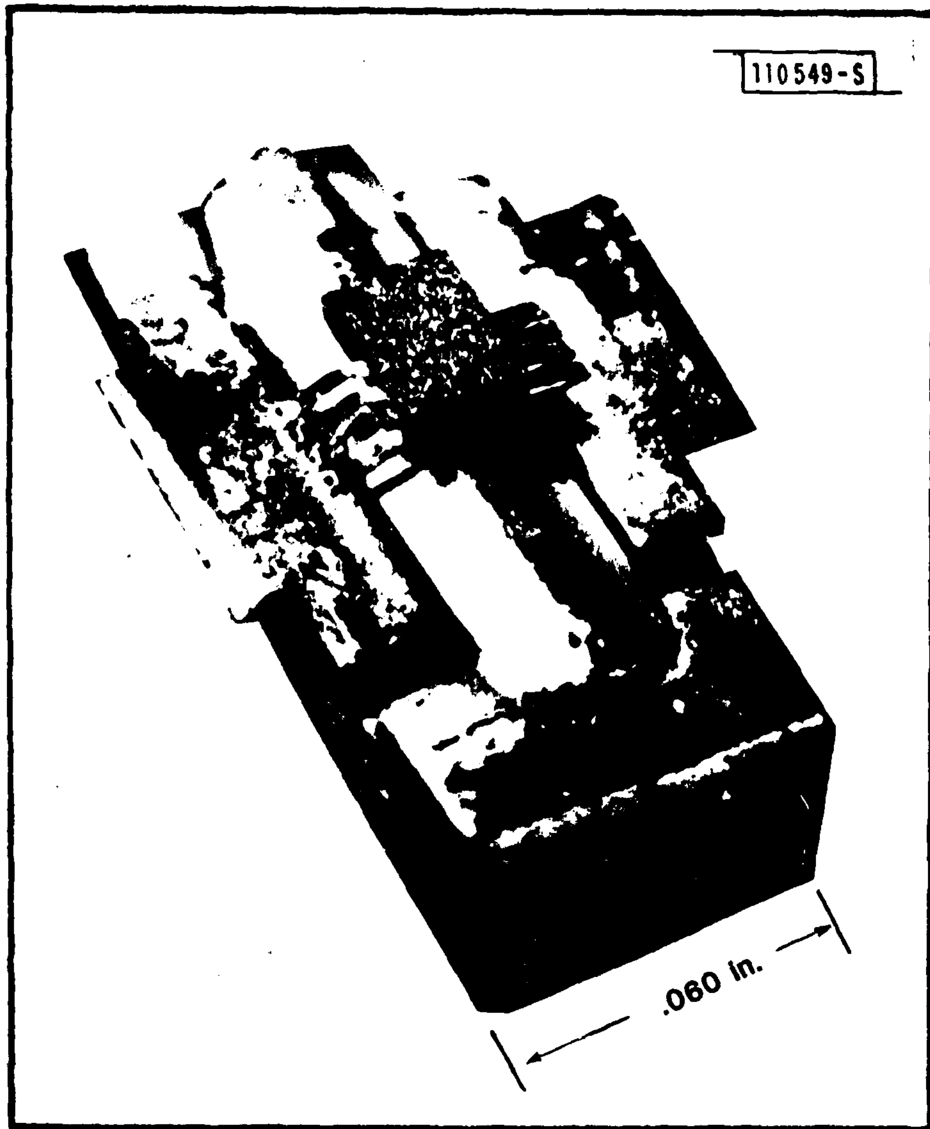


Fig. 1. 0.5 W GaAs MESFET.

III. TEST FIXTURE DEVELOPMENT

The GaAs MESFETs are being characterized at Lincoln Laboratory using specially designed fixtures and unique components which were developed for operation at K-band frequencies.

A bias-tee was designed and constructed for use between 12 and 24 GHz based on a microwave-diplexer filter. The bias-tee is constructed using air and teflon-loaded coaxial transmission-line sections. The through-loss of the bias-tee measures less than 1 dB from 12.6 to 24 GHz. Between 15 and 21.5 GHz the loss measures between 0.25 and 0.50 dB. DC resistance through the low-pass filter section measures $\approx 30\text{m}\Omega$. The bias-tee is shown in Fig. 2.

A slabline transistor holder was designed and constructed as shown in Fig. 3. The slabline construction consists of two parallel ground planes separated by an air gap. Suspended between the ground planes is a center conductor with a circular cross-section. The slabline is precision-made with a 50Ω characteristic impedance. At the center of the slabline is a shim which is large enough to mount a flip-chip packaged GaAs FET. The FET is held in place by two clamps which hold the flange of the flip-chip carrier on the shim. Electrical contact is made by resting the center conductors of the slabline on the drain and gate standoffs of the transistor. The conductors are held in place by a rexolite yoke which also applies the appropriate contact pressure.

Air-dielectric slabline was chosen for several reasons. First, the 50Ω characteristic impedance is unaffected by movement of the center conductor in the vertical direction. This allows freedom of movement for positioning the conductors on the gate and drain standoffs and allows for different standoff heights due to the manufacturing tolerances of the flip-chip package. Second, the air-dielectric structure provides very low losses, an improvement that enhances the accuracy of device performance measurements. Third, the slabline structure easily lends itself to variable impedance matching by the introduction of a moveable slug into the slabline structure. Figure 4 shows the slabline holder with one side removed, exposing the center conductors and tuning slugs. The tuning slugs are black-anodized aluminum.

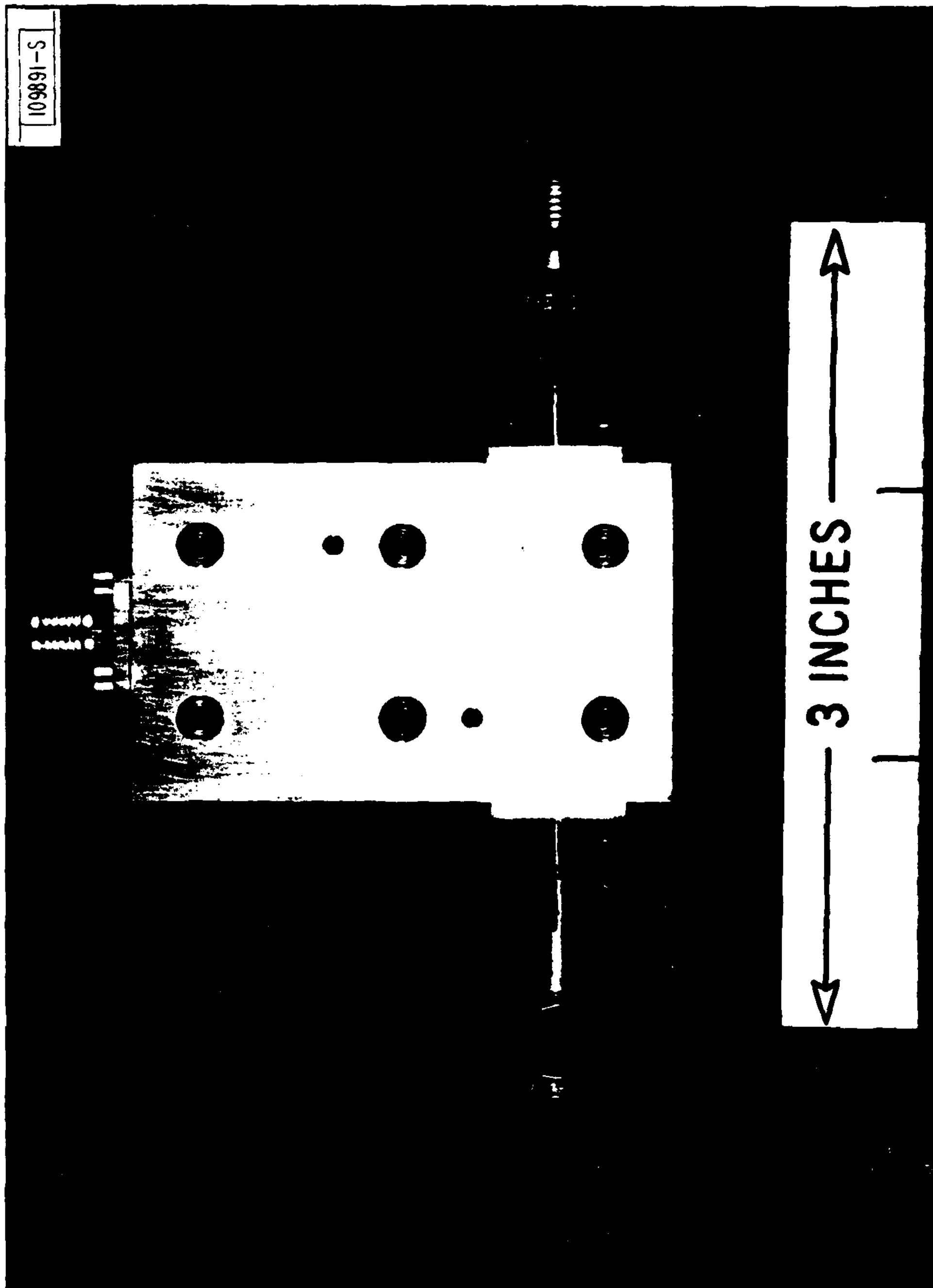


Fig. 2. Microwave diplexer bias-tee.

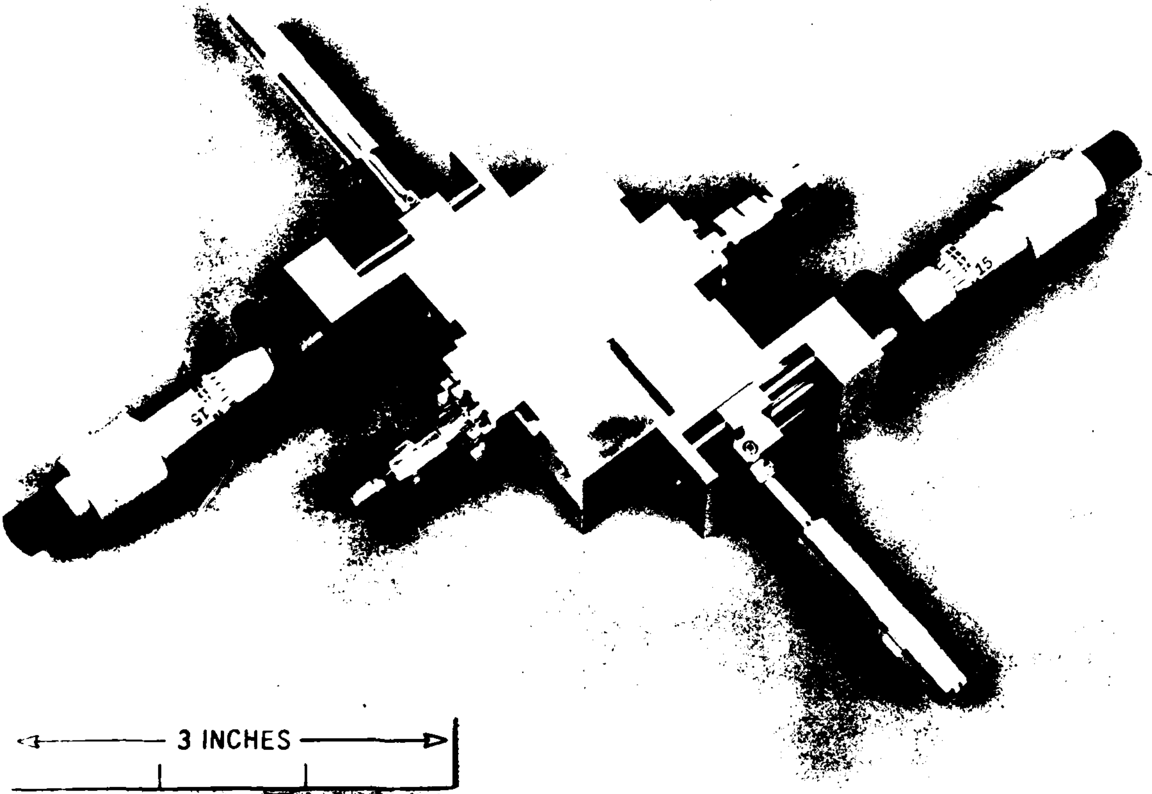


Fig. 3. Slabline transistor holder.

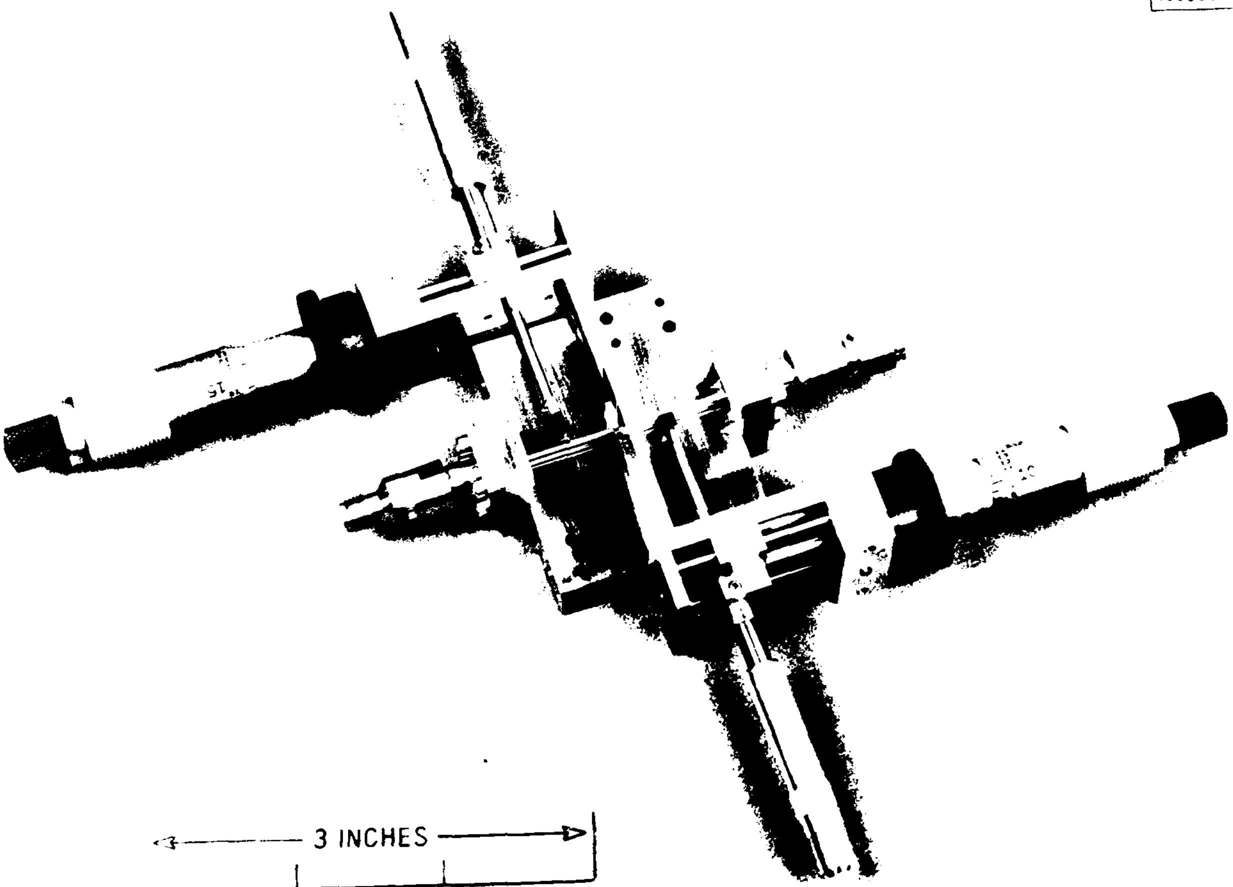


Fig. 4. Slabline transistor holder with side removed showing internal construction.

The slabline test fixture provides a versatile characterization tool at 21 GHz. When used as a precision 50Ω test fixture the slabline can be used for large and small-signal network analysis of the 21 GHz GaAs FETs. With the addition of the variable tuning slugs, the transistors can be matched for optimum performance at any particular frequency in the band of interest. Gain, efficiency, and output power can then be measured for any desired set of operating parameters, including frequency, input-power level, and bias conditions. Because of the small losses in the slabline and tuning structures, these measurements yield useful data on the performance which can be expected when these devices are used in an amplifier circuit.

Finally the slabline fixture can serve as a test-bed for various matching filter configurations which are designed from the data obtained in large-signal input-impedance and load-pull measurements.

IV. GaAs FET CHARACTERIZATION

A simplified block diagram of the GaAs FET characterization set-up is shown in Fig. 5. The set-up is shown configured for load-pull or gain measurements. By turning the waveguide switch and reversing the connections on the harmonic converter and the device-under-test (DUT), the set-up can be configured for large-signal input-impedance measurements.

Computer-controlled automatic error correction is vital to obtain accurate measurements at 21 GHz. In addition, the signal generator, an HP 8620, 2-22 GHz sweeper, is phase-locked to an HP 8660 synthesizer to maintain low phase noise and high frequency accuracy during the measurements. A Tektronix 4051 graphic controller is used to perform the necessary error correction and to control and gather data from the instruments in the test set-up.

Although the load-pull set-up is similar to others that have been published previously, [REF 5, 6] the calibration technique is unique, and the method of absolute output-power measurement is new. The output-power measurement technique determines the actual output power of the device-under-test without the errors normally caused by lossy test fixtures, bias-tees, couplers, tuners, and other components in the set-up.

A model of the load-pull measurement is shown in Fig. 6. The load-pull tuner and waveguide termination are lumped together to obtain the load-reflection coefficient (Γ_L). The purpose of the load-pull measurement is to determine the load reflection coefficient at the plane of the device-under-test which is labeled the reference plane. Between the reference plane and the load is shown the measurement plane, which may exist only in a mathematical sense. In an ideal system, the measurement plane may be defined as the position in the test set-up where the measured reflection coefficient is identical to the actual reflection coefficient. A manually operated network analyzer is adjusted so that the measurement plane is at the reference plane and, with limited accuracy, the desired reflection coefficient is read directly from the analyzer screen. Real-world network

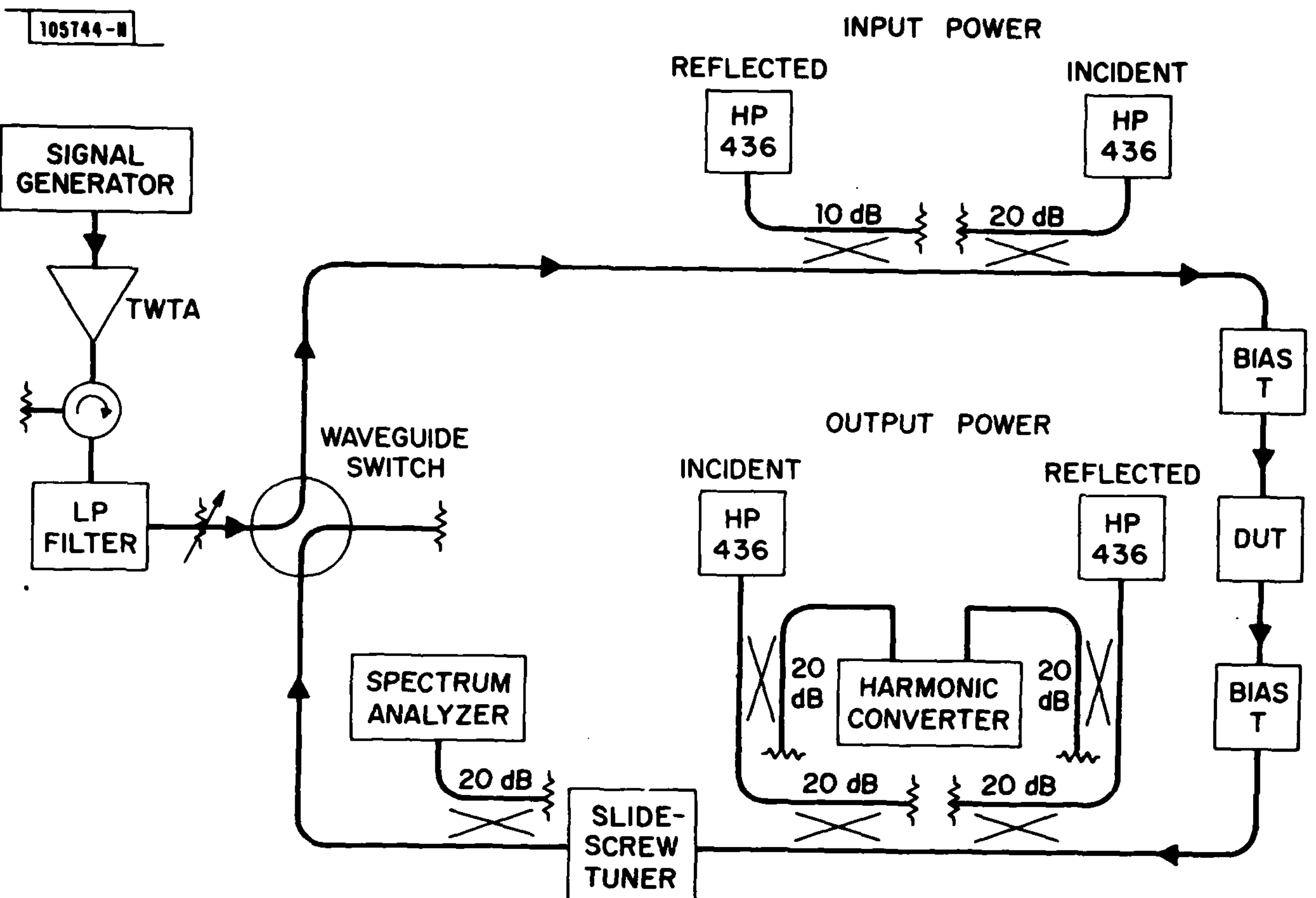


Fig. 5. Load-pull measurement set up.

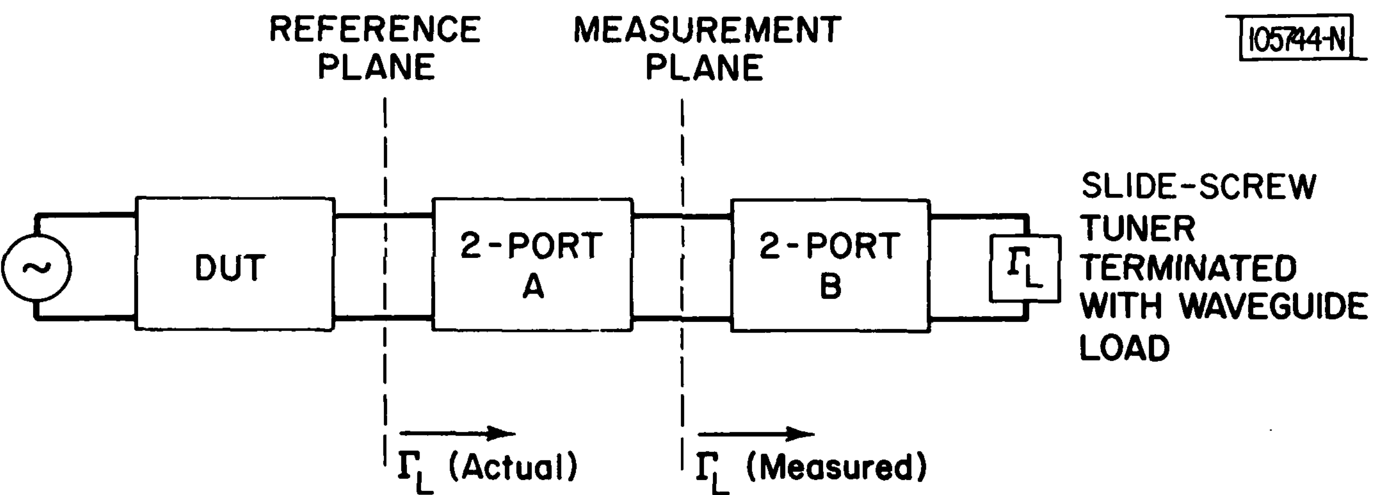


Fig. 6. Load-pull measurement model.

analyzers may have no physically accessible location which corresponds to the measurement plane. In the general case, the measurement plane is separated from the reference plane by the effects of errors in the system, including the finite directivity of couplers, losses, and differential line lengths between the reference and test ports of the harmonic converter. The effects of these errors can be modeled as an imaginary two-port which connects the reference plane to the measurement plane [REF 7]. If the two-port parameters of the imaginary two-port, are known, the reflection coefficient at the reference plane can be found by de-embedding the measured reflection coefficient through the imaginary two-port.

The two-port S-parameters of the imaginary two-port can be determined for the load-pull measurement by the technique shown in Fig. 7. The load has been replaced by the signal source, and the device-under-test has been replaced by a short at the reference plane. The reflection coefficient of the short (Γ_{short}) appears to the analyzer as $1/\Gamma_{short}$. The relationship between the measured reflection coefficient (Γ_M) and the reflection coefficient at the reference plane (Γ_R) is given by

$$\Gamma_R = S_{11_A} + \frac{S_{21_A} S_{12_A} \Gamma_M}{1 - \Gamma_M S_{22_A}} \qquad (1)$$

where S_{11_A}, S_{21_A}, S_{12_A}, and S_{22_A} are the two-port S-parameters of the imaginary two-port. Equation 1 may be rewritten as

$$\Gamma_R = S_{11_A} + \Gamma_R \Gamma_M S_{22_A} - \Gamma_M \Delta S_A \qquad (2)$$

where

$$\Delta S_A = S_{11_A} S_{22_A} - S_{21_A} S_{12_A} \qquad (3)$$

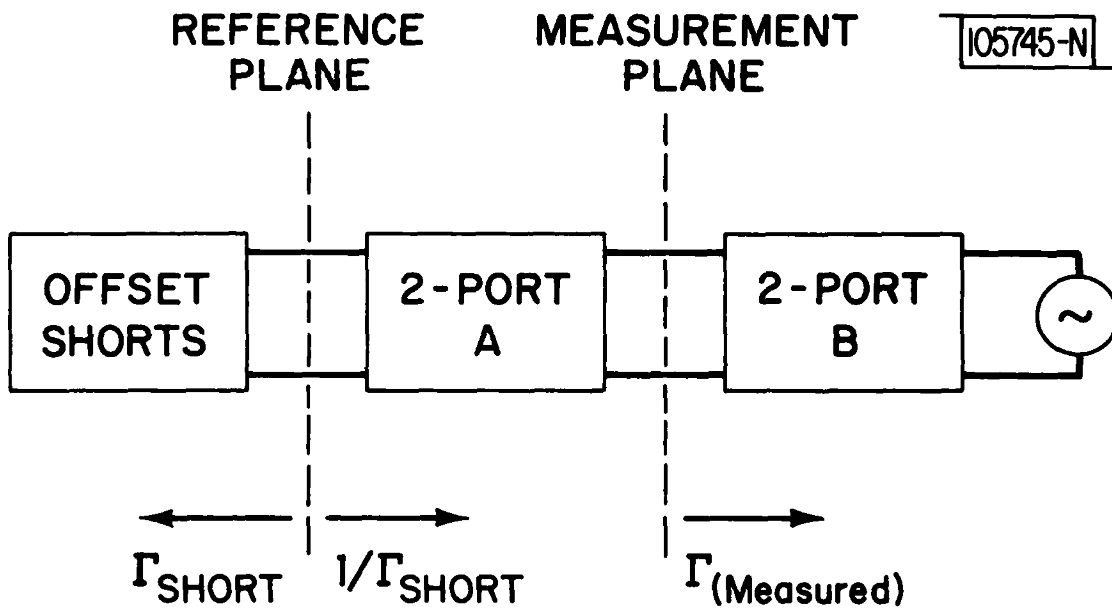


Fig. 7. Load-pull calibration model.

The three unknowns in equation 2 are S_{11_A}, S_{22_A}, and ΔS_A. By making three measurements using three arbitrary (but known) standards, a system of three equations with three unknowns (of the form of equation 2) can be solved simultaneously, yielding the S-parameter values needed in equation 1. The S-parameters are given by the following equations:

$$S_{22_A} = \frac{(X_3 - X_2)\, X_1\, \Gamma_1 + (X_1 - X_3)\, X_2\, \Gamma_2 + (X_2 - X_1)\, X_3\, \Gamma_3}{(X_1 - X_2)\, X_3\, \Gamma_1\, \Gamma_2 + (X_2 - X_3)\, X_1\, \Gamma_2\, \Gamma_3 + (X_3 - X_1)\, X_2\, \Gamma_1\, \Gamma_3} \tag{4}$$

$$\Delta S_A = \frac{S_{22_A}\,(\Gamma_1\, X_2 - \Gamma_2\, X_1) - (X_2 - X_1)}{X_1\, X_2\, (\Gamma_1 - \Gamma_2)} \tag{5}$$

$$S_{11_A} = \Delta S_A\, \Gamma_1 - \frac{S_{22_A}\, \Gamma_1 + 1}{X_1} \tag{6}$$

$$S_{21_A}\, S_{12_A} = S_{11_A}\, S_{22_A} - \Delta S_A \tag{7}$$

where X_i = actual reflection coefficient of standard i.
Γ_i = measured reflection coefficient of standard i.

The most convenient standards to use for the load-pull measurement are a "reference" short and two different-length offset-shorts. For the best calibration the length of the offset-shorts should be chosen such that the angles of the reflection coefficients of the three shorts differ by $\approx 120°$ from each other, which places the shorts symmetrically around the outer edge of the Smith chart. When two of the shorts lie in the same quadrant of the Smith chart, inaccuracies can occur due to the finite resolution of the arithmetic processor which is used to do the calculations.

A 50Ω load cannot be used as a load-pull calibration standard since $1/\Gamma_L$ for a 50Ω load is ∞, which is beyond the dynamic range of the analyzer.

The offset shorts which are used with the slabline test fixture are shown in Fig. 8. The shorts are constructed identically to the slabline fixture except that the shim for mounting the GaAs FET is replaced by a solid plate.

Until now one of the major drawbacks of the loadpull technique was that an accurate measurement of the device's output power could not be obtained. This is because the output power was measured after the load-pull tuner. The losses in the load-pull set-up between the device-under-test and the tuner are dependent on the standing wave which exists in this region. Therefore, the losses vary with different settings of the tuner. The loss in the tuner itself is also a function of the tuner settings and, therefore, cannot be accurately taken into consideration. These losses result in large inaccuracies in the load-pull measurement, because the indicated optimum-power point is a system measurement of the entire load-pull set-up and not of the device-under-test.

In a recent paper [REF 6] a differential-power-meter technique was reported which makes use of two power meters to measure the forward and reflected power before the tuner. The output power is then found by taking the difference between the forward and reflected powers. This technique eliminates the variable losses due to the tuner, but it still does not take into account the variable losses due to the standing waves between the device-under-test and the tuner. The effects of a standing wave on a low-loss component such as a bias-tee are illustrated by example in Fig. 9. The problem becomes most severe for high standing-wave ratios, where the effective loss becomes very high.

A new technique for measuring output power is shown in Fig. 10. A single power meter is placed between the tuner and the device-under-test to measure the power incident on the load-pull tuner. Calibration of this power meter is accomplished in the usual way by substituting a known power source at the frequency of interest in place of the device-under-test. This meter can now

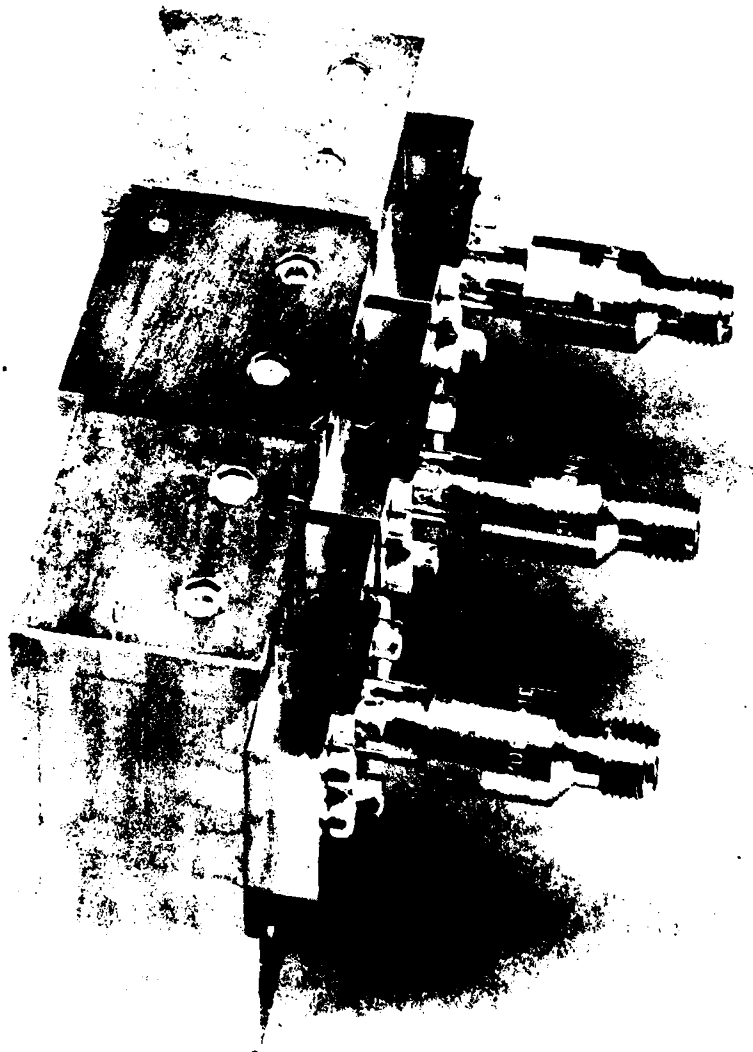
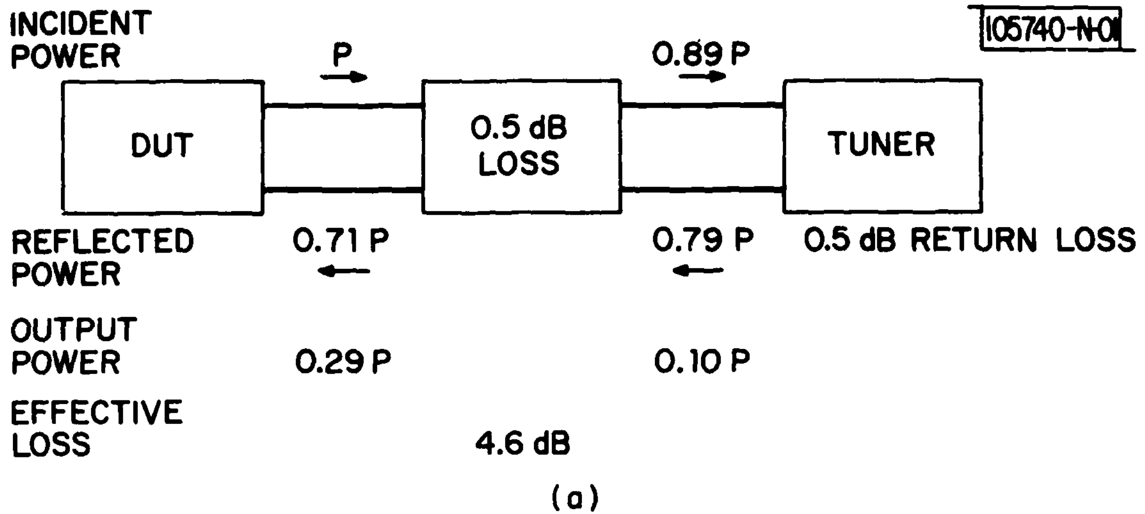


Fig. 8. Slabline reference and offset shorts.



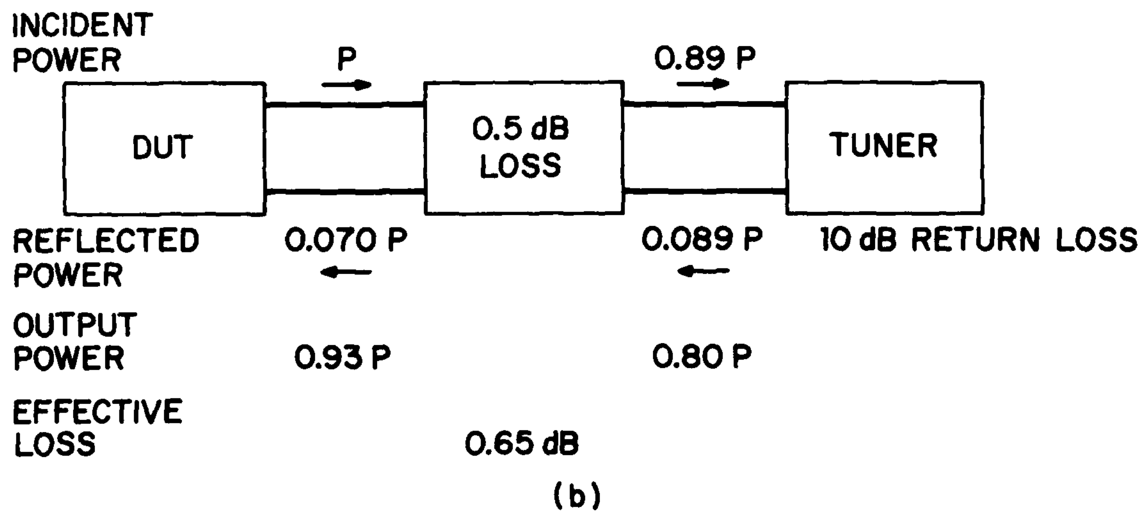
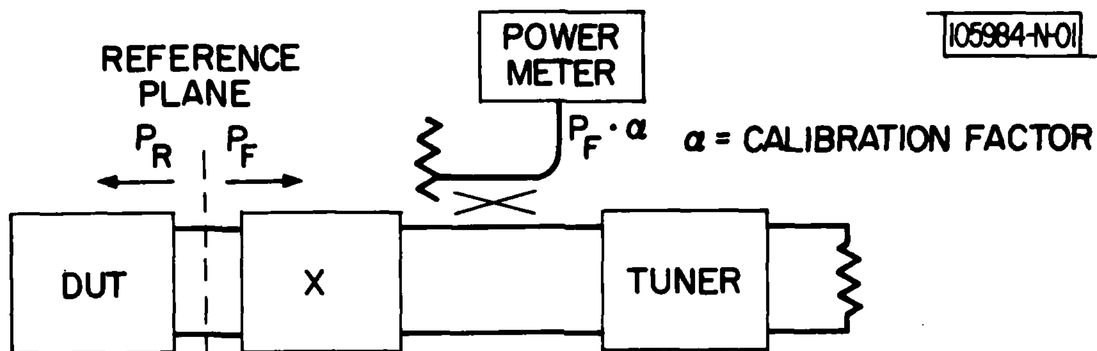


Fig. 9. Losses in a region of high standing waves: (a) Low return loss. (b) High return loss.



$$\vec{\Gamma}_L$$

$$\frac{P_R}{P_F} = |\Gamma_L|^2$$

$$P_{OUT} = P_F - P_R$$

$$P_{OUT} = P_F\,(1 - |\Gamma_L|^2)$$

Fig. 10. Load-pull power measurement.

measure the actual forward power at the reference plane of the device-under test. The reflected power at the device-under-test is calculated from the actual load reflection coefficient which has been determined in the load-pull measurement. The forward and reflected powers are related to the load reflection coefficient by:

$$\frac{P_R}{P_F} = |\Gamma_L|^2 \qquad (8)$$

Since

$$P_{OUT} = P_F - P_R \qquad (9)$$

then

$$P_{OUT} = P_F (1 - |\Gamma_L|^2) \qquad (10)$$

Equation 10 gives the actual output power of the device-under-test at the reference plane of the load-pull measurement.

V. DEVICE PERFORMANCE

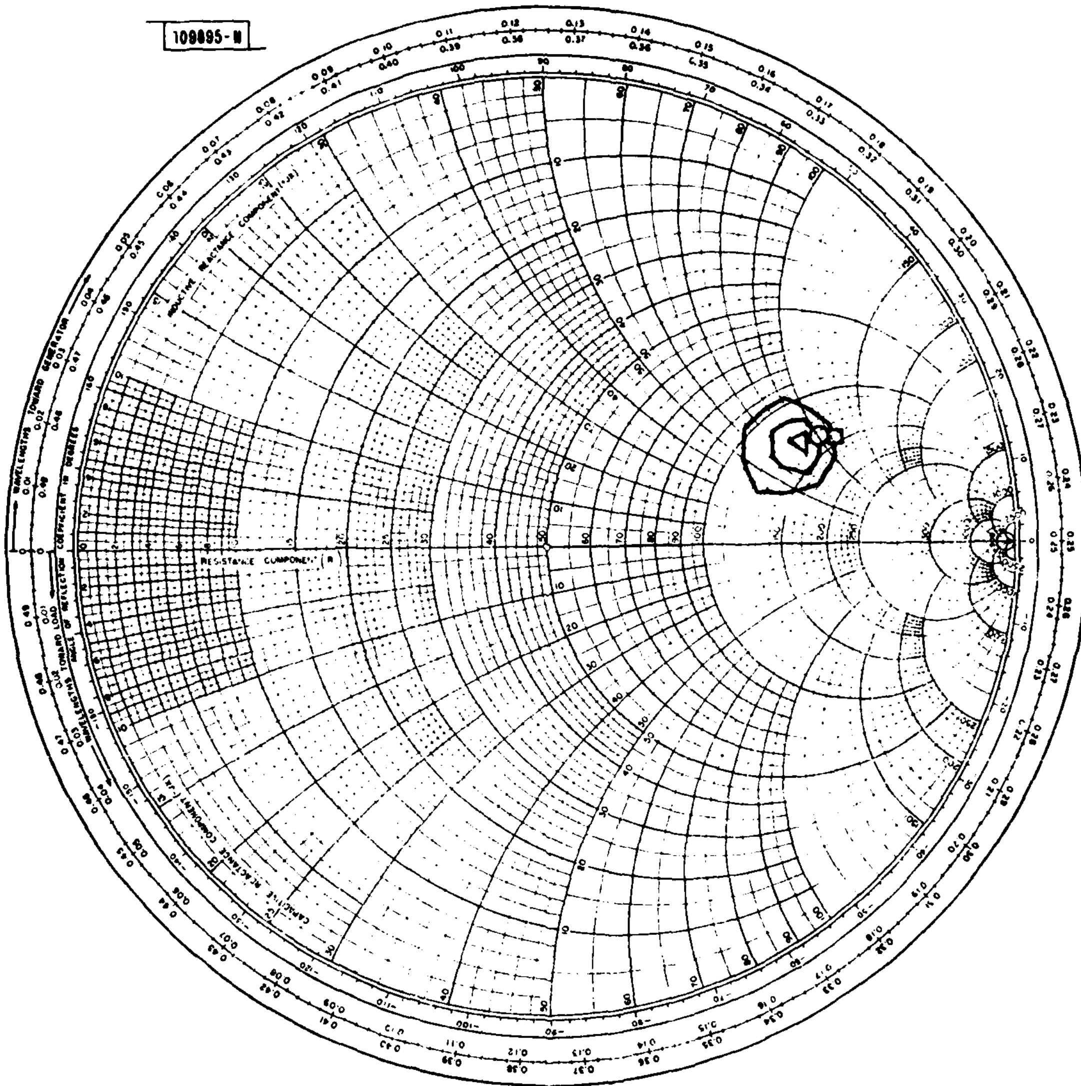
Initial measurements on the FETs showed that the desired load impedance was very close to the limits of tuning which could be achieved by the slide-screw tuner alone. In order to achieve greater accuracy and tuning range, a slabline matching circuit was constructed using stepped-impedance transmission-line sections.

Subsequent measurements were made with the aid of the partial matching provided by the slabline matching circuit. The load-pull data was then de-embedded from the matching filter to provide load impedance data at the transistor. A typical load-pull measurement is shown in Fig. 11.

Load impedance and bias conditions for optimum power and for optimum efficiency have been determined for several transistors. The spread in measured load impedances for both optimum power and optimum efficiency is shown in Fig. 12. Figure 13 shows histograms of the number of measured devices which fall into various performance ranges of power and efficiency. Separate histograms are shown for the same devices with high-power bias and tuning, and with high-efficiency bias and tuning conditions, at both 20 and 21 GHz. The highest power measured at 21 GHz was 620 mW with 3 dB of gain and 24.3% power-added efficiency. The same device when tuned and biased for optimum efficiency produced 400 mW of output power with 3.7 dB of gain and 35.7% power-added efficiency.

Characterization of the large-signal input impedance of the GaAs FETs has yielded the typical data shown in Fig. 14.

A number of GaAs FETs have also been characterized for gain, output power, and efficiency with the inclusion of the slug tuners in the slabline test fixture. Figure 15 shows a summary of measurements taken on 17 different devices from three different wafers. Figure 15 shows the best power-added efficiency obtained for each device and the corresponding gain and output power. The best efficiency obtained with the slabline tuners is 22.3% with 4.5 dB of gain and 288 mW of output power at 21 GHz. Figure 16 shows the power, gain, and efficiency versus RF drive level of a typical device tuned for maximum power-added efficiency in the slabline tuner.



RING	P OUT (W)	GAIN (dB)	EFF	IDC (A)
△	0.284	3.56	0.304	0.095
○	0.281	3.52	0.304	0.093
□	0.274	3.41	0.300	0.091

Fig. 11(a). 0.5 W power MESFET load-pull measurement.

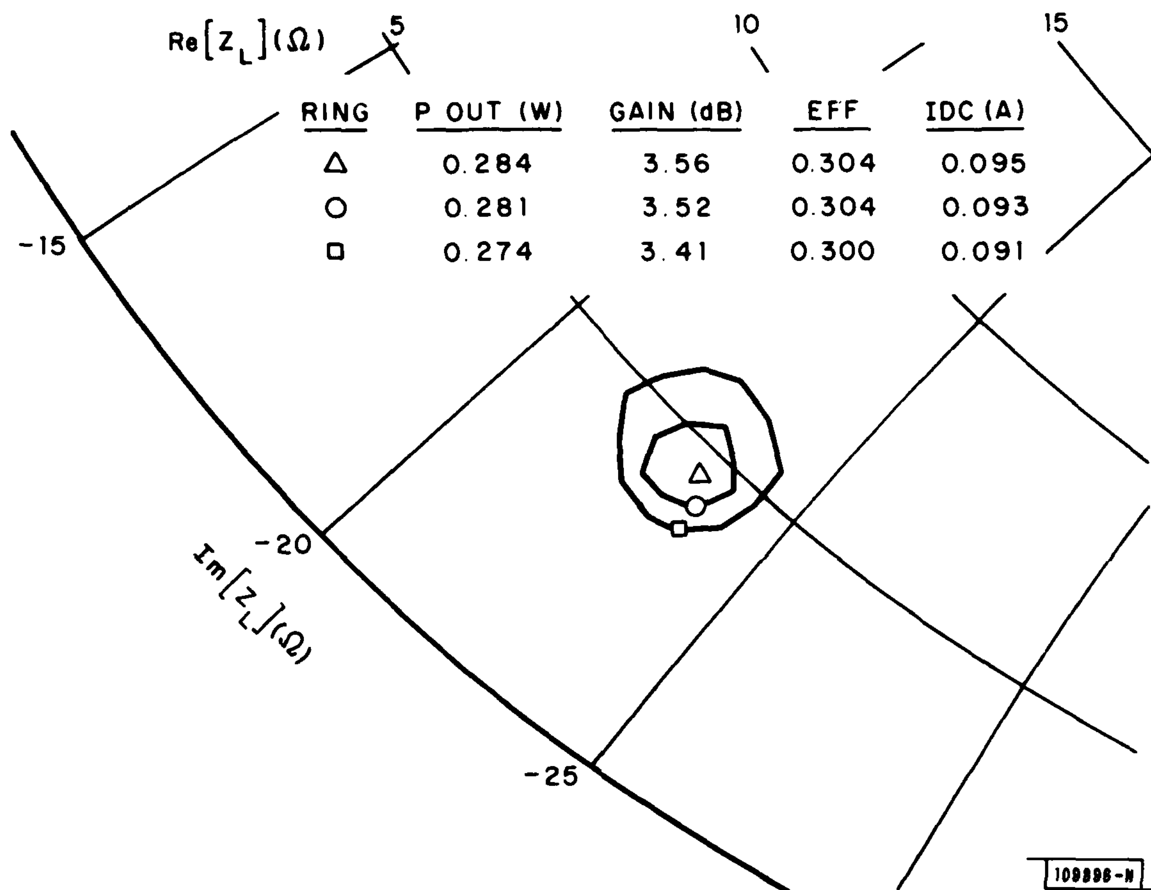
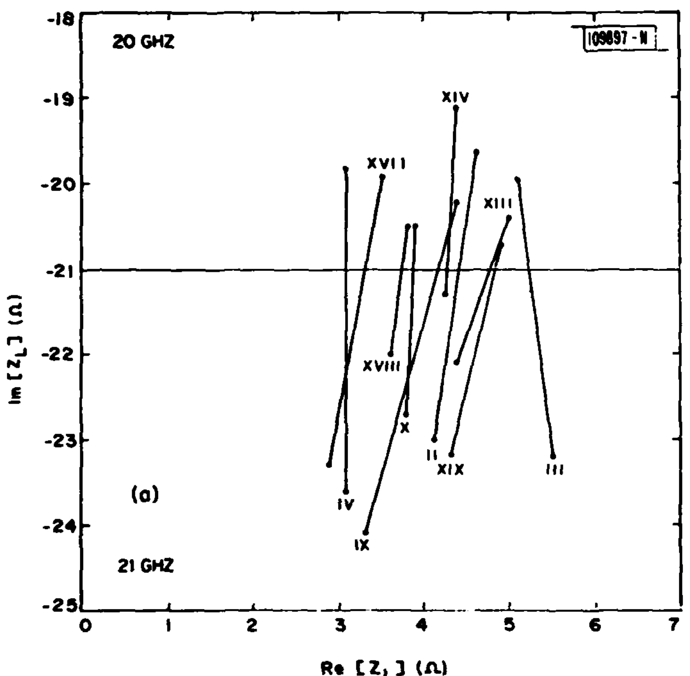


Fig. 11(b). 0.5 W power MESFET load-pull de-embedded data.



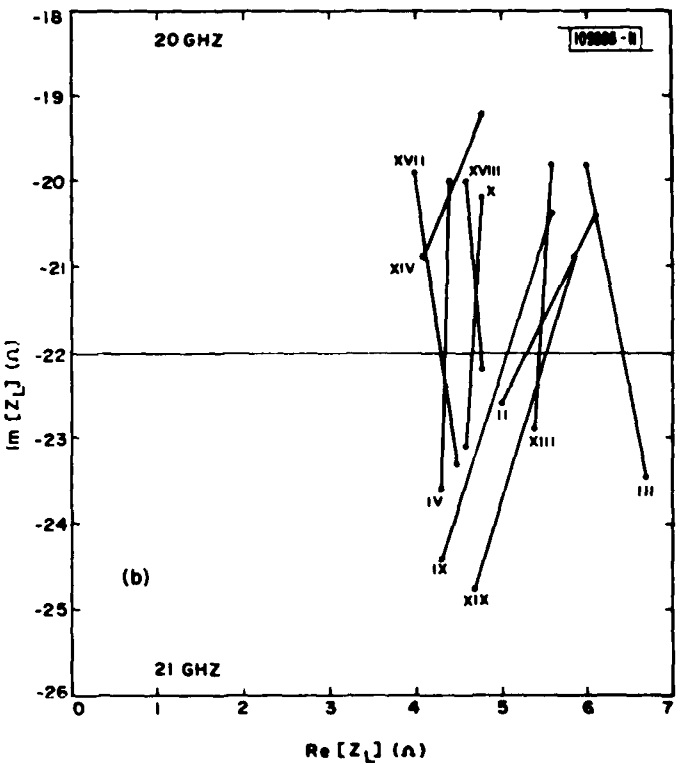
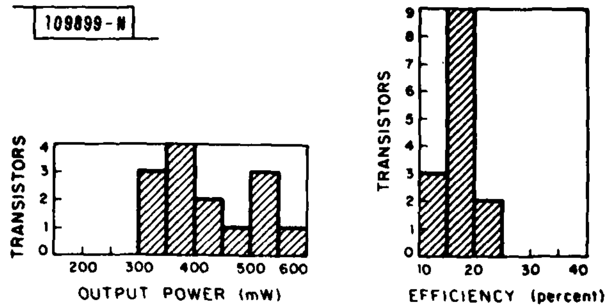
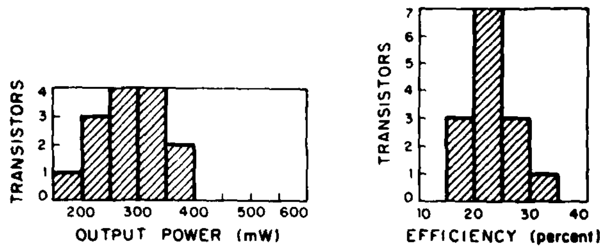
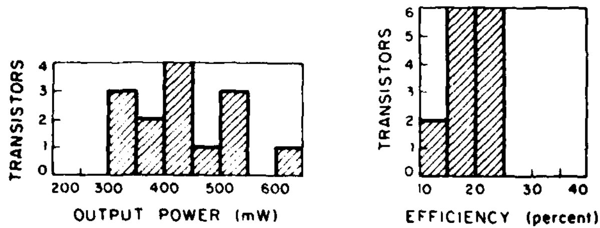


Fig. 12. 0.5 W power MESFET measured optimum load impedances: (a) Optimum power bias and tuning. (b) Optimum efficiency bias and tuning.







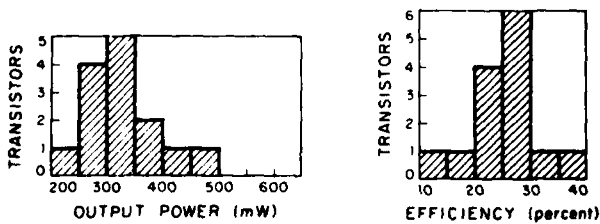


Fig. 13. 0.5 W power MESFET performance summary: (a) 20 GHz optimum power bias and tuning; (b) 20 GHz optimum efficiency bias and tuning; (c) 21 GHz optimum power bias and tuning; (d) 21 GHz optimum efficiency bias and tuning.

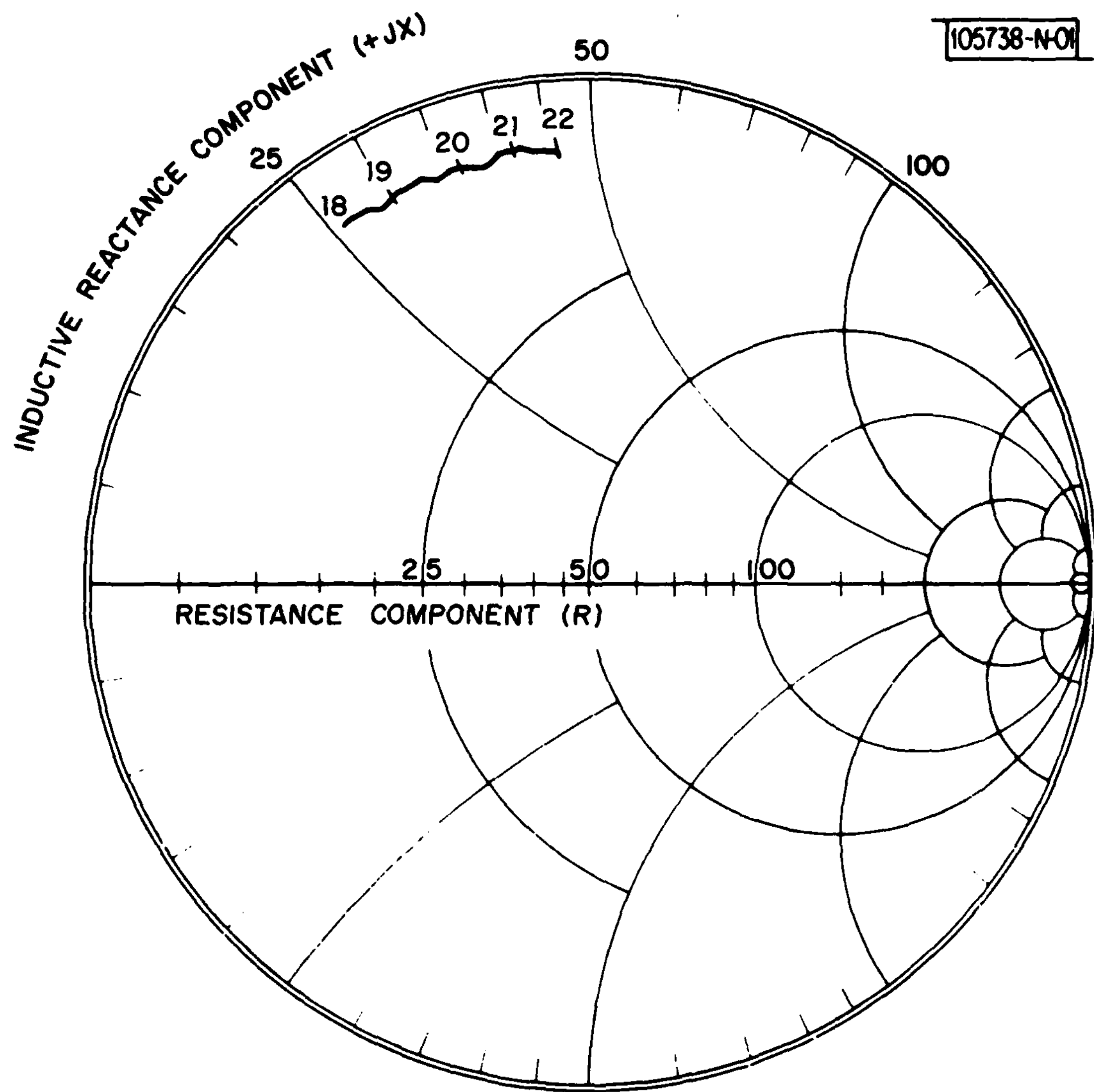


Fig. 14. 0.5 W power MESFET large-signal input impedance.

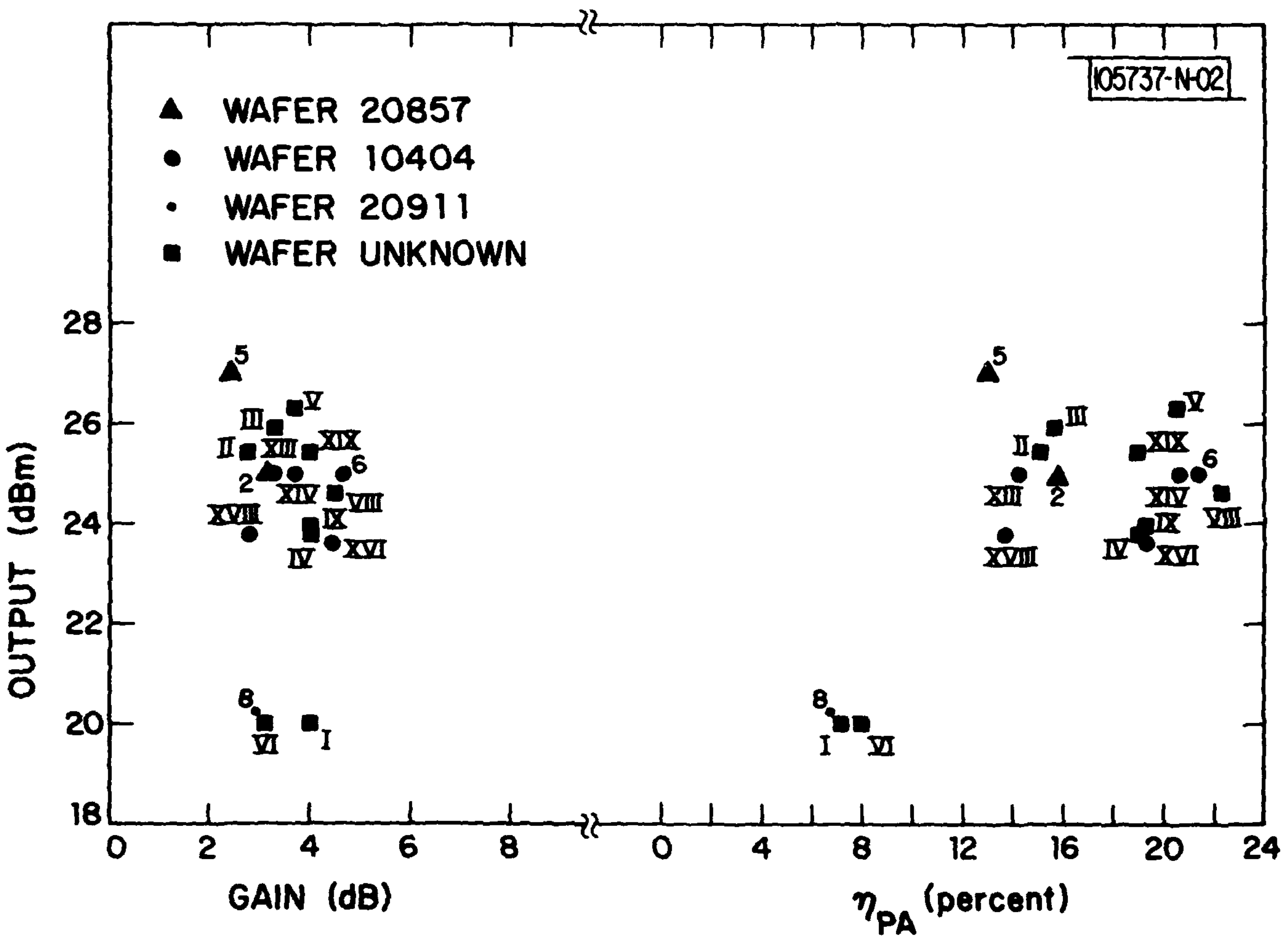


Fig. 15. Survey of GaAs FET tuned amplifier performance at 21 GHz.

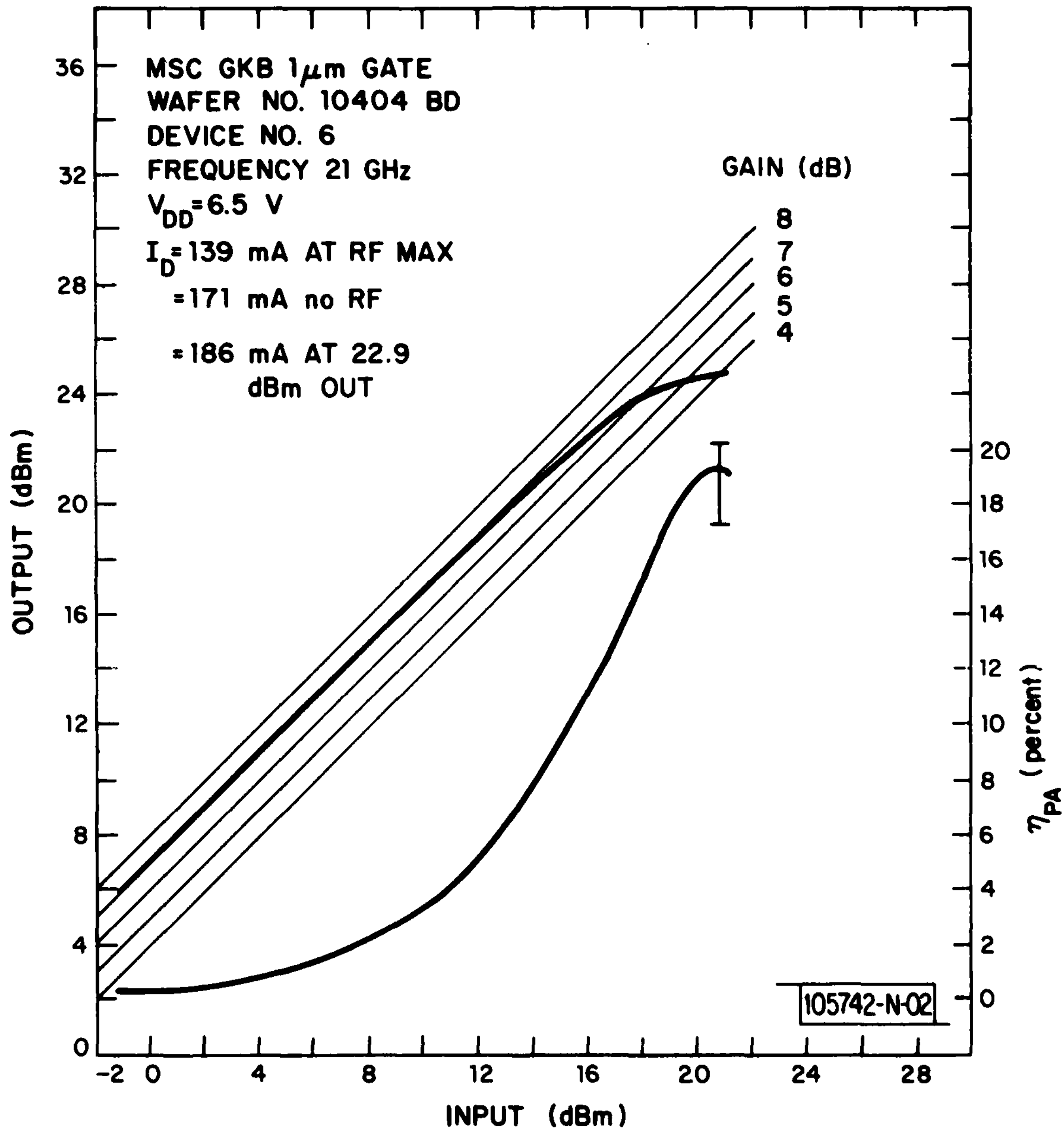


Fig. 16. Typical performance vs RF drive level.

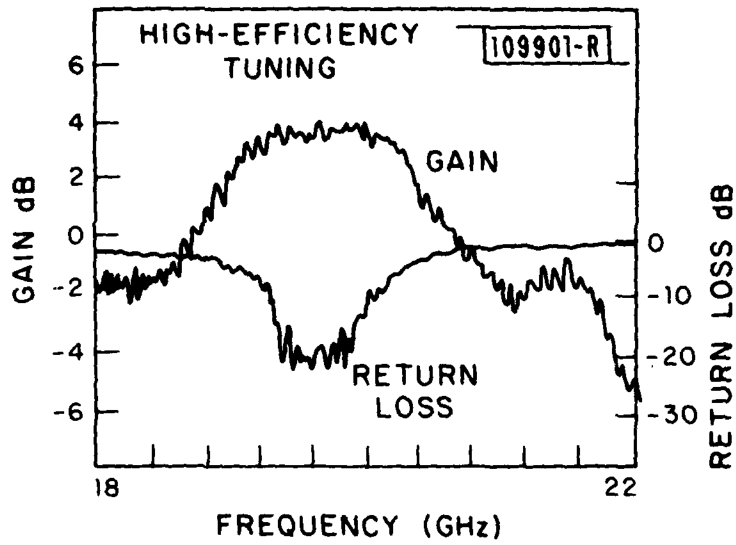
Slabline matching circuits were fabricated for one device, and a comparison between load-pull performance and measured amplifier performance at 20 GHz is given in Table II.

TABLE II

COMPARISON BETWEEN LOAD-PULL PREDICTIONS AND AMPLIFIER PERFORMANCE AT 20 GHz.

CONFIGURATION	BIAS	OUTPUT POWER	GAIN	EFFICIENCY
Loadpull Predictions	Power	530 mW	3.0 dB	21.7%
	Efficiency	350 mW	4.0 dB	25.6%
Amplifier	Power	377 mW	3.0 dB	19.5%
	Efficiency	267 mW	3.4 dB	24.8%
Amplifier With Additional Slug Tuning	Power	453 mW	3.0 dB	20.0%
	Efficiency	290 mW	3.4 dB	25.6%

Optimization of the input and output matches was achieved by the addition of slabline tuning slugs. Figure 17 shows the swept gain and return loss of the amplifier with slug-tuning assistance. The large signal gain is essentially flat from 19.2 to 20.2 GHz.



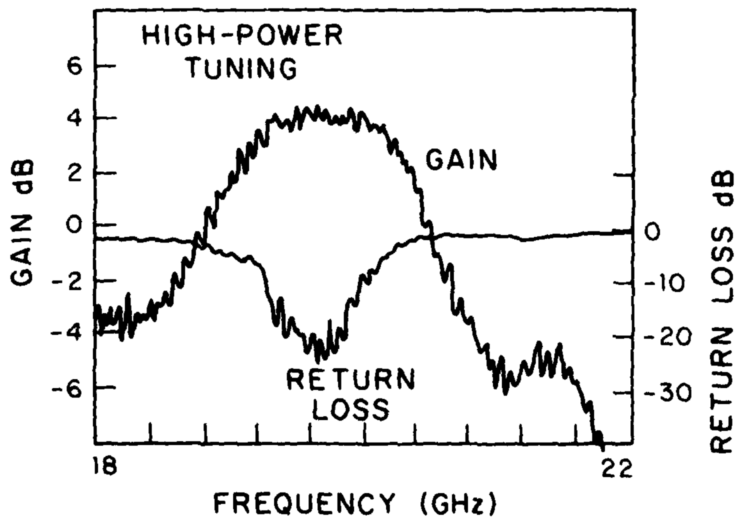


Fig. 17. Swept response of 20 GHz FET amplifier.

VI. CONCLUSION

This report describes the progress in the development of components for a 21 GHz solid-state satellite transmitter. The techniques for characterizing state-of-the-art GaAs FETs at 21 GHz have been discussed as well as the performance milestones which have been achieved. The measurements which have been presented show that potential GaAs FET performance at 21 GHz is considerably better than what has been achieved in amplifier circuits using more conventional characterization techniques. Perhaps the real potential of state-of-the-art GaAs FETs will not be realized until low-loss internal matching techniques are realized.

ACKNOWLEDGMENTS

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This report describes the development of GaAs MESFET power amplifiers at 21 GHz. Techniques for making large-signal loadpull and "S" parameter measurements at these frequencies, and the measured device characteristics are presented. A unique method of obtaining accurate gain and power measurements is discussed. Design methods and data are presented on 21 GHz amplifiers with more CW power and higher efficiency than previously achieved.

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