HARDWARE AND SOFTWARE IMPROVEMENTS TO A PACED DATA ACQUISITION -- etc(U)

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THESIS

HARDWARE AND SOFTWARE IMPROVEMENTS TO A PACED DATA ACQUISITION SYSTEM FOR TURBOMACHINES

by

Patrick Anthony McCarville

June 1981

Thesis Advisor: R. P. Shreeve

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Hardware and Software Improvements to a Paced Data Acquisition System for Turbomachines.

Modification of the phase lock loop synchronizing circuits and of the method of input/output communication used in a synchronized data sampling system, are reported. A device known as PACER which used an analog phase lock loop for synchronization and produced a non linear set of synchronizing pulses, was modified to use a CMOS digital phase lock loop, resulting in a linear set of pulses. The associated programming which controlled the data
acquisition process and sequencing, was changed to use the direct memory access feature of the system computer. This enabled data, from high response pressure transducers mounted in a turbomachine, to be taken once every rotor revolution rather than once every ten revolutions. A user's manual for paced data acquisition is included.
Hardware and Software Improvements
to a Paced Data Acquisition System
for Turbomachines

by

Patrick Anthony McCarville
Lieutenant Commander, United States Navy
B.S., University of New Mexico, 1972

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Author

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ABSTRACT

Modification of the phase lock loop synchronizing circuits and of the method of input/output communication used in a synchronized data sampling system, are reported. A device known as PACER which used an analog phase lock loop for synchronization and produced a non linear set of synchronizing pulses, was modified to use a CMOS digital phase lock loop, resulting in a linear set of pulses. The associated programming which controlled the data acquisition process and sequencing, was changed to use the direct memory access feature of the system computer. This enabled data, from high response pressure transducers mounted in a turbomachine, to be taken once every rotor revolution rather than once every ten revolutions. A user's manual for paced data acquisition is included.
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LIST OF SYMBOLS AND ABBREVIATIONS

SYMBOLS
A  Driver Amplifier
B  4-Bit binary counter
C  Comparator
F  Buffer Amplifier
U  AND gate
L  Latching Flip Flop
D  Delay Flip Flop
I  Inverter
178  PACER I/O controller port
118  A/D I/O controller port

ABBREVIATIONS
A/D  Analog-to-Digital
I/O  Input-Output
RTE  Real-Time Executive
1/Rev  Once per Revolution
1/BL  Once per Blade Passage
PLL  Phase Lock Loop
CMOS  Complementary Metal Oxide Semiconductor
TTL  Transistor-Transistor Logic
DMA  Direct Memory Access
DCPC  Dual Channel Port Controller
TP  Test Point
ACKNOWLEDGEMENT

To my thesis advisor, Dr. Raymond P. Shreeve, goes my sincere appreciation for his steadfast moral and technical support. Without his timely and intuitive guidance, this project would not have culminated in the results reported herein.

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Finally, to Mr. Alan McGuire goes my gratitude for his most professional work in the drawings and figures completed for this report.
I. INTRODUCTION

The device described herein and referred to as the "PACER" is part of a computer controlled data acquisition system in use at the Turbopropulsion Laboratory at the U.S. Naval Postgraduate School. It is an electronic interface unit built of solid state and integrated circuit components. The PACER was designed to allow the acquisition of data from high response transducers mounted in the case of rotating machines to be synchronized with respect to rotor position. Using the PACER, the analog to digital conversion of the data from a particular transducer can be programmed to occur at any position of the rotor with respect to the transducer, independent of rotor speed.

The PACER was first designed and built in a "bread board" configuration in 1976 by James C. West as described in Reference (1). U.S. patent no. 4,181,962 was issued for the PACER on January 1, 1980. The present hardware configuration of PACER involves minor but important changes which improve its performance and are documented in this report.

The original PACER made it difficult for the typical user to acquire accurate data in a reasonable amount of time for the following three reasons:

(1) The timing pulses generated within PACER were not always spaced linearly in time between blade pair
synchronizing pulses. This resulted in data which in some cases was subtly distorted, and in other cases appeared to have noise riding on it.

(2) The range over which the PACER could follow rotor RPM changes and remain synchronized was limited to approximately $\pm 15\%$ of the initial RPM at which the PACER was set to take the data. This required repeated, and somewhat involved, manual adjustment of an RPM "lock-on" procedure to acquire data at different speeds.

(3) The rate at which data could be taken was limited below the desired rate. This meant that rather than being able to sample data on every revolution of the rotor, the system was only capable of taking data once every 8 to 10 revolutions, depending on RPM.

The methods used to improve the performance of the PACER fall into two areas, hardware and software. Hardware changes were used to improve PACER linearity, eliminate manual lock-on procedures, and increase speed-following range. A change in acquisition software was used to increase the rate at which data could be taken.

The change in PACER hardware consisted of replacing the original analog 562 phase lock loop with a CMOS digital phase lock loop and eliminating the discrete components forming the coupling circuit in the PLL feedback path. The change to acquisition software involved use of the DMA (direct memory
access) feature of RTE-IVB system software [Ref. 2] which is incorporated in the I/O driver written for the PACER.

As a result of the hardware and software changes which were made, all of the limitations described above were eliminated. The improvement in PACER performance was verified using test programs and rotating machine signal simulation circuits which enabled controlled test techniques to be employed.

In the following section of this report a description of the entire paced data acquisition system is given. Section III describes the changes made to PACER hardware and the effects of those changes, while Section IV describes the change to acquisition software. In Section V the results of the changes are verified with a report of the system tests. Section VI lists conclusions and recommendations for further system development. Appendix A contains detailed hardware circuit design figures and Appendix B details the software programs - both acquisition FORTRAN and system assembly language drivers. Finally Appendix C is a step by step system users manual for paced data acquisition.
II. PACED DATA ACQUISITION SYSTEM DESCRIPTION

A. GENERAL DESCRIPTION

Components of the system are shown schematically in Figure 1 and details of the circuits, including the modifications made in the present work are shown in Figures 2-4. The PACER acts as a secondary controller on the interface between the Hewlett-Packard HP 21-MX computer and the A/D converter. Referring to Fig. 1, in a normal (not paced) data taking sequence, the 21MX would call on the A/D converter to take an analog data sample, convert it to digital, and output it to the computer memory. Since the computer program execution cannot be synchronized to the rotation of the machine shaft, the data sample would be from a random, unidentified point.

In a paced data acquisition sequence, the PACER provides the timing control to the 21MX computer. After the 21 MX computer passes a word (IBLADE) to the PACER defining the desired position, the PACER acts as an intermediary. It intercepts the computer command to the A/D converter, tells the computer that the A/D converter is in the process of acquiring the data, then sends a command pulse to the A/D converter at a time synchronized to the desired position in the cycle of the rotation of the machine.
The sequence of events for paced data acquisition using the software developed in the present work is as follows:

(1) The user enters the main program (which was written to be used for system testing or for data acquisition).

(2) The main program prompts the user for information regarding the (rotor) position(s) desired at which to start taking data points. This information defines the integer IBLADE.

(3) The main program calls the PACER, passes IBLADE to the PACER, and receives rotation speed (1RPM) from the PACER. Control then returns to the main program.

(4) The main program calls the A/D converter telling it to take a number of data samples (N) (at the desired point). When complete, control is returned to the main program.

(5) If a survey of positions (for example, across a pair of blade passages) has been programmed using a DO loop, the main program repeats steps (2) and (3), incrementing IBLADE each time until the loop is finished.

(6) When all data have been taken and stored in the computer memory, the main program converts the digital data (which are binary whole numbers) to decimal values scaled appropriately to the \( \pm 1.0 \) volt range of the A/D converter. As programmed, it then outputs that data to the desired peripheral(s) (i.e. the printer, plotter, or terminal).
B. SYSTEM SOFTWARE

The software used in the data acquisition should be viewed as consisting of two separate parts, the RTE-IVB operating system which is generated in-house following standard procedures supplied by Hewlett-Packard, and the system test and operation FORTRAN program which may be modified at any time by the user operating in the RTE-IVB system.

1. RTE-IVB Operating System

The RTE-IVB (Software) Operating System is generated (and can be regenerated) by the System Manager in a process which "configures" the System for the particular set of (I/O) devices which the computer must address [Ref. 3]. RTE-IVB permanently resides on disc and is automatically loaded when the system is turned on. It consists of a collection of software modules which perform system resource management, operator requests for utility programs (FORTRAN compiler, file editor, etc.), and user program scheduling for time sharing [Ref. 4]. RTE-IVB is visible to the user through interaction at the terminal. It allows multi-programming through its scheduling modules so that more than one user's program may be active at a time. The input/output (I/O) drivers are a set of modules in the RTE-IVB System. They are the software routines which control the input and output communication between the user's program and addressed peripheral devices. The drivers enable efficient use of peripherals which act at different speeds by allowing one or more fast I/O requests to be
processed while waiting for a request from a slow peripheral device to be completed. A driver written for the PACER (DVR.70) and a driver written for the A/D converter (DVR.56) are part of RTE-IVB and are listed in Appendix B.

2. System Test and Operation Program

The system test and operation program (A2D) is a FORTRAN program written and used in the course of the present work. A listing and flow diagram are given in Appendix B. Program A2D converts the user's requests, which are entered at the terminal, to the parameters required by the RTE-IVB I/O drivers. It is an interactive program consisting of two parts. The first part, a system test (subroutine ADTES), is entered if the user wants to carry out a test of the paced data acquisition system simply to ensure that all components are operating correctly. The second part, (Subroutine RPACE), is executed if paced data is to be acquired from a test rig. Both the "test" and "operation" portions of A2D use the FORTRAN statement "CALL EXEC" to enter the appropriate driver. The CALL EXEC statement, with its accompanying parameters, transfers control from the FORTRAN program to the assembly language driver for the device requested. A simplified flow diagram of the CALL EXEC routine is shown in Figure 5. The driver initiates the input or output task as specified in the parameters which it received. If the task is for "output", after the task is initiated control may return to the calling FORTRAN program or another user's program. If the task
requires "input", then control may be passed to another pro-
gram, but not back to the calling program, since the calling
program must have an input value to continue executing. This
permits efficient use of the computer's time, which is essen-
tial for multi-programming, while waiting for a slow peripheral
device to complete its cycle of operation.

C. SYSTEM HARDWARE

The hardware devices used in paced data acquisition are
the HP-21MX computer with printer, its magnetic disc, plotter,
and terminal, the HP 5610A A/D converter and the PACER.

1. Hewlett Packard HP 21 MX Computer

The HP 21 MX is a (Micro-programmable) mini-computer
having 128 machine instructions and 32K of logical main frame
memory. In the present configuration a 20 megabyte capacity
disc and disc operating system are an integral part of the
system. A detailed description of the computer is given in
Reference 2.

An important feature which is typical of computers of
this size is the input-output structure. With a limited
number of relatively slow I/O devices to be serviced, the
computer can communicate with all devices through a single
port known as the I/O bus. Each device requires its own
I/O interface on the bus. The interface acts as a filter and
ensures that output information is received only by the device
designated to receive it and that input information is put
on the bus from only one device at a time. The I/O software
drivers control the I/O hardware interfaces by commands to
either "turn-on" or "turn-off".

2. **Hewlett Packard HP 5610A A/D Converter**

   The HP 5610A analog-to-digital converter accepts
analog data input on up to sixteen different channels and
under computer controlled multiplexing converts to a 10 bit
binary data output. With an input conversion aperture of
50 nanoseconds, rapidly changing signals (100 KHz) can be
converted accurately. The HP 5610A can operate in one of
six modes as described in Reference 5. Currently the paced
data acquisition system uses the "random access mode" in
which a specific channel is sampled on receipt of a command
word and an encode command pulse from the 21 MX computer.
The command word tells the A/D converter which mode of opera-
tion to use and which channel number to sample. The encode
command pulse triggers the data conversion to start 2 μsec
later. The data conversion itself is finished in a total
time of 10 μsec. Using computer-issued encodes, which is
the mode required for paced data, the sample cycle time is
20 μsec. Hence data can be converted at rates of up to
50,000 samples per seconds, depending on how rapidly each
successive command word is received.

   The other mode which is used only for non-paced data
is the Free Run, Random Access mode. In this mode the com-
mand word is required as before, but no encode command is
needed from the computer. The A/D converter simply converts data as fast as it can (100,000 samples per second) on the selected channel. This mode is not addressed further in this report.

3. PACER

A schematic of the PACER is shown in Figure 2. In its original form, a detailed description of the internal operation is given in Ref. 1. The PACER consists of two major sections, an "RPM counting section" and a "synchronized command pulse section". The "RPM counting section" continuously counts the number of 250 KHz time base pulses that occur between the once-per-revolution pulses received from the test rig. This number of counts is available as an output (IRPM) from the PACER on every revolution cycle.

The "synchronized command pulse" section is the heart of the PACER. It uses a phase lock loop to generate 256 pulses within each pair of blade passages (i.e. 128 pulses from blade #1 to blade #2 and 128 pulses from blade #2 to blade #3). At the same time, these pulses are counted and compared with the programmed data conversion location specified in IBLADE. When the comparison is true, a command to the A/D converter (A/D Device Command) is generated. Thus a command to convert a data sample is synchronized with a desired position of the rotation rotor in the machine.
III. CHANGES TO PACER HARDWARE

In order to determine the cause of the non-linearity in the PACER, a test chassis was built to provide easy access to the four circuit boards and to allow modifications to be attempted without interference to the working unit. The test chassis is shown in Figure 6. It is electrically identical to the system PACER shown in Figure 7 and uses the same four circuit boards. Using the test PACER with an oscilloscope it was possible to examine the wave forms, at any point in the PACER circuit. In so doing, it was found that even with the lock-on procedure recommended in Reference 1, the output pulses from the PLL (256·Fo/2) were not always linearly spaced between the beginning and end of the input pulses (Fo/2). This non-linearity is seen in the oscilloscope traces shown in Figure 8, which shows the signal at counter Bl. At counter Bl the pulse frequency is 1/32 of the output frequency of the PLL which allows the non-linearity to be obvious to the eye. It was further noted that a deviation of as little as 3° from the ideal 270° phase relation called for in Reference 1, caused non-linear spacing and excessive unsteadiness ('jitter') of the pulses into counter Bl. These problems were inherent in the 562N PLL when used with digital waveforms because an analog phase comparator was used in that particular circuit [Ref. 6].
A CD4046 (CMOS) PLL was therefore chosen to replace the 562N. The CD4046 uses a digital phase comparator to maintain lock [Ref. 7] and is specifically designed to operate with digital waveform inputs as are found in the PACER application. It also permits, with proper associated component design, operation over an extremely wide frequency range (by so-called frequency tracking) without loosing lock.

The changes which were made in the PLL and associated circuitry are shown in Figure 3. Both the PLL and the discrete component coupling circuits were changed. The replacement of the old coupling circuits with CMOS-to-TTL (4050B Buffer) and TTL-to-CMOS (7417 Drivers with pull-up resistors) matching devices was necessary because of the special requirements of the CMOS PLL with regard to interfacing [Ref. 7]. The detailed circuitry of the CD4046 (CMOS) PLL is shown in Figure 4. Specific details of the components are given in Appendix A.
IV. CHANGE TO ACQUISITION SOFTWARE

A. METHODS OF INPUT/OUTPUT

The two methods available under RTE-IVB for input and output are the "standard" method and Direct Memory Access (DMA). In both methods the software driver controls the initiation and completion of the I/O request. Figure 9 is a schematic representation of the hardware and software involved in an I/O request in the paced data acquisition process. The standard I/O method requires that the software driver be entered for each data sample taken. In contrast, the DMA I/O method uses the "dual channel port controller" option of the 21 MX computer to bypass the requirement to return to the driver for each new data sample [Ref. 2]. Thus by using DMA, the time involved in executing the software driver for each sample is saved.

B. INCORPORATION OF DMA

The system software was changed so that DMA was used for the A/D I/O process. The DCPC option was added to the system in 1977. The driver DVR56 was subsequently modified by Hewlett Packard to permit DMA for I/O operation with the A/D converter. The use of the DMA feature required only that the proper parameters be specified in the CALL EXEC statement for the A/D converter. Table I lists the parameters,
with their meanings, for the CALL EXEC statements used to call the A/D converter and the PACER through the drivers DVR56 and DVR70 respectively. The parameter "N", which is passed in the call to driver DVR56, sets up the DMA option in the 21 MX I/O interface logic through the Dual Channel Port Controller (DCPC). The program A2D was written so as to use the DMA feature. A flow chart, listings, and parameters used in program A2D and the drivers DVR56 and DVR70 are given in Appendix B.
V. RESULTS

Tests were run to verify the linearity of the new CMOS PLL circuitry, to demonstrate the automatic lock on feature, and to determine the speed at which data was acquired. The tests were run using the test pulse generation circuit on circuit board #4 of the PACER. This circuit provides an electronically produced simulation of the 1/Rev and 1/Blade pulses that would ordinarily be received from the test rig. The test set up for the tests is shown in Figure 10. An external signal generator was used to provide the driving signal to the pulse generating circuit at the desired blade passing frequency. Appendix C gives detailed procedures for performing a simulation test run.

A. LINEARITY TEST

Figure 8 shows a comparison of PLL output pulses from the 562N PLL and the new CMOS digital PLL circuits. It can be seen that the new circuitry produces symmetric and evenly spaced pulses while the old PLL circuit does not.

A linear ramp test signal was input to the A/D converter on analog channel 0. The PACER test portion of program A2D was run calling for a survey across the simulated blade pair. The test was repeated for the old and new PLL circuits. Figures 11 and 12 show the output results from the PACER
using the old and new PLL circuits respectively. The apparent "bending" of the ramp test signal when seen as the graphed output from the old PLL method is due to the inherent non-linearity of the 562N PLL. The strict linearity of the CMOS digital PLL circuit was noted.

B. AUTO LOCK-ON TEST

The new CMOS digital PLL requires no lock-on procedures as did the 562N PLL [Ref. 1]. Tests were run to confirm that while varying the blade passing frequency, the new PLL remained in a locked-on condition. It was shown that within the design range of the PLL circuitry, any variation of blade passing frequency (RPM) was followed without error by the digital phase lock loop. Two separate PLL circuits were designed, each one covering a range of blade passing frequencies. One PLL circuit now covers the range from 250 Hz to 2.5 KHz. The other covers the higher range from 3 KHz to 11.1 KHz. The reasons for this division are explained in Appendix A.

C. TEST OF ACQUISITION TIME

Using the software methods used in Reference 1, a short test program calling for a specified number of data samples to be taken, was run. Clock time accurate to .1 millisec was recorded by the program just before the first sample and just after the last sample of data was acquired. The lapsed time for the total acquisition was output. It was shown that up to 10 revolutions of the machine rotor where required for each data sample to be taken.
After changing to the DMA software method described in section IV, similar tests were run. The results of these tests are shown in Table II. It was noted that the interval between samples was reduced to less than one revolution of the machine rotor.
VI. CONCLUSIONS AND RECOMMENDATIONS

The desired improvements in the paced data acquisition system were achieved; namely,

(1) The speed of acquisition of successive data samples was increased to enable data to be sampled on every revolution.

(2) The correlation between the position recorded for a paced data sample and the physical position of the probe with respect to the rotor at acquisition, was significantly improved through an improvement in the linearity and stability of the PLL and associated circuitry.

(3) The manual adjustments previously required for each small range of RPM were entirely eliminated by the reported hardware modifications.

With the present hardware and software the PACER operates as fast as is possible given the constraint that the 21 MX computer operates always in the interrupt mode for all I/O operations. If the need arises to survey across a blade pair on one resolution and the computer can be dedicated to the single task of acquiring paced data, then the non-interrupt mode of 21 MX I/O processing could be used. This change would eliminate other users during the paced data program operation. It would require that the drivers DVR56 and DVR70
to be rewritten in assembly language and loaded into the RTE-IVB operating system by the system manager. It is noted however that the maximum data rate of 100,000 samples per sec cannot be exceeded using the present A/D converter.
Table I. CALL EXEC Parameters

To call the PACER (DVR70)

CALL EXEC (1, LU, IRPM, LEN, IBLADE)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Meaning</th>
<th>Limits/Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I/O</td>
<td>1</td>
</tr>
<tr>
<td>LU</td>
<td>device reference number</td>
<td>19</td>
</tr>
<tr>
<td>IRPM</td>
<td>RPM timing counts returned</td>
<td>N/A</td>
</tr>
<tr>
<td>LEN</td>
<td>number IRPM of words passed</td>
<td>0, 1</td>
</tr>
<tr>
<td>IBLADE</td>
<td>data position indicator</td>
<td>0-35,584</td>
</tr>
</tbody>
</table>

To clear the PACER

CALL EXEC (3, LU)

<table>
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<tr>
<th>Parameter</th>
<th>Meaning</th>
<th>Limits/Value</th>
</tr>
</thead>
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<tr>
<td>3</td>
<td>clear the device as above</td>
<td>3, 19</td>
</tr>
<tr>
<td>LU</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

To call the A/D (DVR56)

CALL EXEC (1, IDRT, IBUF, N, ICHAN, ICODE)

<table>
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<th>Meaning</th>
<th>Limits/Value</th>
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<tr>
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<td>I/O</td>
<td>1</td>
</tr>
<tr>
<td>IDRT</td>
<td>device reference number</td>
<td>20</td>
</tr>
<tr>
<td>IBUFF</td>
<td>data storage array name</td>
<td>dimension 256</td>
</tr>
<tr>
<td>N</td>
<td>number of samples</td>
<td>1-99</td>
</tr>
<tr>
<td>ICHAN</td>
<td>input channel number</td>
<td>0-15</td>
</tr>
<tr>
<td>ICODE</td>
<td>mode of A/D operation</td>
<td>0-7</td>
</tr>
</tbody>
</table>
Table II. Data Acquisition Times

<table>
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<tr>
<th>Run</th>
<th>Number Samples</th>
<th>RPM</th>
<th>Time</th>
<th>Time/Rev</th>
<th>Time/Sample</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Before DMA</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>100</td>
<td>17,300</td>
<td>1.61</td>
<td>.0035 sec.</td>
<td>.0161 sec.</td>
</tr>
<tr>
<td>2</td>
<td>100</td>
<td>17,400</td>
<td>1.60</td>
<td>.0032 &quot;</td>
<td>.016 &quot;</td>
</tr>
<tr>
<td>3</td>
<td>20</td>
<td>7,500</td>
<td>.51</td>
<td>.008 &quot;</td>
<td>.025 &quot;</td>
</tr>
<tr>
<td>4</td>
<td>20</td>
<td>8,000</td>
<td>.45</td>
<td>.0075 &quot;</td>
<td>.0225 &quot;</td>
</tr>
<tr>
<td>5</td>
<td>500</td>
<td>30,000</td>
<td>9.51</td>
<td>.002 &quot;</td>
<td>.019 &quot;</td>
</tr>
<tr>
<td>6</td>
<td>500</td>
<td>29,900</td>
<td>9.50</td>
<td>.002 &quot;</td>
<td>.019 &quot;</td>
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<tr>
<td><strong>After DMA</strong></td>
<td></td>
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<td>1</td>
<td>100</td>
<td>15,100</td>
<td>.398</td>
<td>.00397</td>
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<td>.004</td>
<td>.004</td>
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<tr>
<td>3</td>
<td>100</td>
<td>8,000</td>
<td>.750</td>
<td>.0075</td>
<td>.0075</td>
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<td>4</td>
<td>100</td>
<td>30,000</td>
<td>.200</td>
<td>.002</td>
<td>.002</td>
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Table III. Components Used in PACER

<table>
<thead>
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<th>COMPONENT</th>
<th>SCHEMATIC NUMBER</th>
<th>VALUE OR TYPE NO.</th>
<th>High Board</th>
<th>Low Board</th>
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<tr>
<td>R1</td>
<td></td>
<td>10 KΩ</td>
<td>4.7 KΩ</td>
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<tr>
<td>R2</td>
<td></td>
<td>100 KΩ</td>
<td>100 KΩ</td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td></td>
<td>1 MΩ</td>
<td>1 MΩ</td>
<td></td>
</tr>
<tr>
<td>R4</td>
<td></td>
<td>39 KΩ</td>
<td>47 KΩ</td>
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<td>12 KΩ</td>
<td>12 KΩ</td>
<td></td>
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<tr>
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<td></td>
<td>10 KΩ</td>
<td>12 KΩ</td>
<td></td>
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<td>C1</td>
<td></td>
<td>50 pf</td>
<td>.001 μf</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td></td>
<td>1.5 μf</td>
<td>1.5 μf</td>
<td></td>
</tr>
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<td><strong>Counter</strong></td>
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<td>Bl thru B10</td>
<td></td>
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<td>74193</td>
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<tr>
<td><strong>Latch</strong></td>
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<td>Cl thru C4</td>
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<td>9324</td>
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<td>Ul thru U3</td>
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<td>I1, I2</td>
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<td>Fl thru F5</td>
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<td>N4050B</td>
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<tr>
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<td>Al thru A4</td>
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<td>7417N</td>
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<td>PLL</td>
<td></td>
<td>CD4046</td>
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</table>
Figure 1. Paced Data Acquisition System Components
Figure 3. Original and Revised PACER Circuits
Figure 4. CD4046 PLL Circuit Detail
Figure 5. EXEC CALL Flow Diagram
Figure 6. PACER Test Chassis
Figure 8. Pulse Trains at Counter B1 for Analog & Digital PLL Circuits
Figure 9. Paced I/O Request Flow Diagram
Figure 11. Ramp Test Data from Original PACER
APPENDIX A
HARDWARE DESIGN DETAILS

A.1 INTRODUCTION

The PLL circuit is shown in detail in Figure 4. A listing of component values is found in Table III.

Two separate PLL circuits were designed and incorporated into the hardware; one for each of two frequency ranges. This was done in order to cover a very large total frequency range while maintaining fast response to changes in frequency [Ref. 7]. In the following sections the design procedure which was followed is documented.

A.2 DIGITAL PHASE LOCK LOOP (CMOS) DESIGN

The CD4046 digital PLL requires four areas of external design [Ref. 7].

(1) Selecting the timing capacitor $C_1$ which determines the center of the operating frequency range.

(2) Selecting the values of $R_2$ and ratio of $R_1$ to $R_2$ which determine the upper and lower bounds of the lock range.

(3) Selecting the ratios of $R_3$ to $R_4$, $R_3$ to $C_2$, and their values, which contribute to determine the damping ratio and settling time of the second order feedback loop.
(4) Interfacing the CMOS integrated circuit design with the TTL integrated circuits already in the PACER.

These areas are detailed in the following sections.

A.2.1 Timing Capacitor

In the following discussion, figures and pages are quoted with respect to Reference 8, the main source for design information. To begin the design a value of R2 was chosen within the limits listed on page 228 of Ref. 8. The value of C1 was approximated using figure 5(b) of Ref. 8. The value was then readjusted after testing to compensate for the effects of the following component values.

A.2.2 R1/R2

The chosen frequency range (fmax/fmin) was used to enter figure (c) of Ref. 8. The ratio R1/R2 was obtained from the data in that figure using the design value of the supply voltage to the PLL. Knowing the ratio R1/R2 and the value of R2 selected in section A.2.1, the value of R1 was obtained.

A.2.3 R3/R4/C2

The design of the loop low-pass filter was a trial and error iterative process because of effects from the counting circuits Bl and B2 present in the loop [Ref. 7]. The RC time constant of R3 and C2 determined the settling time of the loop while the ratio of R3 to R4 determined the damping ratio.
The nominal values found in Reference 7 were used initially and then these were adjusted to obtain what was considered to be the best loop response to changes in the input frequency. Loop response time was found by putting small but rapid perturbations on the test frequency, then noting the time to regain phase lock-on. By balancing the response time (required to be as fast as possible) against the settling time resulting from the loop damping ratio (at a minimum to maintain stability) across the frequency range, a satisfactory overall loop response was attained.

A.2.4 Interfacing

Due to the extremely high input and output impedances of CMOS integrated circuits, an interfacing buffer was needed between the CMOS PLL output from pin 3 and the TTL counter (B1) input to pin 5 (Fig. 2). Also, interface drivers were needed between the outputs of TTL counters B10 and B2 and the inputs to the CMOS PLL at pins 14 and 3, respectively.

The buffer between PLL pin 4 and counter B1 pin 5 simply required wiring one of the unused buffers which were part of the N4050B Hex buffer chip already in the PACER. Since the N4050B used a +5 VDC supply, the required transition from PLL +15V logic level to the counter +5v logic level was made.

In order to transition from the TTL (+5v) logic level of counters B10 and B2 outputs to the required PLL input levels (greater than +7v for logic 1), two 7417N TTL drivers
were used with 12 kΩ "pull up" resistors on their outputs. This gave a high logic level of +15v and a low state current drain on the drivers of only 1.25 ma each, well within their fan out capability [Ref. 9].
APPENDIX B
SOFTWARE DETAILS

This Appendix contains the following materials:

B.1 ACQUISITION FORTRAN PROGRAM A2D [Ref. 10]
   B.1.1 Program A2D Flow Chart
   B.1.2 Program A2D Listing
   B.1.3 Program A2D Parameter Listing

B.2 SOFTWARE DRIVERS [Ref. 11, See Note 1]
   B.2.1 Flow Chart
   B.2.2 Pacer Driver DVR 70
   B.2.3 A/D Driver DVR 56

Notes on Software Drivers


2. The driver flow chart in B.2.1 is a simplified diagram which shows the basic process for a typical driver. DVR 70 contains a series of steps which pass IBLADE (output) and a section which receives IRPM (inputs). The initiator section first outputs IBLADE to the PACER. After that, control is returned to the Central Interrupt Controller to await the PACER interrupt signal indicating it has IRPM ready to output. When the interrupt occurs, the completion section of DVR 70 is entered and IRPM is passed.
DVR 56, on the other hand, has only the input function to complete. It accomplishes this task as the standard driver indicated in the flow chart B.2.1. The beginning of DVR 56 configures the DMA feature of the RTE-IVB [Ref. 2].

B.1 ACQUISITION FORTRAN PROGRAM A2D

(See following pages).
B.1.1 Program A2D Flowchart

START

TEST OR DATA

TEST

PROMPT USER FOR PARAMETERS

ADTES

DATA

EQUIP SET

AGAIN?

STOP

ADTES

ENTER BLADE PAIR TO SURVEY

N

EQUIP SET?

Y

ACQUIRE TEST DATA AT EACH POSITION

N

CONVERT BINARY TO DECIMAL

Y

PLOT EACH DATA SAMPLE VS POSITION

RETURN

RPACE

SURVEY ACROSS BLADE

Y

TAKING DATA AT DESIRED POINT

N

TAKING DATA AT 256 POINTS ACROSS PAIR SELECTED

OUTPUT DATA

RETURN

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B.1.2 Program A2D Listing

PROGRAM A2D
C PACED DATA ACQUISITION
C OPERATION AND TEST PROGRAM
C P. A. MCCARVILLE APRIL 1981

COMMON IRPM
INTEGER CHANL, AVERG, SURVEY, MODE, PAIR, POSIT, OFFSET

WRITE (1, 95) * WILL THIS BE SYSTEM TEST OR DATA RUN? 1=DATA 0=TEST *
READ (1, *) ITEST
IF (ITEST EQ. 1) GO TO 96
CALL ADTES(IGCB)
CONTINUE
GO TO 999

96 WRITE (1, 97) ENTER TEST NUMBER *
READ (1, *) NC
99 WRITE (1, 100)
100 FORMAT (1, *) N1
IF (N1 LE. 1) GO TO 102
101 WRITE (1, 110)
110 FORMAT (1, *) CHNL, SURVEY, PAIR, POSIT, AVERG, OFFSET*
READ (1, *) CHNL, SURVEY, PAIR, POSIT, AVERG, OFFSET
GO TO 107

102 WRITE (1, 120)
120 FORMAT (1, *) CHNL, DATA CHANNEL. LIMITS 0-15*
READ (1, *) CHNL
103 WRITE (1, 130)
130 FORMAT (1, *) AVERG*
WRITE (1, 110)
110 FORMAT (1, *) SURVEY, PAIR, POSIT, AVERG, OFFSET*
READ (1, *) SURVEY, PAIR, POSIT, AVERG, OFFSET
GO TO 107

104 WRITE (1, 145)
145 FORMAT (1, *) WHICH BLADE PAIR DO YOU WISH TO SEE? LIMITS *
READ (1, *) PAIR
105 WRITE (1, 113)
113 FORMAT (1, *) WHICH POSITION BETWEEN BLADE PAIR? LIMITS *
READ (1, *) POSIT
MODE = 1
GO TO 107

104 WRITE (1, 145)
145 FORMAT (1, *) WHICH BLADE PAIR DO YOU WISH TO SEE? LIMITS *
READ (1, *) PAIR
WRITE (1, 115)
115 FORMAT (1, *) DO YOU WANT TO OFFSET THE SURVEY? 1=YES 0=NO *
READ (1, *) OFFSET
WRITE (1, 165)
165 FORMAT (1, *) DO YOU WANT TO OFFSET THE SURVEY? 1=YES 0=NO *
READ (1, *) OFFSET
WRITE (1, 166)
166 FORMAT (1, *) ENTER % OFFSET, WILL DELAY START % OF 256 *
READ (1, *) OFFSET
90 WRITE (1, 170)
170 FORMAT (1, *) IS A/D CONVERTER ON? IS TEST SET-UP READY? *
READ (1, *) NO
91 WRITE (1, 172)
172 CALL RPACE (CHNL, AVERG, SURVEY, MODE, PAIR, POSIT, OFFSET, N2)
92 WRITE (1, 177)
93 WRITE (1, *) N3
94 IF (N3 EQ. 1) GO TO 90
95 WRITE (6, 160)
SUBROUTINE RPACE (ICHAN, IAVG, ISURV, IMODE, IPAIR, CIPOSIT, IOFFS, N2)

DATA ACQUISITION SUBROUTINE

REAL SRVPT(99), ITIME(5)
N=IAVG
CALL EXEC (ITIME, IYEAR)
WRITEx(6,90)

FORMAT(/, 10X, "THIS IS TEST ", 12, " RUN ON JULIAN",
* " DATE ", 13, 3X, I4, ")
IF (ISURV . EQ. 0) GO TO 120

SINGLE POINT ACQUISITION

IF (IMODE . EQ. 0) GO TO 100

CALL EXEC (3,19)
CALL EXEC (1,19, IRPM, IBLADE)
CALL EXEC (1, 20, IDUFF, ICHAN, 0)
RBUFF = RBUFF + FLOAT(IBUFF(I))/32768.
DATA = RBUFF/IAVG
DO 130 J = 1, N
RBUFF = RBUFF + FLOAT(IUFF)/32768.
SRVPT(J) = DATA

SURVEY ACROSS BLADE PAIR ACQUISITION

DO 125 IOFFS = 1, 100/IOFFS

IDUFF = IDUFF + 1
CALL EXEC (3,19)
CALL EXEC (1,19, IRPM, IBLADE)
CALL EXEC (1, 20, IDUFF, N, ICHAN, 0)
RBUFF = 0
DO 130 K = 1, N
RBUFF = RBUFF + FLOAT(IUFF)/32768.
SRVPT(J) = DATA

OUTPUT TABLES/PRINT

WRITE (6,146)
WRITE (6,149)
WRITE (6,150)
WRITE (6,151)
WRITE (6,152)
WRITE (6,153)
WRITE (6,154)
WRITE (6,155)
WRITE (6,156)
WRITE (6,157)

120 IF (IOFFS . EQ. 0) GO TO 125
125 IF (IOFFS . EQ. 0) GO TO 127
DO 140 J = 1, 125

GO TO 195
127 IOFFS = 1
DO 140 J = 1, 125
IDUFF = IDUFF + 1
CALL EXEC (3,19)
CALL EXEC (1,19, IRPM, IBLADE)
CALL EXEC (1, 20, IDUFF, N, ICHAN, 0)
RBUFF = 0
DO 130 K = 1, N
RBUFF = RBUFF + FLOAT(IUFF)/32768.
DATA = RBUFF/IAVG
SRVPT(J) = DATA

GO TO 195

RETURN
END
SUBROUTINE ADTES(ICCB)

TEST OF THE PACED DATA ACQUISITION SYSTEM

COMMON IRPM
DIMENSION ICCB(192)
INTEGER TIME(5), NOCR(2), IVOLT(128)
REAL RVOLT(128)
DATA NOCR /0000339, 0404339/
DATA ICHAN /0/  
101 FORMAT(" THIS WILL TEST THE PACED DATA SYSTEM FOR ",  
" CONTINUITY AND LINEARITY. \(*/\), \(*/\) ENTER THE SIMULATED",  
" BLADE PAIR TO VIEW. LIMITS 1-8")
WRITE (1,101)
READ (1, *) IPAIR
100 WRITE (1,102)
102 FORMAT(" THE TEST SET UP READY AS PER MANUAL ?",  
" =YES 0=NO")
171 READ (1, *) N4
172 IF (N4 .EQ. 0) GO TO 100
173 IBLADE = 0
174 IBLADE = IBLADE+256*IPAIR
175 DO 129 I=1,129
176 IBLADE=IBLADE+1
177 CALL EXEC (3,19)
178 CALL EXEC (1,19 IRPM,1,IBLAD)
179 DO 129 CALL EXEC(1,19,IVOLT(I),1,ICHAN,0)
180 DO 45 JS=1,129
181 RVOLT(I)=FLOAT(IVOLT(I))/32768.
182 LU=13
183 ID=2
184 CALL PLOT(IGCB, ID, LU)
185 CALL LIMIT(IGCB, 0., 200., 0., 187.)
186 CALL SETAR(IGCB, 1.)
187 CALL VIEWP(IGCB, 0., 140., 20., 80.)
188 CALL WINDW(IGCB, 0., 120., 0., 1.)
189 CALL FXB(IGCB,1.)
190 CALL LIMIT(IGCB, -2., 0.5, 0., 0., 8., 5., 1.)
191 CALL MOVE(IGCB, 1., RVOLT(I))
192 ID=5
193 DO 55 K=2,129
194 EX=FLOAT(K)
195 CALL DRAW(IGCB, EX, RVOLT(K))
196 CALL VIEWP(IGCB, 0., 150., 0., 100.)
197 CALL WINDW(IGCB, 0., 150., 0., 100.)
198 CALL MOVE(IGCB, 64., 90.)
199 CALL CPLOT(IGCB, -10., 0., 0.)
200 CALL LABEL(IGCB)
201 WRITE(LU,160)
202 160 FORMAT(" PACED RAMP TEST DATA")
203 CALL PLOT(IGCB, ID, 0)
204 LU=160
205 RETURN
206 END
B.1.3 Program A2D Parameter Listing

CHANL/ICHAN  The A/D analog input channel to be sampled.
AVERG/IAVG   The number of samples per position to be averaged.
SURVEY/ISURV Survey/single position selection
MODE/IMODE   Paced/free run-normally 1
PAIR/IPAIR    The pair of passages selected
POSI/IPOSIT   The position within the pair of passages
OFFSET/IOFFS To start the survey later than position #1 within the pair passages. Entered as % of 256.
IRPM          See Table I
IBLADE        See Table I
IBUFF         The name of the set of digital data storage locations
N2            Test number that date
RBUFF         Floating point data storage
PTDATA/DATA   The data value at the selected point
SRVPT         The array holding the data surveyed
IGCB          Graphics control block, graphics package usage nonaccessible.
B.2.2 Pacer Driver DVR 70

PAGE 3002 NO 1

8139 AH FRIDAY 4 AUG. 1979

PACER DRIVER

AUTHOR: JIM HOBBS

REV. 7A024 JDM

FOAT 1,7A, C.7A, C.X1, I.XY

THIS PACE DRIVER WILL OUTPUT A BLADE NUMBER TO
THE PACE AND RETURN THE RPM VALUE.

CALLING SEQUENCE:

CALL EVENT(L, UL, IRP, LEN, 16, I, LANE) >>> NORMAL INPUT (READ)

CALL EVENT(3, UL) >>> CLEAR CONTROL ON PACER

CALL EVENT(L, UL, IRP, LEN, 16, I, LANE) >>> NORMAL INPUT (READ)

CALL EVENT(3, UL) >>> CLEAR CONTROL ON PACER

CALL EVENT(L, UL) >>> CLEAR CONTROL ON PACER

RETURN TO TOC

NOTES

1. CLEAR CONTROL AND NO SUBFUNCTION RMTS SET

2. CLEAR CONTROL RMTS SET

3. CLEAR CONTROL RMTS SET

4. CLEAR CONTROL RMTS SET

5. CLEAR CONTROL RMTS SET

6. CLEAR CONTROL RMTS SET

7. CLEAR CONTROL RMTS SET

8. CLEAR CONTROL RMTS SET

9. CLEAR CONTROL RMTS SET

10. CLEAR CONTROL RMTS SET

11. CLEAR CONTROL RMTS SET

12. CLEAR CONTROL RMTS SET

13. CLEAR CONTROL RMTS SET

14. CLEAR CONTROL RMTS SET

15. CLEAR CONTROL RMTS SET

16. CLEAR CONTROL RMTS SET

17. CLEAR CONTROL RMTS SET

18. CLEAR CONTROL RMTS SET

19. CLEAR CONTROL RMTS SET

20. CLEAR CONTROL RMTS SET

21. CLEAR CONTROL RMTS SET

22. CLEAR CONTROL RMTS SET

23. CLEAR CONTROL RMTS SET

24. CLEAR CONTROL RMTS SET

25. CLEAR CONTROL RMTS SET

26. CLEAR CONTROL RMTS SET

27. CLEAR CONTROL RMTS SET

28. CLEAR CONTROL RMTS SET

29. CLEAR CONTROL RMTS SET

30. CLEAR CONTROL RMTS SET

31. CLEAR CONTROL RMTS SET

32. CLEAR CONTROL RMTS SET

33. CLEAR CONTROL RMTS SET

34. CLEAR CONTROL RMTS SET

35. CLEAR CONTROL RMTS SET

36. CLEAR CONTROL RMTS SET

37. CLEAR CONTROL RMTS SET

38. CLEAR CONTROL RMTS SET

39. CLEAR CONTROL RMTS SET

40. CLEAR CONTROL RMTS SET

41. CLEAR CONTROL RMTS SET

42. CLEAR CONTROL RMTS SET

43. CLEAR CONTROL RMTS SET

44. CLEAR CONTROL RMTS SET

45. CLEAR CONTROL RMTS SET

46. CLEAR CONTROL RMTS SET

47. CLEAR CONTROL RMTS SET

48. CLEAR CONTROL RMTS SET

49. CLEAR CONTROL RMTS SET

50. CLEAR CONTROL RMTS SET

51. CLEAR CONTROL RMTS SET

52. CLEAR CONTROL RMTS SET

53. CLEAR CONTROL RMTS SET

54. CLEAR CONTROL RMTS SET

55. CLEAR CONTROL RMTS SET

THIS PAGE IS BEST QUALITY PRACTICABLE

Page 55
NORMAL RETURN TO INC NOW

TEVIT CLA JMP 1,70.I RETURN TO INC

CONTINUATION/COMPLETION SECTION

ENTER CONT' CHECK FOR SPURIOUS INTERRUPT
CONFIGURE I/O IS A REQUEST IN PROGRESS?

GET BLADE NUMBER

GET RPM FROM PACER

ENTRY TO SUBROUTINE

A35C OF I/O DEVICE, CHECK IF CONFIGURED
YFS, BYPASS CONFIGURATION

SAVE CURRENT I/O CHANNEL NUMBER
COMBINE LIA WITH I/O
START IT

MAKE OTA INSTRUCTION
START IT

MAKE OCR INSTRUCTION
START IT

RETURN FROM SUBROUTINE
CONSTANTS/STORAGE/LINKS

CURRENT I/O SELECT CODE VALUE
DUMMY SELECT CODE
INPUT FROM DEVICE INSTRUCTION
RETURN POINT IN INITIATION SECTION

DEFINE START OF COMM AREA

END

END
B.2.3 A/D Driver DVR 56

ADVR56 T=00003 IS ON CR00002 USING 00024 BLKS R=0000

0001 ASMB,R,L.B.C DVR56 JUNE 71
0002 WED (1311/2311 SUBSYSTEM ATE DRIVER)
0003 NAM DVR56
0005 INT 1.56,C.56

0065 * FORTRAN CALL: CALL EXEC (I, IDAT, IBUFF, N, ICHAN,ICODE)
0090 * IDAT: SUBSYSTEM DEVICE REFERENCE NUMBER
0091 * IBUFF: INTEGER ARRAY (DATA STORAGE BUFFER)
0092 * N: NUMBER OF CONVERSIONS (DATA POINTS)
0093 * ICHAN: CHANNEL NUMBER
0094 * ICODE: SUBSYSTEM/MODE;
0095 * 1: 2311 DIG ENCODER
0096 * 2: 2311 DIG FREE
0097 * 3: 2311 SEQ FREE
0098 * 4: 2310 DIG
0099 * 5: 2310 SEQ

0120 * INITIATION SECTION

0133 * CONFIGURE INITIATION SECTION 10

0144 * STA B SAVE 10 ADDRESS
0154 * STA IOR OTA CONFIGURE
0164 * STA 1012 A/D
0174 * STA 1013 CONVERTER
0184 * STA 1015
0194 * STA 1016
0204 * ADA =9300 IO INSTRUCTIONS
0214 * STA 107
0224 * ADA =6400
0234 * STA 1010
0244 * STA 1014
0254 * LDA CHAN IOR OTA
0264 * STA 102 CONFIGURE
0274 * ADA =81100 DMA
0284 * STA 108 IO INSTRUCTIONS
0294 * STA 105
0304 * ADA =84000
0314 * STA 103
0324 * XOR =84100
0334 * STA 104
0344 * STA 105
0354 * ADA =84104
0364 * STA 1011
0374 * SPC 1

0384 * VALID REQUEST CHECK
0394 * LDA EQT6,1 READ
0404 * CPA =41 ERROR CLA,INA NO - REJECT
0414 * JMP 43 YES
0424 * CLR,INA RETURN
0434 * LDA EQT6,1 NUMBER OF REQUESTED DATA POINTS GREATER THAN ZERO?
0444 * JMP ERROR NO - GO TO REJECT
0454 * SPC 1
0464 * CONSTRUCT DMA CONTROL WORD

0474 * SPC 1
0484 * LDA =41011 10 2310 OPERATION
0494 * LDA B IO ADDRESS INTO B
0504 * ADA =82000 ADD CLC OPTION
0514 * LDA EQT10,1 CODE WORD INTO B
0524 * ADD =q 6 & OR 77 I.E., 2310?
0534 * SPC 1 YES
0544 * JMP 2311 NO, 2311 Operation
0554 * STB 00.61 SET TO 2310 SEQ OR DIG MODE

58
ADD STC OPTION

SET SWITCH TO 2311 OPERATION

IF CODE 0 OR ADD STC OPTION

SAVE DMA CONTROL WORD

* CONSTRUCT A/D CONTROL WORD

CHANNEL # TO A

ICODE COMMAND PROGRAM

PACER ENABLE BIT

FREE RUN BIT

RESET A/D CONVERTER

COMMAND WORDS TO DMA AND A/D

CHANNEL TO DMA

BUFFER ADDRESS TO DMA INPUT BIT

DMA BIT

TURN OFF INTERRUPT

2310 OR 2311 OPERATION?

RETURN

NORMAL

RETURN

CHANNEL # TO A

OUTPUT RANDOM MODE

SET DIGITIZE MODE

OUTPUT DIG MODE

ACTIVATE 2310 DIG OR SEQ?

DIGITIZE

SEQUENTIAL
0160  ELA RAR
0161  IDR = 040000  SET SEQ MODE
0162  JMP 10B
0163  SKP
0164  * COMPLETION SECTION
0165  C.56  NOP
0166  IDR  CLC  CONFIGURE
0167  STA  #1  CLC DMA INSTRUCTION
0168  CLC DMA
0169  LDA  EOT4,1  A/D ADDRESS
0170  AND  #777  TO A
0171  IDR  OTA  CONFIGURE OTA A.2.D
0172  STA  #0  INSTRUCTION
0173  CLA,CEE  TURN OFF
0174  OTA A.2.D  PAGER
0175  LDB  EOT8,1  TRANSMISSION LOG
0176  EOB, RBR  TO B
0177  JMP  C.56,1  RETURN COMPLETION
0178  SKP
0179  * CONSTANTS
0180  CLC  C.56
0181  OTA  C.56
0182  OTA  C.56
0183  D0, S1  RBS 1
0184  M0111  RBS 1
0185  SPC 3
0186  IO  EQU 0
0187  0.2.D  EQU 0
0188  DMA  EQU 0
0189  TEMP  EQU  C.56
0190  A  EQU 0
0191  R  EQU 1
0192  T  EQU 3
0193  * SYSTEM BASE PAGE COMMUNICATION AREA
0194  SPC 1
0195  .  EQU 1508
0196  .  SPC 1
0197  EOT4  EQU  +11
0198  EOT5  EQU  +13
0199  EOT6  EQU  +14
0200  EOT7  EQU  +15
0201  EOT8  EQU  +16
0202  EOT9  EQU  +17
0203  SPC 1
0204  CMAN  EQU  +19
0205  INTBA  EQU  +4
0206  DUMMY  EQU  +55
0207  SPC 3
0208  END
APPENDIX C
PACED DATA ACQUISITION
USERS MANUAL

The two sections of this Appendix describe the use of program A2D for both (C.1) System Verification and (C.2) Test Data Acquisition.

C.1 SYSTEM VERIFICATION

In order to verify the complete paced data acquisition system (software and hardware), the following steps should be followed using the equipment shown in Fig. C.1.

C.1.1 Procedure

A WaveTek 142 signal generator or equivalent should be used to drive the test pulse feature of the PACER.

(1) Connect the "sync" output of the signal generator to the "sync" input on the PACER panel (Fig. 7).
(2) Connect the 50 Ω output of the WaveTek to the A/D analog channel to be tested (normally 0) and to the oscilloscope.
(3) Turn on the A/D converter.
(4) Set the WaveTek panel switches to produce a ramp voltage of 1 volt maximum peak amplitude from the 50 Ω output.
(5) On the PACER front panel connect the jack marked "BL" INPUT to the jack marked "BL" OUTPUT. Do
the same for the jacks marked "REV" INPUT and "REV" OUTPUT.

(6) Make sure "PACER ON" switches are in the "ON" position.

(7) Ensure that the Card #3 with the frequency range encompassing the blade passing frequency set on the WaveTek generator is installed in the PACER. If necessary remove the front panel air vent and replace Card #3 with the proper range card. Card #3 is shown in Figure 7.

(8) Turn on the PACER power switch and verify that the red pilot lamp is lit on the front panel.

(9) Log on the 21MX computer following the directions in the TPL Data Acquisition Manual.

(10) Once logged on, mount cartridge 28. Turn on the plotter and select the desired pen. Call up the Acquisition (Fortran) Program A2D with the command RP, A2D. Run the program with the command RU, A2D. The interactive program will prompt the user for responses. The responses are explained in the prompts which are given at the terminal. The prompts are as follows:

(a) System test or data run: enter 0.

(b) Simulated blade pair to survey: enter any number 1-8.

(c) Is test set-up ready: if yes-enter 1, if no-enter 0.
After prompt (c) is answered yes, and if the test is successful, the plotter will plot the same ramp signal that was set on the oscilloscope in C.1.1 step 4 (Fig. 12). The linearity and smoothness of the ramp signal indicate the degree to which data acquired under pacer control agree with the analog data input to the A/D converter.

C.2 TEST DATA ACQUISITION

In order to acquire paced data from the compressor (or other) test rig, the following steps should be followed with the equipment shown in Fig. C.1.

C.2.1 Procedure

(1) Cables to the PACER from the optical timing wheel on the test machine should be connected as shown in Fig. C.2. Verify the transducer input connections to the A/D converter at the A/D junction box.

(2) Turn on the A/D converter. Turn on the signal conditioner.

(3) Log on the 21MX computer following directions in the TPL Data Acquisition User's Manual. Call the Acquisition (Fortran) Program A2D by using the command RP, A2D. Then run the program by issuing the command RU, A2D.

(4) The interactive program will prompt the user for the following:

63
(a) System Test or Data Run: enter 1.
(b) Test number - enter integer.
(c) Do you wish prompting: Yes - enter 1, no - enter 0.

From this point on, the program prompts are self-explanatory.

(5) At the completion of the data acquisition, the data values are printed out as shown in Table C-I.

(6) The final prompt will ask if another run is desired.

C.2.2 Data Storage

The survey data acquired in the program A2D is contained in the data memory locations SRUPT (J) where \( J = 1 \rightarrow 256 \). The program A2D may be modified to output the data as desired by the user or to pass the data to a user-written subroutine for analysis.
Table C-1. Paced Data Output from Program A2D
THIs IS TEST #5 RUN ON JULIAN DATE 149 1981

PACED SURVEY DATA

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<th>Time (s)</th>
<th>Paced Survey Data</th>
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<td>0.0937500</td>
</tr>
<tr>
<td>0.1953125</td>
<td>0.2148439</td>
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<tr>
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<td>0.5742188</td>
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<tr>
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<td>0.8146063</td>
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<td>0.9259393</td>
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<td>1.0165253</td>
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<tr>
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<td>0.7039725</td>
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COMPRESSOR RPM FOR THIS RUN WAS 10541.4

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM TOP CORNER TO DDC
Figure C2. Cable Connections for Test Data Acquisition
LIST OF REFERENCES


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<tr>
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<th>Distribution List</th>
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