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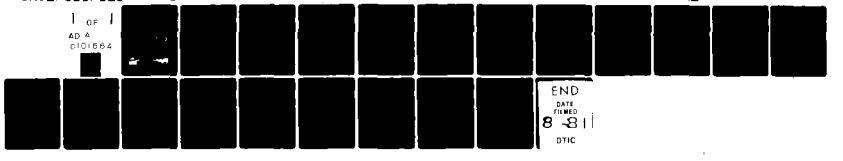

LEVEL 2

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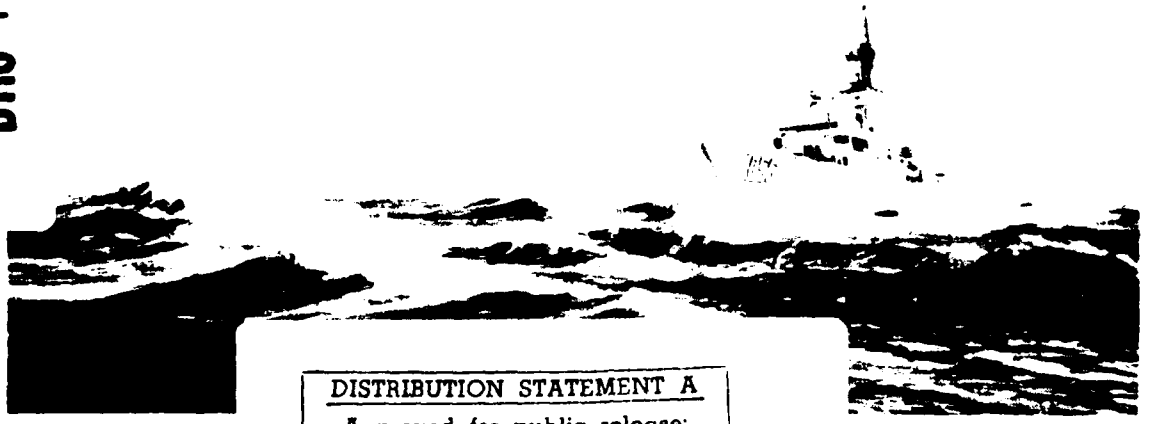
N00014-75-C-1146

Coding for Navy UHF Satellite Communications CODEC Evaluation Study



HARRIS

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Coding for Navy UHF Satellite Communications CODEC Evaluation Study.

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Washington, C C. 20360

(11) 14 May 1981

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INTRODUCTION

Harris Corporation, GESD, is pleased to submit this report regarding further experimental verification tests performed on the NAVELEX coder-decoder unit. The codec unit was developed under contract as an element of the UHF Satcom Coding Study. The codec design philosophy, employing convolutional encoding and Viterbi decoding, was discussed in the Phase I report. A later Phase II report was concerned with the breadboard codec itself, along with the testing program conducted at the Navy Postgraduate School in Monterey.

Our recent experimental effort has been concerned with resolving some hardware problems in the breadboard codec. Additional performance data has also been collected in this process.

Preliminary Test Configuration

Preliminary testing of the codec was attempted using a "back-to-back" configuration. The internal PN data sequence generator was used to supply a signal to the modulator-encoder circuitry. The coded modulator output was then directed to the demodulator via the analog data port. This port serves as an input to the AGC-quantizer-bit synchronizer signal path. A problem in obtaining decoder bit synchronization with the received data sequence was traced to an inactive -5 volt power supply output. The absence of this supply voltage causes a loss of the received signal at the AGC gain block "quantizer" input. By temporarily restoring the -5 volt level with an external supply, we were able to obtain an acceptable quantizer input signal from the AGC gain block. (Some minor adjustment to the multiplier bias level via R8 on card XA2A17 was required, in order to remove the D.C. level apparent at the quantizer input).

Once the input to the bit synchronizer-quantizer was established, the codec was operable in the coded and uncoded modes. (The decoder is configured to perform either a 3-bit soft decision or a 1 bit hard decision on the received data prior to Viterbi decoding). The internal error comparator circuitry was suspected of somewhat erratic error indications in the initial checkout tests. As a consequence, we were led to consider a test configuration which would employ an external data source/data error analyzer unit.

Error Performance Test Configuration

In this test configuration, a data waveform is supplied by the external data error analyzer. For our performance tests, a pseudonoise baseband data sequence of length 63 was selected. This data waveform is then corrupted by additive random noise derived from an adjustable noise source. The resulting data signal plus random noise is supplied to the demodulator analog input, at which point the signal power and noise power in the data-signal bandwidth are determined. These quantities allow us to establish a value of Eb/No for the bit error test.

The decoded data stream, which is obtained from the decoder output port (front panel) is then supplied to the data error analyzer. The error analyzer may be configured to measure the resulting bit error rate for an established signal to noise ratio. (The signal to noise ratio is varied by the adjustment of the r.m.s. output of the noise source. Each measurement of signal and noise power is referenced to the demodulator analog input port). This measurement technique has been employed successfully in the past to determine the bit error rate performance of telephone line modems. The results of this particular method depend upon the accurate measurement of the noise power in the data signal bandwidth. This is normally accomplished by filtering the noise prior to the measurement of the noise power via an r.m.s. voltmeter.

The filter chosen in this case was a single-pole Butterworth filter, with a 3dB frequency equal to the data rate of 9600 bps. The noise equivalent bandwidth of such a filter is well known, and allows for the accurate measurement of the noise power in the data-bandwidth.

It is worthwhile to note that this "measurement shaping filter" is not in the signal path, and thus the noise apparent at the demodulator analog input is substantially "white". The filter is employed only to measure the noise power in the bandwidth of the data signal. For convenience, the codec tests were performed at a channel rate of 9600 bps. (This rate establishes the 3dB point of the noise measurement filter).

With the test configuration described above, we were able to confirm the operation of the codec in the coded and uncoded modes, employing all of the available coding rate selections. (Specifically, BER versus Eb/No data was determined from the experimentation. Refer to Appendix).

DISCUSSION AND SUMMARY

The NAVELEX breadboard codec performance has been verified in the uncoded and coded modes at all code rates. The operation of the data interleaver/de-interleaver and differential encoder/decoder has also been substantiated in the performance tests. Both the 1-bit hard decision and the 3-bit soft decision decoder modes are operational. Our initial difficulties in the checkout phase were determined to originate in a defective -5 volt power supply module, which is being replaced.

It was also necessary to perform some minor adjustments to the AGC gain block D.C. bias control (R8). Through careful adjustment of this bias control, an acceptable signal output to the quantizer-bit synchronizer was obtained. This nulling adjustment allows for optimum coder-decoder performance in the presence of zero-mean noise, by eliminating the D.C. offset present at the quantizer input.

- Performance Test Results

As a measure of codec system performance, Bit Error Rate versus Eb/No data has been obtained through the method described earlier in this report. The bit error measurements were performed at a channel rate of 9600 bits/second in the various coded channel modes, with the noise power spectral density as the independent variable. In order to establish a performance baseline for our tests, data was also obtained with the codec set in the "uncoded" mode.

The experimental results indicate the performance improvement which may be obtained through coded communications. The coding gain obtained is a function of the code rate, with the highest code rate ($R=\frac{1}{2}$) exhibiting the best performance, followed by R=2/3 and R=3/4 coding respectively. (Note that these results are for a fixed channel rate of 9600 bps, and are in general agreement with the theoretical performance predictions for convolutional encoding and Viterbi decoding. Refer to the Appendix) The use of data interleaving/deinterleaving provided a minimal codec performance improvement (< 1dB) in the coded channel modes for non-burst errors. In theory, the error performance of the interleaved code should be identical to that of the subcode for purely random (i.e. gaussian noise induced) errors. With pseudo-random interleaving, the subcode and the

interleaved code have the same minimum distance, and one would not expect a performance improvement for non-burst type errors. (In our tests, we are not introducing burst errors and thus are not using the data interleaving/deinterleaving function to an advantage).

A possible explanation for some differences in our recent test results versus those obtained in the Monterey testing program may be found through a comparison of the basic test configurations used. In the test configuration employed at HESD, the corrupted baseband encoded data was introduced directly into the decoder analog data input. The test configuration used in the Monterey program included a PSK modulator, RFI simulator and an AN-WSC-3 receiver. The decoder analog input port thus received the baseband data through an interface with the AN-WSC-3 receiver.

Normally, one would expect some performance degradation to be introduced by a modulator-receiver test configuration relative to a "back-to-back" test configuration. This would be the case if, for example, the noise power introduced in our test configuration was band-limited to the same extent as the AN-WSC-3 receiver baseband output. The test configuration employed at HESD does not, however, significantly band-limit the output of the random noise source. Thus, for equivalent BER performance, the Eb/No ratios required in our tests may appear to be higher than those required in the Monterey performance tests. The excess total random noise power applied to the decoder analog input by our test configuration must contribute to a degradation of the decoder performance, at the AGC-quantizer level.

Some insight into the preceding situation was obtained by placing a low-pass Butterworth filter into the signal path, in order to eliminate much of the excess noise power apparent at the decoder analog input. (The filter had a noise equivalent bandwidth higher than the bit-rate bandwidth, and was inserted into the signal path between the summing amplifier and decoder analog input. Refer to the diagrams in the Appendix). With the codec in the uncoded mode, BER performance data was obtained as a function of Eb/No. The resulting data indicated a significant improvement in performance, as compared to the experimental results obtained earlier, without the signal prefiltering.

A closer correlation between our experimental results and those obtained in the Monterey test program would be expected if the spectral characteristics of the AN-WSC-3 receiver output were duplicated by such a signal prefilter.

APPENDIX

A BLOCK DIAGRAMS

B ERROR TEST CONFIGURATION

C BER VERSUS Eb/No DATA

BLOCK DIAGRAM DEVELOPMENT

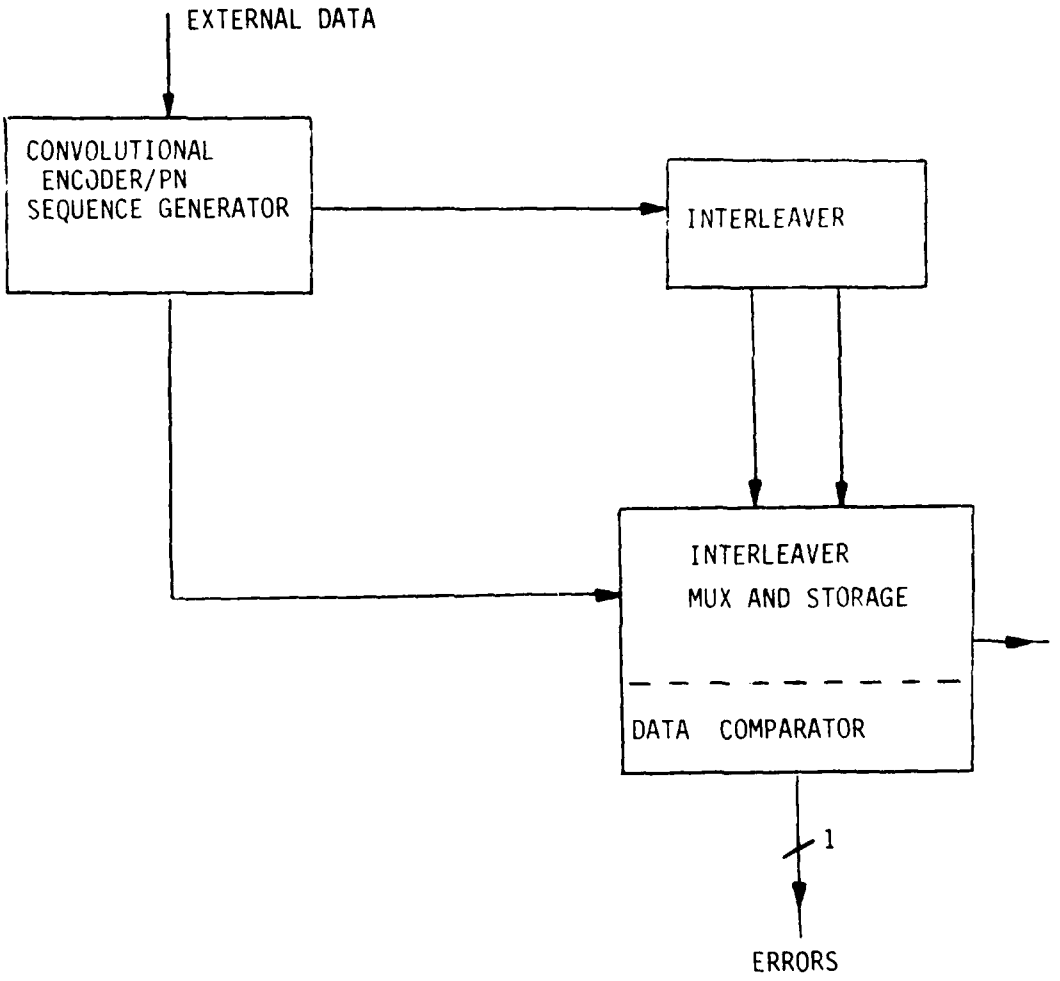
During our preliminary checkout of the coder-decoder unit, it was apparent that much of the existing hardware design documentation was in the form of detailed schematic diagrams. These diagrams are included in the Codec Operating Guide (Phase II). By tracing through most of the coder-decoder circuitry, an intermediate level codec block diagram representation was developed. These block diagrams should prove to be helpful in any diagnostic work performed on the coder-decoder.

Convolutional Encoder

The convolutional encoder is implemented with a discrete (LS378 D- flip flop) shift register, a programmable read only memory and associated logic circuitry. This design approach inherently allows for the multiple - code rate selection function. The data input to the encoder may be derived from bipolar/TTL external inputs, or from an internal PN sequence generator. (The PN sequence generator consists of a 7 stage maximal length linear feedback shift register with the associated logic gates). The output of the convolutional encoder is passed to the interleaver, where a pseudo-random permutation is performed on the encoded data. This is accomplished by inserting the data into a 1008-location random access memory via a pseudo-random addressing sequence. The addressing sequence is again stored in a programmable read only memory. The encoded and interleaved data, which is derived from the RAM, is then available for transmission to the modem/channel.

The internal error comparator circuit consists of a shift register of the same type as is used in the PN sequence generator. This shift register is manually synchronized to the received data stream via a front panel push button. A bit by bit comparison of the generated PN sequence and the received data sequence thus provides an output indication of the channel bit errors. (The BER may then by measured via an external counter).

CODER BLOCK DIAGRAM



Bit Synchronizer

The bit synchronizer design employed in the NAVELEX codec was first developed independently on a similar digital communications program. (Some elements of the original quantizer and the AGC were not incorporated into the codec design). Internal bit synchronization is used in the codec whenever the decoder must operate upon an incoming analog data signal, as in an actual communications link.

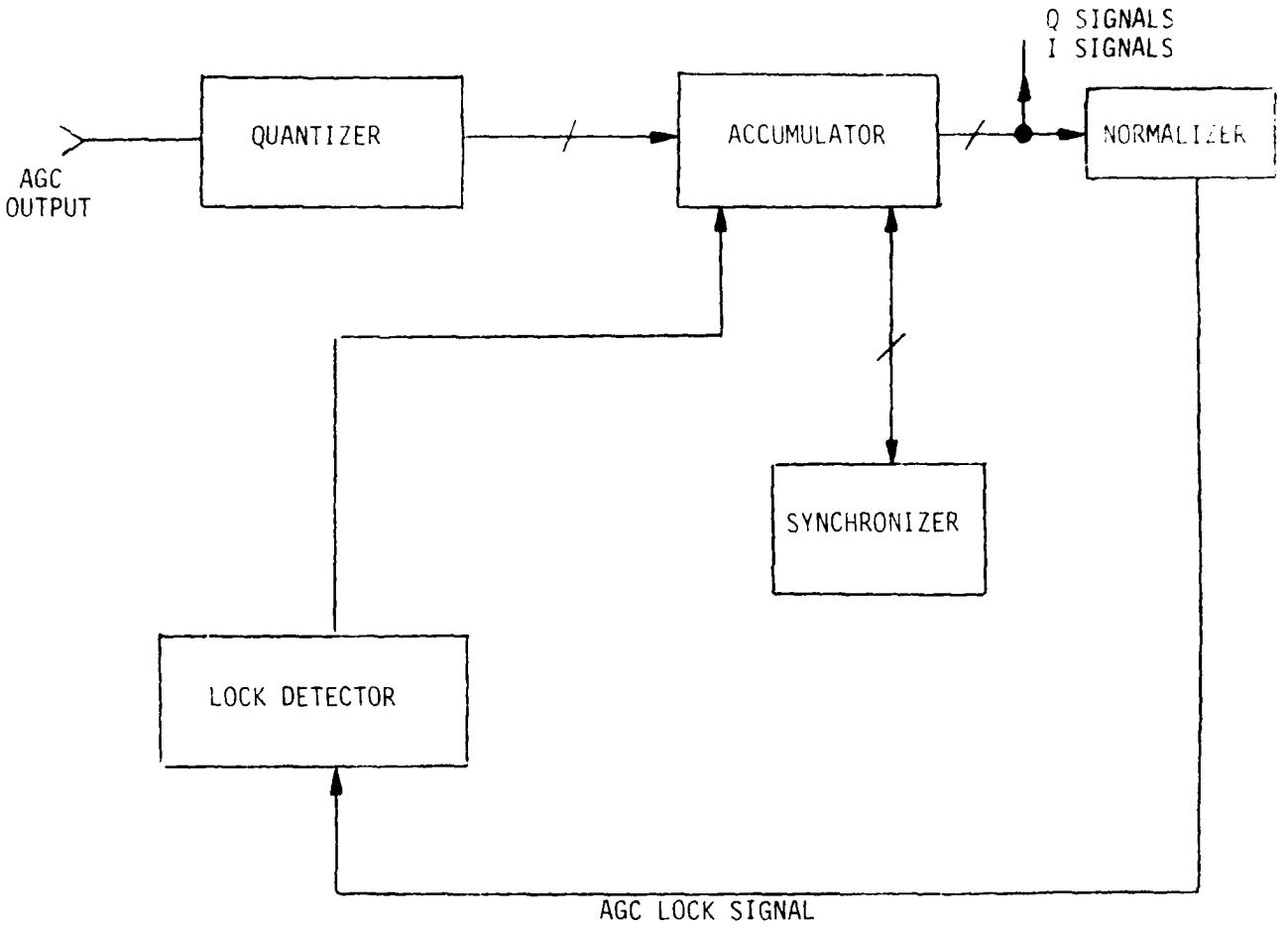
The analog data is first conditioned within an AGC gain block stage, which provides some "squaring-up" of the incoming data sequence as well as the gain control functions. It is in the AGC gain stage where some nulling adjustment of the output d.c. level was required in order to provide the proper signal into the quantizer.

Following the AGC function, the received data is applied to a set of 8 open-collector level comparators within the quantizer block. These level comparators perform the quantizing function upon the received data signal, and provide digital-compatible signals for the soft-decision process. The comparator outputs are directed to a data-sampling storage register and level encoder which then produces the actual 3-bit soft decision representation of the received data.

The 3-bit soft decision data representation is then applied to the accumulator registers as an update signal. (The original bit synchronizer provided both I and Q channel representations of the data stream, presumably in a QPSK signalling application). The accumulator 3-bit soft decision output signals are then applied to a normalizer stage, one output of which is an AGC lock signal to the lock detector. The lock detector, upon receiving the AGC lock signal shifts the accumulator-synchronizer from a scan/sweep mode to a locked mode.

When the bit synchronizer has acquired lock, the 3 bits of the quantizer-level encoder form an optimum representation of the incoming data signal. The sign bit and most significant bit are identical to the incoming data, while the least significant bit is an inverted representation of the data signal. The acquired data signal is then applied to the decoder circuitry.

BIT SYNCHRONIZER BLOCK DIAGRAM



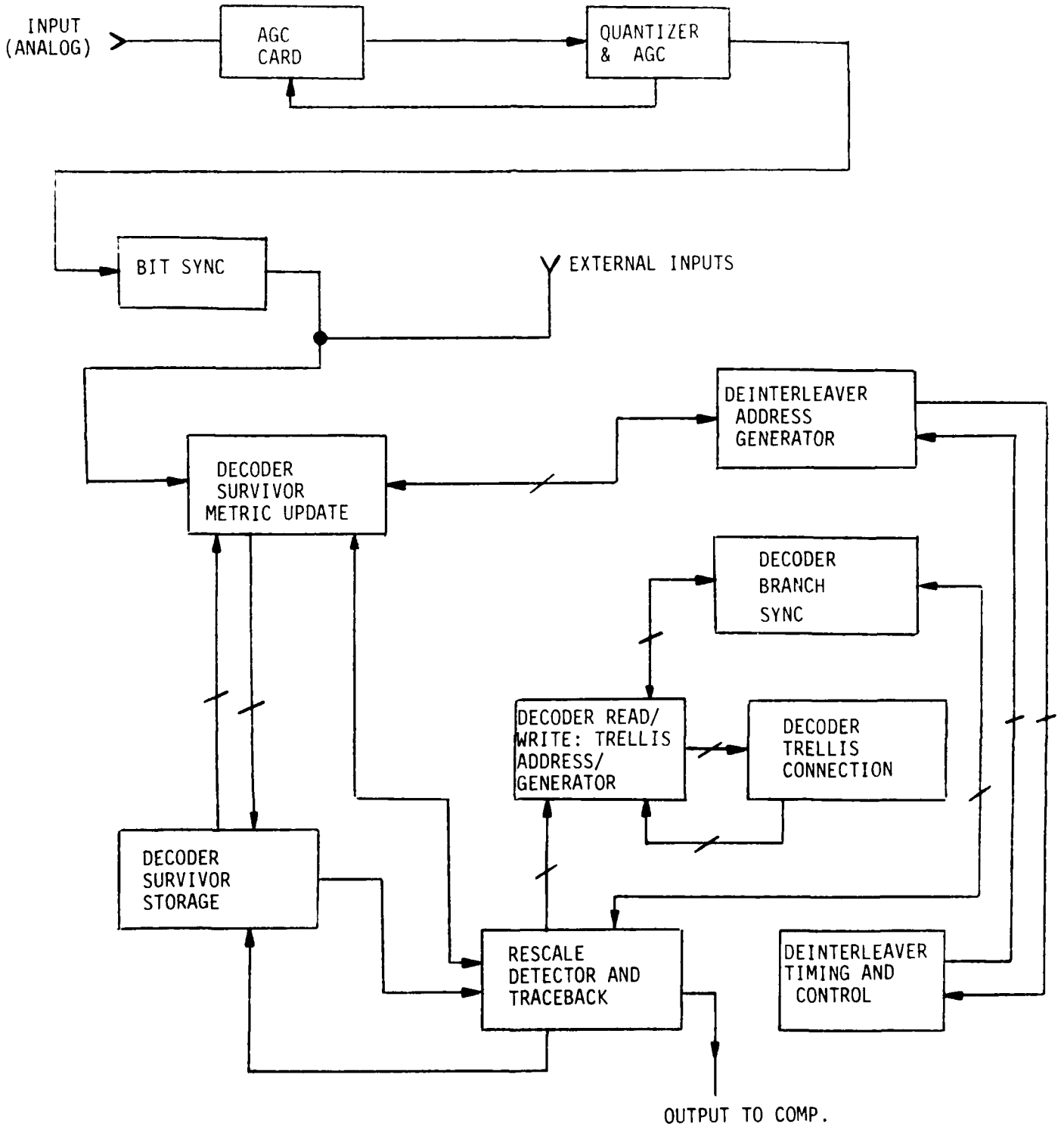
Viterbi Decoder

The decoder employed in the codec provides for Viterbi decoding of the received data stream. The function of pseudo-random data deinterleaving is also provided in order to extract the subcode from the interleaved code. (The deinterleaving function performs the inverse operation of the data interleaver).

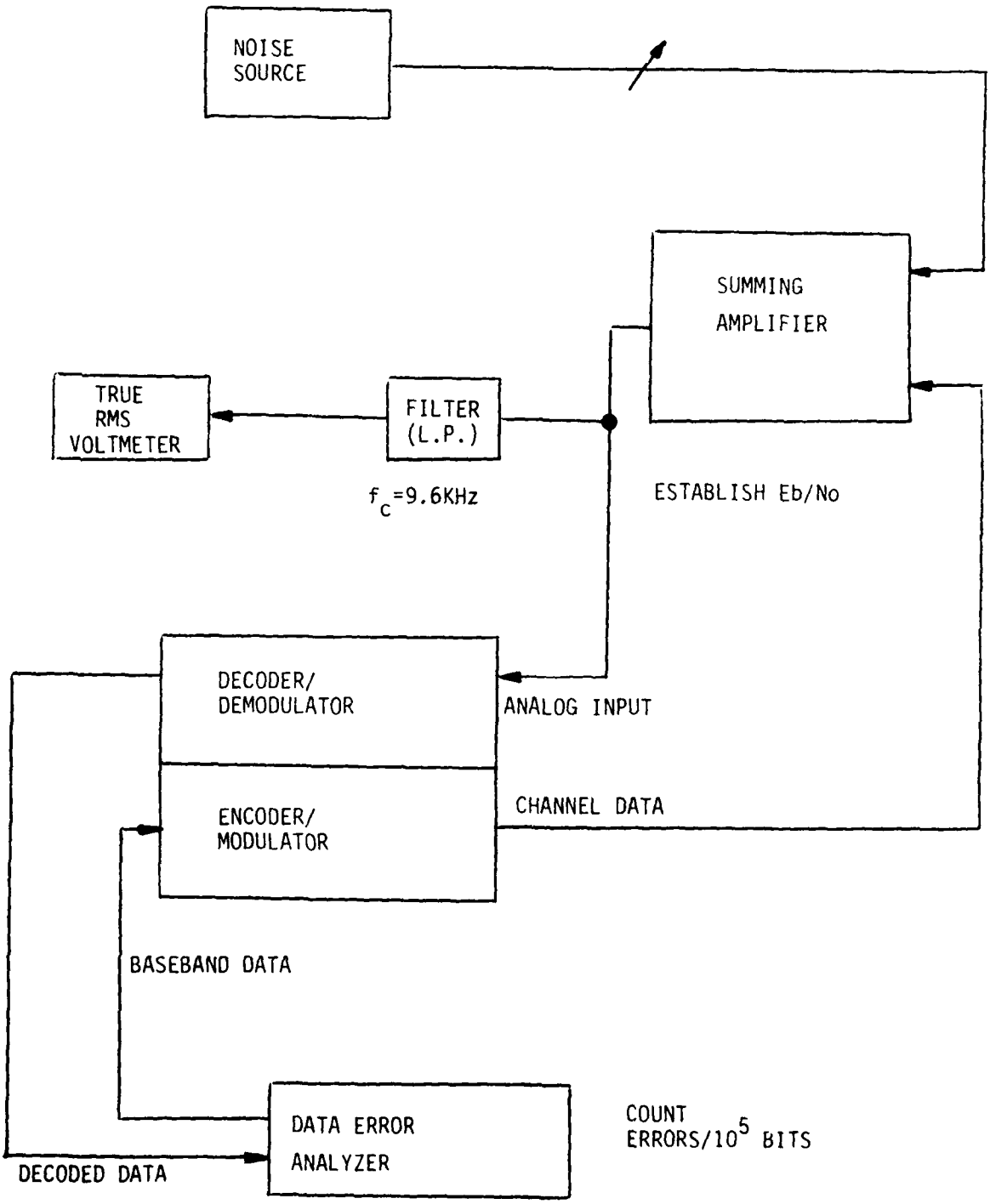
The deinterleaved data is then operated upon by the Viterbi decoder, which performs the maximum likelihood decoding algorithm . As a decoder, the Viterbi algorithm involves the recursive determination of the shortest (i.e., most likely) path from an input state sequence to an output state sequence. This is accomplished by computing and storing the trellis path segments corresponding to an input sequence. The most likely (i.e., shortest) path segments are then selected as survivors. Given a finite input state sequence, the algorithm will terminate at some time t_K with the shortest path stored as the survivor. The path survivor is then an optimal representation of the input state sequence at time t_K.

The decoder implementation which is presented in the following block diagram was extracted from the detailed schematic diagrams.

DECODER BLOCK DIAGRAM



ERROR PERFORMANCE TEST CONFIGURATION



Determination of Eb/No

Consider the noise output of the measurement filter under "no signal" conditions to be bandlimited gaussian noise. If No is the power spectral density of the filter input, then $|H(f)|^2$ No is the filter output power spectral density where H(f) is the filter transfer function.

For an n^{th} order Butterworth filter, the noise-equivalent bandwidth is related to the 3dB rolloff point by

$$B_N = f_{3dB} \int_0^\infty \frac{1}{1+X^{2n}} dx$$

$$= \frac{\pi f_{3db}/2n}{\sin(\pi/2n)}$$

$$B_N = \frac{\pi}{2} f_{3dB} \quad \text{for } n=1$$

For a Butterworth filter (n=1) which is loaded by a 600 ohm voltmeter impedance, the transfer function relating the input voltage to the output voltage is as follows:

$$H(f) = \frac{R_o}{j\,2\pi f\, R_{in}R_o\, C + R_{in}+R_o}$$

In the above expression, R_{in} represents the filter resistance, and R_o represents the voltmeter impedance which is in parallel with C.

Let $\alpha = R_o$

$\beta = R_{in} + R_0$

$\delta = 2\pi R_{in}R_o C$

Thus

$$|H(f)|^2 = \frac{\alpha^2}{\delta^2 f^2 + \beta^2}$$

By definition,

$$Bn = \frac{1}{Ho^2} \int_0^\infty |H(f)|^2 \, df; \text{ then}$$

$$Bn = \frac{\beta^2}{\alpha^2} \int_0^\infty \frac{\alpha^2}{f^2\delta^2 + \beta^2} \, df$$

$$= \frac{\beta}{\delta} \tan^{-1} \frac{\delta f}{\beta} \Bigg|_0^\infty$$

$$= \frac{R_{in} + R_o}{2\pi R_{in} R_o C} \tan^{-1} \frac{2\pi R_{in} R_o C f}{R_{in} + R_o} \Bigg|_0^\infty$$

$$= \frac{\pi}{2} \frac{R_{in} + R_o}{2\pi R_{in} R_o C}$$

which is the desired result.

Using the bit rate equals bandwidth approximation for the channel data, the bit energy to noise power spectral density ratio may be found from the following relation

$$Eb/No = \frac{Ps}{Pn}\left(\frac{Bn}{R}\right)$$

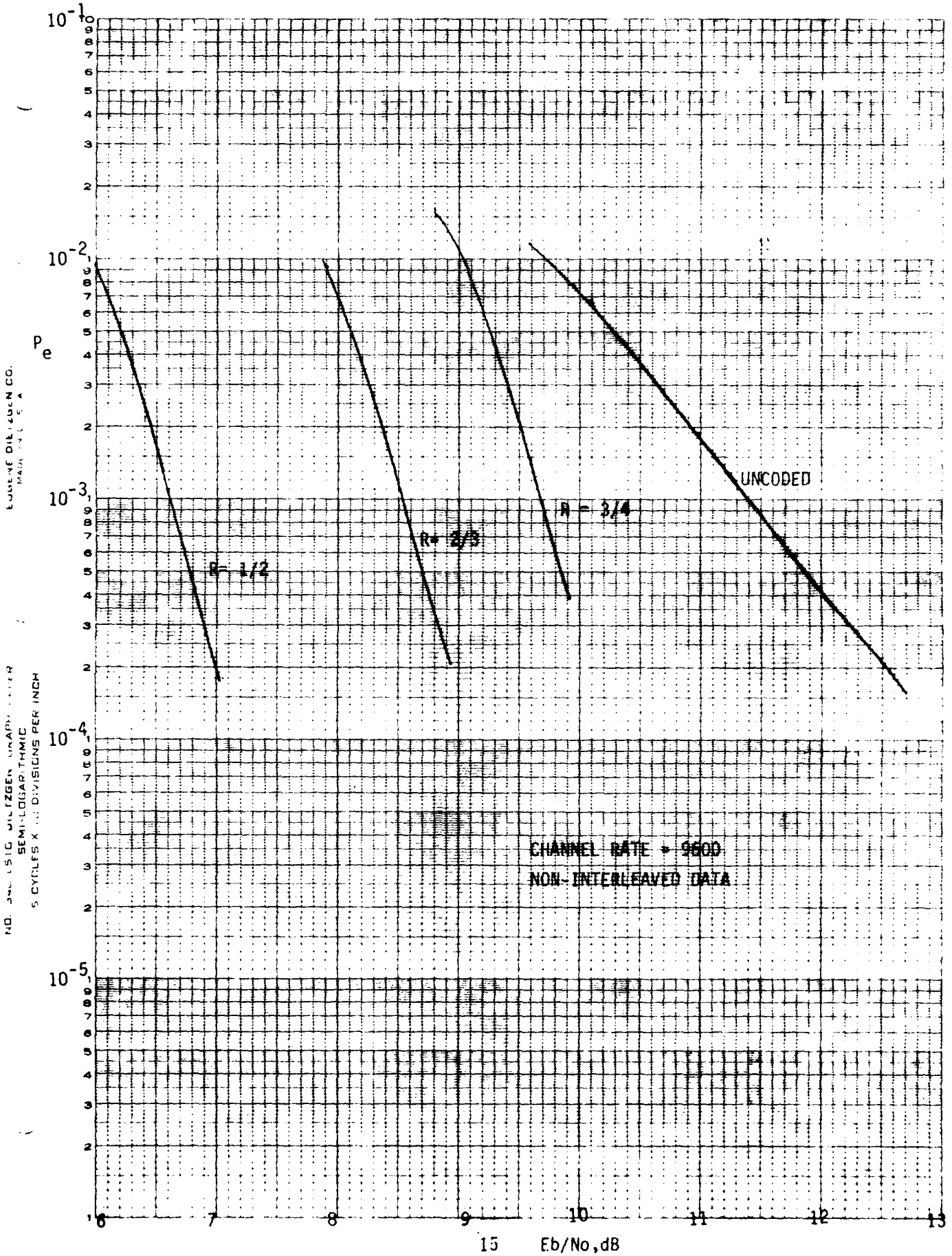
where

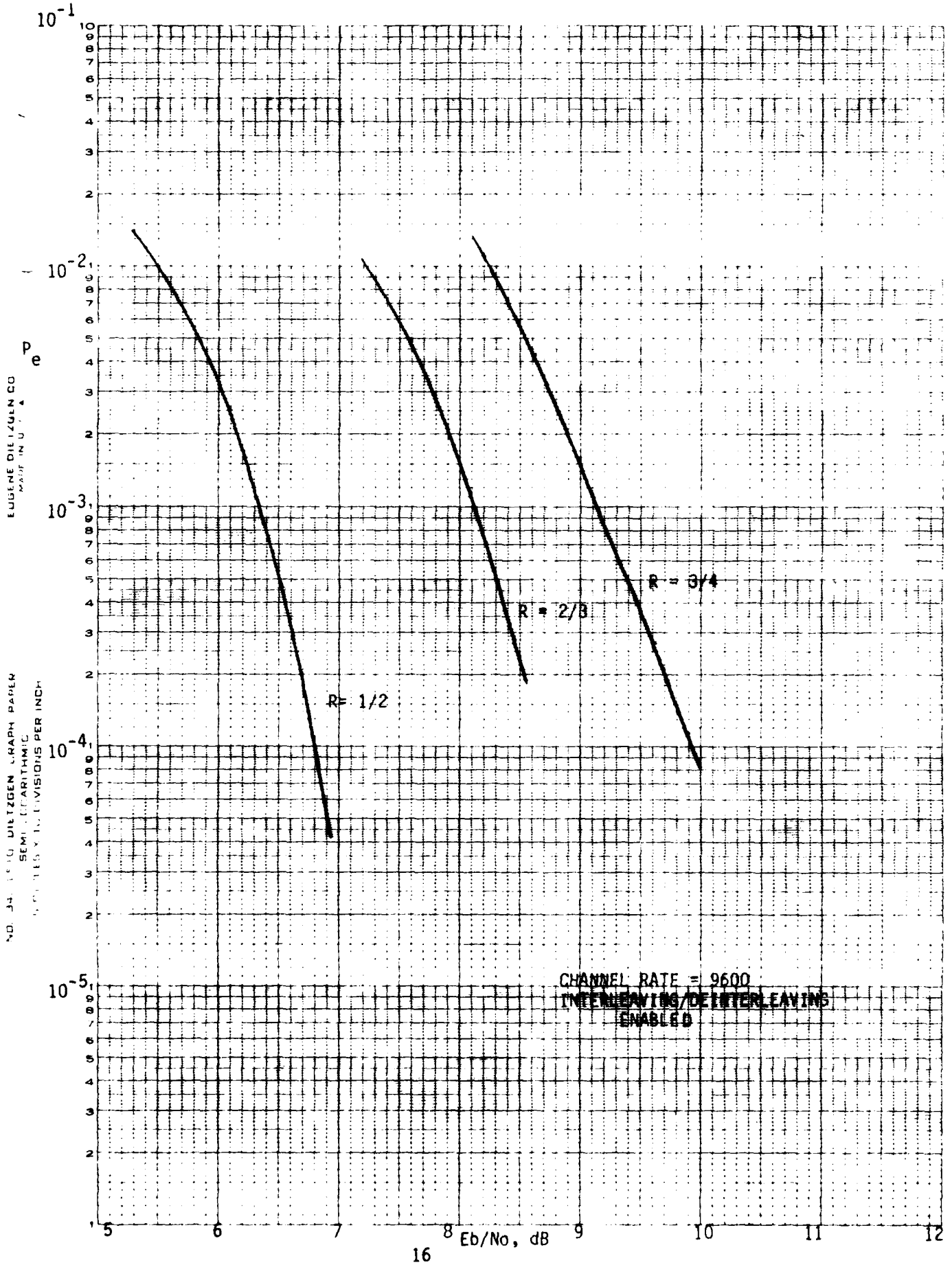
Ps = RMS signal power

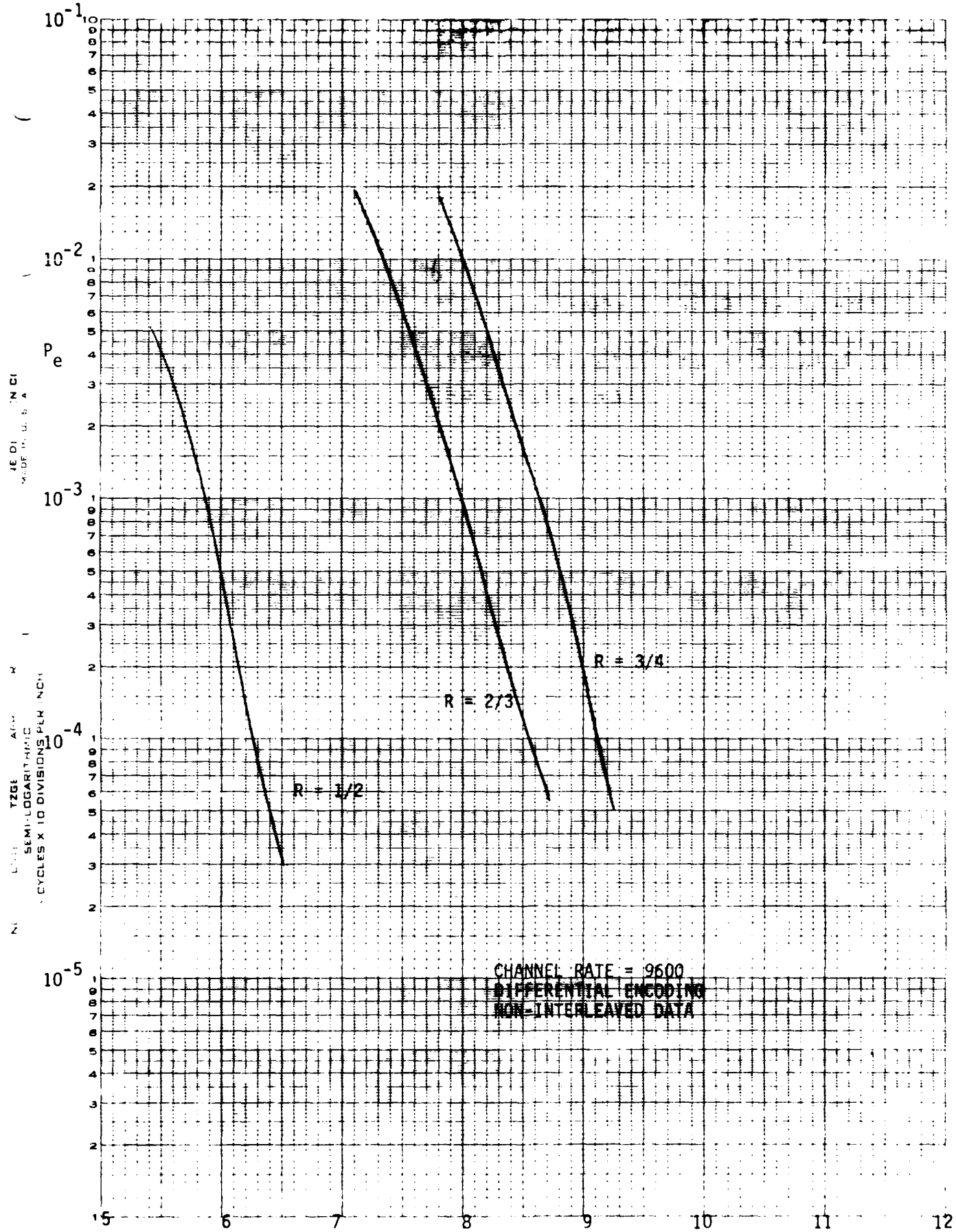
R = Channel rate

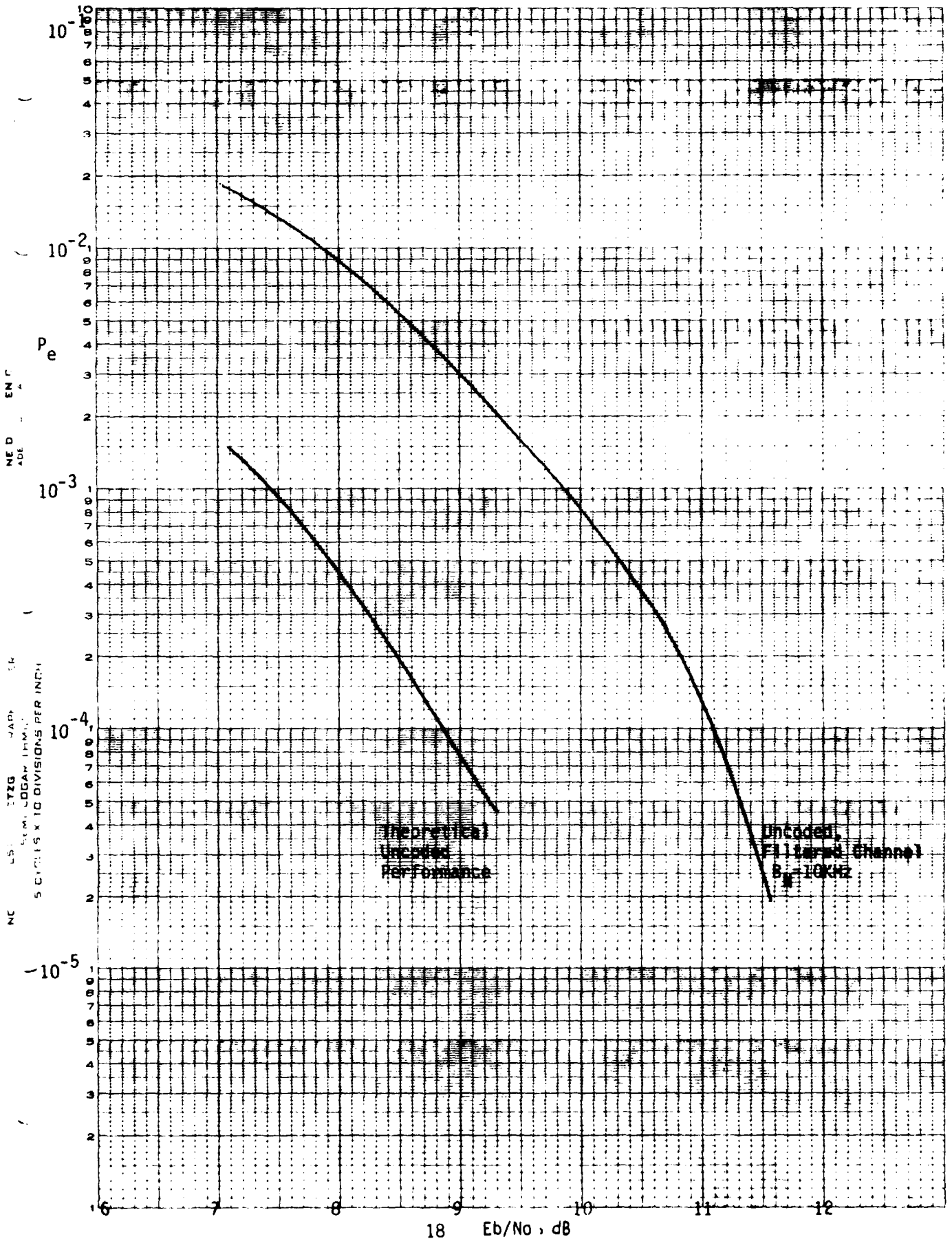
Pn = RMS noise power with the measurement filter loaded

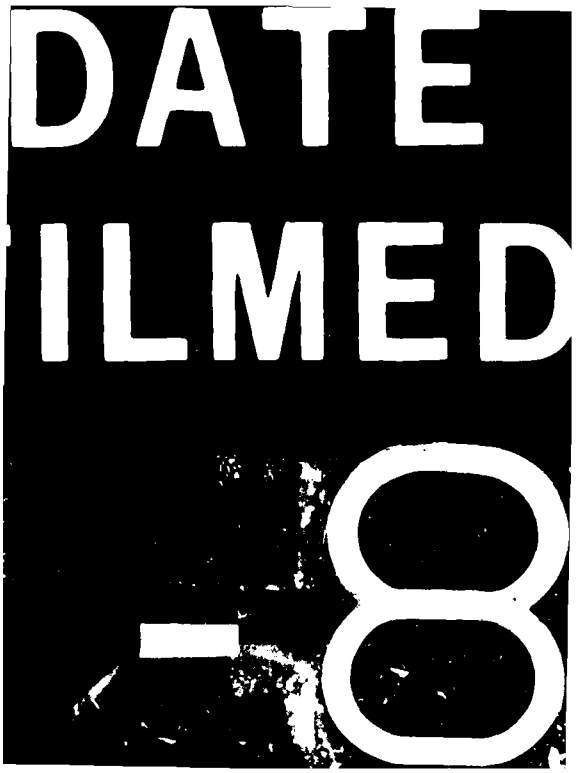
Bn = Noise equivalent bandwidth of the measurement filter


10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
P_e
R= 1/2
R= 2/3
R = 3/4
UNCODED
CHANNEL RATE = 9600
NON-INTERLEAVED DATA
6
7
8
9
10
11
12
13
Eb/No,dB


10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
P_e
R = 1/2
R = 2/3
R = 3/4
CHANNEL RATE = 9600
INTERLEAVING/DEINTERLEAVING
ENABLED
5
6
7
8
9
10
11
12
Eb/No, dB


10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
P_e
R = 3/4
R = 2/3
R = 1/2
CHANNEL RATE = 9600
DIFFERENTIAL ENCODING
NON-INTERLEAVED DATA
5
6
7
8
9
10
11
12
Eb/No,dB


10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
P_e
Theoretical Uncoded Performance
Uncoded, Filtered Channel
B_N=10KHz
6
7
8
9
10
11
12
Eb/No , dB


DATE
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