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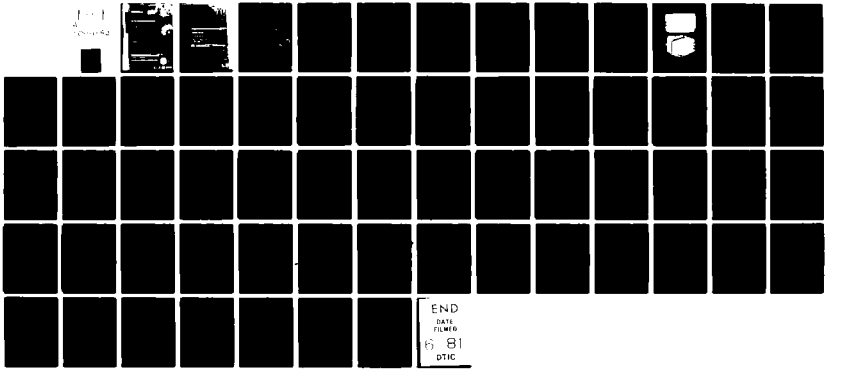

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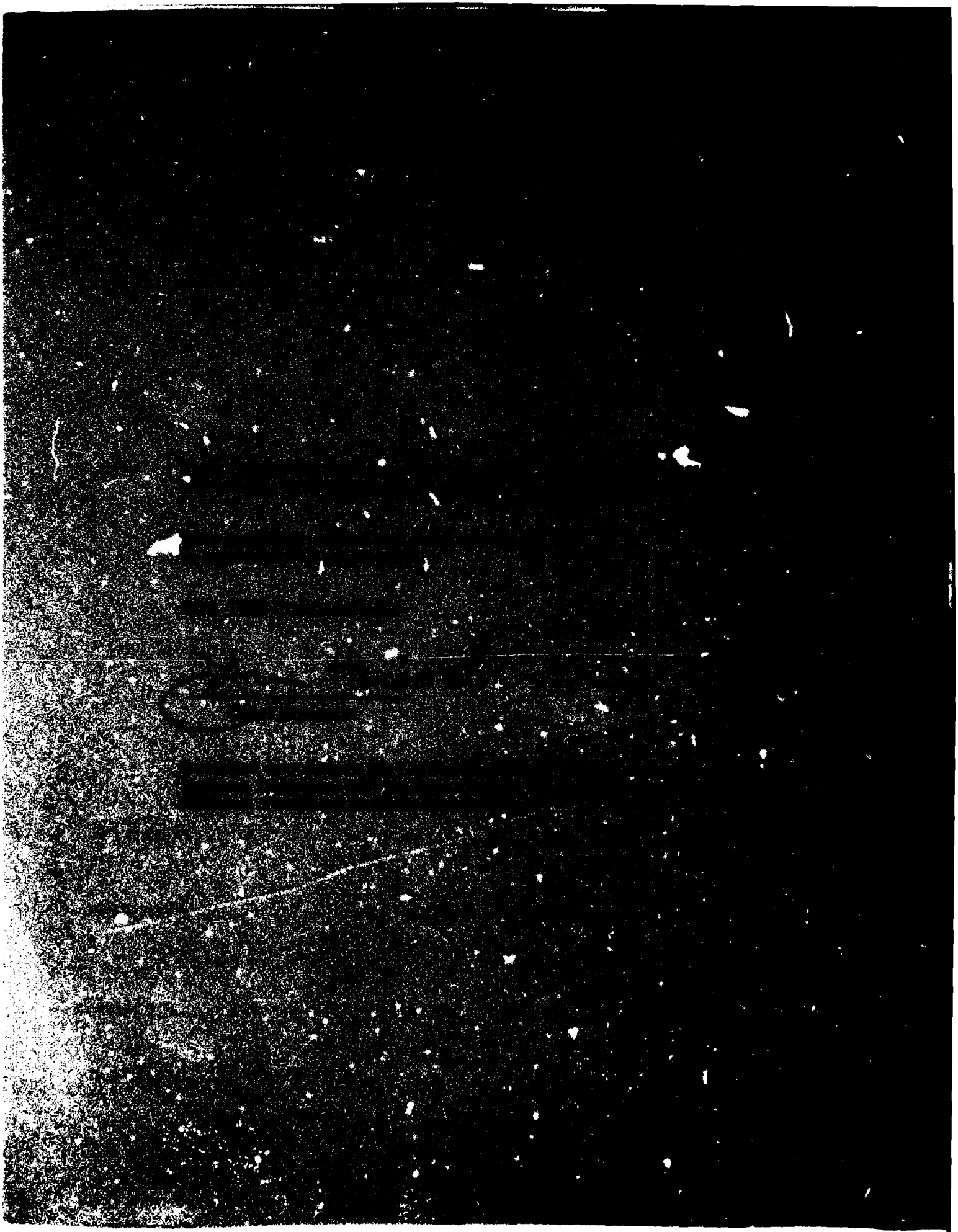

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes an 18-channel command decoder-selector which operates in conjunction with an HF command receiver to allow secure and reliable radio control of high altitude balloon payloads. A detailed technical description and test results are also included.

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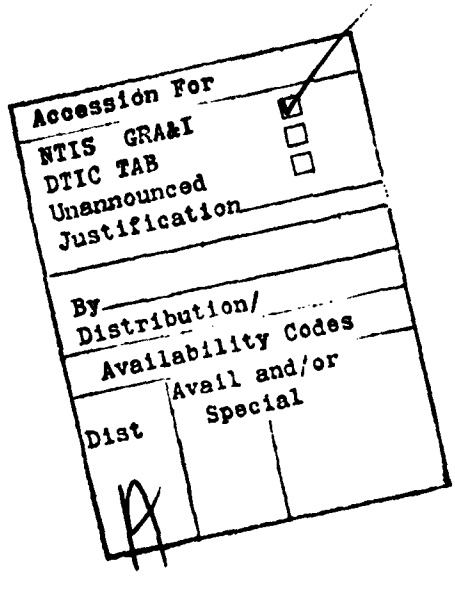
Preface

The author wishes to thank SSgt Ganion for his assistance in the development and testing of the BCS-18A Command Decoder-Selector, Lawrence Smart for the development of the printed circuit art work, and Andrew Carten for the many helpful hints and suggestions during the writing and editing of this report.



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BSC-18A Command Decoder-Selector

1. INTRODUCTION

This report describes the BCS-18A Command Decoder-Selector developed under In-House Work Unit 76591201, and also serves as a user's reference manual for the Command Decoder-Selector. (The Command Decoder-Selector will herein be called simply the "command selector" or "selector.")

The command selector is a key component of a ground-air-ground data and control system. It was designed primarily for use with high-frequency (HF) balloon-borne command receivers to allow secure and reliable radio control of high-altitude long-distance balloon payloads. It can be used, however, with any command receiver which is capable of driving the tone filters in the selector.

In its intended application, the command selector operates in conjunction with a ground-based command tone generator and transmitter, and a balloon-borne receiver and transmitter. This system employs several discrete audio tones, in various combinations, to distinguish between 18 command channels. The function of the command selector is to decode the audio tones transmitted from the ground, using the information to select and energize the desired channel. It then provides a ground closure to activate a particular balloon system function. The selector also provides a unique output voltage or code for each command channel. This code

(Received for publication 20 August 1980)

or voltage is transmitted back to the control station to indicate proper channel acquisition or command status. (Section 3, Technical Approach, describes channel selection and output codes in detail.)

2. DESCRIPTION OF EQUIPMENT

2.1 Technical Characteristics

The technical characteristics of the command selector are listed in Table 1. The unit is protected against reverse polarity and is current-limited.

Table 1. Technical Characteristics

Power Requirements:	12 V to 28 V at 40 mA Standby 160 mA max. (during command)
Tone Filter Frequencies:	7 tone filters within a frequency band of 300 Hz to 3000 Hz
Tone Filter Selectivity:	+/-2 Hz (typical)
Tone Filter Accuracy:	+/-0.1 percent
Audio Input Impedance:	55 ohms
Audio Drive Level:	1 V rms per tone
Operating Temperature:	-40 deg C to +55 deg C
Operating Ambient Pressure:	1014 mb to 0.2 mb
Connectors:	1 each DA-15P (15 pins) 1 each DB-25S (25 pins)
Channel Outputs:	18 ground closures rated at 1 A max. resistive load
Dimensions:	5-3/4 in. (H) × 4 in. (W) × 6-1/2 in. (D)
Weight:	3 lb. 1.5 oz.

2.2 General Description

The command selector consists of four panel-mounted printed circuit boards enclosed by an aluminum protective case (see Figures 1 and 2). Inputs and outputs are provided by two front panel connectors. All printed circuit boards use edge

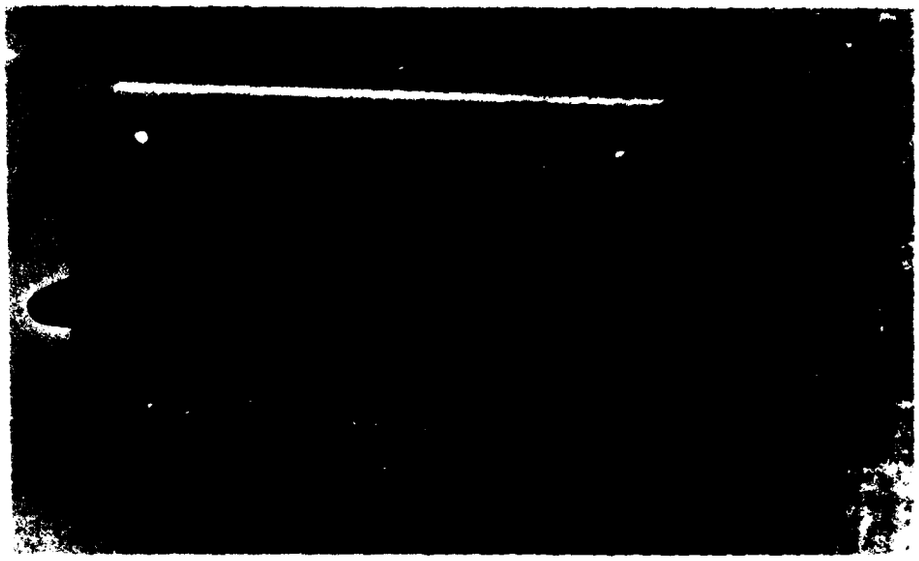

Figure 1. BCS-18A Command Decoder-Selector

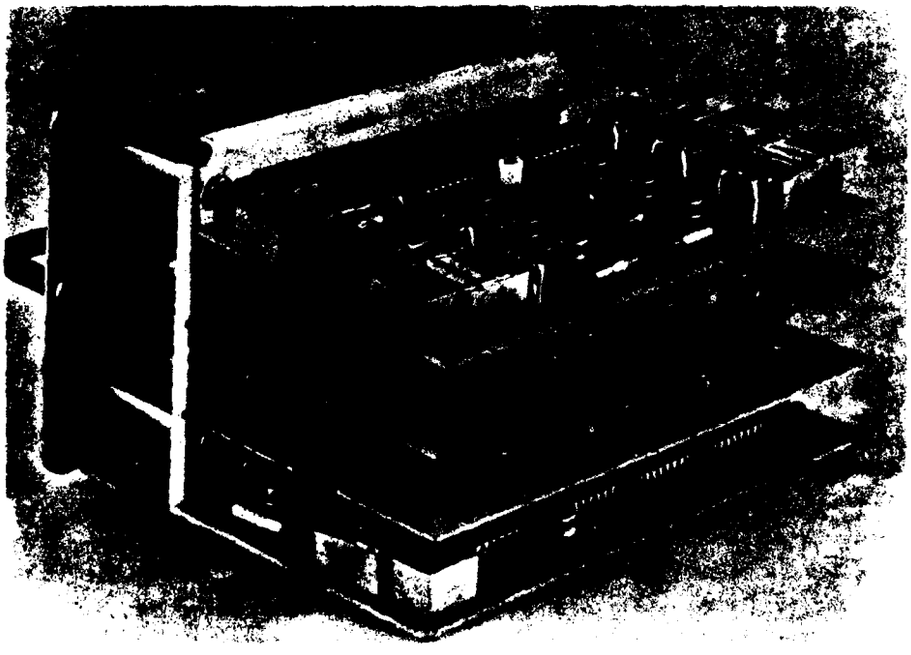

Figure 2. BCS-18A Selector (Case Removed)

connectors. Internally, all logic functions are performed by low-power C-MOS integrated circuits with high noise immunity. For ease of maintenance, trouble-shooting, and repair, all active components (tone filters, integrated circuits, transistors, and relays) utilize sockets. The physical dimensions of the selector are listed in Table 1.

3. TECHNICAL APPROACH

This section describes the operation of the command selector in general terms. The reader should refer to Section 4, Theory of Operation, for detailed circuit descriptions.

3.1 Audio Tone Frequencies and Combinations

The ground-based tone generator provides seven different audio tones, with frequencies between 300 Hz and 3000 Hz, for transmission to the balloon system's command selector. When particular commands are desired, combinations of four tones (three tones for command selection and a fourth tone for command execution) are used. The seven possible tones allow enough different combinations of four to accommodate 18 command channels. Table 2 shows the combinations used, with tones A through F serving in the channel selection role. Tone G is the common command execution tone. The basic decoder-selector concept was developed by Zenith Radio Corporation in the early 1960's under an Air Force contract. However, the implementation of the concept in the command selector is completely different from that used originally by Zenith.

3.2 Channel Selection and Execution, An Overview

The channel selection step must be accomplished before a command is executed. This step utilizes three sequenced tones. Two are used together to create a combined output (for example, tones A and B would produce output AB). To keep modulation at reasonable levels, the command tone generator removes the two-tone combination after 2 sec, when a third tone (for example, F) starts. After a subsequent 3.5-sec delay, a channel becomes "selected." The command selector then generates a special code or voltage appropriate to the selected channel to verify channel acquisition. This code or voltage is transmitted back to ground control.

After the control station receives the channel selection confirmation, it sends a fourth tone (G) to the command selector. When this fourth tone is present for 3.5 sec, the selected channel becomes energized and stays energized until the steps are taken at ground control to remove all tones. Upon deactivation of the channel, the same verification code, if used, is regenerated by the command selector.

Table 2. Tone Combinations, Reply Codes and Reply Voltages

Tones	Reply Codes		Decimal Equivalent	Voltage Verification Output*
	Morse	Octal		
Ch 1 AB + D + G	SSU	001	1	0.1 V
Ch 2 AB + E + G	SSR	002	2	0.2 V
Ch 3 AB + F + G	SSW	003	3	0.3 V
Ch 4 AC + D + G	SSD	004	4	0.4 V
Ch 5 AC + E + G	SSK	005	5	0.5 V
Ch 6 AC + F + G	SSG	006	6	0.6 V
Ch 7 BC + D + G	SSO	007	7	0.7 V
Ch 8 BC + E + G	SUS	010	8	0.8 V
Ch 9 BC + F + G	SUU	011	9	0.9 V
Ch 10 DE + A + G	SUR	012	10	1.0 V
Ch 11 DE + B + G	SUW	013	11	1.1 V
Ch 12 DE + C + G	SUD	014	12	1.2 V
Ch 13 DF + A + G	SUK	015	13	1.3 V
Ch 14 DF + B + G	SUG	016	14	1.4 V
Ch 15 DF + C + G	SUO	017	15	1.5 V
Ch 16 EF + A + G	SRS	020	16	1.6 V
Ch 17 EF + B + G	SRU	021	17	1.7 V
Ch 18 EF + C + G	SRR	022	18	1.8 V

*When a channel is energized 0.05 V is added to the channel reply voltage.

Alternatively, if voltage verification is used, that voltage will return to its standby value. This information (code or voltage) is transmitted back, to indicate completion of the command function.

With this overview in mind, this report will now examine in greater depth the decoding and code generation functions involved. The channel 1 tones will be used as an illustrative example.

3.3 Tone Decoding

Table 2 shows that tones A, B, D, and G are required to activate channel number 1.

Tones A and B are transmitted first by the control station. Referring to Figure 3, the overall block diagram for the command selector, one sees that these two tones are detected by the A and B tone filters. The tone filter outputs are then amplified, rectified, and integrated to provide the A and B inputs to the tone

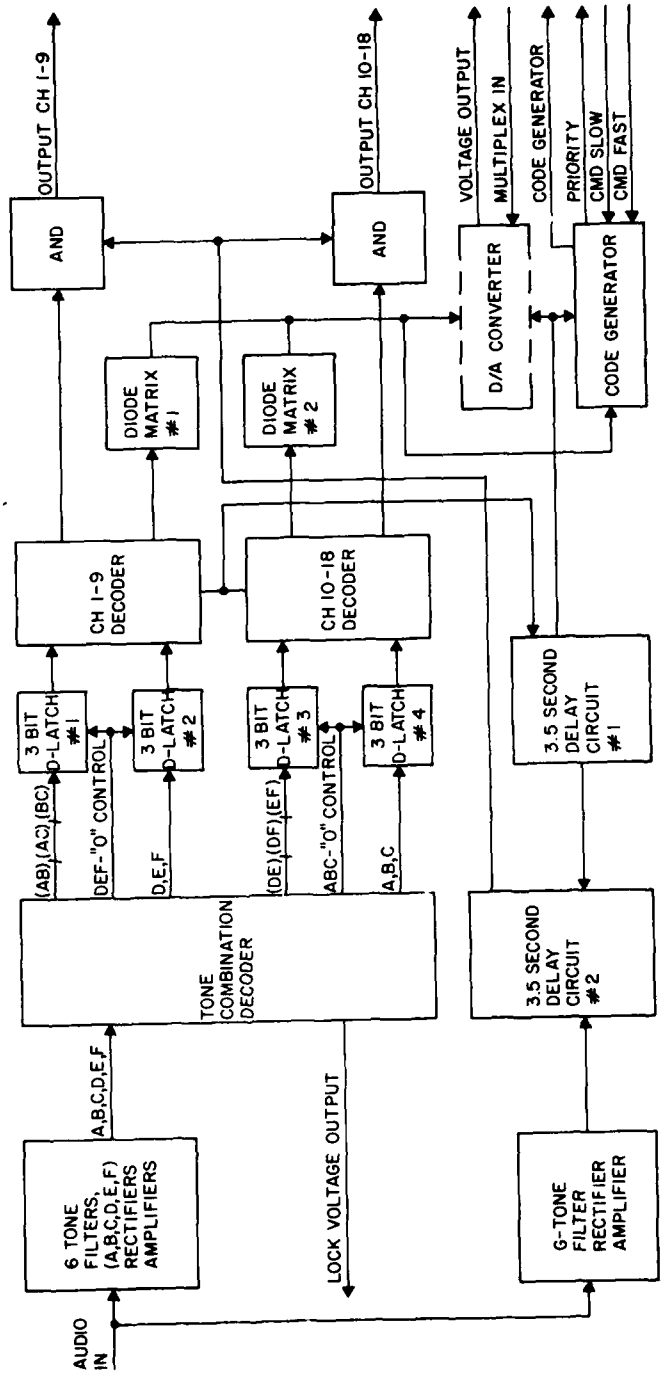

Figure 3. BCS-18A Selector Block Diagram

combination decoder. This decoder generates the AB and ABC-"0" outputs. AB is transferred to the output of the No. 1 D-latch. The ABC-"0" output disables the No. 3 and No. 4 D-latches to prevent the selection of channels 10 through 18.*

As previously mentioned, the control station disables the tone combination of A and B after 2 sec, and, at the same time, initiates the transmission of tone D to the balloon. This tone is also filtered, amplified, rectified, and integrated by the command selector, whose tone combination decoder provides outputs D and DEF-"0". Because the dc outputs from the tone filters have a small dropout delay when a tone is removed, the outputs for tones A, B, and D are all present simultaneously for a short time. The AB output of the tone combination decoder feeds latch No. 1, and the D output feeds latch No. 2. After a small time delay, the DEF-"0" output activates the control of these two latches, to lock in the information (AB + D) already received and to prevent further data transfer into them.

The outputs of latch No. 1 and latch No. 2 go to the channel (1-9) decoder, which selects the relay for channel 1. In addition, the decoder starts a 3.5-sec time delay (controlled by time delay circuit No. 1) and provides an input to diode matrix No. 1. The diode matrix is the controlling item in the production of the channel selection verification code or voltage, described in detail in Section 3.4. This code or voltage is generated when the 3.5-sec delay ends and is transmitted to the ground control station, to confirm, in this case, selection of channel 1.

The channel selection verification is received by the ground station where the channel indication is displayed or printed. The ground station operator then adds the tone G to the modulating signal of the command transmitter. When received and decoded at the balloon, this tone initiates a second 3.5-sec delay, controlled by delay circuit No. 2. At the end of this delay, the channel 1-9 AND gate is activated and channel 1 becomes energized, to execute the desired remote-controlled function. Once the remote function has been performed, the control station operator removes the G-tone and then the D-tone from the modulation of the ground transmitter. This initiates a repeat verification transmission from the balloon, to indicate that the command channel has been deactivated. The command selector is now ready to accept other commands.

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*The ABC-"0" and DEF-"0" outputs are also used to control the lock voltage output. This output controls a dual frequency scanning command receiver, which normally samples two radio frequency signals. If one of these signals contains one of the command selection tones (A, B, C, D, E, F), the lock voltage stops the scanning action and the receiver will lock to the command signal. (See Section 4.2.)

3.4 Verification Modes

3.4.1 TYPES OF MODE

The verification modes generated by the command selector to confirm channel selection and channel deactivation can take one of two forms (serial codes or voltage levels), depending on the kind of verification board actually installed in the channel selector (see Sections 4.4 and 4.5). If a serial code is used, the decimal equivalent channel number is recorded or displayed at the control center. If the voltage level output is used, a voltage output is displayed or recorded per the voltage verification format of Table 2.

The serial codes will be described first, with the channel 1 verification code used as the example. (The voltage level output will be discussed in Section 3.4.3.)

3.4.2 SERIAL CODES

Referring to Figure 3, one sees that the command selector's diode matrix No. 1 supplies binary inputs to the code generator when a serial verification code is to be used. The code is actually generated: (1) at the end of the first 3.5 sec time delay, the "selection" delay described above, and (2) when the G-tone has been removed by ground control. It begins and ends with a synchronization pulse, with two identical 9-bit code sequences in between.

Serial codes are either 3-letter Morse codes (in the slow reply mode) or 3-digit octal codes (in the fast reply mode). During the short channel-reply time period, the output from the code generator is given priority and switches the modulation of the data transmitter from its normal input (for example, an encoder) to the channel verification code. This is a disadvantage of the serial code in that it interrupts the transmission of data from other sources in the balloon system.

Serial verification codes have been chosen so that the decimal equivalent of a particular output code corresponds to a channel number. Table 2 shows that the output code for channel 1 is SSU in Morse code or 001 in octal code. These outputs represent the number 1 in the decimal system. Table 2 also indicates that eight Morse code letters, used three at a time in various combinations, can account for all 18 channel numbers. Table 3 shows these individual letters and their equivalent numbers in other systems.

3.4.3 VOLTAGE VERIFICATION (VV) OUTPUT

The serial codes can be replaced with a voltage verification (VV) output if desired. In this case, the diode matrix shown on Figure 3 provides binary inputs to the digital-to-analog (D/A) converter on the voltage verification board, instead of to the serial code generator. With the VV board installed, the number of the selected channel is represented by an output whose value (in volts) is nominally 1/10th the numerical value of the channel. For example, the voltage output, when

Table 3. Morse Code Equivalent Numbers

Letter	Characters	Binary	Octal	Decimal
S	dot-dot-dot*	000	0	0
U	dot-dot-dash	001	1	1
R	dot-dash-dot	010	2	2
W	dot-dash-dash	011	3	3
D	dash-dot-dot	100	4	4
K	dash-dot-dash	101	5	5
G	dash-dash-dot	110	6	6
O	dash-dash-dash	111	7	7

*Dash = 1, Dot = 0

channel 1 is selected, is 0.1 V. (Table 2 shows the voltage outputs for all channels.) Later, when a channel is energized, 0.05 V is added to the verification voltage.

Normally, the output from the VV board (see Section 4.5) is a voltage applied to the "multiplex in" terminal which, like temperature or battery voltage does not have to be monitored continuously. The terminal can also be grounded. When a channel is selected, the output voltage switches to the output of the D/A converter. That voltage, as measured by an onboard PCM encoder, constitutes the verification output transmitted to the control station.

The time delays and the decoding components on the VV board are the same as on the code generator board. However, the VV board time delays can be eliminated by a switch, when necessary. This option is likely to be exercised if command receivers operating at very-high or ultra-high frequencies (VHF or UHF) are used, since those frequencies are tightly controlled and the distance over which they are effective is limited to line of sight. In the case of HF signals, which are more likely to encounter spurious tones and interference, the time delays provide much-needed channel security.

4. THEORY OF OPERATION

4.1 General

This section describes the operation of the command selector in detail by following the signals and logic levels through all four circuit boards.

The interwiring diagram (Figure 4) shows that command selector inputs and outputs are fed through connectors P1 (15 pins) and J1 (25 pins), respectively. The diode CR1 provides reverse polarity protection. Regulator A1, which accommodates supply voltages of 12 to 30 V, furnishes 12 V to all circuit boards. It also provides overvoltage protection and limits current to 1.5 A.

The command selector's four printed circuit boards ((1) Tone Decoder, (2) Channel 1-9 Selector, (3) Channel 10-18 Selector, (4) Serial Code Generator or Voltage Verification) plug into the connectors J2 through J5. Each board uses a unique key slot so that damage and mating with the wrong connector can be prevented. These boards will now be described in turn.

4.2 Tone Decoder Board

Figure 5, the tone decoder schematic diagram, shows that the audio signal from the command receiver is applied to pin Y of the tone decoder board. This pin feeds six tone filters (FL-A through FL-F). All are resonant reed electronic bandpass filters, with sharp selectivity and very good temperature stability.

A typical resonant reed tone filter consists of two coils coupled by a small magnet attached to the end of the resonant reed. The input or drive coil and the output or pickup coil are identical and interchangeable. There is no output from the pickup coil unless the signal applied to the drive coil is of sufficient amplitude and is at the resonant frequency of the reed. With the proper input signal, the reed starts to vibrate and the motion of its magnet induces a sinusoidal voltage in the pickup coil.

The pickup (output) coils of the resonant reed tone filters are all connected to an array of operational amplifiers, A1 through A6, also mounted on the Tone Decoder Board. The C-MOS output stages of these amplifiers can switch (within a few millivolts) between the supply voltage and ground. In their normal state (no applied input voltage), the amplifiers are biased with a dc offset voltage,* which keeps their outputs saturated at ground potential, to inhibit the amplification of noise and low-level signals.

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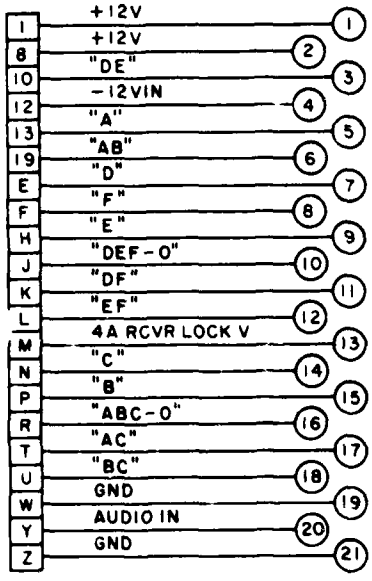
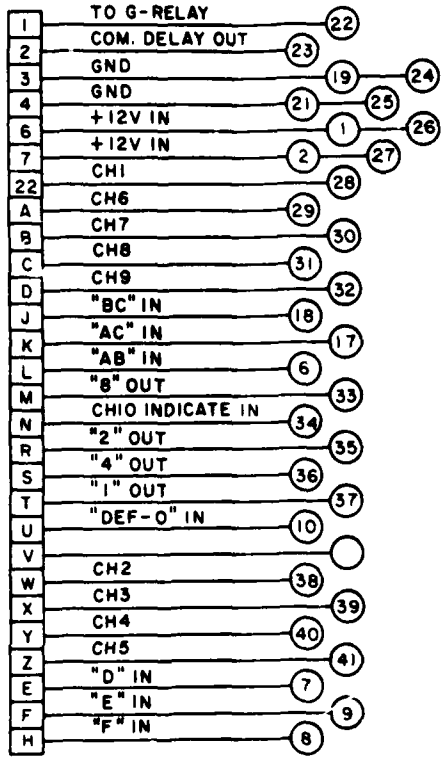
*The dc offset voltage is produced by the current through the pickup coils which are connected between the inputs of the amplifiers. The Zener diode CR2 (5.1 V), the pickup coil, which has a resistance of 400 ohms, and an 8.2K-ohm resistor form a biasing network for each amplifier. This combination produces an offset voltage of 237 mV. (5.1 V × 400/8200 + 400)

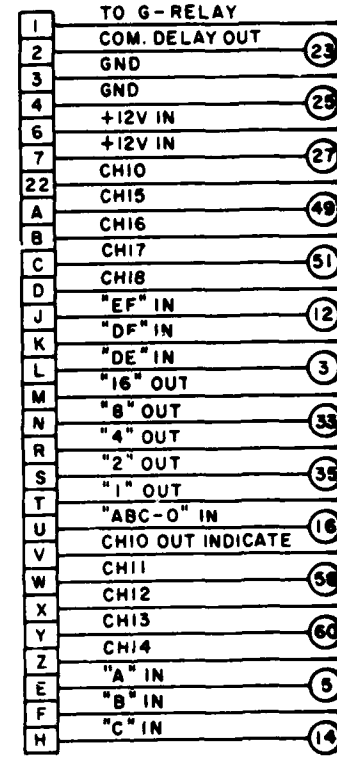
J2 R644
TONE DECODER

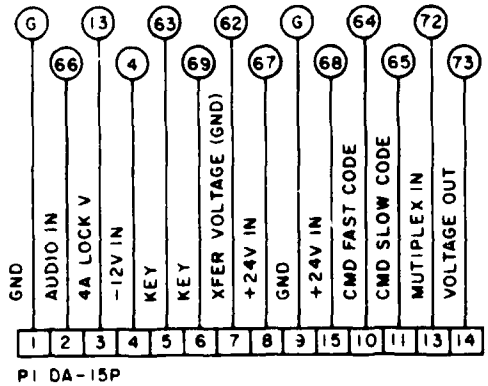


J3 R644
CHANNEL 1-9 SELECTOR

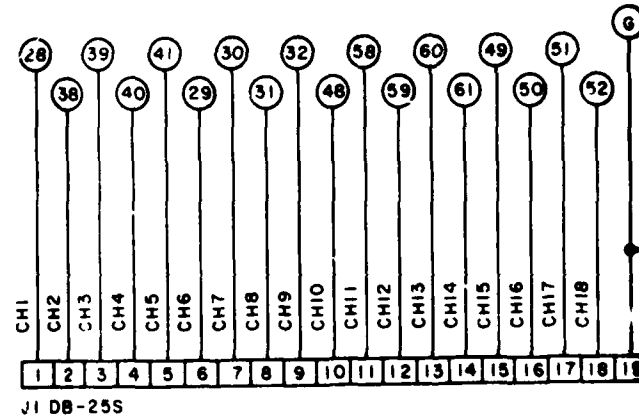


J4 R644
CHANNEL 10-18 SELECTOR

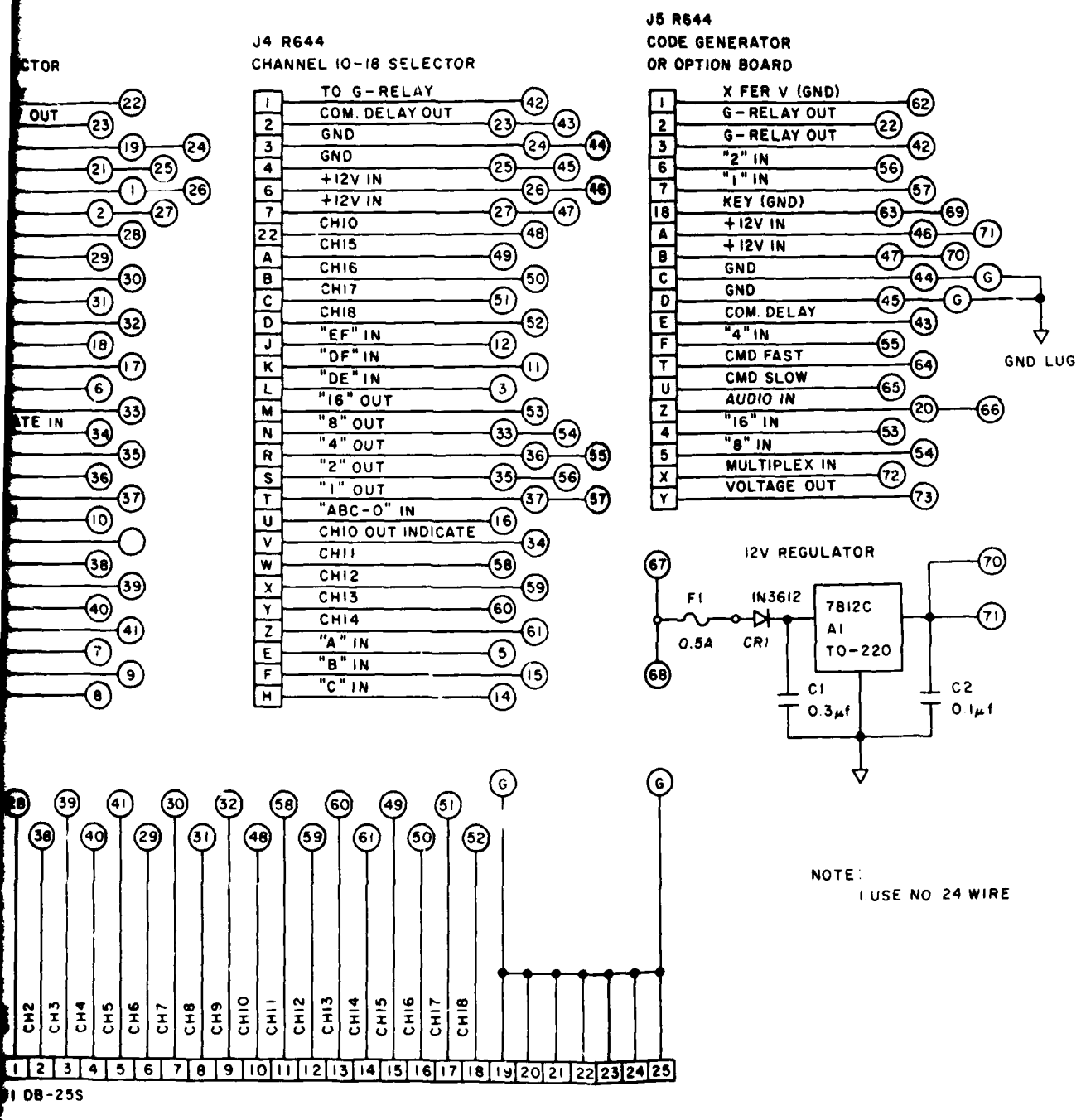




P1 DA-15P

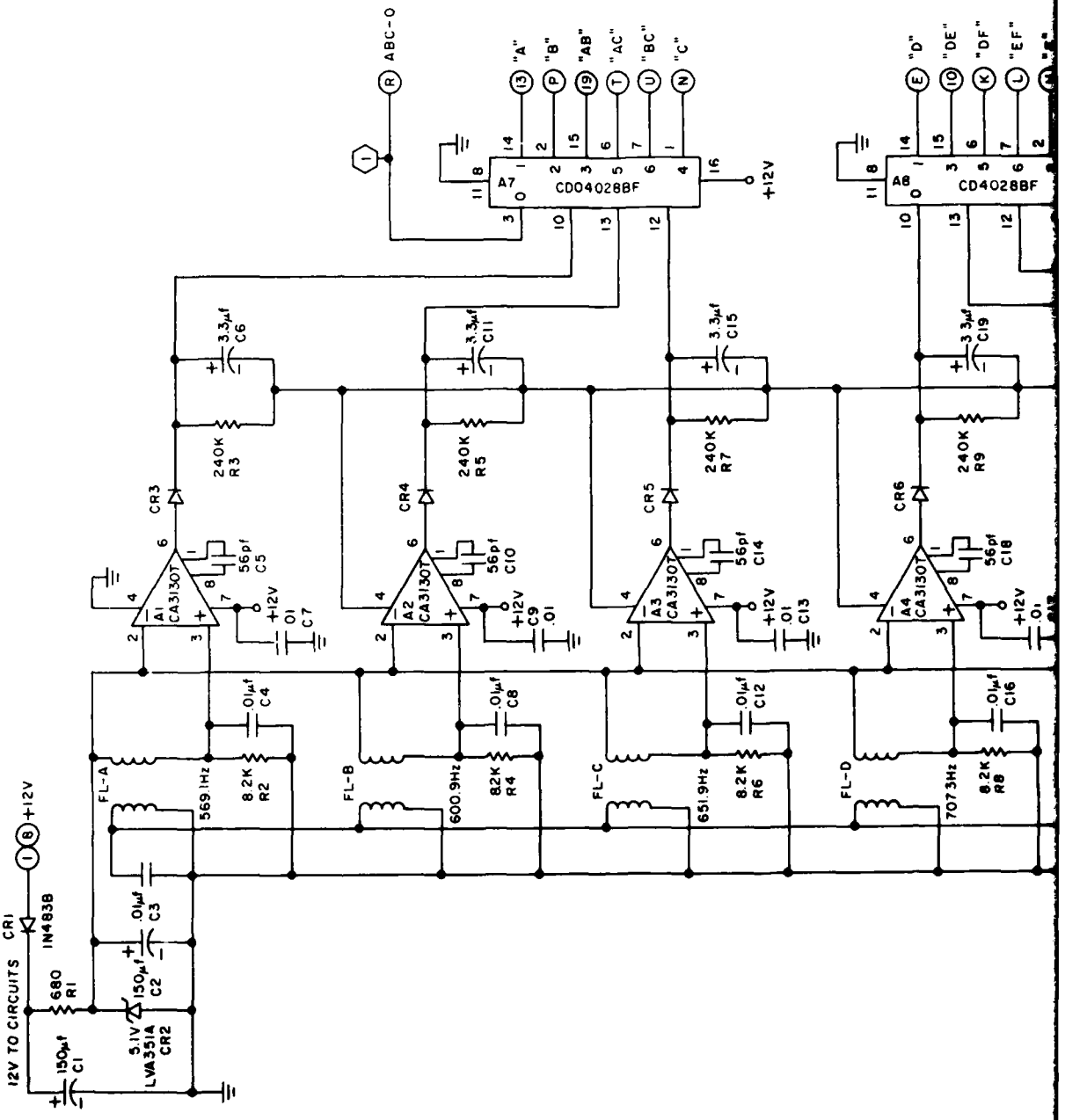


J1 DB-25S



NOTE:
USE NO 24 WIRE

Figure 4. BCS-18A Selector Interwiring



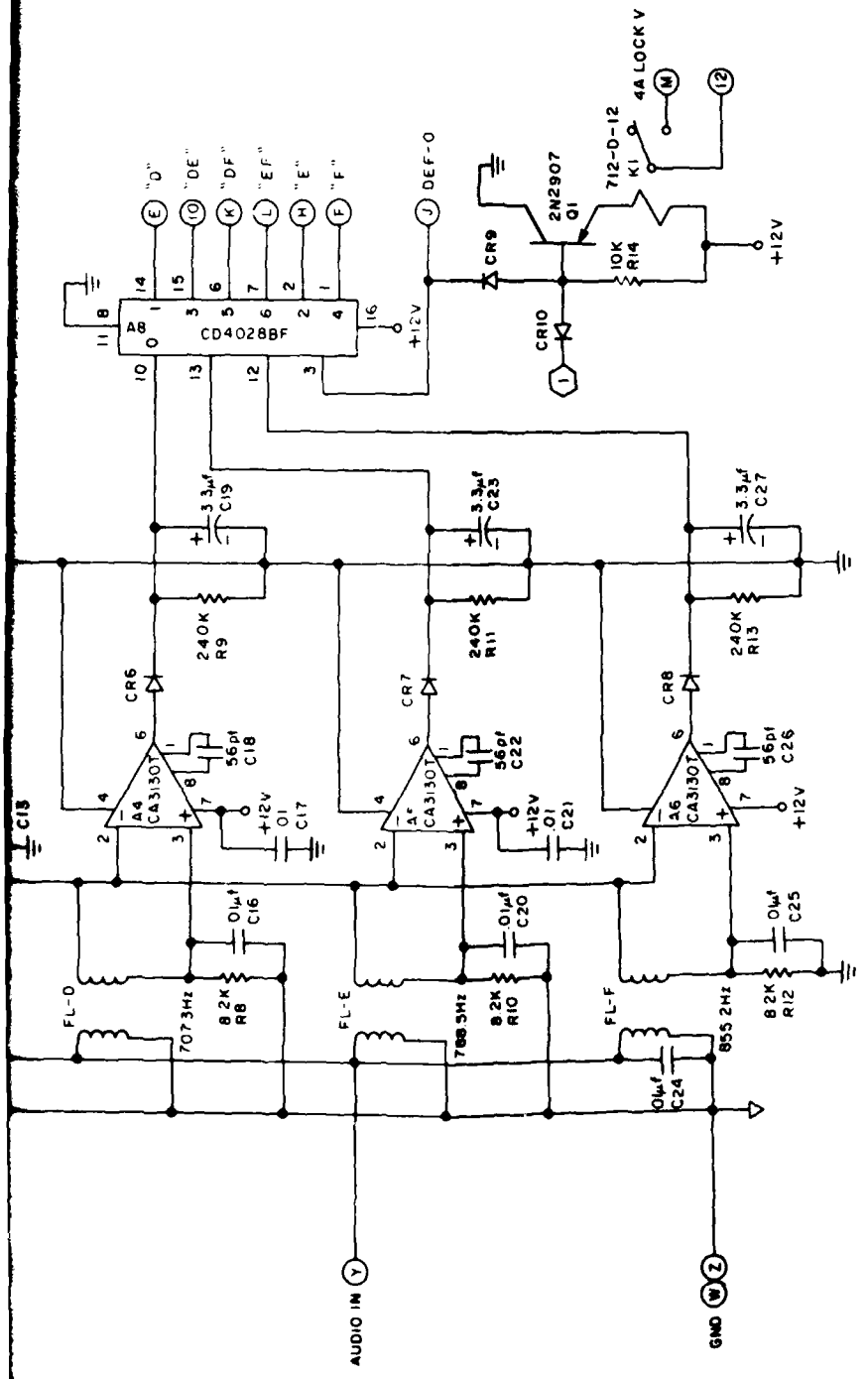


Figure 5. Tone Decoder Schematic

When the output of a tone filter exceeds the offset voltage, its associated amplifier produces a square wave output with an amplitude equal to the supply voltage. The decoding of Tone A is a typical case: The voltage in the pickup coil of filter FL-A is applied to the noninverting input of amplifier A1. The resulting square wave is rectified by CR3 and integrated by C6 (3.3 μf), which feeds A7, the tone combination decoder for tones A, B, and C. (A8 is the tone combination decoder for tones D, E, and F.)

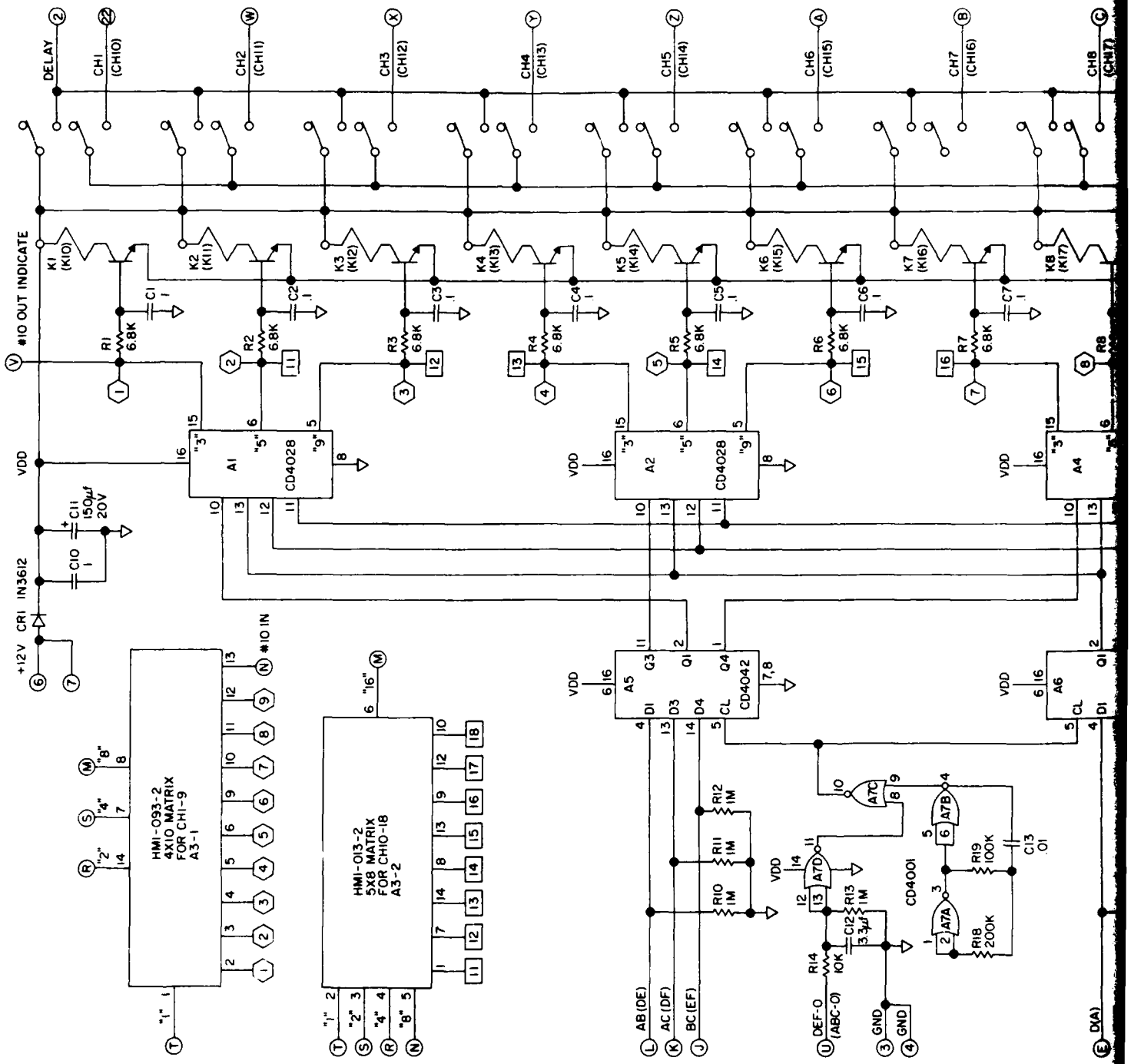
Tone A decoder circuit components CR3, R3, and C6 constitute a fast charge/slow discharge system, which is an important feature during channel acquisition, as will be discussed in the sections on the channel selector boards (Sections 4.3 and 4.4). The decoder circuits for the other tones are identical.

A7 and A8 are employed as binary to octal decoders here, and they provide the dual and single tone inputs (for example, AB and D) to the channel selector boards. Decoders A7 and A8 also furnish ABC-"0" and DEF-"0" outputs, respectively. When any one of the six selection tones is received, one of these outputs (ABC-"0" or DEF-"0") activates transistor Q1. Q1 then energizes the relay, K1, whose "lock voltage" stops the scanning action of the dual frequency command receiver, as described in the footnote to paragraph 3.3.

4.3 Channel Selector Circuit Boards

The selector circuits for the 18 command channels are shown on the composite schematic diagram of Figure 6. Actually, two separate circuit arrangements are involved, each on its own circuit board. One decodes command channels 1 through 9; the other, channels 10 through 18. The two boards are physically identical except that each uses a different diode matrix for channel verification. (The key slots on the edge connectors are also different.) The logic inputs of the two selector circuit boards are furnished by the just-described tone decoder board. On Figure 6, the inputs for channels 1-9 are shown above the input lines, while those for channels 10-18 are shown in parentheses below the lines.

Components A5 and A6 on Figure 6 are present on both selector circuit boards. They represent the 3-bit D latches discussed earlier in Section 3.3. (See Figure 3, D-latches No. 1 through No. 4. A5 represents latches No. 1 and No. 3; A6, No. 2 and No. 4.) Logic levels (0 or 1) on the "D" inputs (D1, D3, D4) of the clocked "D"-latches A5 and A6 are transferred to their respective outputs (Q1, Q3, Q4) during the positive input clock cycle, and the information is retained or latched at the outputs when the clock inputs return to low and remain low. The data transfer and latching function for these latches is controlled by the input on selector board terminal U (ABC-"0" or DEF-"0"). This input is inverted by A7D, which controls the NOR gate A7C, whose output feeds the clock signal to the latches A5 and A6.



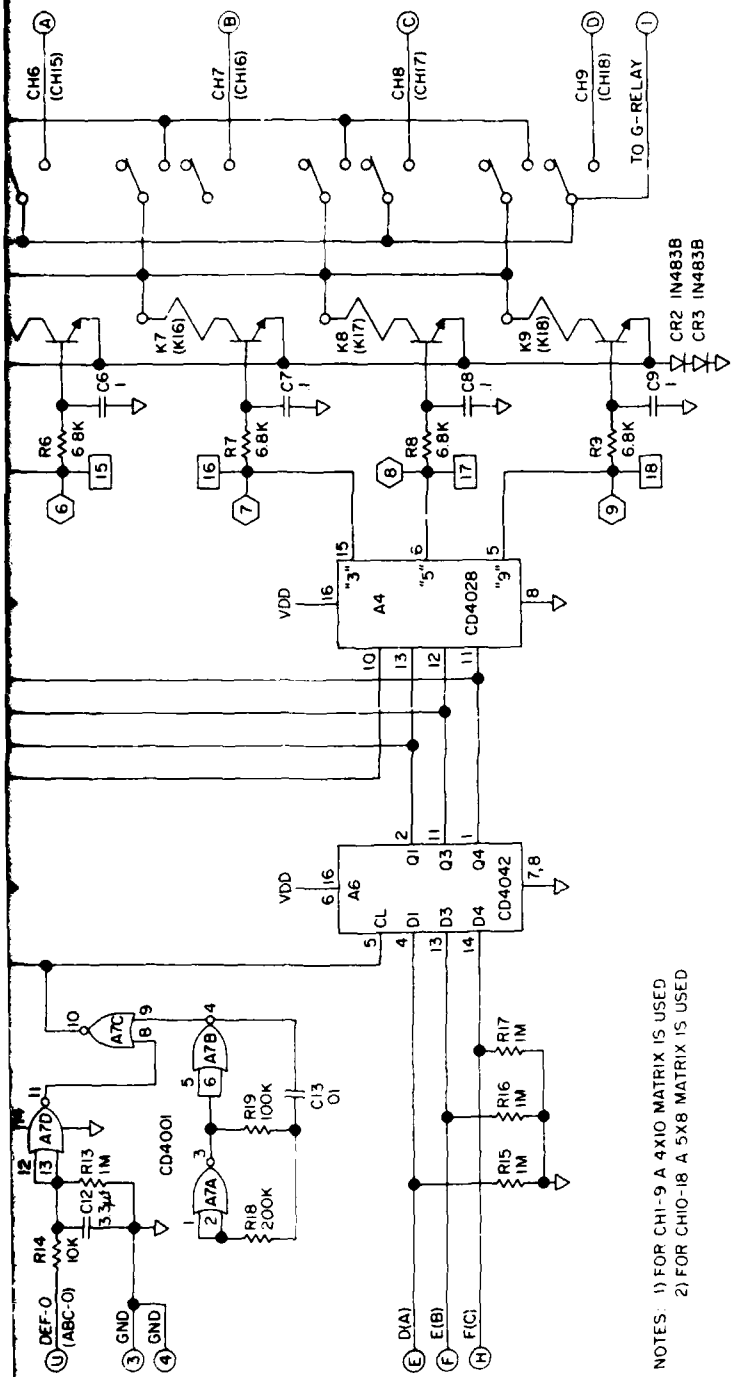


Figure 6. Composite Channel Selector Schematic

The clock signal for these latches is generated by the circuit of A7A, A7B, R18, R19, and C13. The output frequency of the clock generator is approximately 1000 Hz (T = 1 msec), which is applied to the "NOR" gate A7C.

When the latch control input on terminal U is high, the "NOR" gate A7C is allowed to pass the oscillator signal to the clock inputs of A5 and A6, but when the control input is low, A7C becomes disabled and its output is forced low. Therefore, data transfer occurs during the time when the control input (terminal U) is high, and the data is latched at the outputs of A5 and A6 when the control input is low.

During the standby mode when none of the command tones are received, both ABC-"0" and DEF-"0" inputs to the two selector boards are high, while the rest of the tone and tone combination inputs are low. This causes continuous data transfer of all zeros to the outputs of A5 and A6, thus no channel selection can occur.

To illustrate the channel selection process, examine the case of selecting channel 1. At first, when tones A and B are received, the inputs AB and DEF-"0" are high, while ABC-"0" and all other tone and tone combination inputs are low. ABC-"0" controls the latches A5 and A6 on the selector board for channels 10-18, and DEF-"0" controls A5 and A6 for channels 1-9. The ABC-"0" input (low) latches the outputs of A5 and A6 for channels 10-18, and also inhibits further data transfer. Because all inputs to the selector board for channels 10-18 were low before ABC-"0" switched to low, all outputs of A5 and A6 are also low, which prevents channel selection on this board.

The AB input (high) on the selector board for channels 1-9 is transferred to the output (Q3) of A5 because DEF-"0" is still high. Shortly thereafter, tone D is received and tones A and B are removed (controlled by the command tone generator). The D input goes high, and the DEF-"0" input switches from high to low instantly while the AB input stays high for a short period of time, the length of which is controlled by a dropout delay circuit on the tone decoder board. During this time, the clock signal to A5 and A6 is still enabled because the DEF-"0" latch control signal is delayed by the time constant of R14 and C12 (10 K and 3.3 μf), and the D input is transferred to Q1 of A6; once the voltage across C12 decreases to the switching point voltage of A7D, the output of A7C is forced low. This latches the outputs of A5 and A6 on the selector board for channels 1-9. These outputs remain latched for as long as the D signal is applied; however, the E and F signals will provide the same function after A5 and A6 become latched.

The outputs of latches A5 and A6 provide the binary-weighted inputs to the three binary-coded decimal (BCD) to decimal decoders A1, A2, and A4, which perform the actual channel relay selections and also provide the inputs to the diode matrix. Each BCD-to-decimal decoder has one input from A5, which is

derived from a dual-tone combination, and three inputs from A6, generated from single tones. The dual-tone combination inputs have a binary-weighted value of 1, while the single-tone inputs are weighted as 2 (A or D), 4 (B or E) and 8 (C or F). From these input combinations of 1 and 2, 1 and 4, and 1 and 8, the outputs for the numbers "3," "5," and "9" are generated by each BCD-to-decimal decoder. A1 controls the first three channels, A2 the second three, and A4 the last three channels on each selector board.

For the case of channel 1, A1 decodes the inputs AB and D with binary values of 1 and 2. The output "3" of A1 supplies the base current through R1 to the transistor of relay K1, which is then activated, and one set of contacts switches the supply voltage to terminal 2. The voltage is used by the code generator or voltage verification board to start a 3.5-sec time delay circuit. The other set of contacts will energize the selected channel once the G-tone relay has been activated (ground closure).

The other channels are selected in the same manner by substituting the appropriate tone combinations shown on Table 2. All 18 channel relays have a double pole/double throw (DPDT) contact arrangement. The arms of one set of contacts are connected to the supply voltage, and the normally open contacts of the same set are paralleled and connected to terminal 2, which starts the same 3.5-sec time delay circuit on the code generator or voltage verification board. Therefore, all time delays are the same, no matter which channel is selected. The arms of the other set of contacts are connected to the output of the energize (G) relay so that channel output (ground closure) occurs only when the energize (G) relay is also activated. All relay transistors and spike suppression diodes (not shown on the schematic) are mounted inside the relay case.

All emitters of the relay transistors are connected in series with diodes CR2 and CR3 to ground. This increases the noise immunity for relay activation from 0.7 V (one base-emitter junction) to 2.1 V, because each diode also provides a forward voltage drop of 0.7 V. To further increase noise immunity for stray radio frequency signals generated in or around the balloon control package, every base of the relay transistors is bypassed by a 0.1-μf capacitor (C1-C9).

Figure 6 shows that the BDC-to-decimal decoders A1, A2, and A4 also furnish the inputs to the diode matrices A3-1 and A3-2. The numbers 1-9 in hexagons at the outputs of A1, A2, and A4 are connected to the corresponding numbers on the diode matrix A3-1 on the selector board for channels 1-9. Likewise, the numbers 11-18 in rectangles are interconnections between the decoders and the diode matrix A3-2 for channels 11-18. The reply input for channel 10 is connected from terminal V of the channel 10-18 selector board to pin N of the channel 1-9 selector board, where it becomes an input to A3-1. The corresponding matrix outputs ("1" to "1", "2" to "2", etc.) from the two selector boards are paralleled and connected to the

code generator or voltage verification board, where they are used to determine the reply codes or voltage outputs.

Figure 7 is the schematic diagram of the two diode matrices already programmed. The pattern of each matrix is formed by burning out the fusible links on these diodes which are not needed for the desired output. Each matrix is programmed to perform decimal-to-binary conversions. The numbers in the hexagons are the decimal inputs, and the numbers in circles are the binary weighted outputs. When a channel is selected (channel input high), the binary weighted outputs are also high wherever a diode is connected between the column input and the row output. For example, the matrix output for channel 11 is high in the "1," "2," and "8" output positions and low for the "4" and "16" output positions, which is the binary number of 01011. This number will be used to generate the code output for channel 11.

4.4 Code Generator Board

4.4.1 GENERAL CONSIDERATIONS

The code generator board is used interchangeably with the Voltage Verification board described in Section 4.5. When the balloon control package does not include a PCM encoder, the code generator board is used to verify command channel selection and execution. The circuits on this board control two separate 3.5-sec time delays (the selection delay and the energize or execution delay), generate the channel verification codes, decode the energize tone G, and provide the ground closure for the final output of the selected command channel. The sequence in which these functions occur will now be described.

When a channel becomes selected, an input from either one of the selector boards provides the start signal for the 3.5-sec selection delay circuit. At the end of 3.5 sec, the code generator is activated. The code sequence starts with a small pause, followed by a synchronization pulse and another pause. The pulse code for the selected channel is then generated, followed by another pause, repetition of the same pulse code and another pause. A second synchronization pulse and another small pause end the sequence.

A 9-bit binary pulse code, which represents the selected channel number, is utilized. Zeros are represented by unit pulses and ones are represented by pulses with a duration of 3 unit pulses. A pause with a duration of 3 unit pulses is formed between every three pulses. This provides the appearance of a Morse code in the slow reply mode, or an octal code in the fast mode. The speed of the reply codes is selectable by command, which provides four different clock frequencies for the code generator. In the slow reply mode, a Morse code with three letters per code is used; in the fast reply mode (octal code), the basic speed of the code is multiplied

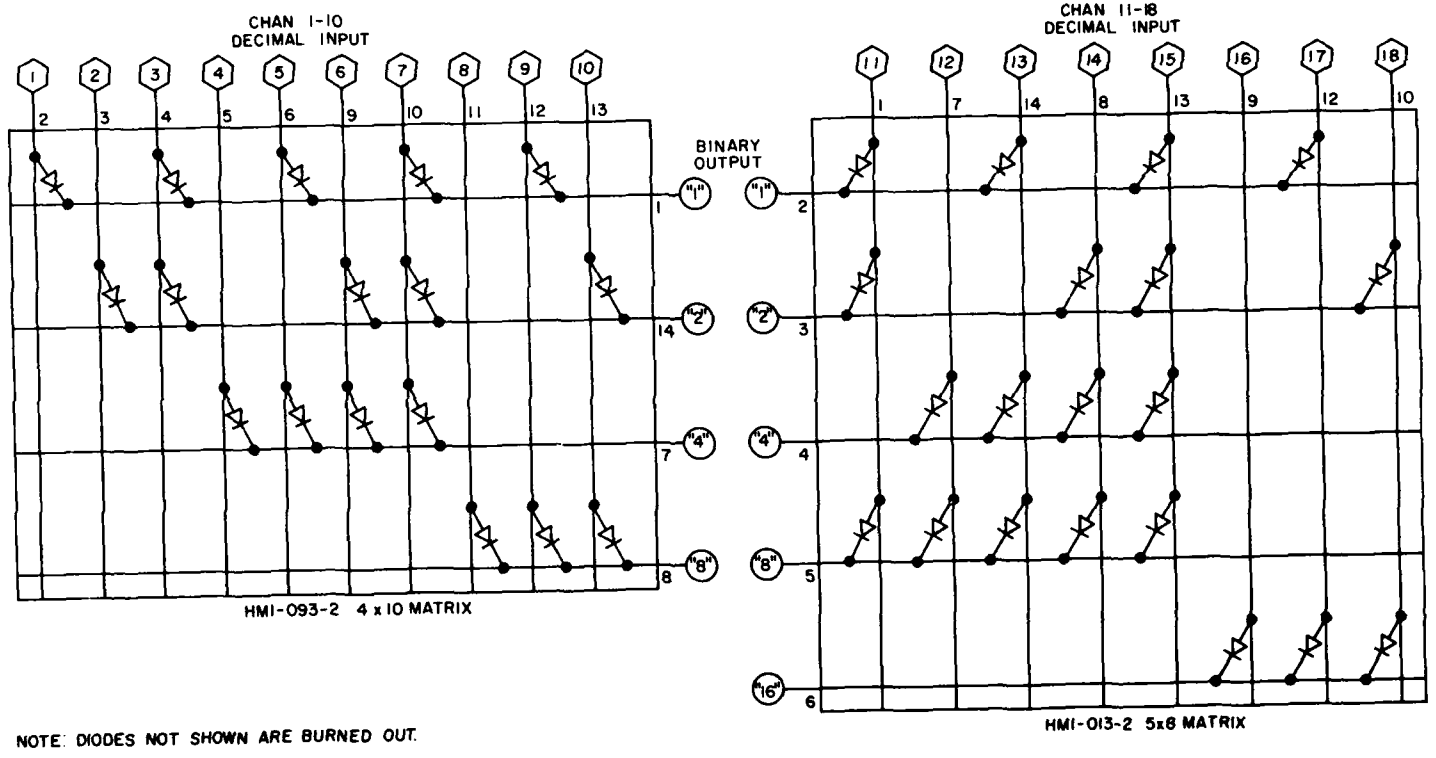


Figure 7. Matrix Program Schematic

by either 8, 16, or 32, but the format of the code is retained. The pulse code is transmitted to ground control, where it is decoded and displayed or printed as the selected channel number.

After verification of channel selection by ground control, the energize tone G is added. This tone is detected and starts the 3.5-sec energize delay circuit on the code generator board. After the delay, the energize relay is activated to provide the ground closure to the selected channel relay. This energizes the remote-controlled function.

When a command channel is to be deactivated, the energize tone G is removed. This starts the same verification code described above, and also deactivates the energize relay. After the code has been received, ground control removes the channel select tone, and the command channel becomes deactivated. The details of the time sequences involved and the code generation will now be described.

4.4.2 TIMING SIGNALS

Reference should be made to the schematic diagram of the code generator board in Figure 8. All timing signals on this board are derived from a 74.565-kHz oscillator formed by the crystal Y1, the inverters A17C and A17D, and their associated resistors. This particular frequency was chosen to be compatible with the Encoder/Timer unit, which is usually part of the balloon control and data package. The timer portion of that unit serves as a backup system for bringing about balloon termination. It, too, uses a clock frequency of 74.565 kHz, which produces one pulse per hour when divided by two 14-stage binary counters $((74,565 \times 3,600) \div 2^{28})$. The encoder portion of the Encoder/Timer unit generates a 9-bit pulse code, which is controlled by the same timer clock. Because the format and pulse durations of this code are identical to the code generated by the command selector, code detection, translation, and display at the ground station are the same for both units.

The crystal oscillator provides the clock input to the 14-stage counter A10, whose outputs distribute the timing signals to the code generator and the time delay circuits. The periods of those outputs used and their functions are listed in Table 4.

The periods of Q13, Q10, Q9, and Q8 are the same as the unit pulses used in the code format for the various code speeds. They represent the binary zeros, while ones have a pulse width of 3 unit pulses.

4.4.3 RESET PROCEDURE

All counters and flip-flops used on the code generator board are reset (disabled) with a logic 1 applied to their reset lines, and they are "enabled" or ready to count when the reset input is 0. When power is first applied, every counter and flip-flop (A6, A7, A8, A4 and A3B, A3A, A5) which play a role in the code generation process becomes reset.

Table 4. A10 Output Information

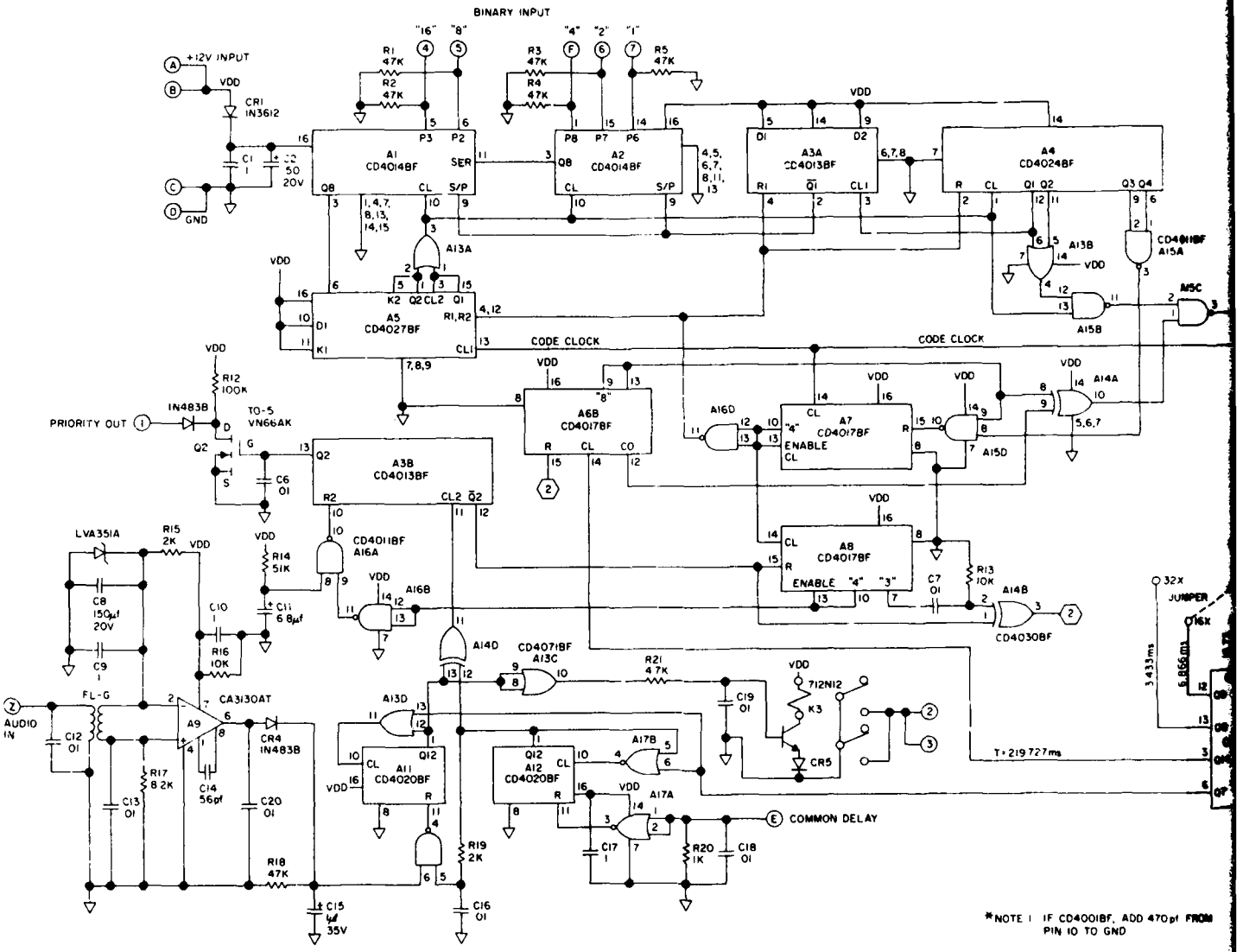
A10 Outputs	Period	Use (Clock input for)
Q14	219.72 msec	Synchronization pulse
Q13	109.86 msec	Slow code (Morse code)
Q10	13.732 msec	Fast (8X) code (octal code)
Q9	6.866 msec	Fast (16X) code (octal code)
Q8	3.433 msec	Fast (32X) code (octal code)
Q7	1.7166 msec	3.5-sec delay circuits

Initially, when power is applied, the voltage across the capacitor C11 is at ground potential (logic 0). This forces the output of A16A high, which resets the flip-flop, A3B. The output of A3B is now 0 on Q2 and 1 on $\overline{Q2}$, which resets decade counters A8 and A6, using the exclusive OR gate A14B for resetting A6. The "8" output of A6 (logic 0) is inverted by the NAND gate A15D which resets A7. The "4" output of A7 (logic 0) is inverted by A16D, which applies a logic 1 to the reset inputs of the J-K flip-flop A5, the flip-flop A3A, and the seven-stage counter A4. This reset sequence is accomplished almost instantly when power is first applied. Shortly thereafter, when the voltage across the capacitor C11 reaches the supply voltage, the output of A16A switches from high to low, which enables A3B. Flip-flop A3B is now ready to accept a clock input to start the code generation. The necessity for this multiple feedback reset procedure will become more apparent after the description of the verification code time sequence.

A12, a 14-stage counter, is used to generate the 3.5-sec selection delay. This counter is disabled or reset by the pull-down resistor R20, which forces the output of the NAND date A17A high. Because A12 is disabled or reset, Q12 of A12 is low, which is inverted by A16C, keeping A-11 disabled. A-11 is also disabled by a logic 0 on the other input (pin 6) to A17A. This input is only high when the energize tone G is received and decoded by A9 and its associated components, otherwise it is low. A-11 becomes enabled when both the inputs to A17A are high. This only occurs after the selection time delay when Q12 of A12 is high and the tone G is decoded at the same time. After A-11 becomes enabled, it generates the 3.5-sec energize delay for final channel activation.

4.4.4 SELECTION TIME DELAY (3.5 SEC)

The circuit formed by the 14-stage counter A12, the NOR gate A17B, and the inverter A17A control the 3.5-sec selection time delay. When any one of the 18 channels becomes selected, the output from the channel selector boards applies a



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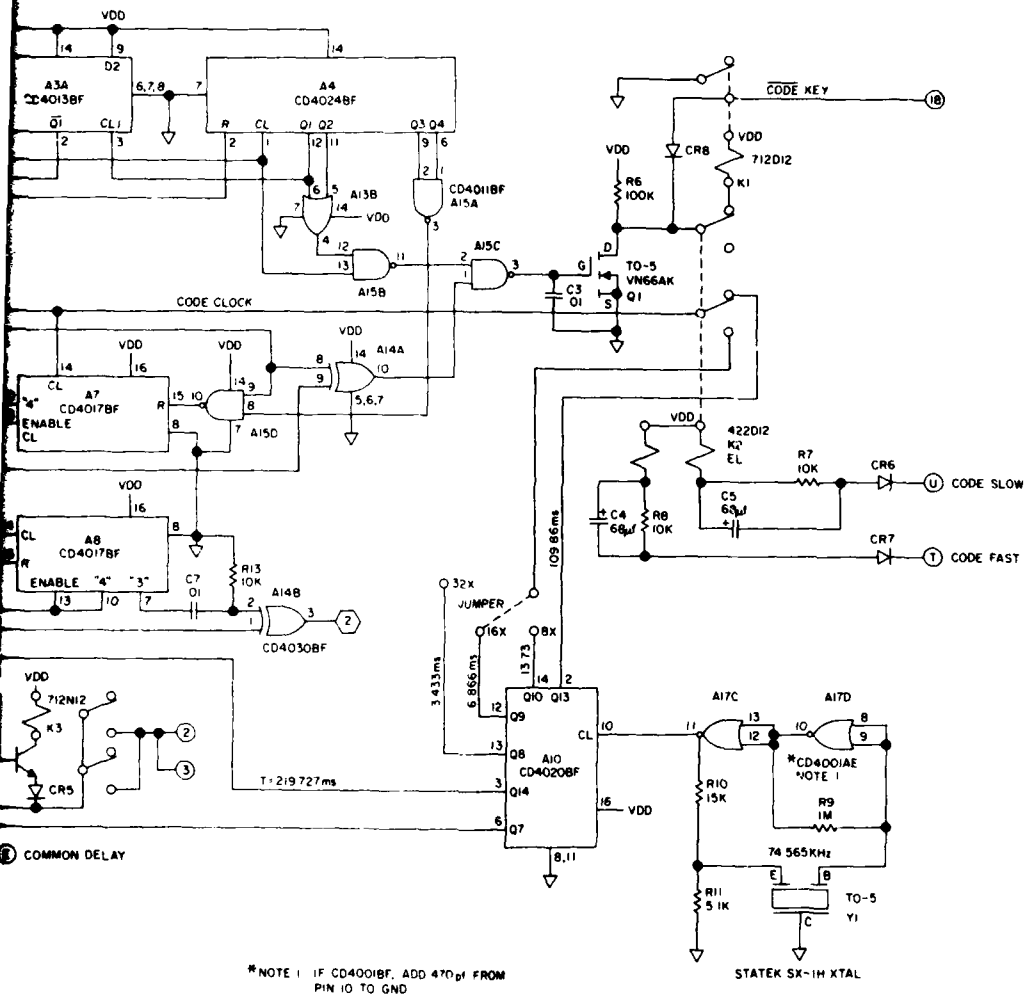


Figure 8. Code Generator Schematic

2

logic 1 to pin E (common delay) on the code generator board. This signal is inverted by A17A, and A12 becomes enabled, thereby initiating the 3.5-sec delay.

The clock signal for A12 is furnished by Q7 of A10 and is gated by the NOR gate A17B. The frequency of this signal is 582.5 Hz (74.565 kHz $\div 2^7$), which provides the period (T) of 1.7166 msec. After 2^{11} (2048) input pulses, or a time delay of 3.5156 sec (2048 × 1.7166 msec), the Q12 output of A12 switches to logic 1 and remains 1 as long as the input on pin E (common delay) is high, because the NOR gate A17B is disabled by a 1, thereby disabling the clock input to A12. The logic 1 on Q12 of A12 also enables A16C, which controls A-11, and the positive transition of Q12 starts the verification code sequences via the exclusive OR gate A14D, which provides the clock input to A3B. A3B plays a key role in the code generation process.

4.4.5 CODE GENERATION

4.4.5.1 Initial Considerations and Facts

All decade counters (A6, A7, A8) are incremented by a positive (rising) transition at their clock inputs. The "clock enable" input (pin 13) of these counters is connected to one of the decoded outputs: "8" for A6, "4" for A7, and "4" for A8. This has the effect that the counters will count input pulses until the decoded output where the "clock enable" is connected goes high, and that output will remain high until the counter is reset again.

The counter A4 is incremented by a negative (falling) transition on its clock input. It is used to generate the pauses between every three code pulses and also to sense the end of the 9-bit code.

The flip-flop A3A controls the mode of operation of the 8-stage parallel or serial input-serial output shift registers A1 and A2. These shift registers convert the code-determining parallel binary inputs from the channel selector boards into a serial output on Q8 of A1. They operate in two modes: When the serial-parallel control input (S/P) is high, the data on the parallel input lines (P1-P8 for each) is transferred or jammed into the shift register synchronously with the positive transition of the clock line. However, when the S/P control is low, the internal data and then the serial input data is shifted out in sequence with positive transitions of the clock line. This means that after parallel data transfer, all Q outputs are the same as the previous P-inputs; thus, when the serial mode is used, the previous P-inputs appear on Q8 in sequence with the clock signal. P8 appears first, then P7, etc., until the clock input stops.

A5 is a dual J-K flip-flop. It is used to sense zeros and ones and to generate a pulse with a duration of 1 unit for a zero, and a pulse with a duration of 3 units for a one. Q1 of A5 divides the "code clock" frequency by two when the reset line is low. The output Q1 of A5 provides the clock input to CL2 of A5. Whenever J2

of A5 is high, the positive clock transition on CL2 will switch Q2 high also, and the next positive clock input will return it to low, but when J2 is low, Q2 remains low. The OR function (A1A3) of outputs Q1 and Q2 of A5 provide the wave form for the zeros and ones.

The latching relay K2 controls the code speed. When the relay is in the slow code position, the "code clock" is furnished by Q13 of A10, which has a period (T) of 109.73 msec. In the fast code mode, the relay switches the "code clock" to higher frequency outputs of A10. These outputs are selectable by a jumper between the relay and A10. A10-Q10 (T = 13.73 msec) multiplies the code speed by 8, A10-Q9 (T = 6.866 msec) by 16, and A10-Q8 (T = 3.433 msec) by 32. Higher code speeds could be used; however, the limited response time of the printer at the ground station and also the code transmission media employed are the deciding factors of the code speed utilized.

4.4.5.2 Code Generator Time Sequence

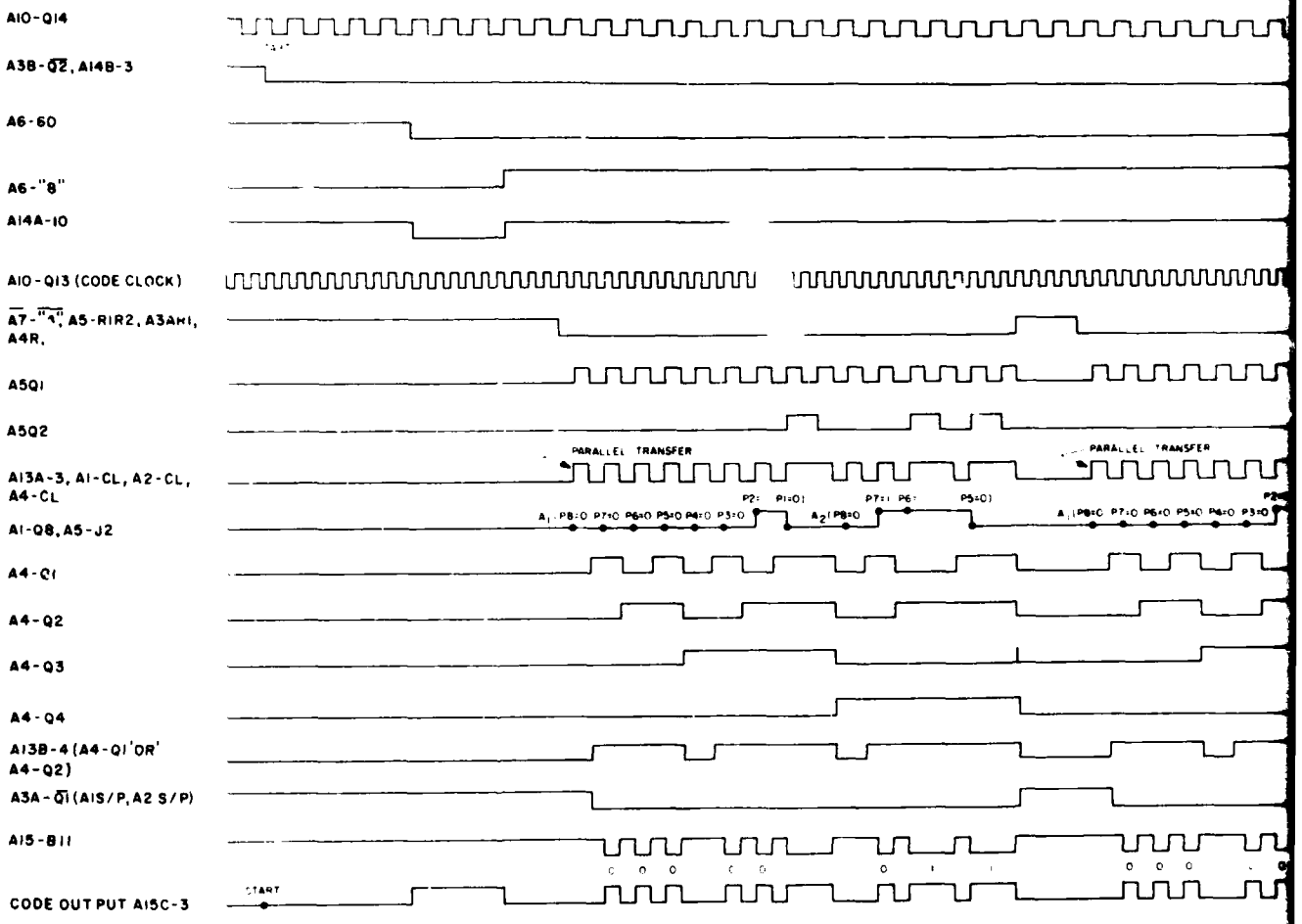
This section describes the time sequence of the verification code, using channel 11 as an example. The slow code speed is used so that the timing relationship between the various outputs can be represented on the same drawing.

The number 11, in a 9-bit binary system, is 000 001 011. Therefore, the binary inputs to the code generator board are high on pins 5, 6, and 7 ("8," "2," and "1") and low on pins 4 and F. These inputs are furnished by the matrix output of the selector board for channels 10-18, which become the code-determining inputs (P1-P8) to shift registers A1 and A2. The inputs (P1-P8) of A1 and A2 not designated on the schematic diagram are all grounded (logic 0).

The code sequence is initiated by Q12 of A12, which provides the clock input to A3B via the exclusive OR gate of A14D. This occurs after the 3.5-sec selection time delay. At this point, close attention should be paid to the code time sequence diagram of Figure 9 and the schematic diagram of the code generator of Figure 8.

The output Q2 of A3B activates the "priority" output (logic 0) on pin 1 of the code generator board, and $\overline{Q2}$ enables decade counters A8 and A6 via A14B. The "priority" output controls the output of the modulation multiplexer in the balloon control and data package. During the command verification code generation, the modulation of the balloon's data transmitter is transferred from the normal modulation input to the channel verification code output. The "priority" output remains activated until the end of the command verification code.

After A6 is enabled, it counts five clock pulses furnished by Q14 of A10, which has a period of 219.717 msec. At that time the output "CO" (carry out) of A6 switches to 0. The exclusive OR of "CO" and "8" of A6 provides a 0 on pin 1 of A15C, which starts the synchronization pulse on the output of A15C. Three counts later, the "8" output of A6 goes high, the counter stops counting, the synchronization pulse ends, and the inversion by A15D enables A7.


A10-Q14
A38-$\overline{Q2}$, A14B-3
A6-60
A6-"8"
A14A-10
A10-Q13 (CODE CLOCK)
$\overline{A7}$-"4", A5-R1R2, A3AH1, A4R,
A5Q1
A5Q2
A13A-3, A1-CL, A2-CL, A4-CL
A1-Q8, A5-J2
A4-Q1
A4-Q2
A4-Q3
A4-Q4
A13B-4 (A4-Q1 'OR' A4-Q2)
A3A-$\overline{Q1}$ (A1S/P, A2 S/P)
A15-B11
CODE OUT PUT A15C-3
PARALLEL TRANSFER
PARALLEL TRANSFER
START

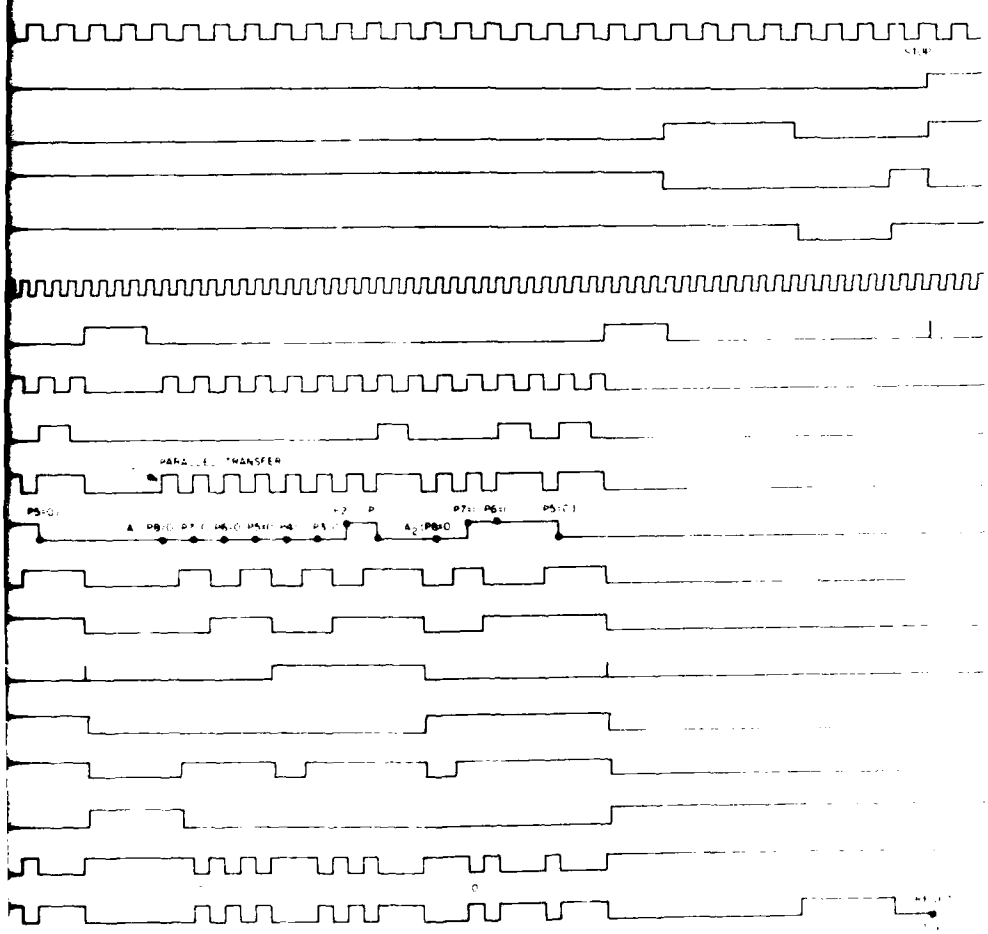


Figure 9. Code Time Sequence Diagram

The time duration for the sync pulse is always the same because the timing of the code sequence in this time period is generated by the fixed output Q14 of A10. The sync pulse has a time duration of 659.19 msec (3 × 219.73 msec). The pause before the sync pulse is not constant, however. Its length depends on where the code start pulse begins within the clock cycle of A10-Q14; it can vary from 879.8 msec (4 × 219.73 msec) plus 0.86 msec (half-clock period of A10-Q7), to plus 218.87 msec (219.73 msec–0.86 msec).

After the synchronization pulse ends, the "8" output of A6 goes high, the decade counter A7 becomes enabled, and counts 4 "code clock" pulses and stops. The "4" output of A7 is inverted by A16D, which enables (reset line low) A5, A3A, and A4, and increments the decade counter A8 by one. Then, the next positive transition of the "code clock" switches Q1 of A5 high. This also appears at the output of A13A, thereby providing the clock input to A1 and A2. At this moment, the parallel data on the inputs of A1 and A2 is transferred (jammed) into the shift registers because the serial parallel control (S/P), connected to $\overline{Q1}$ of A3A, is still high. These inputs are high (1) on P2 ("8") of A1, and on P7 ("2") and P6 ("1") of A2, while the rest of the P-inputs are low (0). The binary ones are generated from the matrix output for channel 11, which is high in the "8," "2," and "1" position of the binary number.

Then, at the first negative transition at the output of A13A, counter A4 is incremented. Q1 of A4 applies a clock input to A3A. $\overline{Q1}$ of A3A, in turn, switches the serial-parallel control (S/P) of A1 and A2 from high to low, changing the mode of operation from parallel to serial. The previous parallel inputs (zeros and ones) of A1 and A2 will now appear sequentially on both Q8 of A1 and J2 of A5, synchronously with the positive transitions of the A13A output.

The output of A13A follows the input from Q1 of A5, until J2 of A5 goes high. When J2 of A5 is high, Q2 will also go high and remain high for the duration of one input period from Q1 of A5, and then return to zero again. The OR function of Q1 and Q2 of A5 provides a pulse width of three "code clock" periods when A5-J2 is high, compared to a unit "code clock" period when it is low. In this manner, the final code output, through A15C, provides a 3-unit pulse width for a binary "1," and a 1-unit pulse width for a binary "0." This relationship is used in the Morse code characters for dashes and dots, and the same relationship is maintained in the faster octal codes.

The negative transitions of the output wave of the OR gate A13A increments the counter A4. A4-Q1 divides the A13A output frequency by 2, A4-Q2 by 4, A4-Q3 by 8, and A4-Q4 by 16. The inverted code ($\overline{code}$) is produced at the output of the NAND gate A15B, which has one input from A13A and the other from A13B. The output of A13B is low when both Q1 and Q2 of A4 are low. This is the case during reset (0 count), and after 4, 8, and 12 counts. During this period, the

NAND gate 15B is inhibited, but when either Q1 or Q2 of A4 is high, the output wave from A13A is inverted by A15B. The NAND function of the outputs of A15B and A14A provides the actual code output, through A15C.

4.4.5.3 Spacing

When Q1 and Q2 of A4 are both low, the code output is also low for a duration of three "code clock" periods, because A15B is inhibited during two "code clock" periods, which is followed by a low from the output of A13A with a duration of one "code clock" period, inhibiting A15B during this time period. This forms the pause between the first, second, and third Morse code letters, as well as the space after every third binary bit in the octal code.

4.4.5.4 Second Code Cycle

The first 3-letter or 9-bit cycle of the code requires 12 A13A pulses. During the negative transition of the 12th pulse, outputs Q3 and Q4 of A4 are momentarily high. When this happens, A15A supplies a low to A15D, which resets A7, and the "4" output of A7 changes to low. This low is inverted by A16D, resetting A5, A3A, and A4. After A4 is reset, Q3 and Q4 of A4 become low. This switches the output of A15A high and, in turn, the output of A15D low. Thus, A7 is enabled again. After four "code clock" pulses, the "4" output of A7 goes high, starts the second code cycle, and increments the counter A8 for the second time. The second code cycle is identical to the first one because channel 11 is still selected and the binary code-determining inputs are still the same. After the second cycle, the same reset sequence as that for cycle 1 is followed. Then A7 counts four "code clock" pulses and increments A8 for the third time.

The "3" output of A8 is differentiated by C7 and applied to A14B, which resets A6 momentarily, forcing the A6-"8" output low. This output disables A7, A5, A3A, and A4. A6 starts counting clock pulses from the output of A10-Q14 until the A6-"8" output goes high. During this time, the code waveform is low (long pause) until the A6-"CO" output switches from high to low. At this point, another synchronization pulse begins and ends when A6-"8" becomes high. The A6-"8" output enables A7 again. A7 counts four "code clock" pulses and stops. The A7-"4" output increments the counter A8 for the fourth time, which switches the A8-"4" output high. This output is applied to A16B, which inverts the signal and forces the output of A16A high, resetting A3B. The $\overline{Q2}$ output of A3B resets and disables all counters and flip-flops as described at the beginning in the Reset Procedure, 4.4.3. At the same time, the "priority" output on pin 1 of the code generator board is disabled by Q2 of A3, thus restoring the normal modulation to the balloon's transmitter.

The inverted code ($\overline{code}$) on pin 18 of the code generator board is inverted again in the transmitter modulator such that the ground station receives the actual code output. The keying relay K1 is only used in the slow code mode, and it is only

necessary when the code output is interfaced with negative supply circuits; otherwise, it can be eliminated.

4.4.5.5 Channel Activation

After the reply codes are received by the ground station, the execute tone G is added to the modulation of the ground transmitter. This tone is decoded on the code generator board, similar to the decoding described for the tone decoder board.

The G-tone is detected by the filter FL-G, and amplified by A9. The output of A9 is rectified and filtered. The resulting voltage across C15 enables A-11 via A16C, initiating the 3.5-sec energize time delay. At the end of that delay, A-11-Q12 activates the relay K3. This delay circuit consists of A-11 and A13D. The clock frequency from A10-Q7 for A-11 is gated through A13D. It works in the same fashion as the selection delay. Q12 of A-11 switches to high after 2048 clock periods of 1.7166-msec duration, which provides a delayed output of 3.5 sec. When Q12 of A-11 goes high, the NOR gate A13D becomes disabled, and A-11-Q12 remains high until it is reset again. The A-11-Q12 output is buffered by A13C, which provides the drive to the relay transistor and activates K3.

The output of K3 is connected to all channel relays so that the selected channel and K3 provide the actual ground closure output.

4.4.5.6 Deactivation

When a channel is to be deactivated, the G-tone is removed from the modulation of the ground transmitter. This resets A-11, and Q12 of A-11 starts the code generation process again. The channel select code is then removed. This process is the same as previously described, unless, in violation of procedure, the channel select tone (B for channel 11) and the G-tone are removed simultaneously. In that case, the reply code will be all zeros (SSS). In either case (full code or all zeros), complete deactivation of the selected channel is indicated.

4.5 Voltage Verification (VV) Board

A voltage verification board can be used, in place of the previously-described code generator board, when a voltage output is desired for channel verification. However, this requires the presence of a balloon-borne PCM (pulse code modulation) encoder or some other means of measuring the channel voltage output, which is then transmitted back to ground control. Figure 10 is the schematic diagram of the VV board.

The board consists of a digital-to-analog converter (D/A), two time delay circuits, and a tone decoder for the energize tone G, which activates the energize or execute relay K1.

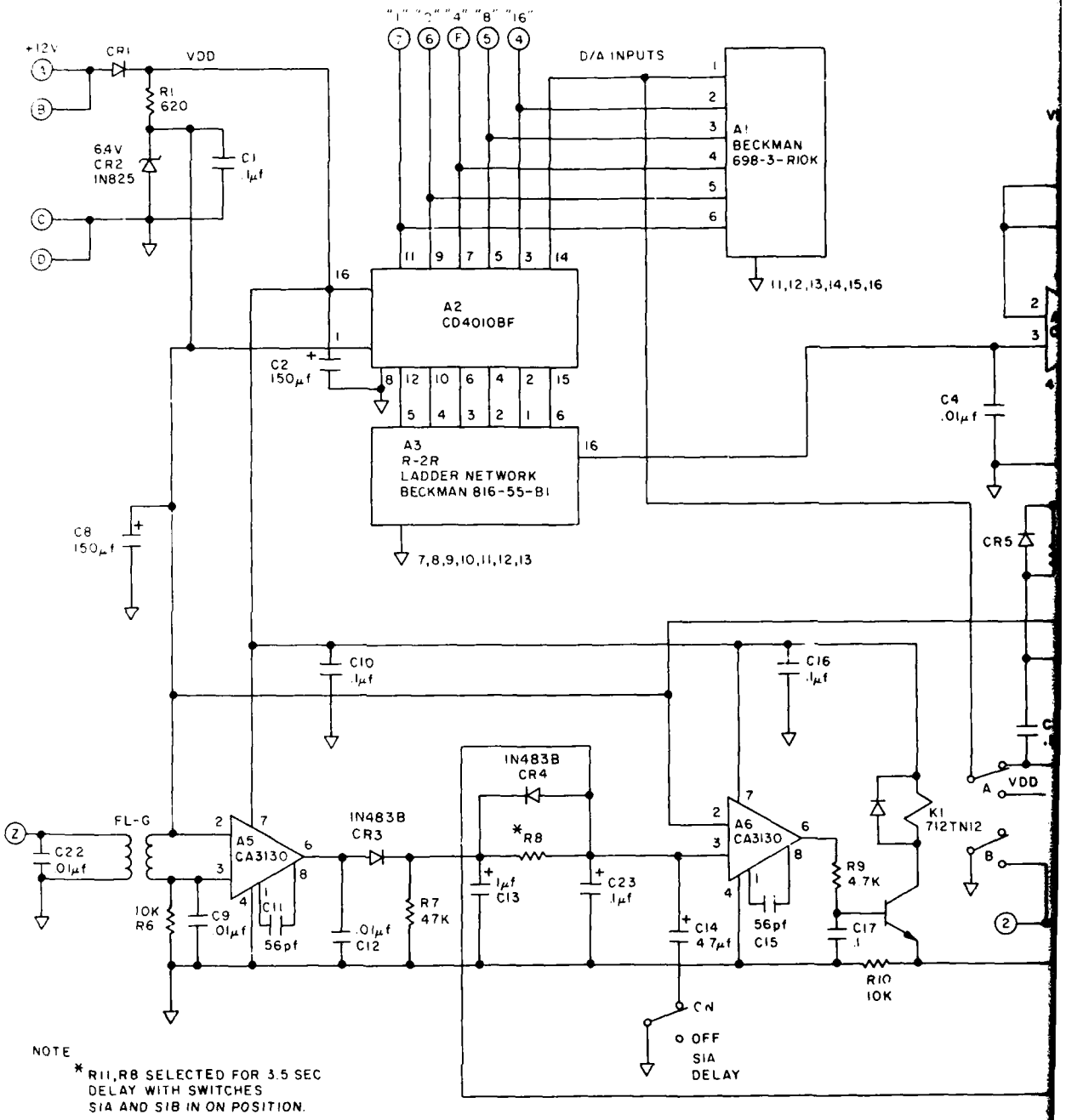
When a channel is selected, the digital outputs (zeros and ones) from the diode matrix of one of the selector boards are applied to the D/A inputs (pins 4, 5, 6, 7, and F). These inputs determine the corresponding outputs of A2. A2 applies power and grounds to the R-2R resistor ladder network A3, which provides a binary weighted voltage output to A4. The final voltage output is adjusted by R4 so that 0.1 V times the number of the selected channel equals the voltage output. This voltage will finally appear on pin Y after the relay K2 becomes activated. Before K2 is activated, the voltage on pin X of the multiplex input appears on pin Y through the normally closed contact of K2. The multiplex input can either be grounded or a voltage can be applied so that the PCM encoder will normally measure the voltage on pin X. However, when K2 is activated, the voltage verification output will be measured and transmitted to ground control, indicating the selected command channel.

The relay K2 becomes activated by a delay circuit through A7. When any one of the 18 channels is selected, B+ is applied to pin E (common delay) of the VV board, and the current through R11 charges the capacitors C18 and C24 (the switch S1B in the delay position). As soon as the voltage on pin 3 of A7 reaches a value slightly higher than the 6.4 V applied to pin 2 of A7, its output switches from 0 to B+. This energizes the relay transistor and K2 activates. When the switch S1B grounds C18, the time delay for this action is 3.5 sec, the same delay as the 3.5-sec selection time delay on the code generator board. However, when the switch is in the open position, the time delay is disabled and K2 becomes activated as soon as B+ appears on pin E (common delay). The same type of circuit is used in the energize delay.

The instant activation mode should only be used when a secure frequency command receiver frequency, not prone to interference, is employed.

The relay K1, which finally provides the ground closure to the selected command channel, cannot be activated unless K2 is activated first. Before K2 is activated, the resistor R13 is grounded through a normally-closed contact of K2, and connected to pin 3, the noninverting input, of A6. This provides a bias much lower than the voltage on pin 2 of A6, and keeps the output of A6 saturated at ground potential. However, even if A6 had an output, K1 still could not be activated, because the emitter resistor R10 (10K) keeps the current through the relay coil of K1 well below the required pull-in current.

After K2 is activated and the verification voltage code has been received at ground control, the G-tone is sent to the balloon control instrument. Tone G is then filtered by FL-G, amplified by A5, rectified by CR3, and integrated by C13, the same procedure as on the code generator board. The resultant voltage across C13 provides power to R8, which supplies the charging current to C14 and C23 (assuming the switch, S1A, is in the delay mode, C14 grounded). After a delay of


+12V
CR1
VDD
R1
620
6.4V
CR2
IN825
C1
.1μf
"1" "2" "4" "8" "16"
D/A INPUTS
A1
BECKMAN
698-3-R10K
11,12,13,14,15,16
A2
CD4010BF
C2
150μf
A3
R-2R
LADDER NETWORK
BECKMAN 816-55-B1
7,8,9,10,11,12,13
C4
.01μf
C8
150μf
CR5
C10
.1μf
C16
.1μf
IN483B
CR4
IN483B
CR3
FL-G
C22
.01μf
A5
CA3130
A6
CA3130
*R8
K1
712TN12
A
VDD
B
R9
4.7K
C17
.1
R10
10K
C13
.1μf
C23
.1μf
C14
4.7μf
C15
56pf
C11
56pf
C9
.01μf
R6
10K
C12
.01μf
R7
47K
CN
OFF
SIA
DELAY
NOTE
* R11,R8 SELECTED FOR 3.5 SEC
DELAY WITH SWITCHES
S1A AND S1B IN ON POSITION.

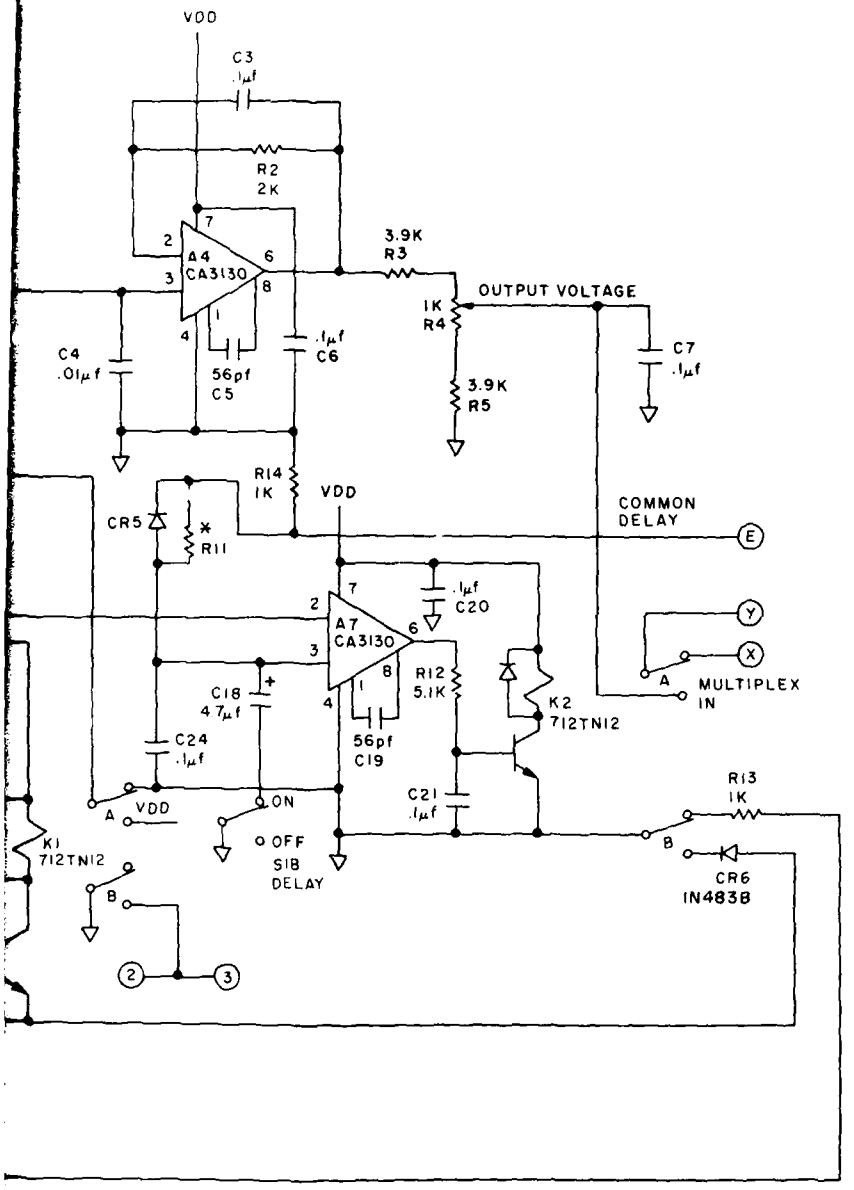


Figure 10. Voltage Verification Board Schematic

3.5 sec (energize delay), the voltage on pin 3 of A6 becomes slightly higher than the voltage on pin 2 of A6, which switches the output from 0 to B+, thereby activating K1.

The ground closure of K1, which is in series with the selected channel relay contacts, provides the final channel output. At the same time, the other set of contacts of K1 feeds the input of the least-significant bit (LSB) of the D/A converter, adding 0.05 V to the channel verification voltage.

The addition of 0.05 V to the channel verification voltage output indicates to ground control that the selected command channel has been activated.

Channel deactivation is accomplished by removing the G-tone, which subtracts 0.05 V from the previous voltage output of the D/A converter. Then, removal of the select tone deactivates relay K2, which switches the output on pin Y from the D/A converter output back to the multiplex input voltage.

4.6 Code Reception at Ground Control

4.6.1 GENERAL CONSIDERATIONS

The command selector and a 16-channel encoder/timer unit, also developed under this Work Unit, are usually part of the same control and data package for long-duration, over-the-horizon balloon flights. The up and down link transmissions for this particular system can utilize radio signals in the HF band to take advantage of long-distance signal propagation. However, for short-duration balloon flights, radio signals in other frequency bands can be employed.

The maximum allowable bandwidths of assigned frequencies in the HF spectrum are fairly narrow, which limits the data rate or code speeds. For this reason, a relatively slow octal code is generated by the data encoder as well as by the command selector. Both units provide a 9-bit binary pulse code. Three binary bits are grouped together to form an octal code, which gives the appearance of Morse code letters when the code speed is very slow.

The code speeds of the encoder and command selector can be programmed simultaneously by command. The encoder digitizes the channel input voltage into a maximum of 512 binary codes (9 bits), and the resolution is adjusted to 10 mV. Therefore, the code output can represent a maximum of 5.11 V when all 9 bits are binary ones. The number of the selected channel of the command selector is also equal to the binary number of the code output. Therefore, the decoding equipment will represent the selected channel number of the command selector or the voltage of the encoder input by simply converting binary numbers into decimal numbers.

4.6.2 DATA PRINTER

Two types of ground-based decoding equipments were designed, a 16-channel, 3-digit numeric display unit, and a printer unit interfaced with the decoding

circuitry. At the ground station, the pulse widths of the code elements are measured to determine binary ones and zeros (a zero is a unit pulse width and a one has a pulse width of 3 unit pulses). The decoding circuitry uses a bit counter, which resets during the spaces after the 9-bit code format, and also a channel counter, which resets during the synchronization pulse. This sync pulse is always generated before the code output of channel 1 by the encoder and before and after the channel select verification codes by the command selector.

The decoded sync pulse provides a print command and at the same time disables the data lines to the printer input. A blank consequently shows up on the paper tape where the decoded data is normally printed. This blank provides a visual offset between the first and last channel of the encoder, and also before and after the channel verification codes of the command selector. However, the channel select verification codes can be identified very easily because the blanks always appear before channel 1 and after channel 2, which is not the case for the encoder data. This makes the command channel verification numbers stand out from the rest of the data.

The decoding circuitry at ground control must transform the detected binary number into a binary coded decimal (BCD) number, which is then routed to the parallel data input lines of the printer. In the slow code mode (Morse code), data can be printed after every code group of 9 bits. However, when the code speed is multiplied by 32, the printer cannot respond fast enough to print the data. In this case, the data for two channels is printed on the same line.

In addition to the data (encoder voltage or the number of the selected command channel in the case of the command selector), the printer provides the time of day in hours, minutes, and seconds before the data, and also the decoded channel number of the encoder after the data. All three items (time, data, and channel number for the encoder) are printed on the same line with visual offsets between each group. The printout interval of time information can be programmed by an external switch on the printer without affecting the data or it can be completely disabled. However, when the paper tape is to be used for a permanent record of the balloon flight, time printout is always incorporated.

4.6.3 DISPLAY UNIT

When a magnetic tape recorder is available to record and store the data from a balloon flight, a 16-channel, real-time data display unit is used to provide the status of the balloon payload. This unit employs the same decoding circuitry as the printer interface unit.

Each channel consists of a 3-digit LED (light emitting diode) numeric display. The serial code from the balloon is decoded into a binary number, which is then transformed into a parallel BCD code suitable for the input to each numeric display.

The sync pulse before every code frame from the encoder code resets the channel counter so that subsequent data is routed to the proper display, where it is latched until it is updated by the next code frame. Therefore, the number for the selected command channel will always appear on channels 1 and 2 on the display unit, which is identical to the sequence on the paper tape of the printer.

After a channel select verification code from the selector, the channels from the encoder are momentarily routed to the wrong display channel because the sync pulse after the select verification code resets the channel counter. However, the next code frame from the encoder starts with a sync pulse which resets the channel counter again, and subsequent channels are routed to the correct numeric display. This peculiarity is also observed on the paper tape of the printer unit.

5. TEST RESULTS

5.1 General

The prototype command selector was tested extensively, both on the ground and in actual balloon flights. During the course of that testing, various time delays were used before the 3.5-sec period was officially adopted. The verification code format also underwent revision during the tests. The results of the test program can be summarized as "excellent," in that the command selector has been shown to be a very efficient and reliable device which, in conjunction with the other command system components, allows positive and secure remote activation of selected functions.

5.2 Laboratory Tests

The command selector protype unit was subjected to customary bench checks prior to its first balloon flight. Then, after performing very successfully on several flights, during which 7-sec channel selection and execution time delays were employed, it was subjected to a much more rigorous laboratory test. Different time delays and audio signals from local radio stations were used to determine whether false channel activations would occur.

In the first test, the output of an FM receiver tuned to a local broadcast station (music) was applied to the command selector audio input for a duration of one week. The time delay used was 7 sec. One channel acquisition (selection) was experienced. There was no channel activation, however, because the G-tone relay was never energized. The "selected" channel dropped out during the reply code, as indicated by all zeros in the second cycle of the verification code.

The same test was performed, with a 3.5-sec time delay, for another week. Again there was one acquisition, but not an activation. The time delay was changed

to 1.8 sec, and the same test was conducted again. During that one-week period, two channel acquisitions were experienced, but no channel activation.

The FM receiver used in the test has a linear audio output, which means that a fairly high dynamic range of the music power was applied to the resonant reed tone filters. With loud music, the bandwidth of the filters increases and the chance for false channel activation also increases. On the other hand, the command receivers normally used with the command selector are equipped with an automatic audio gain control (AGC) circuit, which limits the level of audio signals applied to the tone filters. This decreases the likelihood of false channel acquisition in actual flight.

5.3 Flight Tests

A 3.5-sec time delay was selected for the final design. Several units with this time delay were then tested during actual balloon flights. Again, these tests proved to be very successful. Originally, a 6-bit verification code was used, which was repeated three times. This code was not the same as the data encoder format used in conjunction with the balloon control package, however, and thus was not compatible with the display unit and the printer at the ground control station. The result was a change to the 9-bit code described in Section 4.4.6.

6. SUMMARY AND CONCLUSIONS

The BCS-18 Command Selector has been described in detail, both for the casual reader and for technical personnel concerned with its operation and maintenance. Its intended use as part of a ground controlled command system for the remote activation of the balloon payload and housekeeping functions has been established. The approach taken in the development of the BCS-18A has been outlined, and the important issues of channel selection, verification, and activation has been treated in depth, with emphasis on the logic employed and the circuits used to implement the logic. Testing of the unit has been described, and the excellent results obtained from those tests have been summarized.

It is concluded that the objectives of the in-house work unit have been met successfully, and that the BCS-18A Command Selector is a highly reliable, very secure piece of equipment, fully suited to its intended use.

7. PARTS LIST

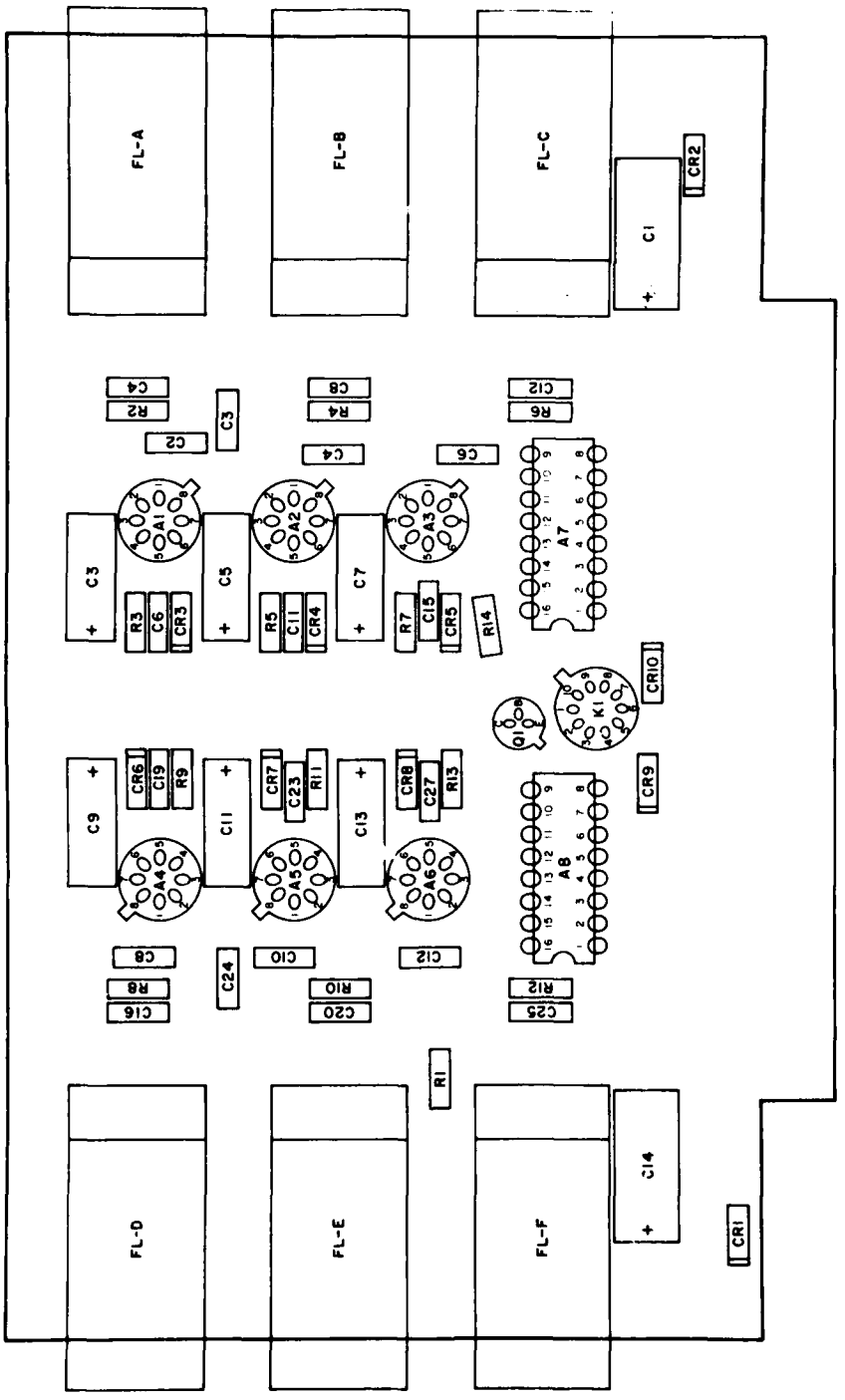


Figure 11. Tone Decoder Board Layout

Parts List
Tone Decoder

Symbol	Description	Part No. or Type	Vendor
A1	Integrated Circuit	CA3130AT	RCA
A2	Integrated Circuit	CA3130AT	RCA
A3	Integrated Circuit	CA3130AT	RCA
A4	Integrated Circuit	CA3130AT	RCA
A5	Integrated Circuit	CA3130AT	RCA
A6	Integrated Circuit	CA3130AT	RCA
A7	Integrated Circuit	CD4028BF	RCA
A8	Integrated Circuit	CD4028BF	RCA
C1	Capacitor 150 µf 20 V	MMTP	Mallory
C2	Capacitor 150 µf 20 V	MMTP	Mallory
C3	Capacitor 0.01 µf 100 V	CK05BX103K	
C4	Capacitor 0.01 µf 100 V	CK05BX103K	
C5	Capacitor 56 pf 200 V	CK05BX560K	
C6	Capacitor 3.3 µf 20 V	MMTP	Mallory
C7	Capacitor 0.01 µf 100 V	CK05BX103K	
C8	Capacitor 0.01 µf 100 V	CK05BX103K	
C9	Capacitor 0.01 µf 100 V	CK05BX103K	
C10	Capacitor 56 pf 200 V	CK05BX560K	
C11	Capacitor 3.3 µf 20 V	MMTP	Mallory
C12	Capacitor 0.01 µf 100 V	CK05BX103K	
C13	Capacitor 0.01 µf 100 V	CK05BX103K	
C14	Capacitor 56 pf 200 V	CK05BX560K	
C15	Capacitor 3.3 µf 20 V	MMTP	Mallory
C16	Capacitor 0.01 µf 100 V	CK05BX103K	
C17	Capacitor 0.01 µf 100 V	CK05BX103K	
C18	Capacitor 56 pf 200 V	CK05BX560K	
C19	Capacitor 3.3 µf 20 V	MMTP	Mallory
C20	Capacitor 0.01 µf 100 V	CK05BX103K	
C21	Capacitor 0.01 µf 100 V	CK05BX103K	
C22	Capacitor 56 pf 200 V	CK05BX560K	
C23	Capacitor 3.3 µf 20 V	MMTP	Mallory
C24	Capacitor 0.01 µf 100 V	CK05BX103K	
C25	Capacitor 0.01 µf 100 V	CK05BX103K	
C26	Capacitor 56 pf 200 V	CK05BX560K	
C27	Capacitor 3.3 µf 20 V	MMTP	Mallory
CR1	Diode	1N483B	
CR2	Diode Zener	LVA351A	TRW
CR3	Diode	1N483B	
CR4	Diode	1N483B	
CR5	Diode	1N483B	
CR6	Diode	1N483B	
CR7	Diode	1N483B	
CR8	Diode	1N483B	
CR9	Diode	1N483B	
CR10	Diode	1N483B	

Parts List
Tone Decoder (Cont.)

Symbol	Description	Part No. or Type	Vendor
FL A	Tone Filter	RF 20	Bramco
FL B	Tone Filter	RF 20	Bramco
FL C	Tone Filter	RF 20	Bramco
FL D	Tone Filter	RF 20	Bramco
FL E	Tone Filter	RF 20	Bramco
FL F	Tone Filter	RF 20	Bramco
K1	Relay 12 V	712D-12	Teledyne
Q1	Transistor PNP	2N2907	
R1	Resistor 680 ohms 1/4 W	Carbon Comp.	
R2	Resistor 8.2K ohms 1/4 W	Carbon Comp.	
R3	Resistor 47K ohms 1/4 W	Carbon Comp.	
R4	Resistor 8.2K ohms 1/4 W	Carbon Comp.	
R5	Resistor 47K ohms 1/4 W	Carbon Comp.	
R6	Resistor 8.2K ohms 1/4 W	Carbon Comp.	
R7	Resistor 47K ohms 1/4 W	Carbon Comp.	
R8	Resistor 8.2K ohms 1/4 W	Carbon Comp.	
R9	Resistor 47K ohms 1/4 W	Carbon Comp.	
R10	Resistor 8.2K ohms 1/4 W	Carbon Comp.	
R11	Resistor 47K ohms 1/4 W	Carbon Comp.	
R12	Resistor 8.2K ohms 1/4 W	Carbon Comp.	
R13	Resistor 47K ohms 1/4 W	Carbon Comp.	
R14	Resistor 10K ohms 1/4 W	Carbon Comp.	

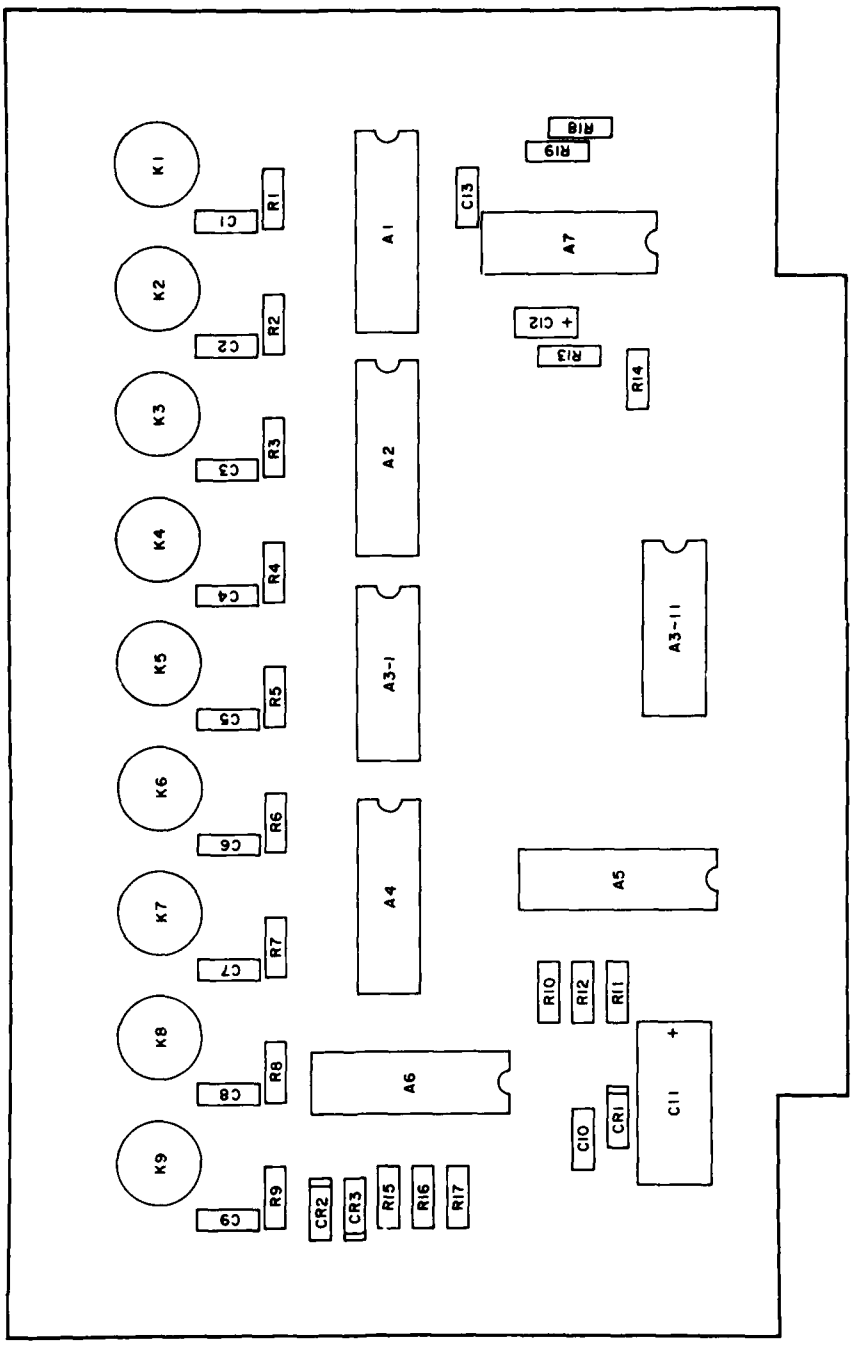


Figure 12. Channel Selector Board Layout (1–18)

Parts List
Channel Selector

Symbol	Description	Part No. or Type	Vendor
A1	Integrated Circuits	CD4028BF	RCA
A2	Integrated Circuits	CD4028BF	RCA
A3-1	Integrated Circuits	HM1093-2	Harris
A3-11	Integrated Circuits	HM1013-2	Harris
A4	Integrated Circuits	CD4028BF	RCA
A5	Integrated Circuits	CD4042BF	RCA
A6	Integrated Circuits	CD4042BF	RCA
A7	Integrated Circuits	CD4001AE	RCA
C1	Capacitor 0.1 μf 50 V	CK05BX104K	
C2	Capacitor 0.1 μf 50 V	CK05BX104K	
C3	Capacitor 0.1 μf 50 V	CK05BX104K	
C4	Capacitor 0.1 μf 50 V	CK05BX104K	
C5	Capacitor 0.1 μf 50 V	CK05BX104K	
C6	Capacitor 0.1 μf 50 V	CK05BX104K	
C7	Capacitor 0.1 μf 50 V	CK05BX104K	
C8	Capacitor 0.1 μf 50 V	CK05BX104K	
C9	Capacitor 0.1 μf 50 V	CK05BX104K	
C10	Capacitor 0.1 μf 50 V	CK05BX104K	
C11	Capacitor 150 μf 20 V	MMTP	Mallory
C12	Capacitor 3.3 μf 60 V	MMTP	Mallory
C13	Capacitor 0.01 μf 100 V	CK05BX103K	
CR1	Diode	1N3612	
CR2	Diode	1N483B	
CR3	Diode	1N483B	
K1	Relay 12 V	712TN-12	Teledyne
K2	Relay 12 V	712TN-12	Teledyne
K3	Relay 12 V	712TN-12	Teledyne
K4	Relay 12 V	712TN-12	Teledyne
K5	Relay 12 V	712TN-12	Teledyne
K6	Relay 12 V	712TN-12	Teledyne
K7	Relay 12 V	712TN-12	Teledyne
K8	Relay 12 V	712TN-12	Teledyne
K9	Relay 12 V	712TN-12	Teledyne
R1	Resistor 6.8K ohms 1/4 W	Carbon Comp.	
R2	Resistor 6.8K ohms 1/4 W	Carbon Comp.	
R3	Resistor 6.8K ohms 1/4 W	Carbon Comp.	
R4	Resistor 6.8K ohms 1/4 W	Carbon Comp.	
R5	Resistor 6.8K ohms 1/4 W	Carbon Comp.	
R6	Resistor 6.8K ohms 1/4 W	Carbon Comp.	

Parts List
Channel Selector (Cont.)

Symbol	Description	Part No. or Type	Vendor
R7	Resistor 6.8K ohms 1/4 W	Carbon Comp.	
R8	Resistor 6.8K ohms 1/4 W	Carbon Comp.	
R9	Resistor 6.8K ohms 1/4 W	Carbon Comp.	
R10	Resistor 1M ohms 1/4 W	Carbon Comp.	
R11	Resistor 6.8K ohms 1/4 W	Carbon Comp.	
R12	Resistor 6.8K ohms 1/4 W	Carbon Comp.	
R13	Resistor 6.8K ohms 1/4 W	Carbon Comp.	
R14	Resistor 10K ohms 1/4 W	Carbon Comp.	
R15	Resistor 1M ohms 1/4 W	Carbon Comp.	
R16	Resistor 1M ohms 1/4 W	Carbon Comp.	
R17	Resistor 6.8K ohms 1/4 W	Carbon Comp.	
R18	Resistor 200K ohms 1/4 W	Carbon Comp.	
R19	Resistor 100K ohms 1/4 W	Carbon Comp.	

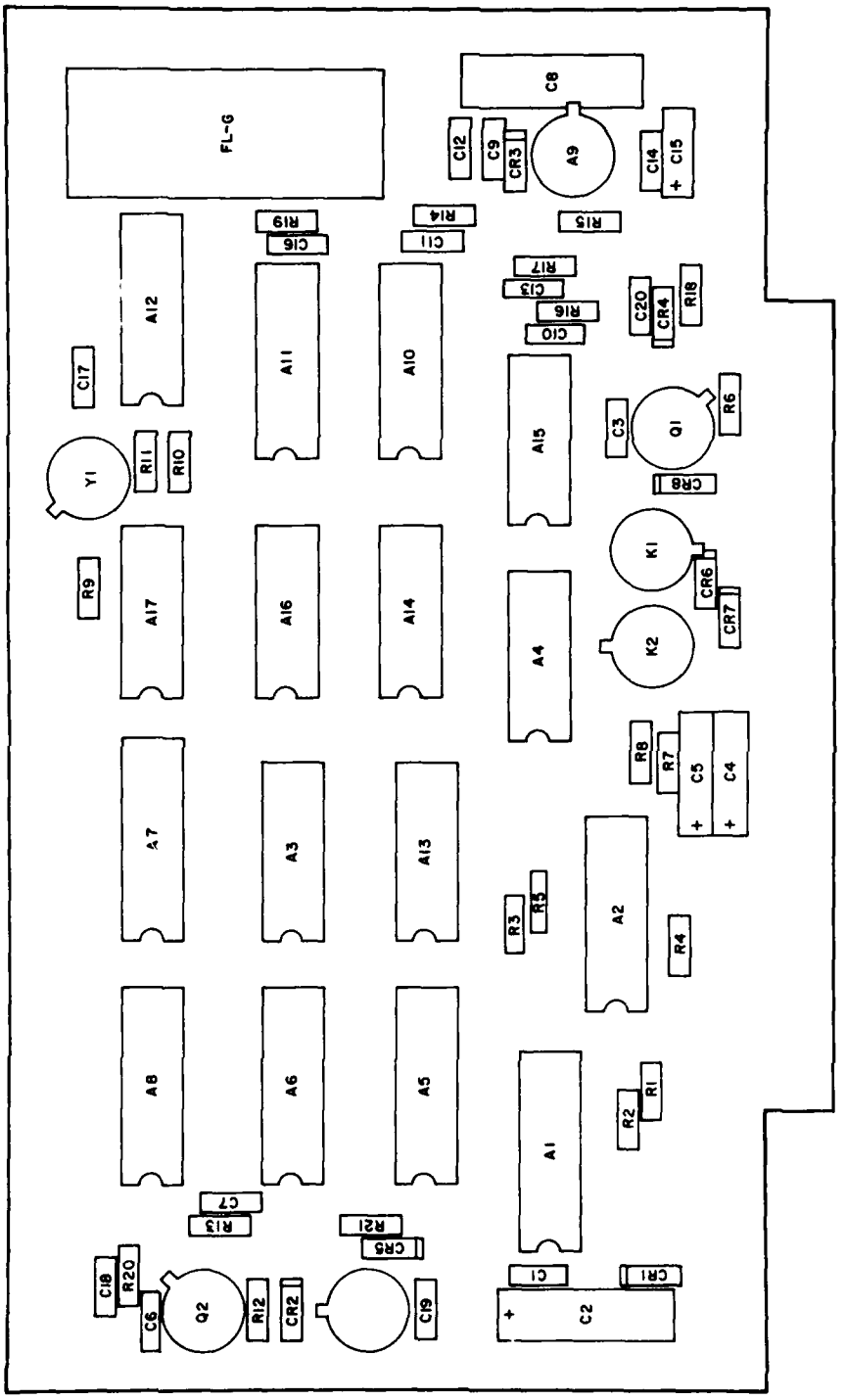


Figure 13. Code Generator Board Layout

Parts List
Code Generator
(for SEL)

Symbol	Description	Part No. or Type	Vendor
A1	Integrated Circuit	CD4014BF	RCA
A2	Integrated Circuit	CD4014BF	RCA
A3	Integrated Circuit	CD4013BF	RCA
A4	Integrated Circuit	CD4024BF	RCA
A5	Integrated Circuit	CD4027BF	RCA
A6	Integrated Circuit	CD4017BF	RCA
A7	Integrated Circuit	CD4017BF	RCA
A8	Integrated Circuit	CD4017BF	RCA
A9	Integrated Circuit	CA3130AT	RCA
A10	Integrated Circuit	CD4020BF	RCA
A11	Integrated Circuit	CD4020BF	RCA
A12	Integrated Circuit	CD4020BF	RCA
A13	Integrated Circuit	CD4071BF	RCA
A14	Integrated Circuit	CD4030BF	RCA
A15	Integrated Circuit	CD4011BF	RCA
A16	Integrated Circuit	CD4011BF	RCA
A17	Integrated Circuit	CD4001AE	RCA
C1	Capacitor 0.1 µf 50 V	CK05BX104K	
C2	Capacitor 150 pf 20 V	MMTP	Mallory
C3	Capacitor 0.01 µf 100 V	CK05BX103K	
C4	Capacitor 68 µf 15 V	MMTP	Mallory
C5	Capacitor 68 µf 15 V	MMTP	Mallory
C6	Capacitor 0.01 µf 100 V	CK05BX103K	
C7	Capacitor 0.01 µf 100 V	CK05BX103K	
C8	Capacitor 150 µf 20 V	MMTP	Mallory
C9	Capacitor 0.1 µf 50 V	CK05BX104K	
C10	Capacitor 0.1 µf 50 V	CK05BS104K	
C11	Capacitor 6.8 µf 20 V	MMTP	Mallory
C12	Capacitor 0.01 µf 100 V	CK05BX103K	
C13	Capacitor 0.01 µf 100 V	CK05BX103K	
C14	Capacitor 56 pf 200 V	CK05BX560K	
C15	Capacitor 10 µf 35 V		
C16	Capacitor 0.01 µf 100 V	CK05BX103K	
C17	Capacitor 0.1 µf 50 V	CK05BX104K	
C18	Capacitor 0.01 µf 100 V	CK05BX103K	
C19	Capacitor 0.01 µf 100 V	CK05BX103K	
C20	Capacitor 0.01 µf 100 V	CK05BX103K	
CR1	Diode	1N3612	
CR2	Diode	1N483B	
CR3	Diode Zener	LVA351A	TRW
CR4	Diode	1N483B	
CR5	Diode	1N483B	
CR6	Diode	1N483B	
CR7	Diode	1N483B	
CR8	Diode	1N483B	

Parts List
Code Generator (Cont.)
(for SEL)

Symbol	Description	Part No. or Type	Vendor
FL-G	Filter, Tone	RF20	Bramco
K1	Relay 12 V	712D-12	Teledyne
K2	Relay 12 V	422D-12	Teledyne
K3	Relay 12 V	712TN-12	Teledyne
Q1	Transistor	VN66AK	Siliconix Inc.
Q2	Transistor	VN66AK	Siliconix Inc.
R1	Resistor 47K ohms 1/4 W	Carbon Comp.	
R2	Resistor 47K ohms 1/4 W	Carbon Comp.	
R3	Resistor 47K ohms 1/4 W	Carbon Comp.	
R4	Resistor 47K ohms 1/4 W	Carbon Comp.	
R5	Resistor 47K ohms 1/4 W	Carbon Comp.	
R6	Resistor 100K ohms 1/4 W	Carbon Comp.	
R7	Resistor 10K ohms 1/4 W	Carbon Comp.	
R8	Resistor 10K ohms 1/4 W	Carbon Comp.	
R9	Resistor 1M ohms 1/4 W	Carbon Comp.	
R10	Resistor 15K ohms 1/4 W	Carbon Comp.	
R11	Resistor 5.1K ohms 1/4 W	Carbon Comp.	
R12	Resistor 100K ohms 1/4 W	Carbon Comp.	
R13	Resistor 10K ohms 1/4 W	Carbon Comp.	
R14	Resistor 51K ohms 1/4 W	Carbon Comp.	
R15	Resistor 2K ohms 1/4 W	Carbon Comp.	
R16	Resistor 10K ohms 1/4 W	Carbon Comp.	
R17	Resistor 8.2K ohms 1/4 W	Carbon Comp.	
R18	Resistor 47K ohms 1/4 W	Carbon Comp.	
R19	Resistor 2K ohms 1/4 W	Carbon Comp.	
R20	Resistor 1K ohms 1/4 W	Carbon Comp.	
R21	Resistor 4.7K ohms 1/4 W	Carbon Comp.	
Y1	Crystal	SX-1H	Statek

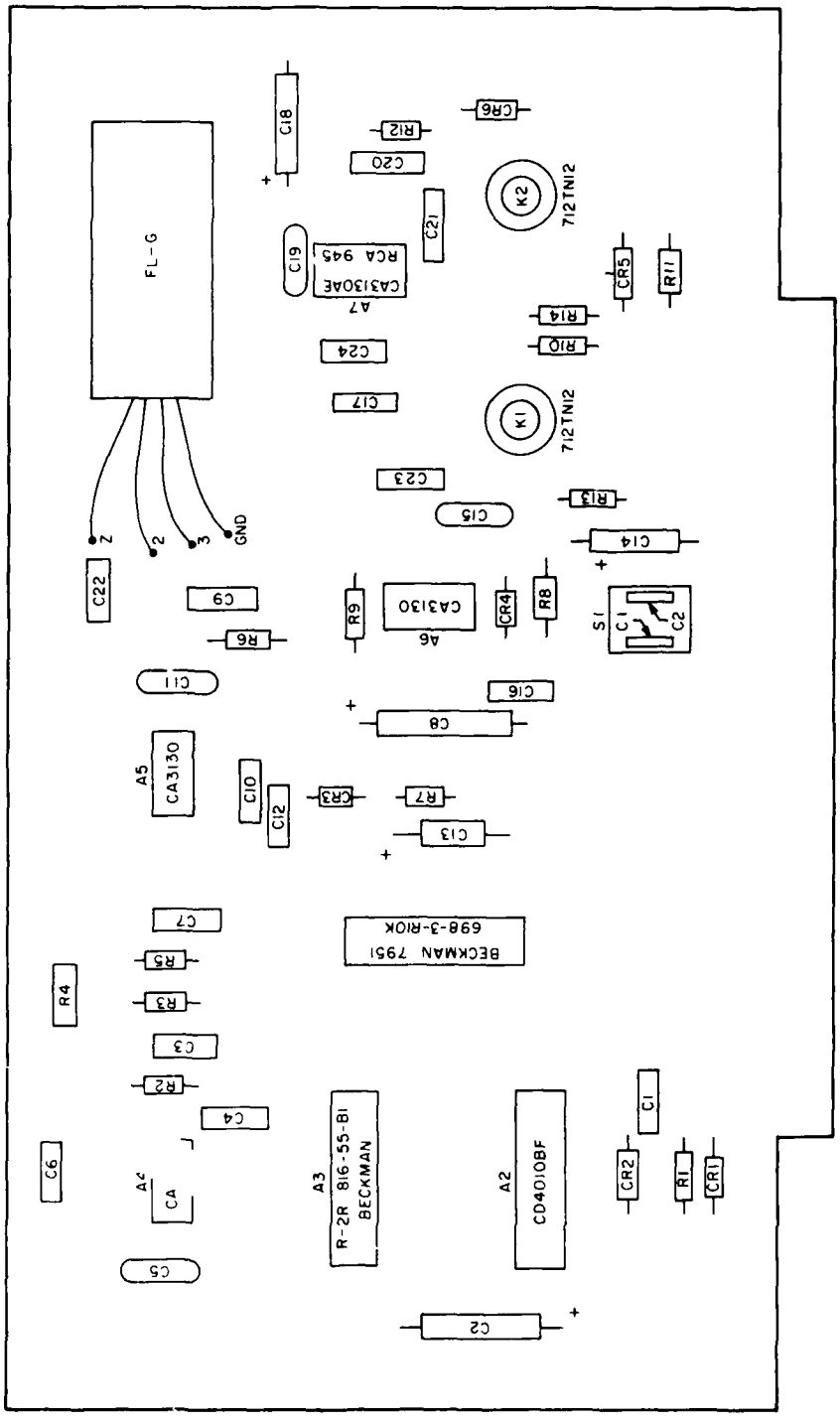


Figure 14. Voltage Verification Board Layout

Parts List
Voltage Verification Board

Symbol	Description	Part No. or Type	Vendor
A1	Resistor Network	698-3-R10K	Beckman
A2	CMOS-Buffer	CD4010BF	RCA
A3	R-2R Ladder Network	816-55-B1	Beckman
A4	Amplifier	CA3130AE	RCA
A5	Amplifier	CA3130AE	RCA
A6	Amplifier	CA3130AE	RCA
A7	Amplifier	CA3130AE	RCA
	Note: All Capacitors are ±10%		
C1	Capacitor 0.1 μf 50 V	CK05BX104K	
C2	Capacitor 150 μf 20 V	MMTP	Mallory
C3	Capacitor 0.1 μf 50 V	CK05BX104K	
C4	Capacitor 0.01 μf 100 V	CK05BX103K	
C5	Capacitor 56 pf 200 V	CK05BX560K	
C6	Capacitor 0.1 μf 50 V	CK05BX104K	
C7	Capacitor 0.1 μf 50 V	CK05BX104K	
C8	Capacitor 0.50 μf 20 V	MMTP	Mallory
C9	Capacitor 0.01 μf 100 V	CK05BX103K	
C10	Capacitor 0.1 μf 50 V	CK05BX104K	
C11	Capacitor 56 pf	CK05BX560K	
C12	Capacitor 0.01 μf 100 V	CK05BX103K	
C13	Capacitor Tantalum 0.1μf 50V	CSR13G105KM	
C14	Capacitor Tantalum 4.7μf 50V	CSR13G475KM	
C15	Capacitor 56 pf 200 V	CK05BX560K	
C16	Capacitor 0.1 μf 50 V	CK05BX104K	
C17	Capacitor 0.1 μf 50 V	CK05BX104K	
C18	Capacitor Tantalum 4.7μf 50V	CSR13G475KM	
C19	Capacitor 56 pf 200 V	CK05BX560K	
C20	Capacitor 0.1 μf 50 V	CK05BX104K	
C21	Capacitor 0.1 μf 50 V	CK05BX104K	
C22	Capacitor 0.01 μf 100 V	CK05BX103K	
C23	Capacitor 0.1 μf 50 V	CK05BX104K	
C24	Capacitor 0.1 μf 50 V	CK05BX104K	
CR1	Diode	1N483B	
CR2	Diode, Zener	1N825	
CR3	Diode	1N483B	
CR4	Diode	1N483B	
CR5	Diode	1N483B	
CR6	Diode	1N483B	
R1	Resistor 620 ohms 1/4 W	Carbon Comp.	
R2	Resistor 2K ohms 1/4 W	Carbon Comp.	
R3	Resistor 3.9K ohms 1/4 W	Carbon Comp.	
R4	Resistor 1K ohms 1/4 W	Carbon Comp.	
R5	Resistor 3.9K ohms 1/4 W	Carbon Comp.	

Parts List
Voltage Verification Board (Cont.)

Symbol	Description	Part No. or Type	Vendor
R6	Resistor 10K ohms 1/4 W	Carbon Comp.	
R7	Resistor 47K ohms 1/4 W	Carbon Comp.	
R8	Resistor * ohms 1/4 W	Carbon Comp.	
R9	Resistor 4.7K ohms 1/4 W	Carbon Comp.	
R10	Resistor 10K ohms 1/4 W	Carbon Comp.	
R11	Resistor * ohms 1/4 W	Carbon Comp.	
R12	Resistor 5.1K ohms 1/4 W	Carbon Comp.	
R13	Resistor 1K ohms 1/4 W	Carbon Comp.	
R14	Resistor 1K ohms 1/4 W	Carbon Comp.	
*R8, R11 selected for 3.5 sec delay with switches S1A and S1B in ON position (1M ohm typ.)			
S1	Switch, DIP DPDT	76C02	Grayhill

Bibliography

1. Handbook of Instructions for Command Selector BCS-2A-3818, (1964) Zenith Radio Corp., 6501 W. Grand Avenue, Chicago, IL.
2. RCA COS/MOS Integrated Circuits (1977).
3. Semiconductor Data Library–CMOS, Volume 5/Series B, Motorola, Inc. (1976).

Appendix A

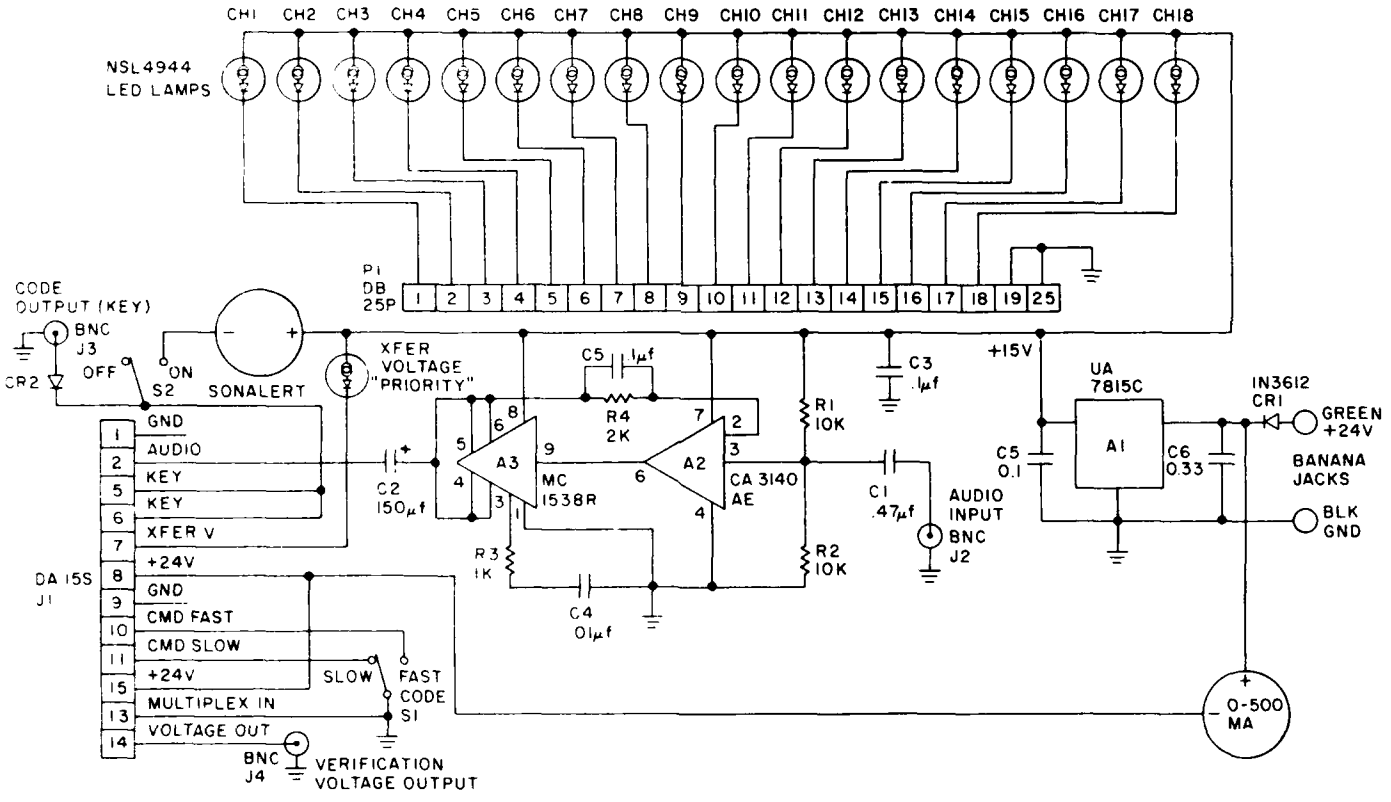
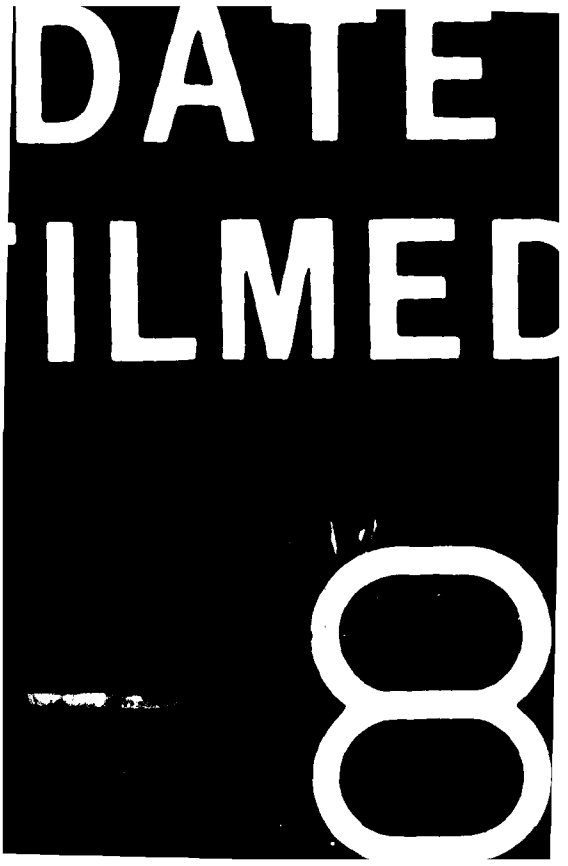


Figure A1. BCS-18A Selector Test Box Schematic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