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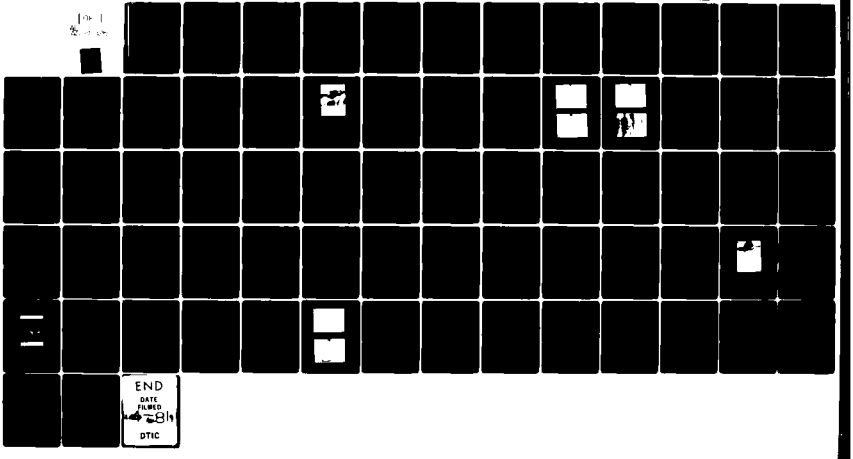

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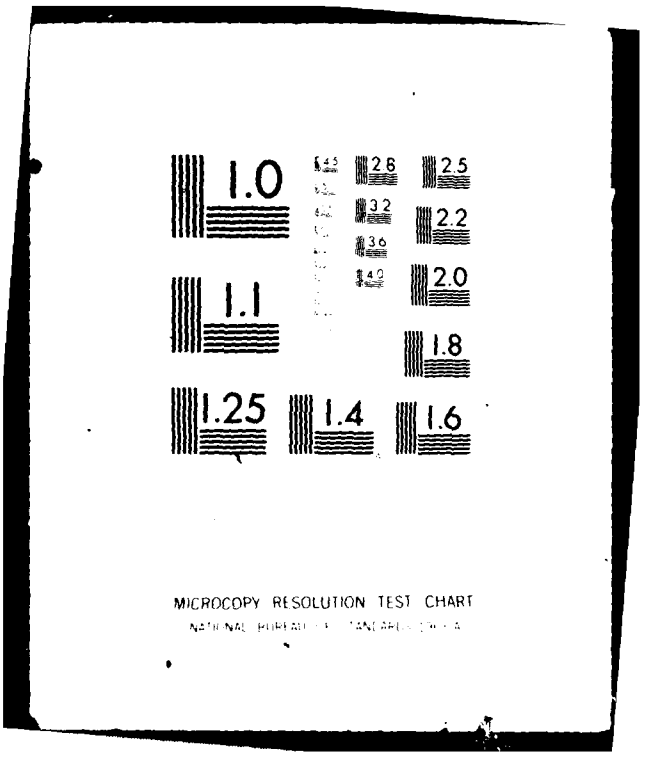
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SUBMICRON FETs USING MOLECULAR BEAM EPITAXY

ANNUAL REPORT NO. 3
(August 1979 - August 1980)

Prepared by:

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Electron-beam exposure and MBE material have been used to achieve quarter-micron gate length GaAs FETs. A noise figure of 1.2 dB with an associated gain of 13 dB has been measured at 8 GHz.

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FOREWARD

The work reported here was supported by the Office of Naval Research, Washington, D.C., under contract N00014-77-C-0655, and managed by Mr. Max Yoder. The program was aimed at developing FETs with gate lengths of around 0.25 micron and looking for any evidences of velocity overshoot.

The work was carried out in the Varian Corporate Research Solid State Laboratory. The authors wish to thank M. Pustorino, C. Hooper, H. J. Lee, S. Lombardi, and J. Dully for technical assistance. The Varian Vacuum Division is gratefully acknowledged for providing the MBE-360 system used in this work. Valuable discussions with M. Yoder and R. L. Bell are gratefully acknowledged.

SUMMARY

Using electron-beam exposure and MBE GaAs, FETs have been fabricated with gate lengths of around 0.2 micron. A noise figure of 1.2 dB with an associated gain of 13 dB has been measured at 8 GHz. Problems with gate and source resistance appear to be limiting the performance. A new technique to increase the gate cross-sectional area and a study concerning the problem of g_m compression are described. A theoretical treatment of the minimum noise figure with respect to source inductance is also given, showing the importance of decreasing it for frequencies above X-band.

TABLE OF CONTENTS

I. INTRODUCTION

A portion of the Introduction to Annual Report No. 2 will be repeated here, followed by a brief summary of the accomplishments up to the end of that reporting period and the problem areas to be dealt with as perceived at the start of this reporting period.

"Transient velocity overshoot" was proposed by Ruch[1] in 1972 to explain why GaAs, while having only a marginal advantage over Si with regard to the saturated drift velocity in the high field region (Fig. 1), is able to outperform Si in a FET structure. Cold electrons injected at the source may never reach their steady-state velocity before being collected at the drain, but travel at a higher velocity, approximately

$$v = \mu_o E \qquad (1)$$

where μ_o is the low field mobility, before relaxation effects take place. This transient phenomenon is due to the disparity between the energy and momentum relaxation times, causing the average velocity in the channel to overshoot its usual saturation value.

Figure 2 shows a computed plot of velocity vs. distance down the channel for both GaAs and InP, assuming a constant field.[2] These plots illustrate the significant role that velocity overshoot can play in increasing the effective electron velocity in submicron gate devices. Silicon also shows velocity overshoot, but the improvement is much smaller and would require gate lengths less than 1000 Å to realize it.[1] It may thus be possible to increase the effective saturated velocity in the FET channel without resorting to "super velocity" materials, by reducing the gate length of GaAs FETs.

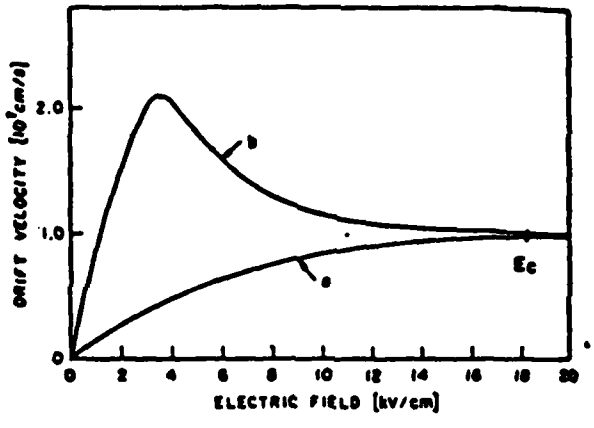


Fig. 1 Velocity-field characteristics in GaAs and silicon.[1)]

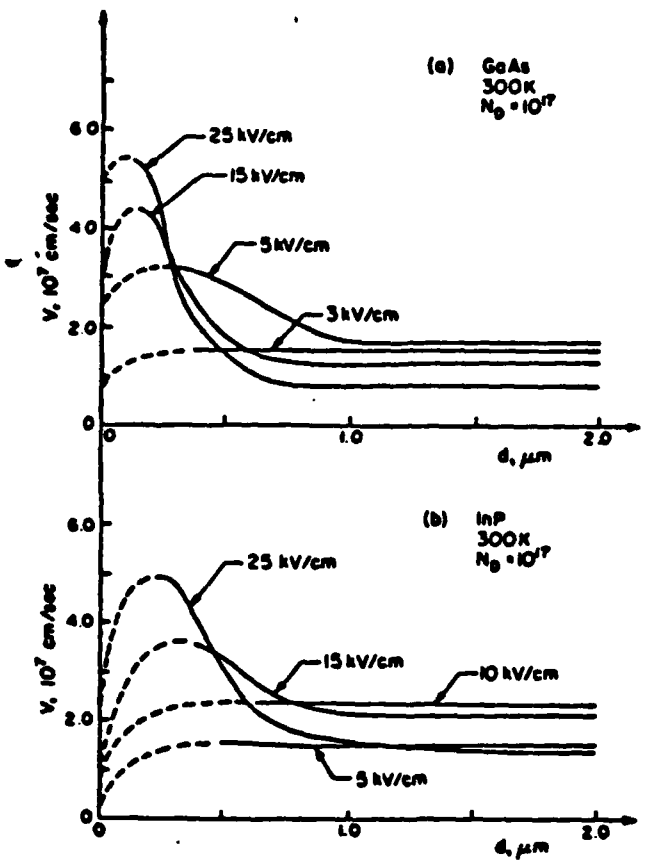


Fig. 2 Instantaneous velocity vs distance for 300°K, $N_a = 10^{17}$; (a) GaAs, (b) InP.[2]

It may well be that the proposed performance advantages of "super velocity" alloys such as InGaAsP will only be realized by the mechanism of velocity overshoot. As shown by the computations of Littlejohn, et al.[3] in Fig. 3, while the computed static velocity-field characteristic of InGaAsP shows a higher low field mobility, which can be utilized by velocity overshoot according to Eq. (1), the velocity in the high field region is less than that of GaAs. Thus, the investigation of the transient effects of velocity overshoot for other materials such as InP, InGaAs, InGaAsP and other promising materials is also a matter of importance.

In addition to the benefits available from higher carrier velocities in the channel, FET performance is, of course, improved directly by scaling down dimensions. However, besides the ability to provide quarter-micron openings in resist with electron beam photolithography, the gate metallization scheme must preserve the resist profile, the active layer must be thinner to prevent g_m reduction (Annual Report No. 1 of this contract), and the effective source-gate spacing must be reduced to avoid source resistance domination. In addition to all this, it may be that a reduction in device width or the addition of multiple gate pads may be necessary to overcome the increased gate resistance brought about by using such small gate lengths. If a narrower-width device is used, it may be necessary to integrate a driver FET of larger dimensions on the same ship to drive the off-the-chip parasitics involved in the realization of practical broadband microwave amplifiers (being a second stage, its gain and noise figures are of less importance).

Concerning the progress in rf performance at the start of this reporting period, a minimum noise figure of 1.5 dB with an associated gain of 15 dB had been achieved. These results were the best obtained for MBE material as reported in the literature to date. This was primarily accomplished by a reduction in gate length. The parameter limiting device performance was primarily the gate resistance, which was high because of the small gate metal cross section, caused in turn by

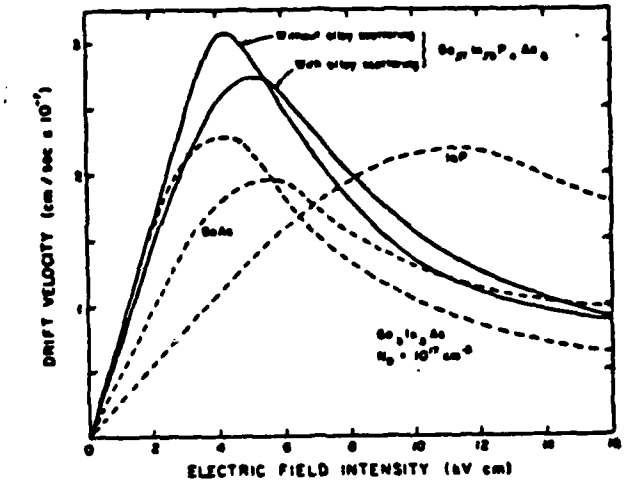


Fig. 3 Velocity-field characteristic of $Ga_{0.27}In_{0.73}P_{0.4}As_{0.6}$ with and without random potential alloy scattering. Shown for comparison are the velocity-field curves for GaAs, InP, and $Ga_{0.5}In_{0.5}As$. The doping level is $10^{17} cm^{-3}$. 3)

the resist opening being gradually closed by metal buildup on the resist edge during the evaporation. Efforts to plate up the gate were not successful, and a new mask design using two gate pads to lower the gate resistance had been implemented, but improved performance had not been realized because of the longer gate length dimensions (the result of using a new mask set and using a new computer with its different writing speed). Also, R_s appeared to be significantly higher than it should be from theoretical considerations by about a factor of 3 or 4.

The high doping of the n^+ contact layer prevented profiling the wafer for doping. Even with the n^+ layer etched off or using a wafer grown without the n^+ layer for calibration purposes, Schottky-barrier leakage prevented good profiles from being obtained. This problem seemed always to occur with MBE material, but virtually never with VPE material. The uncertainty in the exact doping profile of the MBE layers was dealt with by monitoring the channel current as the gate region was thinned. It appeared that better noise figures resulted when the active layer was thinned below its 1200 Å as-grown thickness, thereby diminishing the importance of stopping the thinning abruptly at the n^+-n interface.

The first task to be addressed on the current phase of the contract was to reduce the gate length with the new mask set. Once the equivalent gate resistance, r_g, falls below the source resistance R_s, R_s should be more thoroughly investigated as to why it is not as low as it theoretically should be. As to the term $g_m L_s/C_{gs}$ (where g_m is the transconductance, L_s the source inductance, and C_{gs} the gate capacitance) that is a part of the input resistance r_{in}, it is not certain if this term should be included when computing the minimum noise figure. So far it has been, and it can only be reduced by reducing L_s. Figure 4 shows a geometry that might be used to reduce L_s through the use of plated-through source contacts from the back side. Figure 4 also shows how a further reduction in gate resistance can be made through the use of multiple gate connections.

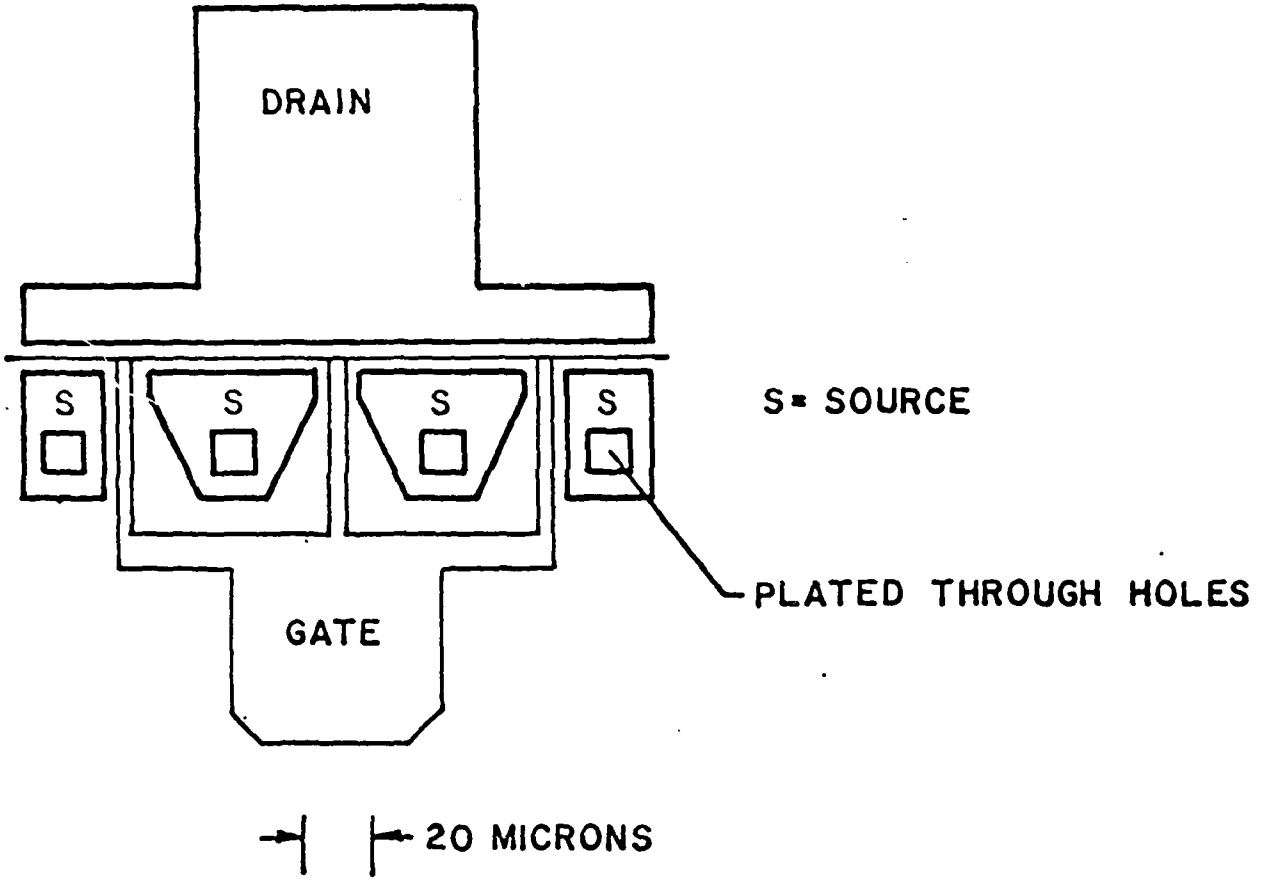


Fig. 4 Plated-through source geometry.

Once r_g and R_s have been sufficiently reduced to allow study of the properties of the intrinsic device, the ultimate goals of this contract can be addressed:

(1) determination of the optimum channel thickness and doping for a given gate length,

(2) fabrication on different crystalline orientations to observe any anisotropy of the electron velocity overshoot effect that may occur; this will be done by determining the effective saturation drift velocity, v_s, by the techniques developed under ONR Contract N00014-77-C-0125[4] and described in the final report of that contract,

(3) evaluation of the use of an MBE AlGaAs buffer layer for carrier confinement to the active layer.

2. DEVICE FABRICATION AND EVALUATION

2.1 Brief Summary

Table I gives a compilation of the device results obtained during this reporting period. The best performance was obtained for run EB 26 for which minimum noise figures, NF_m, as low as 1.2 dB with associated gains, G_a, of 13 dB were measured at 8 GHz. The previous best results were NF_m = 1.5 dB and G_a = 15 dB at 8 GHz, accomplished with run EB 16.

All of the devices were fabricated with the process shown in Fig. 5 using the dual gate pad geometry of Fig.6 (with the exception of run EB 19 which was reported in the previous report, but was included in Table I to include the results of the s-parameter measurements made for device 19-5 during this period). Figure 7 shows the typical channel profile obtained for all the runs. A comparison of Table I with Table I of the previous annual report reveals a reduction in the input resistance r_{in} by about a factor of two by going from the single gate to the dual gate geometry. Whereas 25-40 ohms were measured for the single gate Z = 150 micron devices, 11-20 ohms were measured for the dual gate Z = 150 micron devices. It appears, however, that gate resistance is still a significant portion of the input resistance.

The calculated minimum noise figure, $NF_{m\ calc}$, is computed from the BTL formula[5]

$$NF_{m\ calc} = 1 + kfL^{5/6}\left(\frac{N_D}{a}\right)^{1/6} Z^{1/2}\,(r_g + R_s) \qquad (2)$$

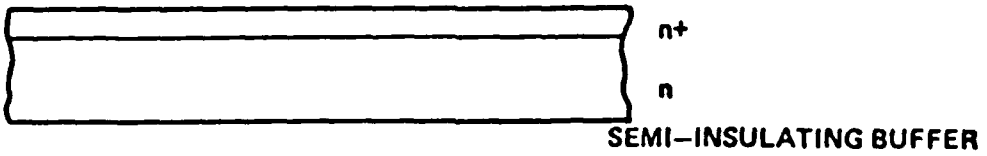
$$= 1 + kfL^{5/6}\left(\frac{N_D}{a}\right)^{1/6} Z^{1/2}\, r_{in}^{1/2}$$

where k = 0.033 for "good" FET material, f is the frequency in GHz, L is the gate length in microns, N_D is the channel doping in units of $10^{16}cm^{-3}$,

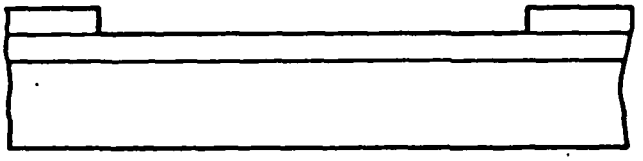
TABLE I

COMPILATION OF DEVICE RESULTS

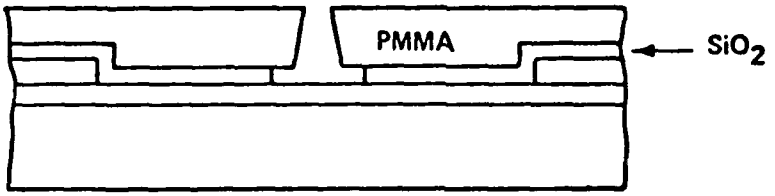
Run	Design	Device	Mag at 8 GHz (dB)	NF_m at 8 GHz (dB)	G_a at 8 GHz (dB)	L (μm)	r_{in} (ohms)	R_s (ohms)	V_p (V)	NF_m calc (dB)	v_s 10^7 cm/sec
EB 19	Z = 75 μm		15 - 16								
		19-2				0.55	15.1		1.3	1.6	
		19-3		2.13	11.3	0.36		9.7			
		19-4	16 at 12 GHz								
		19-5		2.4	10.6	0.335	18.1	7.2	1.8	1.19	
EB 22	Z = 150 μm										
		22-1					22.5				
	Dual gate pad	22-2		2.3	10.4	~0.35					
		22-3		2.12	11.0	~0.35					
EB 23	"	23-1		2.49	10.8						
		23-2		1.65	12.0	0.195	19.4	4.8	1.1	1.19	
		23-3		1.73	13.2	0.26	11.2	6.0	1.1	1.15	
		23-4		1.7	12.6	0.23	16.5	4.7	1.2	1.25	
		23-5							1.1		1.23
EB 25	"	25-1	14.5	2.37	11.9						
		25-2	14.8	2.67	14.3						
		25-3		2.04	13.6						
		25-4	16.0	1.48	14.2						
		25-5	17.1	1.62	13.9						
EB 26	"	26-1	15.8	1.45	13.5		20.4	6.35			
		26-2	16.2	1.54 (1.27)	14.0 (12.8)		16.4	6.15			1.3
		26-3	16.7	1.45	12.6	0.19					
		26-4		1.19	13.1	0.16	15.8			0.965(1.14)	
		26-5		1.19 (1.31)	13.2 (13.3)		12.9	5.2			1.37
EB 27	"			1.53	11.9						
				1.64	12.6						
EB 28	"	28-1		1.79	10.9						
		28-2		1.75	12.4						
		28-3		1.67	13.9						
		28-4		1.86	11.4						
BF 15-12	"			3.15	10.4						



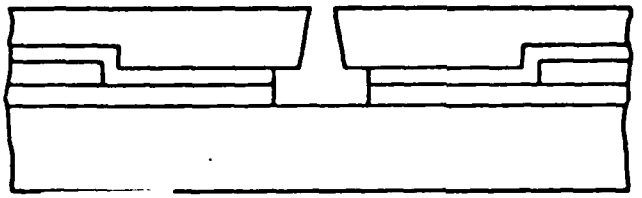
(a) STARTING MATERIAL



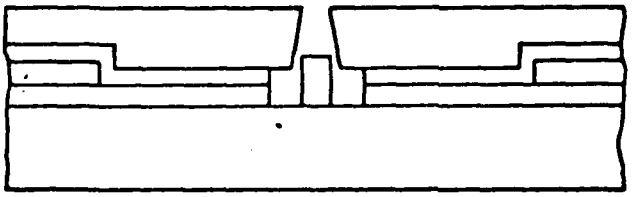
(b) OHMIC CONTACTS



(c) GATE DEFINITION



(d) CHANNEL ETCH



(e) GATE DEPOSITION

Fig. 5 FET fabrication process.

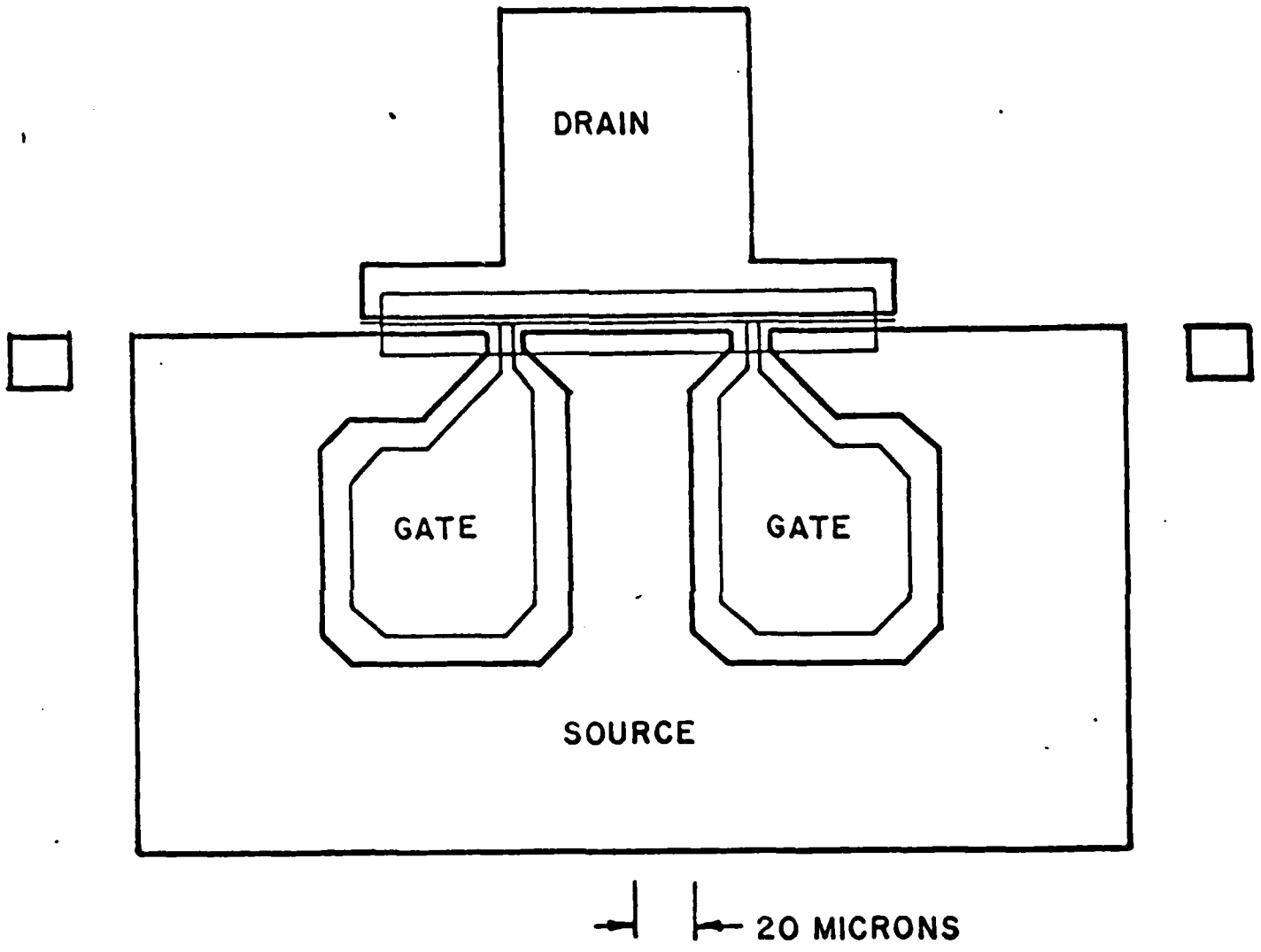


Fig. 6 Dual gate pad geometry.

Fig. 7 Cross section of gate channel area.

a is the active layer thickness in microns, and Z is the gate width in mm. r_{in} is the input series resistance of the FET, which includes the intrinsic channel resistance r_c and the parasitic gate and source resistances r_g and R_s, respectively. The value of r_{in} is determined directly from the s-parameter measurements using

$$r_{in} = r_{11} = \frac{g_{11}}{g_{11}^2 + (b_{11} + b_{12})^2} \qquad (3)$$

which is considered to be far more accurate than deducing it from such parameters as the specific contact resistance of the ohmic contacts , the resistivity of the gate metallization, and the gate metallization cross-sectional area, which is the technique used by BTL in applying Eq. 2.

A new microstrip jig was fabricated which enabled both the s-parameters and the minimum noise figure to be measured on the same device without re-diebonding (which usually destroys the device). The source leads remain intact also, and only the gate and drain leads need to be loosened and re-attached on the ends opposite from the FET pads. This avoids the problem of trying to deduce the performance of one set of devices from the parameters of another set of devices by making assumptions on how their differences should be handled. As shown in Table I, this new jig enabled both rf and s-parameter measurements to be ma e for device EB 19-5 and nearly all of the devices of runs EB 23 and EB 26.

The effective saturated drift velocity v_s in Table I is determined from a plot of the drain current I_d vs $\sqrt{\phi_B - V_g + I_d R_s}$ where ϕ_B is the built-in gate voltage and V_g the gate bias. The slope of this plot is directly proportional to v_s at the depletion region edge.[4]

2.2 Detailed Commentary on the Device Runs

With the exception of the run done with VPE material, all of the device runs used MBE material having a one-micron buffer layer, a 1200 Å thick n-type active layer doped $3.5 \times 10^{17} cm^{-3}$, and an n^+ contact layer doped greater than $10^{19} cm^{-3}$. The material parameters are nominal (intended) and were seldom checked, primarily because of the difficulty in profiling the MBE material (mentioned in previous reports). All growths were done at 581°C.

Run EB 19 was described in the previous report and is included in Table I to give the results of the s-parameter data for device 19-5 using the new microstrip jig which enabled both the s-parameters and the minimum noise figure to be measured for the same device. This run was made on MBE wafer #189, which used SnTe doping for both the n and the n^+ layers using the same SnTe furnace.

Run EB 22 used MBE wafer #190 which also used SnTe doping for both the n and n^+ layers using the same SnTe furnace. The adherence of the gate metal for EB 22 was not good, as evidenced by wiggles in the gate stripe. Difficulty in optically determining whether or not the gate exposures were good and difficulty in seeing the SiO_2 edge to determine when to cease etching plagued these runs. These were results of the new mask set and using a new computer with its different writing speed.

Run EB 23 used MBE wafer #239 which used SnTe doping for both the n and n^+ layers, but with different SnTe furnaces to eliminate the need to wait approximately an hour between growths for the SnTe furnace to equilibrate to the higher temperature needed to grow the n^+ layer.

Run EB 25 used MBE wafer #259 which used Sn for the active layer and SnTe for the n^+ layer (the switch to Sn was in order to duplicate wafer #126 which gave the low noise figures of run EB 16.)

Many of the devices from run EB 25 exhibited g_m compression near zero gate bias, with one such characteristic being shown in Fig. 8. Figure 9 shows the drain characteristic of an uncompressed device. It is to be noted that whether compressed or uncompressed, the g_m's of both devices are very high (54 mmho for Fig. 8 and 58 mmho for Fig. 9). Both types of devices have about the same saturation current and the same pinch-off voltage, but the g_m/step is reversed for each. It seems that part of the compression problem can be seen in the gate forward characteristic. Figure 10 shows the forward characteristic for the compressed device, while Fig. 11 shows it for the uncompressed device.

It appears that the higher g_m may be due to higher channel doping as indicated by assuming $v_s = 1.3 \times 10^7$ cm/sec and computing a value of $3.9 \times 10^{18} cm^{-3}$ from a plot of I_d vs $\sqrt{\Phi_B - V_g}$. Run EB 25 was made from MBE wafer #259 which supposedly was a repeat of wafer #126, except for the n^+ layer which was done with SnTe and doped very high ($>10^{19} cm^{-3}$). For the active layer, the same Sn settings were used as for run #126, but because of an intervening Sn crucible change, the same temperature settings evidently resulted in a much higher doping.

Figures 8 and 9 were obtained from devices on the unscribed wafer. After scribing and bonding into the amplifier circuit to obtain the results in Table I, the g_m's had degraded to around 30 mmhos. Further effort on understanding the problems of run EB 25 was not deemed useful, since they seem to be peculiar only to this run.

Run EB 26 used MBE wafer #239, which was also used for run EB 23. The devices of Table I were first bonded into an amplifier circuit to obtain the above data, then rebonded for s-parameter measurements, and then two of the devices were rebonded back into the amplifier circuit to obtain the values shown in parenthesis. Perhaps EB 26-2 was not tuned well enough the first time, and perhaps EB 26-5 had deteriorated a bit

Fig. 8 Drain characteristic of compressed device.

Fig. 9 Drain characteristic of uncompressed device.

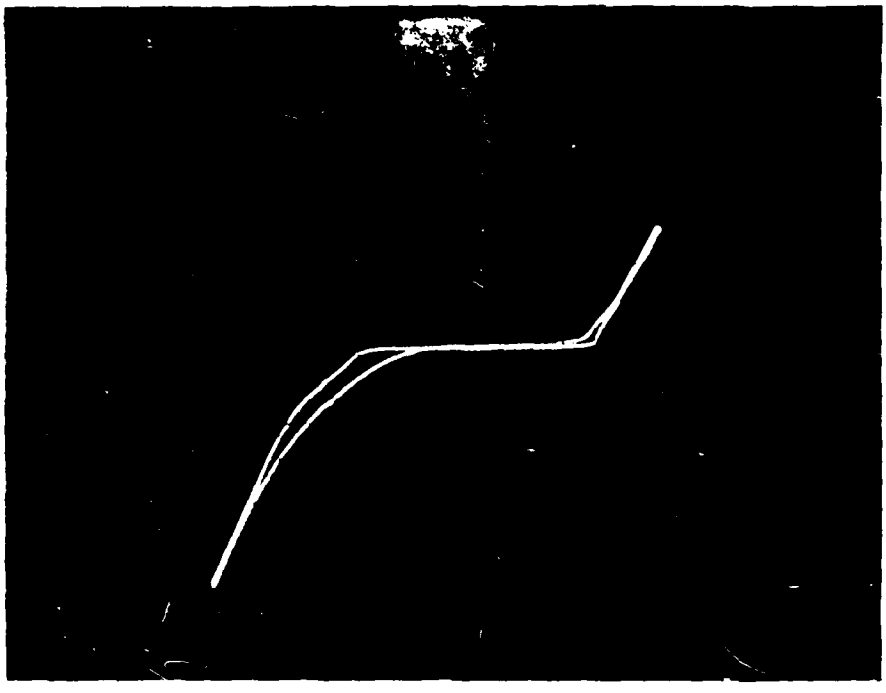


Fig. 10 Forward characteristic of compressed device.

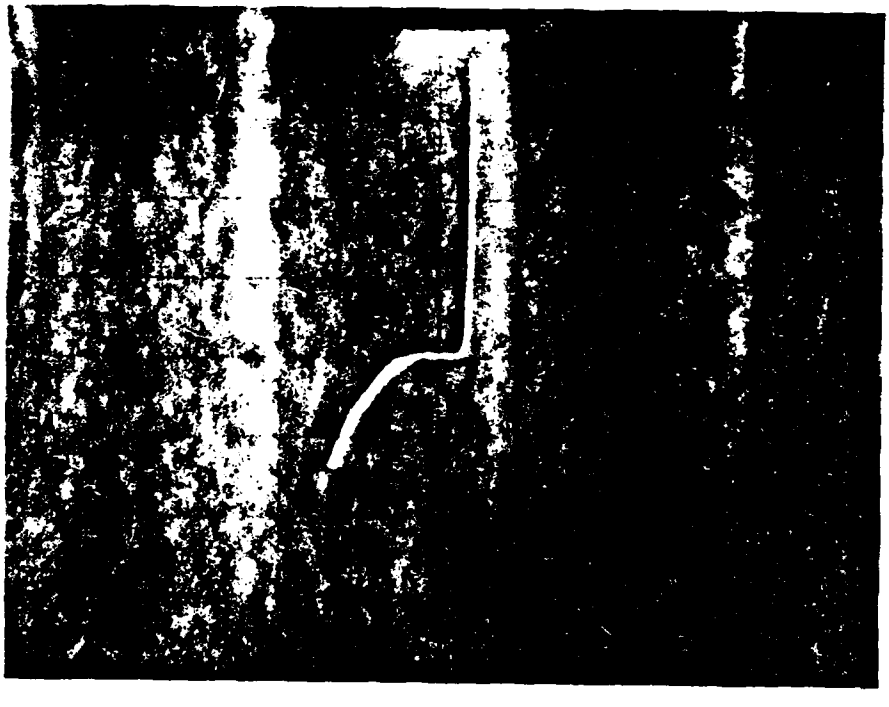


Fig. 11 Forward characteristic of uncompressed device.

from the many rebondings. It is not certain how much significance should be placed on a 0.1-dB difference when the noise measure is 2.6 dB. This run, then, has yielded the best noise figures yet on this program.

The gate lengths for 26-3 and 26-4 were measured because they had already been destroyed in the R_s measurement (measurement of the gate length in the SEM invariably degrades the device). The s-parameter data for 26-3 was found to be inconsistent, and r_{in} could not be determined. As a result, NF_m could only be computed for 26-4 and is shown in the table. Although v_s was only computed for the two devices shown, these values were considered to apply to all of the devices since the drain characteristics for 26-1 and 26-5 were virtually the same, as were also the drain characteristics for 26-2, 3 and 4.

Run EB 27 was made on MBE wafer #315, which used Si for the active layer dopant and SnTe for the n^+ layer dopant. Si doping has been found to give 20% higher mobilities than either Sn or SnTe, and its doping level is independent of the substrate growth temperature. SnTe was still used for the n^+ layer, since Si is unable to achieve the high doping that SnTe can. The channel was thinned too much, resulting in low values of current (8-10 mA) and also the gates were fairly long (0.3-0.5 micron).

Another run (run EB 28) was made on MBE wafer #315 to evaluate the merits of Si doping, but without the excessive thinning of run EB 27. For the two best runs to date (runs EB 16 and 26), Table II shows that the minimum noise figure always occurred at $I_d \simeq$ 12-19 mA with only a second-order dependence upon I_{dss} which ranged from 15 to 41 mA. While run EB 27 had been thinned to 10-15 mA, run EB 28 was thinned to 20-25 mA. The high noise figure values may be due to high gate resistance and/or long gate lengths. No analysis was done on this run.

TABLE II

BIAS AT MINIMUM NOISE FIGURE

Device	NF_m (dB)	G_a (dB)	V_d (V)	V_g (V)	I_d(mA)/I_{dss}(mA)
16-1	1.55	13.8	2.29	-0.825	19/41 = 0.463
16-2	1.47	15.7	1.9	-0.125	14.5/18 = 0.805
16-3	1.45	14.3	2.16	0	15.2/15.2 = 1.0
26-1	1.45	13.5	2.4	-0.25	14/20 = 0.7
26-2	1.54	14.0	2.3	-0.177	13.5/18 = 0.75
26-3	1.45	12.6	2.4	-0.24	19.5/25 = 0.78
26-4	1.19	13.1	1.92	-0.204	12/17 = 0.705
26-5	1.19	13.2	1.97	-0.3	13/21 = 0.62

A VPE wafer (TRS 55-22) with no buffer layer or n^+ layer was used to see if NF_m occurring near I_{dss} is peculiar to the MBE material. The currents were low (8-10 mA), and the bias point for NF_m occurred near I_{dss} just as it does for the MBE material devices in Table II.

In order to assess any differences between MBE and VPE material, several device runs were made on VPE wafer #BP 15-12. This wafer used Te doping to minimize diffusion, and had a 6-micron buffer layer, a 0.3-micron active layer doped $10^{17}cm^{-3}$, and a 0.3-micron n^+ layer doped around $10^{18}cm^{-3}$. The first device run on this material was made in parallel with the device run on MBE wafer #314, but resulted in conduction between adjacent devices due to an insufficient mesa etch, a result of the very thick layers. The second device run was done in parallel with the device run on MBE wafer #315, with the gate region being thinned down to give the same current as the MBE devices. The resulting devices had g_m compression, perhaps being due to the deep gate recess (~0.4 micron). This makes it more difficult to clean out any residue that remains in the recess prior to the gate evaporation. One device from this run gave the data shown in Table I. A third try was made on the VPE material, but it appears that because of the high mesa height (the n^+ and n layers combined were 0.6 micron thick), the gate exposures were ill-defined and lack sharpness.

Further details of the device runs included in Table I are covered in the following sections which deal with the specific problem areas concerning minimum noise figure, g_m falloff with frequency, gate resistance and g_m compression.

III. MINIMUM NOISE FIGURE CONSIDERATIONS

All of the devices in Table I have a significantly smaller value of calculated NF_m than was actually measured, with the discrepancy being about 0.5-0.6 dB. This discrepancy is especially significant for run 23 where three devices all have about the same value of measured NF_m. Using the parameters measured for these same devices, they all have about the same value of computed NF_m. Although the computed NF_m for device EB 26-4 is only about 0.2 dB below the measured value, it cannot be certain that this close agreement is characteristic of run EB 26 since the result is only for one device (due to reluctance to measure L and thus destroy the remaining devices which have given the best results to date). This is the first time that such a discrepancy has been consistently demonstrated with so many devices from the same run (mainly as the result of the new microstrip jig) and suggests that a closer examination be made as to why better values of NF_m are not measured.

First of all, is the BTL formula given by Eq. (2) an accurate descriptor of the values actually measured? BTL claims it is, as does Avantek[6] and perhaps others. Maybe the amplifier microstrip jig used is incapable of the optimum noise match, or maybe the losses in the matching networks are improperly accounted for. These latter two cases are not felt to be the reasons, especially to the extent to account for the 0.5-0.6 dB differences observed. With regards to Eq. (2), the possibility exists of the use of values for the parameters which are in error. However, L is measured directly by the SEM for each device and r_{in} is determined from the s-parameter measurements, so one would not expect these parameters to be in much error. Z and f, of course, can be expected to be quite accurate. The channel doping N_D is assumed to be $3.5 \times 10^{17} cm^{-3}$ based upon earlier dummy runs, and the channel thickness, a, is then determined by direct measurement of the pinchoff voltage. Although the assumption for the value of N_D may be in error by at most a

factor of 2 or so, $2^{1/6} = 1.12$ which is close enough to unity to be insignificant. According to BTL, $k \cong 0.033 - 0.036$ for "good" material in the early paper,[5] but was revised to 0.04 in a later paper.[7] A value of 0.033 was used for the data in Table I. If 0.04 were used, $NF_{m\ calc}$ would increase by about 0.2 dB for run EB 23.

To evaluate the quality of material used for FET fabrication, a technique has been developed whereby the drain current, I_d, is plotted as a function of $\sqrt{\phi_B - V_g + I_d R_s}$.[4] The slope of this plot yields the effective saturated drift velocity, v_s, in the channel across its depth. Figure 12 shows such a plot for a device from run 23, and with $N_D = 3.5 \times 10^{17} cm^{-3}$, a value for v_s of 1.23×10^7 cm/sec was obtained from the slope. This value is essentially equal to the 1.3×10^7 cm/sec value obtained for what is considered "good" material for the longer gate length FETs made in this laboratory using VPE and MBE material. Values of around 1.3×10^7 cm/sec have been obtained for all the other EB runs made previously and so the material quality was considered "good" for those runs. However, if the assumed doping value is inaccurate, or if velocity overshoot is increasing v_s above what is would be for a longer gate length, then perhaps the material cannot be considered "good" and a larger value of k should be used in Eq. (2). If 1.3×10^7 cm/sec is the appropriate value, this would indicate the absence of any evidence for velocity overshoot for these submicron-gate-length devices. The values of NF_m were measured at values of gate bias ranging from -0.4 to -0.6V, and Fig. 12 reveals a "tail" in the plot beginning at about -0.6V which gives increasingly lower values of v_s as the gate bias proceeds further. The fact that the active layer is grown in-situ along with a one-micron-thick buffer layer and also that a slight tail is always seen in such plots even for the best of material are reasons for assuming that v_s retains its value all the way to the active layer-buffer layer interface. On the other hand, this tail may indicate degradation of v_s near the interface and explain why NF_m occurs at the gate bias it does. It doesn't seem reasonable that Cr out-diffusion from the substrate would affect the active layer only near the interface after diffusing through the buffer layer.

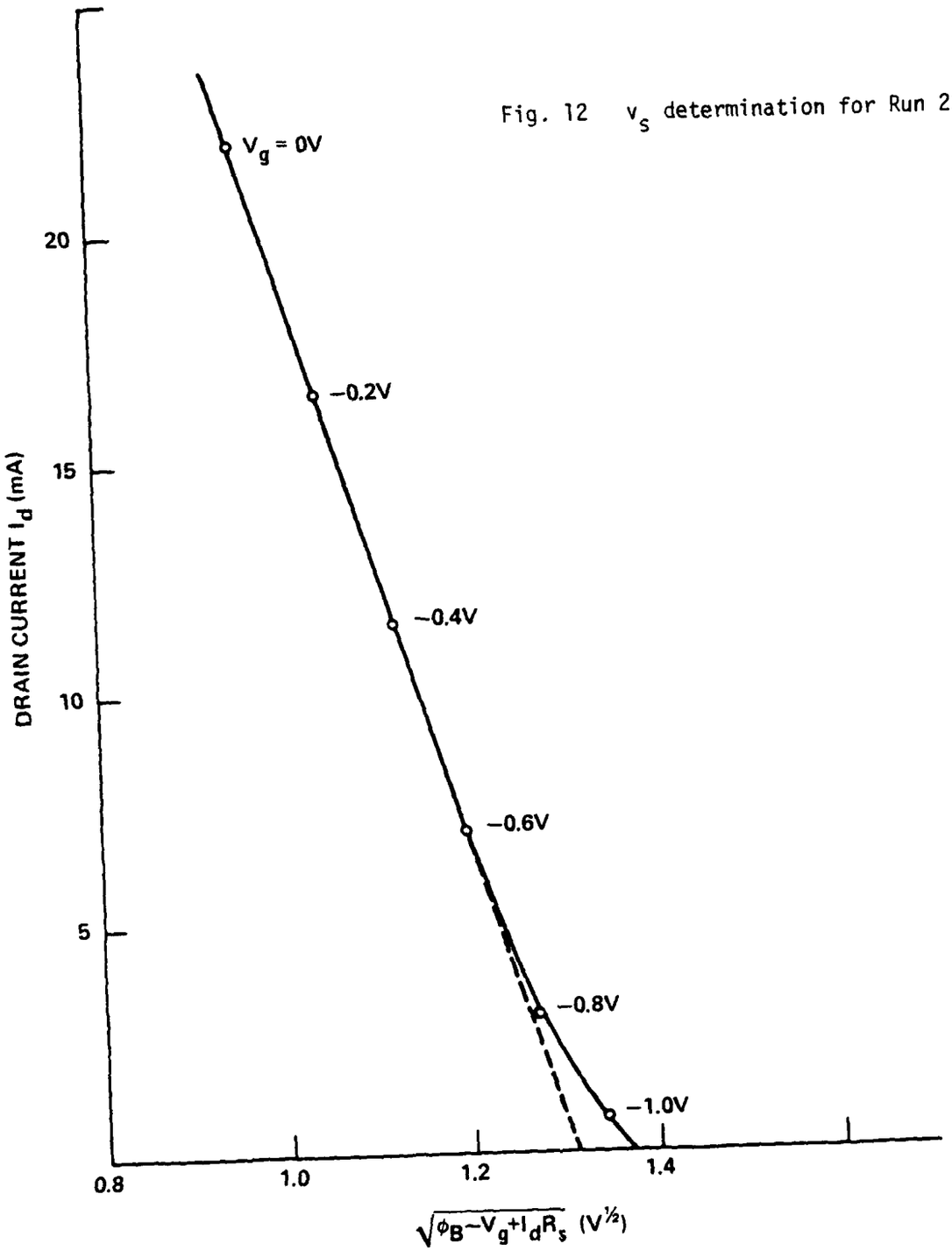


Fig. 12 V_s determination for Run 23.

The following sections deal with whether or not $g_m L_s/C_{gs}$ should be included in Eq. (2), whether the replacement of $r_g + R_s$ by r_{in} is valid in Eq. (2) considering the distributed nature of the input, and whether g_m falloff with frequency is indicative of inferior material quality.

3.1 Minimum Noise Figure Dependence on Source Inductance, L_s

The point to be determined is whether it is correct to include $g_m L_s/C_{gs}$ as part of r_{in} when using Eq. (2) to compute $NF_{m\ calc}$ as has been done for the values in Table I. If not, the values of $NF_{m\ calc}$ will be significantly lower, since $g_m L_s/C_{gs}$ is a sizeable fraction of r_{in} as Table III clearly shows. Does the Fukui formula ignore L_s or does it truly not belong in Eq. (2)? The only way to find out is to derive NF_m with L_s included in the noise model.

For the simple FET noise model shown in Fig. 13, where $r \cong r_g + R_s + r_c$ (r_c is the intrinsic channel resistance) and R_{sn} and X_{sn} are the source resistance and reactance for optimum noise match, the noise figure is given by

$$MF = 1 + \frac{\overline{e_{in}^2}}{\overline{v_{sn}^2}} + \frac{\overline{i_d^2}\,\omega^2 C_{gs}^2}{\overline{v_{sn}^2} g_m^2}\left[\left(R_{sn} + r + \frac{g_m L_s}{C_{gs}}\right)^2 + \left(X_{sn} - \frac{1}{\omega C_{gs}} + \omega L_s\right)^2\right] \qquad (4)$$

Obviously, the optimum value of X_{sn} is $\frac{1}{\omega C_{gs}} - \omega L_s$, so inserting this into Eq. (4) and setting $\partial NF/\partial R_{sn}$ equal to zero gives the optimum value for R_{sn} as

$$R_{sn} = \sqrt{\frac{r + A^2 B}{B}} \qquad (5)$$

where

$$A = r + \frac{g_m L_s}{C_{gs}} = r_{in}, \text{ the real part of } z_{11} \qquad (6)$$

TABLE III

INPUT RESISTANCE BREAKDOWN

Device	r_{in} (ohms)	$g_m L_s / C_{gs}$ (ohms)	R_s (ohms)	r_g (ohms)
19-2	15.1			
19-5	18.1	4.0	7.2	6.9
23-2	19.4	6.18	4.8	8.42
23-3	11.2	4.66	6.0	0.54
23-4	16.5	5.8	4.7	6.0
26-1	20.4	4.35	6.35	9.7
26-2	16.4	4.48	6.15	5.77
26-4	15.8	6.24		
26-5	12.9	4.83	5.2	2.87

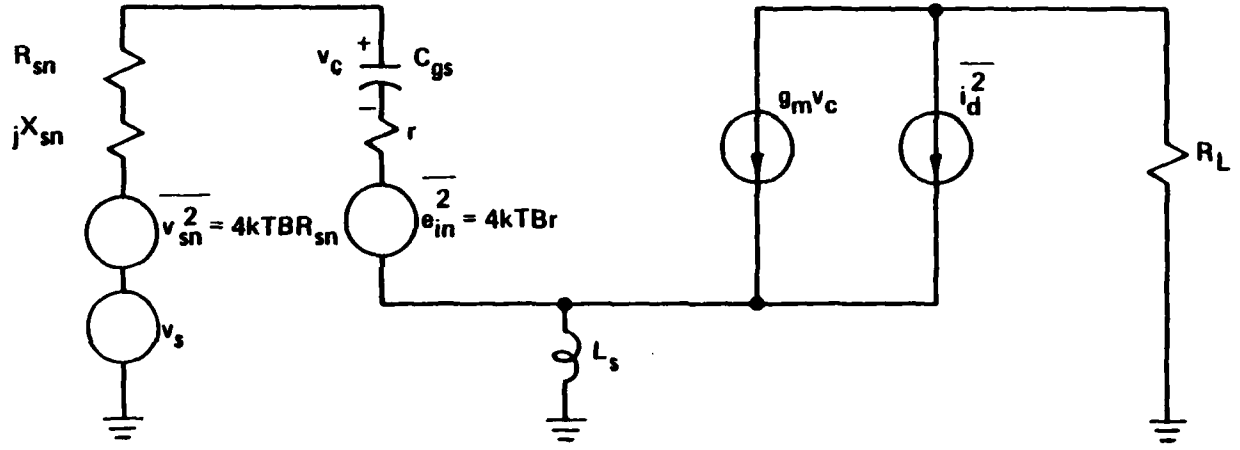


Fig. 13 Simple FET noise model which includes the effect of source inductance.

$$B = \omega^2 C_{gs}^2 R_{eq} \tag{7}$$

$$R_{eq} = \frac{i_d^2}{4kTBg_m^2} \tag{8}$$

R_{eq} is the result of the common practice of referring the output noise to the input with an equivalent noise resistance.[8] Substitution of Eqs. (5), (6), and (7) into Eq. (4) gives the minimum noise figure NF_m as

$$NF_m = 1 + 2r_{in}\omega^2 C_{gs}^2 R_{eq} + 2(r\omega^2 C_{gs}^2 R_{eq} + r_{in}^2 \omega^4 C_{gs}^4 R_{eq}^2)^{1/2} \tag{9}$$

Podell[9] has found empirically for one-micron gate length FETs that

$$R_{eq} = \frac{1.25}{g_m} \quad . \tag{10}$$

Using Eq. (10) in Eq. (9) along with parameter values at 8 GHz for run EB 26 results in all terms but the term containing r being negligible, giving

$$NF_m \cong 1 + 2\omega C_{gs}\sqrt{rR_{eq}} \quad . \tag{11}$$

Inserting Eq. (10) into Eq. (11) gives

$$NF_m \cong 1 + 2.24\,\omega C_{gs}\sqrt{\frac{r}{g_m}} \tag{12}$$

which is nearly identical to Fukui's equation [7]

$$NF_m = 1 + 2.5\omega C_{gs}\frac{r_g + R_s}{g_m} \tag{13}$$

which he uses as a basis to obtain the final expression of Eq. (2). The only differences between Eqs. (12) and (13) are very minor -- the intrinsic

channel resistance r_c is not included in Fukui's equation, and the numerical factor difference can be accounted for by the empirical relationship of Eq. (10). Thus Eq. (9) can be regarded as a more general form of Fukui's equation, which is Eq. (2). Secondly, Eq. (12) indeed shows that $g_m L_s/C_{gs}$ should not enter Eq. (2) and should be subtracted from r_{in}.

$$NF_m = 1 + k\, f\, L^{5/6} \left(\frac{N_D}{a}\right)^{1/6} Z^{1/2} \left(r_{in} - \frac{g_m L_s}{C_{gs}}\right)^{1/2} \qquad (14)$$

As an example, if $g_m L_s/C_{gs}$ were subtracted out from r_{in} for device EB 26-4, $NF_{m\ calc}$ in Table I would be reduced from 0.965 dB to 0.768 dB. If in addition k is also increased from .033 to .04, $NF_{m\ calc}$ becomes 0.912 dB.

Equation (9) indicates that L_s effects will become more pronounced as the frequency increases. Since Fukui's equation appears to be valid at the lower frequencies, it can be used to compute R_{eq}. Setting Eq. (11) equal to Eq. (2) gives

$$R_{eq} = \frac{\left[K\, L^{5/6}\, (N_D/a)^{1/6}\, Z^{1/2}\right]^2}{4\pi\, C_{gs}^{\ 2} \times 10^{-6}} \qquad (15)$$

which enables Eq. (9) to be used at the higher frequencies where Eq. (2) is no longer valid. To continue the example of EB 26-4, at 24 GHz Eq. (14) gives 2.3 dB, while Eq. (9) gives 3.26 dB, illustrating the significance of the higher-order ω terms in Eq. (9).

3.2 Distributed Gate Resistance

If R_g is the end-to-end resistance of the gate stripe and G_s is the source conductance R_s^{-1}, the gate and source resistances are distributed as shown in Fig. 14. For a single gate pad on one end,[10]

$$r_{in} = \sqrt{R_g R_s}\ \coth\sqrt{\frac{R_g}{R_s}} \quad . \tag{16}$$

For $R_g << R_s$, Eq. (16) reduces to

$$r_{in} \cong R_s + \frac{R_g}{3} \quad , \tag{17}$$

which is the form assumed in Fukui's noise figure equation.[11] However, for the short gate length FETs of this contract, $R_g \geq R_s$, so such an approximation may be in serious error. When r_{in} from the y-parameter data is used for $R_s + r_g$ in Eq. (2), Eq. (16) is actually being used for the intended form of Eq. (17). Will this make a significant difference and can this account for at least part of the reason why the measured values of NF_m are higher than the computed values using Eq. (2)? Of course, based on the preceeding development in Sec. 3.1, one could always argue that the form of Eq. (16) is the correct expression that should have been used in Eq. (2) by Fukui in the first place.

For the dual pad gate structure shown in Fig. 6, if R_g and R_s are still the total gate and source resistances, respectively, then for one-fourth of the device width Eq. (16) can be used by replacing R_g and R_s by $R_g/4$ and $4R_s$, respectively. The total input resistance is then found by dividing this result by 4, since there are 4 of these one-fourth segments in parallel. This gives

$$r_{in} = \sqrt{\frac{R_g R_s}{4}}\ \coth\sqrt{\frac{R_g}{16R_s}} \quad . \tag{18}$$

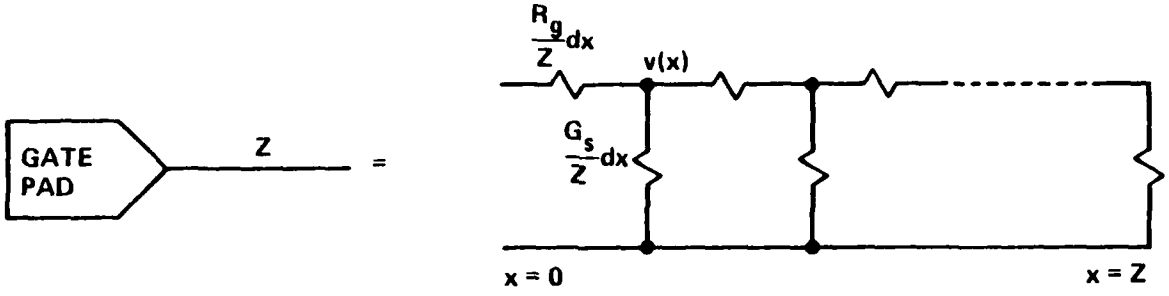


Fig. 14 Model for gate and source resistance distribution.

For $R_g << 16R_s$, Eq. (18) reduces to

$$r_{in} \cong R_s + \frac{R_g}{48} \quad , \tag{19}$$

while for $R_g >> 16\ R_s$,

$$r_{in} \cong \frac{\sqrt{R_g R_s}}{4} \quad . \tag{20}$$

Figure 15 gives a plot of the ratio of Eq. (18) to Eq. (19) as a function of $f = R_g/R_s$. For values of f below about a factor of 50, Eq. (19) is a very good approximation to Eq. (18).

An example of the use of the above formulas are the devices of run EB 26, for which a value of around 6 ohms was measured for R_s. R_s was measured by forward-biasing the gate with respect to the grounded source and measuring the floating drain potential. This technique gives R_s directly, even when the fact that the gate resistance is distributed is taken into account. To this value of R_s should be added the term $g_m L_s/C_{gs}$ and also the intrinsic channel resistance r_c which are both distributed with respect to the gate resistance in the same manner as R_s. g_m and C_{gs} are determined from the y-parameters and L_s is computed from a formula[12] using the appropriate values for the source lead bonds. Typically, it has been found that r_c can be ignored as evidenced by the small change in r_{11} as the gate bias is changed from zero to values approaching pinch-off (see Table II of the previous report on this contract). For device EB 26-4 in particular, R_g was determined to be around 280 ohms from a measurement between the two gate pads. With $g_m L_s/C_{gs}$ determined to be 6 ohms for this device, and ignoring r_c, Eq. (18) gives

$$r_{in} = \frac{\sqrt{280(6+6)}}{4} \coth \sqrt{\frac{280}{16(6+6)}} = 17.3 \text{ ohms} \quad .$$

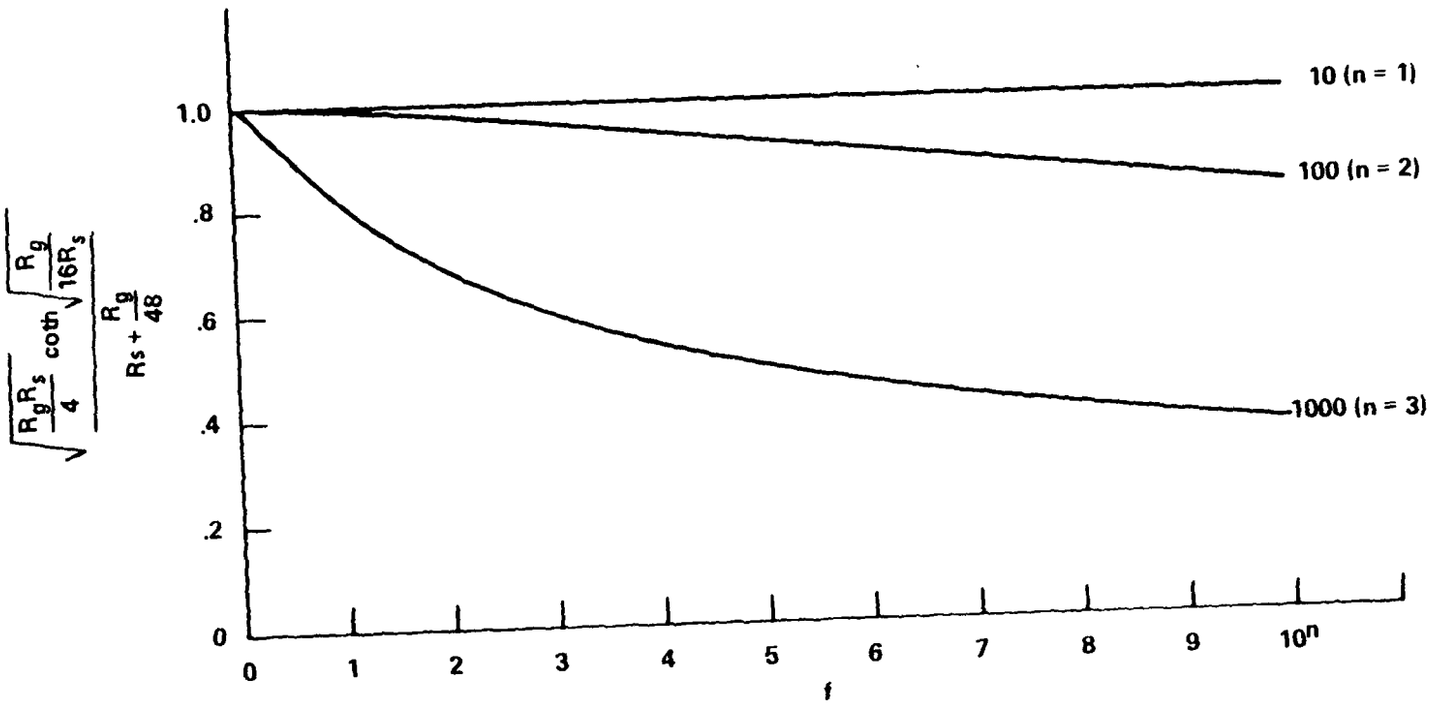


Fig. 15 Degree of fit of approximation to r_{in} with the actual value as a function of $f = R_g/R_s$.

The actual value of r_{in} as given by r_{11} measured from 2 to 10 GHz is 15.8 ohms, which is in good agreement with the value given by Eq. (18). Eq. (19) gives

$$r_{in} = 6 + 6 + \frac{280}{48} = 17.8 \text{ ohms} \quad ,$$

which overestimates the true value, but is still in good agreement. With $f = \frac{280}{12} = 23.3$, Fig. 15 indeed shows the 0.97 factor difference obtained above.

The gate length L of device EB 26-4 was measured to be 0.16 microns and is triangular in cross section as determined by SEM observation. The triangular nature of the gate is a result of the evaporated Au acting as a two-dimensional fluid and flowing out over the edges of the resist opening, to gradually close it off (see Sec. 4). For a measured triangle height of 2700 Å and for a device width Z of 147 microns, upon assuming bulk conductivity for Au ($\rho = 2.44 \times 10^{-6}$ *ohm-cm*),

$$R_g = \frac{2\rho Z}{Lh} = \frac{2(2.44 \times 10^{-6})(147 \times 10^{-4})}{(0.16 \times 10^{-4})(0.27 \times 10^{-4})} = 166 \text{ ohms} \quad .$$

Since R_g was measured to be 280 ohms, evidently the actual resistivity is

$$\rho = 2.44 \times 10^{-6} \ \frac{280}{166} = 4.1 \times 10^{-6} \text{ ohm-cm} \quad ,$$

which is about a factor of 1.7 higher than the bulk value. This is consistent with the factor of 2 found by Fukui[11] for his Al gate.

In summary, in spite of $R_g > 16\ R_s$, the use of Eq. (18) rather than Eq. (19) in computing NF_m (since using r_{11} for r_{in} (Eq. (3)) is in effect using Eq. (18)) does not significantly lower the computed value of NF_m to account for the differences in Table I with the measured values.

Even if it did lower it significantly, it still is the more correct expression to describe NF_m and should have been used by Fukui in place of $R_s + r_g$ in the first place (for the devices he is modeling $r_g << R_s$ so that it made no difference in his case).

3.3 g_m Falloff with Frequency

One of the significant observations made during this period was the reduction in g_m in going from dc to 8 GHz. Table IV gives a compendium of all the devices tested so far for which the frequency dependence of g_m can be inferred. This reduction in g_m at 8 GHz would not seem to be due to capacitive or inductive effects, since g_{21} is relatively constant from 2 to 8 GHz.

These lower values of g_m at 8 GHz probably indicate an increase in the noise figure, as indicated by the g_m dependence of NF_m as expressed in Eq. (13). It seems clear that any g_m reduction could seriously affect not only NF_m but G_a also. Although Table IV reflects only the g_m values at $V_g = 0$, it would be reasonable to conclude that a similar reduction would also occur at the bias used to achieve NF_m.

For many of the devices in Table IV, g_{mdc} was not measured prior to observation in the SEM for gate length determination which invariably degraded g_m, and consequently no values are listed. $NF_{m\ calc}$ was computed for devices EB 16-1 and 19-3 using parameters inferred from the other devices from the same run. All the other values of $NF_{m\ calc}$ used parameters measured for the same device, with devices EB 6-1, 6-5, and 11-3 requiring re-diebonding while devices 19-5, 23-2, 23-3 and 23-4 and all of the devices of run EB 26 used the new microstrip jig mentioned previously. In general, there appears to be a significant reduction in g_m with frequency for all the runs except possibly for run EB 16, which basically is the only run for which $NF_{m\ calc}$ agrees with NF_{mrf} (with the

TABLE IV

SUMMARY OF g_m FREQUENCY DEPENDENCE (V_g = 0)

Device	g_{mdc} (mmho)	g_{mrf} (mmho)	NF_{mrf} (dB)	$NF_{m\ calc}$ (dB)
EB 6-1	32	23.2	2.23	2.14
EB 6-3		30		
EB 6-5	26	22	2.2	2.02
EB 11-3	28	19.6	1.83	1.495
EB 16-1	28		1.55	1.49
EB 16-2	28		1.47	
EB 16-3	28		1.45	
EB 16-4	26	25.0		
EB 16-5		20.3		
EB 16-6		25.3		
EB 19-1		11.5		
EB 19-2		10.0		
EB 19-3	11.5		2.13	1.78
EB 19-5	13.0	11.0	2.4	1.19
EB 21-3	31.0	24.6		
EB 21-4	26.0	21.3		
EB 21-5	32.5	21.0		
EB 22-1		19.5		
EB 22-2	26.0		2.3	
EB 22-3	31.0		2.12	
EB 23-1			2.49	
EB 23-2	28.4	18.0	1.65	1.19
EB 23-3	27.0	18.0	1.73	1.15
EB 23-4	28.0	20.0	1.7	1.25
EB 26-1	27.0	17.5	1.45	
EB 26-2	26.0	15.0	1.54 (1.27)	
EB 26-3	22.5	14.5	1.45	
EB 26-4	25.0	16.0	1.19	.965 (1.14)
EB 26-5	28.2	18.0	1.19 (1.31)	

exception of run EB 6). Table IV stresses the need to understand and solve this problem of g_m reduction with frequency. An inductor and resistor in shunt in the source lead or a capacitor in series with a resistance both across the g_m current generator (see Appendix A) would give the observed frequency dependence, but such models do not seem to have any physical basis in reality. It would rather seem that this phenomenon is related to a materials problem such as back-side gating or deep-level traps. The decrease in g_m with frequency has been attributed by Zylbersztejn et al[13] to hole traps, mostly located on the substrate side of the epilayer/substrate interface. They suggest that this problem is eliminated by going to a buffer layer a few microns thick. Indeed, the MBE material grown using SnTe doping is not trap-free, as evidenced by the constant leakage current beyond pinch-off for Au Schottky-barrier dots (deposited for the purpose of obtaining doping profiles of the active layers). It is because of this leakage current that it is difficult to obtain good doping profiles of the active layers.

If indeed traps are responsible for the reduction in g_m, it would mean that the rf value is the trap-free one and the one that should be used to compute v_s rather than from the dc value. This would mean a lower value of v_s, but then maybe because of the traps perhaps v_s is indeed less than the 1.3×10^7 cm/sec value observed for "good" material. However, it seems improbable that traps could increase the dc g_m for every run just the correct amount so that the "good" value for v_s would result every time.

3.3.1 Backside Gating

To check on the possibility of backside gating being responsible for the reduction in g_m with frequency (i.e., gating of the channel from the buffer layer side which would be expected to be absent in the GHz frequency range, but present at dc), the alignment mark (an ohmic contact on the buffer layer) was probed with the gate floating on

devices from runs EB 23 and 26. It was found that the alignment mark could modulate the channel, even to the point, in some cases, of matching the modulation from the gate pad when the device was exposed to microscope light. Even without light, the alignment mark would modulate the channel, but typically to a lesser degree.

When modulated from the metallized back of the chip, strong modulation of the channel occurs, but unlike the alignment mark modulation, the modulation disappears in the absence of light. However, only minimal modulation (~0.6 mmho) was seen when the gate was grounded, and this became even less when the light was removed. Some devices were found whose gates had lifted off, leaving only an etched channel. When the backside of the metallized substrate was pulsed, a little modulation would be seen with light, but typically the voltage on the substrate would have to exceed a threshold voltage ranging from 2 to 8V. No modulation was seen without the microscope light.

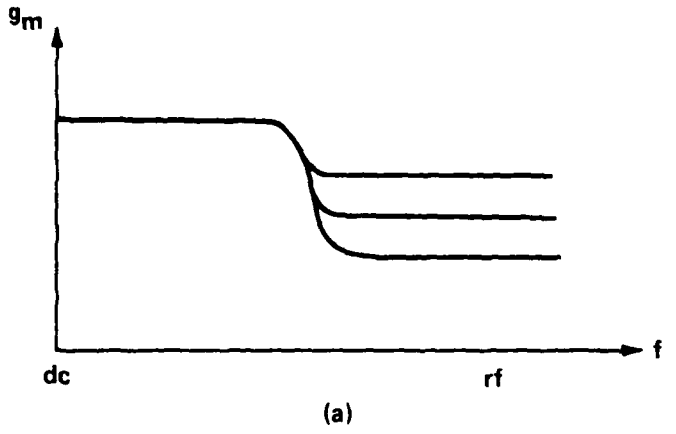
Other devices were observed that had had no gate exposure so that the n^+ layer still remained. Again, by pulsing the backside of the substrate, modulation of the channel current could be seen for some of the devices in the presence of light, while others showed no evidence of modulation. None of the devices showed any evidence of modulation without the microscope light. For those that showed modulation, with an I_{dss} value of ~70 mA, only about 7 mA of modulation was seen as the substrate bias was pulsed from 0 to -20 V. The same data was obtained when the alignment mark was pulsed.

We were surprised to find that the substrates were conducting from any ohmic contact on the top surface (i.e., the alignment mark on the buffer layer on the source and drain contacts on the mesa) to the metallized back side of the substrate. For example, a device from run EB 26 was found to give 5 μA at 20 V and 20 μA at 40 V for a negative bias on the alignment mark (typical of other devices from this run also). When

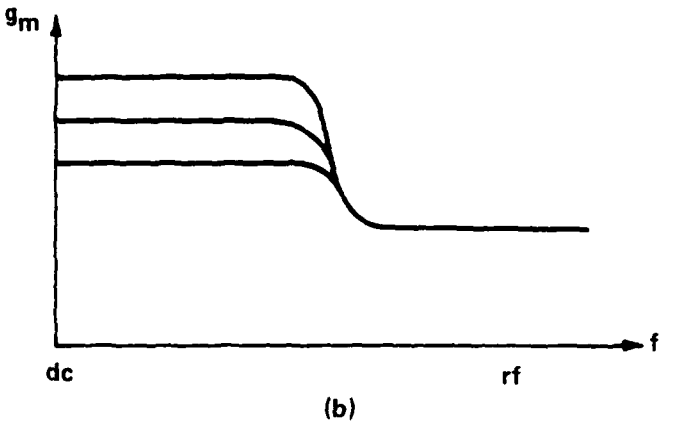
microscope light was incident on the device, the conduction rose a significant amount so that 20 μA was achieved at less than 10 V. Devices from run EB 23 acted the same, as well as devices from previous MBE runs. In fact, this was found to be true of some devices made on VPE material, and even an NEC FET showed this behavior (conduction with light, but none without light for the NEC device)!

By way of summary, no modulation was seen by pulsing either the alignment mark or the substrate that was of the order needed to account for the observed g_m falloff, unless floating gate metallization was present which was connected to the gate pad and usually (but not always) microscope light was incident. Grounding the gate reduces any modulation to a very small amount, and removal of light eliminates even this small amount. All this would seem to suggest little or no backside gating and that the alignment mark is communicating to the gate pad through either a conducting buffer layer or a surface conducting layer produced by microscope light. Perhaps capacitive coupling from the backside to a surface conducting layer and thence to the gate is why the backside modulation occurs. More likely, it is due to the substrate conduction brought on by incident light. Maybe carriers are generated throughout the substrate by the longer wavelength specturm of the microscope light, since it seems unlikely that the diffusion length for holes would be more than at most several microns.

If indeed backside gating was responsible, it would mean that the rf value for g_m was the correct one and the dc value was inflated from its design value; but observation of Table IV shows a much bigger spread in g_m values in the rf range than at dc (26-32 mmhos vs. 14.5-30 mmhos), suggesting the situation shown in Fig. 16a rather than that shown in Fig. 16b. Suposedly, all the devices have the same active-layer doping, so that the dc value rather than the rf value would appear to be the correct value corresponding to the material parameters.



(a)



(b)

Fig. 16 Variation of g_m with frequency illustrating dispersion.

Backside gating would be expected to disperse the g_m values rather than bring them together. Perhaps R_s can explain the variation seen in the dc values. Table I shows that v_s, which is computed from the dc values, shows little variation from run to run, but it certainly would show a much larger variation if the rf data were used.

3.3.2 Efforts to Increase the Buffer-Layer Thickness

As mentioned previously, it has been suggested in the literature[13] that hole traps at the substrate interface can account for g_m falloff with frequency, and the recommendation was made to eliminate this by going to a buffer layer several microns thick, perferably 5 microns at least. The one-micron-thick buffer layers presently used would not be considered thick enough by this article to avoid the problem, if it indeed exists.

Run EB 24 was made on MBE wafer #258, which had the regular thicknesses for the active and n^+ layers, but had a 2-micron-thick buffer layer instead of the usual one-micron thickness. Two runs were made on this thicker buffer layer wafer, but one of the runs would not pinch off and the other had a pinchoff voltage of around 10 V. It was concluded that either the buffer layer was conducting or the active layer was too thick.

A device run was made on MBE wafer #314, which used Si doping for the n layer and SnTe for the n^+ layer and employed a 5-micron-thick buffer layer. After completion of the fabrication, it was determined that the buffer layer was conducting, as evidenced by lack of pinchoff, high output conductance, and ohmic conduction between adjacent devices. The conclusion was reached that this same problem of a conducting buffer layer existed for run EB 24 with the 2-micron-thick buffer layer, indicating problems with compensation of the impurities in the buffer layer for growths thicker than one micron.

SIMS analysis of one-micron-thick buffer layers has shown no Cr outdiffusion from the substrate. Figures 17 and 18 show the SIMS profiles for Cr for MBE wafers #116 and #259. The Cr level falls from a level of $5 \times 10^{16} cm^{-3}$ in the substrate to below the $5 \times 10^{15} cm^{-3}$ background level within 500 Å of the substrate-buffer layer interface. Therefore, Cr is not responsible for compensation in the buffer layer. It appears that whatever is doing the compensating is only able to do so for the first micron or so of growth. Perhaps the ability to grow a good insulating layer depends upon how soon the growth occurs after the system was opened to air. Initially, there is plenty of C, O_2, and H_2O to provide compensation, but as time goes on, they may be pumped off and as runs are made, As covers the contaminants on the walls and traps them, and the top surfaces of the sources which are contaminated are used up. It seems probable that, if thicker buffer layers are not viable by MBE, part of the buffer layer can be grown by VPE.

An effort was made to determine at what point the MBE buffer layer became conducting, and it was proposed to do this by putting down ohmic contacts onto the buffer layer and measuring the resistance after etching off fixed amounts of the buffer layer. This profile of resistance vs. depth could then be used to determine roughly the conductivity profile of the buffer layer. Initially, two wafers (#385 and #384) having one-micron-thick buffer layers were tested, one being grown with the nonused source furnaces at their idle temperature and the other being grown with the nonused source furnaces off. Both wafers were about the same, with the ohmic contacts giving Schottky-barrier characteristics with ~20 V soft breakdowns. These same results were also obtained for 2- and 5-micron-thick buffer layers (#412 and #411), both grown with the nonused source furnaces at their idle temperatures. The only conclusion that could be reached was that when the first 5-micron-thick buffer layer was grown (MBE wafer #314), a new PBN crucible was used whose impurities were gettered out by the Ga source, while the above growths were done with fresh Ga in the already-gettered PBN crucible. The same ohmic

Fig. 17 Cr profile for MBE wafer #116.

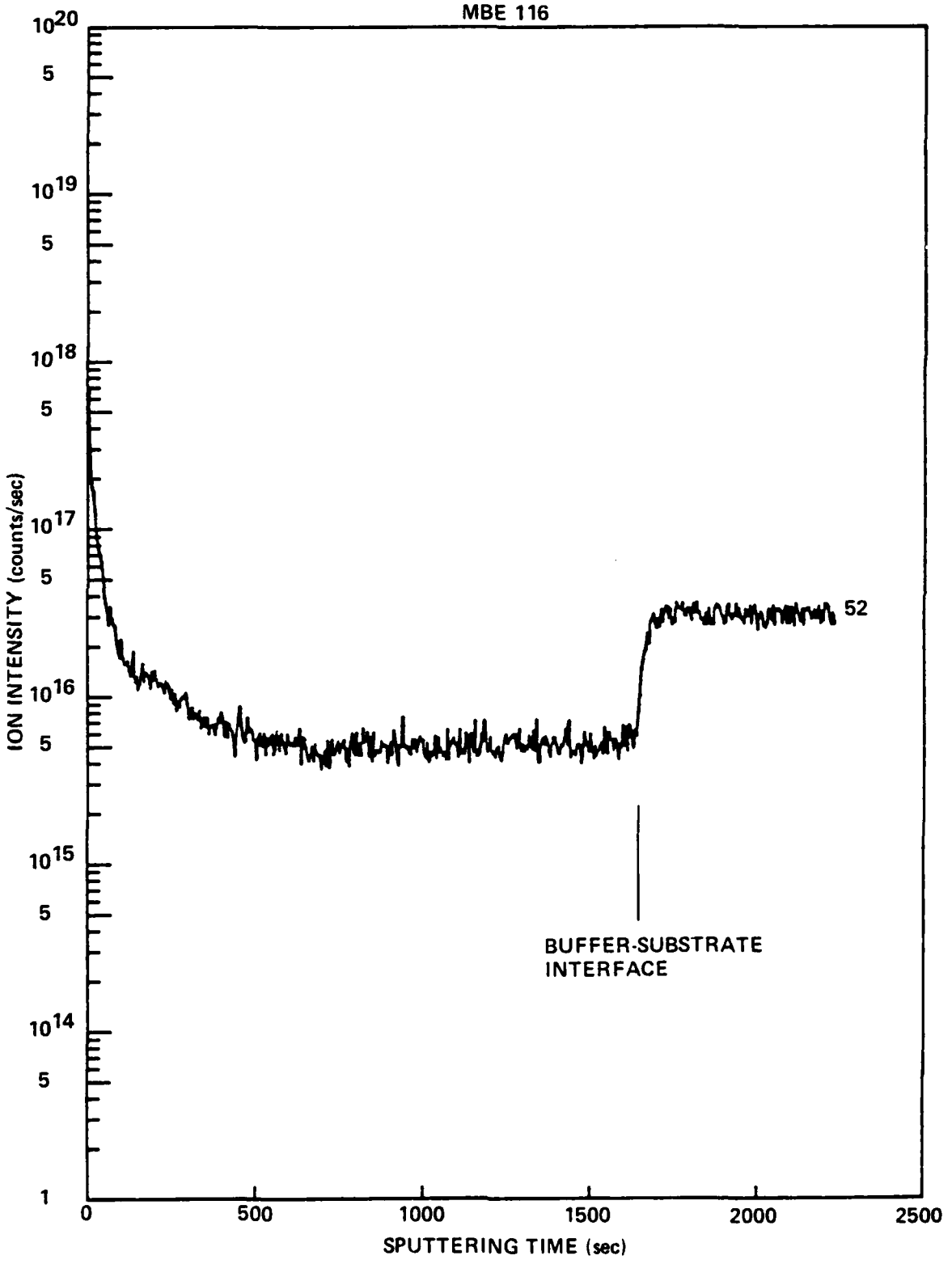
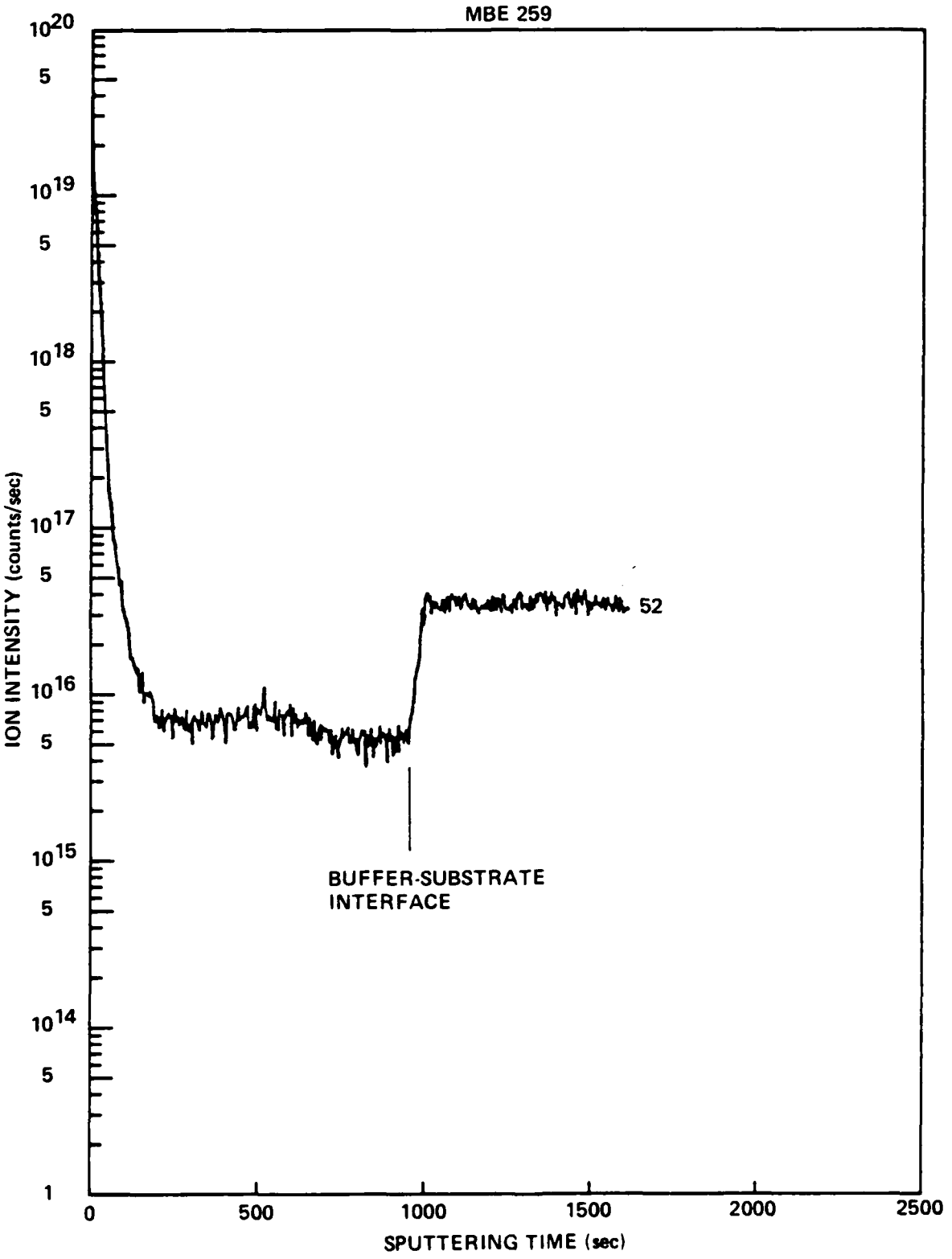


Fig. 18 Cr profile for MBE wafer #259.



contact experiments done on bare Cr-doped substrates without the buffer layer give higher breakdown voltages, typically 100 V or higher.

There is a possibility that, with the addition of n^+/n mesas under the ohmic contacts (i.e., the actual device structure) the conduction between adjacent contacts could become ohmic. Work on the buffer layer aspect of improving the noise figure was halted in favor of concentrating the effort toward the more important matter of reducing the gate resistance.

4. GATE METALLIZATION

Two basic problems concerning the gate metallization were addressed during this phase of the contract. The foremost problem is to reduce the gate resistance. Although the dual gate pad geometry accomplished a significant decrease in the gate resistance, Table III still shows that r_g is a significant portion of the input resistance r_{in}. As discussed in Annual Report No. 2 on this contract, besides the small gate length, the problem of gate resistance is further compounded by the typically triangular cross-section of the gates. It appears that the resist opening is gradually closed by metal buildup on the edge of the resist mask defining the gate electrode during the gate metal deposition. This problem appears to be basic to the fabrication of such small gate lengths.[14] Section 4.1 deals with the efforts made to alleviate this problem.

A second problem is that Au is not a reliable gate metallization; however, the evaluation of the devices so far has not demanded reliability. As described in more detail in Annual Report No. 1 of this contract, Al was found to give g_m compression and sputtered Pt was found to lengthen the gate -- hence the reason for using Au at the start of this contract. The only problem found with using Au is that it does not stick well to GaAs, so occasionally the gates will lift off or develop wiggles in them. The decision was made to try electron beam-evaporated Ti/Pt/Au which is used successfully as the gate metallization for power FETs; however, the first dummy run using this scheme showed g_m compression similar to that seen using Al. Section 4.2 describes the study made to determine the cause and solution to the problem of g_m compression.

4.1 Efforts to Increase Gate Cross-Sectional Profile

As discussed in the previous report, efforts to plate up the gate to increase its cross-sectional area were not found to be satisfactory

because invariably the gate length was found to increase significantly. Whereas a technique that lengthens the gate 0.1-0.2 microns may be acceptable for longer gate length devices, it is unacceptable for the purposes of this contract, since such increases in length are comparable to the intended length.

The closure of the resist opening as the gate metal is evaporated, which is responsible for the triangular high-resistance gates, is believed to be caused by the evaporated metal acting as a two-dimensional fluid and flowing sideways out over the edge of the resist.[15] In an effort to shrink the source size in order to reduce the thermal radiation from it and also collimate it better, a ceramic mask with a 1/4-inch opening was placed over the 1-cm diameter source boat. The same boat current was used as used without the mask, so the evaporant atoms were approximately as energetic as before, but the total evaporation rate was reduced by half. In spite of better collimation and lower thermal radiation, the problem of triangular gates remained virtually the same. This means that the energy of condensation of the atoms rather than thermal input from source radiation or source collimation is the crucial parameter.

An attempt was made to achieve the mushroom profile in the resist by using two different electron energies for the exposure; the first exposure at the regular 20-KeV value and the second at around 2-3 KeV to expose the resist to a shallower and wider depth of 0.5-0.7 micron.[16-18] However, in lowering the beam energy from 20 KeV to 2-3 KeV, the alignment was lost and the beam energy was too low to see enough detail to allow re-alignment. Even 5 KeV was found to be very difficult to align. Consequently, this particular approach was abandoned.

Probably the most promising technique investigated thus far is one employing two layers of resist separated by a thin Al layer to achieve a mushroom-type gate profile. Figure 19 shows a preliminary test of

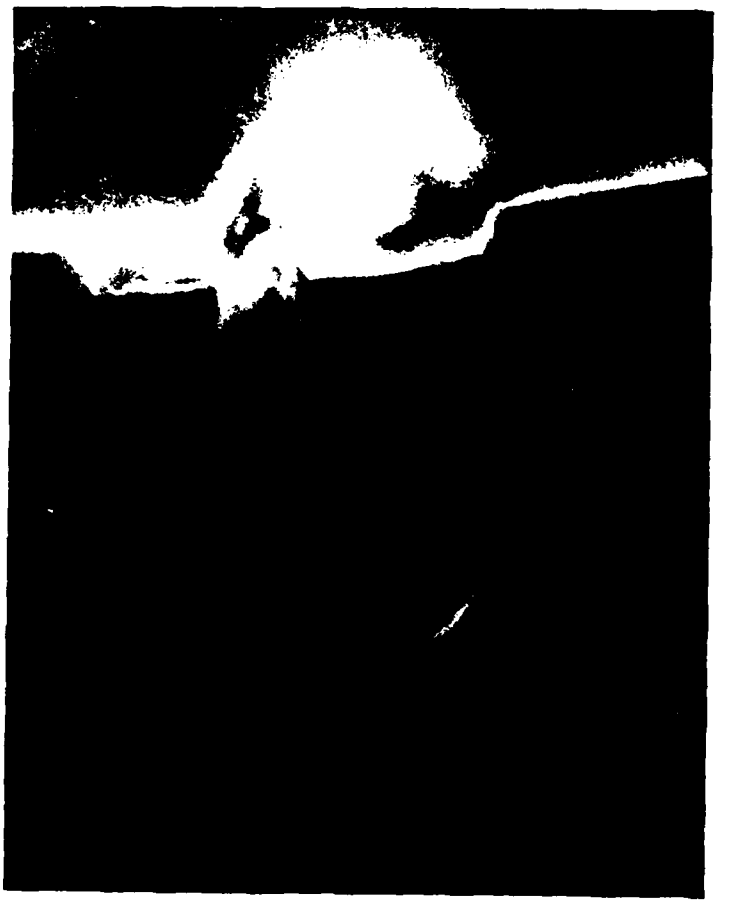


Fig. 19 Mushroom gate configuration.

this technology; however, no device runs have been made using it because of yield difficulties. The problem mainly lies in performing a sequence of operations without being able to monitor them visually.

Because of apparent problems in etching the Al between the resist layers (it seems that small spots will sometimes not etch), sputtered SiO_2 was tried between the resist layers. It was felt that the ease of etching the CVD SiO_2 used to define the n^+ channel through the small resist aperture should also apply to sputtered SiO_2. However, the SiO_2 deposition was too hot and wrinkled the PMMA, making it difficult to remove the resist from the surface.

Ti was tried next between the resist layers, but it appeared to be very difficult to etch using buffered HF. A plasma O_2 descum was tried, but this followed by the HF etch appeared to be as difficult a process, if not more so, than the Al interface initially used, so a return was made to Al. Figure 20 shows the mushroom gate as produced with an Al interface and Al as the gate metal (Al is used in place of Ti/Pt/Au to conserve Au while the mushroom gate process is being perfected). Allowing more overdevelopment of the top resist layer seems to be a key in improving the process. There seems to be increasing conviction among those involved that the process using the Al interface can be made a viable technique for reducing FET gate resistance in sub-half-micron-gated structures, by further refinement of the technology.

4.2 g_m Compression

Figure 22 shows what is meant by g_m compression, where maximum g_m occurs at some negative gate bias rather than at zero bias where it theoretically should. Although it is not certain that g_m compression adversely affects NF_m which usually occurs with negative bias on the gate anyway, it was felt that the problem deserved attention and effort towards understanding and eliminating it.

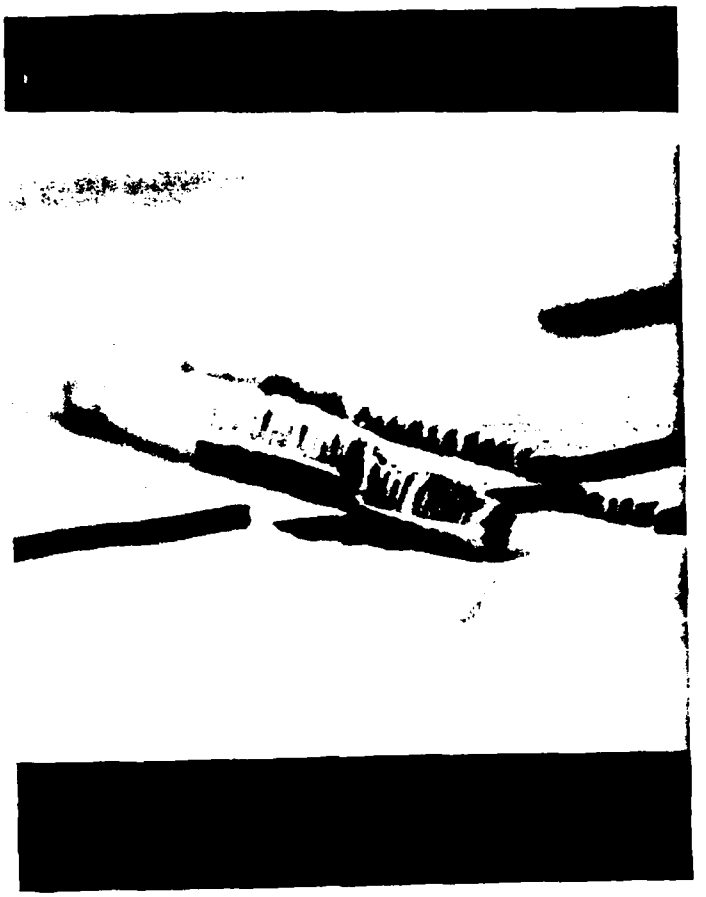


Fig. 20 Mushroom gate along channel.

To conserve Au, it was decided to use Al for the purposes of this study, and to do this work with a filament evaporation system which was more readily available for use. The rationale was that once the g_m compression problem was solved for Al, it would also be solved for Ti/Pt/Au. Power FETs are made in these laboratories using Ti/Pt/Au without exhibiting g_m compression, with the last cleaning step being either a 20-sec 10:1 H_2O:HF dip or with AZ developer, both followed by a DI water rinse. These cleaning steps were tried with submicron Al gates, but without success. Compression also resulted when plasma etching with Freon 12 (which etches GaAs) was used as the last step. To make sure organic residue was not responsible for the compression, a run was given an oxygen plasma descum, but the g_m compression persisted.

At this point, the entire body of results obtained so far was analyzed. Fact #1 is that g_m compression is almost always seen with Al and Ti, but not with Au. Fact #2 is that even with the same cleaning steps, the power FETs never show compression while the sub-half-micron FETs of this contract do, and the only apparent differences are the size of the resist opening and the resist itself. Fact #1 suggests the possibility that an oxide is involved, because of the high reactivity of Al and Ti with O_2, while Au is virtually inert. Indeed, the only time g_m compression was seen for the power FETs was when the evaporation system was exposed to air after a small amount of Ti was evaporated and before the remaining Ti/Pt/Au was evaporated. This clearly demonstrates the ability of Ti to getter either O_2 or H_2O from the ambient air. Both Al and Ti can reduce the most stable gallium and arsenic oxides, as indicated by the following listing of the heats of formation of the most stable oxides.[19]

Ga_2O_3	-86.0	kilocalories per gram-atom of oxygen
As_2O_3	-52.3	"
Al_2O_3	-133.5	"
TiO	-124.0	"

It may be that the surface states associated with Al_2O_3 and TiO are responsible for g_m compression, while the surface states associated with gallium and arsenic oxides do not give compression. Another possibility is residual water vapor in the evaporation system.[20] While the system used for Ti/Pt/Au pumps down to around 10^{-8} torr, the system used for Al only pumps down to around 10^{-6} torr. At 10^{-6} torr, 100 Å/min. of H_2O impinges on the surface, while at 10^{-8} torr it is only 1 Å/min. Both Al and Ti are known to getter H_2O and incorporate it in evaporated films.

Concerning fact #2, one major difference is aperture size. H_2O will outgas from a recess in the resist at a rate proportional to the aperture size and independent of the depth. Thus a 0.2-μm opening would take 5 times longer than a 1-μm opening (which is the resist opening size for the power FETs) to get rid of the H_2O. Also, the resists have many similarities to plastics, which are notorious for outgassing H_2O. Possibly, PMMA is worse than AZ 1350 J (which is used for the power FETs) in this regard. Figure 21 shows a scaled comparison between the resist apertures for the power FETs and the sub-half-micron FETs. The overhang may be even more significant than the aperture size. Ga is quite reactive with oxygen, so a prebake (even in vacuum) to drive off any water may form gallium oxide, which in turn will be reduced by Ti or Al.

With the above facts in mind, a run was made in the Ti/Pt/Au system to utilize the higher vacuum, and the improvement was significant. As with the runs done in the Al system, a citric acid etch was used (which was not used for the very first run using Ti/Pt/Au). It was found that a 10:1 HF dip after the citric acid etch would attack the SiO_2-resist interface and leave pockets from which water could possibly outgas, resulting in more g_m compression; consequently, the HF dip after the citric acid etch was eliminated. Even with all these modifications, g_m compression was still seen about half the time, although so slight that it was not apparent at first glance. Figure 22 shows the g_m compression

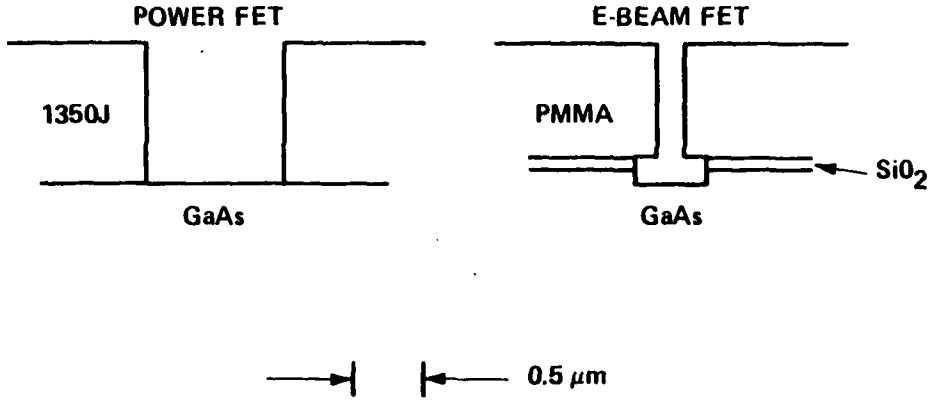


Fig. 21 Aperture comparison between power & electron-beam-exposed FETs.

with Ti/Pt/Au at the start of this study, and Fig. 23 shows the "worst case" degree of g_m compression as it occurs at the present time. In Fig. 23, the voltage steps are smaller to make the compression more obvious.

It has been computed that it should take only 600 μsec to pump out a 0.2-μm aperture filled with 2500 Å of water, so residual water would not appear to be the problem. On the other hand, the resist may be likened to neoprene in terms of its degassing rate (5×10^{-6} torr-ℓ/sec/cm^2).[21] For a 0.2-μm aperture, the water contamination rate would thus be 4300 Å/min., while for a one-micron aperture, it would only be 170 Å/min.! This could explain why the small gate length devices seem to have more of a g_m compression problem than the wider one-micron-long power FET devices when the metal deposition is done in the same system. In addition, it may be that the PMMA has a higher degassing rate than 1350 J (i.e., it may have a greater tendency to act like Swiss cheese in terms of its ability to store water and subsequently outgas it). Perhaps an initially rapid gate metallization will minimize sufficiently the water contamination.

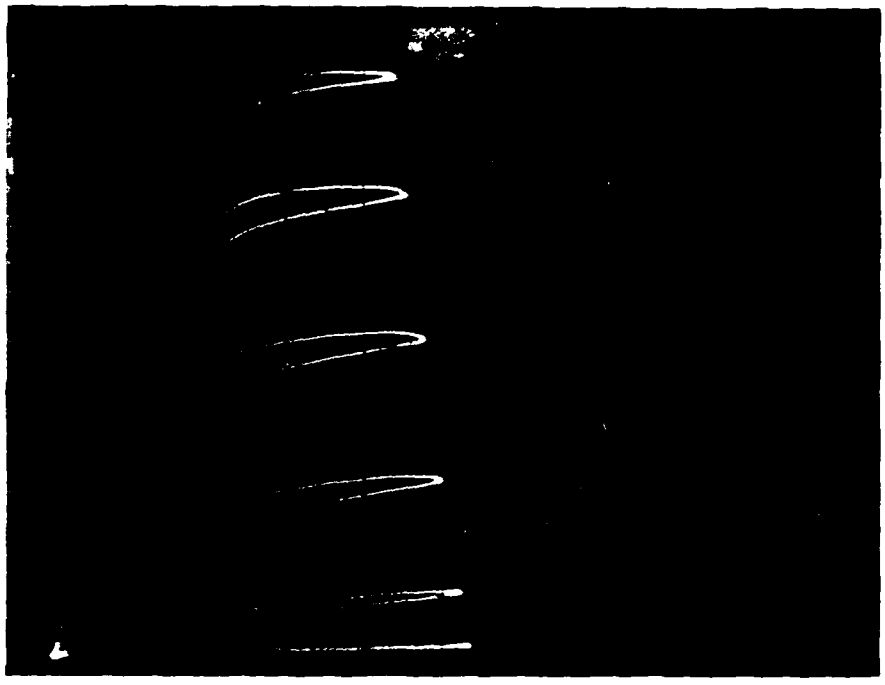


Fig. 22 Initial g_m compression for Ti/Pt/Au.
(5 mA/div., 0.5 V/div., -0.5 V/step)

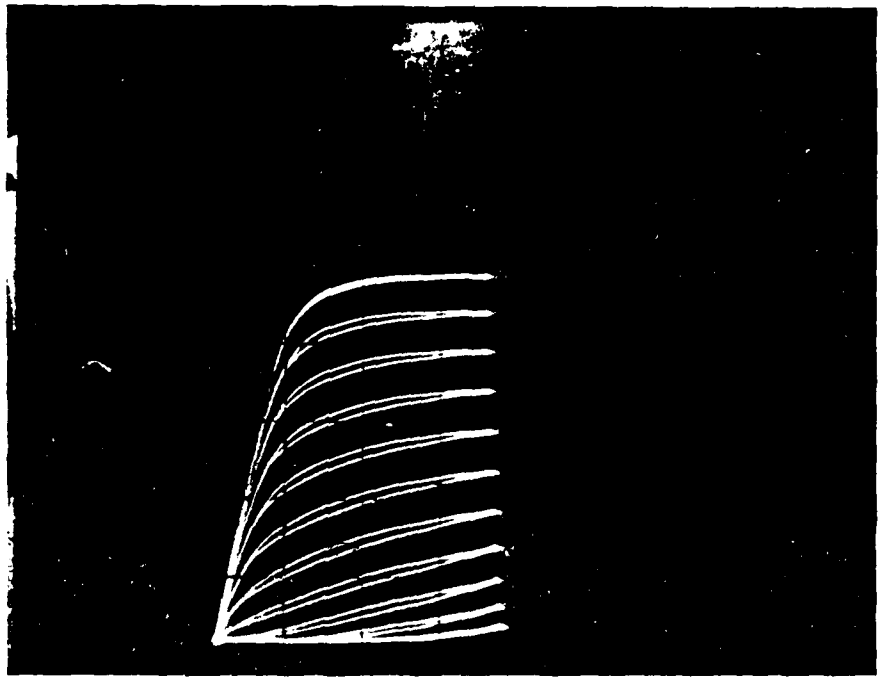


Fig. 23 Final g_m compression for Ti/Pt/Au.
(10 mA/div., 1 V/div., -0.2 V/step)

5. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

5.1 Accomplishments and Problems Solved

During this period, the rf performance at 8 GHz was improved from a minimum noise figure of 1.5 dB with an associated gain of 15 dB to a minimum noise figure of 1.2 dB with an associated gain of 13 dB. This improvement was primarily accomplished by going from one to two gate pads.

It was also shown that the term $g_m L_s/C_{gs}$ should not be included in the Fukui noise-figure formula. This reduces the computed value of the minimum noise figure, but an increase of the value of k in the Fukui equation from 0.033 to a revised value of 0.04 brings the computed noise figure back to about where it was. A derivation of the minimum noise figure including the effects of L_s shows that L_s can increase the minimum noise figure significantly at higher frequencies.

5.2 Continuing Problems

In spite of the dual gate pad geometry, high values of gate resistance r_g continue to dominate the minimum noise figure due to premature closure of the gate opening by sideways metal flow during deposition. A technique to increase the gate metallization cross-section has not yet been perfected.

R_s continues to be higher than expected. Assuming bulk mobilities and a contact resistivity of 10^6ohm-cm^2, the computed source resistance should be 2 ohms instead of the 6 ohms measured. One of the reasons why R_s has not been explored in more detail to date is because SEM observation of the channel region is needed to obtain the various spacings, and this invariably degrades the device.

5.3 New Problems Uncovered

A switch was made from Au to a more reliable gate metallization, Ti/Pt/Au, only to encounter g_m compression once again as with Al at the start of this contract. After an extensive series of tests, the conclusion was reached that either residual water takes too long to pump out through the small gate opening in the resist, or that the resist continually outgasses water. If the latter is the case, an initial fast deposition of the gate metallization might help alleviate the problem. Typically the amount of g_m compression still remaining after taking the necessary precautions to minimize water contamination is so slight that device performance would not be expected to be affected significantly anyway.

g_m falloff with frequency has been observed, but its cause and its effect on the rf performance has not been determined. An effort to increase the buffer layer thickness from one to five microns was thwarted by the MBE buffer layers becoming conducting beyond a thickness of one micron.

Because of the degradation that occurs to the device drain characteristic when observed with the 20-kV SEM electron beam, it may be that some material degradation in the channel also occurs when the gate region is exposed with a 20-kV beam.

5.4 Recommendations for Future Work

For future work, the areas needing either improvment --or at least investigation -- in order to improve the performance in Table I, are the following:

(1) reduction in gate resistance, r_g, by increasing the gate cross-sectional area,

(2) reduction in source resistance, R_s,

(3) elimination (or at least investigation) of the observed phenomenon of transconductance reduction in going from dc to the GHz range,

(4) reduction of source inductance, L_s,

(5) investigation of possible degradation of the gate region in the process of electron-beam exposure of the gate resist, and

(6) in addition, there is a need to develop a reliable gate in place of the evaporated Au gate now used.

Problems (1) and (2) definitely are hurting the device performance; (4) is less important at 8 GHz but will become important in the 20 to 40 GHz region, while (3) and (5) are only potential problems at present. During the current phase of the contract, most of the effort was centered on items (1) and (3) (i.e., development of a mushroom gate structure and a 5-micron-thick buffer layer) because they seemed to promise the highest payoffs. As has already been discussed, problems have arisen in carrying out these tasks. Minimizing source inductance (Task 4) is also an important task. Figure 4 shows a geometry that might be used to reduce L_s through the use of plated-through source contacts from the back side. Finally, in investigating possible trapping effects under Task (3), it may be useful to fabricate devices on ion-implanted or VPE material for comparison purposes. Once r_g and R_s have been sufficiently reduced to allow study of the properties of the intrinsic device, the ultimate goals, as listed in the Introduction, can be addressed.

5.5 Projected Performance Goals

Using the geometry of Fig, 6, the gate resistance r_g for the most recent device run (EB 26) has ranged from 2.2 to 5.8 ohms (with L varying

from 0.16 to 0.4 microns). Consequently, it would seem reasonable to assume that r_g should be reduced to less than 1 ohm with the mushroom structure of Fig. 19. For reasons of computation, then, r_g will be set at 1 ohm. Assuming bulk mobilities and a contact resistivity of 10^6 ohm-cm^2, the computed source resistance should be 2 ohms instead of the 6 ohms measured. Assuming that an investigation will rectify this, R_s values should reach 2 ohms.

Using the above goal values along with L = 0.2 micron and a value of 5 ohms for $g_m L_s / C_{gs}$ (typical for run EB 26) yields the table below using Eq. (9).

TABLE V

Projected NF_m Results

Frequency	Projected NF_m	Projected NF_m with $L_s = 0$
8 GHz	.773 dB	
24 GHz	2.69 dB	2.04 dB

This table shows the importance of reducing L_s for operation at the higher frequencies. Hence some development such as the geometry of Fig. 4 will be needed to bring about this reduction.

APPENDIX A: CAN REACTANCES SIMULATE g_m FALLOFF WITH FREQUENCY?

The question is, can g_{21} exhibit the form shown in Fig. A.1 with L's and C's?

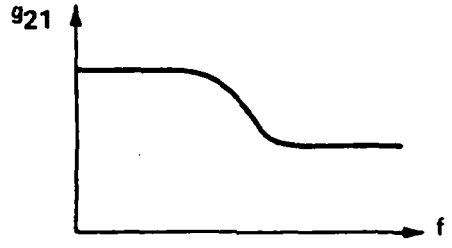


Fig. A.1

For the simple model shown in Fig. A.2,

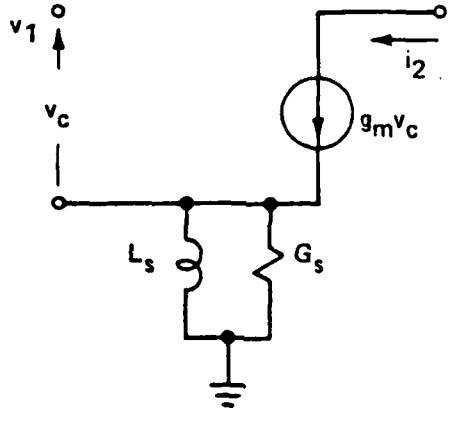


Fig. A.2

then at dc, $g_{21} = g_m$, while at $\omega = \infty$, $g_{21} = g_m/(1 + g_m R_s)$.

Analytically,

$$g_{21} = g_m \left(\frac{1 + \omega^2 L_s^2 G_s (g_m + G_s)}{1 + \omega^2 L_s^2 (g_m + G_s)^2} \right)$$

which gives the dependence shown in Fig. A.1.

The simple model in Fig. A.3 also exhibits the same dependence.

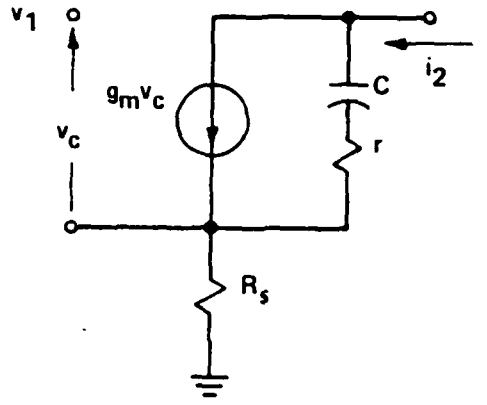


Fig. A.3

At dc, r doesn't enter g_{21}, and at $\omega = \infty$, it shunts g_m. Analytically,

$$g_{21} = g_m \left(\frac{1 + g_m R_s + \omega^2 r C^2 [r(1 + g_m R_s) + R_s]}{(1 + g_m R_s)^2 + \omega^2 C^2 [r(1 + g_m R_s) + R_s]^2} \right).$$

At $\omega = 0$, $g_{21} = g_m/(1 + g_m R_s)$, while at $\omega = \infty$,

$$g_{21} = \left(\frac{g_m}{1 + g_m R_s} \right) \left(\frac{r}{r + R_s/(1 + g_m R_s)} \right)$$

where since the last factor is less than unity, g_{21} falls off with frequency.

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