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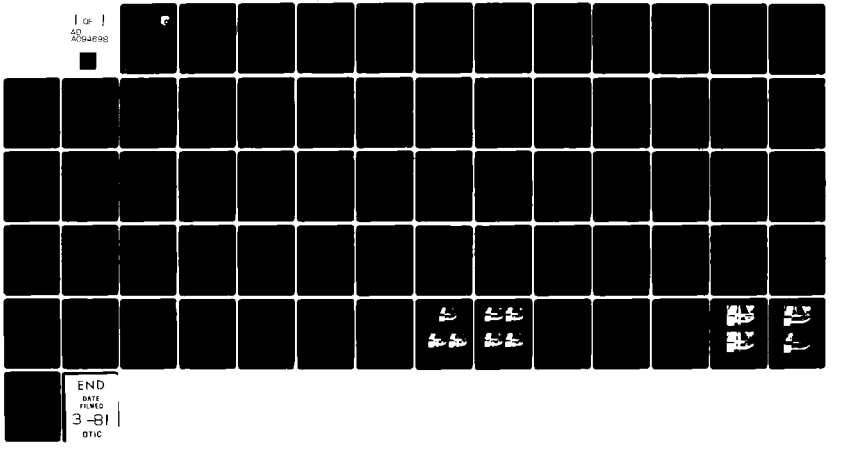

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VIDEO BANDWIDTH COMPRESSION SYSTEM

David Ludington

General Electric Company
Aircraft Equipment Division
Utica, New York 13503

August 1980

TECHNICAL REPORT AFWAL-TR-80-1113

Final Report for Period 15 September 1978 to 15 November 1979

Approved for public release; distribution unlimited.

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This technical report has been reviewed and is approved for publication.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of this program was the development of a Video Bandwidth Compression brassboard model for use by the Air Force Avionics Laboratory, Wright-Patterson Air Force Base, in evaluation of bandwidth compression techniques for use in tactical weapons and to aid in the selection of particular operational modes to be implemented in an advanced flyable model.

The bandwidth compression system is partitioned into two major

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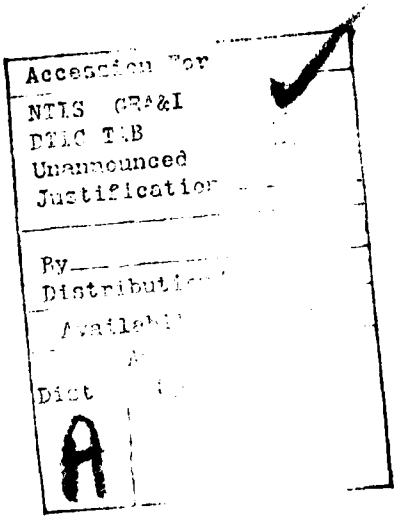
20. ABSTRACT (Cont.)

divisions: the encoder, which processes the input video with a compression algorithm and transmits the most significant information; and the decoder where the compressed data is reconstructed into a video image for display.

The brassboard model was designed using custom analog CCDs for the transform function and standard TTL circuits for the DPCM, memory and timing functions. The 32 point serial-to-parallel converter (used in the encoder transform section) was implemented using existing 8-point devices connected in a parallel/serial configuration. This required the addition of inverting amplifiers to maintain the correct signal phase. Because of pin limitations, the 32 x 32 matrix multiplier (used in both the encoder and decoder transform sections) was partitioned into two chips each with 32 inputs and 16 of the coefficient outputs. The 512 x 480 x 2 bit frame store memory was implemented using 1024 x 8 bit static bipolar devices with access times of 120 nsec.

The system was packaged using 9-1/2 inch x 9-3/4 inch cambion type wire wrap boards and housed in standard 19 inch rack-mounted enclosures. The encoder and decoder are housed in separate enclosures, each containing 11 wire wrap boards and power supplies.

System test results show that the variations in image resolution as a function of compression level correspond to results obtained through computer simulation. However, in addition to the gradual loss of resolution due to increased bandwidth compression, fixed pattern noise (10 to 12 percent of full scale) is evident in the output image in the form of vertical lines. Recommendations for reduction of this noise include changing the hybrid coding block size from 32 to 16 samples and incorporating the inverse scaling function, located between the inverse DPCM and inverse transform, on the decoder matrix multiplier chips.



PREFACE

This report summarizes the efforts of the General Electric Company on the development of a Video Bandwidth Compression brassboard model for the Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio. The work was done by the General Electric Company, Aerospace Electronic Systems Department, Utica, New York on Contract F33615-78-C-1401.

The work was accomplished during the period 15 September 1978 to 15 November 1979.

This report is submitted in accordance with the requirements of the Contract Line Item 0002, DD1423 Sequence No. 8.

The basic purpose of the effort was to develop a brassboard model for use in the evaluation of bandwidth compression techniques for use in tactical weapons and to aid in the selection of particular operational modes to be implemented in an advance flyable model.

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I. INTRODUCTION

This is the final technical report on the Video Bandwidth Compression System program being conducted by the General Electric Company, Aerospace Electronic Systems Department (GE/AESD), Utica, New York, for the Air Force Avionics Laboratory on Contract F33615-78-C-1401. This report summarizes the efforts completed during the period 15 September 1978 through 15 November 1979.

The overall objective of this effort is to develop a versatile laboratory breadboard model of a real-time bandwidth compression system capable of being miniaturized consistent with the size, power and cost goals of video controlled electro-optically guided glide bombs, such as the GBU-15 Modular Guided Glide Bomb.

This report will present a brief overall description of the Video Bandwidth Compression System followed by a detailed description of the design of each of the system modules. Test results are summarized and recommendations relative to future program efforts are also discussed.

II. SYSTEM DESCRIPTION

1. Basic System

The Video Bandwidth Compression System consists of two rack mounted boxes, the encoder and the decoder.

The encoder box accepts a standard NTSC compatible monochrome composite video signal and outputs data, sync, and clock signals for use by a modem.

The decoder box accepts data, sync, and clock signals from a modem and outputs a standard NTSC compatible monochrome composite video signal.

a. Equipment Features

The standard NTSC compatible monochrome picture consists of 525 lines at a 30 Hz rate (Figure 1). These 525 lines make a single frame that is divided into two fields of 241 one-half active video lines each. There are two vertical retrace/blanking intervals of 21 lines each. The net result is a 2:1 interlace of the two fields to form the single frame. Approximately 16 percent of the horizontal line time is devoted to retrace/blanking.

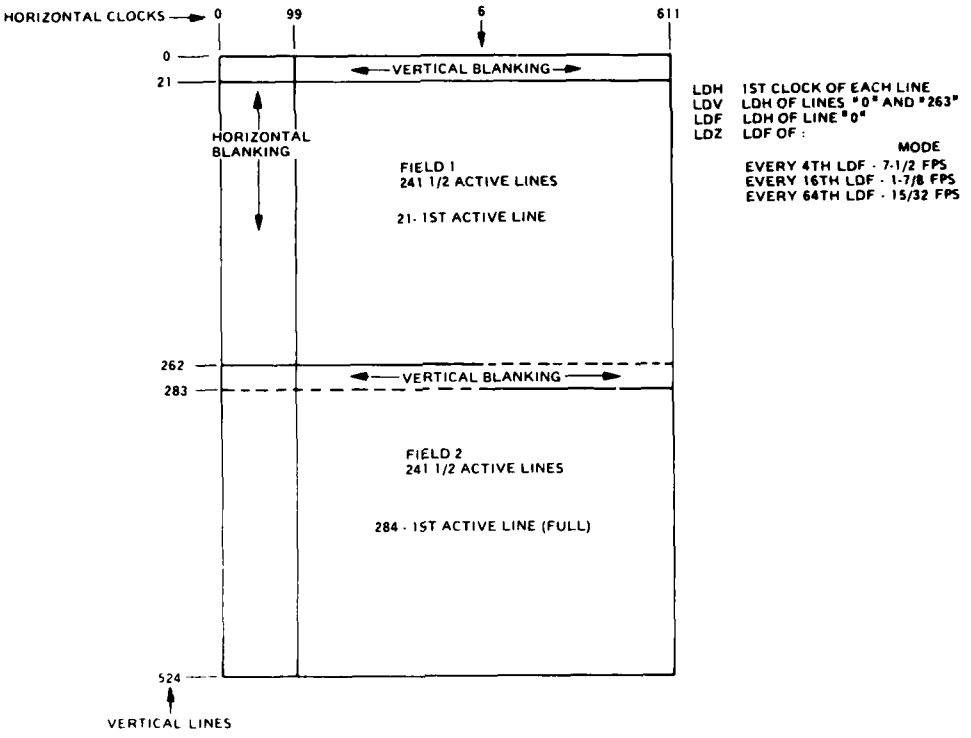


Figure 1. Picture Sync

In the vertical direction the Video Bandwidth Compression System uses 240 of the 241 one-half active lines in each field for the 480 line resolution case. This results in vertical blanking periods of 22 lines and 23 lines for Field 1 and Field 2 respectively. The 2:1 interlace is thus preserved. The 240 line resolution case consists of Field 1 only with the same data being reused for Field 2 in the monitor. The 128 line resolution case uses every other line of Field 1 with the data being interpolated for the missing lines in the monitor which again, has Field 1 data repeated for Field 2.

The Video Bandwidth Compression System divides the horizontal line into 612 intervals with a 9.639 MHz clock. The first 100 clocks are horizontal blanking time and the remaining 512 clocks are active video time. This gives a maximum resolution of 512 pixels (picture elements) in a horizontal line. The 256 pixel and 128 pixel per line resolutions are formed by dividing the clock by 2 and 4 respectively during the active video time.

The pixels along a line are taken in 32 pixel segments and "cosine transformed" into 32 cosine coefficients. The cosine coefficients are compared, coefficient by coefficient, segment by segment, with their corresponding cumulative total from the previous lines to implement a differential pulse code modulation (DPCM) loop.

The "bandwidth compression" in the system is actually performed in a "bit packer" that follows the DPCM loop. In the bit packer, individual coefficients are assigned numbers of significant bits from 5 to 0 to make up different average "bits-per-pixel" for the entire picture. These significant bit assignments per coefficient for all 60 modes are stored in a single, easily replaceable, 1K x 8 UV-EPROM per unit.

Since all bandwidth compression is done within a single TV frame, there is no frame to frame, or field to field memory to cause temporal artifacts.

The 60 modes of operation consist of all possible combinations of:

FRAME RATE	-	15/32, 1-7/8, 7-1/2, 15
RESOLUTION	-	512 (x 480), 256 (x 240), 128 (x 120)
BITS/PIXEL	-	0.5, 0.75, 1.0, 1.5, 2.0

2. Encoder Unit Equipment Specification

a. Inputs

The unit accepts and will synchronize to the standard NTSC compatible monochrome composite video signal.

The modem data master clock, 4.8 MHz, can be supplied externally or the unit can use an internally generated modem clock.

The unit operates off standard 115 volt ac, single phase, 60 Hz power. The power supplies operate from 47 Hz to 440 Hz; however, the cooling fans are 60 Hz only.

b. Control Section

The control selection is by the front panel switches. These are:

FRAME RATE	-	15/32, 1-7/8, 7-1/2, 15
RESOLUTION (pixels x lines)	-	512 (x 480), 256 (x 240), 128 (x 120)
BITS/PIXEL	-	0.5, 0.75, 1.0, 1.5, 2.0
MODEM CLOCK	-	50, 75, 100, 150, 200, 300, 600, 1200, 2400, 4800
SOURCE SELECT	-	INTERNAL/EXTERNAL
CHANGE MODE	-	Push to implement mode change

The system has 60 possible modes. The mode being executed is displayed on the front panel with LEDs. A mode change to the switch settings is initiated by the "mode change" push button. The actual mode change will occur at the next frame zero.

c. Bits-Per-Coefficient Assignments

The Bits-Per-Coefficient Assignments for all five possible "bits-per-pixel" selections are stored in a single 1K x 8 UV-EPROM (ultraviolet erasable programmable read-only memory). This UV-EPROM is easy to change. The assignments it contains are "booted" into an operating RAM (random access memory) during each frame zero, Field 1, vertical blanking interval.

d. Digital Outputs (TTL, 50 ohm, BNC)

The encoder unit has three basic outputs:

(1) Serial encoded compressed video data at the modem clock rate. This output is available on two separate BNC's to allow for mode stripping in the decoder unit, independent of the data path. Jamming can then be added to the data path without affecting the mode control.

(2) Internally generated modem data clock. This is available to sync the decoder unit directly, or a modem if desired.

(3) The synchronization signal from the encoder unit tells the decoder unit when the next mode control word is present for decoding and a new frame of data is starting.

e. Output Data Rate

The serial encoded compressed video data will be "bit-stuffed" into the lowest bits-per-second rate that will ac-

cept it. This will minimize the number of zeros transmitted on the digital data link between frames of data and result in the lowest data rate possible for a given mode.

f. Mechanical

The unit is contained in a standard 19-inch-wide rack mountable chassis, 12-1/4 inches high by 19 inches deep. The unit is equipped with tilting slides for easy accessibility.

Power and signal inputs and outputs are located on the rear panel. The front panel has power and mode switches and indicators, along with several test BNC's for sync and signals.

3. Encoder Overall Block Diagram (Figure 2)

a. Input V eo Board

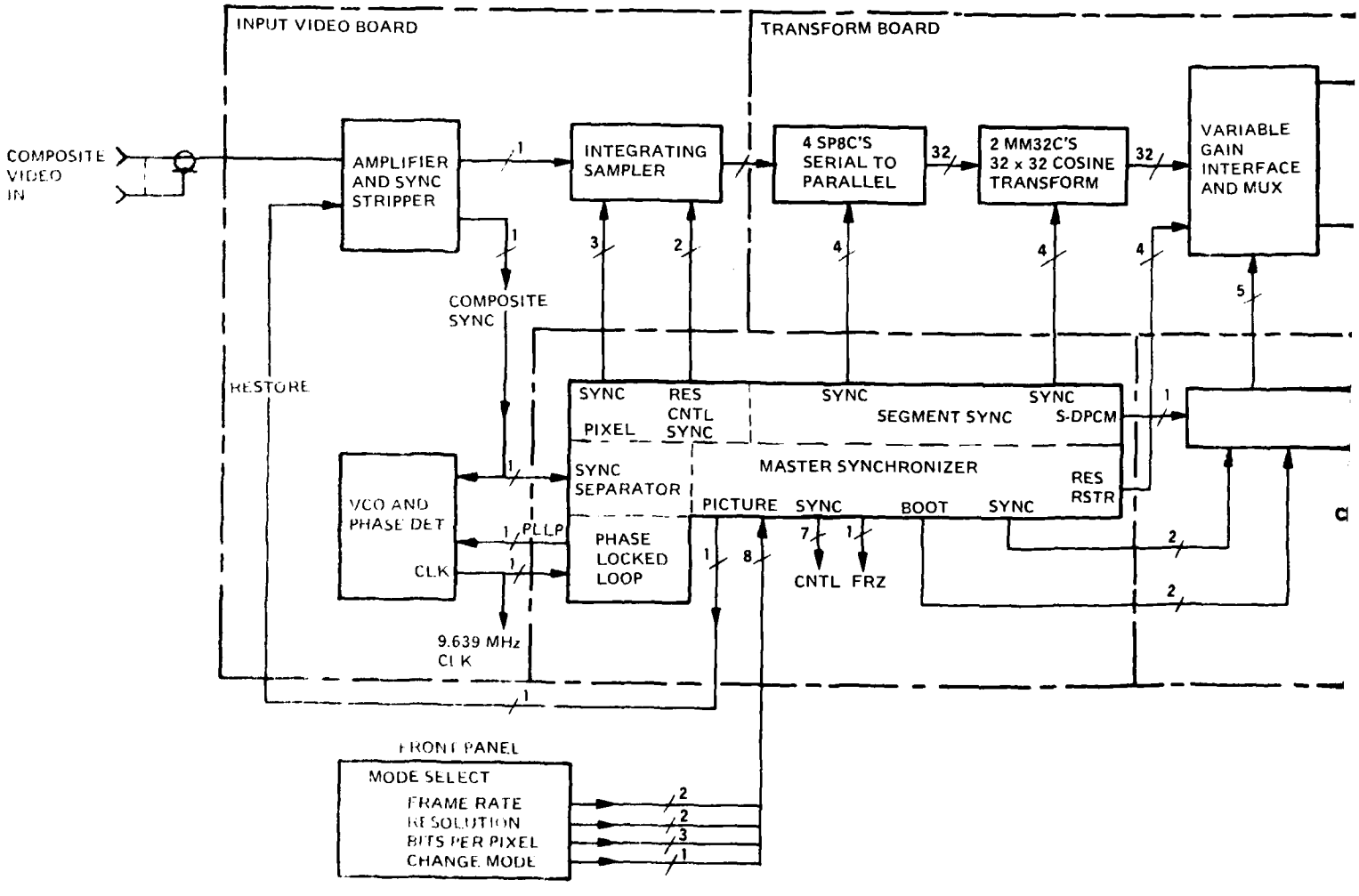
In the Input Video Board, the composite input video signal is amplified, dc restored, and is sent to an integrating sampler. The composite sync is stripped off the amplified video and sent to the phase-locked-loop phase detector and the master synchronizer board sync separator.

The integrating sampler performs a true power integration over each pixel, regardless of its size. In the 512 along-the-line pixel mode, the integrating sampler integrates 512 times; in the 256 mode, it integrates for twice as long, giving 256 outputs, and in the 128 mode, it integrates four times as long, giving 128 outputs of video voltage to the serial-to-parallel converter that feeds the 32 x 32 cosine transform matrix multiplier.

b. Master Synchronizer Board

The composite sync is separated into horizontal sync, vertical sync, and Field 1 sync pulses that are sent to a phase locked loop. In the phase locked loop, a 9.639 MHz VCO clock is phase locked to the horizontal sync pulses. A horizontally derived dc restore pulse is returned to the sync stripper. A vertical line counter in the master synchronizer is locked to the Field 1 pulse to provide all vertical line timing for the remainder of the system.

The master synchronizer contains essentially three sections. The first section is a vertical line synchronizer which provides the picture sync. The picture sync does the RAM booting, the vertical blanking, and the frame counting functions. The second part of the master synchronizer is the pixel sync. The pixel sync provides synchronization for the integrating sampler and the start of the segment sync. The segment sync por-


INPUT VIDEO BOARD
TRANSFORM BOARD
COMPOSITE VIDEO IN
AMPLIFIER AND SYNC STRIPPER
INTEGRATING SAMPLER
4 SP8C'S SERIAL TO PARALLEL
2 MM32C'S 32 x 32 COSINE TRANSFORM
VARIABLE GAIN INTERFACE AND MUX
COMPOSITE SYNC
RESTORE
SYNC
RES CNTL SYNC
PIXEL
SYNC
SEGMENT SYNC
SYNC
S-DPCM
MASTER SYNCHRONIZER
SYNC SEPARATOR
RES RSTR
PICTURE
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BOOT
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BITS PER PIXEL
CHANGE MODE

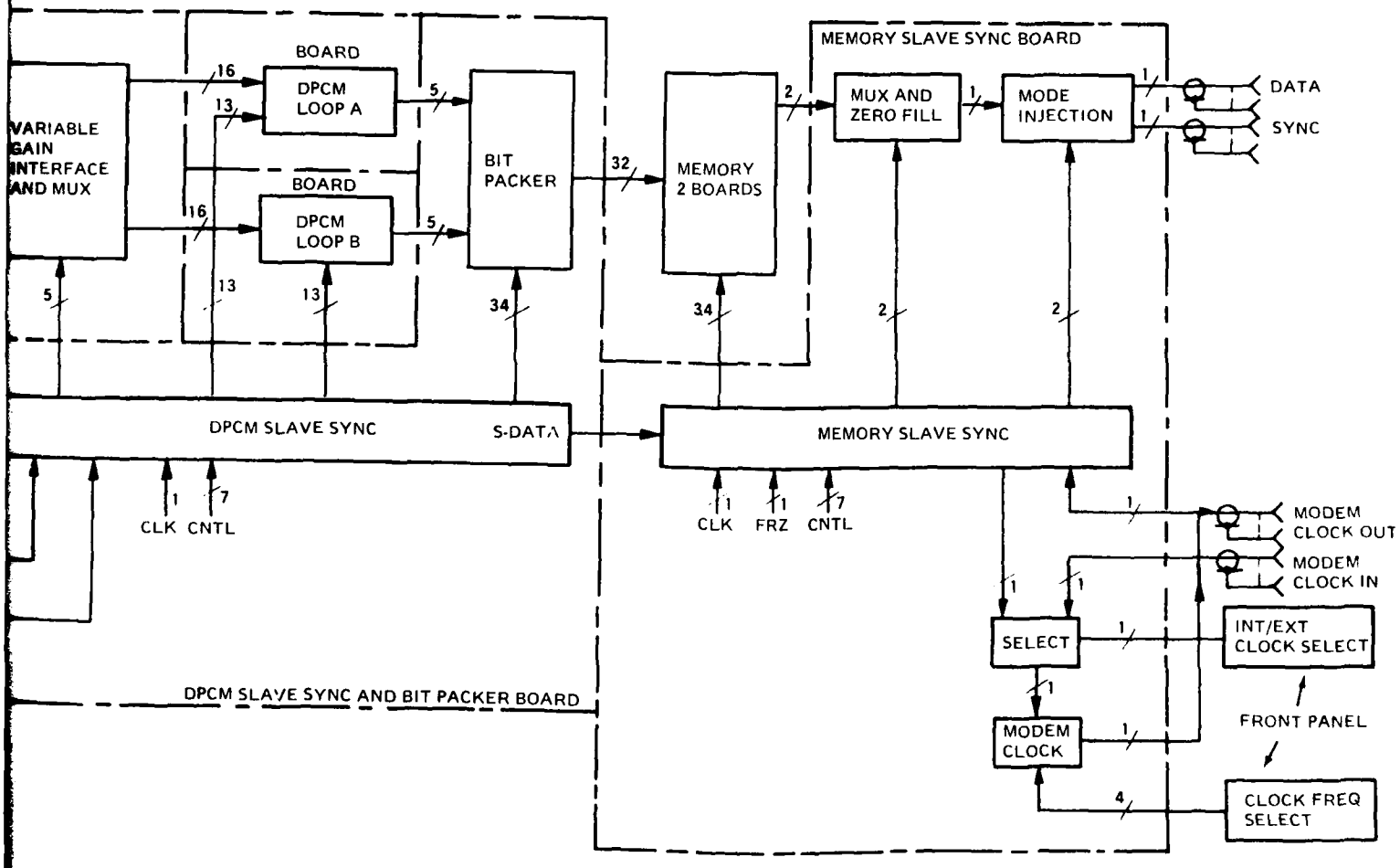


Figure 2. Encoder Overall Block Diagram

tion of the master synchronizer provides all the sync pulses necessary for the serial-to-parallel conversion and the 32 x 32 cosine transform matrix multipler. Both of these analog devices operate in real video time. The remaining outputs of the master synchronizer are the control and start pulses for the variable gain interface/MUX and the DPCM slave synchronizer.

c. Transform Board

The Transform Board contains the serial-to-parallel converter chips that convert 32 serial analog samples into 32 parallel analog samples each segment time. These 32 parallel analog samples are transformed into 32 cosine coefficients in the 32 x 32 cosine transform matrix multiplier.

The transform coefficients are then weighted by variable gains. The outputs of the variable gain interface/MUX are two video lines that each contain, in sequence, 16 of the coefficient outputs of the 32 x 32 cosine transform.

d. Differential Pulse Code Modulation Loops (DPCM)

Each of the DPCM loops takes one of the video lines from the transform board. The DPCM loops contain the averaged values of a given coefficient stored from the previous lines. These previous average values are subtracted from the new value and the resulting difference is then converted from analog to digital form. The 8-bit A/D output is transformed to a 5-bit nonlinear quantized word, and presented to the bit packer. DPCM loop A operates on the 16 most significant coefficients, while DPCM loop B operates on the 16 least significant coefficients.

e. DPCM Slave Sync and Bit Packer

The actual bandwidth compression function is performed in the bit packer. In this unit, pairs of 5-bit words are presented simultaneously from the two DPCM loops to the bit packer. The bit packer, taking them in sequence, determines how many bits of each word (from 5 to 0) are to be saved, and packs the bits into 32-bit words which are presented to the main memory for storage.

The DPCM slave synchronizer provides all the control signals for the two DPCM loops. It also contains the information to operate the bit packer, and control the number of bits per coefficient that are packed into 32-bit words. Another output of the DPCM slave synchronizer is the control signal to the memory slave synchronizer telling the memory when it has a 32-bit word to place in storage.

The DPCM loops operate at a different clock frequency from the rest of the system because they must accomplish their job in less than a full segment time. This results from the matrix multiplier output having to settle before the DPCM loop can start operating on the coefficients.

f. Memory Boards

The two Memory Boards contain sufficient storage to hold all the 32-bit words required for the greatest resolution and highest number of bits per pixel for a single frame. This storage is organized by the memory synchronizer to form a swinging door buffer that divides the memory being used in half to allow the first half to start outputting while the second half is still being filled.

g. Memory Slave Synchronizer Board

The Memory Slave Synchronizer Board keeps track of the number of 32-bit words that have been processed. When the memory is half full, this board switches banks so that the first bank, which is not full and represents half of the video data, can start being read out as serial data. The serial data is generated with a mode control word on its leading edge, so that the decoder will know what mode follows in terms of resolution, frame rate, and bits per pixel. When the memory slave synchronizer has finished outputting both halves of the memory, it then fills the remaining time with zeros until the first half of the memory is loaded with the next picture to be outputted serially.

A modem clock generator is included in the encoder unit to transmit the serial data. This modem clock has a large number of possible frequency selections. If the modem master clock is to be supplied externally, this is a simple switch selection.

h. Front Panel

The Front Panel of this unit contains the mode selection controls for frame rate, resolution, and bits per pixel. A pushbutton implements a change in mode at the time of the next frame cycle, i.e., when the present mode has completed its current cycle. LED indicators indicate the present mode being processed.

4. Decoder Unit Equipment Specification

a. Inputs

The signal inputs to the decoder unit are the three outputs of the encoder unit. These are:

(1) The serial encoded compressed video data at the modem clock rates. This signal is inputted on two separate lines to allow for mode stripping independent of the data path. Jamming can then be added to the data path without affecting the mode control. This feature will be front panel switch selectable.

(2) The unit accepts a modem clock to clock the data in.

(3) The synchronization signal from the encoder unit tells the decoder unit when the next mode control word is present for decoding and a new frame of data is starting.

The unit operates off standard 115 volt ac, 60 Hz, single phase power. The power supplies operate from 47 Hz to 440 Hz; however, the cooling fans are 60 Hz only.

b. Output

The unit puts out the standard NTSC compatible monochrome composite video signal.

c. Mechanical

The unit is contained in a standard 19-inch wide rack-mountable chassis, 12-1/4 inches high by 19 inches deep. The unit is equipped with tilting slides for easy accessibility.

Power and signal inputs and outputs are located on the rear panel. The front panel has power and mode switches and indicators, along with several test BNC's for sync and signals.

5. Decoder Overall Block Diagram (Figure 3)

a. Memory Slave Sync Board

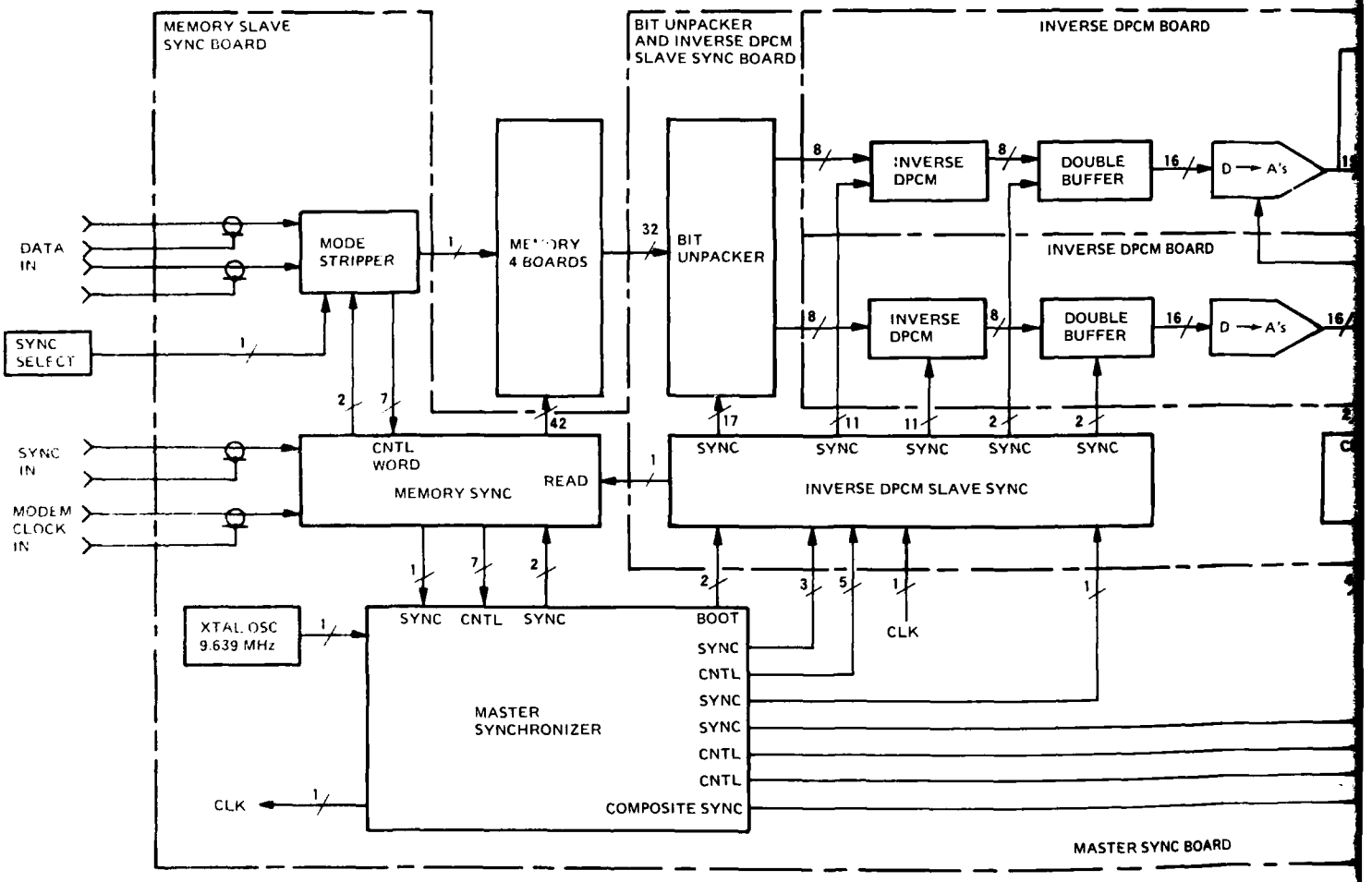
The signal inputs to this board are the signals out of the encoder unit or an intervening modem system. These signals are:

(1) Serial data

(2) Sync pulse

(3) Modem clock.

The "data in" is brought in on two separate connectors so that, as an option, the mode may be stripped off independent of the data, allowing the data to be jammed without jamming the mode word.


MEMORY SLAVE
SYNC BOARD
BIT UNPACKER
AND INVERSE DPCM
SLAVE SYNC BOARD
INVERSE DPCM BOARD
DATA
IN
MODE
STRIPPER
MEMORY
4 BOARDS
BIT
UNPACKER
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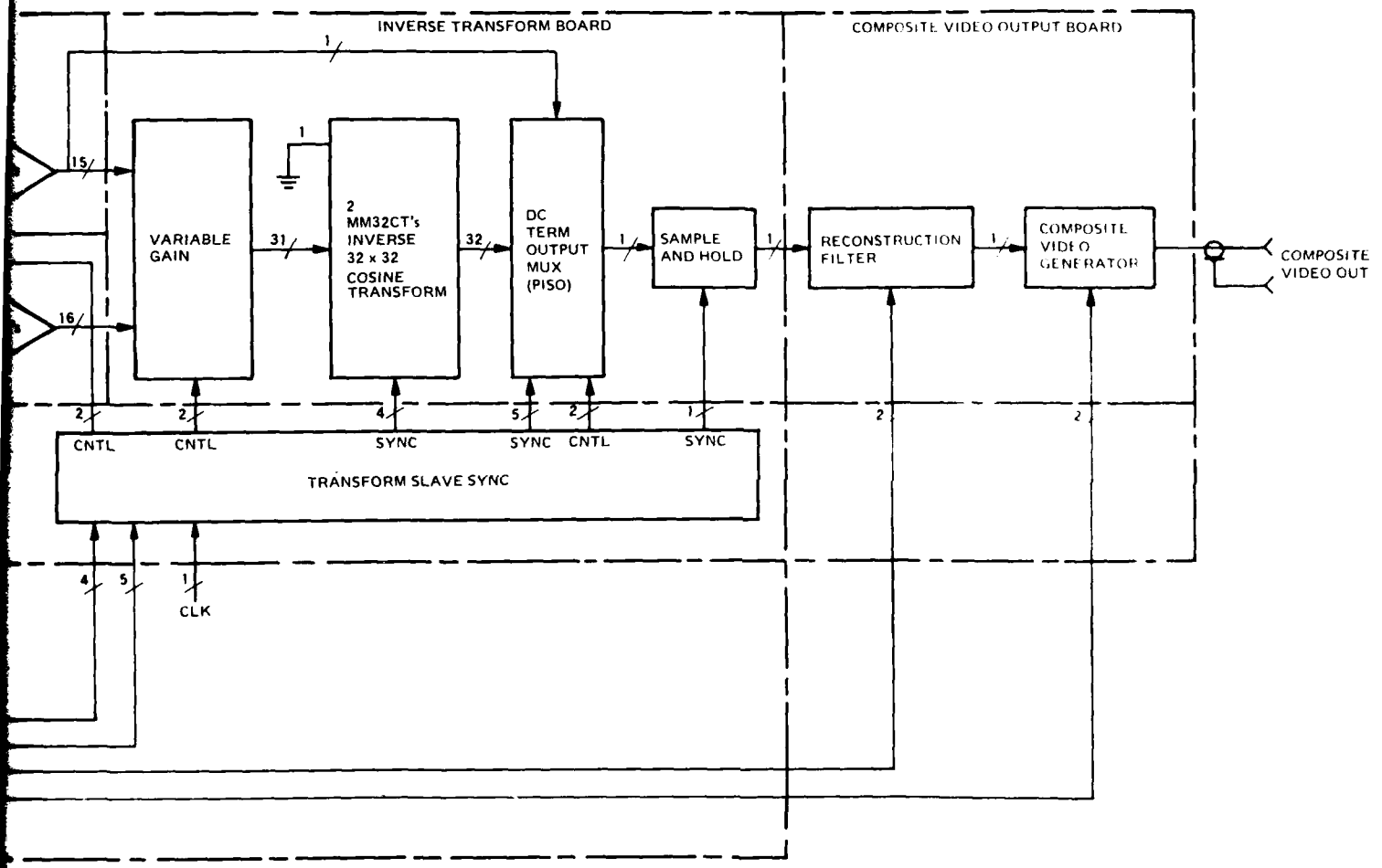


Figure 3. Decoder Overall Block Diagram

The mode information is stripped out of the front of the incoming data stream. It is used to set up the memory synchronizer so that when the memory is full, the memory synchronizer swaps over to its other half for reading out to the monitor. This allows a new picture to be read in while the old one is refreshing the monitor. The memory synchronizer also swaps the mode control word so that it remains with the corresponding memory contents.

b. Memory Boards

The four Memory Boards contain sufficient storage to hold twice over all the 32-bit words required for the greatest resolution, and highest number of bits per pixel for a single frame. The memory is organized into two parts to make a "swinging door" buffer so that one half can be filled while the other half is being used to refresh the monitor.

c. Master Synchronizer Board

The decoder master synchronizer contains a 9.639 MHz master crystal oscillator. A standard television composite sync generator is phased locked to this master oscillator to supply the composite sync for the output to the monitor. This master synchronizer is frame synced to the sync input from the encoder unit so that the decoder/encoder units are in basic frame synchronization. It provides the horizontal and vertical line syncs to the inverse DPCM slave synchronizer and the inverse transform slave synchronizer.

The inverse transform slave synchronizer receives its timing inputs from the master synchronizer and provides all the required pulses for the D/A's; the control signals for the variable gain amplifiers; and the clocks for the inverse transform, the output multiplexer, and the resampler.

d. Bit Unpacker and Inverse DPCM Slave Sync Board

The inverse DPCM slave synchronizer provides all the synchronization and control signals to the bit unpacker and the two inverse DPCM loops. The bit unpacker takes 32-bit words from the memory and unpacks them to form the 16 8-bit words per 32-pixel element that are the inputs to the two inverse DPCM loops.

e. Inverse DPCM Loop Boards

The inverse DPCM loop memories contain average coefficient values from the previous lines. These values are combined with the 8-bit words from the bit unpacker to generate the new coefficients for the inverse transform. Each loop generates 16 of the required 32 coefficients. The outputs of

DPCM loops are 16 words of 8 bits each, making a total of 32 8-bit words. These words are double buffered at the output of the inverse DPCM so that the D/A's feeding the inverse transform will have their data for an entire segment. Regardless of the real time resolution, the bit unpacker and inverse DPCM loops always operate at the same speed, which is the speed required of them in the 512 resolution case. In the two lower resolution cases, the DPCM loop operates rapidly, stops, and waits until it is time for it to be started again.

f. Inverse Transform Board

The 32 x 32 inverse cosine transform is fed through 31 variable gain amplifiers by the 32 D/A's. The variable gain amplifiers provide the reverse of what was done in the encoder when the individual coefficient gains were raised to allow the DPCM loops to operate in a manner that filled their full dynamic range with the small values of the lower order coefficients. The dc coefficient is bypassed around the transform to allow the transform to operate at a slightly better dynamic range.

The outputs of the inverse cosine transform are the values of the next 32 pixels with the dc component missing. These outputs are parallel-to-serial multiplexed, with the dc term added in continuously to form 32 picture elements in a row. To remove settling glitches, the output of this multiplexer is resampled each pixel. This part of the system operates in real video time; therefore, when resolutions are changed, the multiplexer speed must change with the resolution.

g. Composite Video Output Board

On this board, the resampled video is passed through a reconstruction filter whose time constant is changed as a function of resolution to provide smooth transitions from pixel-to-pixel. The video is then mixed with the composite sync and properly adjusted in amplitude to provide the standard NTSC (RS 170) composite video.

III. DETAILED MODULE DESCRIPTION

1. Encoder Module

a. Transform Processor Section

The Transform Processor block diagram is shown in Figure 4. This module is divided into four major sections; video input, forward transform, variable gain interface, and multiplexer and output buffer.

(1) Video Input Section

The video input section contains an amplifier, sync stripper and integrating sampler as shown in Figure 5.

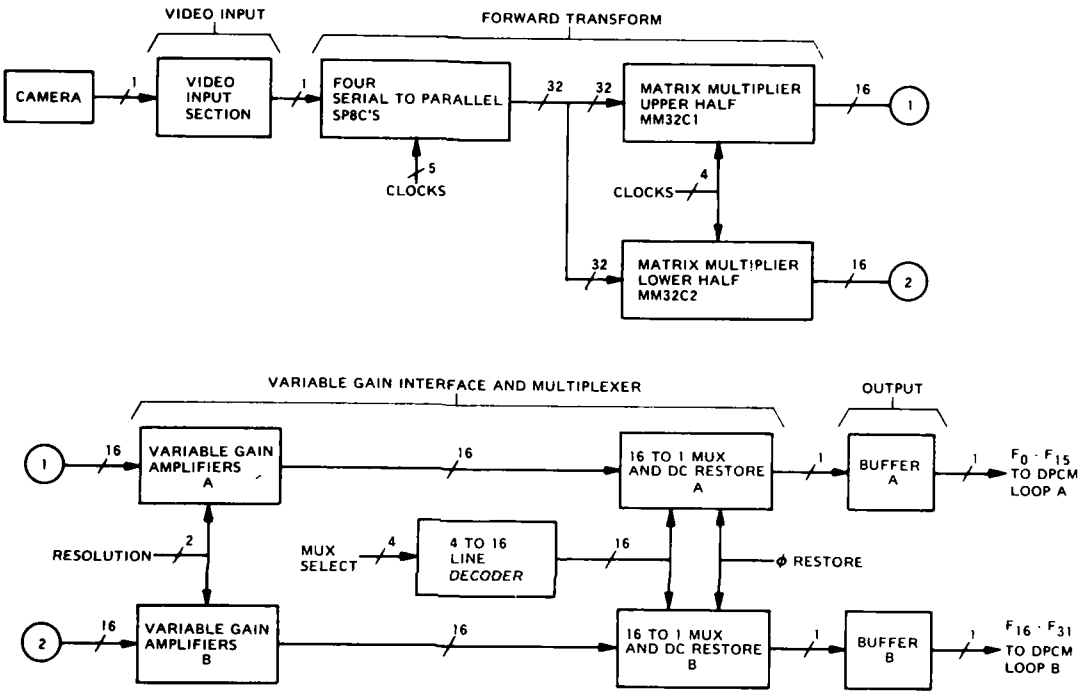


Figure 4. Transform Processor Block Diagram

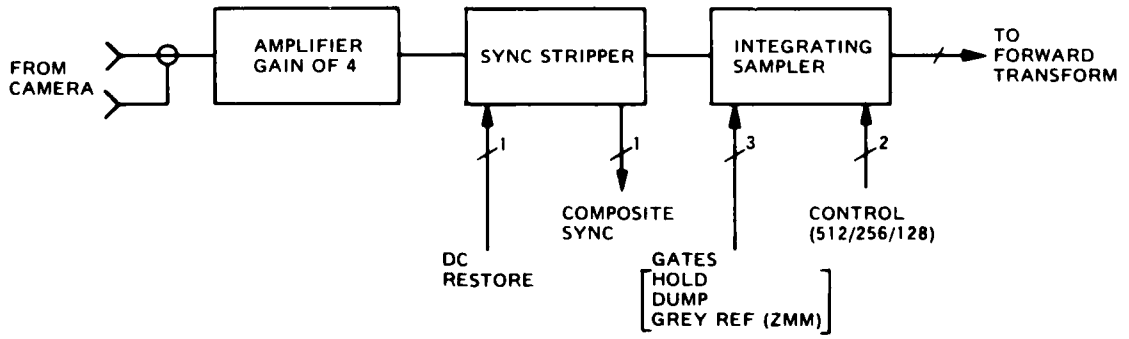


Figure 5. Video Input Section

The input video amplifier provides the correct terminating impedance (75 ohms) for the camera output and raises the video level to 4 volts peak-to-peak.

The sync stripper performs a dc restore on the input video using a precision gated restorer. A threshold comparator detects composite sync which is then stripped off and sent to the master synchronizer as a TTL level signal. The master synchronizer returns the dc restore gate to the sync stripper.

The integrating sampler provides a true power average (area under the curve) output for each pixel regardless of resolution mode. The circuit consists of a video voltage controlled current source whose output current is integrated in a capacitor to form the SP8C input voltage. This integration is performed during the bulk of a pixel time, held just prior to the SP8C "fill and spill" input sampling period and then dumped to zero to repeat the cycle for the next pixel time. The current source, capacitor, or both are changed with resolution changes.

The output to the SP8C is held at a grey reference level during the "zero matrix multiplier" (ZMM) gate which occurs during horizontal blanking time.

(2) Forward Transform Section

The Forward Transform Section performs a one-dimensional 32-point cosine transform on the input video which is described mathematically by:

$$F_K = \frac{1}{N} \sum_{i=1}^{N} X_i, \quad K = 0 \qquad (1)$$

and

$$F_K = \frac{2}{N} \sum_{i=1}^{N} X_i \cos \frac{(2i - 1)K}{2N}, \quad K = 1 \quad 31$$

where

$N = 32$
X_i = input video samples
F_K = cosine transform coefficients.

In matrix notation this is expressed as:

$$\underset{(32 \times 1)}{\begin{bmatrix} F_0 \\ F_1 \\ F_3 \\ \vdots \\ F_{31} \end{bmatrix}} = \sqrt{\frac{2}{N}} \underset{(32 \times 32)}{\begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & & 1/\sqrt{2} \\ C_{1,1} & C_{1,2} & \cdots & C_{1,32} \\ C_{2,1} & C_{1,2} & \cdots & C_{2,32} \\ \vdots & \vdots & & \vdots \\ C_{31,1} & C_{31,2} & \cdots & C_{31,32} \end{bmatrix}} \underset{(32 \times 1)}{\begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ \vdots \\ X_{32} \end{bmatrix}} \qquad (2)$$

where

$$C_{K,i} = \text{cosine transform kernel} = \cos \frac{\pi(2i - 1)K}{2N}, \quad \begin{matrix} K = 0 \rightarrow 31 \\ i = 1 \rightarrow 32 \end{matrix}$$

The 32-point cosine transform will be implemented using three General Electric designed devices which are currently being constructed. These are an eight port serial-to-parallel converter (SP8C), and two matrix multipliers with the required cosine weighting on chip (MM32C1,C2).

In order to implement the 32 x 32 cosine transform kernel matrix with the matrix multipliers, the partitioning shown in equation (3) will be implemented. Thus,

$$\begin{bmatrix} F_0 \\ \vdots \\ F_{15} \\ \hline F_{16} \\ \vdots \\ F_{31} \end{bmatrix} = \begin{bmatrix} \\ \text{MM32C1} \\ (16 \times 32) \\ \hline \\ \text{MM32C2} \\ (16 \times 32) \\ \\ \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ \vdots \\ X_{31} \\ X_{32} \end{bmatrix} \qquad (3)$$

where MM32C1 contains the upper half of the cosine matrix and MM32C2 contains the lower half of the cosine matrix.

Notice that the first 16 transform coefficients (F_0 through F_{15}) are obtained by multiplying all 32 input samples through MM32C1, and the last 16 transform coefficients (F_{16} through F_{31}) are obtained by multiplying all 32 input samples through MM32C2.

The function of the four SP8C serial-to-parallel converters is to obtain the 32 input video samples (X_i's) and format them into the 32 x 1 column vector required at the matrix multiplier inputs. This is accomplished by connecting the four devices as shown in Figure 6. The input video to SP8C No. 1 is sampled eight times at a 4.8 MHz rate, which takes 16 clock periods to achieve. The first eight odd-numbered samples are then output in a serial format through output port No. 9 while the next eight odd-numbered samples are being taken. At the same time SP8C No. 1 takes the remaining odd-numbered samples, SP8C No. 2 resamples the first set at its input. This procedure is duplicated using even-numbered samples by the other two SP8C's until, after 32 sampling clocks, all 32 samples appear in a column vector at the parallel outputs of the SP8C's. The parallel output data is available for approximately 29 clock periods (3 microseconds in the 512 resolution mode).

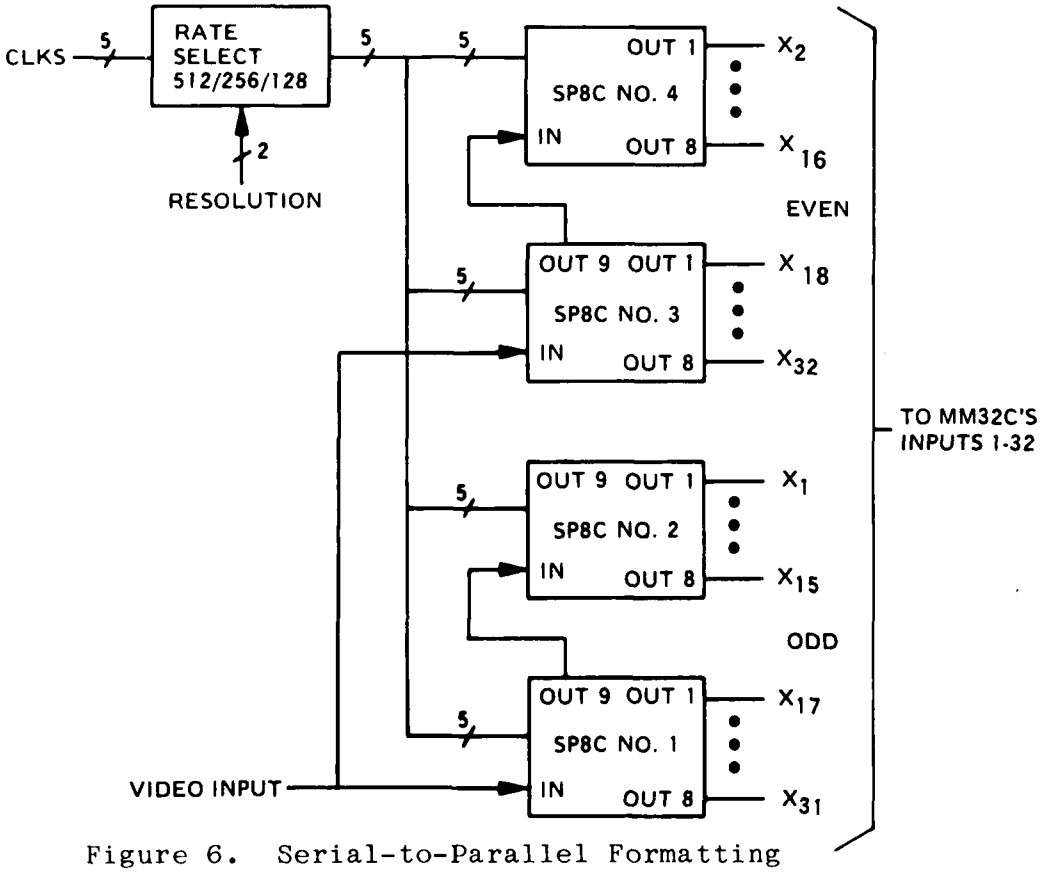


Figure 6. Serial-to-Parallel Formatting

The resolution selection determines the rate at which the serial-to-parallel devices sample the input video. This is accomplished by changing the Φ_C', Φ_C, Φ_L, Φ_p and Φ_{ID}

clock rates as shown below while maintaining the relative clock phasing. The timing for this section is shown in Figure 7.

Resolution	ϕc, $\phi c'$, ϕID (MHz)	ϕp, ϕL (MHz)
512	9.6	0.150
256	4.8	0.0750
128	2.4	0.0375

This 32 x 1 output vector of video samples is then applied to the inputs of both matrix multipliers as shown in Figure 8. The 16 outputs of MM32C1 are then the first 16 transform coefficients given by:

$$\begin{bmatrix} F_0 \\ F_1 \\ \vdots \\ F_{15} \end{bmatrix} = \sqrt{\frac{2}{N}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & \cdots & 1/\sqrt{2} \\ C_{1,1} & C_{1,2} & \cdots & C_{1,32} \\ \vdots & \vdots & & \vdots \\ C_{15,1} & C_{15,2} & \cdots & C_{15,32} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ \vdots \\ X_{32} \end{bmatrix} \quad (4)$$

and the 16 outputs of MM32C2 are the last 16 transform coefficients given by:

$$\begin{bmatrix} F_{16} \\ F_{17} \\ \vdots \\ F_{31} \end{bmatrix} = \sqrt{\frac{2}{N}} \begin{bmatrix} C_{16,1} & C_{16,2} & \cdots & C_{16,32} \\ C_{17,1} & C_{17,2} & \cdots & C_{17,32} \\ \vdots & \vdots & & \vdots \\ C_{31,1} & C_{31,2} & \cdots & C_{31,32} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ \vdots \\ X_{32} \end{bmatrix} \quad (5)$$

The transform coefficients are available at the matrix multiplier outputs for approximately 2.7 μsec in the 512 resolution mode.

Notice that at this point the transform coefficients have been divided into two distinct units, group A (F_0 through F_{15}) and group B (F_{16} through F_{31}). The desired 32 cosine transform coefficients are calculated at a 300, 150 or 75 kHz rate depending on the resolution mode selected. This is accomplished by changing the ϕ_1, ϕ_2, ϕ_R and $\overline{\phi_R}$ clock rates, keeping the same relative phasing. The timing diagram for the forward transform is also shown in Figure 7.

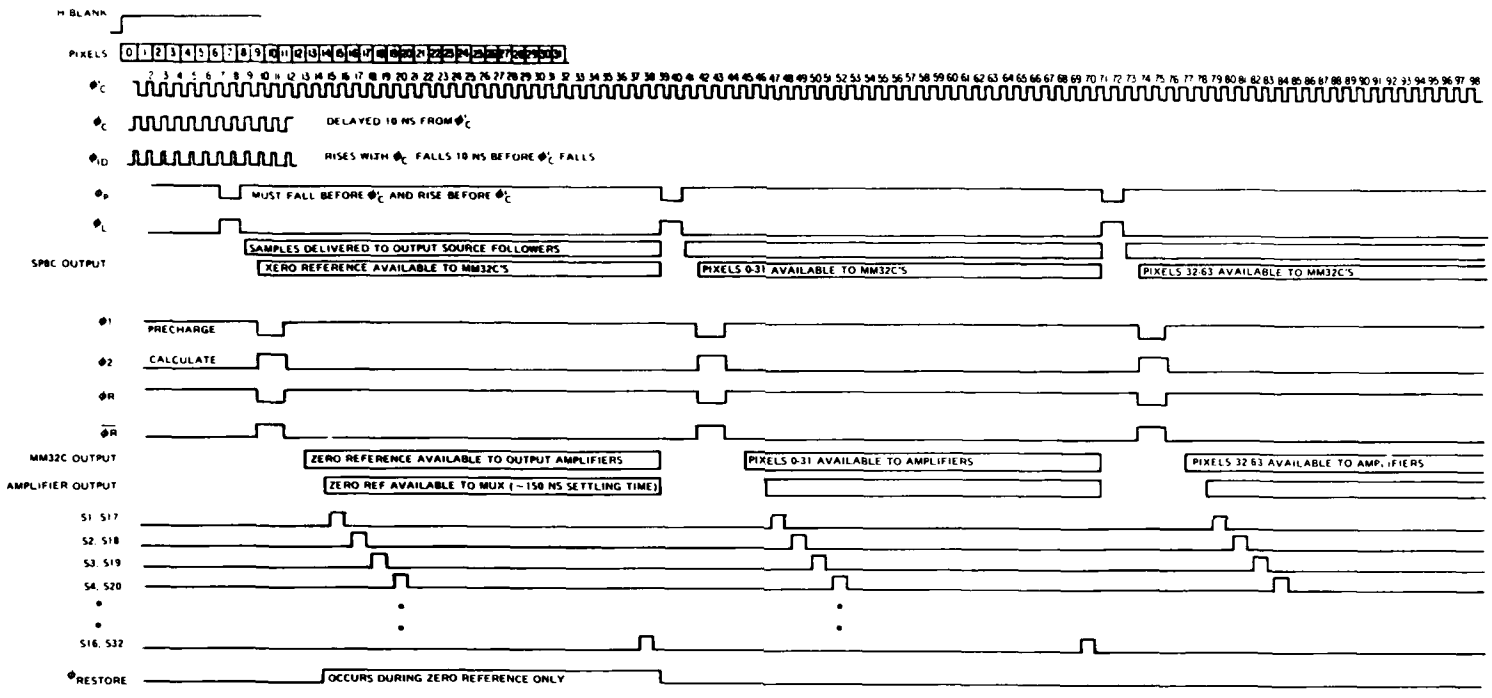


Figure 7. Encoder Master Timing

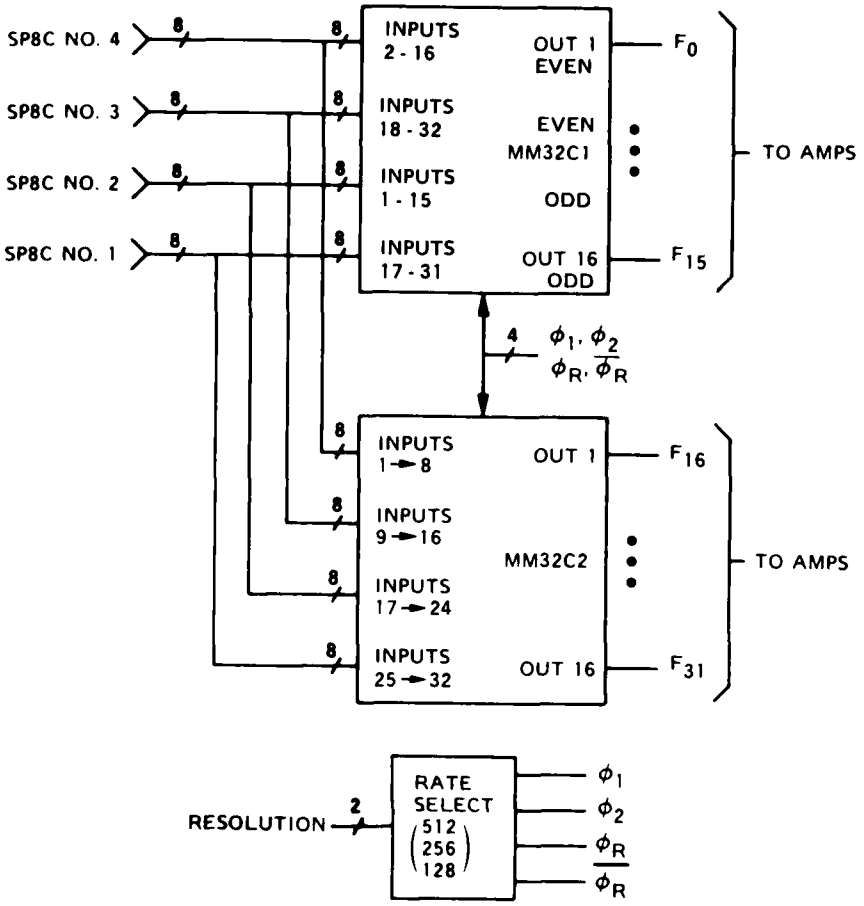


Figure 8. Matrix Multiplier Organization

(3) Variable Gain Interface and Multiplexer

This section is divided into two parallel paths as shown in Figure 4. For brevity, only one path will be described for the numerical gains of the amplifiers.

The purpose of the variable gain interface and multiplexer section is to select the 32 transform coefficients for use by the DPCM loops, to provide coefficient gain control and to remove bias or offset errors introduced by the SP8C or MM32C devices, which could be on the order of several tenths of volts over temperature.

The gain stage (Figure 9) is provided by 32 CA3100 operational amplifiers. The gain is switch-selectable to three levels depending on the resolution mode selected, using HI-201 analog switches. For example, R36 sets the gain for the 512 resolution while R1 and R2 set the gain for the 256 and 128

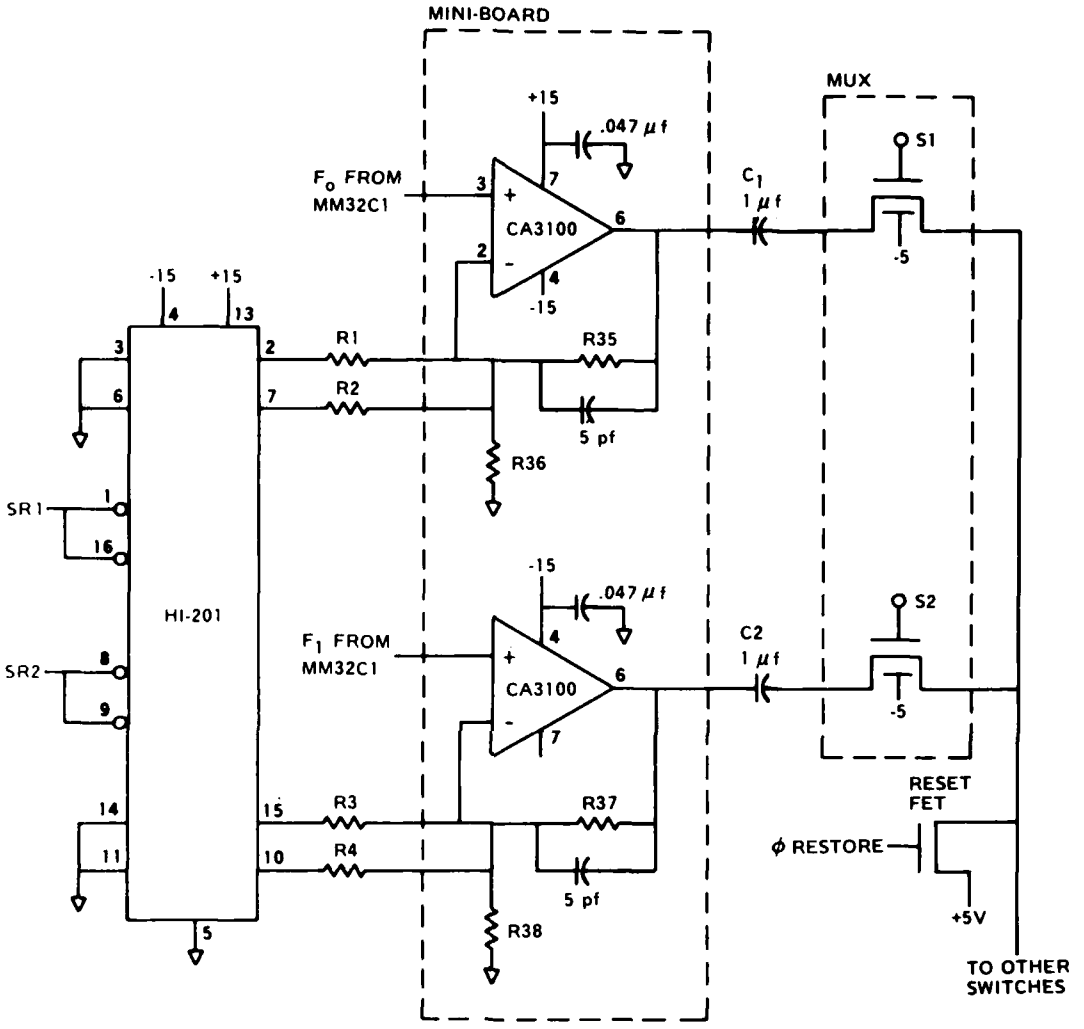


Figure 9. Typical Amplifier Mini-board Circuit

resolutions. The switching is performed simultaneously on all 32 output amplifiers. A typical amplifier miniboard circuit is shown in Figure 9. A printed circuit board contains two complete amplifier circuits in a space 1.0 in. x 0.15 in. x 0.4 in. The amplifier section contains 16 of these boards, 8 boards for each matrix multiplier. These amplifiers will provide an output swing > ±2 volts and will settle in 150 nsec. The output goes through a capacitor to an analog switch. The 16 SD-5000 analog switches in each of the two paths make up a high speed 16:1 analog multiplexer circuit which operates at 6.4 MHz. The control signals

for this multiplexer from a 4:16 line decoder which feeds open collector buffers that pull the control signals up to +15 volts. The 4:16 line decoder is run by the DPCM read address counter. Both multiplexers are run synchronously to interface with the two DPCM loops.

The capacitor, multiplexer, and reset FET together form the dc restore circuit. During horizontal blanking, a grey reference is applied to the transform. The restore FET turns on and the multiplexer is cycled through all its positions. This charges the capacitors (C1 through C32) to the reference transform levels. During the active line time, the reset FET is turned off, allowing the outputs to change as a function of the transformed video, independent of offsets introduced by the SP8C or MM32C devices.

The timing for the multiplexer and dc restore sections are also shown in Figure 7.

(4) Output Buffer

The Output Buffer stage is shown in Figure 10. These are LH0033 ultra high speed buffers, with an output offset adjust to center the grey reference level into the two DPCM loops. One circuit buffers the output of each variable gain interface and multiplexer path. The coefficients outputted to the DPCM loops are ±2 V levels centered at a 5 V reference level.

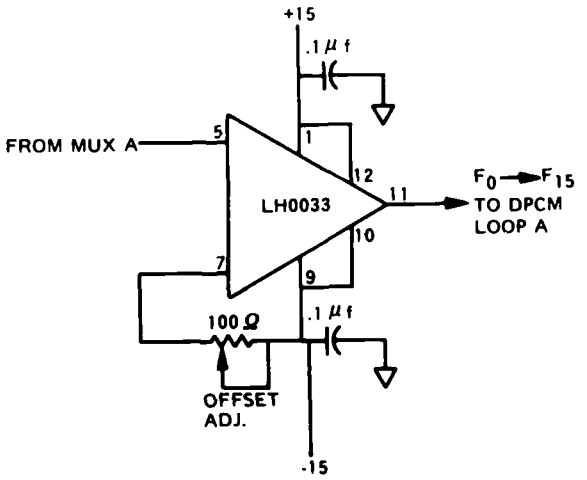


Figure 10. Typical Output Buffer

b. DPCM and Bit Packer

The differential pulse code modulation (DPCM) and bit packer block diagram is shown in Figure 11. These two units are used to DPCM and then bit pack a line of TV video data which is then stored in the frame store memory of the encoder. Inputs to the DPCM circuitry are 32 analog voltages representing the coefficients associated with a block of 32 pixels. The encoder has 2 DPCM loops, where each loop processes 16 coefficients whose outputs are time multiplexed to the bit packer logic which operates at twice the rate of each DPCM loop.

Operation of the two DPCM loops and bit packer logic is initiated by the SDPCM signal which is decoded from the master pixel counter. The occurrence of this signal is a function of the line resolution selected. It occurs 16 times per TV line in the 512 pixel mode, 8 times per TV line in the 256 pixel mode, and 4 times per line in the 128 pixel mode. The first active line of every field is DPCMed against zero via the ZFL signal which is decoded from the line counter of the encoder; each line thereafter is DPCMed against the previous line whose contents have since been stored in the DPCM line memory RAM.

Upon receipt of the SDPCM signal the DPCM read address counter steps through 16 addresses and then stops itself and waits for the next SDPCM signal to arrive. During these 16 read address times, the DPCM line memory sequentially places the DPCM coefficients of the previous line at the input to the DPCM D/A converter. At the same time, it sequentially selects the corresponding coefficient of the present line and gates them through the 16:1 analog multiplexer, via the four LSB bits of the read address, and places them at the input of the analog multiplexer buffer amplifier. These two analog signals are then summed and A/D converted to an 8-bit number and requantized by DPCM PROM No. 1 to a 5-bit number. This 5-bit number is then handed off to the bit packer and at the same time requantized to an 8-bit number by DPCM PROM No. 2. This 8-bit requantized number is a function of the number of bits saved by the bit packer. The requantized 8-bit output word from DPCM PROM No. 2 is then summed with its corresponding value as it appeared at the beginning of the cycle when it was read out of the DPCM line memory. This summed output from DPCM Adder No. 1 is then checked for overflow and underflow and limited if necessary. The 8-bit output from the limiter is then scaled by Adder No. 2 and presented to the input of the DPCM line memory. The data being presented to the input of the line memory at the end of a DPCM cycle is written back into the line memory at the same address from which it was read at the beginning of the cycle. This completes one cycle of the DPCM loop. Sixteen cycles are required by each DPCM loop to process a block of 32 pixels.

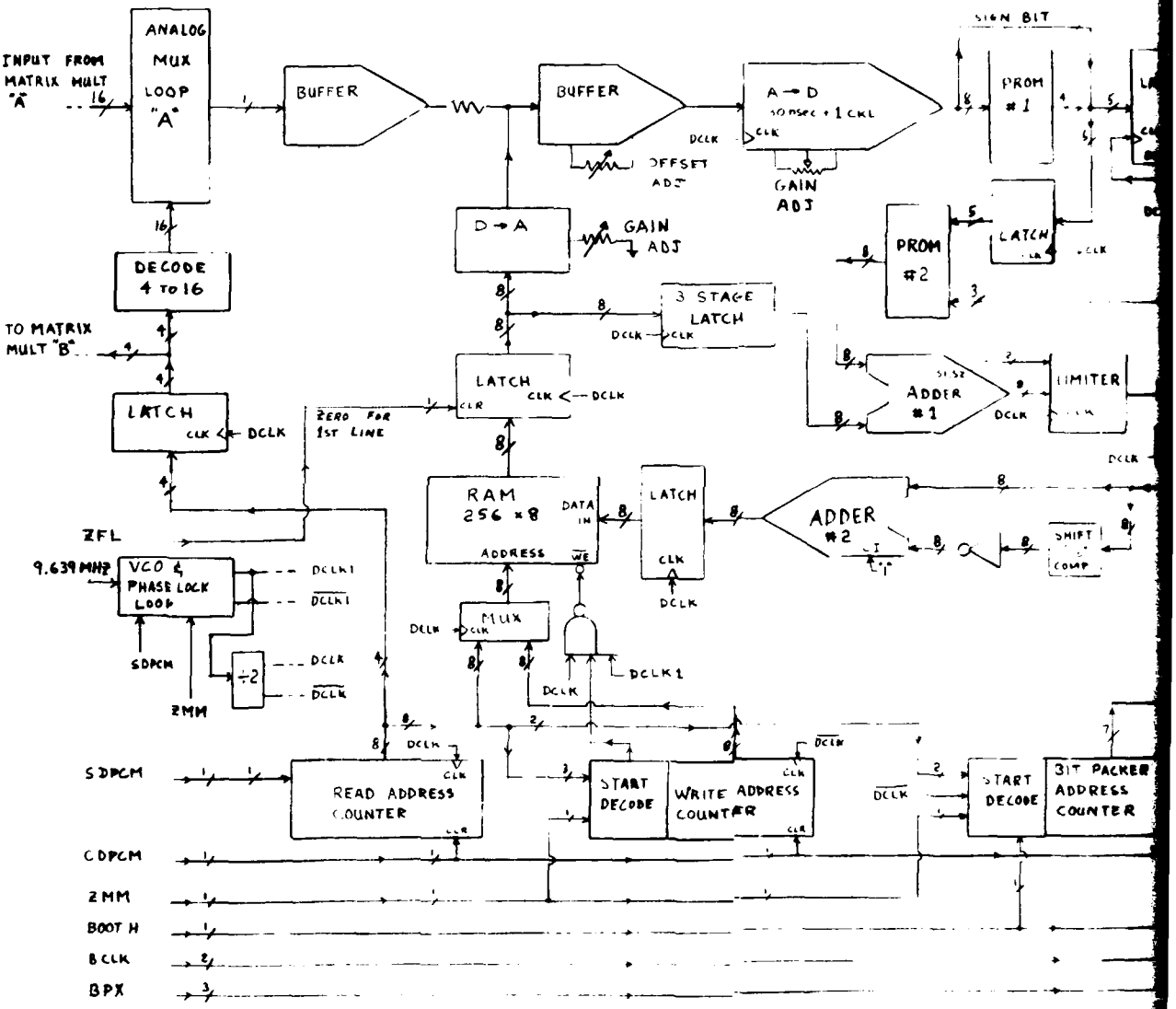


Figure 11. Encoder DPCM

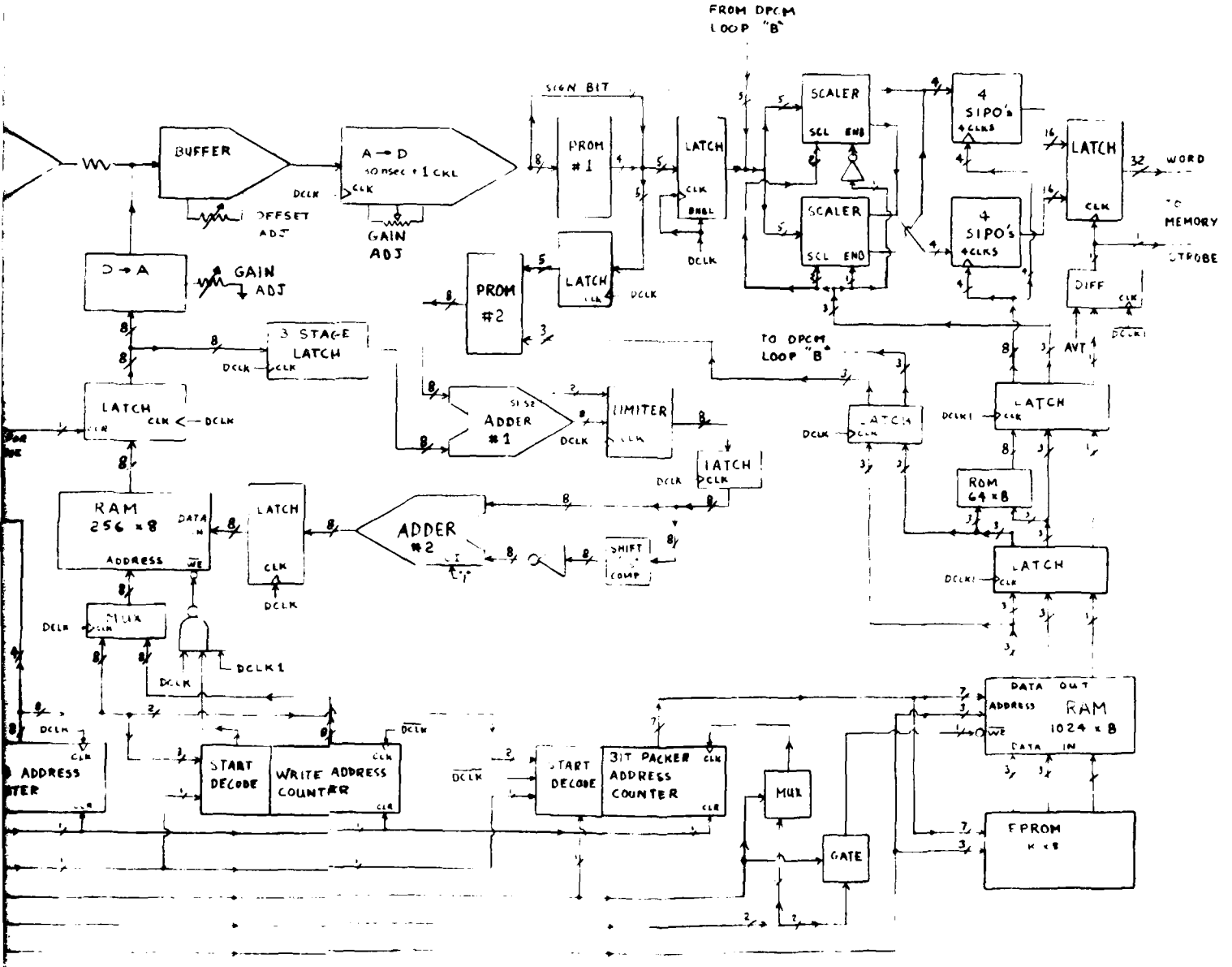


Figure 11. Encoder DPCM and Bit Packer Detailed Block Diagram

A separate write address counter is required by the DPCM line memory due to the 6-clock-period delay through the DPCM loop before data is available to be written back into the line memory at the same address, from which it originated. The delayed 6-clock-period start of the write address counter is accomplished by using the decode of six from the three LSB's of the read address counter to start the write address counter. Once the write address counter is started, it also steps through 16 addresses and then stops itself in the same manner as the read address counter.

The bit packer takes the 32 consecutive 5-bit words presented to it by the two DPCM loops and saving from 0 to 5 bits of each word. These saved bits are then packed into continuous 32-bit words, which are then stored in the encoder's frame store memory. The bit packer is controlled by its own RAM memory which is boot loaded from the EPROM during the vertical blanking time of Field No. 1. The bit packer RAM contains seven bits of information for each coefficient presented to it for packing. The information in this 7-bit word is as follows: 3 bits are used to tell how many bits of each 5-bit word are to be saved, 2 bits are used by the scalers to align the 5-bit input word with the appropriate serial-in/parallel-out shift registers, 1 bit is used to exchange scaler outputs. Thus a wraparound function of the 5-bit input word is provided with respect to the serial-in/parallel-out shift registers, and the last bit is used to signal the frame store memory that a 32-bit word is ready to be stored. The first 6 bits described above are also used to address a 64 x 8 ROM which generates the 8 clock strobes used to serially clock the 8 serial-in/parallel-out bit packer output shift registers. The bit packer read address counter is started three clock periods after the start of the DPCM read address counter. The three-clock-period delay represents the group delay time through the DPCM loop before valid data is presented to the bit packer. Once started, the bit packer read address counter steps through 32 addresses and then stops itself and waits for the next decode of 3 from the read address counter before starting again. These 32 bit packer addresses provide 16 bit packer control words for each of the 21 DPCM loops. Figure 12 shows the relative timing between the three address counters used in the DPCM and bit packer circuitry.

The external control inputs required by the DPCM loops and bit packer are frame rate, resolution, bits per pixel, and mode change.

c. Frame Store Memory

The encoder frame store memory receives 32-bit parallel data words from the encoder bit packer and provides 32-bit data words serially to the modem. A frame 0 (FR0) input signals

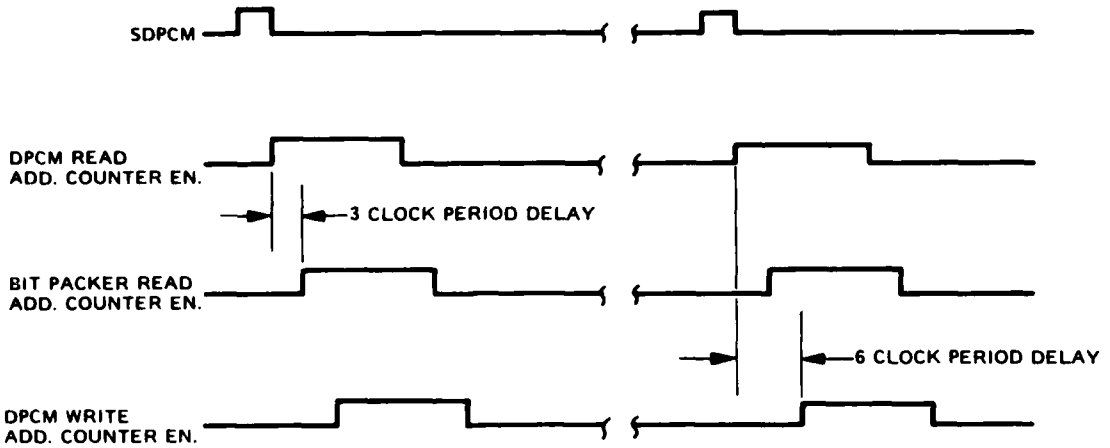


Figure 12. DPCM and Bit Packer Address Counter Relative Timing

that incoming data words are to be stored and transmitted, and a data strobe (DATA$) input indicates that a data word is currently on the data lines.

Other inputs to the memory includes a 9.6 MHz clock, a modem clock, and a 16-bit control word. The control word is transmitted immediately preceding the start of a frame of serial data. For built-in-test purposes the memory is capable of generating its own FRO, DATA$, 9.6 MHz clock, and modem clock. When in the test mode, the 32-bit word present on the data lines will be stored and transmitted regardless of the states of the other inputs.

A complete cycle of the memory starts with a FRO signal. The first data word will be latched into Memory 1 by the incoming DATA$. The word is then written into location 0 of Memory 1 and the memory address is incremented. Each successive word is written in successive memory locations until the first field of FRO is completely stored in Memory 1. The second field of FRO is then stored in the same manner in Memory 2. When Memory 1 has been filled, data will immediately start being read from Memory 1 starting at location 0. Each word is read into a parallel-in/serial-out (PISO) shift register. The serial data passes through a selector to a 16-bit shift register. As the first word is read into the PISO, a sync signal is generated. This sync signal loads the control word into the 16-bit shift register. The control word will thus immediately precede the signal data to the modem. The sync signal is delayed with a shift register so that it is outputted with the last bit of the control word. The sync and the serial data are outputted to the modem.

(1) Memory Section

Figure 13 is the detailed block diagram of the Memory section. A DATA$ is provided by the timing and control board to latch incoming data whether or not it is used. A write signal (WR1, WR2) from the control board is present if the data is to be written. The write signal enables the output of the latch and disables the output of the memory. Thus the incoming data word is placed on the memory data bus.

A 13-bit address word provided by the control board provides memory addressing. The lower 10 bits are provided directly to the memory address bus. The upper three bits are decoded to provide eight chip selects. Together the address word permits addressing of 8192 32-bit words. A write enable ($\overline{WR1}$, $\overline{WR2}$) provided by the control board writes the word on the data bus into the location specified by the address word.

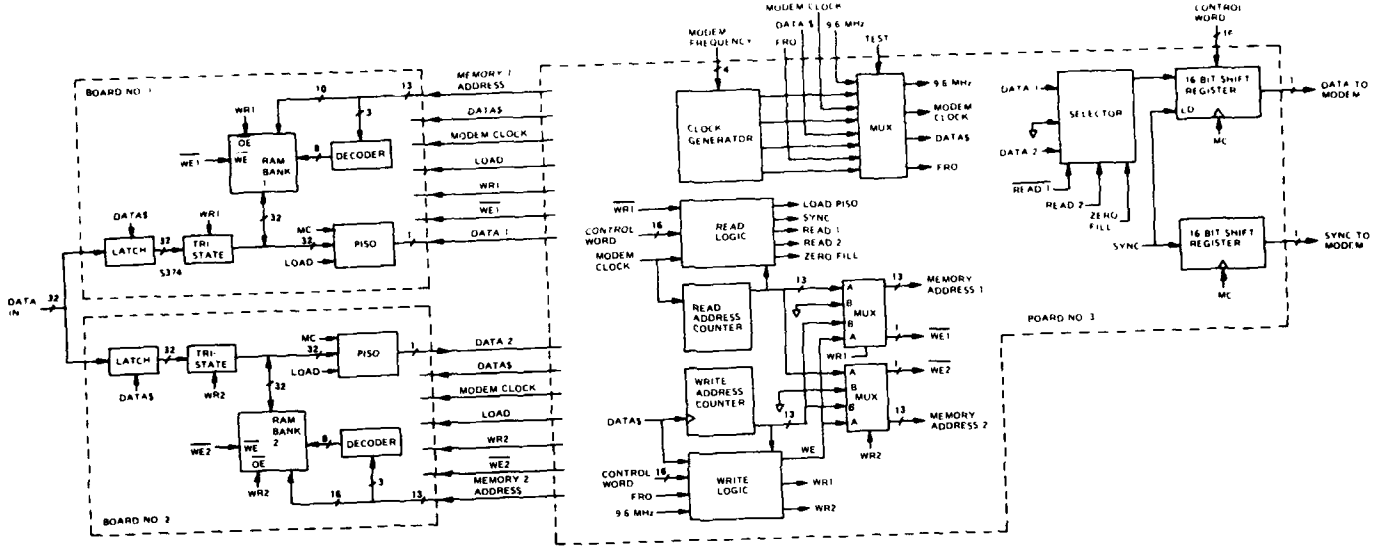


Figure 13. Encoder Memory Block Diagram

When the write signal (WR1, WR2) is in the disable state, the memory board is in the read mode. The tristate output of the latch is disabled and the data bus carries the word stored at the memory location specified by the address word. A load signal from the control board loads the 32-bit word into the parallel-in/serial-out shift register. The word is then shifted out serially to the control board.

(2) Timing and Control (Figure 14)

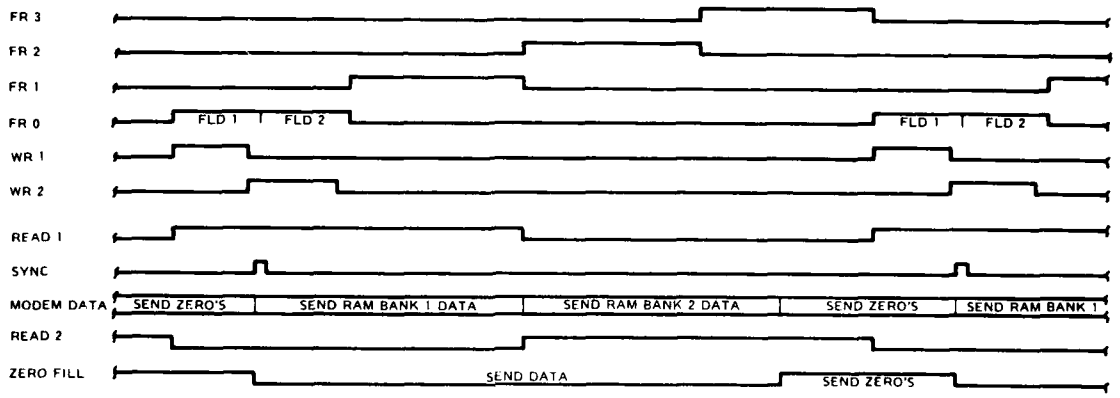


Figure 14. Encoder Memory Timing Diagram

The Timing and Control board is divided into four sections: read logic, write logic, control word insertion, and built-in-test.

The four signals required for the operation of the encoder memory are the modem clock, the 9.6 MHz clock, FR0, and DATA$. If these signals are not provided, they may be generated by the built-in-test circuitry. A test control signal determines whether the input signals or the internally generated signals are used. The test circuit can generate all of the required modem rates and these rates are determined by a 4-bit word.

Control word insertion is accomplished using shift registers. The SYNC signal generated by the read logic shifts the control word into the register which adds it to the front of the signal data. A shift register also delays the SYNC signal. The data selector is controlled by READ 1 and READ 2 signals from the read logic and selects the memory from which the serial data is being read. A third signal, ZERO FILL, holds the selector output at 0 regardless of the other selector signals.

The write logic circuitry generates the signals required to correctly write the data words into the memories. The leading edge of a FRO initializes the counter and each subsequent DATA$ increments the counter. When the counter reaches an address determined by the control word, it is reset to 0 and counts Memory 2 locations. The WR1 and WR2 signals determine which memory will be written into and also control the address multiplexers which determine whether read or write addresses go to each memory. The WR signal is generated in the write logic and writes the data word into memory.

The read logic generates the signals needed to sequentially read a complete frame of information and send out the data words serially to the modem. The read logic is initialized by the the trailing edge of a WR1 signal so that the reading of data begins as soon as the first memory has been filled. Data words are loaded into the PISO shift register every 32 modem clocks to give a continuous data stream until both memories have been sent. As with the write logic, the number of words per memory is obtained from the control word and this information is used to switch memories. When the second memory has been read, a ZERO FILL signal is generated which causes zeros to be sent to the modem until a new frame is ready to be sent. The sync pulse is generated at the start of the read cycle.

d. Encoder Master Synchronizer

The Encoder Master Synchronizer board (Figure 15) contains five basic sections: the master clock and sync generator, the pixel sync generator, transform sync generator, the line sync generator, and the picture sync generator.

(1) Master Clock and Sync Generator

The fundamental frequency source for the master synchronizer is a 19.278 MHz voltage controlled oscillator (VCO) that is divided by 2 to obtain the master 9.639 MHz pixel clock. This VCO is phase locked to the leading edge of the incoming video composite sync such that there are 612 clocks per horizontal line time. In addition, the incoming composite sync Field 1 pulse is detected for line counter synchronization.

(2) Pixel Sync Generator

The pixel counter, using the 9.639 MHz clock, counts out 612 pixels per Load Horizontal ($\overline{\text{LDH}}$). $\overline{\text{LDH}}$ is a single pixel in length and occurs during the 612th pixel. The pixel address following the trailing edge of $\overline{\text{LDH}}$ is all zeros. The first 100 pixels are horizontal blanking time, the remaining 512 are active video.

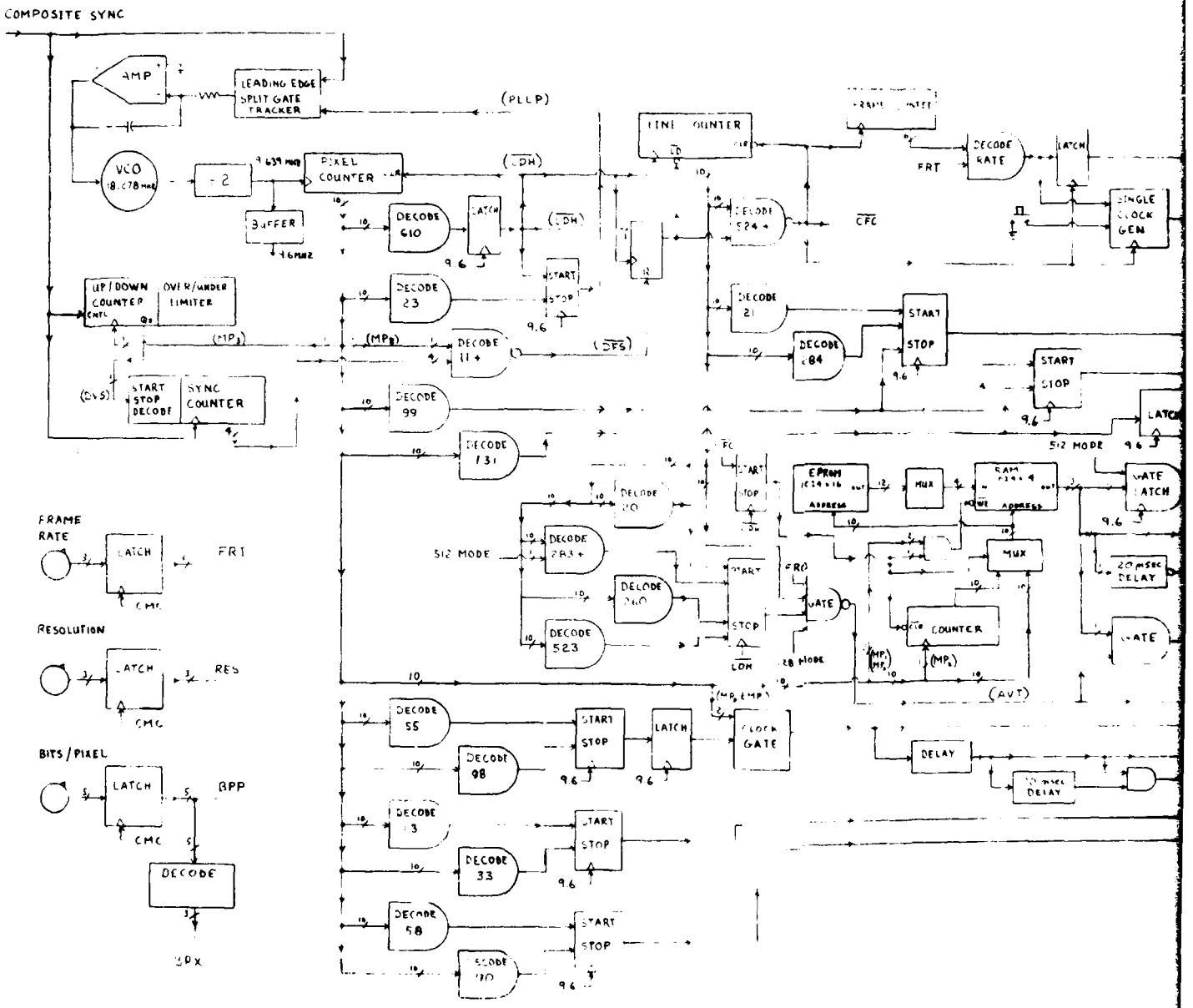


Figure 15. Encoder Master Synchronizer Detailed B

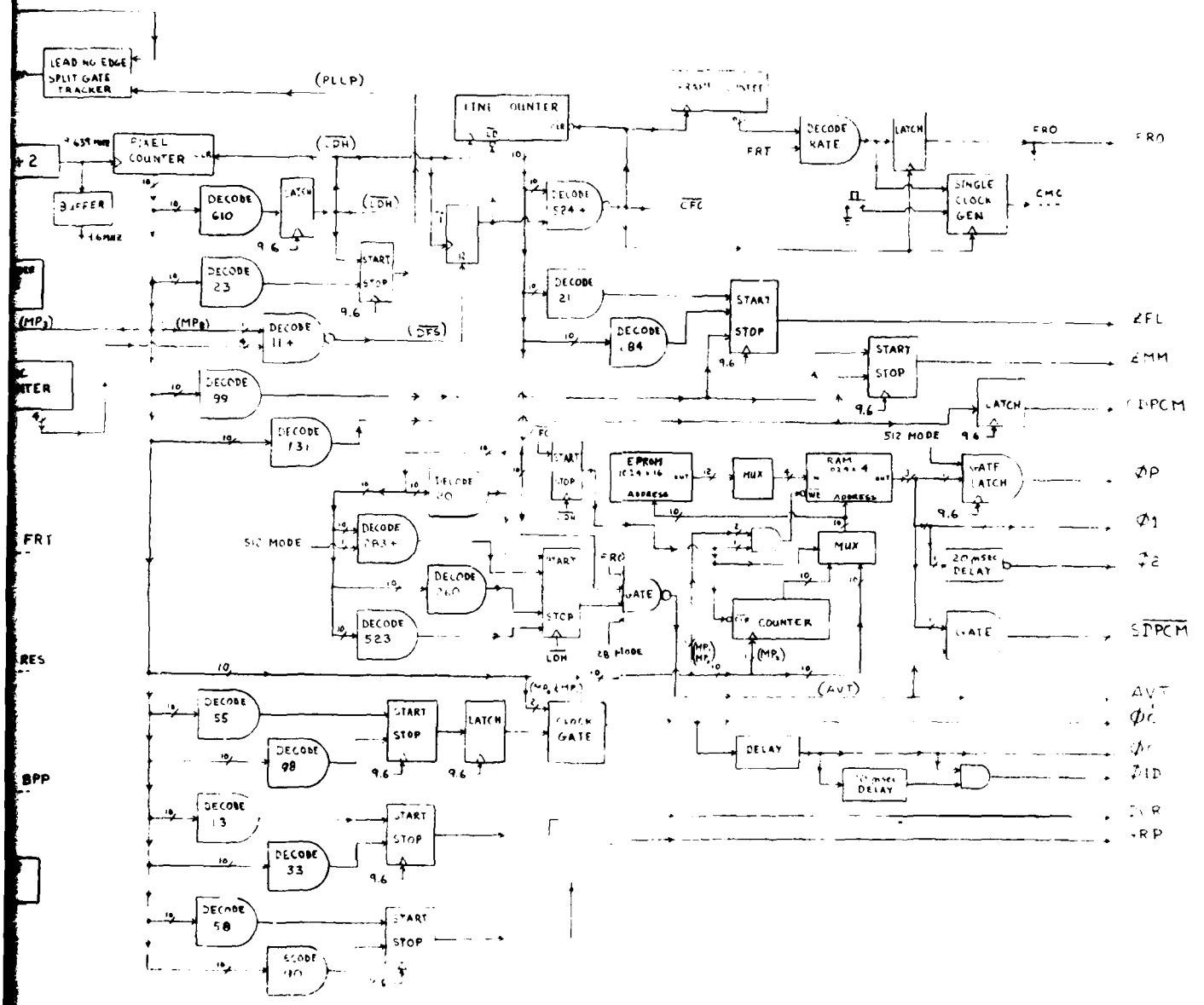


Figure 15. Encoder Master Synchronizer Detailed Block Diagram

The pixel synchronizer generates the pulses for the phase-locked loop (PLLP), the dc restoration (DCR), the clear DPCM (CDPCM), and the start DPCM (SDPM).

(3) Transform Sync Generation

Closely connected to the pixel counter is the transform sync generator, which produces all the pulses required by the series-to-parallel and cosine transform chips. The exact timing of most of these clocks and pulses is controlled by a high speed RAM that is "boot loaded" from UV-EPROM during Field 1 vertical blanking. This allows easy alteration of timing during debug and initial system evaluation. In addition, tapped delay lines are used for some clocks to obtain correct phasing. The timing variations for different resolution modes are stored in different parts of the RAM.

(4) Line Sync Generation

The line counter counts out 525 lines per frame. The clock field counter ($\overline{CFC}$) is a line time in length and occurs for the 525th line. The line address is all zeros following the trailing edge of $\overline{CFC}$. The first 21 lines are vertical blanking and are followed by the 240 active video lines of Field 1. The next 23 lines are vertical blanking again followed by the 240 active video lines of Field 2. A single line at the end of Field 2 is added to the first vertical blanking period to form a total of 22 lines of vertical blanking. This preserves the interlace for a standard TV signal.

The line synchronizer generates the boot and address signals to load the DPCM/bit packer control RAM from EPROM during Field 1 vertical blanking. It generates the active video time (AVT) gate and the zero first line (ZFL) gate.

(5) Picture Sync Generation

The frame counter counts out 2, 4, 16, or 64 frames to obtain the frame zero (FR0) that will be compressed, digitized, stored, and transmitted. The number counted between FR0's is part of the mode selection. The other output of the picture synchronizer is the change mode clock (CMC) that causes a mode change on the next FR0 when the front panel button is pressed.

2. Decoder Modules

a. Display Refresh Memory

The display refresh memory receives serial data from the modem and provides 32-bit parallel data words to the bit

unpacker. An incoming sync signal latches the received control word and indicates the start of a frame of data. Two complete frames can be held in memory so that one may be read while another is being stored. A sync signal output indicates that a new frame is ready to be read by the bit unpacker. The bit unpacker then controls the reading of the data.

Inputs to the display refresh memory include a 9.6 MHz clock, a modem clock, the serial data, and sync. The bit unpacker provides a read strobe (READ$), and LINE START, and REREAD signals to control the reading of frames of data. The 16-bit control word is stripped from the start of an incoming frame and is made available as an output. When in the test mode, the 9.6 MHz clock and the READ$ are generated internally.

A complete cycle of the memory begins with an incoming SYNC signal which strips the control word and resets the write counters. After 32 modem clocks, the first data word is contained in the serial-in/parallel-out shift register and will be latched into each memory board. The latch outputs are enabled only in Memories 1 and 2. The word is then written in location 0 of Memory 1. Each successive word is then written in successive memory locations until the first field is written. The next word will be written in location 0 of Memory board 2 and so on until a complete frame is contained in Memories 1 and 2. Writing is then stopped until another SYNC is received. The next sync signal will start the write sequence in Memory 3 so that the second frame is stored in Memories 3 and 4. The start of a write sequence in Memories 1 and 2 will simultaneously cause the read sequence to start in Memories 3 and 4. The read sequence begins with location 0 of Memory 3 and the read addresses are incremented by the trailing edge of the READ$ from the bit unpacker. The SYNC OUT signal tells the bit unpacker that the next data word read will begin a frame. The complete frame will be read from Memories 3 and 4; either 2, 4, 16, or 64 times depending on the mode of operation while a single frame is being written into Memories 1 and 2.

(1) Memory Section

Block diagrams of the memory boards are shown in Figure 16. The serial data enters each memory board through a serial-in/parallel-out shift register. Every 32 cycles of the modem clock, a LOAD signal from the control board causes a complete 32-bit parallel word to be latched. A write signal (WR1, WR2) enables the output of the latch and disables the output of the memory. Thus the data bus will contain an incoming data word.

The memory addressing is the same as for the encoder memory. The upper 3 bits of the 13-bit memory address

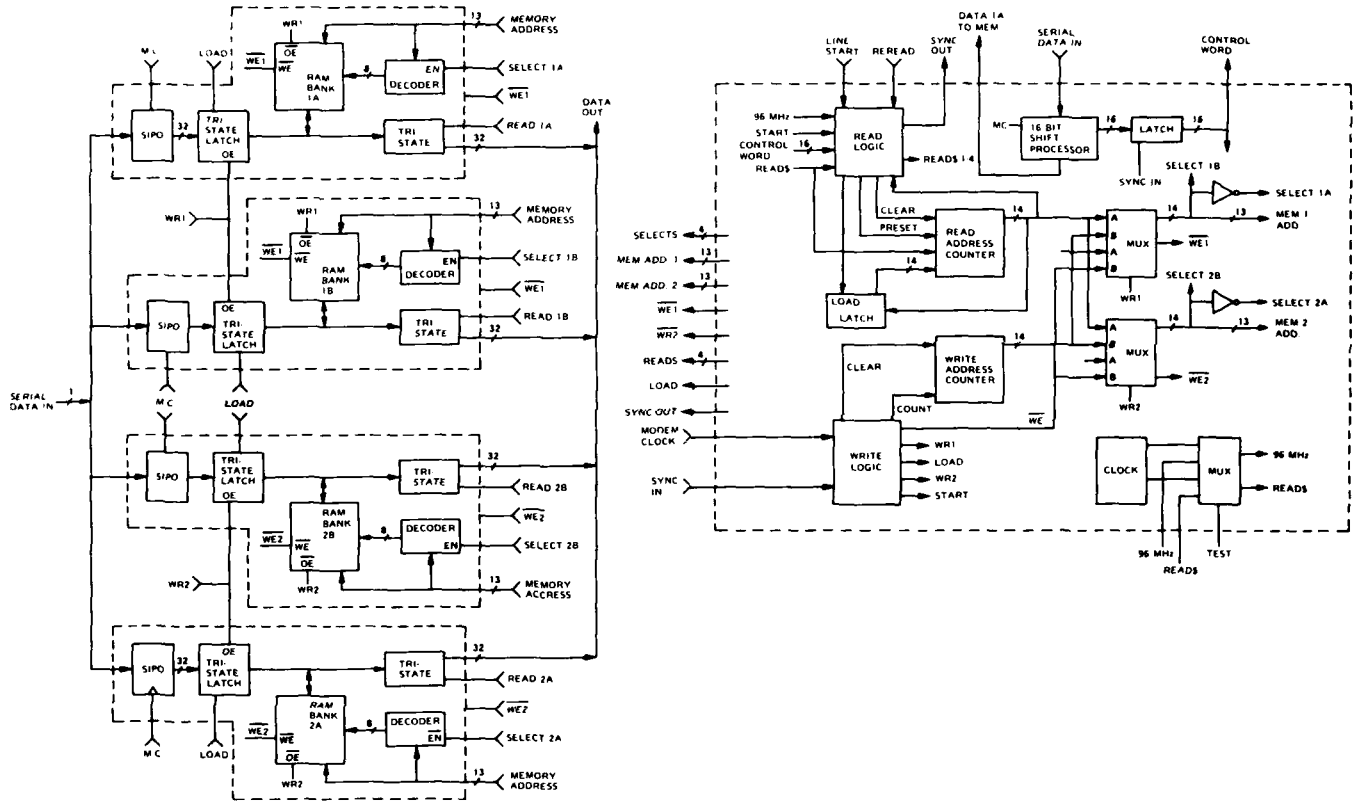


Figure 16. Display Refresh Memory Block Diagram

Figure 16. Display Refresh Memory Block Diagram

word are decoded to provide chip selects. The lower 10 bits become the address signal input to each 1K x 8 RAM. A write enable (WR1, WR2) signal causes the word on the data bus to be written at the specified address.

When in the read mode, the WR1 signal disables the output of the input data latch and enables the memory output. The data bus then contains the data word contained in memory at the address specified. A read signal then enables the output of the tristate output buffer. At any given time, only one memory board will have the output buffer enabled. The word on the output data lines will be changed only when a READ$ from the bit unpacker indicates that the word has been used. At that time the memory address will be incremented.

(2) Timing and Control (Figure 17)

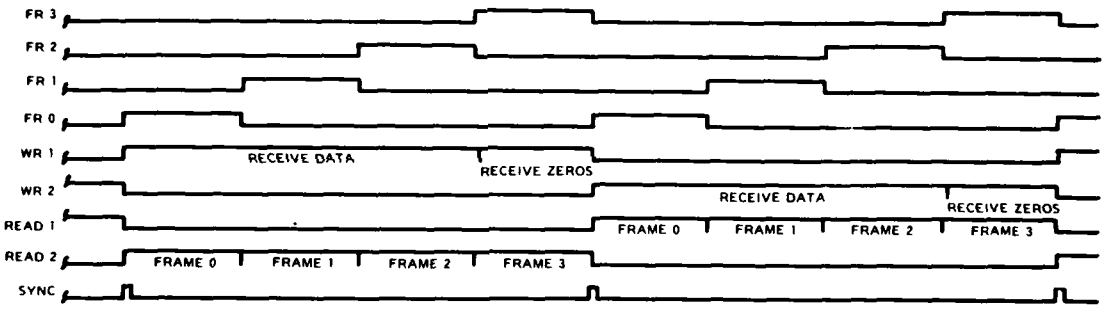


Figure 17. Display Refresh Memory Timing Diagram

The Timing and Control circuitry is basically composed of the same four sections as the encoder timing and control; read logic, write logic, control word stripping, and built-in tests.

The decoder memory requires a modem clock, a 9.6 MHz clock, and a read strobe. When in the test mode, the 9.6 MHz clock and read strobe are generated internally, but the modem clock must be the same as the clock in the encoder. The test signal switches the memory from external 9.6 MHz clock and read strobe to the internally generated ones, but it is expected that the modem clock will be supplied from the encoder.

The 16-bit control word precedes a frame of serial data and is latched as it passes through the 16-bit shift

register. As the last bit of the control word enters the shift register, the sync signal goes high. The trailing edge of the clock pulse then causes the control word to be latched so it is continuously available and updated with each frame.

The write logic generates the signals for converting the serial data to parallel and for writing it into memory. The incoming sync signal initializes the write logic and starts the bit counter. Every 32 modem clock cycles, a LOAD signal is generated to latch in the 32-bit words. Fifteen modem clocks after it is latched, a write enable pulse (WE) writes the word into memory. The address counter is incremented by the load signal except for the first word. On the first LOAD pulse, counting is inhibited so that the first word is written at location 0. Counting proceeds until an entire frame has been stored. In the encoder memory, the counter needs to count only a field, whereas the decoder memory must count a frame. Thus, a 14th bit is needed. This bit controls whether data is being written into the first or the second of the pair of memory boards available at the time for writing. The write signals (WR1, WR2) determine the pair of memory boards to be written into, and also control the address multiplexers. The write signals simply toggle back and forth with each incoming signal. It is not necessary for the read logic to know the number of words per frame since writing can be inhibited when the memories are full.

The read logic is initialized by a start signal from the write logic and generates a sync output indicating that a new frame is starting. Once started, the read logic is controlled by incoming READ$, LINE START, and LINE REREAD signals. The counter is similar to the write address counter except that it has the capacity to reread a group of data words. The READ$ input causes the memory address to be incremented on the trailing edge so the next data word is available. If a particular group of data words is to be reread, a LINE START causes the current address to be saved. When it is desired to return to that address, a REREAD signal restores it to the read address counter. When a complete frame of data has been read, the counter is returned to 0 and the read process continues. The number of words per frame is obtained from the control word.

b. Bit Unpacker and Inverse DPCM

The Bit Unpacker and Inverse DPCM are shown in Figure 18.

The bit unpacker used in the decoder performs the function of reconstruction 32 consecutive 8-bit words per picture segment from the 32-bit words being presented to it by the decoder frame store memory. These reconstructed 8-bit words that the bit unpacker produces correspond to the DPCM PROM No. 2

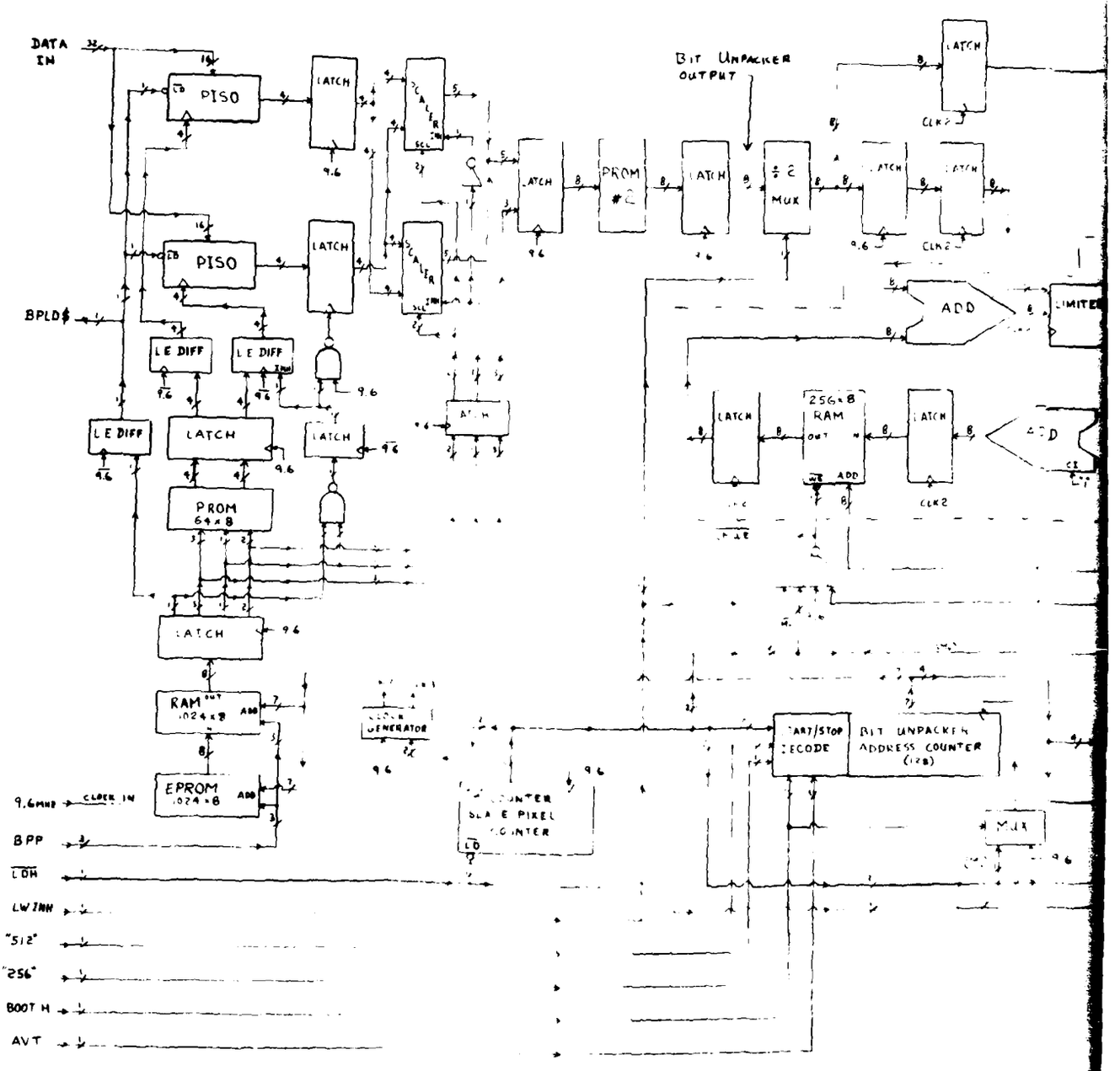

DATA IN
PISO
PISO
LATCH
BPLD$
LE DIFF
LE DIFF
LE DIFF
LATCH
LATCH
PROM 64 x 8
LATCH
RAM 1024 x 8
EPROM 1024 x 8
9.6MHz
CLOCK IN
BPP
LDH
LWINH
"512"
"256"
BOOT H
AVT
BIT UNPACKER OUTPUT
LATCH
PROM #2
LATCH
÷ 2 MUX
LATCH
LATCH
ADD
LIMITER
LATCH
256 x 8 RAM
LATCH
ADD
CLK2
START/STOP DECODE
BIT UNPACKER ADDRESS COUNTER (12B)
MUX

Figure 18

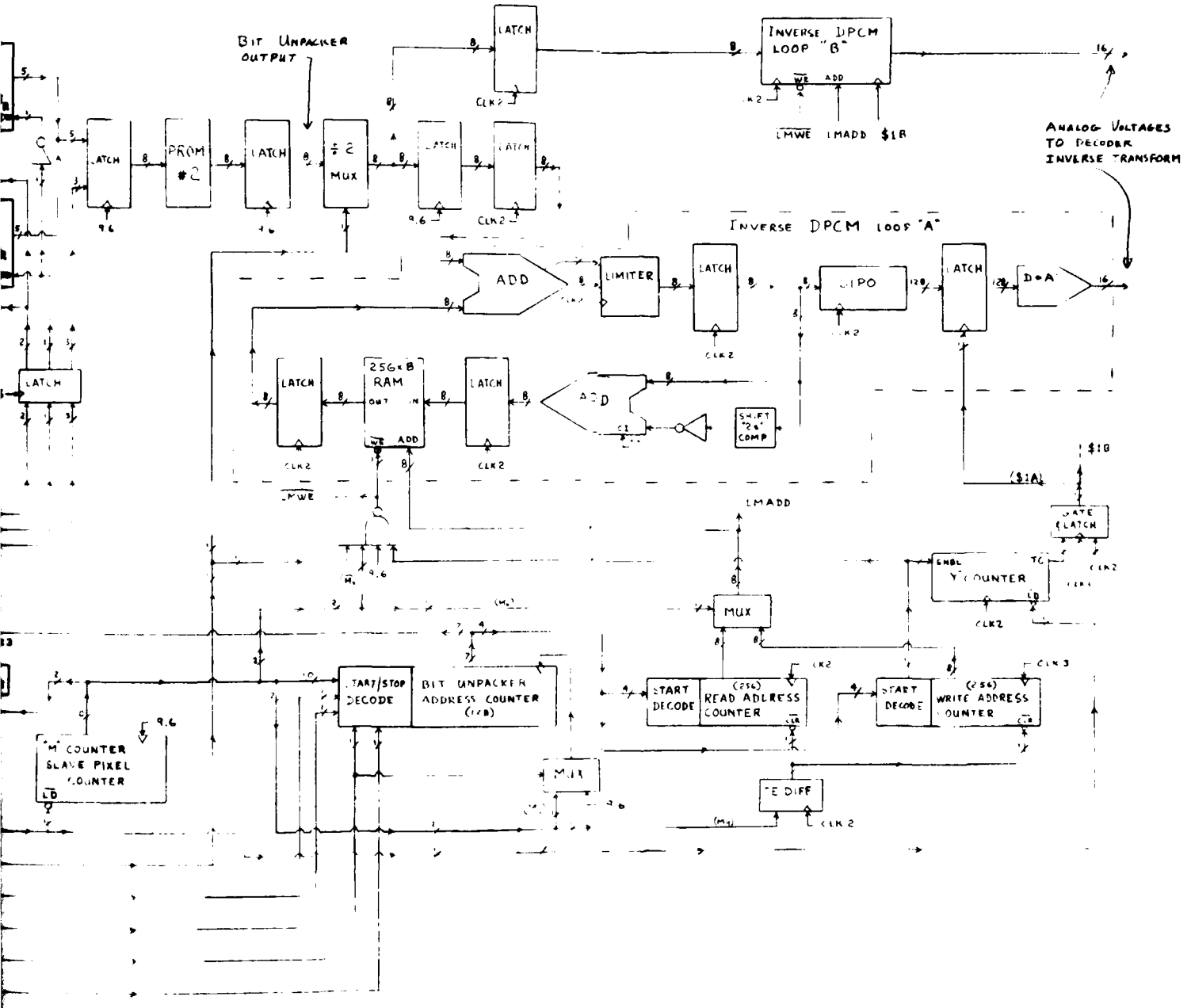


Figure 18. Decoder Bit Unpacker and Inverse DPCM Detailed Block Diagram

output words of the encoder. These 8-bit words are then time multiplexed, 16 to each, to the two inverse DPCM loops whose 16 outputs are D/A converted and presented as analog voltages to the decoder transform module. Operation of the bit unpacker and inverse DPCM loops is similar to that described for the encoder.

The address counter of the bit unpacker is started by a slave pixel counter ("M" counter) which is preloaded at the start of every TV line. When the slave pixel counter reaches terminal count, it starts the address counter of the bit unpacker, which then steps through 32 addresses, thus unpacking 32 8-bit words. The value loaded into the slave pixel counter corresponds to the group delay from the frame store memory of the decoder, through the decoder, to the active horizontal video time of each line. The inverse DPCM read and write address counters are started by decoding the appropriate clock delays from the bit unpacker address counter. Once started, both counters step through 16 addresses and then stop themselves. The address counter of the bit unpacker is started at the terminal count of the slave pixel counter, and every 32 clocks thereafter, for the 512 pixel mode, or every 64 clocks thereafter for the 256 pixel mode, or every 128 clocks thereafter for the 128 pixel mode.

The bit unpacker also requires seven control signals as did the encoder bit packer. These seven control signals perform the same function and are used in the same manner as those previously described for the encoder bit packer. These control signals are stored in the bit unpacker RAM memory which is boot loaded during vertical blanking time of Field No. 1. Picture resolution and bits-per-pixel mode information is supplied to the bit unpacker and inverse DPCM loops via the mode control register located in the frame store memory unit.

Linear line interpolation is performed when in the 120 line mode by dividing the output of the bit unpacker by two every other TV line. Writing into the line memory of the inverse DPCM is inhibited during the line times that the output of the bit unpacker is divided by two.

c. Inverse Transform Processor

The Inverse Transform Processor module (see Figure 19) is divided into four major sections: variable gain input, inverse transform, multiplexer, and output. This module takes the 32 coefficients from the inverse DPCM D/A outputs and generates composite video at the 30-frame-per-second rate required by the monitor.

(1) Variable Gain Input Section

The Variable Gain Input Section contains 32 amplifier circuits. The gains of these amplifiers are switch-selectable to three levels, depending on the resolution mode selected, using HI-201 analog switches. The gains here are the inverse of the gains added in the encoder transform. A typical gain circuit is shown in Figure 20. As before, two of these circuits will be incorporated onto a printed circuit board, thus 16 miniboards are required at the matrix multiplier inputs. The outputs of these amplifiers are an approximation of the transform coefficients obtained at the outputs of the forward transform matrix multipliers before scaling.

(2) Inverse Transform Section

The general mathematical description of the inverse transform is:

$$\hat{X}_i = C^T \hat{F}_K \tag{6}$$

where X_i is the approximation to the original subblock pixels and is obtained by multiplying the transpose matrix of the cosine weights in the forward transform by the reconstructed forward transform coefficients (F_K). In the matrix notation, this is expressed as:

$$\begin{bmatrix} \hat{X}_0 \\ \hat{X}_2 \\ \vdots \\ \hat{X}_{32} \end{bmatrix} = \sqrt{\frac{2}{N}} \begin{bmatrix} 1/\sqrt{2} & C_{1,1} & C_{2,1} & \cdots & C_{31,1} \\ 1/\sqrt{2} & C_{1,2} & C_{2,2} & \cdots & C_{31,2} \\ \vdots & \vdots & \vdots & & \vdots \\ 1/\sqrt{2} & C_{1,32} & C_{2,32} & \cdots & C_{31,32} \end{bmatrix} \begin{bmatrix} \hat{F}_0 \\ \hat{F}_1 \\ \vdots \\ \hat{F}_{31} \end{bmatrix} \tag{7}$$

As in the forward transform, partitioning is required to accommodate the two matrix multiplier devices. This is given by:

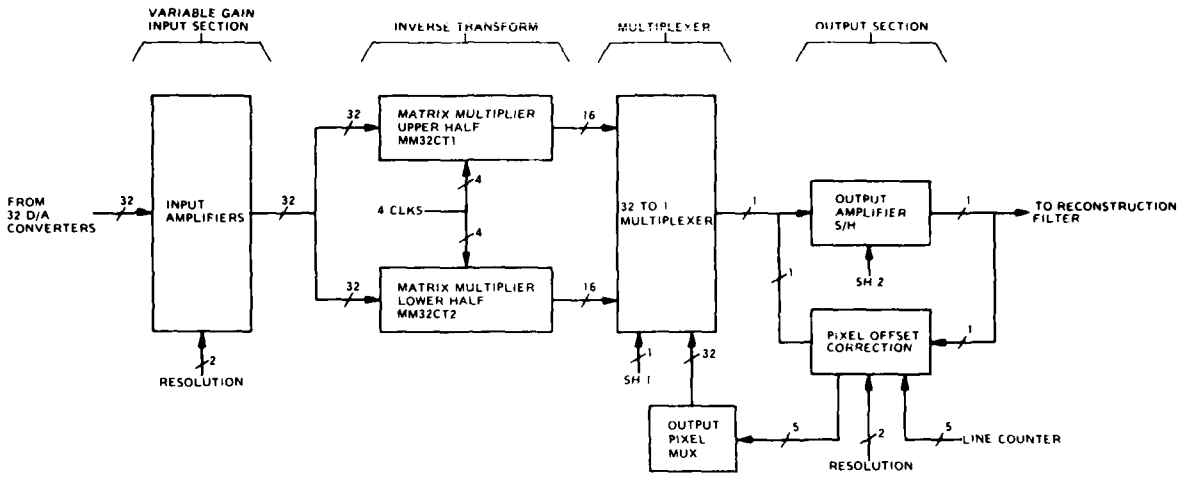


Figure 19. Decoder Transform Block Diagram

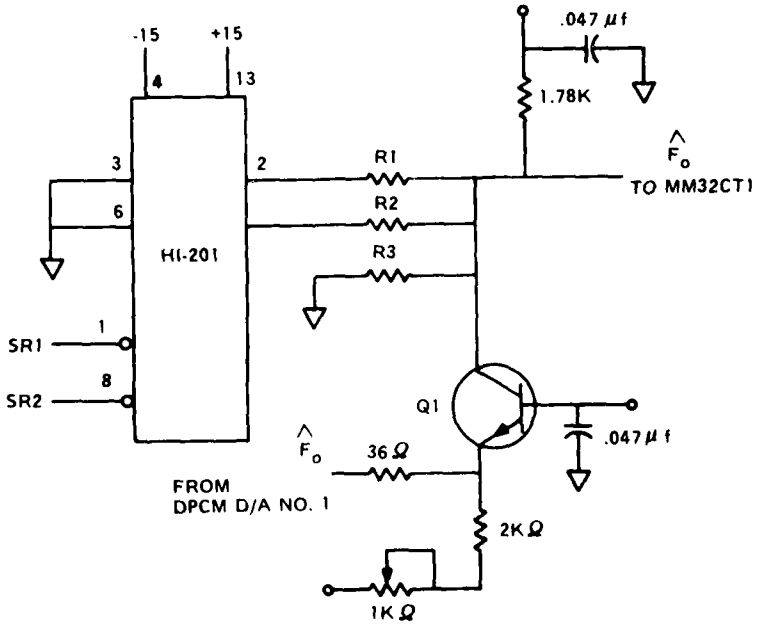


Figure 20. Typical Input Gain Circuit

$$\begin{bmatrix} \hat{X}_1 \\ \vdots \\ \hat{X}_{16} \\ \hline \hat{X}_{17} \\ \vdots \\ \hat{X}_{32} \end{bmatrix} = \begin{bmatrix} \text{MM32CT1} \\ (16 \times 32) \\ \hline \text{MM32CT2} \\ (16 \times 32) \end{bmatrix} \begin{bmatrix} \hat{F}_0 \\ \hat{F}_1 \\ \vdots \\ \hat{F}_{30} \\ \hat{F}_{31} \end{bmatrix} \qquad (8)$$

where MM32C1 contains the upper half of the cosine transpose matrix, and MM32CT2 contains the lower half of the cosine transpose matrix. Figure 21 shows the matrix multiplier configuration used in the decoder. The output values are calculated at a 300, 150 or 75 kHz rate depending on the resolution mode selected in the encoder. This is accomplished by changing the ϕ_1, ϕ_2, ϕ_R and $\overline{\phi}_R$ clock rates keeping the size and relative phasing the same. The matrix multiplier timing is shown in Figure 22.

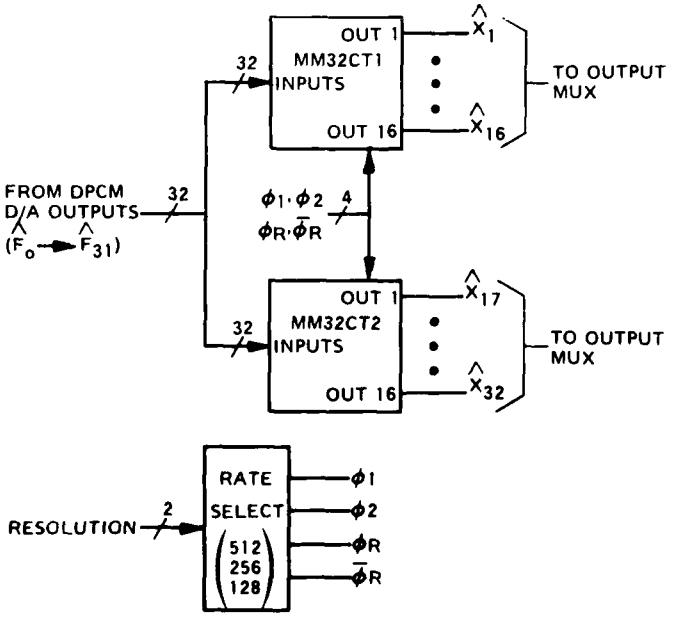


Figure 21. Matrix Multiplier Configuration

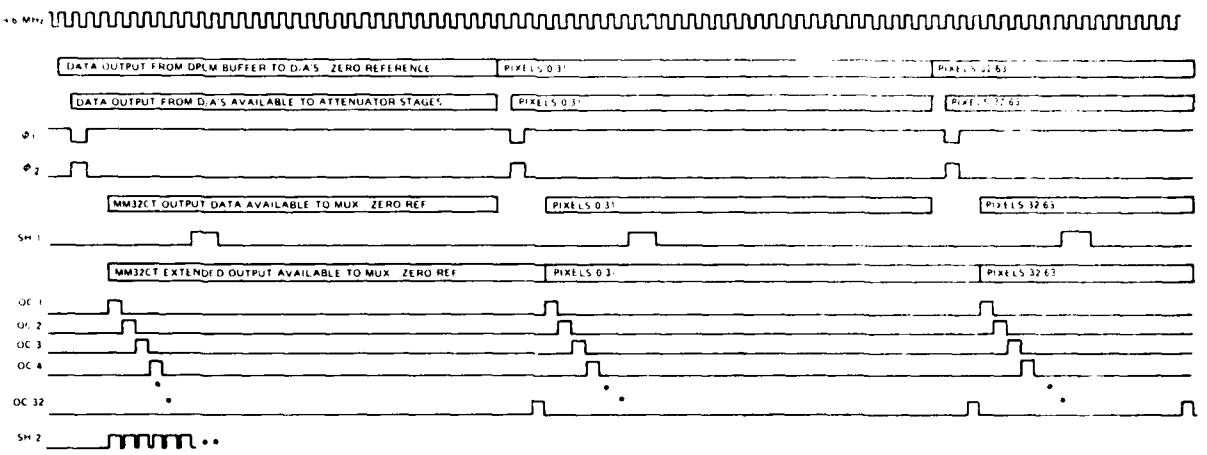


Figure 22. Decoder Master Timing

(3) Multiplexer Section

The purpose of this section is to perform the parallel to serial conversion on the 32 x 1 vector of approximated pixel values (X_i) obtained at the matrix multiplier outputs. Two types of output circuits are required, the first is a simple multiplexer and the second incorporates a sample and hold circuit. These circuits are shown in Figures 23 and 24. The control signals for the multiplexer are TTL levels obtained from the output pixel multiplexer which is run by the RAM address counter.

Owing the D/A and matrix multiplier settling times, there is only time to multiplex 28 pixel values. Thus the sample and hold circuits are required on the last five output lines to extend the time that the outputs are available long enough for the multiplexer to complete its cycle. Multiplexer timing is shown in Figure 22.

(4) Output Section

The Output Section contains the output amplifier, output sample and hold, output buffer, and the bias or offset correction circuitry. The output amplifier, sample and hold, and output buffer are shown in Figure 25. This section runs at 9.6, 4.8 or 2.4 MHz depending on the resolution selected. The sample and hold is used to clean up the multiplexer glitches and the buffer provides the drive to the reconstruction filter.

The offset correction circuitry is shown in Figure 26. This incorporates a comparator, up/down counter, 64 x 9 RAM and a D/A. A comparator at the output of the buffer

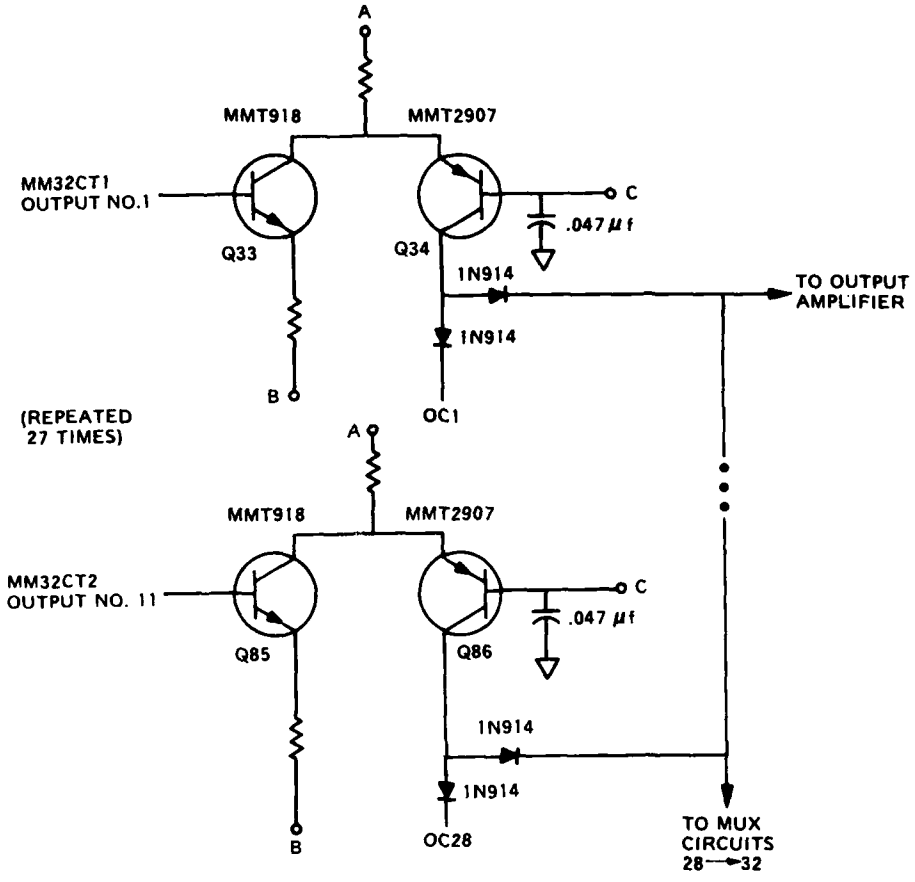


Figure 23. Output Multiplexer Without Sample and Hold

is used to compare the outputs to a ground level. This occurs during horizontal blanking when the reference transform is being processed. As the multiplexer cycles, each output is checked for bias or offset by the comparator. The value of the offset is stored in the RAM. During active time, the RAM is addressed by the pixel counter, and its output is D/A converted and summed into the output amplifier at the proper time to cancel out the offsets. The RAM value is updated each line during horizontal blanking, and the value is held for the active line time. The output is a serial stream of analog data to the reconstruction filter.

d. Video Reconstruction

Video Reconstruction takes place on the composite video output board. The single sampled video input coming from

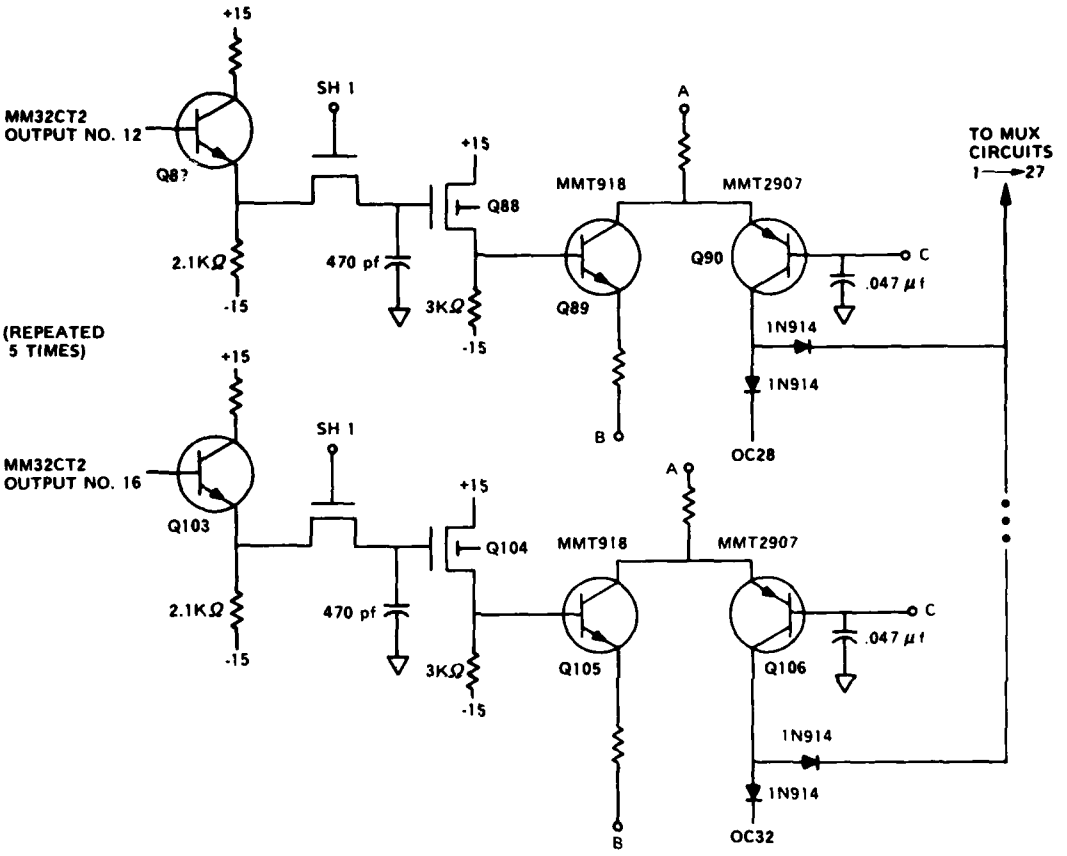


Figure 24. Output Multiplexer With Sample and Hold

the inverse transform board is passed through one of three filters, one for each resolution mode. These filters are automatically selected by the mode control word. The filtered video is mixed with composite sync from the master synchronizer to RS-170 standard levels. This composite video signal is buffered, ac coupled, and becomes the decoder output.

e. Decoder Master Synchronizer

The Decoder Master Synchronizer board (see Figure 27) contains four basic sections. These are:

(a) Master oscillator, clock generation

(b) Pixel sync generation

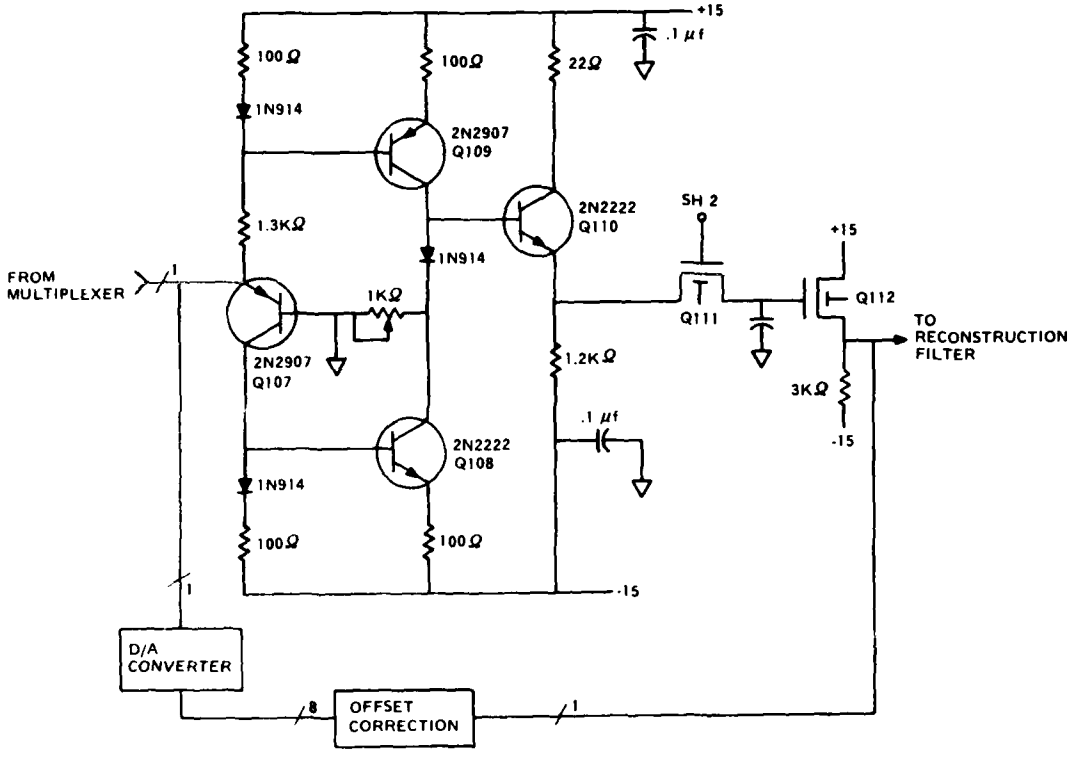


Figure 25. Output Section

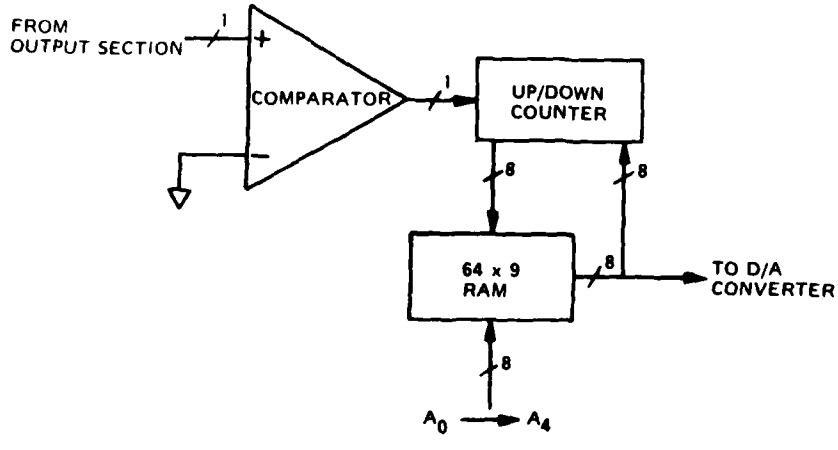


Figure 26. Offset Correction

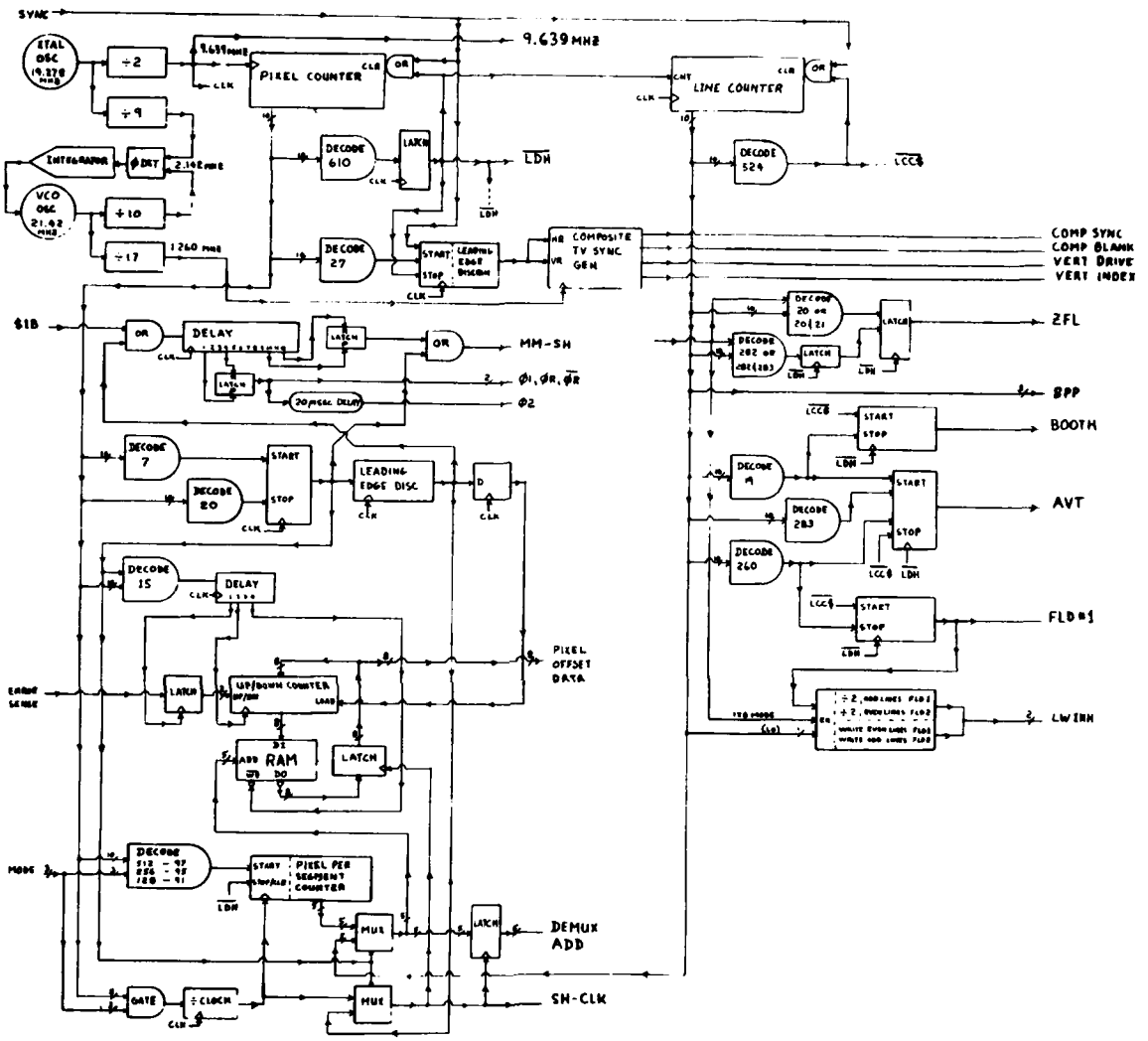


Figure 27. Decoder Master Synchronizer Detailed Block Diagram

(c) Inverse transform sync generation

(d) Line sync generation

(1) Master Oscillator, Clock Generation

The fundamental frequency source for the master synchronizer is a 19.278 MHz crystal oscillator that is divided by 2 to obtain the master 9.639 MHz pixel clock. The 1.260 MHz clock required by the TV composite sync generator is

derived from a 21.42 MHz voltage controlled oscillator (VCO) that is phase locked to the master crystal through divider chains.

Picture sync, coming from the memory synchronizer when the memories exchange places, is used to resync the phased locked loop dividing counters to insure minimum jitter from picture-to-picture.

(2) Pixel Sync Generation

The pixel counter, using the 9.639 MHz clock, counts out 612 pixels per load horizontal ($\overline{LDH}$). $\overline{LDH}$ is a single pixel in length and occurs during the 612th pixel. The pixel address following the trailing edge of $\overline{LDH}$ is all zeros. The first 100 pixel addresses are horizontal blanking time, the remaining 512 are active video.

Picture sync is used to reset the pixel counter which in turn resets the composite TV sync generator. This occurs when the memory buffers exchange.

(3) Inverse Transform Sync Generation

The inverse transform sync generator produces the clocks to operate the inverse cosine matrix multipliers and output demultiplexer. A complete set of these clocks occurs once each segment along a horizontal line. The clock rate, and hence the number of segments along a line, is a function of the resolution.

The pixel-per-segment counter generates a 5-bit address used to demultiplex the parallel video pixels out of the matrix multipliers into a serial video stream. The same address goes to a RAM that contains the digital information necessary to subtract out any pixel-to-pixel offsets from the serial video.

The mode commands select the proper starting decode and clock rate for a given resolution. Line number is substituted for pixel-per-segment count during horizontal blanking time while mid-grey digital values are forced into the matrix multipliers to allow any pixel offsets to be taken out by the offset correction servo loop.

The actual matrix multiplier clocks are generated on tapped delay lines to allow easy adjustment during initial test and evaluation.

(4) Line Sync Generation

The line counter counts out 525 lines per frame. The line counter clear strobe (LCCS) is a line time in

length and occurs for the 525th line. The line address is all zeros following the trailing edge of LCCS. The first 21 lines are vertical blanking and are followed by the 240 active video lines of Field 1. The next 23 lines are vertical blanking again followed by the 240 active video lines of Field 2. A single line at the end of Field 2 is added to the first vertical blanking period to form a total of 22 lines of vertical blanking. This preserves the interlace for a standard TV signal.

Picture sync is used to reset the line counter when the memory buffers exchange. The line sync generates various "housekeeping" signals such as: BOOT, which loads the control RAMs in the slave synchronizer during Field 1 vertical blanking; ZFL to start the inverse DPCM loop off at mid-grey during each field, and LWINH required by the inverse DPCM loop during the 128 resolution mode.

III. SYSTEM EVALUATION

1. Test Results

The test setup of Figure 28 was used to obtain the static test results (Figure 29) for the Video Bandwidth Compression system. A digitized image, stored in the Honeywell 6660 computer, was formatted into a standard RS-170 video image by the Grinnel display generation and recorded on video tape. The output of the video tape recorder was either connected directly to the video monitor to establish the reference image or was used as the video source for the Video Bandwidth Compression system. To provide hard copy, a 35 mm camera was used to photograph the video image displayed on the video monitor. Figure 29(a) shows the reference image while Figures 29(b) through (g) show system performance with the combination of three available resolutions (512, 256, 128) and the extremes of the bits/pixel selections (2 B/P and 0.5 B/P).

Several visual effects are evident in the system output images in addition to increased bandwidth compression. The most noticeable of these is the presence of vertical lines other than those associated with block boundaries. These lines are the result of imperfections in the present circuit implementation. The other visual effect is a loss of contrast in a block when a full-scale black-to-white or white-to-black transition is present in the source video image. When a full-scale transition occurs, the DPCM loop is saturated and the full magnitude of the change is not transmitted to the decoder. The scene statistics were used to set the quantizer levels in the DPCM to determine at which point saturation occurs for each coefficient. To guard against saturation coefficient, gains can be reduced but at the expense of reduced overall image resolution.

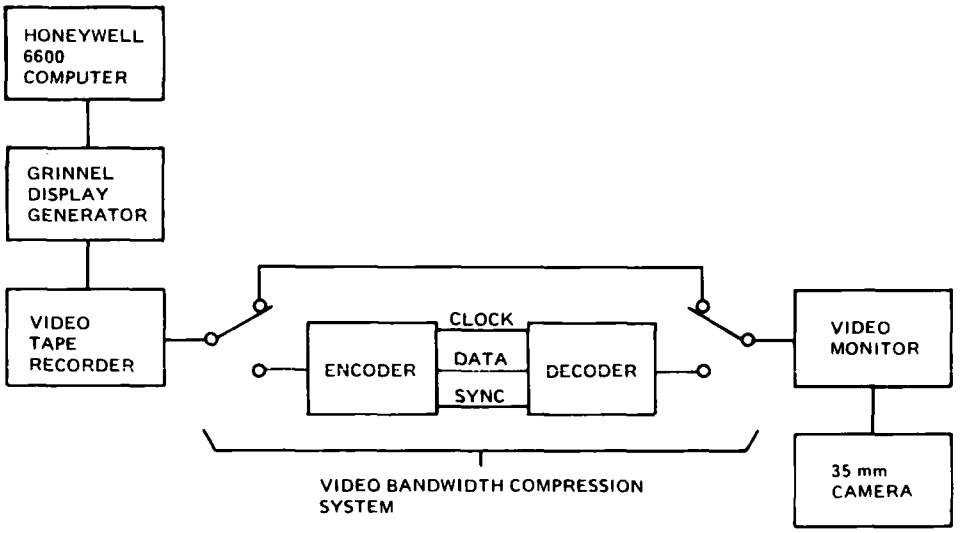
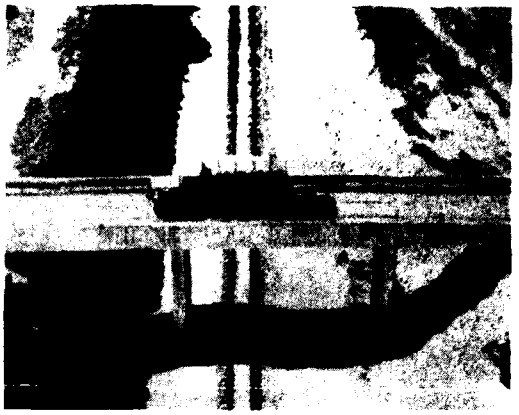


Figure 28. Test Setup

a. Sources of Pattern Noise

The primary source of error in the video output of the bandwidth compression brassband is the presence of vertical lines, which are in addition to the block boundaries produced in normal operation of the 1D/DPCM algorithm. In processing the 1D/DPCM algorithm, any fixed errors which appear in the same position in each horizontal line will be perceived as a vertical stripe. The sources of errors in the brassboard module are a function of the horizontal resolution as shown in Table 1.

In the 512 resolution mode (9.6 MHz sampling rate), the primary source of error in the encoder is the unbalance between the discrete CCD devices and the associated inverting amplifiers. The unbalance in device parameters generates a pattern noise at the input of the matrix multiplier that is carried through the remainder of the system. In the decoder, the signal-to-noise ratio is degraded by low signal output from the matrix multiplier combined with some matrix multiplier clock feedthroughs. In addition, marginal settling times distributed throughout the parallel-to-serial converter and offset correction circuit introduce a noise pattern from pixel-to-pixel. For the 512 resolution mode, the pattern noise contribution in the encoder and decoder are of equal magnitude and are equal to 6 to 8 percent of the full-scale video output.

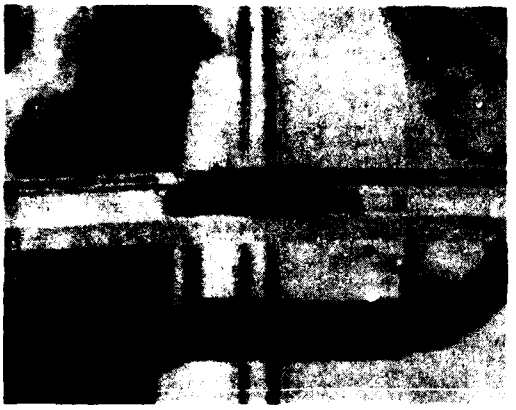


(a) Reference

(b) 512 2 Bit/Pixel

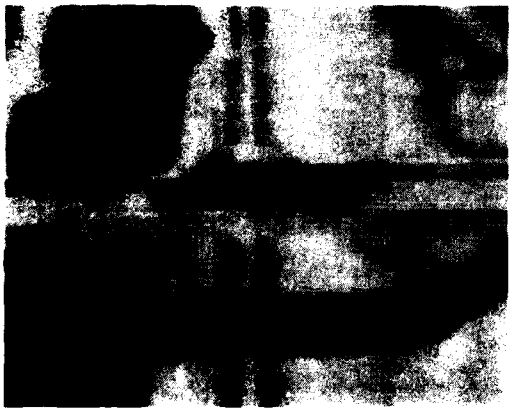
(c) 512 0.5 Bit/Pixel

Figure 29. Test Results (Sheet 1 of 2)



(d) 256 2 Bit/Pixel

(e) 256 0.5 Bit/Pixel



(f) 128 2 Bit/Pixel

(g) 128 0.5 Bit/Pixel

Figure 29. Test Results (Sheet 2 of 2)

TABLE 1. BRASSBOARD NOISE SOURCES

Encoder	
Resolution	Noise Sources
512	• Discrete CCD Devices
256	• Discrete CCD Devices • Rate change on CCD's
128	• Same as 256 mode
Decoder	
Resolution	Noise Sources
512	• Parallel-to-Serial Converter • Low Signal Output from Matrix Multiplier • Matrix Multiplier Clock Feedthrough
256	• Low Signal Output From Matrix Multiplier • Matrix Multiplier Clock Feedthrough
128	• Same as 256 mode

The 256 and 128 resolution modes have the same sources of error. In the encoder, these errors consist not only of parameter variations between charge-coupled device (CCDs) but another source of error is due to the change in clock rate between the reference sample in horizontal blanking (10 MHz sampling rate) and the video sample during the remainder of the horizontal line (5 MHz for 256 resolution or 2.5 MHz for 128 resolution). In the decoder, the primary source of noise is the low signal output from the matrix multiplier coupled with matrix multiplier clock feedthrough since the lower processing rates allow enough settling time for the parallel-to-serial converter and offset correction circuit. For the 256 and 128 resolution modes, the encoder contributes the most noise ($\simeq$10 percent) while the decoder contributes only 4 to 5 percent.

In addition to the errors described previously there is a noise contribution due to gain variations in the parallel-to-serial converter in the decoder. These variations will be most evident on peak black or white signals and are less than 4 percent of full scale.

b. Corrective Measures

The corrective measures being considered for reducing fixed pattern noise in the output video image are listed in Table 2.

TABLE 2. SYSTEM CHANGES TO REDUCE FIXED PATTERN NOISE

• Reduce transform block size from 1 x 32 to 1 x 16
• Incorporate inverse scaling on the inverse transform matrix multiplier
• Keep the sampling rate fixed at 5 MHz

The reduction in block size achieves a reduction in hardware complexity while incurring only a small reduction in system signal-to-noise performance.* In the encoder the benefits are achieved both for the discrete chip version, where the serial-to-parallel and matrix multiplier chips are separate, and the production version where the two functions are combined. In the discrete chip version, the advantage is that the pin count is reduced so that the whole matrix multiplier function can be placed on one chip. This eliminates adjustment between chips and minimizes layout associated noise problems. Also the number of discrete 8-point serial-to-parallel converters required is reduced from 4 to 2 which in turn eliminates the need for inverting amplifiers. When the serial-to-parallel converter and matrix multiplier are combined, the reduction in block size reduces the chip size, which will result in a higher production yield. In the decoder, the reduction in block size again allows the whole matrix multiplier function to be placed on one chip. In addition, the number of input D/A converters and output buffers required is reduced from 32 to 16.

A straightforward solution to the problem of a low signal-to-noise ratio in the decoder is to combine the inverse scaling function, which is performed directly ahead of the inverse transform, along with the inverse transform function on the decoder matrix multiplier chip. The rationale for this approach can be demonstrated with reference to Equation (8)

*AFAL-TR-75-173, "Video Data Compression Study for Remote Sensors"

$$Y(i) = \sum_{i=1}^{N} \sum_{j=1}^{N} \frac{C_{ij} X_j}{\sum_{j=1}^{N} C_{ij}} \quad (8)$$

If the inverse scaling is performed off chip, as is presently done, higher frequency turns of X_j are greatly reduced in amplitude and thus the output signal level Y(i) is greatly reduced in magnitude. If inverse scaling of the DPCM output is done on the chip, then the input X_j will have a larger magnitude. For these larger inputs to have the same relative contribution to the output as before, the respective matrix multiplier top weights C_{ij} must be reduced by the same amount. When the C_{ij} are reduced, the fixed attenuation constant in the denominator:

$$\sum_{j=1}^{N} C_{ij}$$

is reduced and the output level Y(i) will be increased.

Improved system performance can be achieved by running the transform at a fixed rate of 5 MHz. To satisfy the various production system data rates, only the bit packer will be modified. Table 3 shows how three of the data rates currently being used in Phase I brassboard system would be handled in the Phase II flyable model. Simulation results shown in Figures 30 through 33 verify this approach.

TABLE 3. PHASE II EQUIVALENT DATA RATES

Phase I	Phase II
512 at 1 B/P	256 at 2 B/P
256 at 1 B/P	256 at 1 B/P
128 at 1 B/P	256 at 0.5 B/P

The benefits that will result from a constant sampling rate of 5 MHz are that a fixed low-pass filter can be used in the encoder to prevent aliasing (eliminating the need for an integrating sampler) and the parallel-to-serial converter and offset correction circuit in the decoder will have adequate settling time.

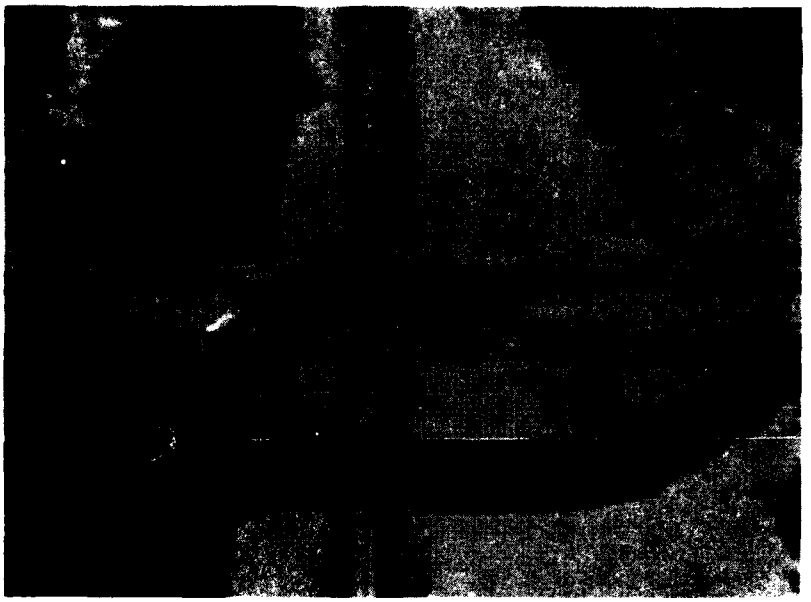


Figure 30. 256 Resolution 1 Bit/Pixel

Figure 31. 512 Resolution 0.5 Bits/Pixel

Figure 32. 128 Resolution 1 Bit/Pixel

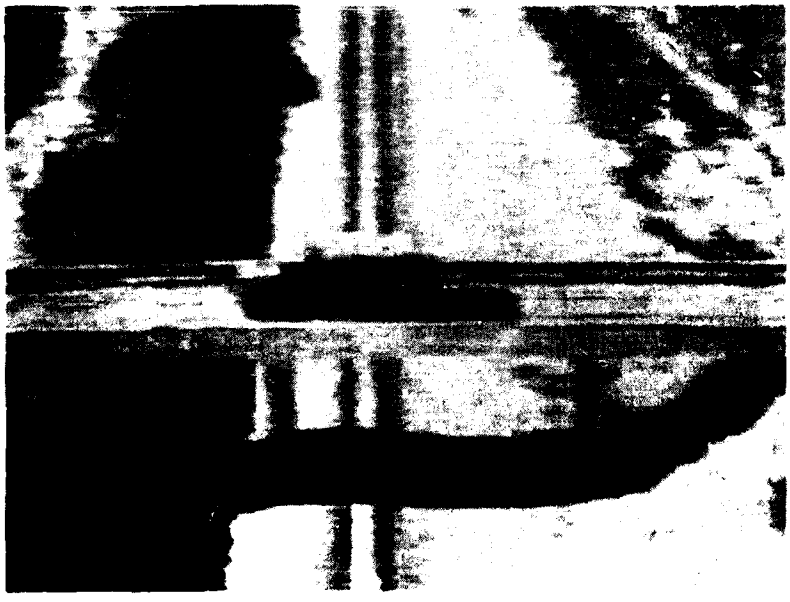


Figure 33. 512 Resolution 0.25 Bits/Pixel

2. Summary

A brassboard model was developed for the Air Force Avionic Laboratory to be used in evaluation of bandwidth compression techniques for tactical weapons. To achieve the flexibility required for a complete evaluation, 60 modes were implemented, which consisted of all combinations of resolution (512, 256, 128), bits per pixel (2.0, 1.5, 1.0, 0.75, 0.5) and frame rate (15, 7-1/2, 1-7/8, 15/32). Real-time system operation was achieved by using CCDs to implement the transform portion of the hybrid coding algorithm. This allows a reduction in frame store size since data is stored in the compressed domain.

System test results show that the variations in image resolution as a function of compression level correspond to results obtained through computer simulation. However, in addition to the gradual loss of resolution due to increased bandwidth compression, fixed pattern noise (10 to 12 percent full scale) is evident in the output image in the form of vertical lines. Recommendations for reductions of this noise include changing the hybrid coding block size from 32 to 16 samples and incorporating the inverse scaling function, located between the inverse DPCM and inverse transform, on the decoder matrix multiplier chips.

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