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CAPLESS ANNEALING OF ION IMPLANTED GaAs

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1 September 1978 through August 1980,

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A capless "powder annealing technique" (PAT) is described and is shown to enable reproducible annealing of ion implanted GaAs without the need of a protective cap. This method employs finely powdered graphite as the annealing medium with a layer of finely crushed GaAs beneath it providing an As-rich environment which prevents the GaAs substrate from decomposing at typical annealing temperatures of 850°C. Using rf spark-source mass spectrometry, an As concentration in excess of the equilibrium value of As over GaAs at the annealing

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temperature is found in the post-process powder. The crushed GaAs layer is essential in providing this high As concentration.

Using this annealing technique, the high resistivity of semi-insulating GaAs substrates is preserved throughout the high temperature treatment. Photo-luminescence measurements at 77K indicate the presence of an As vacancy complex through the existence of an emission band centered near 1.4eV. This, however, does not appear to affect the resistivity of the substrates. On the other hand, analysis of the surface layers of substrates using secondary ion mas spectro-scopy (SIMS), reveals a correlation between the degradation in resistivity of some substrates and presence of Mg. Mass spectrometry measurements reveal a considerable amount of Mg in the as-received graphite powder, although its concentration decreases after the powder is used in PAT processes. The purity of the graphite powder is thus a critical factor in PAT annealing.

Comparison of doping profiles in Se and S ion implanted GaAs annealed with PAT and with dielectric capping show that the capped ones consistently exhibit wider doping profiles. Using LSS parameters, the effective diffusion coeffi-cients for the two annealing techniques are deduced, and a diffusion enhancement in capped annealing of a factor of two is obtained. Using SIMS, the Cr profiles near the surface of the substrates have also been studied for the two annealing methods and a similar enhancement in Cr diffusion is observed for the dielectri-cally capped material. These difference in diffusion of impurities during the annealing cycle is attributed to the strain induced by the dielectric cap, an effect absent in the capless PAT process. Using Al_2O_3 backside caps, the dif-fusion is shown to increase with the applied strain. The diffusion coefficient deduced for zero strain agrees with the results of capless annealing.

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1.0 INTRODUCTION

Ion implantation has become an important technology for fabricating GaAs devices. A wide range of doping can be obtained with excellent control of carrier concentration and profile depth. Microwave devices such as field effect transistors (FETs) with state of the art performance have been fabricated using ion implantation. In addition, the ability to dope selected areas of a substrate has made possible a complete planar process in GaAs integrated circuits. Full development of ion implantation and associated processing technology is important to realize the potential of GaAs devices.

A necessary processing step associated with ion implantation is the activation of implanted atoms and the removal of damage produced by the irradiation. This usually involves annealing the substrates at temperatures approaching 900°C. Unprotected GaAs tends to dissociate and lose As at temperatures above 600°C. To prevent this from occurring a dielectric cap such as silicon nitride is usually employed. This additional processing step is, however, not always desirable. In addition to occasional failure of the cap to adhere to the substrate, the mechanical strain induced at the cap-substrate boundary can lead to enhanced diffusion of dopants during the thermal cycle, and the activation of implanted atoms is often dependent on the choice of capping material and method of deposition. A capless method of annealing ion implanted GaAs is therefore desirable both as a practical processing technology and as a useful tool for studying phenomena associated with ion implantation.

This report summarizes the results of a two year detailed study of capless annealing of GaAs. The most important requirement for such a scheme is a stable As-rich environment. In the present approach this is provided by a powdered graphite medium which retains the As emitted from a crushed GaAs source. Compatibility with ion implantation device fabrication requires high thermal stability of semi-insulating substrates and good activation of implanted dopants. Results obtained here indicate that such qualities are consistently obtained with the powder annealing technique. It has been observed that the diffusion of impurities is enhanced when a dielectric cap is used during annealing. A probable cause of this enhancement is the strain induced by the Si_3N_4 front side cap. Results of experiments using Al_2O_3 backside caps to simulate the strain show a definite increase in diffusion with strain. The diffusion deduced for zero strain agrees with the results of capless annealing.

2.0 THE POWDER ANNEALING TECHNIQUE

The powder annealing technique[1] (PAT) which uses finely powdered graphite and crushed GaAs source to provide a stable As-rich environment for the GaAs substrates during the high temperature annealing is described in this section. A review of the experimental procedure is presented in Section 2.1. A model of excess As in the annealing medium as the mechanism of protection to the GaAs substrate is described in Section 2.2. Results of analysis of the contents of the graphite powder is also given. The important role of the crushed GaAs layer as the source of As is demonstrated in Section 2.3.

2.1   Experimental Procedure

The powder annealing technique investigated under this program is best described by reference to Fig. 2-1. The assembly for holding the annealing medium and the substrate consists of a boat made of high purity graphite. The bottom of the boat is first lined with a layer of finely crushed GaAs. This is followed by a layer of finely powdered graphite (the annealing medium). The substrate to be annealed is placed facing the graphite powder, and the annealing is performed in a tube furnace under a reducing atmosphere of palladium purified hydrogen, as illustrated in Fig. 2-2.

Before any annealing is attempted, a newly prepared medium must first be suitably conditioned. The method used here is as follows. The assembly, without any substrate, is first baked at a relatively low temperature of

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GaAs SAMPLE ⎯⎯⎯→ ⎯ H$_2$ ⎯

POWDERED GRAPHITE

CRUSHED GaAs

⎯ HIGH PURITY GRAPHITE BOAT
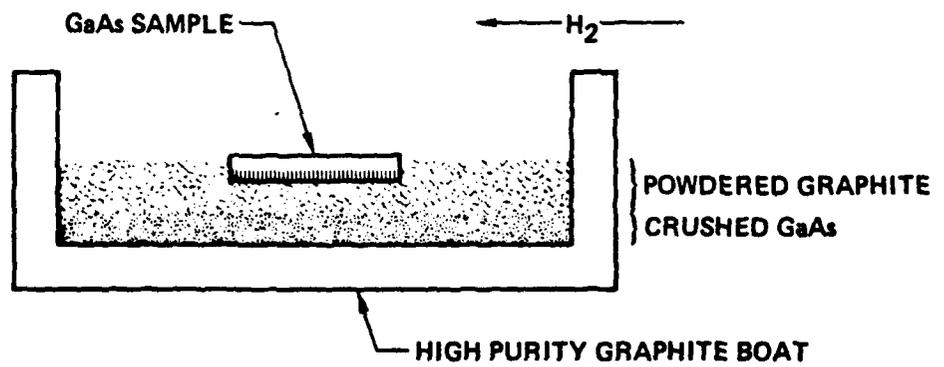
**ESSENTIAL ELEMENTS OF THE POWDER
ANNEALING TECHNIQUE (PAT)**

Fig. 2-1   Essential elements of the powder annealing technique (PAT).

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EXHAUST ↑   ↓ UHP H₂

GRAPHITE BOAT

TO VACUUM PUMP
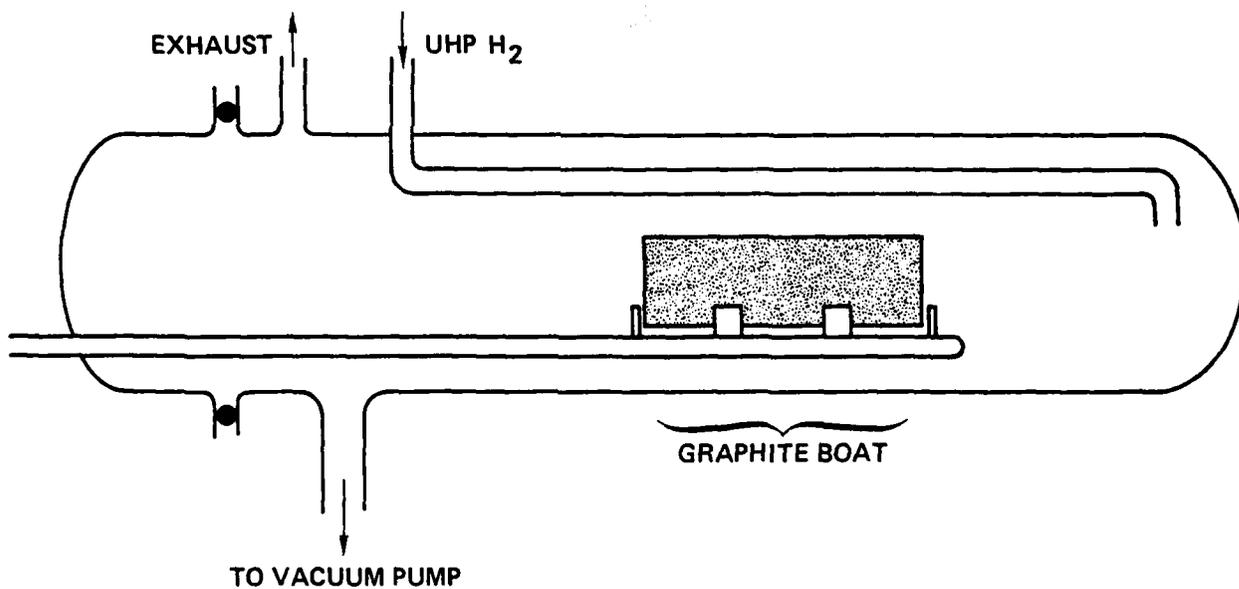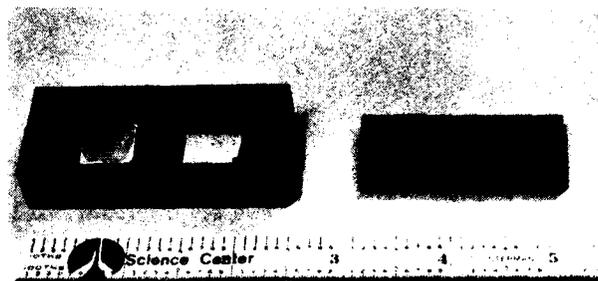
Fig. 2-2 Apparatus used for capless annealing of ion implanted GaAs.

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approximately 200°C under vacuum to drive out adsorbed moisture, oxygen, and volatile impurities. It is then heated in hydrogen to the temperature used in annealing. It has been found that this arrangement and conditioning procedure provide satisfactory performance in subsequent capless annealing.

2.2   Excess As in Powdered Graphite Layer

Since a bare GaAs substrate decomposes and loses As at the high annealing temperatures, any annealing procedure owes its success to proper protection of the surface. In a capless annealing method, this can be achieved by an excess of As close to the surface. In this case a considerable amount of As must be present in the powdered graphite layer. Moreover, the concentration of As must be in excess of that corresponding to As in equilibrium over GaAs. It is proposed that in the conditioning procedure, the crushed GaAs decomposes due to the high temperature. The emitted As is adsorbed by the powdered graphite layer which has a large surface area due to the small particle size. A steady-state situation can be reached, and since the As does not occur in a free state, a stable concentration can be maintained without elaborate arrangements to control the source of excess As. This is reflected by the observation that once an annealing medium is properly conditioned, subsequent reconditioning is unnecessary.

A test has been made to confirm the presence of As in the powdered graphite layer. Samples of the powder, both before and after being used, have been analyzed for As content. Since crushed GaAs is used in the process, it is anticipated that this cannot be completely separated from the powdered

graphite sample, and measurement of Ga content is made in order to rule out any erroneous As result due to residual GaAs particles. The analyses also provide a chance to evaluate the commercially available graphite powder for possible adverse effects due to impurities.

The analysis using R.F. spark-source mass spectrometry was performed by Technology of Materials, Inc., 2030 Alameda Padre Serra, Santa Barbara, California 93103. The results, given in their report number 971140, are summarized in Table 2-1. Sample B is as-received powdered graphite, and sample C has been used in PAT processes. The two most interesting elements are of course Ga and As. In the "before" sample, Ga is not detected above the uncertainty level, while no As is found down to the detection limit. In the "after" sample, however, both Ga and As are detected in appreciable quantity. The amount of Ga is found to be 260 parts per million (ppm) by weight, while As is present in a high concentration of 2000 ppm. Obviously this amount of As cannot be accounted for by the GaAs remaining in the sample. It is also clear, by looking at the much lower concentration of other elements present besides C, that this As must be present in an elemental form, although it is likely that it has been adsorbed by the graphite.

A simple calculation reveals how this concentration of As compares with the equilibrium value of As over GaAs. The powdered graphite has a density of roughly 0.12 gm/cm^3 as received. From the measurements, the net As concentration after PAT processing is 1740 ppm. Assuming that the As exists

TABLE 2-1

IMPURITY CONCENTRATIONS IN GRAPHITE POWDERS
(in parts per million by weight)

Sample B

Element	Detection Limit	Graphite Powder
C	.01	Major
B	.001	1.3
N	.3	5.4
O	.1	3.6
Mg	.05	310
Si	.1	4.9
S	.1	2.3
Ti	.1	0.55
F	.01	<85
Na	.05	<3.5
Al	.1	<4.5
K	.1	<1.8
Ca	.05	<0.86
Cr	.1	<3.2
Fe	.1	<2.7
Ni	.1	<5.7
Ga	.05	<18
In	.05	<27

Sample C

Element	Detection Limit	Graphite Powder
C	.01	Major
N	.3	0.88
O	.1	2.6
Mg	.05	1.9
Si	.1	1.5
S	.1	0.41
Ga	.05	260
As	.05	2000
B	.001	<0.25
F	.01	<2.7
Na	.05	<0.65
Al	.1	<1.7
K	.1	<0.16
Ca	.05	<0.10
Ti	.1	<0.61
Cr	.1	<0.19
Fe	.1	<0.76
Ni	.1	<1.3
In	.05	<0.84

No hydrogen determination was made.
Gold and tantalum were not reported as gold foil and
tantalum slits were used in the analysis
The elements given in the lower half as upper limits are
limited due to either interference or residuals.

mainly in the form of As_2, which is the dominant form at the temperature of 850°C used in annealing, the volume concentration of As is about 8.4 x $10^{17}/cm^3$. One atmosphere at 850°C corresponds to 6.5 x $10^{18}/cm^3$. Reported values of vapor pressure of As_2 over GaAs at 850°C are about 10^{-6} atm.[2] If the surface of the substrate remains in close contact with the conditioned graphite powder, it is in effect inside a considerably As rich environment. Loss of As by the substrate can therefore be prevented. In actual usage the graphite powder is compacted by a factor of the order of 10, and the effective concentration of As is further increased.

Of the other elements present, most are negligible except Mg. Since Mg is electrically active in GaAs, this can cause a conducting layer at the surface. The origin of Mg in as-received powdered graphite is believed to be contamination from the tools used in commercial processing. The distribution of Mg near the substrate surface has been studied by SIMS and is described in in Section 3.4. Process improvements to eliminate possible problems arising from the Mg present in the graphite powder have been instituted and are also described in that section.

2.3   Crushed GaAs Layer as Effective Source of As

In the powder annealing technique, two arrangements of supplying As to the graphite powder using GaAs are possible. A piece of "source" GaAs substrate can be placed beneath the powdered graphite layer, as illustrated in Fig. 2-3(a). This results in a roughly symmetric situation. The boundary between the "source" substrate and the powder is an abrupt plane. The concen-

tration of As near this boundary is given by the equilibrium of As over GaAs, and serves as the source for the diffusion into other parts of the powder layer. The concentration of As elsewhere in the layer is therefore lower than the equilibrium value. Loss of As by the substrate to be annealed and placed at the top of the powder is inevitable, and reproducibility is expected to be poor.

Another arrangement, routinely used in PAT, is illustrated in Fig. 2-3(b). Here, a layer of finely crushed GaAs is used as the source of As. The small particle size offers significant increase in surface area per unit volume. Left alone, the equilibrium concentration of As remains unchanged. When the powdered graphite is laid on top of the crushed GaAs, a gradual transition occurs between the two layers. The effective concentration of As, as seen by the graphite powder, is vastly increased because of the increase in surface area per unit cross-section of boundary. It is therefore possible to produce a concentration of As near the top substrate which is above the equilibrium value over GaAs.

An experiment comparing the two arrangements of As source has been carried out. Semi-insulating substrates from an ingot suitable for PAT have been treated under the same thermal cycle. In the usual arrangement of crushed GaAs, high resistivity is preserved following the heat treatment, indicating the effectiveness of PAT in protecting the substrate. Using a GaAs substrate as the As source, however, all the samples show an appreciable drop in resistivity, and degradation in surface quality is apparent. This comparison, therefore, serves to support the arguments presented here on the role of the crushed GaAs layer as an effective source of excess As.

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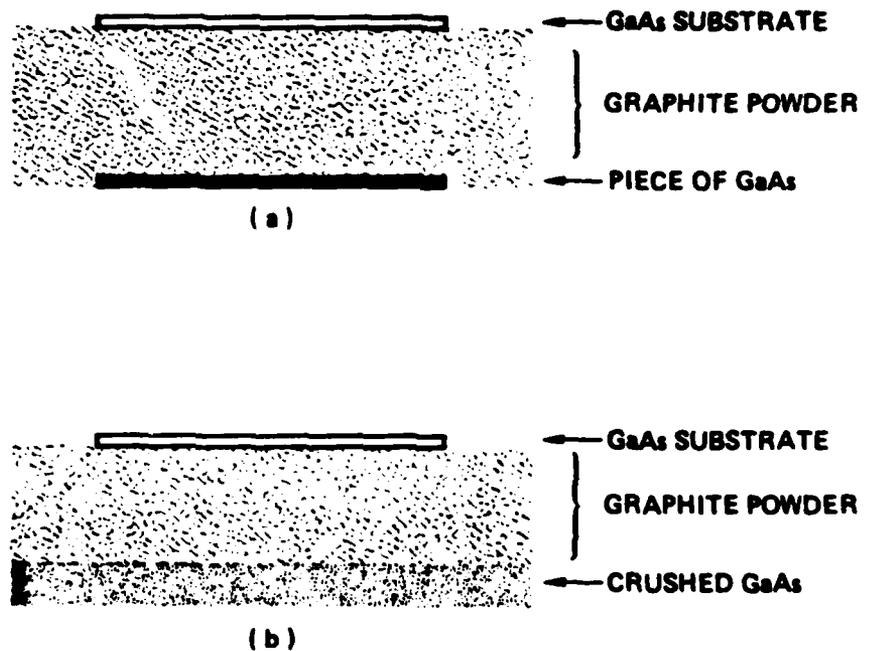
Fig. 2-3   Arrangement of annealing media with underlying layers of
(a) a piece of GaAs substrate, and (b) crushed GaAs.

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3.0 COMPARISON OF PAT AND CAPPED ANNEALING PROCESSES

3.1 Thermal Stability of Semi-insulating GaAs

The effectiveness of the PAT process in providing protection to the substrate surface during the high temperature annealing is demonstrated by its ability to prevent thermal conversion of selected GaAs ingots. To facilitate comparison with the results obtained using capping for annealing, ingots that have previously been qualified for ion implantation were chosen. Samples of un-implanted semi-insulating substrates from these ingots were annealed using the PAT process. Gold-germanium contacts were deposited and alloyed, and van der Pauw - type patterns were defined on these samples. The sheet resistance of the samples was then determined by a four-point measurement using a pico-ammeter and an electrometer. The results of unannealed and PAT processed samples, together with results of previous qualification tests are given in Table 3-1. The qualification criterion for GaAs ingots suitable for ion implantation is $R_s > 10^6 \Omega/\square$ after capped annealing.

It is observed that degradation in resistivity occurs in some substrates following PAT annealing. In order to understand this difference among ingots, these substrates have been studied using photoluminescence (PL) for defects and shallow impurities, photo-induced transient spectroscopy (PITS) for deep levels, and secondary ion mass spectroscopy (SIMS) for the

TABLE 3-1

Sheet resistivity of unannealed and annealed Cr doped GaAs obtained
by four-point measurement using a van der Pauw pattern.

| Ingot Number | Unannealed | Sheet Resistance, $\Omega/\square$ | |
		Si_3N_4 CAP Qualification	PAT
XS3608	2.1×10^9	$>10^6$ (f, t) $>10^8*$	8.4×10^7
XS3737	6.8×10^9	$>10^7$ (f, t)	4.1×10^5
XS3805	7.5×10^9	$>10^8$ (f) $>10^7$ (t)	1.2×10^5
XS3809	7.8×10^9	$>10^7$ (f, t)	3.0×10^5

All qualification results were obtained after Kr bombardment except *
which was thermal annealed, f, t refer to the front and tail portions of
the ingots, respectively.

chemical nature of the surface layer. These are described in Sections 3.2,
3.3 and 3.4. As discussed in Section 2.2, the impurities, notably Mg, in the
graphite powder can cause the observed thermal conversion. Correlations among
these measurements are discussed in Section 3.4.1. Process improvements have
been implemented according to the findings, and the effects are also given in
that section.

3.2   Defect Studies with Photoluminescence (PL)

In order to study the observed difference among the ingots, we have taken photoluminescense (PL) measurements at 77K on substrates annealed with silicon nitride capping and with PAT. In the PAT processed samples, weak emissions centered around 1.36 eV and 1.4 eV are observed in additional to the bandgap emission at 1.5 eV as shown in Fig. 3-1. Such bands are not observed in capped annealed samples. The 1.36 eV band has been attributed to Cu impurities on Ga sites,[3] while the 1.4 eV band is believed to be associated with As vacancy complexes.[4] The ratio of intensities of the 1.4 eV to bandgap peaks given in Table 3-2 varies from 4.7×10^{-2} for a XS3737 sample to 1.9×10^{-2} for XS3608. While there is a trend, as expected, for the qualified ingot to exhibit weaker emission following annealing, the difference in intensity among the samples can account for the significant difference in the apparent thermal stability of semi-insulating property, since the As vacancies in the sample C 26 of ingot XS3608 apparently do not affect its semi-insulating property.

TABLE 3-2

Relative peak intensity of the 1.4eV photoluminescence
band in PAT annealed GaAs

Ingot Number	Anneal Number	1.4 eV Peak Relative to Bandgap Peak (%)
XS3608	C26	1.9
XS3737	C26	4.7
XS3805	C25	4.3
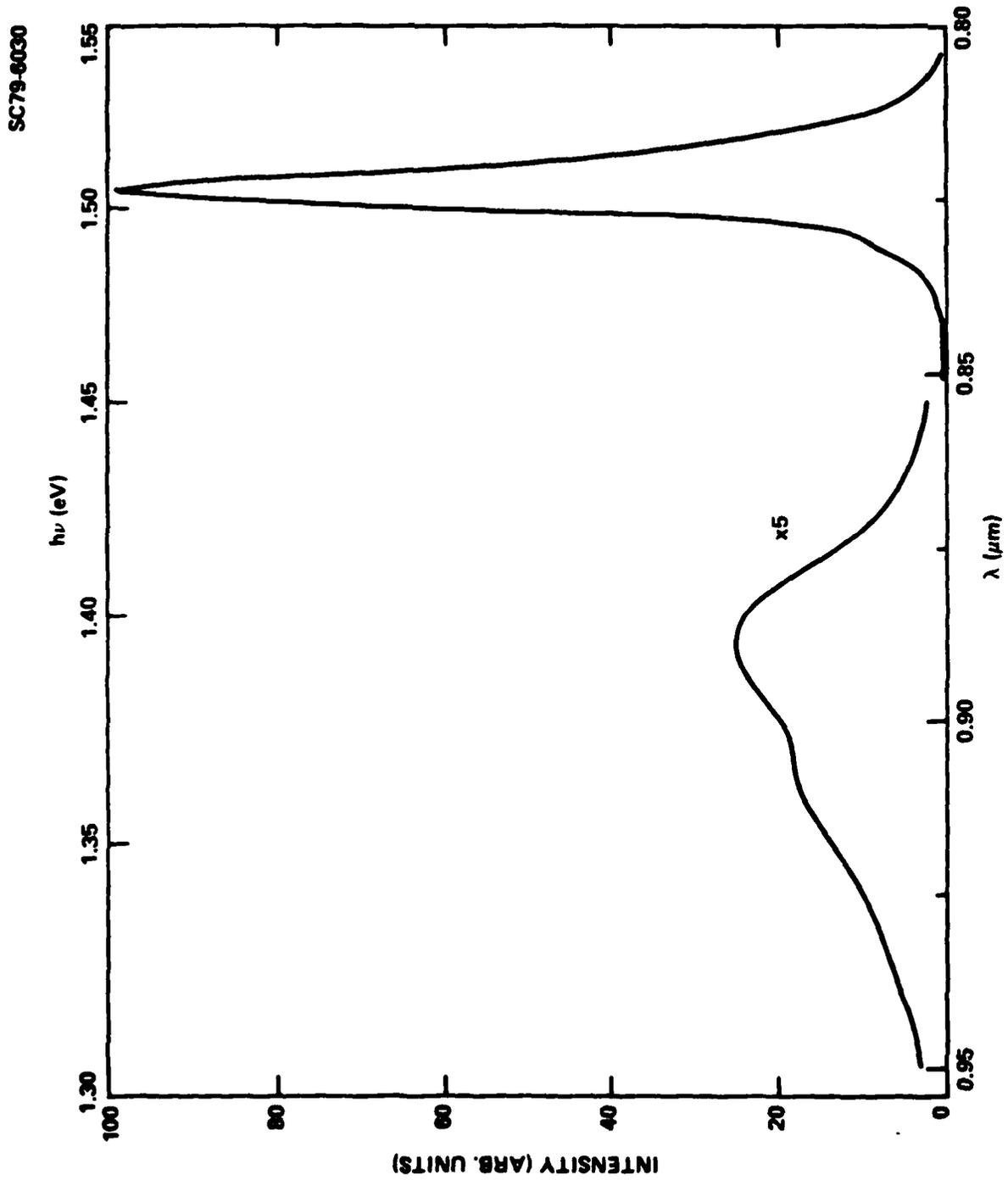
Fig. 3-1 Photoluminescence (PL) spectrum at liquid nitrogen temperature of sample C26-2, a PAT annealed substrate from ingot XS3737.

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3.3   Deep Level Studies With Photo Induced Transient Spectroscopy (PITS)

A brief survey of deep levels in PAT processed GaAs substrates has
been undertaken. The purpose of this study is to discover major differences
among capped and capless annealed samples as well as ingots that behave
differently in qualification tests. The study is conducted using photo-
induced transient spectroscopy (PITS). PITS is a transport technique which
detects the transient rise or decay of the sample photocurrent during chopped
illumination. A typical PITS spectrum is obtained by sampling either the
photo current rise (R-PITS) or decay (D-PITS) at two points in time, with the
difference $\Delta I = [I(t_1)-I(t_2)]$ recorded continuously as a function of temper-
ature. Any peaks observed in the spectrum will correspond to trap emission
rate e_t which is directly proportional to the sampling rate $\Delta t^{-1} = (t_2 - t_1)^{-1}$. Successive temperature scans at different sampling rates can therefore
determine both the trap energy and capture cross section, assuming a single-
exponential rise or decay. The magnitude of a particular PITS peak is a
function of the trap emission rate and the degree of trap filling under the
simplified assumptions of complete trap filling and a single time constant
exponential decay, the magnitude of the free carrier concentration is given by

$$\Delta n(t) = n_t e_t \tau \exp[-e_t t]$$

where n is the trap concentration and τ is the free-carrier lifetime. In some
instances, however, a transient signal "inversion' can take place; this
corresponds to a transient overshoot in the case of R-PITS and undershoot for
D-PITS. Such an "inversion" is possible in the case of a shallow trap and a

deep recombination center where the trap cross section S_t is much smaller than the recombination center cross section S_r.[5]

The PITS spectra of several samples of unannealed and capped and capless annealed substrates from different GaAs ingots has been obtained with a sampling time of 3mS. Figure 3-2 illustrates the normalized PITS spectra of a capped annealed and a capless annealed sample from the same ingot. No significant difference in traps is observed. Figure 3-3 illustrates the spectra of two capless annealed samples from different ingots. Some difference is noted and an inversion is observed in one sample. The same features are however also observed in an unannealed sample of this ingot, as illustrated in Fig. 3-4. From the general survey of these PITS spectra it can be concluded that the capless PAT process does not introduce particular changes in the trap distribution of the GaAs material. It can therefore be utilized in connection with analytical tools such as PITS in material characterization studies where the dielectric cap can be undesirable.

3.4   Surface Layer Studies With Secondary Ion Mass Spectroscopy (SIMS)

3.4.1   Mg Impurities in Graphite Powder

A possible reason for the deterioration in the substrate following annealing with PAT is contamination by impurities in the graphite powder. As shown in Sec. 2.2, the as-received graphite powder contains a considerable amount of Mg which decreases significantly after several PAT processings. It is very probable, then, that this Mg has diffused into the substrate and

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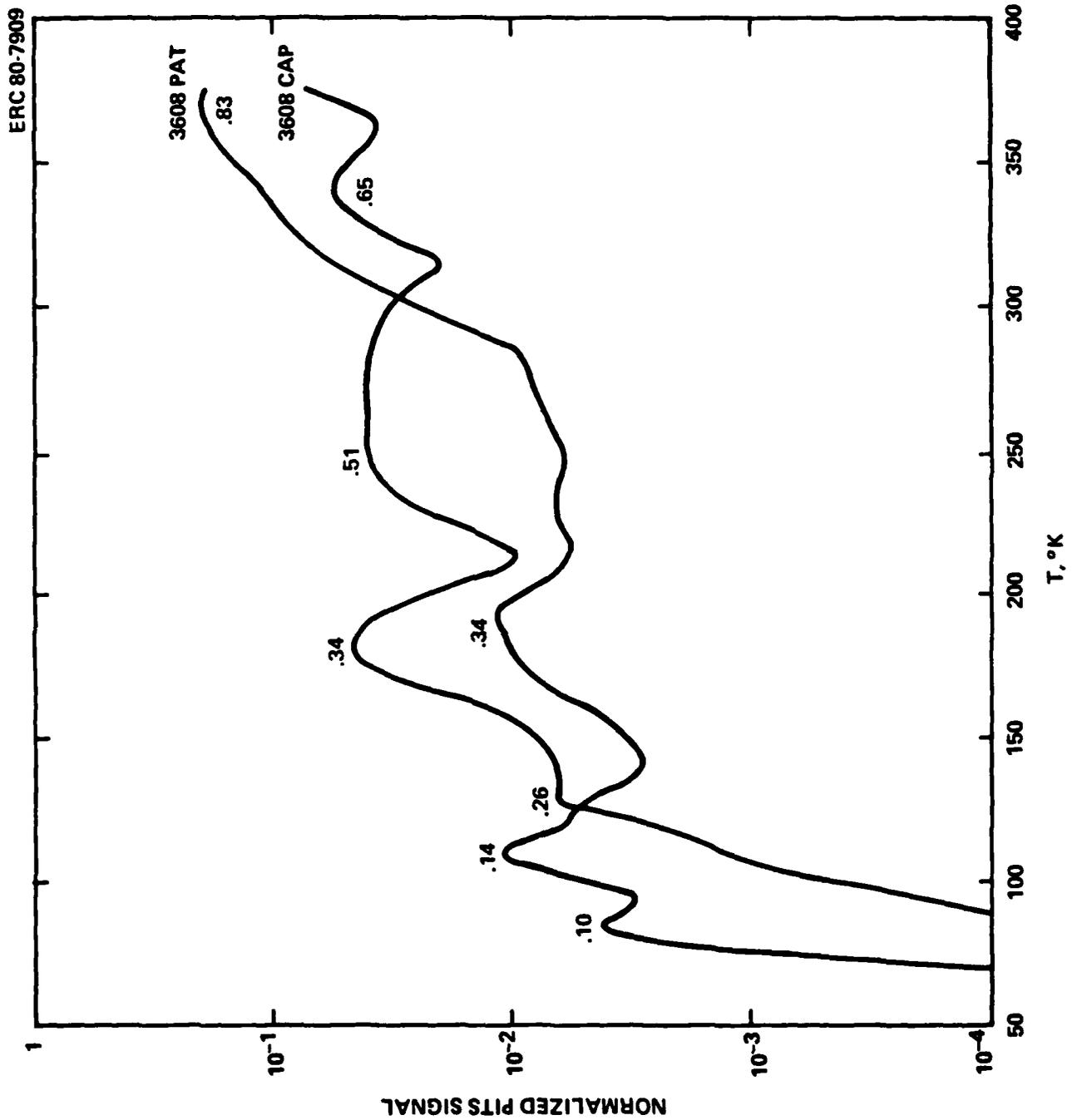
Fig. 3-2 3-msec normalized PITS spectra of capped and PAT annealed GaAs, ingot No. 3608.

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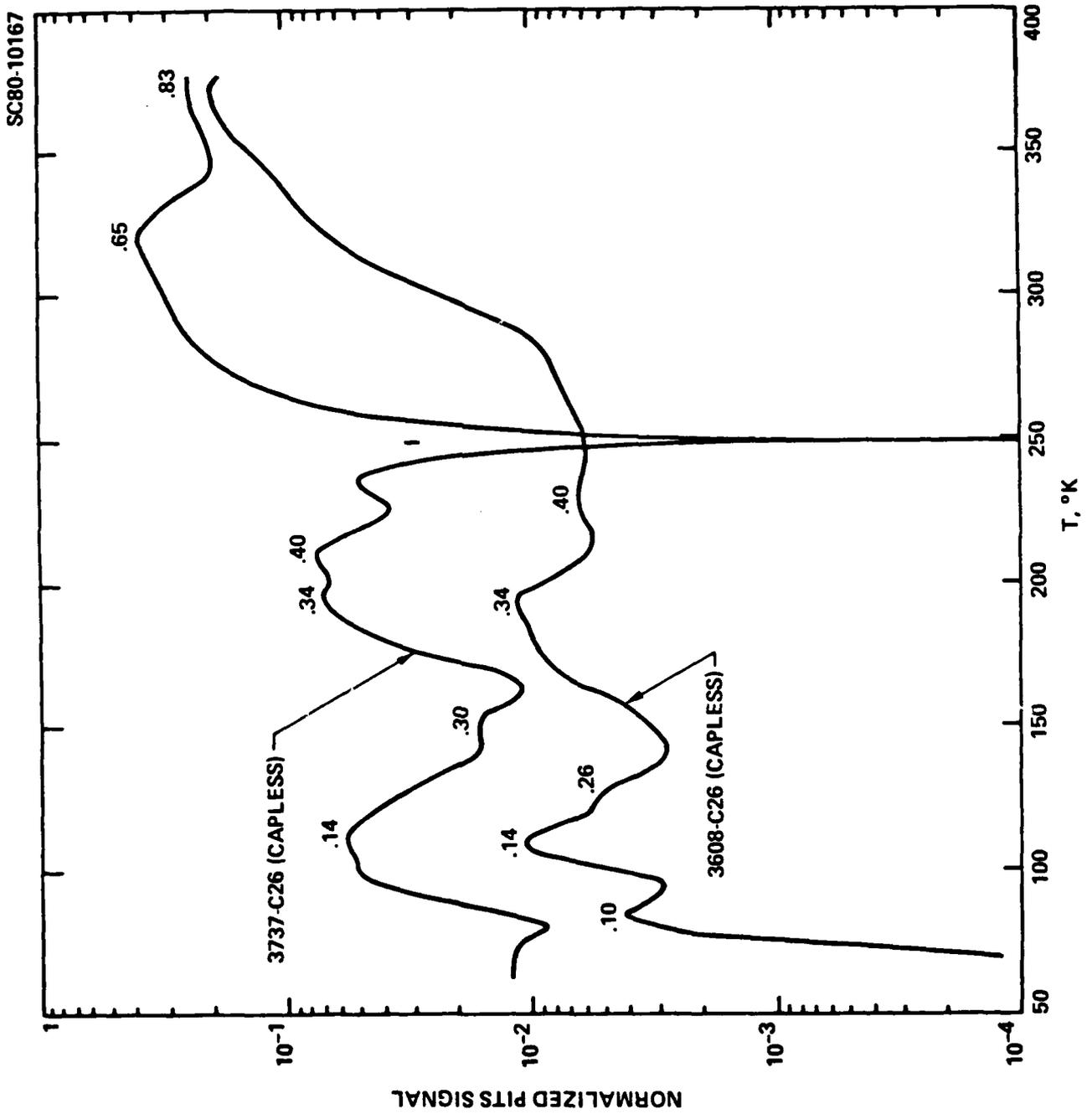
Fig. 3-3 PITS spectra of PAT annealed GaAs, Ingot No. 3608 and 3737.

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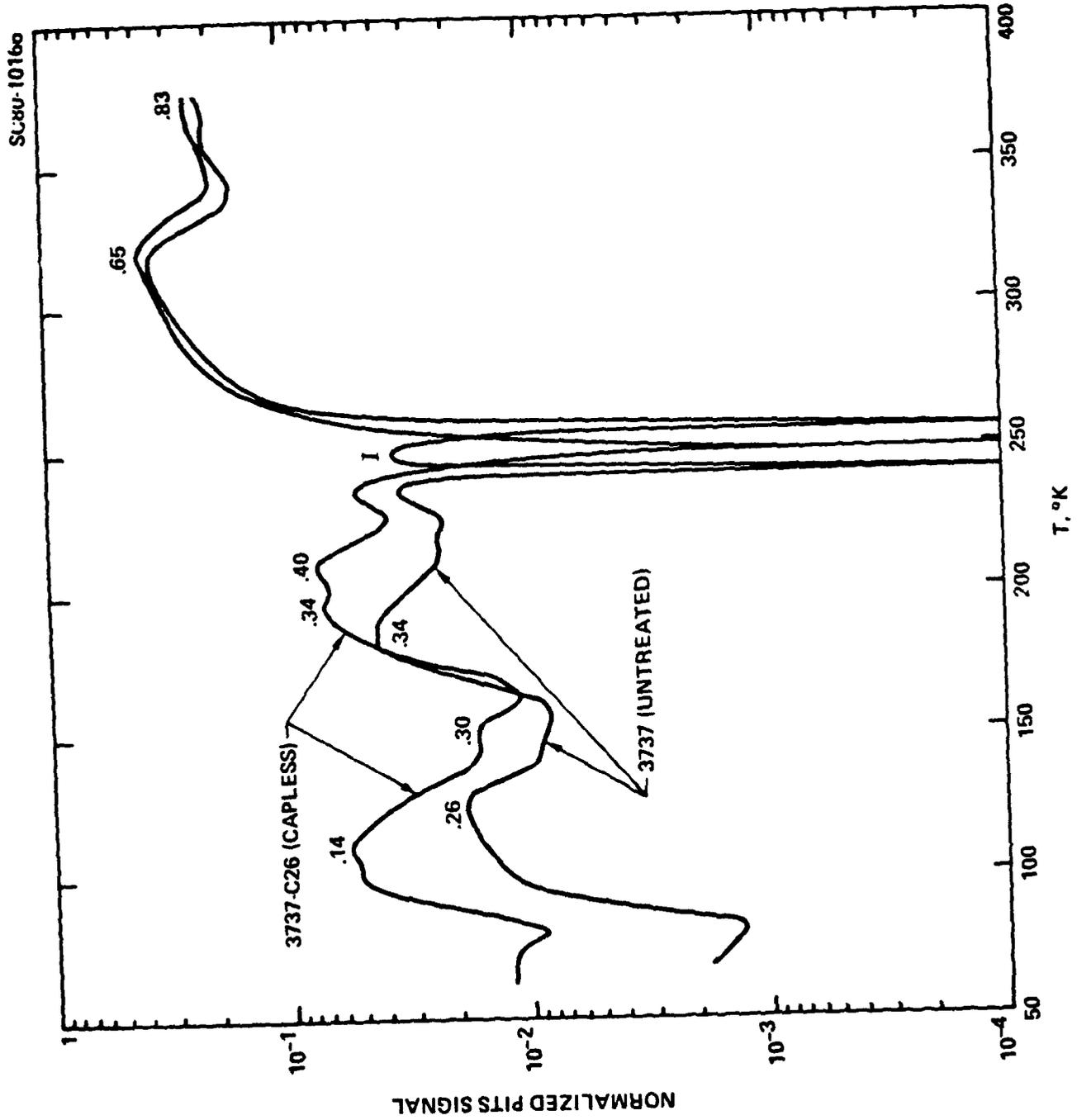
Fig. 3-4 PITS spectra of PAT annealed and unannealed GaAs, Ingot No. 3737.

produced a conducting surface layer. The surface layer of the treated substrate should therefore be studied for evidence of such Mg contamination.

The concentration profiles of the elements of interest here have been measured with secondary ion mass spectrometry (SIMS) for various ingots with both capped and PAT annealing. The profile of Mg for two samples from the ingots XS3737 and XS3608 respectively is shown in Fig. 3-5. In the case of the sample with lower Mg content, 3608, the data are close to the uncertainty limit and the actual concentration may be considerably lower than indicated. Comparing the data as measured, the Mg contents differ by a factor of over 300. Both sets of data can be fitted with the curve

$$N(x) = N_o \, \text{erfc}(x/2\sqrt{Dt}) + N_\infty \qquad (1)$$

Values for D of 1.2 and 1.3 x 10^{-14} cm^2/s have been deduced for the samples 3737 and 3608 respectively. These are very close to the published value of 1.6 x 10^{-14} cm^2/s for Mg in GaAs at 850°C.[6] For comparison the sheet resistance of these samples following PAT annealing is given in Table 3-3. The difference in conductivity is approximately 200. This correlates well with the difference in Mg content, assuming that a smaller fraction of Mg at high concentration is electrically active.

The reason for the variation in Mg content of the two samples studied is not well known. This can be due to slight difference in the surface condition of the substrates as well as the actual placement during annealing since

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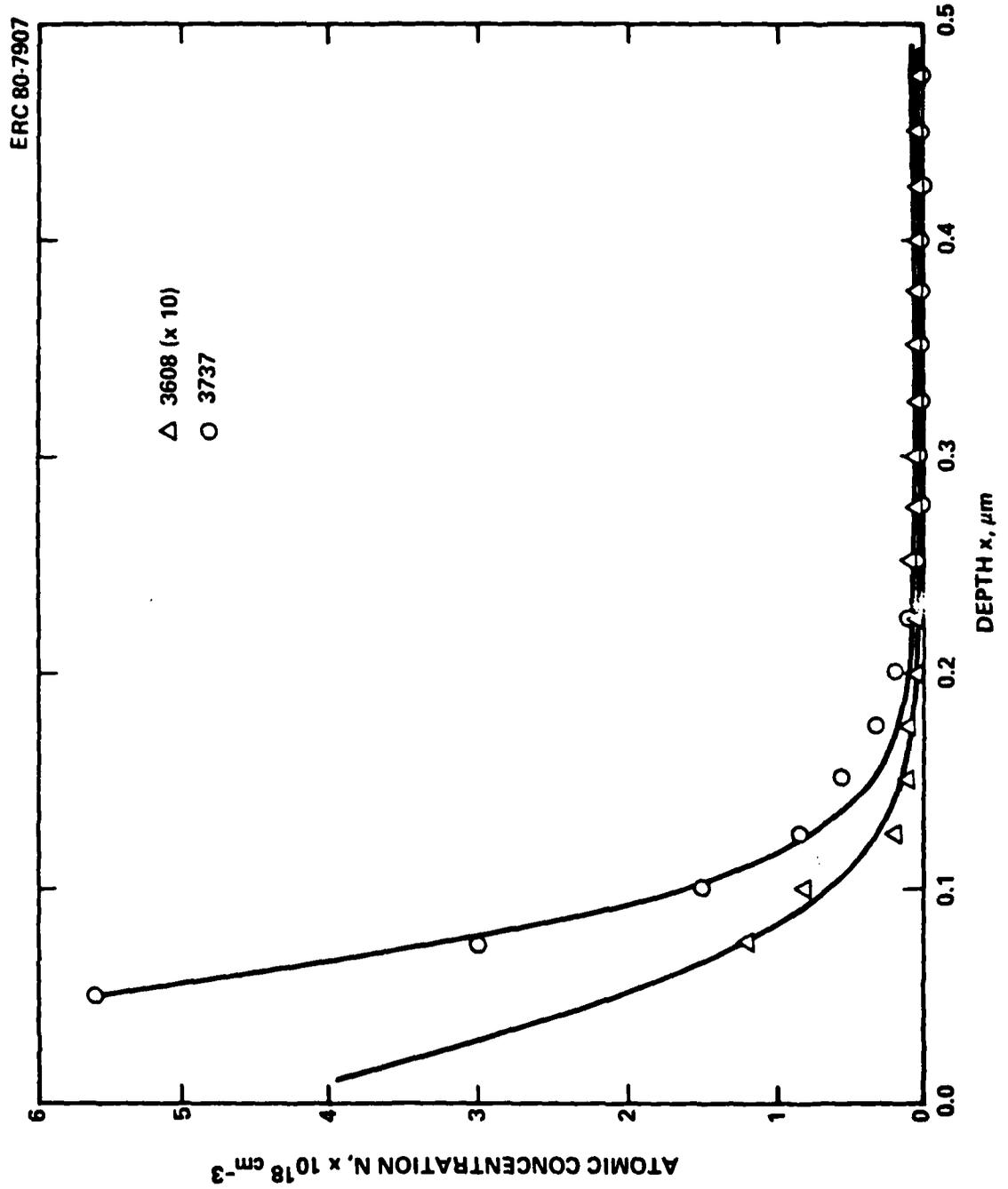
Fig. 3-5   Concentration profile of Mg in samples DS1 from ingot
XS3737 and DS3 from XS3608, both PAT annealed.

TABLE 3-3

Sheet Resistivity of PAT Annealed GaAs

Ingot Number	Sheet Resistance, $\Omega/\square$
XS3608	8.4×10^7
XS3737	4.1×10^5

they are only in loose contact with the graphite powder. Decrease in Mg in
the graphite powder with time is also possible. Since the discovery of the
correlation between the Mg contamination and the degradation in resistivity,
the conditioning procedure of the annealing medium has been revised. As-
received graphite powder is first baked without any GaAs at 850°C under
vacuum. Removal of impurities from the grphite powder under this procedure is
evident from condensations on cooler part of the tube furnace: this is not
observed when the baking under vacuum is limited to about 300°C. The usual
conditioning step of heating the entire medium of powdered graphite and
crushed GaAs in H_2 at 850°C follows this baking. Under the new procedure
successful annealing has been obtained with other GaAs ingots. It is clear
then that purity of the graphite powder is very important to the PAT
process. More work in this area is necessary to enable wide application of
this technique to the processing of GaAs material.

3.4.2 Redistribution of Cr During Annealing

A phenomenum of great interest is the movement of Cr in semi-insulating GaAs substrates during annealing. Several workers have observed depletion of Cr near the substrate surface,[7] and have proposed that this causes a region of under-compensation.[8] If the mechanism of loss of Cr occurs at the substrate surface the resultant profile will be characterized by the out diffusion from the bulk. Difference in diffusion should then be observed in the Cr profile of capped and PAT results.

The Cr concentration profiles were measured by secondary ion mass spectroscopy (SIMS). The samples studied are unimplanted semi-insulating substrates from various ingots, one set capped with silicon nitride during annealing and the other set capless annealed with PAT. Thermal treatment in all cases was 30 minutes at 850°C. Possible variation in sputtering rates was corrected by normalizing to the As count for each step, which also provides the calibration for the concentration. The depth of the sputtered craters were subsequently measured and provide the depth scale. A pair of Cr concentration profiles is plotted in Fig. 3-6. C26-3608 is a PAT annealed substrate from ingot XS3608, and C52-3608 is dielectric capped annealed substrate from the same ingot. It is immediately obvious that more severe out-diffusion of Cr occurred in the dielectric capped case. It has been found that these data can be fitted very well with the profile resulting from an outdiffusion:

$$N(x) = N_0 + (N_\infty - N_0) \ erf(x/2 \ \sqrt{Dt})$$

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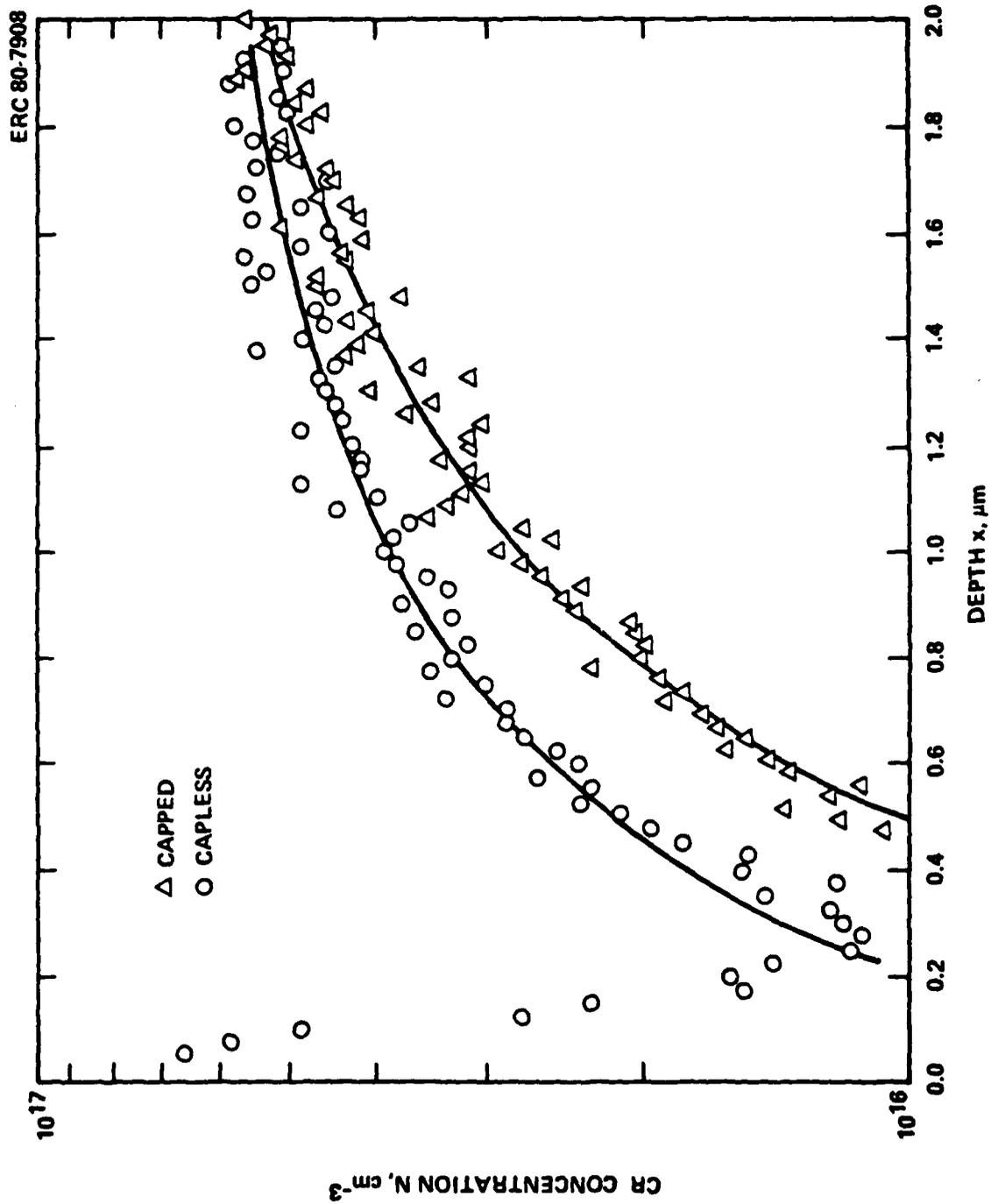
Fig. 3-6 Concentration profile of Cr in samples DS3 (PAT) and DS4 (capped annealed) both from ingot XS3608.

The deduced values of N_∞ and D are listed in Table 3-4. The relative enhancement in diffusion for capped annealing agrees very well with the corresponding results obtained for implanted impurities, although the depths involved vary over an order of magnitude. The value of D for capped annealing also agrees very well with the results given by other workers.

The diffusion in capped annealing is enhanced by a factor of nearly 2 1/2. It is shown in Section 3.5 that the same enhancement is observed in ion-implanted doping profiles. The origin of this enhancement is discussed in a later section.

TABLE 3-4

Diffusion Coefficients and Concentration of Cr in GaAs
Ingot Number XS3608

Sample	Anneal Method	$N_\infty(cm^{-3})$	$D(cm^2/s)$	D_{CAP}/D_{PAT}
C52	Cap	$7.4 \ 10^{16}$	8.0×10^{-12}	2.4
C26	PAT	5.9×10^{16}	3.3×10^{-12}	

3.5 Doping Results: Dielectric Capping Versus PAT Method

In the usual method of annealing with dielectric caps, severe strain can be induced due to difference in thermal expansion. Silicon nitride, the

usual capping material, expands only half as much as GaAs. With a difference in temperature between film deposition and annealing of typically a few hundred degrees, the strain induced is substantial. The magnitude of this strain can be estimated using a one dimensional model: the lengthwise stretch of a thin film on a bar-shaped substrate. The force per unit width required to stretch the film by a fraction $(\Delta \ell / \ell)$ is given by:

$$F = E_f d_f (\Delta \ell / \ell)$$

where E_f is the Young's modulus and d_f is the thickness of the film. The stretch caused by a difference in thermal expansion can be written as:

$$(\Delta \ell / \ell) = (\alpha_f - \alpha_s)\Delta T$$

where $\alpha_{f(s)}$ is the coefficient of thermal expansion of the film (substrate) and ΔT is the difference in temperature between film deposition and annealing. Using published values of E_f[9] and α's,[10] and typical values of d_f and ΔT, the value of F is calculated to be in the range of 10^6 dyne/cm. Such a strain tends to distort the region close to the surface, and the activation and diffusion of implanted atoms can be affected. Thus, difference in the doping profiles obtained through capped annealing and PAT can generally be expected.

Samples of GaAs substrates implanted with Se and S have been success-fully annealed using the capless, powder annealing technique (PAT).

Simultaneous with each run, samples similarly implanted and capped with 1100A
of silicon nitride are subject to the same thermal annealing cycle of 850°C
for 30 minutes. The carrier concentration profile resulting from the doping
is measured using the capacitance-voltage (C-V) technique. In addition, the
sheet carrier concentration and the mobility are measured using van der Pauw
type Hall effect measurements. The profiles of the PAT and silicon nitride
capped samples are compared. Fits have been made to theoretical curves
calculated from LSS range parameters, taking into consideration the diffusion
of dopants during the high temperature anneal. Half Gaussian profiles
calculated for the projected range and standard deviation are used as the
initial distribution.[11] Values of the diffusion constant in the
neighborhood of published data are used to generate families of curves, and
effective values are deduced from the best fits.

The first series of samples investigated were implanted with 300 keV
Se to dose of 3×10^{12} cm^{-2}. When the profile of a silicon nitride capped
sample is compared with that of a PAT sample, a trend is evident: the former
shows more "tailing" into the substrate. Figure 3-7 shows a pair of curves
comparing the profiles of capped (C41N) and a PAT (C40P) sample. Fits to
theoretical curves are made using the following LSS range parameters: pro-
jected range = 1028A and standard deviation = 438A. Diffusion into infinite
medium is assumed. Best fit using a non-linear curve fitting routine for the
profile C41N and C40P is illustrated in Fig. 3-8. The correspondence to a
Gaussian profile is generally good, except near the tail part. A diffusion
constant D of 5.5×10^{-15} cm^2/sec, Dt = 9.9×10^{-12} cm^2, has been deduced for

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CARRIER CONCENTRATION, $N_D(cm^{-3})$

C4IN
300 KeV Se
$3 \times 10^{12}/cm^2$
CAP
850°C 30 min

C40P
300 KeV Se
$3 \times 10^{12}/cm^2$
PAT
850°C 30 min

THICKNESS, t (μm)
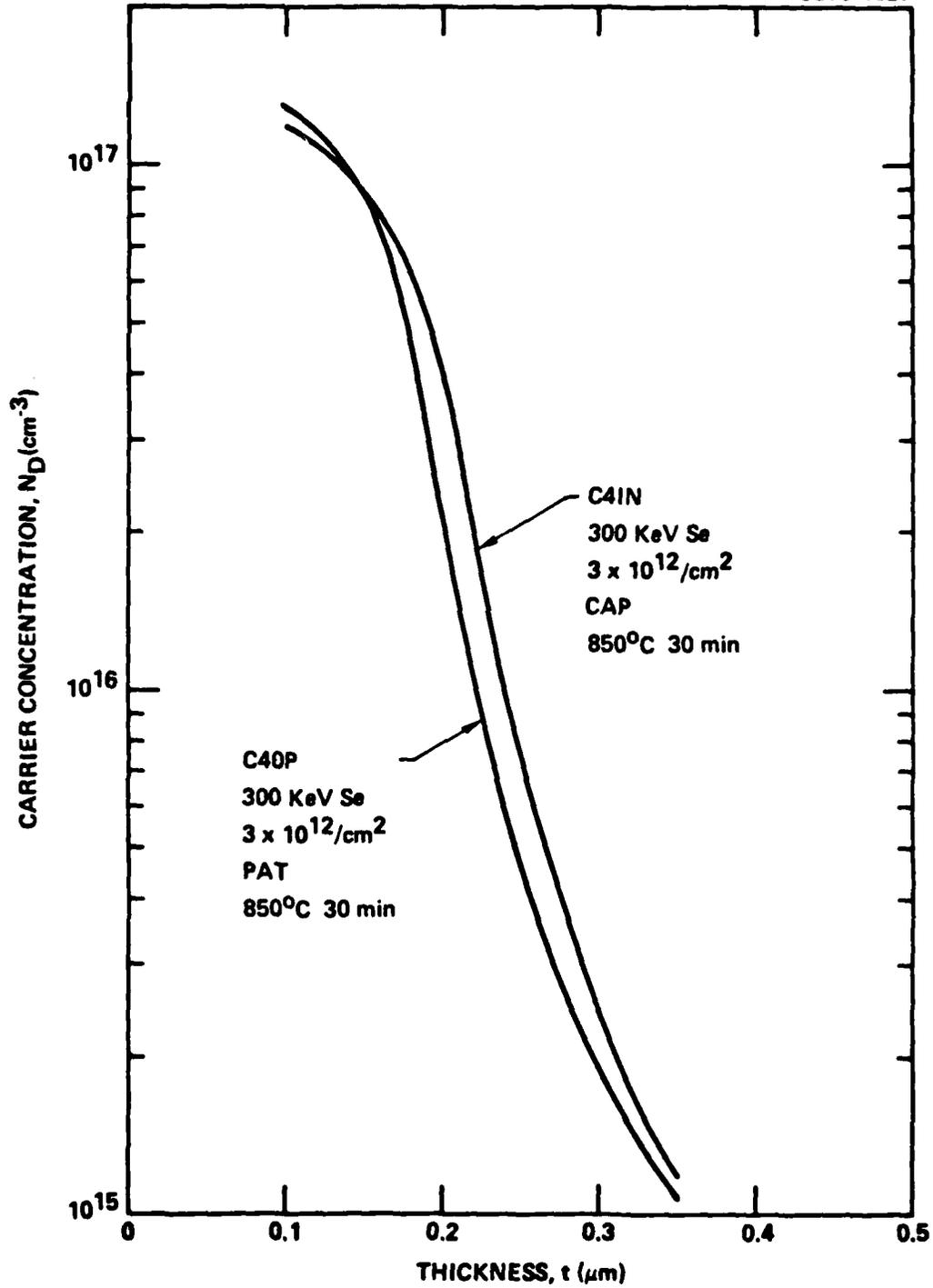
Fig. 3-7   Doping profile of 300 kev Se implanted GaAs with doses of
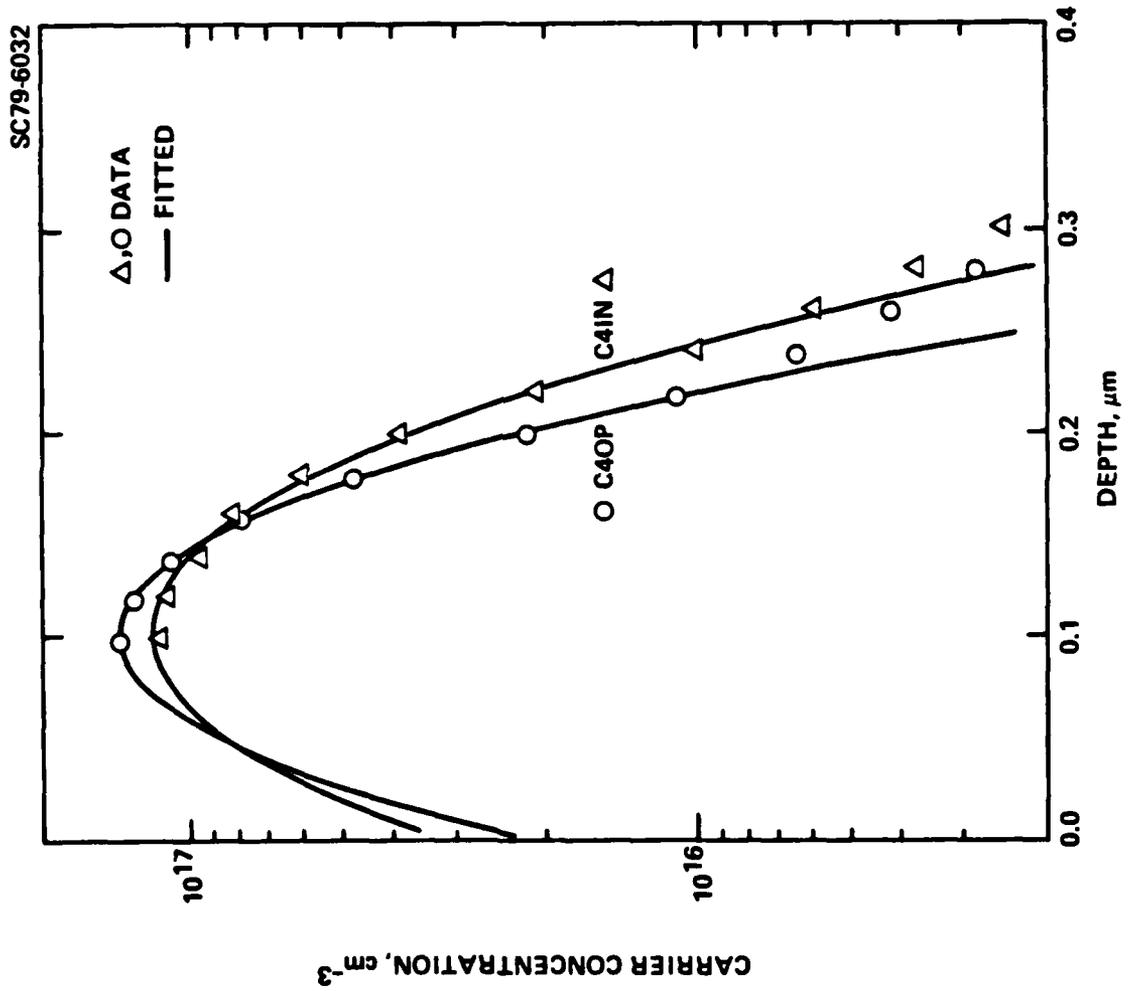$3 \times 10^{12}/cm^2$, annealed with PAT (C40P) and cap (C41N).

Fig. 3-8 Fitted profiles of samples C40P (PAT) and C41N (capped annealed) both implanted with 300 keV Se with doses of $3 \times 10^{12} cm^{-2}$.

the capped sample. On the other hand, a value of $D = 2 \times 10^{-15}$ cm^2/sec, $Dt = 3.7 \times 10^{-12}$ cm^2, for the PAT sample gives the best fit to the experimental curve. Since the broadening of the profile by diffusion is considerably smaller than the LSS standard deviation, the deduced values of D is very sensitive to factors such as systematic errors in measurement and degree of fitness during curve-fitting. Such variations can be as high as 50%. Nevertheless, the relative enhancement in diffusion of a capped sample is roughly twice that in a corresponding PAT one. This trend is also observed in other pairs of samples.

The mobility, μ, and sheet carrier concentration N_s as measured by the van der Pauw method are given in Table 3-5. The mobility in the capped and PAT samples is comparable, and the activation is very close. The low percentage of activation is believed to be a problem associated with the particular ingot.

With the 300 keV Se implanted samples, the minimum depth that can be investigated using C-V measurement is about 1000Å. Since the peak of the profile of 300 keV Se in GaAs falls close to the surface, the measured profile is not complete. It is therefore desirable to obtain further data to improve the confidence.

The next series of samples were implanted with 400 keV Se to a dose of 3.5×10^{12} cm^{-2}. The carrier concentration profiles measured by C-V technique, now showing over half of the curve, again indicate less diffusion of dopant in the PAT samples compared to the silicon nitride capped samples. A pair of curves, a silicon nitride capped sample C46N and a PAT sample C46P, is shown in Fig. 3-9. Using the parameters of projected range = 1371Å and standard
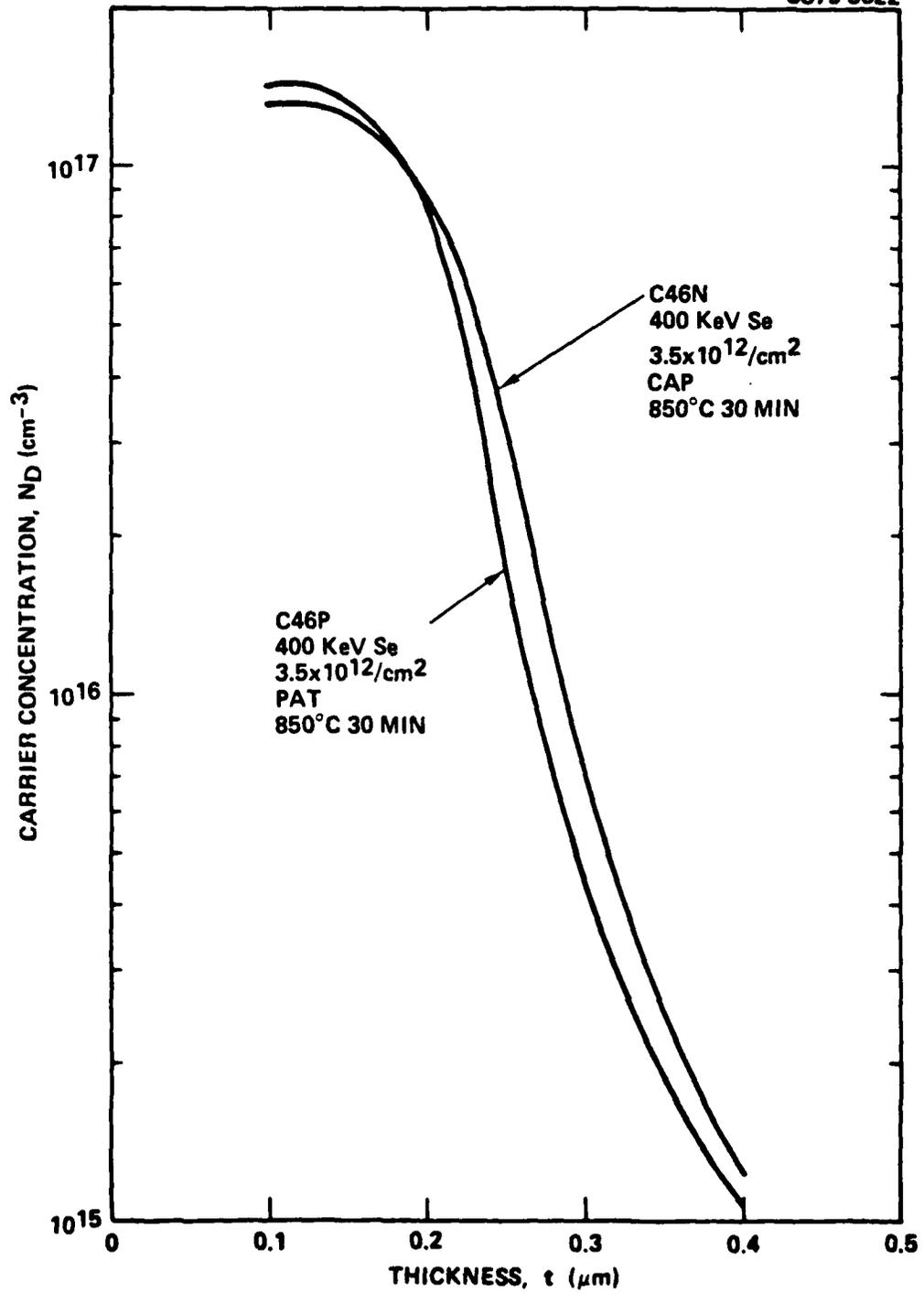
SC79-3822

Fig. 3-9   Doping profile of 400 keV Se implanted GaAs with doses of
3.5 x 10^12/cm^2, annealed with PAT (C46P) and cap (C46N).

TABLE 3-5

Mobility and Apparent Activation in 300 KeV Se Implanted GaAs,
Annealed with PAT and with a Dielectric Cap

Sample	Anneal Method	Ingot	$\mu(cm^2/V\text{-}sec)$	N_s (cm^{-2})	Activation (%)
C40P	PAT	XS3608	4110	8.70×10^{11}	29
C41N	Silicon nitride cap	XS3608	4500	8.79×10^{11}	29

deviation = 557A, a diffusion constant of 4.7×10^{-15} cm^2/sec has been deduced
for the sample C46N, and a value of 1.9×10^{-15} cm^2/sec for C46P, using the best
fit illustrated in Fig. 3-10. The relative enhancement in diffusion, within the
limit arising from experimental errors and curve fitting, agrees well with the
results obtained from the 300 keV samples. Consistency of this trend among 400
keV samples is also good. The mobility and sheet carrier concentration measured
by Hall effect are given in Table 3-6. Again, the values for capped and PAT
samples are very close.

The mobility in the PAT cases is slightly lower than in their capped
annealed counterparts. One reason for this difference is the impurities in the
graphite powder. Commercially available graphite powder has been used throughout
this program. Certain impurities can be reduced with prolonged baking prior to
use. However, even at low concentrations of parts per million, these impurities
can diffuse into the surface layer of the substrate to levels of 10^{16} cm^{-3} or
higher. This can result in the observed reduction in mobility. This is however
not a fundamental problem with PAT. Improvement in the mobility can be obtained
by using purer graphite powder. This should be investigated in future works.
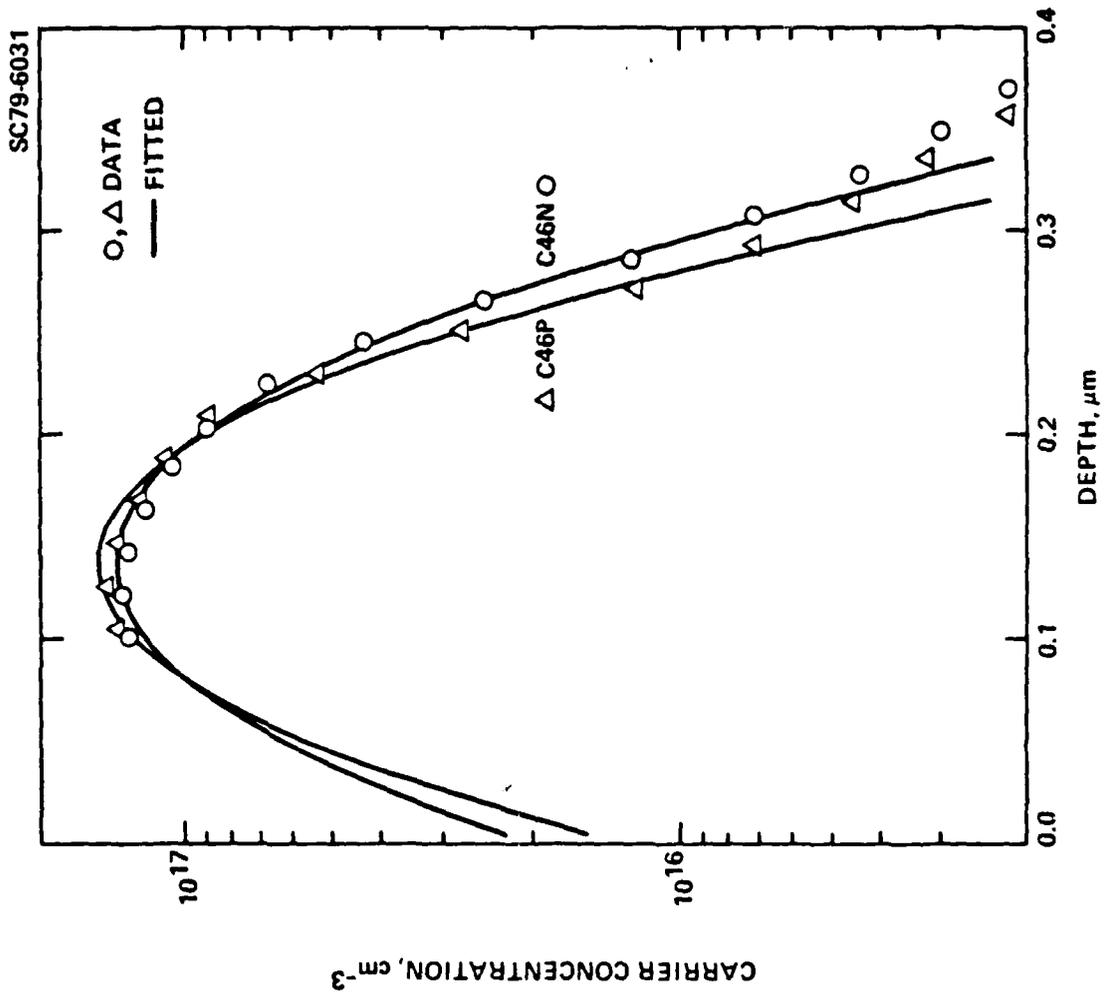
Fig. 3-10 Fitted profiles of samples C46P (PAT) and C46N (capped annealed) both implanted with 400 keV Se with doses of 3.5×10^{12} cm^{-2}.

TABLE 3-6

Mobility and Apparent Activation in 400 KeV Se Implanted GaAs,
Annealed with PAT and with a Dielectric Cap.

Sample	Anneal Method	Ingot	$\mu(cm^2/V\text{-}sec)$	N_s (cm^{-2})	Activation (%)
C46P	PAT	XS3608	4290	1.66×10^{12}	47
C46N	Silicon nitride cap	XS3608	4620	1.70×10^{12}	49

We have also investigated the doping in S implanted GaAs. Sulphur is of particular interest since it diffuses considerably in GaAs, and differences in diffusion are readily observable. The results of the PAT processed sample and the silicon nitride capped one, both of which were implanted with 200 keV S to a dose of 5×10^{12} per cm^2, are very different. The carrier concentration profiles are shown in Fig. 3-11. For the capped sample, best fit is found to be in between the assumptions of diffusion into infinite medium, and no out-diffusion from the substrate. A value of $D = 10^{-13}$ cm^2/sec is obtained. The PAT case is more complicated. Neither of the above assumptions fit the measured profile well. In particular, there is a trend towards fairly high carrier concentration at the surface. By using a Gaussian profile, a value of $D = 2 \times 10^{-14}$ cm^2/sec is obtained. The enhanced diffusion of S is apparent in capped annealed samples in spite of the difficulties in fitting the curves.

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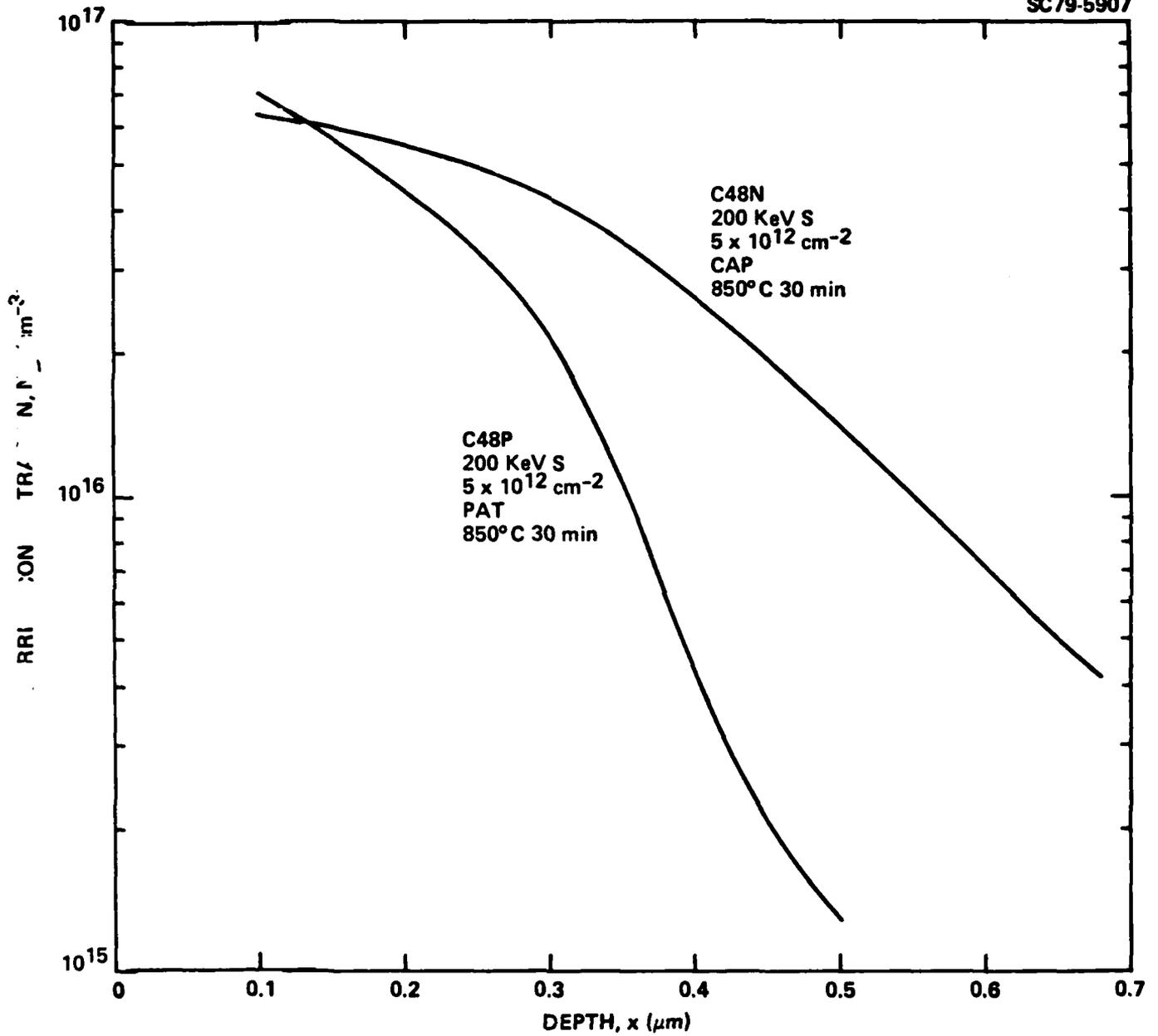
Fig. 3-11 Doping profile of 200 keV S implanted GaAs with doses of $5 \times 10^{12}/cm^2$, annealed with PAT (C48P) and cap (C48N).

The diffusion of Se in GaAs during PAT and capped annealing is summarized in Table 3-7. An enhancement of about 2 1/2 is observed. This is in good agreement with the result of Cr diffusion studied with SIMS, in spite of the depth involved spanning an order of magnitude.

TABLE 3-7

Diffusion Coefficient of Se Implanted in GaAs
and Annealed at 850°C for 30 Minutes

Sample	Se Energy	Anneal Method	$D(cm^2/s)$	D_{CAP}/D_{PAT}
C41N	300 KeV	Cap	5.5×10^{-15}	
C40P	300 KeV	PAT	2.1×10^{-15}	2.6
C46N	400 KeV	Cap	4.7×10^{-15}	
C46P	400 KeV	PAT	1.9×10^{-15}	2.5

It is therefore very likely that the mechanism involved is common to all the cases studied. One possibility is the mechanical strain induced by the cap, which is absent in PAT annealing. This is discussed in detail in the following section.

3.6   Effect of Strain on Diffusion

It has been shown in previous sections that the diffusion of impurities during annealing is enhanced in the presence of a cap. For a silicon-nitride cap of 1100A thick, the relative enhancement is approximately 2 compared to capless PAT cases. In capped annealing, the cap is usually deposited at a temperature considerably lower than the annealing temperature. In addition the cap and the substrate materials generally possess different thermal expansion. Hence during annealing considerable mechanical strain can be induced in the GaAs substrate near the surface. This can affect the extent of diffusion of dopants and the doping profile.

An experiment has been undertaken to observe the effect of strain to the diffusion of dopants during annealing. Controlled mechanical stain is induced to the substrate and the diffusion coefficient is deduced from the doping profile. The method used here is a backside cap of a suitable material which possesses the opposite sense of thermal expansion relative to GaAs as Si_3N_4. A good choice is Al_2O_3. The coefficient of linear thermal expansion[10] of Si_3N_4, GaAs, and Al_2O_3 is given in Table 3-8.

When a thin film of Si_3N_4 (Al_2O_3) is deposited on a GaAs substrate and the combination is heated to a higher temperature, the film becomes stretched (compressed) due to the mismatch in expansion, and the substrate is bent. This is shown in Fig. 3-12a. Since the substrate is much thicker than the film (~ 600 μm compared to ~ 0.1 μm), the two sides of the substrate is under opposite strain of equal magnitude. For a front Si_3N_4 cap the stretched film bends the substrate resulting in a compressive strain in the region of

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DURING Si₃N₄ DEPOSITION — DURING ANNEALING

(ACTIVE LAYER SIDE UP)
(a)

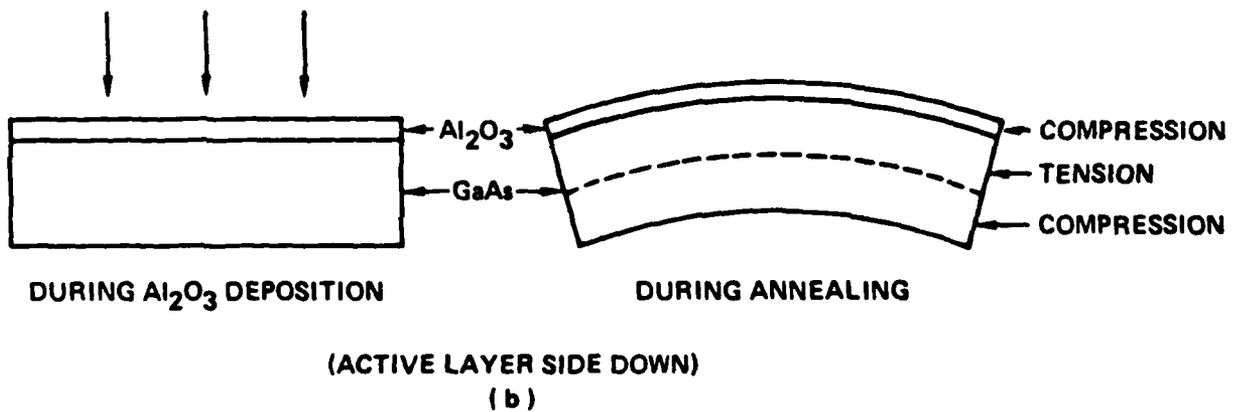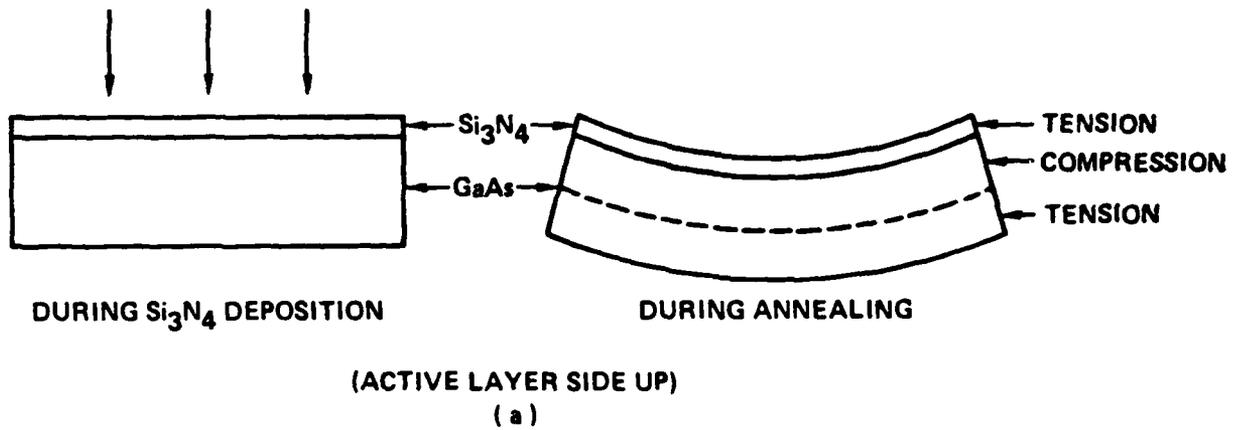DURING Al₂O₃ DEPOSITION — DURING ANNEALING

(ACTIVE LAYER SIDE DOWN)
(b)

Fig. 3-12 Equivalent bending of GaAs substrate during annealing with (a)
Si₃N₄ on the front, and (b) Al₂O₃ on the back.

the active layer. On the other hand, for a back Al_2O_3 cap the compressed film also results in a similar strain to the active region. This is illustrated in Fig. 3-12b. By adjusting the thickness of the films the same amount of strain can be obtained. It should be noted that when both caps are present, since they both tend to bend the substrate in the same sense, the force on the substrate is additive.

TABLE 3-8

Coefficient of Thermal Linear Expansion,
α, 10^{-6} k^{-1}

Si_3N_4	GaAs	Al_2O_3
3.6	7.3	9.4

Consider for simiplicity the one dimensional problem of a thin film on a much thicker beam. The amount of force per unit width required to bend the beam to a radius of R is given by:[12]

$$F = E_s t^2_s/6R$$

where E_s and t_s are the Young's modulus and the thickness of the substrate respectively. On the other hand, the amount of force per unit width required to stretch a thin film by a fraction of $(\Delta l/l)$ is given by:

$$F' = E_f \, t_f (\Delta \ell / \ell)$$

where $(\Delta \ell / \ell) = \Delta \alpha \Delta T$, ΔT being the difference in temperature, $\Delta \alpha = (\alpha_f - \alpha_s)$, and the subscript "f" refers to the film. Values of E for Si_3N_4, GaAs, and Al_2O_3[13,14,15] is given in Table 3-9.

Table 3-9

Young's Modulus, E, $\times 10^{11}$ dyne/cm^2

Si_3n_4	GaAs	Al_2O_3
9.0	7.54	36.6

If the thickness of the substrate is kept constant, then the same radius of curvature will give the same strain near the surface. Comparing a front cap(1) and a back cap(2), this condition is met when:

$$(\alpha_s - \alpha_{f1}) E_{f1} d_{f1} = (\alpha_{f2} - \alpha_s) E_{f2} d_{f2}$$

Using the values of α and E from Tables 3-8 and 3-9, a 500A thick Al_2O_3 back cap will produce the same effect as an 1100A thick Si_3N_4 front cap.

The GaAs substrates used in this experiment come from the same slice in an ingot and are polished on both sides. All are implanted with 375KeV Se

with doses of 3.5×10^{12} cm^{-2}. Half of these are front capped with 1100A of reactive sputtered Si$_3$N$_4$, while the rest are left bare for PAT processing. Al$_2$O$_3$ back cap of different thicknesses are deposited by e-gun evaporation of sapphire. The substrates are annealed at 850°C for 30 minutes in H$_2$. After striping the Si$_3$N$_4$ front cap, where applicable, and cleaning, Al Schottky-barrier dots are deposited and the doping profile is measured using the capacitance - voltage (C-V) technique.

Among a family of doping profiles with Al$_2$O$_3$ back caps of 0A, 500A, 1000A, and 1500A thick, a trend of increasing width of the profile with film thickness is observed. A representative set of curves is illustrated in Fig. 3-13. These substrates have been annealed with both front Si$_3$N$_4$ and back Al$_2$O$_3$ caps. Some scattering of data is observed over each substrate. Such differences are however small compared to the variation observed among the samples. The diffusion coefficient in each case is obtained by fitting a gaussian curve to the doping profile and compare the result with LSS range statistics. For small diffusion coefficients the error induced can be rather large. For this reason, the set of curves for front Si$_3$N$_4$ and back Al$_2$O$_3$ capped samples are used because of the further enhancement in diffusion due to the front cap. The diffusion coefficient of Se in GaAs at 850°C is shown in Fig. 3-14 as a function of the thickness of the Al$_2$O$_3$ back cap. An exponential dependence is observed to fit the trend rather well. Since an 1100A thick Si$_3$N$_4$ front cap produces the same effect as a 500A thick Al$_2$O$_3$ back cap, by extrapolating the data to a thickness of -500A, the diffusion coefficient for the capless annealed case should be obtained. This turns out to be 1.9×10^{-15} cm^2/s, which is in good agreement with the values obtained in this and previous experiments.

SEMICONDUCTOR DOPING PROFILE

375 KeV Se
$3.5 \times 10^{12}/cm^2$
850° C 30 min
Al_2O_3 BACK CAP

41A (0A)
41B (500A)
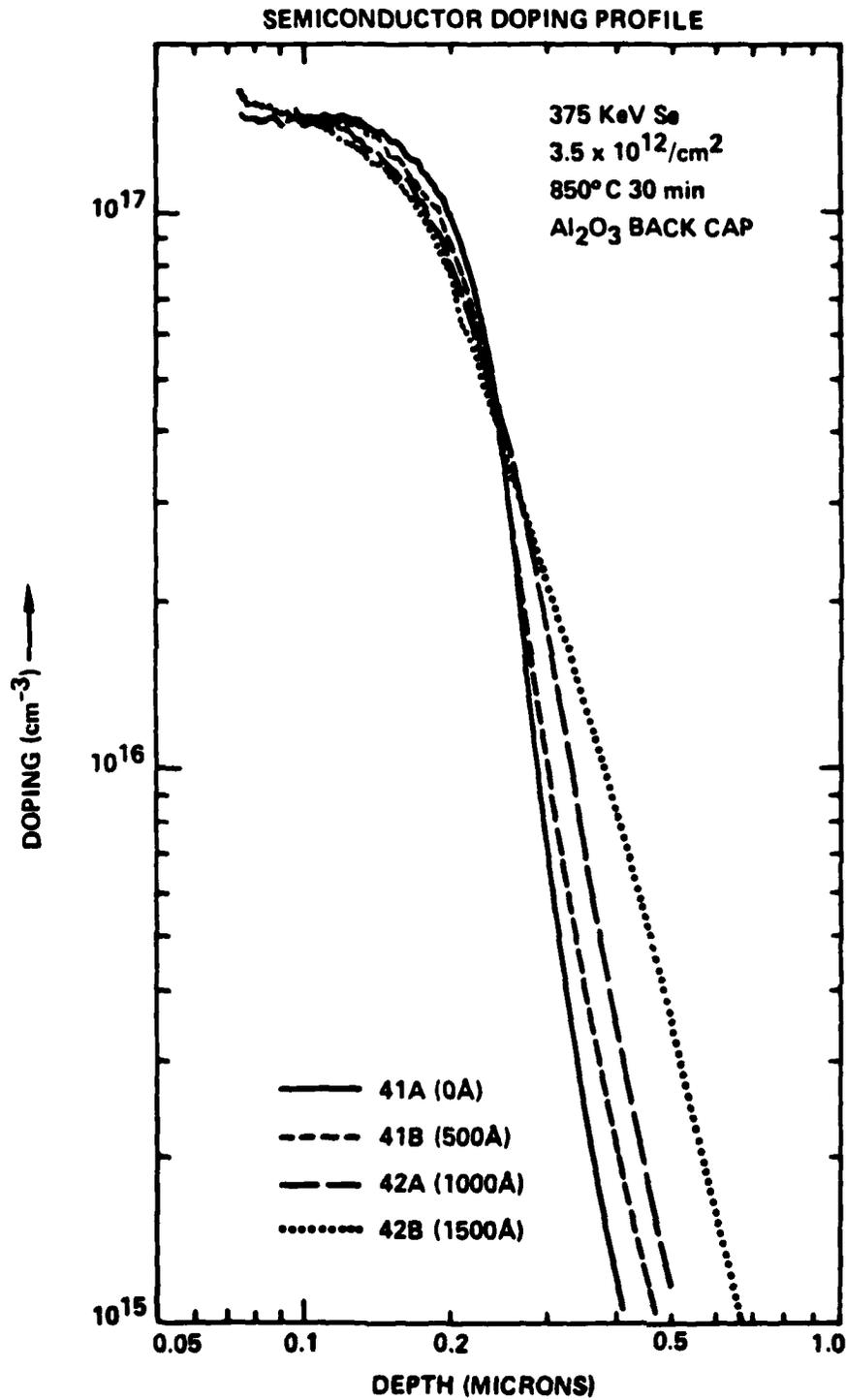42A (1000A)
42B (1500A)

DOPING (cm^{-3})

DEPTH (MICRONS)

Fig. 3-13 Doping profile of 375 KeV Se implanted in GaAs and annealed
at 850°C for 30 minutes with various thickness of Al_2O_3 on
the back.

$D = D_o \exp(d/d_o)$
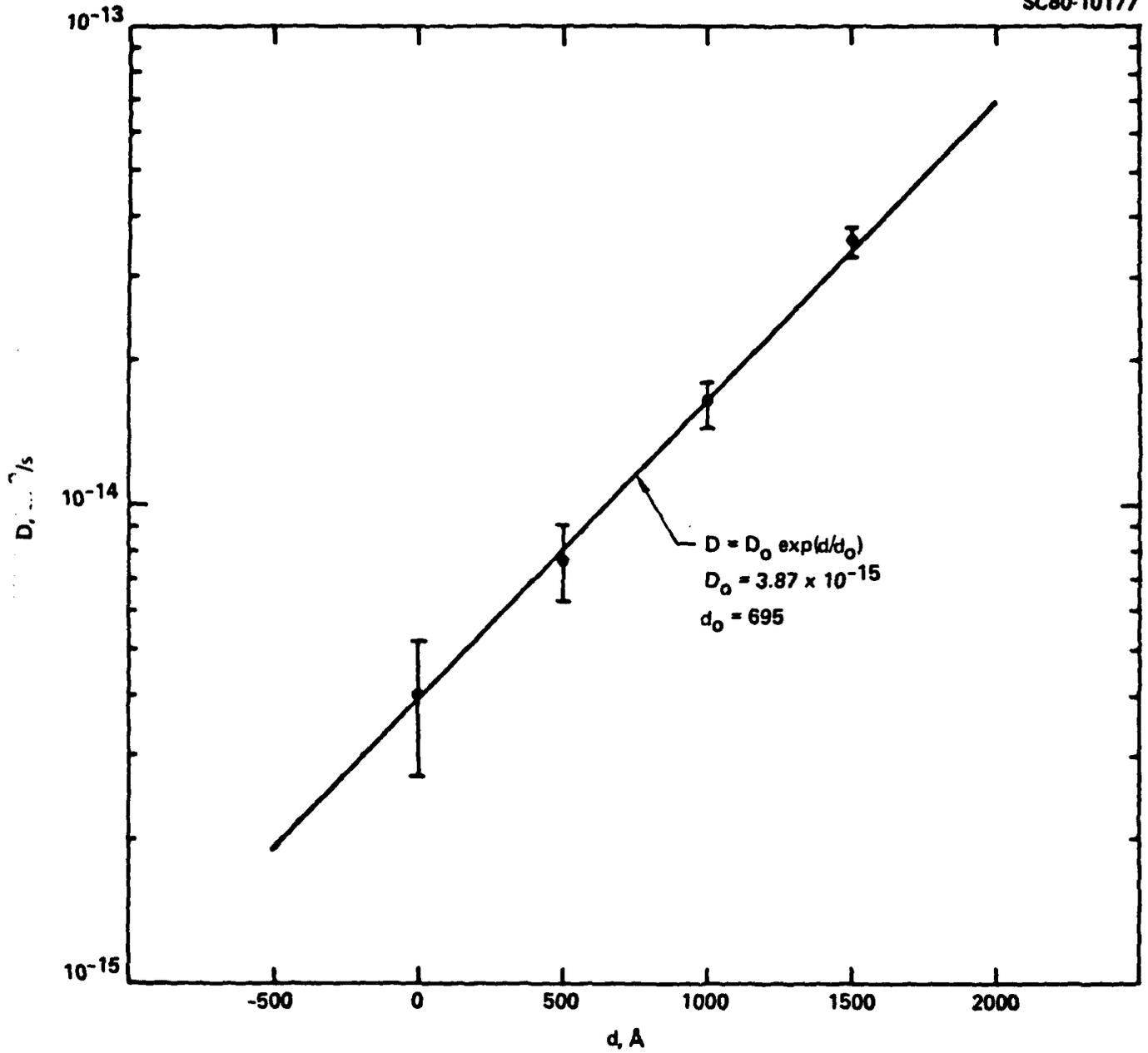$D_o = 3.87 \times 10^{-15}$
$d_o = 695$

Fig. 3-14 Diffusion coefficient of Se in GaAs at 850°C with various thickness of Al_2O_3 back cap.

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While it is beyond the scope of this program to fully investigate the
fundamental mechanism of the enhanced diffusion due to strain, it is
nevertheless possible to explain the observed behavior in a phenomenological
manner. The diffusion coefficient can be expressed as

$$D = D_0 \exp(- E_A/kT)$$

where the activation energy E_A depends on the condition of the crystal
lattace. For small perturbations to the lattice due to strain S, this can be
written as

$$E_A = E_0 - E_1 S$$

where the sign is chosen to agree with empirical results. The strain on the
crystal due to a thin film deposited on it is proportional to the thickness d
of the latter: $S = S_1 d$. The diffusion coefficient can therefore be written
as:

$$D = D_0' \exp(d/d_0)$$

where $D_0' = D_0 \exp(- E_0/kT)$ and $d_0^{-1} = E_1 S_1/kT$. Such a relation is indeed
observed in the present experiment. Assuming an activation energy of about
4eV for Se diffusion in GaAs[6], the change in E_A deduced from this model over
the range of d used in this experiment is only a few percent, and can
therefore be considered a small perturbation.

4.0 SUMMARY AND RECOMMENDATIONS

The work performed in this program has significantly improved the understanding and capability of utilizing capless annealing in ion implanted GaAs technology. The powder annealing technique (PAT) developed here provides high thermal stability of semi-insulating substrates and good activation of ion implanted dopants. Resistivities of $10^8 \Omega/\square$ can be obtained for semi-insulating material and implanted active layers are comparable to ones obtained with capped annealing.

In comparing the distribution of impurities following annealing, capless annealed wafers consistently exhibit less diffusion than capped ones. Using externally induced strain it has been demonstrated that the enhanced diffusion in capped annealing is caused by the strain due to the cap. Capless annealing is therefore a better choice of processing technique for achieving shallow and steep doping profiles. Cr out-diffusion in semi-insulating GaAs substrates has been suggested to result in an under-compensated region near the surface and to give rise to thermal conversion and distortions in doping profiles. With less diffusion in capless annealing, such failure can be reduced. The small diffusion of dopants will also give more consistent agreement with predicted profiles.

The technique investigated here demonstrates that capless annealing of a compound semiconductor can be achieved by using a medium saturated with the more volatile species to prevent the substrate from decomposition. This permits annealing to be performed even when a dielectric cap is impractical

due to chemical reaction or excessive strain to the substrate. A demonstrated advantage of capless annealing is the substantially reduced diffusion of impurities. This can be used to produce sharp doping profiles desirable for millimeter wave devices, and the less severe depletion of Cr and under-compensation near the surface can result in qualification of more GaAs materials for ion implantation. It is also a very useful tool in characterizing GaAs materials. While the PAT process has been demonstrated to provide successful annealing, there are areas where improvements can be made. Higher purity of the graphite powder, for example, can result in higher mobilities in ion implanted layers. It is recommended that further work on this capless annealing technique be pursued, especially in the understanding and control of strain related impurity redistribution for application to material characterization and process development.

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APPENDIX

Related Presentations and Publications

1. D. P. Siu and A. A. Immorlica, Jr. "Capless Annealing of Ion Implanted GaAs," presented at the 21st Electronic Materials Conference, (Boulder, Colorado, June 27-29, 1979).

2. D. P. Siu and A. A. Immorlica, Jr., "Comparison of Doping Profiles in Capless Annealed and Dielectric Capped-Annealed Ion Implanted GaAs," J. Electron. Mat. 9, 857 (1980).

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