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INVESTIGATION OF CHARGE COUPLED DEVICES FOR SIGNAL PROCESSING

University of Illinois

C. T. Sah
P. C. Chan
J. F. Detry
Y. C. Sun

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This report describes a noise correlation processor for automatic low frequency noise power spectra measurements, theoretical analyses of hot electron effects and trapping noise in silicon charge coupled devices, small-signal equivalent circuit measurement of SiO_2-Si interface states, the voltage stimulated capacitance transient spectroscopy (VSCTS or DLTS) of silicon bulk deep levels due to impurities and ion implantation damage for burried channel CCD, spurious DLTS surface signal, and CCD (Cont'd)

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EVALUATION

The present contract provides basic theoretical and experimental information on some of the fundamental material properties of CCD devices such as noise sources due to surface states, and high field and interband ionization effects which limit the performance of such devices in implementing signal processing functions. The results obtained will be useful in enhancing the performance of and defining the limitations of such devices as to speed of operation, dynamic range, and functional density.

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JERRY SILVERMAN
Project Engineer

I. INTRODUCTION

A number of fundamental material properties which limit the performance of silicon charge coupled devices for signal processing are investigated in this program. To get a wide dynamic range, the noise sources must be identified and reduced. To increase the frequency of operation, the basic limitations on the charge transfer speed and charge transfer efficiency must be assessed. This report gives a summary of the studies which aimed at understanding some of these basic limitations.

To facility the study of noise, especially at low frequencies in MOS transistor and CCD structures, a hardware computer-controlled noise correlation processor was built. Its design, error analysis and operation were described in a published RADC report [1] and a summary is give in section II in this final report.

The 1/f low-frequency noise is generated mainly in the output MOS transistor stage of a CCD. For the CCD transfer stages, the dominant noise source is the random thermal generation and capture or trapping of electrons (in n-channel CCD) at the SiO_2-Si interface states. A detailed review of the CCD noise literature is given in a second RADC report [2]. In section IV, a summary of the interface trapping noise is given which extends previous work on thermal emission noise to random capture noise as well as noise due to incomplete filling of the interface states for low and moderate capture rates.

The ultimate transfer speed in CCD is limited by two dominant high electric field effects which occur when the gap and gate lengths are reduced to shorten the charge transfer time. These are the mobility reduction due to the increasing electron energy loss to phonons in high electric fields and the interband impact ionization or electron-hole pair production in high electric fields which obscures the zeros and which also contributes noise.

In section III, the effect of high field mobility reduction on the charge transfer speed is analyzed and the use of appropriate hot electron diffusivity is discussed. The ultimate transfer speed limitation by high electric fields is discussed in section VII which shows its dependence on gate length, mobility reduction, drift velocity saturation and impact ionization effects.

A third high field effect is actually beneficial. This is the reduction of the thermal capture rate of electrons at the interface states in high fields. This would reduce the interface trapping noise as well as transfer efficiency. It is discussed in section IV.

Fundamental measurement methods are described in section V and VI to characterize the interface states in surface channel CCD's and bulk deep levels in buried channel CCD's. The small-signal equivalent circuit model is described in section V and is used to obtain the density of states and the thermal emission and capture rates of electrons and holes at the interface states from MOS admittance measurements. In section VI, the voltage stimulated capacitance transient spectroscopy (VSCTS), an improved DLTS (Deep Level Transient Spectroscopy), is described as a method to determine the recombination parameters of electrons and holes at impurity levels and ion-implantation-damage levels in the bulk of silicon.

II. NOISE CORRELATION PROCESSOR

2.1 Introduction

A hardwired noise correlation processor has been designed, built and tested. The correlator consists of a high speed noise data sampler and multiplier. Noise data can be sampled at selected sample rates (up to 200 KHz) and selected number of samples (up to 16384 samples). These data are then processed by the high speed multiplier and stored in the memory of the processor. They are then clocked into the memory of the Wang 720C programmable desk calculator for further analysis and plotting. The details of design, error analysis and operation of the noise correlator was reported in a previous report [1]. The results are summarized in the next sub-section.

2.2 Experiment Results

A detailed block diagram of the correlator is shown in Figure 2.1. The instrument has several convenient features such an input overload and output ready indicators, adjustable clock, adjustable output gain, adjustable number of samples, and an output recirculate mode for oscilloscope display. Oscilloscope photographs of actual correlator calculated autocorrelation functions are shown in Figure 2.2 for sinusodal, square wave, white noise and Lorentzian noise inputs. The upper trace in each case is the autocorrelation function and the lower trace is the input signal.

Figures 2-3 and 2-4 show plots of the correlator-calculated autocorrelation function and the subsequent calculator-calculated power spectrum. The input signal here is Lorentzian noise with a $1/[1+(f/f_o)^2]$ spectrum. There is some scatter, but a three point average shown in

Figure 2.5 gives a smooth curve with little loss in frequency resolution. In fact, the small filter hump at about 600Hz is still retained.

2.3 Summary

Various sources of error were considered in designing the correlator in order to get the most efficient system in terms of speed, accuracy, size, cost and convenience. These included high frequency aliasing, low frequency resolution, A/D conversion, finite time, finite sampling and quantization. The final correlator uses the incomplete correlation method and four bit input resolution. This system combines the high-speed, dedicated front-end processor (the correlator) with a flexible general purpose computer which can be a calculator, minicomputer or microcomputer.

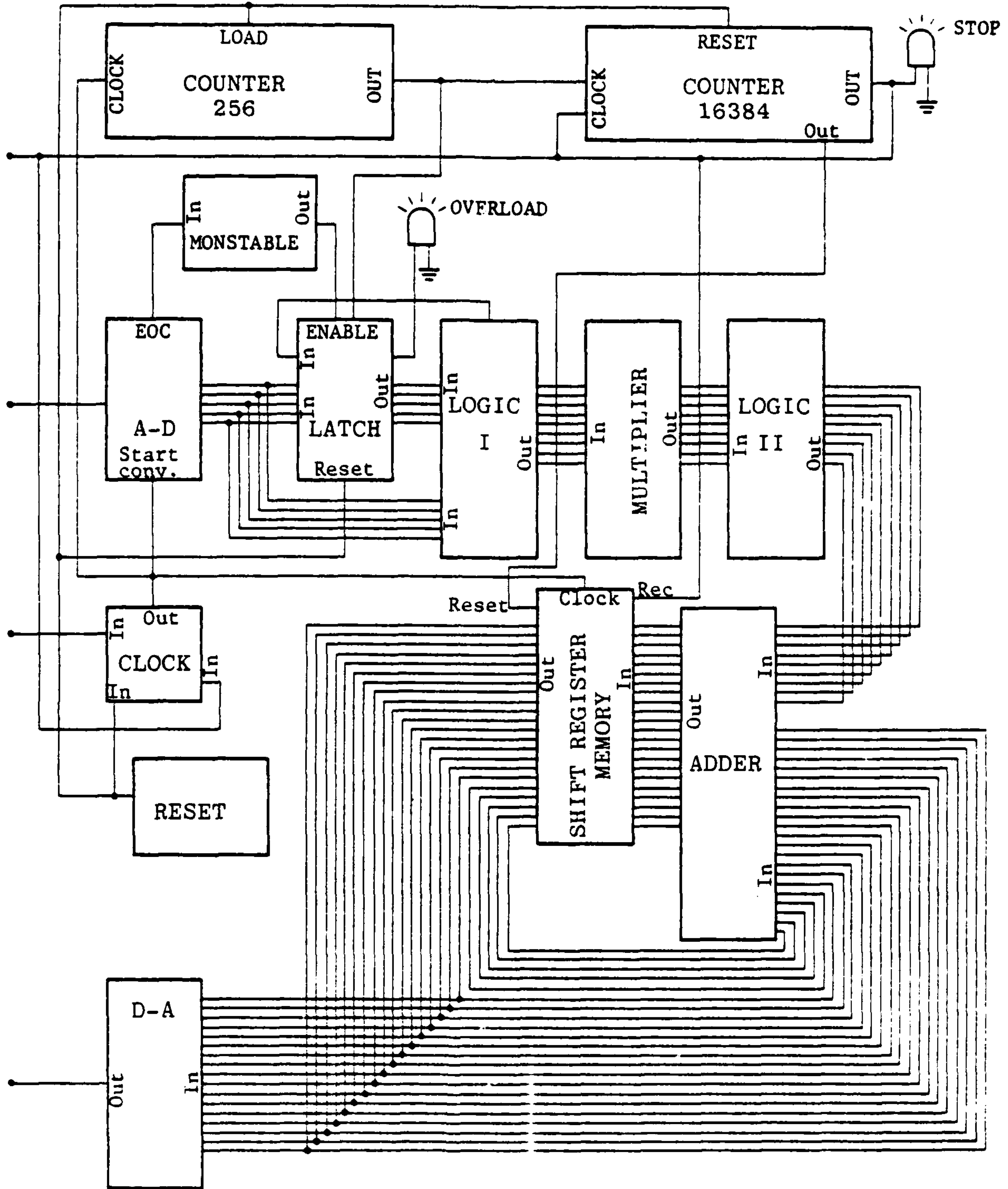
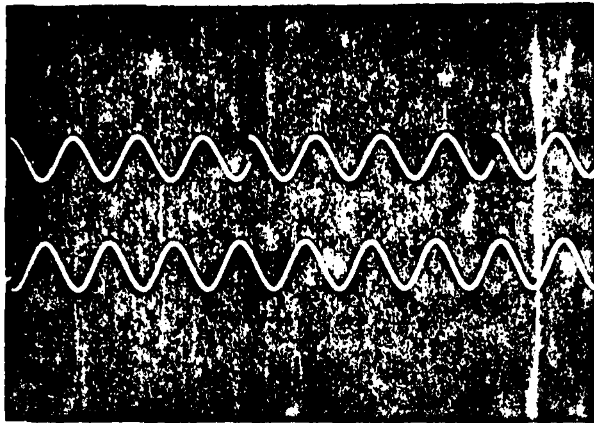
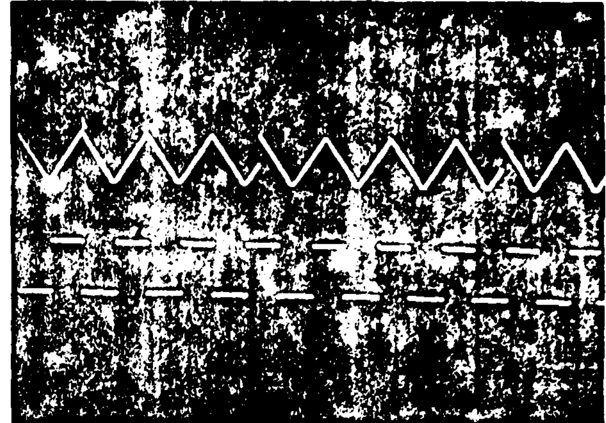


Figure 2.1 Block diagram of the autocorrelator.



(a)



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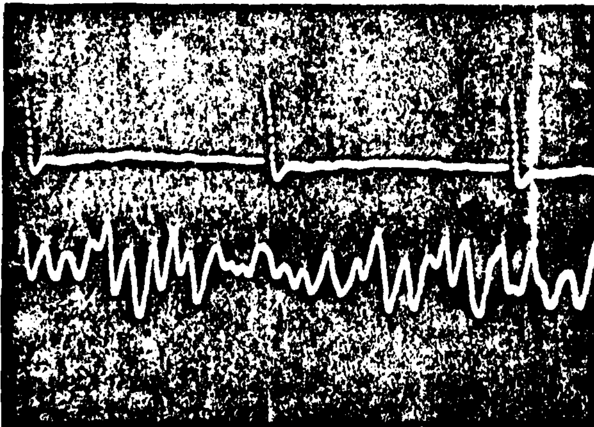

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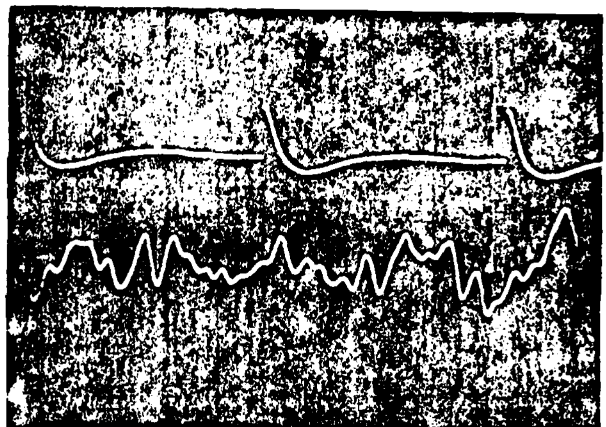


(d)

Figure 2.2 Oscilloscope photographs of the correlator computed autocorrelation functions for (a) sinusoidal, (b) square wave, (c) white noise and (d) Lorentzian noise input signals. The input signals are shown in the lower part of each figure and the autocorrelation functions are shown in the upper part of each figure.

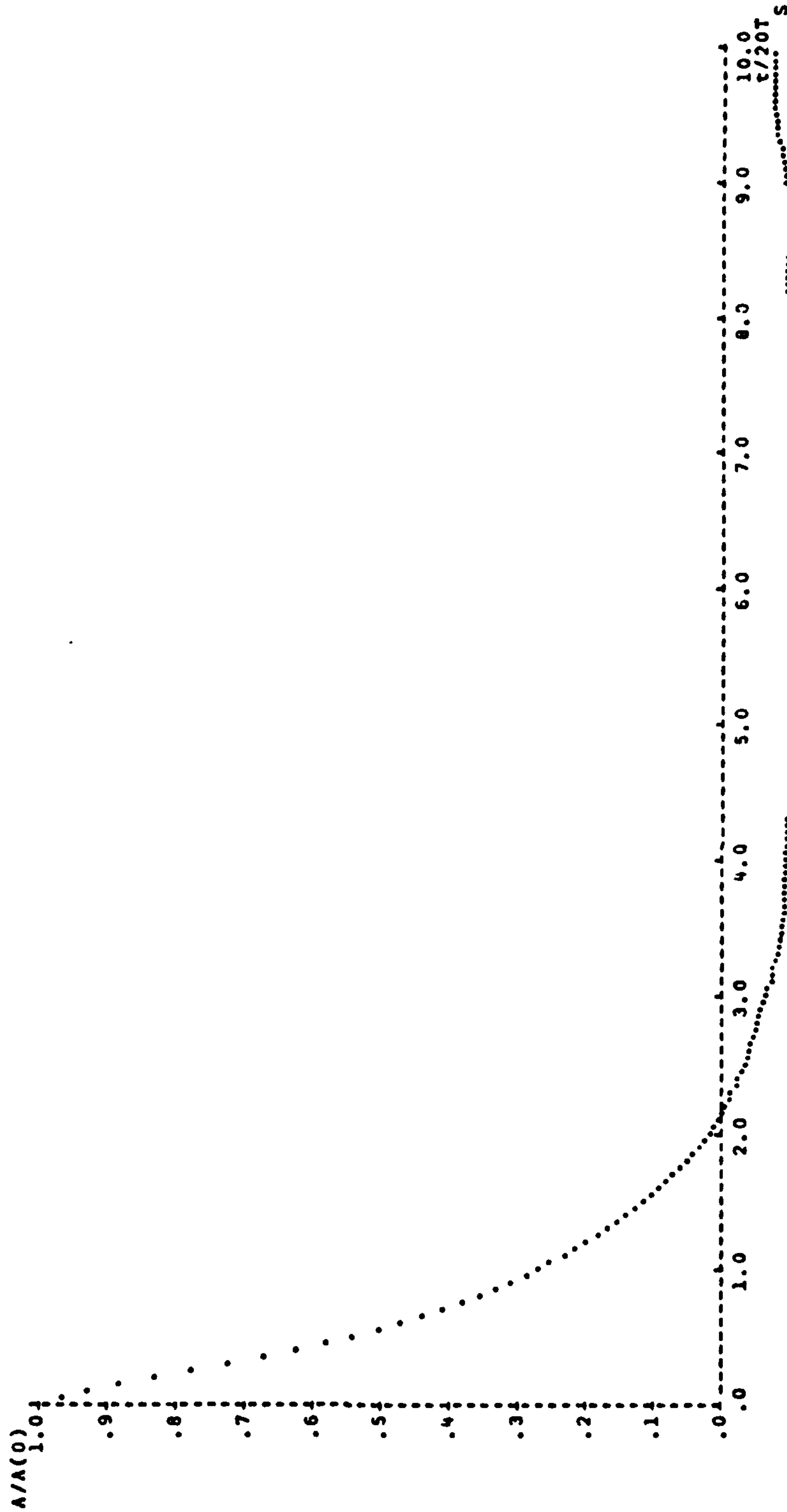
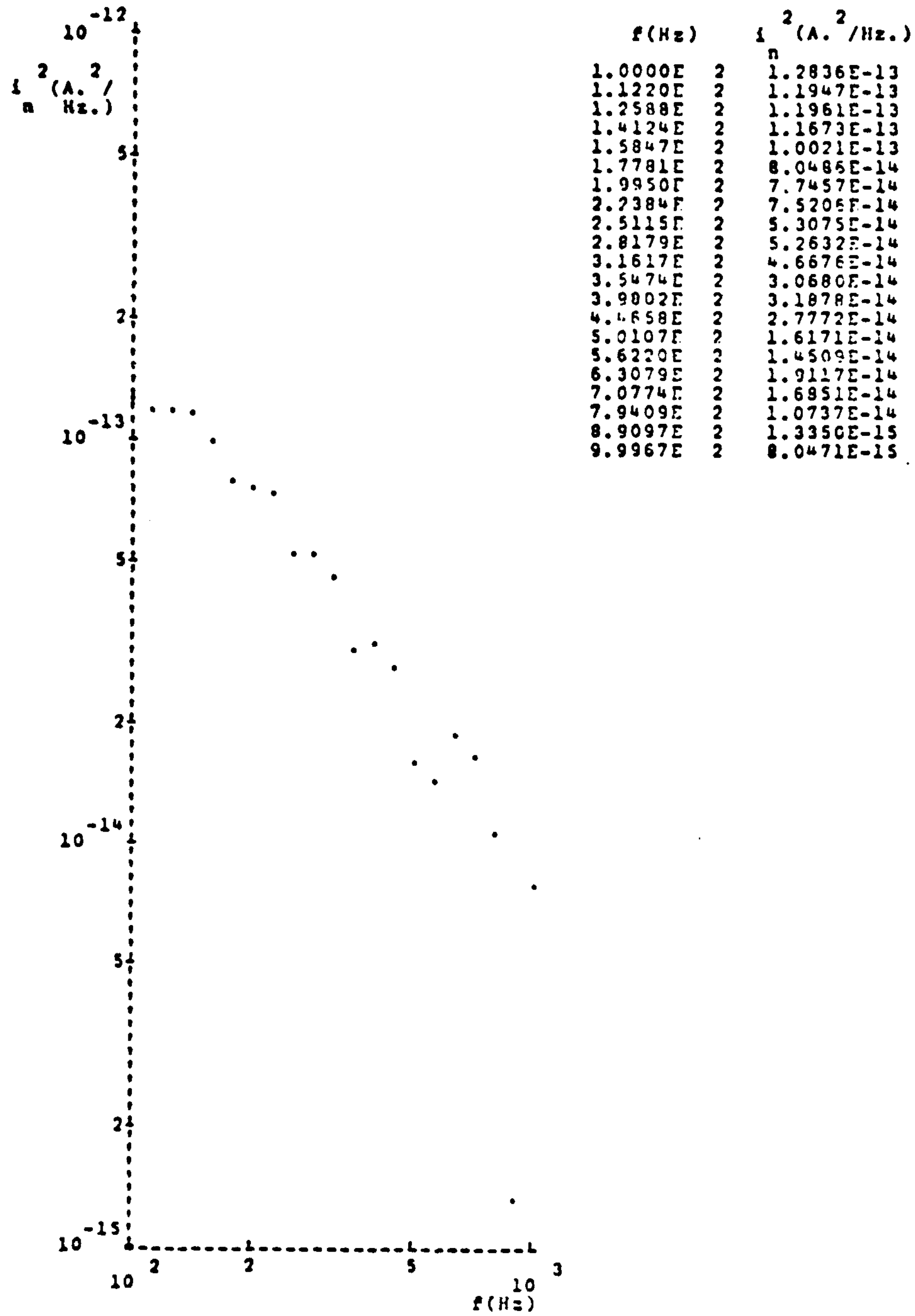


Figure 2.3 The autocorrelation function of a Lorentzian noise.



f(Hz)	i_n^2 (A.^{2}/Hz.)
1.0000E 2	1.2836E-13
1.1220E 2	1.1947E-13
1.2588E 2	1.1961E-13
1.4124E 2	1.1673E-13
1.5847E 2	1.0021E-13
1.7781E 2	8.0486E-14
1.9950E 2	7.7457E-14
2.2384E 2	7.5206E-14
2.5115E 2	5.3075E-14
2.8179E 2	5.2632E-14
3.1617E 2	4.6676E-14
3.5474E 2	3.0680E-14
3.9802E 2	3.1878E-14
4.4658E 2	2.7772E-14
5.0107E 2	1.6171E-14
5.6220E 2	1.4509E-14
6.3079E 2	1.9117E-14
7.0774E 2	1.6951E-14
7.9409E 2	1.0737E-14
8.9097E 2	1.3350E-15
9.9967E 2	8.0471E-15

Figure 2.4 The power spectrum of the Lorentzian noise shown in Figure 2.3.

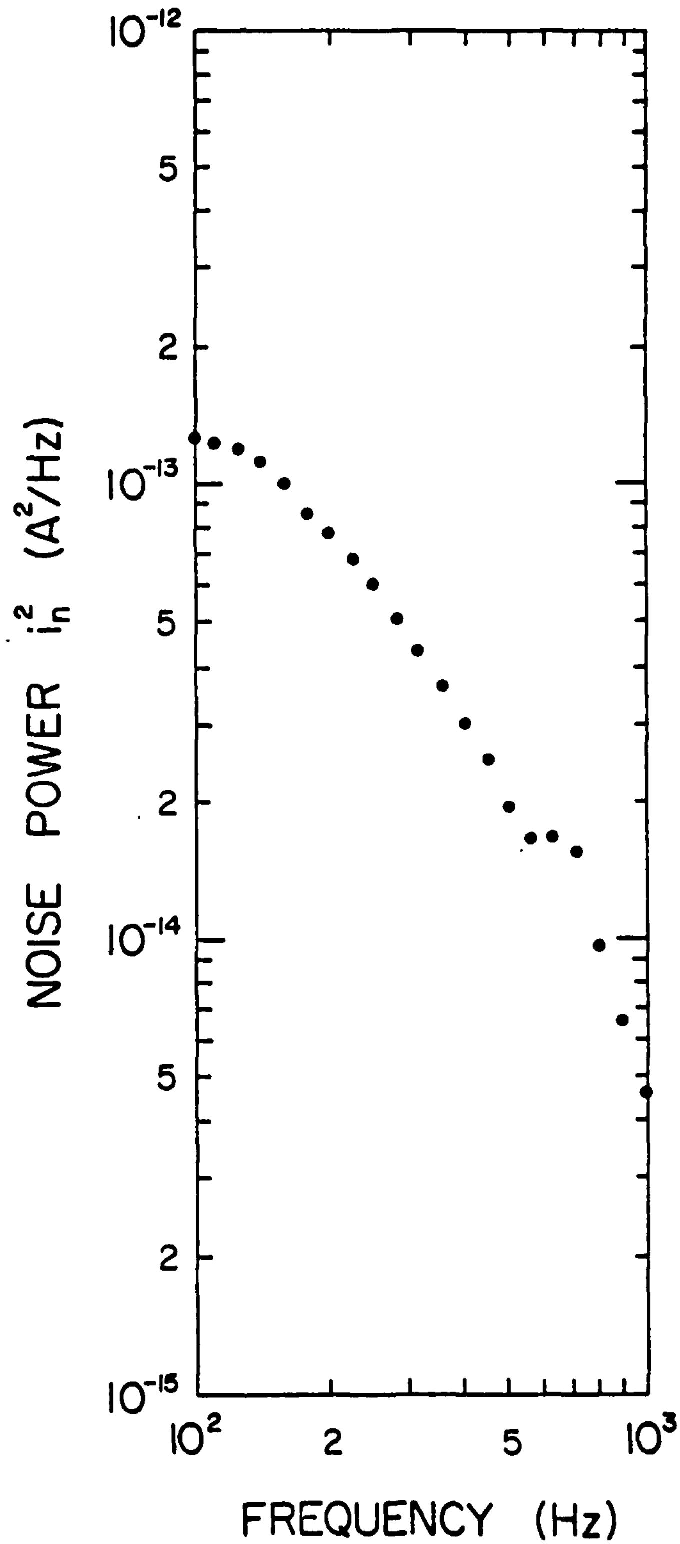


Figure 2.5 The three-point smoothed power spectrum of Lorentzian noise shown in Figure 2.4.

III. HOT ELECTRON EFFECTS IN CHARGE TRANSFER

3.1 Problem Identification

The charge transfer process in short-gate surface-channel charge-coupled devices is mainly governed by the fringing electric field which can be as high as 5×10^4 v/cm [3,4]. Electric fields of this magnitude heat up the charge carriers to kinetic energies of several thousand degrees, far above the lattice temperature. This is known as the hot electron effect [5]. One of the consequences of the hot electron or high field effects is the reduction of mobility and diffusivity due to the increased scattering rate. This could cause drift velocity saturation and limit the charge transfer rate. Trapping noise due to the interface states in CCD devices is also affected by the presence of the high electric field. The high electron temperature or the shifted electron distribution in energy in the conduction band will drastically affect and usually reduce the thermal capture rate of electrons at the interface states. The high electric field will also increase the thermal emission rate of trapped electrons at the interface states due to lowering of the trap potential barrier by the electric field.
In addition, due to the high carrier temperature and electric field, it is possible to cause interband impact generation of electron-hole pairs. This can impose limits on the gate and gap lengths and gate voltages of CCD structures. Trapping noise is considered in section IV. A computer model was developed to provide a quantitative evaluation of the hot electron effect. This is described next.

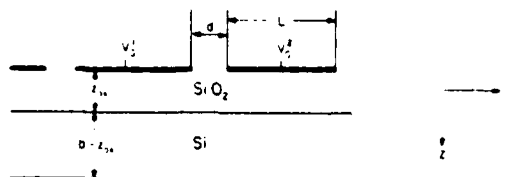


Figure 3.1 The CCD structure used in the computer model.

3.2 Theoretical Model

The structure of the transfer gates used in the model is shown in Figure 3.1. We are only concerned with charge transfer between transfer gates. The input and output stages of the CCD are not considered here. The relevant equations are:

(i) The continuity equation

$$q \frac{\partial n}{\partial t} = \frac{\partial J}{\partial x} . \tag{3.1}$$

(ii) The current equation

$$J = q \frac{\partial}{\partial x}(Dn) + q\mu nE. \tag{3.2}$$

(iii) The Poisson equation

$$\nabla^2 \phi = 0, \quad \text{for } 0 \leq z \leq z_{ox} \tag{3.3a}$$

$$\epsilon_s \nabla^2 \phi = q\,(n - N_I), \quad \text{for } z_{ox} < z < \infty \tag{3.3b}$$

Equation (3.1) through (3.3) are solved simultaneously subject to the boundary conditions given in reference [3]. Equation (3.2) is appropriate for describing hot electron phenomena and was first

derived by Stratton [6], who assumed that the scattering rate does not depend on the position x. In the case of a position dependent scattering rate, the approach of Sah and Lindholm has to be used [7].

The parameters in equations (3.1) through (3.3) are normalized according to Table 3-1. This is equivalent to setting $\varepsilon_s = 1$ and $q = 1$ in Equation (3.1) to (3.3). In Table 3-1, μ_0 and D_0 are the zero field mobility and diffusivity. The numerical values of the parameter used in the calculations are also given in Table 3.1.

Table 3.1 Definition of Normalized Symbols

Parameter	Symbols	Normalized to	Value
Length	x, z	$\lambda_D = \sqrt{\varepsilon_s k_B T_L / e^2 N_A}$	1.30E+3 A
Time	t	$\lambda_D^2 e / \mu_o k_D T_L$	9.34E-12 s
Potential	ϕ	$k_B T_L / e$	2.58E-2 V
Concentrations	n, p, N_I	$N_A \lambda_D$	1.30E+10 cm^{-3}
Electron Temp.	T	T_L	3.00E+2 K
Mobility	μ	μ_o	7.00E+2 cm^2/V-s
Diffusivity	D	D_o	1.81E+1 cm^2/s

To further simplify the calculation, we approximate the inversion layer by a sheet of electrons. Thus, Equations (3.3a) and (3.3b) become

$$\nabla^2 \phi = 0 \qquad 0 \le z < z_{ox} \qquad (3.4a)$$

$$\nabla^2 \phi = qn(x)\delta(z) \qquad z_{ox} \le z < b \qquad (3.4b)$$

$$\phi = 0 \qquad b \le z < \infty \qquad (3.4c)$$

Here, $b = z_d + z_{ox}$ and $z_d(t)$ is the thickness of the silicon surface space charge layer under the gate where the charges are transferred. The advantage of Equation (3.4) over (3.3) is that (3.4) can be

solved using Fourier expansion of ϕ instead of the finite difference method so that substantial saving in computing time is achieved. Our results for the fringe field have been compared with the exact results of Carnes, Kosonocky and Ramberg [8]. It is found that the minimum fringe field as obtained from Equation (3.4) agrees within 20 percent with the exact results from using equation (3.3). Elsewhere, the fringe field values are closer to the exact solution than the minimum value case. Two additional simplifications are used. They are described as follows. The potential between the gates at $z = 0$ was assumed to vary linearly. Therefore, potential barriers do not exist between the gates. This approximation is good for gap length $\leq 1 \mu m$ [9] as considered here. For larger d, the approximation generally breaks down. The second simplification is that $z_d(t)$ is taken to be a constant parameter. The value for $z_d(t)$ does not affect the results significantly for short-gate CCD's. The results presented change less than 2 percent if z_d is varied by a factor of two. The actual values of z_d is determined by N_I, V_G and $n(x,t)$.

In order to obtain the numerical solutions of the system of equations given by (3.1), (3.2) and (3.4), the electric field dependencies of the mobility and diffusivity must be known. The diffusivity is given by $D = (k_B T_e/q)\mu$, where $T_e = T_e(E)$ is the electron temperature of the Maxwellian distribution and $\mu = \mu(E)$. The diffusivity does not depend strongly on electric field since a decrease of mobility with electric field is compensated for by an increase of electron temperature. Thus in our calculations, we take $D(E) = D_0$, the zero electric field diffusivity. This is a good approximation for the diffusivity value measured in the bulk [6, 10, 11]. Elaid et al [4]

used a diffusivity given by $D = (k_B T_L/q)\mu$ where T_L is the lattice temperature. This clearly underestimated the diffusivity when $T_e >> T_L$.

The electric field dependence of mobility can be calculated from the following power balance equation where ε equals electron kinetic energy

$$\langle J\varepsilon \rangle = \langle \partial\varepsilon/\partial t \rangle n \quad (3.5)$$

The rate of energy loss to the lattice $\langle \partial\varepsilon/\partial t \rangle$ for low electric field $T_e \approx T_L$ and for $T_L \approx 300$ K may be approximated by the two-dimensional formula, since we approximated the electron distribution in the silicon surface space charge layer by a two-dimensional sheet as in Equation (3.4b). This equation was given by [12]

$$\langle \partial\varepsilon/\partial t \rangle \approx 2.8\text{x}10^{-9} \; [(T_e/T_L - 1] \quad \text{Watt} \quad (3.6)$$

where the bulk electron-intervalley phonon coupling constant is used. In the region of high electric field when $T_e > 3\ T_L$, an alternate formula is used. The high field formula is

$$\langle \partial\varepsilon/\partial t \rangle \approx 9.64\text{x}10^{-9} \sqrt{T_e/T_L} \quad \text{Watt} \quad (3.7)$$

This is a three-dimension formula for energy loss to intervalley phonons. The electron-intervalley phonon coupling constant from Jacoboni et al [11] was used. The spatial dependencies of electron temperature, T_e, are computed from Equation (3.5), (3.6), or (3.7).

In addition, we need the dependence of mobility on electron temperature in order to obtain its electric field dependence. The explicit formula is a complicated integral over the Maxwellian distribution, $\exp(-E/k_B T_e)$, where E is the kinetic energy of the electron, since both the acoustic and intervally phonon scattering

are important in determining the momentum or mobility relaxation time. This is further complicated by scattering from impurities and oxide-silicon interface imperfections. To use the explicit formula would increase the computation time by one order of magnitude. Instead the following approximation is used for $\mu(E)$

$$\mu = \mu_0 \, [1 + (E/E_c)^2]^{-1/2} \tag{3.8}$$

Here E_c is the critical field. This is a good approximation at low field when $E < E_c$ and the electric field effects on charge transfer and noise are not important. It also predicts the observed velocity saturation at high electric field, when $E >> E_c$.

The critical field was determined by numerical estimates which showed that T_e at $E = E_c$ is about $2T_L$. Thus taking $D = D_0$, $T_e = 2T_L$, and using Equations (3.2), (3.5), (3.6) and (3.8), we find

$$E_c \simeq -(\text{sign } E)\cdot(k_B T_L/\sqrt{2}qn)\cdot(\partial n/\partial x) + \sqrt{(k_B T \partial n/\partial x)^2/2qn + 2.8\text{x}10^{-9}/(q\mu_0/\sqrt{2})} \tag{3.9}$$

For very high surface potential values, E_c also depends on the surface potential [14]. This dependence is not considered here. Energy transport in the x-direction is neglected. This is important only for extremely large values of $\partial T_e/\partial x$.

The system of equations was solved by the following iteration procedure. The Laplace solution of the electrostatic problem is first obtained by setting $n(x) = 0$ in Equation (3.4), and using the Fourier series expansion of the potential given by

$$\phi^0(x,z,t) = \sum_{m=1}^{\infty} \phi_m^{\pm}(t)\cdot\exp(\pm k_m z)\cdot\sin(k_m x) \tag{3.10a}$$

This is similar to the method of reference [8] but it differs in that they considered only the case of $z_d \to \infty$. The solution of the Poisson equation, $\nabla^2\phi^1 = (q/\varepsilon_s)n(x,t)\delta(z)$ is added, which is approximated by [3, 14]

$$\phi^1(x,z,t) \simeq -qn(x,t)\,\frac{(z_{ox}/\varepsilon_{ox})\,(z_d/\varepsilon_{si})}{(z_{ox}/\varepsilon_{ox}) + (z_d/\varepsilon_{si})} \tag{3.10b}$$

$$\simeq -qn(x,t)\cdot(z_{ox}/\varepsilon_{ox}) \tag{3.10c}$$

The approximation given by Equation (3.10c) holds if $(z_{ox}/\varepsilon_{ox}) \ll (z_d/\varepsilon_{si})$. This approximation reduces the transfer time by 5 percent at most but it considerably reduces the computation time since the boundary $z = h$ used in the charge-free solution, $\phi^0(x,z,t)$, is then independent of $\phi^1(x,z,t)$. The potential is given by

$$\phi(x,z,t) = \phi^0(x,z,t) + \phi^1(x,z,t) \tag{3.11}$$

In carrying out the calculations, it was necessary to take more than 400 terms in the Fourier series expansion, Equation (3.10a), to obtain 0.1 percent accuracy in the potential, ϕ. The electric field is then calculated from $E = -\partial\phi/\partial x$ using the solution given by Equation (3.11). This is used in Equations (3.1) and (3.2) which are then solved by the finite difference method as described in [4]. The electron density at the next time step, $n(x,t + \Delta t)$ is then obtained. It is used in Equation (3.10c) to give a new $\phi^1(x,z,t+\Delta t)$, and a new total potential, $\phi(x,z,t+\Delta t)$. The new potential is then used to calculate the electric field and electron density for the next time step. This procedure is repeated until all the charges in the initial distribution $n(x,t=0)$ are transferred from one gate to the adjacent gate. This requires about 3×10^4 normalized time steps.

In several calculations, the final steady-state carrier distribution or potential, $\phi^1(x,z,t=\infty)$, was used as the initial carrier distribution. However, an approximate initial carrier distribution was found to give better that 5 percent accuracy in the computed transfer time for the smallest gap and gate used which are 0.5 and 1 μm respectively. The accuracy is better for the other parameters and or the transfer times of larger gap and gate lengths. This approximate intial charge distribution has an edge distribution of $n(x) = 2n(0)/[1 + \exp(x/\Delta)]$ where $\Delta = (L+d)/30$ and $x = 0$ is the edge of the gate. Most of the numberical computations made use of this initial charge distribution in order to reduce the computation time by a factor of two. Finally, it should be pointed out that it is incorrect to use $\mu = \mu(E)$ for all times as was done in [4]. As $t\to\infty$, Equation (3.9) gives a very large E_c so that Equation (3.8) gives $\mu = \mu_0$ at the end of the transfer when $J = 0$ and $T_e \to T_L$.

3.3 Numerical Results and Discussion

The following values for the various device parameters were used in the numerical calculations: $z_{ox} = 10^{-5}$ cm, $d = 0.5\times10^{-4}$ cm. $T_L = 300$ K, $\varepsilon_{Si} = 11.7\varepsilon_0$ and $\varepsilon_{ox} = 3.9\varepsilon_0$, $z_d = b - z_{ox} = 10^{-4}$ cm, $\mu_0 = 700$ cm^2/v-s, $D_0 = 18.1$ cm^2/s. The saturation velocity was 4×10^6 cm/s and the difference in gate voltage between adjacent electrodes during transfer is 10 V.

Figure 3.2 shows the transferred charge density as a function of position along the interface at four times. Figure 3.3 shows the charge density as a function of time at three positions. Figure 3.4 shows the coefficient η versus transfer time. η is defined as the ratio of charge left behind under the storage gate to the initial charge

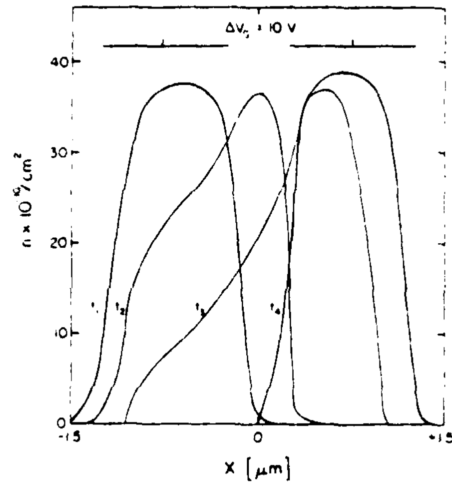


Fig. 3.2 Transferred charge density as a function of position along the interface x. t_1=0.0025ns, t_2=0.0125ns, t_3=0.0275ns, t_4=0.0775ns.

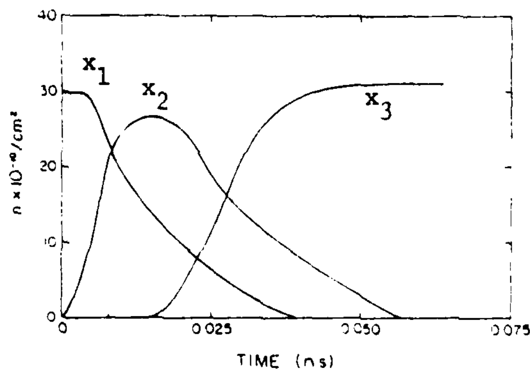


Fig. 3.3 Transferred charge density as a function of time. x_1=-0.75μm, x_2=0.00μm x_3=+0.75μm

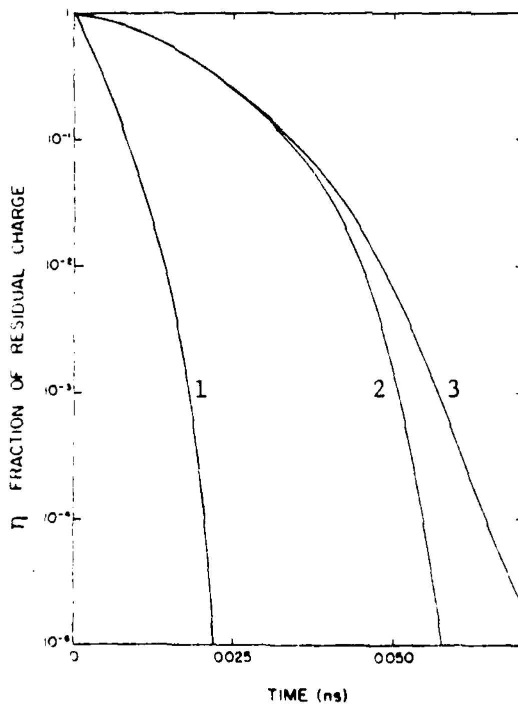


Fig. 3.4 Fractional residual charge under the gate for $n=2.5\times10^{11}$ cm^{-2}.

Curve 1 $\mu = \mu_0$
$D = D_0$

Curve 2 $\mu = \mu(E)$
$D = (k_B T_L/q)\mu(E)$

Curve 3 $\mu = \mu(E)$
$D = D_0$

under the same gate when no interface states are present. Curve 1 neglects the heating of the charge carriers completely. Curve 2 is calculated after using the formulation of reference [4] where hot carrier diffusion is not included properly, and Curve 3 is calculated as described in the previous section using a constant diffusivity $D = D(E=0) = D_0$. The largest effects are caused by the mobility reduction as already noted in reference [4]. Figure 3.5 shows the electron temperature under two transfer gates of 10^{-4} cm.

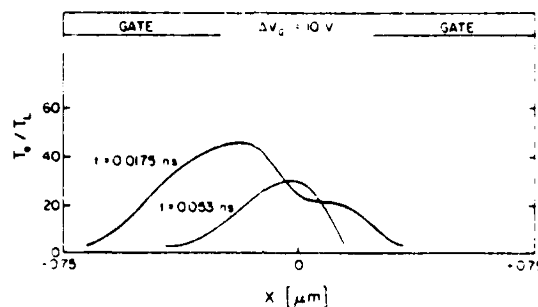


Figure 3.5 Electron temperature below the transfer gate for a gate length of 1 μm at two transfer times. Carrier concentration is $n=2.5x10^{11}cm^{-2}$.

At thermal equilibrium, the mass action law requires that $e^0_{ns} = c^0_{ns}N_c\exp(- /k_BT)$. But $e^0_{ns} = a^0\exp(- /k_BT)$ so that $a^0/c^0_{ns} = N_c = 2.5x10^{19}(T_L/300)^{1.5}cm^{-3}$. At high electric fields such as those encountered in the CCD fringe field region (10^5V/cm), the thermal emission rate increases only slightly which can be largely accounted for by lowering of the trap potential. The field dependence of the frequency factor 'a' is expected to be weak [15]. Thus the main hot electron effect is the reduction of the capture rate. This effect can be characterized by replacing the lattice temperature by the electron

temperature, i.e. $a/c_{ns} = 2.5\times10^{19}(T_e/T_L)^{1.5}$. This dependence can be understood in terms of Lax's cascade theory [16]. Using the Maxwellian distribution, this formula fits the experimental observation in bulk silicon quite well.

The electric field and the carrier temperature are generally complicated functions of space and time. The time dependence of the electric field near the end of the gate where the charge is transferred to the next gate is shown in Figure 3.6 for three carrier densities.

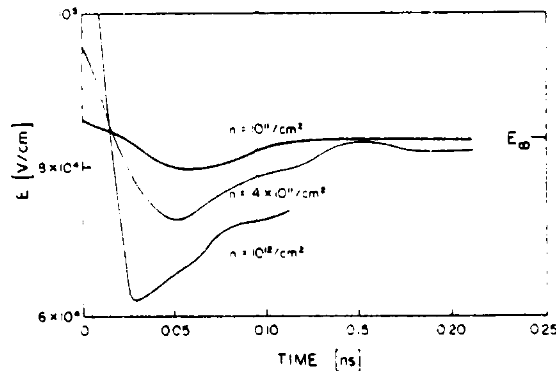


Figure 3.6 Electric field versus time during transfer at the end of the transfer gate. Gate length is L = 2 μm

These results show that the electric field is nearly independent of time only for very small carrier density, n. For this case, an average capture rate can be computed from

$$\bar{c} = L^{-1}\int_0^L [c_{ns}(E)/c_{ns}(0)]dx \qquad (3.12)$$

which is plotted in Figure 3.7 as a function of gate length. For large L, $\bar{c}$ is close to unity since the electron temperature is high only in a small region near the gap between the gates. For small L, $\bar{c}$ is less than unity. The decrease in the electron capture rate at small L causes a reduction in both the interface trapping noise and transfer inefficiency due to carrier trapping by interface states.

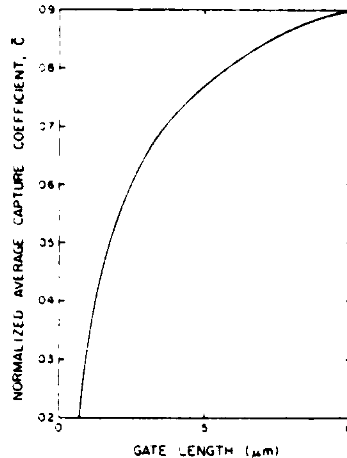


Figure 3.7 Normalised average caputre coefficient versus the gate length. Parameters used are given in the text.

3.4 Summary of Results

In summary, the heating of the charge carriers in CCD's affects the device performance as follows:

(1) The transfer speed is considerably reduced because of the reduction of the mobility as already pointed out by Elsaid et al [4] and shown in Figure 3.4. Diffusion transfer becomes important only near the end of the transfer period.

(2) The noise and the transfer inefficiency due to carrier trapping by interface states are reduced due to decrease in electron capture rate which is only important at short gate length.

One of the major assumptions in our calculations was that the charge carrier heating is stationary, i.e. the time involved is longer than the energy relaxation time which was found to be in the order of 10^{-12} s both experimentally and theoretically for silicon at high electric field [11]. In Figure 3.5, we see that for gates of 1 μm this condition is barely valid. The calculation for non-stationary heating is much more involved. One expects a large range of ohmic mobility and therefore faster transfer [17].

IV. TRAPPING NOISE IN CHARGE COUPLED DEVICES

4.1 Problem Identification

Trapping noise due to random transitions of electrons and holes at interface states has been investigated by several authors [18-21]. The mean square fluctuation of charge per unit area was given by

$$<q_{ss}^2>/A = qk_B TN_{TTS} \ell n2. \tag{4.1}$$

N_{TTS} is the areal density of interface states per eV averaged over the energy gap. A is the active device area. q is the elctron charge ($1.6x10^{-19}$ Coulomb). k_B is the Boltzmann constant. T is the absolute temperature. Equation (4.1) is the noise accquired by a charge packet in a single transfer and it is based on the following assumptions.

(i) Only thermal emission of trapped electrons and holes are included. Random thermal capture events are ignored.

(ii) Time and space variation of electron density during the charge transfer are neglected.

(iii) Complete charge transfer is assumed.

(iv) Interface states are assumed filled to the equilibrium level.

The last assumption was removed by Carnes and Kosonocky [21] whose numerical solutions for high clock frequencies can be approximated by the following equation.

$$<q_{ss}^2>/A \approx qk_B TN_{TTS} \ell n2(c_{ns} n/f_{cl}) \tag{4.2}$$

This result has an additional factor, $(c_{ns} n/f_{cl})$, over the simple solution given by Equation (4.1). This is the fraction of the interface states which are filled when thermal emission begins.

In this section, the other three neglected factors listed above are analyzed using the space-time dependence obtained in section III.

4.2 Theoretical Analysis

When the assumptions are all removed, the simplified mean square fluctuation of charge per unit area, given by Equation (4.1), is generalized to the following approximate form.

$$\langle q_{ss}^2\rangle/A = qk_BTN_{TTS}F \tag{4.3}$$

where the factor, F, has three parts given by

$$F = F_1 + F_2 + F_3 \tag{4.4}$$

They are defined below.

$$F_1 = F_{1c}\, F_{1e} \tag{4.5}$$

$$F_{1c} = \left\{\exp\left(-\int_{t_{on}}^{t_{of}} c_{ns} n dt'\right)\right\}\cdot\left\{1 - \exp\left(-\int_{t_{on}}^{t_{of}} c_{ns} n dt'\right)\right\}$$

$$F_{1e} = \int_{\varepsilon_1}^{\varepsilon_2} d\varepsilon [1 - n_{TS}(t_{on})/N_{TTS}]\cdot\left\{\exp\left(-2\int_{t_{of}}^{t_f} e_{ns} dt'\right)\right\}$$

$$F_2 = \int_0^{\varepsilon_1} d\varepsilon \int_{t_{on}}^{t_{of}} c_{ns} n dt \cdot \exp\left(-2e_{ns}(t_f - t)\right) \tag{4.6}$$

$$F_3 = \int_{\varepsilon_1}^{\varepsilon_2} d\varepsilon \int_{t_{of}}^{t_f} e_{ns} n_{TS} dt \cdot \left\{\exp\left(-2\int_t^{t_f} e_{ns} dt'\right)\right\} \tag{4.7}$$

Here, $\varepsilon = E/k_BT$. ε_2 is roughly the intrinsic Fermi level below which the interface state levels are assumed to be all filled at all time. c_{ns} and e_{ns} are the thermal capture and emission rates of electrons at the interface state whose energy level is E_s or $\varepsilon_s = E_s/k_BT$. $n = n(x,t)$ is the instantaneous electron concentration at position x. The integration time

limits are defined as follows. t_c is the time when the charge begins to move into the receiving gate. t_{on} is the time when the charge under the receiving gate exceeds the background charge (such as that from a fat zero) already under the receiving gate before t_c. $t_c+(2f_{cl})^{-1}$ is the time when the charge under the receiving gate has reached a maximum and begun to decrease or spread out to the next gate. f_{cl} is the clock frequency. t_{of} is the time when the most of the charges have been transferred to the next gate from the receiving gate such that the charge under the receiving gate has dropped to the background level. $t_c+(f_{cl})^{-1}$ is the end of one charge transfer cycle. t_f is approximately $t_c+(f_{cl})^{-1}$.

The energy E_1 or $\varepsilon_1=E_1/k_BT$ separates the faster interface states from the slower interface states. Thus, the states between the conduction band, $E_C=0$, and E_1 have larger thermal emission rates $e_{ns}(E_s<E_1)$ than those between E_1 and the intrinsic Fermi energy, E_2. This energy boundary which divides the shallower and faster states from the slower and deep states is somewhat arbitrary. A rough definition is

$$e_{ns}(E_1) = c_{ns}\langle n(t_{of})\rangle \qquad (4.8)$$

where the electron concentration is averaged over the gate at $t=t_{of}$ and the thermal equilibrium or mass action law relationship

$$e_{ns}(E_1) = c_{ns}(E_1)N_C\exp(-E/k_BT) \qquad (4.9)$$

is used. N_C is the effective density of states of the conduction band.

The Equation (4.3) with the three factors is derived from the rate equation of electron density trapped at the interface state,

$$dn_{TS}/dt = c_{ns}n(N_{TTS} - n_{TS}) - e_{ns}n_{TS} + r_s(t) \qquad (4.10)$$

where $r_s(t)$ is a random generating function. Using the small-signal expansion for small amplitude noise, $n_{TS}(x,t) = n_{TS}^o(x,t) + \delta n_{TS}(x,t)$,

the solution for the fluctuating part of the trapped electron density is

$$\delta n_{TS}(x,t) = \int_0^t dt' r_s(t') \cdot \exp\left(-\int_0^{t'} dt''[c_{ns}n(x,t'') + e_{ns}]\right) \quad (4.11)$$

Taking the ensemble average over the active area of the device, the trapped charge fluctuation is then given by

$$\langle q_{ss}^2(t_f)\rangle/A = qk_B T N_{TTS} \int_0^{\varepsilon_G} d\varepsilon \int_{t_c}^{t_f} dt[(N_{TTS} - n_{TS}^o)c_{ns}n + n_{TS}^o e_{ns}] \times$$

$$\times \exp\left(-2\int_t^{t_f} dt'(c_{ns}n + e_{ns})\right) \quad (4.12)$$

where use is made of

$$\langle r_s(t_1) r_s(t_2)\rangle A = [(N_{TTS} - n_{TS}^o)c_{ns}n + n_{TS}^o e_{ns}]\delta(t_1 - t_2) \quad (4.13)$$

4.3 Summary and Qualitative Interpretation

The third factor, F_3, given by Equation (4.7) reduces to the simple result given by Equation (4.1) for constant N_{TTS} and long transfer time, i.e.

$$F_3 \simeq \ell n2 \quad (4.14)$$

This is the case where the major contribution of noise comes from electron trapping at the deeper interface levels. If the interface state density depends on energy, then

$$F_3 \simeq \ell n2 \cdot [N_{TTS}(E_{max})/N_{TTS}] \quad (4.15)$$

where

$$E_{max} = k_B T\ [c_{ns} N_C (t_f - t_{of})/\ell n2]$$

and N_{TTS} is the average over the energy gap as defined previously and it cancels out the same factor in Equation (4.3).

If the electron density is high or the width of the charge packet is small, i.e. if $c_{ns}n(t_{of}-t_{on}) < 1$, then Equation (4.15) is diminished by this factor to give

$$F_3 \simeq \ln 2 \cdot [N_{TTS}(E_{max})/N_{TTS}] \cdot c_{ns}n(t_{of}-t_{on}) \qquad (4.16)$$

This differs from Equation (5.2) slightly because electron capture, which is incomplete in the time interval $t_{of}-t_{on}$, can continue until the charge packet has completely transferred out of this gate.

The factor F_1 is associated with incomplete filling of the interface state levels. When all the levels are filled, $n_{TS}(t_{on})=N_{TTS}$, and $F_1=0$. Due to incomplete filling, the density of the occupied and unoccupied interface states will both fluctuate over the entire active device area and contribute noise, but at each interface state, the densities are correlated since $n_{TS}(x,t) + [N_{TTS}(x) - n_{TS}(x,t)] = N_{TTS}(x)$. The factor F_{1c} comes from the filled traps and F_{1e} from empty traps.

The second factor, F_2, comes from the random fluctuation of the capture transition into the shallow energy level traps between E_C and E_1. This noise can become dominant when $e_{ns}(t_{of}-t_{on})$ is large and when the electron density is high. At low electron concentrations, its contribution may be comparable to the noise due to random emission and incomplete filling.

V. SMALL-SIGNAL IMPEDANCE OF INTERFACE STATES IN CCD OR MOS DEVICES

5.1 Problem Identification

The major cause of transfer inefficiency in SCCD operated at medium frequencies is the trapping of minority carriers by the interface states located at the Si-SiO_2 interface [22]. The introduction of background charge or fat zero eliminates most of the "fixed loss" due to interface state trapping under the gate. The major source of transfer inefficiency then comes from interface states at the edges of the transfer electrodes. This occurs because the area of interface over which a charge packet is stored is larger than that occupied by background charge [23]. This is sometimes referred to as the non-linear loss since the loss is a function of signal size [24]. Another major source of transfer inefficiency is the trapping of minority carriers by the interface states in the gap between the electrodes. This can be reduced by overlapping the gates of CCD [25]. The role of interface states in causing trapping noise was studied in detail in the previous sections, which showed that the following interface state parameters are required to predict the noise and trapping inefficiency: the density of the interface states, $N_{TTS}(E)$, and the thermal emission and capture rates of electrons (for n-channel CCD), $e_{ns}(E)$ and $c_{ns}(E)$, all as a function of energy. In this section, we describe our effort to use the small-signal equivalent circuit model to obtain these interface states parameters.

5.2 Small-signal Equivalent Circuit Models for an MOS Capacitor with Interface States

The Shockley-Read-Hall (SRH) model of thermal generation-recombination-trapping at an imperfection center has been applied to one-level interface states by Sah [26]. The resulting equivalent circuit is shown in Figure 5.1. For the interface branches, C_{ss} is the trapped charge storage capacitance. G_{ssp} is the hole capture conductance and G_{ssn} is the electron capture conductance. They are defined as follows:

$$C_{ss} = \frac{q^2}{k_B T} N_{TTS} f_{ss} (1-f_{ss}) \tag{5.1}$$

$$G_{ssn} = \frac{q^2}{k_B T} c_{ns} N_S N_{TTS} (1-f_{ss}) \tag{5.2}$$

$$G_{ssp} = \frac{q^2}{k_B T} c_{ps} P_S N_{TTS} f_{ss} \tag{5.3}$$

where N_{TTS} is the areal density of a single-level interface state. f_{ss} is the electron occupancy factor of these states. c_{ns}, c_{ps} are the electron and hole capture rate constants in cm^3/sec respectively. N_S, P_S are the semiconductor electron and hole volume concentration in #/cm^3 at the interface respectively. C_o is the oxide capacitance.

Neglecting bulk generation-recombination-trapping centers, one can simplify the circuit in Figure 5.1 to one-lump equivalence as shown in Figure 5.2 for an n-type substrate device biased into accumulation [26]. C_n is the electron storage capacitance in the bulk. It is given by

$$C_n = \frac{q^2}{k_B T} \int_0^\infty N dx \tag{5.4}$$

Similarly, if the device is biased into inversion and the interface edge effect is neglected, the equivalent circuit of Figure 5.1 can be

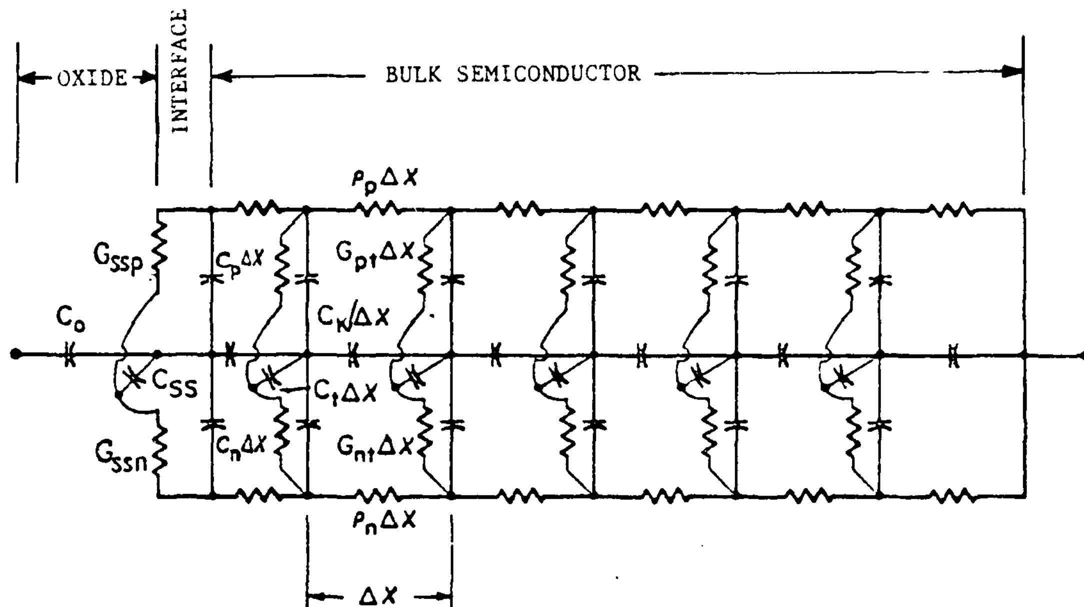


Figure 5.1 The small-signal equivalent circuit for an MOS capacitor deveoped by Sah [26] for a single-level interface state and a single-level bulk recombination center.

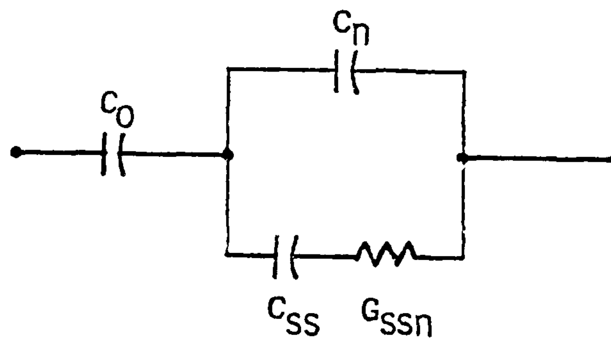


Figure 5.2 Simplified one-lump equivalent circuit for an n-type MOS capacitor with surface accumulation of majority carriers.

simplified to that shown in Figure 5.3 [26]. Y_d is diffusion admittance in the bulk and is given by

$$Y_d = \frac{q^2}{k_B T} D_p P_B (1+\omega\tau_{po})^{1/2}/(D_p\tau_{po})^{1/2} \qquad (6.5)$$

τ_{po} is the minority carrier lifetime. P_B and D_p are the minority carrier concentration and diffusivity respectively. Under some conditions, Y_d is much smaller than other circuit elements and can be treated as an open circuit.

In practice, interface states are not single-level but are distributed in energy and space. The equivalent circuit for interface states distributed in energy can be described by a parallel array of R-C branches, one for each energy as shown in Figure 5.4a [26, 27, 28]. This array can be simplified by integrating over bandgap energies to give the series equivalent circuit of Figure 5.4b. Asymptotic formulae of C_{se} and G_{se} for $\omega\tau_{ss}$<<1 and $\omega\tau_{ss}$>>1 were derived in reference [28], where $\tau_{ss} = C_{ss}/[G_{ssn}(1-f_{ss})]$ in the case of an n-type accumulation region. At very low frequencies with $\omega\tau_{ss}$<<1, we have
with $\omega\tau_{ss}$<<1, we have

$$C_{se} = q^2/\rho_{TTS} \qquad (5.6)$$

$$G_{se} = 2q^2\rho_{TTS}/\tau_{ss} \qquad (5.7)$$

Equation (5.6) comes from the interface state branch only and is valid for all energy levels of the interface states. Therefore it can be used to obtain ρ_{TTS} from experimental data as long as C_{se} of the interface state branch can be extracted from the data.

The effect of interface states distributed into the oxide has been studied using a two-step model, consisting of SRH transitions between

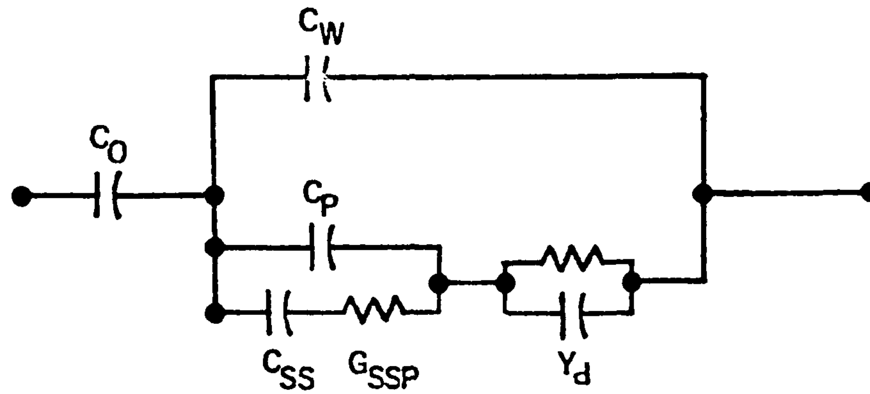


Figure 5.3 Lumped equivalent circuit model for an n-type MOS capacitor biased into inversion range but neglecting the interface edge effect to be illustrated in Figure 5.5.

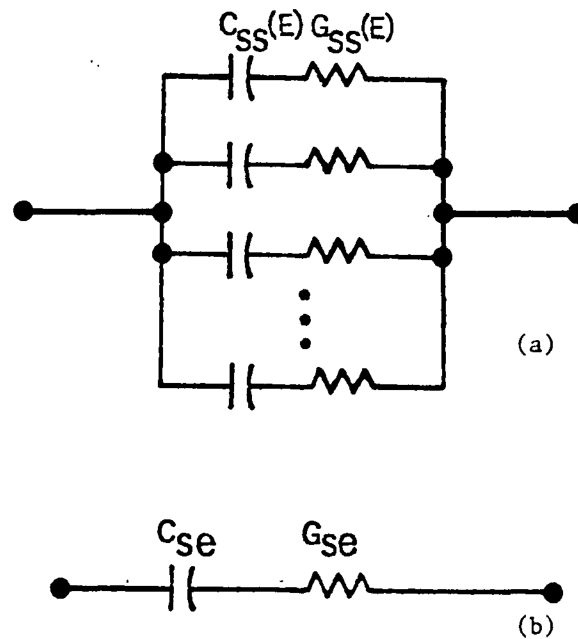
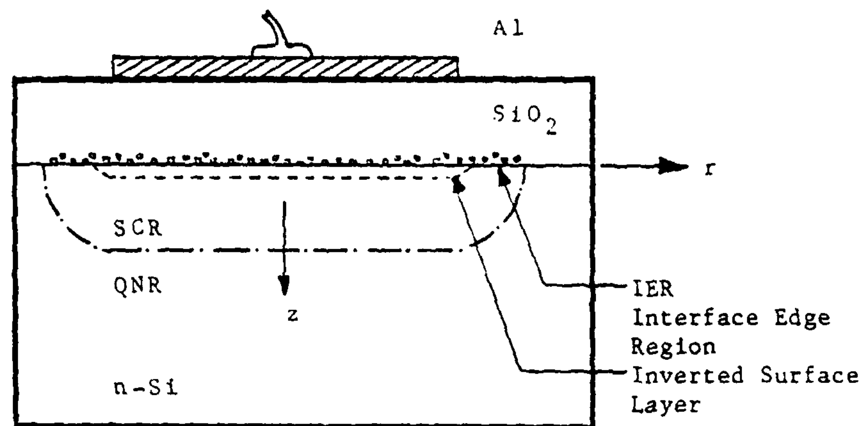


Figure 5.4 Lumped equivalent circuit model for interface states distributed in energy. (a) Each series branch corresponds to states at one energy. (b) A one-lump equivalent circuit for the the distributed circuit shown in figure (a).

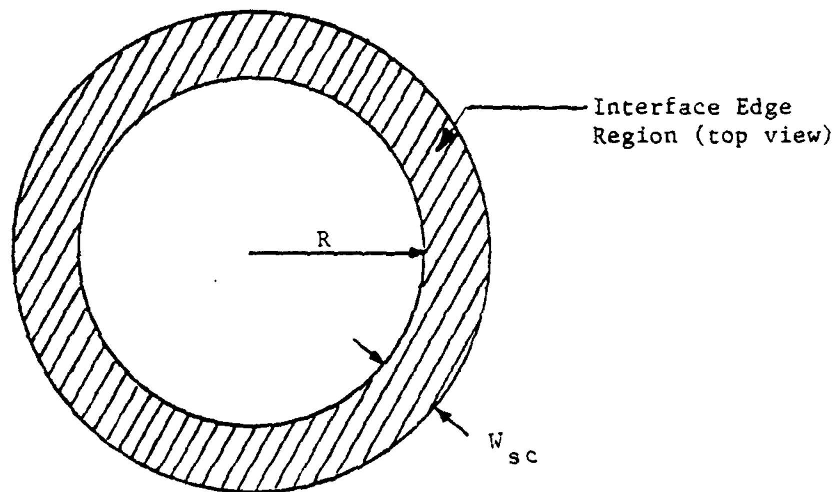
the band and the interface states and elastic tunneling transitions between the interface states and the oxide traps distributed in the oxide. The effect from this distributed tunneling model is most significant on the frequency dispersion of MOS capacitance and conductance at low frequencies, especially for the equivalent series conductance G_{se} which drops at low frequencies.

The experimental data on frequency dispersion for the device biased into inversion cannot be explained by the simple model shown in Figure 5.3 since the minority carrier diffusion admittance is so small that the interface branch could hardly have any effect on the frequency dispersion of the device admittance. Instead, the interface edge region (IER), as shown in Figure 5.5, must be included in the model. A circular geometry is used to simplify the analysis. A two-dimensional equivalent circuit model is formed by adding a transverse branch (in the radial direction) which accounts for the interface edge effect. This is shown in Figure 5.6a. The z direction represents the usual MOS capacitor branch as in Figure 5.3. The transverse or r direction represents the IER branch which is essentially like the usual MOS capacitor branch but with radially distributed interface states in the space charge region of the IER.

The circuit elements for the transverse branch are defined in Table 5.1. G_p^t is treated as a short while C_n, G_{ssn} and G_n^t are treated as open because the semiconductor surface under the gate is inverted. The resulting circuit is shown in Figure 5.6b which is further simplified to Figure 5.6c since G_{ssp} is usually much larger than ωC_{ss} and since C_p in weak inversion is much smaller than C_{ss}. The circuit in Figure 5.6c



(a)



(b)

Figure 5.5 MOS capacitor structure. (a) The cross-sectional view showing the interface edge region (IER) where interface recombination may dominate. (b) The top view of the interface edge region.

Table 5.1 Definition of circuit elements in the transverse branch of Figure 5.6

C_{ss}^{t} = series interface state capacitance of IER

G_{ssn}^{t} = series conductance of interface states in IER due to electron capture-emission

G_{ssp}^{t} = series conductance of interface states in IER due to hole capture-emission

C_{w}^{t} = space charge layer capacitance of IER

Y_{d}^{t} = minority carrier diffusion admittance along the transverse direction

G_{p}^{t} = conductance of holes in valence band from inverted region to IER along the transverse direction

G_{n}^{t} = conductance of electrons in conduction band from inverted region to IER along the transverse direction

is then converted to Figure 5.6d where

$$C_s = C_w + C_w^t \tag{5.8}$$

$$C_{ss}' = C_{ss} \frac{(G_{ssn})^2 + (\omega C_{ss}^t)^2}{(G_{ssn})^2 + \omega^2 C_{ss}^t (C_{ss} + C_{ss}^t)} \tag{5.9a}$$

$$\frac{1}{G_{ss}'} = \frac{1}{G_{ssn}^t} \cdot \frac{1}{1 + (\omega C_{ss}^t / G_{ssn}^t)^2} + \frac{1}{G_{ssp}^t} \tag{5.9b}$$

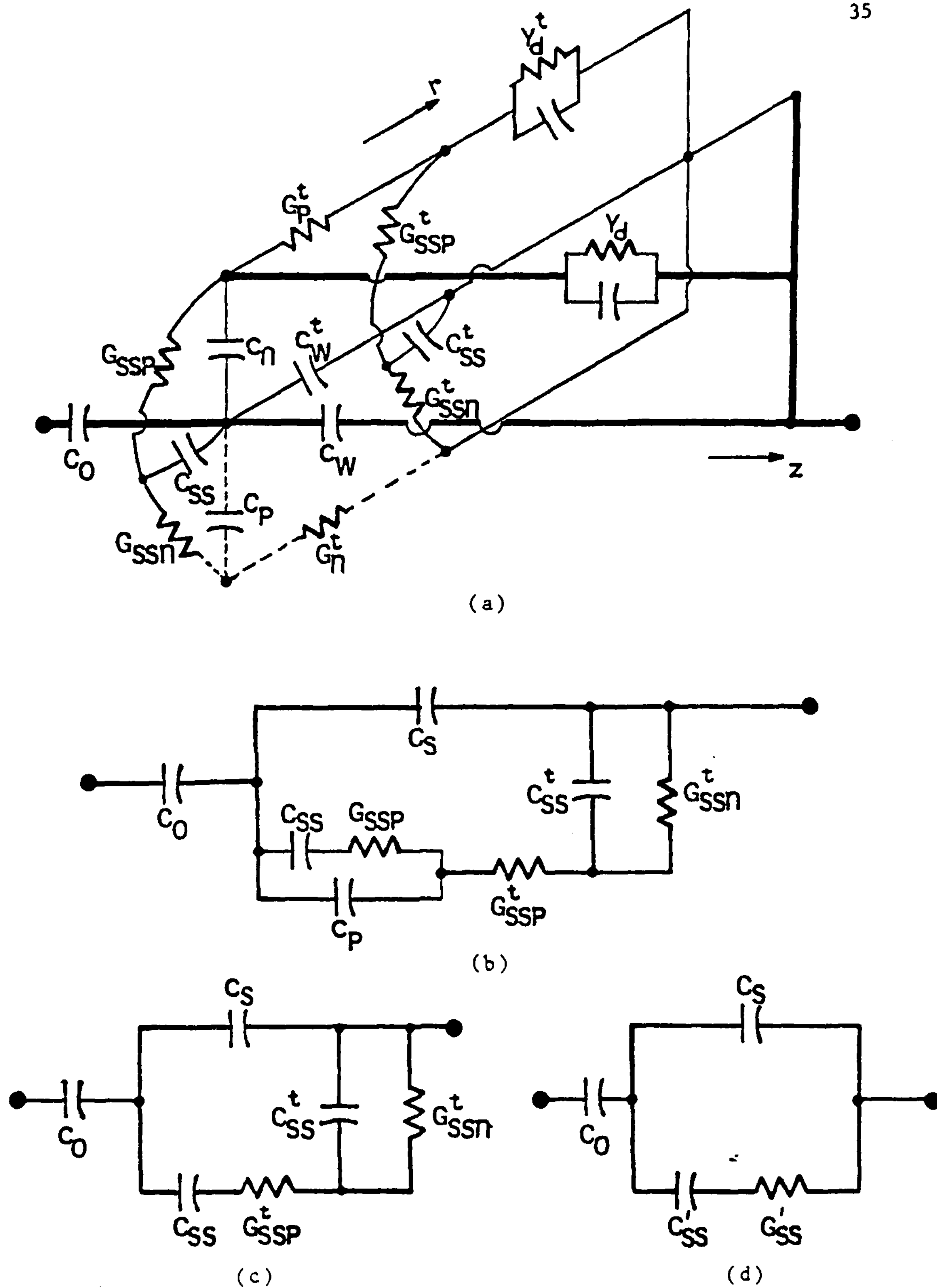


Figure 5.6 Complete and simplified equivalent circuit models for n-type MOS capacitor in inversion with interface edge effect. (a) Two-dimensional model. (b), (c), (d) simplified models where the diffusion admittance Y_d and Y_d^t are opened.

For high and low frequencies, we have

$$\text{(i) } \omega \to \infty \quad G'_{ss} \to G^t_{ssp} \tag{6.10}$$

$$C'_{ss} \to C_{ss}C^t_{ss}/(C_{ss} + C^t_{ss}) \tag{6.11}$$

$$\text{(ii) } \omega \to 0 \quad 1/G'_{ss} \to 1/G^t_{ssn} + 1/G^t_{ssp} \tag{6.12}$$

$$C'_{ss} \to C_{ss} \tag{6.13}$$

Note that the correction $C'_{ss}(\omega \to 0) = C_{ss} + C_p$ must be made for a strongly inverted surface when C_p is comparable to or greater than C_{ss}. The value of the circuit elements can be extracted from the curves of calculated C'_{ss} and G'_{ss}/ω versus frequency from experimental data, using the asymptotic formulae. Finally, we note that the interface edge effect is not important in the accumulation region since the majority carrier conductance and storage capacitance is so large as to short out the IER.

5.3 Device Fabrications and Measurements

The devices used in this study are made on n-type silicon with <111> surface orientation. The geometry of the devices was shown in Figure 5.5. The diameter of the capacitor is 80 mils. Phosphorus predeposition was used to getter impurities and to form an n^+ layer for good back contact. The oxide was grown thermally at 1200°C in dry oxygen, followed by 20 minute annealing in dry argon ambient. The thickness of oxide is about 2600 Å. Room temperature bias stress tests were performed and the 1 MHz C-V curves showed negligible drift of ions in the oxide. This is important since the shift in C-V curves due to mobile ions will cause significant error in the total density of interface states as well as in the frequency dispersion data.

The actual substrate doping densities of the device was obtained from low temperature equilibrium C-V curves with a fast negative voltage ramp. C^{-2} was then plotted against V_G and least-square fitted to obtain $N_{DD} = 2/q\varepsilon_s\ (dC^{-2}/dV_G)$. The minority carrier lifetime, τ_{po}, was measured to be 7.4 μsec. using the capacitance transient method of Sah and Fu [29]. The minority carrier diffusion admittance in Equation (5.5) is $Y_d = 1.73x10^{-9} + j\omega\ 6.43x10^{-15}$ mho/cm^2 when $\omega\tau_{po} << 1$. Since Y_d is small, the approximation that Y_d could be treated as an open circuit in the equivalent circuit compared with other elements is justified.

Three-terminal capacitance and conductance measurements were made from 1 Hz to 10^5 Hz using a PAR-186 phase-sensitive detector-amplifier connected to a Hewlett-Packard Multiprogrammer automatic data acquisition system and a Hewlett-Packard 1000 minicomputer system. The block diagram of the measurement system is shown in Figure 5.7. The details of the admittance bridge are shown in Figure 5.8. The transfer function is proportional to $G_m + j\omega C_m$ if $(G_m + j\omega C_m) << R^{-1}$. The automated data acquisition system is controlled by a user program which steps the bias voltage applied to the device and waits long enough for output of the lock-in amplifier to settle. It then takes a predetermined number of readings. The data are averaged and stored in a magnetic disk file for further analysis. Very accurate experimental data are obtained this way.

Accurate phasing for conductance is achieved by switching-in a lossless capacitor with a value of the order of the oxide capacitance and then looking for the phase at which there is no change in conductance reading when the lossless capacitor is switched in and out. Accurate phasing

Figure 5.7 The block diagram of the computer-controlled data acquisition and analysis system for conductance and capacitance measurements of a MOS capacitor.

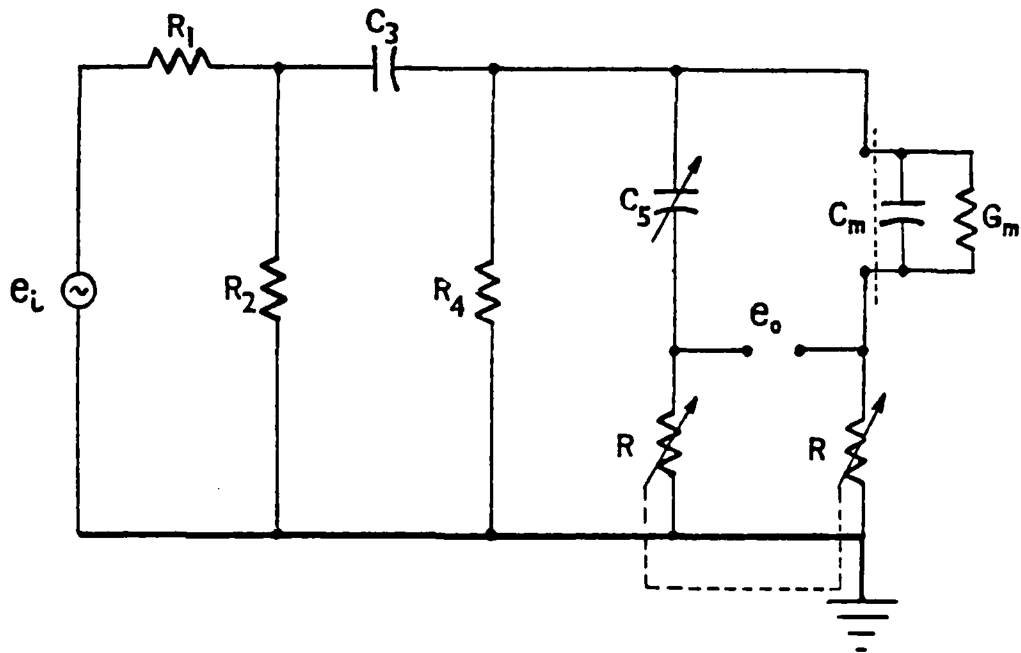


Figure 5.8 The circuit diagram of the admittance bridge using to measure the MOS admittance from 1 Hz to 100 KHz using the PAR-186 phase-sensitive detector. e_i is the reference audio signal and e_o is proportional to a.c. current flowing in the MOS admittance which is connected to the differential input of the PAR-186. C_s is the standard calibration capacitance and C_m and G_m are the equivalent parallel capacitance and conductance of the MOS capacitor under test.

for conductance measurement is achieved in a similar manner by switching-in a deposited precision carbon resistor with very low capacitance. Calibration of the capacitance measurement is made by using a Boonton 71-3A push-button precision capacitor which has been calibrated at each measurement frequency by capacitance bridges. Calibration of the conductance measurement is done by taking advantage of the fact that G/ω is just an equivalent capacitance. The stray capacitance and conductance of experiment jigs, cables and header were subtracted out from the readings of the data acquisition program.

1 MHz capacitance measurement was made by a computer controlled data acquisition system using a Boonton 72A capacitance meter. The amplitude of the small ac signal used in this study was between 1 to 10 mV which is small compared with the thermal voltage $k_BT/q \approx 26mV$, so that the linear small-signal model is valid and the assumption that a constant density of states is being probed by small ac signals is justified.

The experimental frequency dispersion curves of capacitance and conductance versus bias for a typical device are shown in Figures 5.9 and 5.10 respectively. Appreciable frequency dispersion was observed in the frequency range from 1 Hz to 10^6 Hz. Series equivalent circuit elements C'_{ss}, G'_{ss} related to interface states are calculated from the measurements of C_m and G_m by transforming the circuit in Figure 5.11(a) to the circuit in Figure 5.11(b). In doing so, we have assumed that the surface potential at a given bias is the same for different frequencies. Thus, the semiconductor capacitance C_s can be obtained from the 1 MHz C-V curve. C_o, the oxide capacitance was also calculated from the 1 MHz C-V curve in strong accumulation using the method of McNutt and Sah [30]. Accurate determination of the oxide capacitance is important in this study

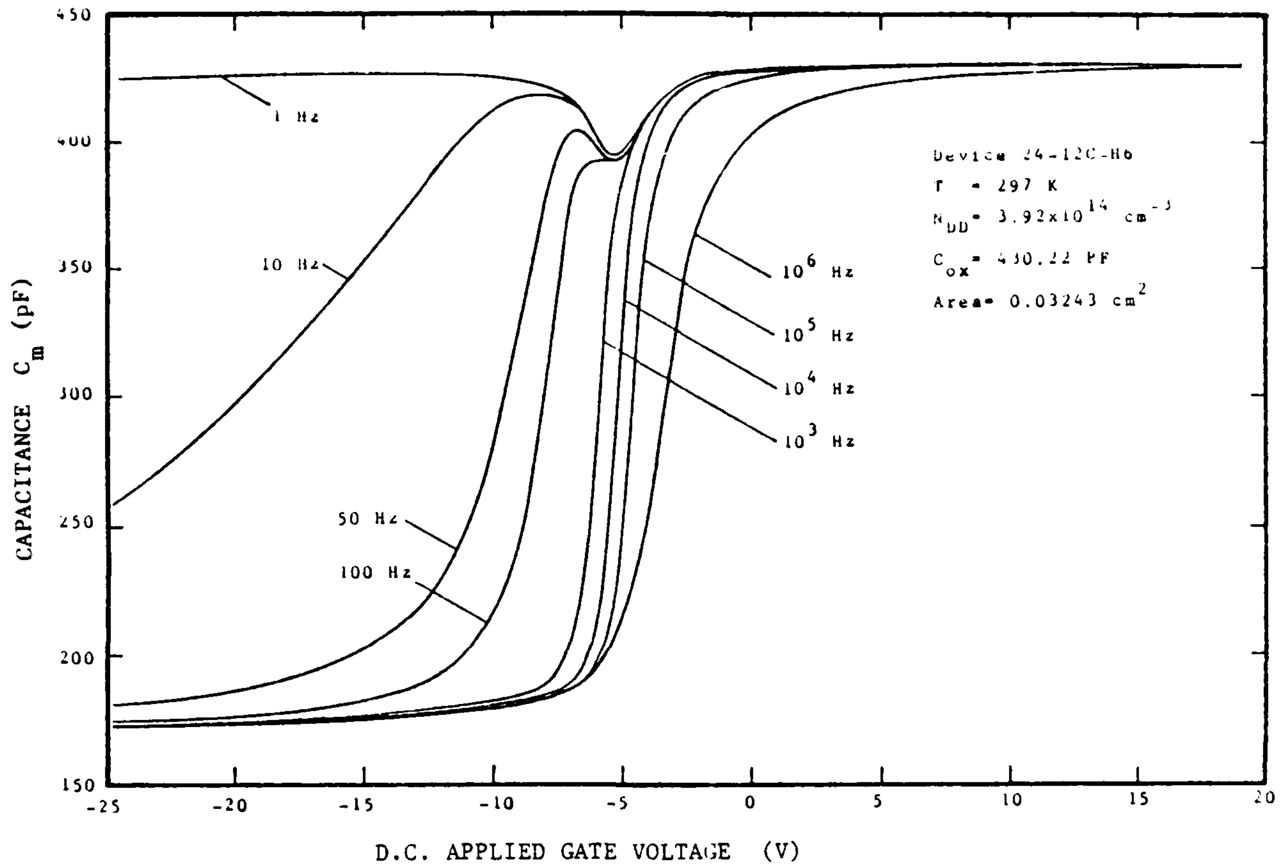


Figure 5.9 The measured equivalent parallel capacitance of MOS capacitor 24-12C-H6 as a function of d.c. applied gate voltage with signal frequency as the parameter.

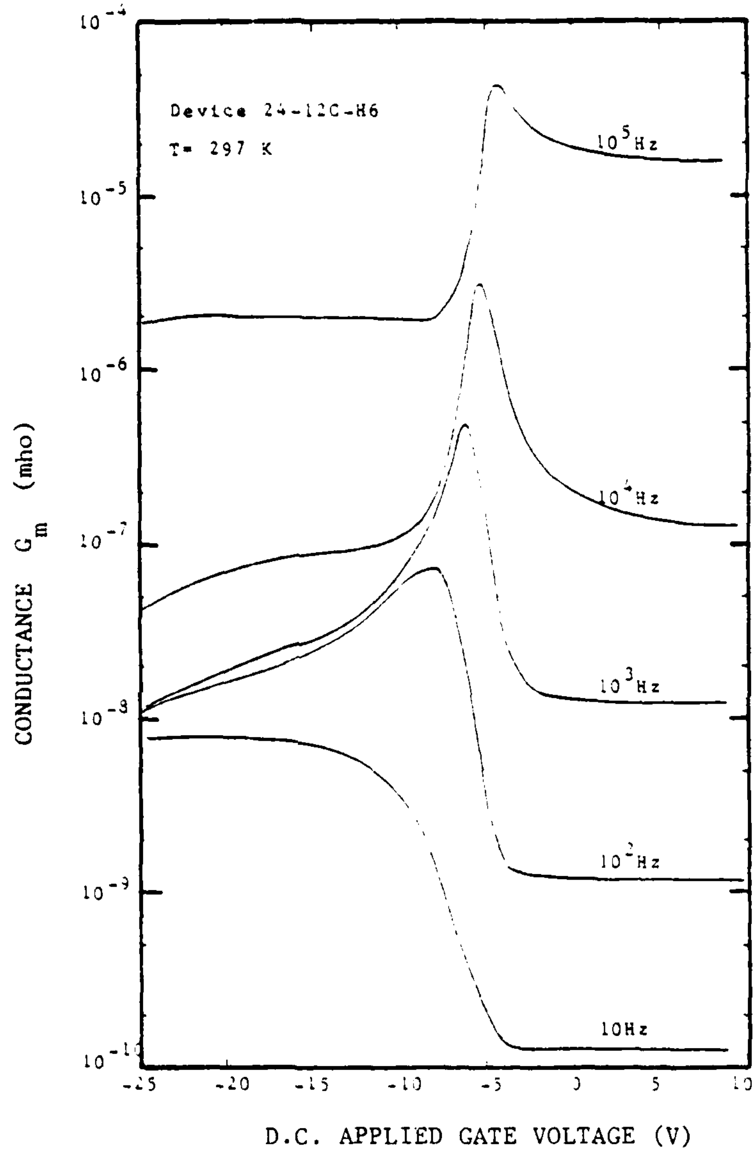


Figure 5.10 The measured equivalent parallel conductance of MOS capacitor 24-12C-H6 as a function of d.c. applied gate voltage with signal frequency as the parameter.

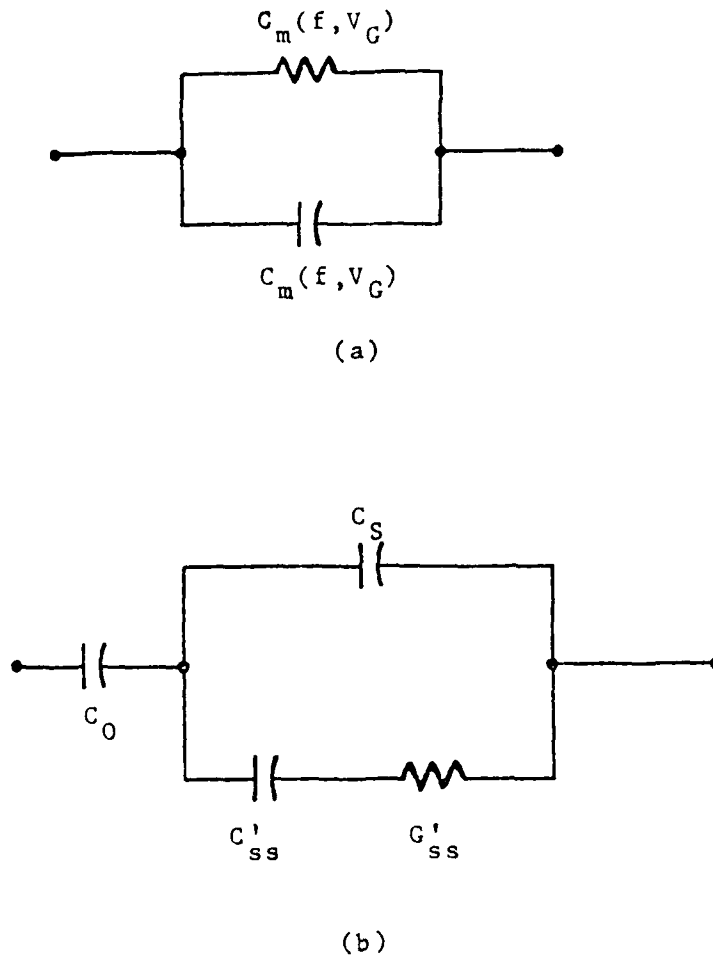


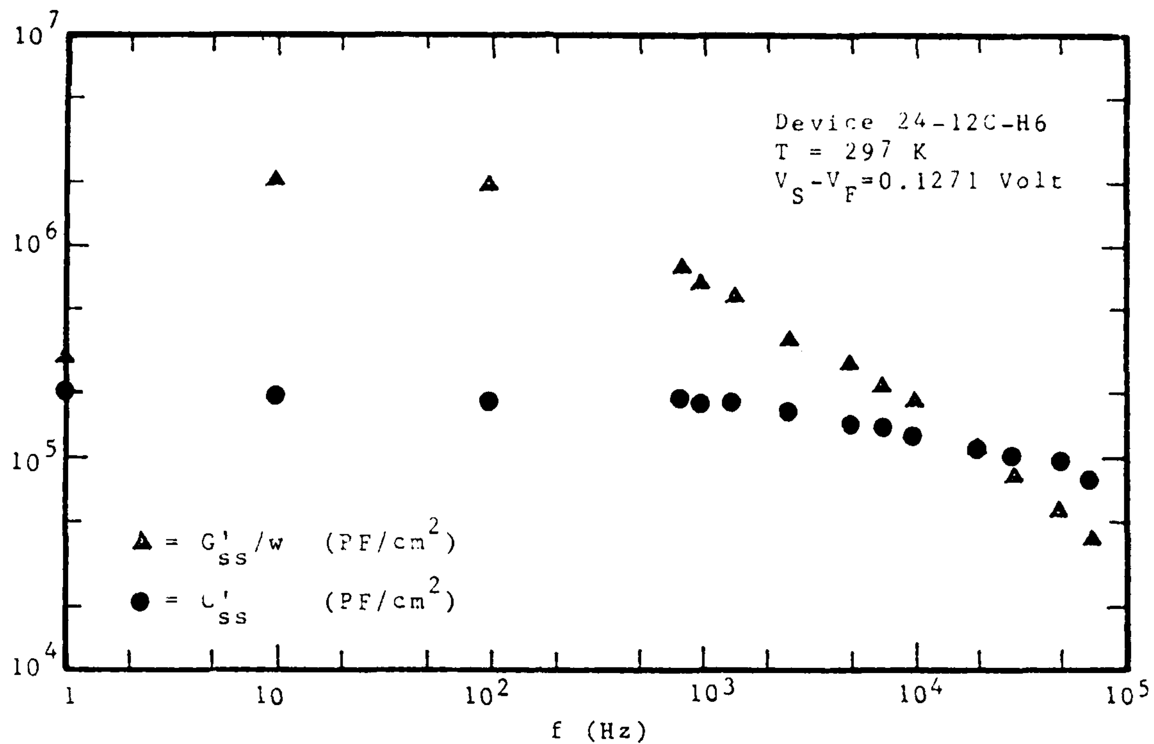
Figure 5.11 Equivalent circuit model of a MOS capacitor. (a) The measured equivalent parallel admittance and (b) the equivalent circuit applied to both surface accumulation and inversion conditions.

because in the accumulation range, the interface states capacitances and the majority carrier storage capacitances are so large that the measured capacitance C_m is close to the oxide capacitance. In accumulation, we have $C'_{ss} = C_{se}$ and $G'_{ss} = G_{se}$ as in Figure 5.4 and 5.2. In inversion, C'_{ss} and G'_{ss} are given by Equation (5.9) and (5.10).

5.4 Discussion of Results

C'_{ss} and G'_{ss}/ω versus frequency are plotted in Figure 5.12 and 5.13 for Device 24-12C-H6 biased into accumulation and inversion respectively. From Figure 5.12 and 5.13, we note that the asymptotic formulae G'_{ss} $(\omega \to \infty) \to G^{t}_{ssp}$ and $C'_{ss}(\omega = 0) \to C_{ss}$ indeed hold. The density of interface states at this potential can be calculated using Equation (5.6), $P_{TTS} = C_{se}/q^2 \approx C'_{ss}/q^2$, which applies to both accumulation and inversion since the equivalent circuits have the same form (Figures 5.2 and 5.6d). The density of interface states was also obtained from Terman's method [31], i.e. by differentiating the 1 MHz C-V curve, dC/dV. The two results agree with each other fairly well in the inversion region ($V_s - V_F < 0$) as indicated in Figure 5.14. In the accumulation region, the σ_{TTS} from low frequency capacitance is 2 to 3 times greater than that obtained by Terman's technique.

The experimental accuracy of the capacitance measurements in inversion for frequencies higher than 10^4 Hz is not good. This fact is clearly shown in Figure 5.9. The capacitance in the inversion region increases only slightly for frequencies above 10^4. The range of surface potentials available in this study is limited by experimental accuracy as well as by the pinning of surface potential due to high density of interface states.



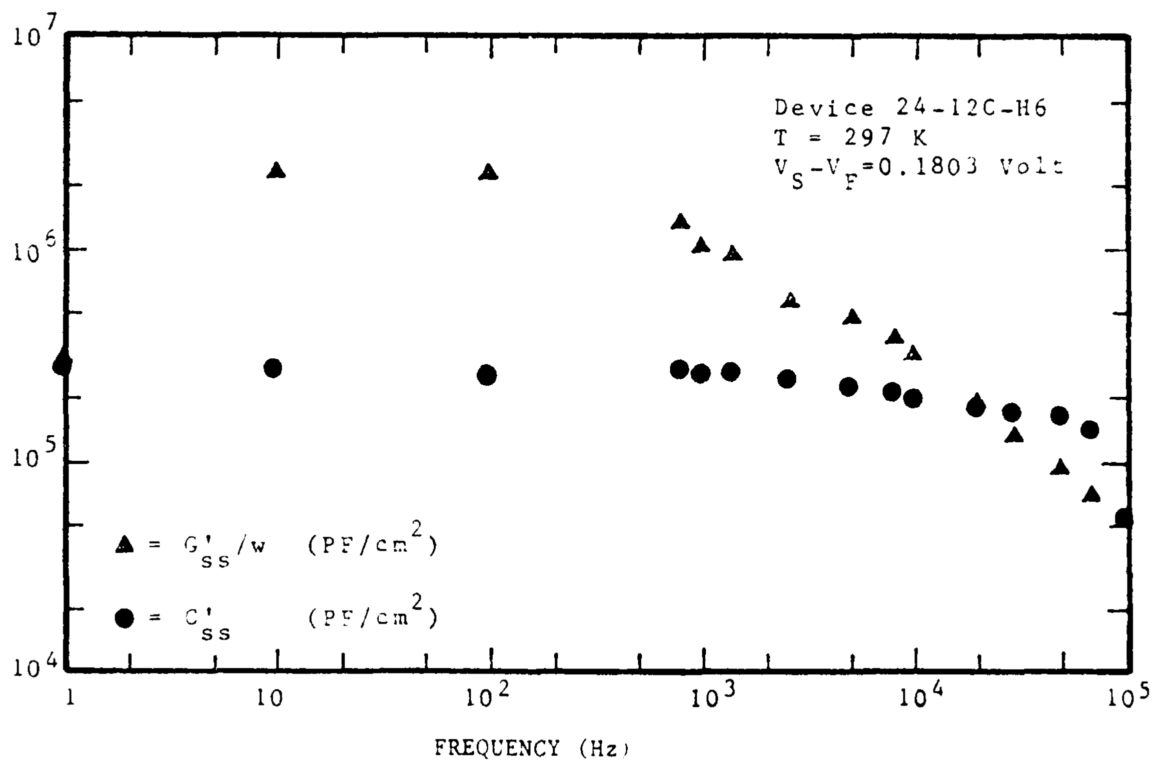


Figure 5.12 C'_{ss} and G'_{ss}/ω versus frequency of MOS capacitor 24-12C-H6 at two interface state energies: E_i+127.1 and E_i+180.3 mV.

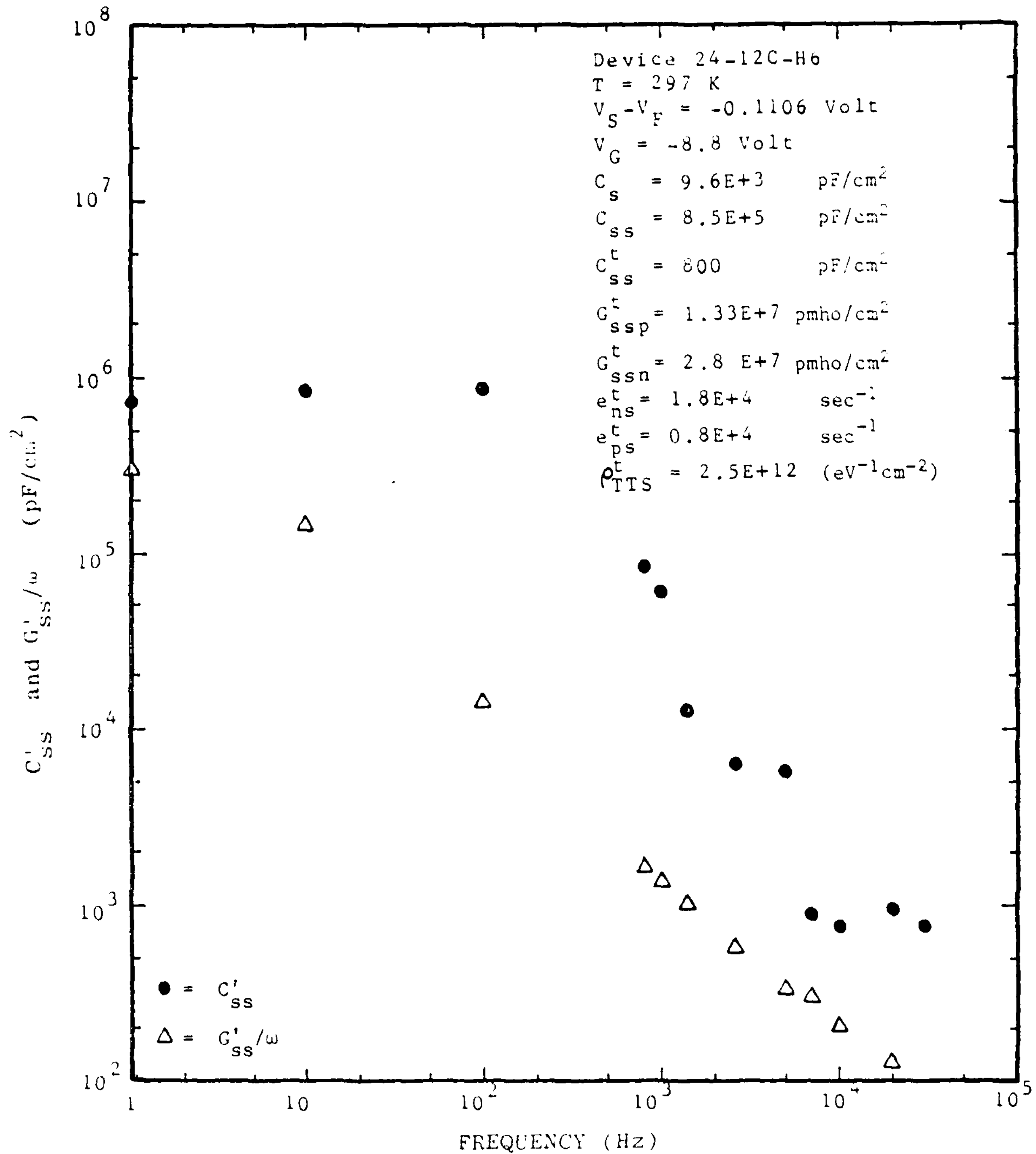


Figure 5.13 C'_{ss} and G'_{ss}/ω versus frequency for Device 24-12C-H6 at a interface state level 110.6 mV above the intrinsic Fermi level.

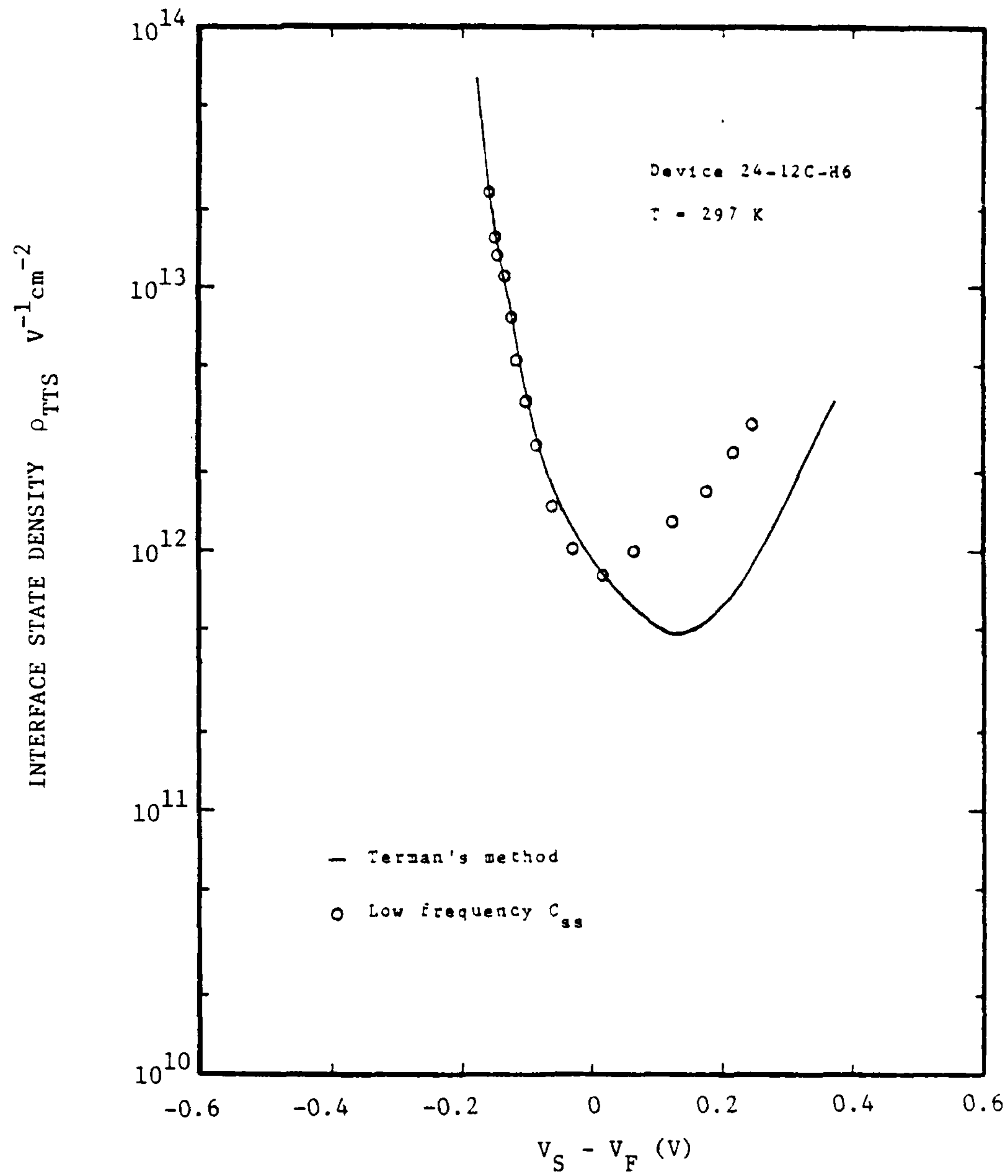


Figure 5.14 Comparison of the interface state density measured by two methods (low frequency C_{SS} and Terman's analysis) as a function of its energy measured from the intrinsic Fermi energy, V_S-V_F. E_C is located near 0.6 V.

The behavior of the low frequency C-V in Figure 5.9 can be readily explained using the equivalent circuit of Figure 5.6d. C_{ss} is estimated to be 8.5×10^5 pF/cm^2 from Figure 5.13. $C_s \approx 10^4$ pF/cm^2 and $C_o \approx 1.33 \times 10^4$ pF/cm^2. Therefore as $\omega \to 0$, C'_{ss} in Figure 5.6d dominates and the measured capacitance approaches the oxide capacitance C_o as shown in Figure 5.9.

5.5 Summary of Results

Simple one-lump equivalent circuits were derived. They were found to be quite successful in explaining the frequency response of interface states. When the device is biased into accumulation, the series equivalent circuit for interface states together with a two-step model involving Shockley-Read-Hall transitions and tunneling processes works well. In the case of an inverted surface, a model which takes into account the interface edge effect is proposed and found to be in good agreement with experimental data. Both circuit models allow one to calculate the density of interface states from low frequency interface state capacitance and the results were compared with those obtained from Terman's high-frequency C-V method [31]. The agreement between these results was quite good. These equivalent circuits contain only linear elements (capacitances and conductances). The interface state properties can be obtained from the experimental values of the circuit elements from the low and high frequency measurements of MOS capacitance and conductance.

VI. BULK TRAPS IN BURIED-CHANNEL CHARGE-COUPLED DEVICES

6.1 Problem Identification

In buried-channel charge-coupled devices (BCCD), the charge is stored away from the $Si\text{-}SiO_2$ interface so that carrier trapping at the interface states can be neglected. In this case, the trapping at bulk impurities and defects limits the device performance. One may introduce a small background charge (or fat zero) to reduce the transfer inefficiency for a BCCD in a similar way to that used for a surface channel CCD. In the presence of background charge, edge effects are the dominant loss mechanism because the signal charge occupies a larger volume than the background charge.

Unlike the interface states, the bulk states (or bulk traps) have discrete energy levels in the energy gap. The thermal emission rate of electron trapped by bulk states is related to the activation energy and temperature by the Arrhenius equation

$$e_n = \sigma_n v_t N_c \exp(-E_A/k_B T). \qquad (6.1)$$

Here σ_n is the capture cross section. v_t is the thermal velocity. N_c is the density of states. E_A is the activation energy. We note that the emission rate, e_n or emission time constant, $\tau_n = 1/e_n$, is an exponential function of temperature. Each species of bulk traps has a characteristic lifetime given by Equation (6.1).

Experimental data of transfer inefficiency versus clock frequencies reveal several peaks [32, 33]. Similar peaks were also reported in BCCD noise measurements [34]. It was shown that for a three phase CCD, the transfer inefficiency due to bulk state trapping reaches the maximum value when the clock frequency is related to

emission lifetimes by [35]

$$f_{max} = (N_z + 1/3)\ [\tau_e \ln(3N_z + 2)]. \qquad (6.2)$$

Here N_z is the number of zeros preceding the first signal "one."

Bulk trap densities between 10^{10} and 10^{12} cm^{-3} have been reported [32-34]. Some of these bulk traps come from metallic impurities such as gold, sulfur and iron unintentionally introduced during processing. These impurities were identified by matching the measured activation energy with the published data of known bulk traps [32]. A more reliable identification is to match the measured emission time constants from the BCCD in a wide range of temperatures with published data of a known bulk trap such as gold [36] and sulfur [37]. The fact that the bulk traps observed in BCCD could also come from process-induced defects [38, 39] has not been noted in the literature.

Ion implantation is used to fabricate BCCD. A large number of bulk trap levels were observed in silicon after ion implantation [40]. It is likely that some of these bulk states may still be present after high temperature annealing since bulk trap densities in the range of 10^9 to 10^{11} cm^{-3} is sufficient to cause problems in BCCD. These bulk traps can also come from thermally-induced defects or quenched-in centers. Yau and Sah [38] reported two trapping levels located at 0.264 and 0.542 eV below the conduction band for n-type silicon. Collet [32] observed two levels at 0.25 and 0.54 eV below the conduction band in his n-channel BCCD. These could very well be the same quench-in levels reported by Yau and Sah.

The objective of this project is to accurately characterize the bulk traps which may be introduced during BCCD processing steps such as

ion-implantation, expitaxial growth, thermal quenching, chemical cleaning and diffusion.

6.2 Experimental Techniques

Transient capacitance techniques [41, 42] are used because of their high sensitivity and also because the experimental conditions of diode fabrication and measurements are very similar to the operating conditions of the BCCD.

Our measurement has been computerized. A block diagram of the apparatus used is shown in Figure 6.1. The device to be measured and the temperature controller are shown in Figure 6.2. The detail operation of the temperature controller was described in a previous report [43]. The temperature controller is implemented in software using proportional plus integral control. The controller is capable of controlling the sample temperature to within ±0.1 K during the measurement in the temperature range from 85 K to 300 K. The controller controls the heater power by altering the output voltage of the HP 6224B power supply through the D/A card. The device temperature is monitored by the Data Precision 5-1/2 digit voltmeter through two isolated input cards.

The data sampling is controlled by a separate program. The sampling program starts an experiment by sending a pre-determined bit pattern to the TTL output card which in term triggers the pulse generator (HP 8010A) to generate a pulse of preset amplitude and duration. The resulting capacitance transient due to the pulse is measured and converted into digital form by a second 5-1/2 digit DVM. The time at which each capacitance data is taken is obtained from the

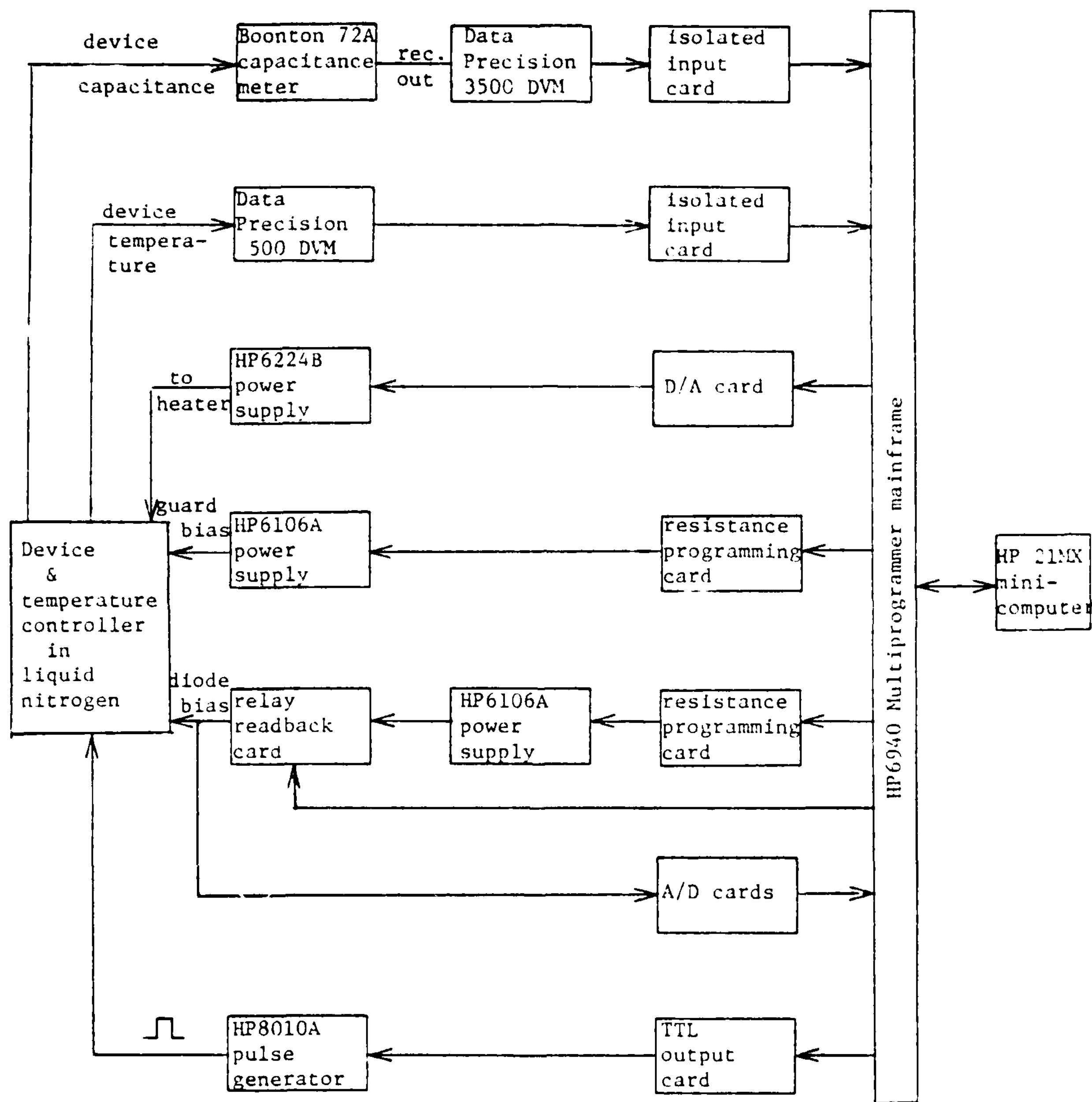


Figure 6.1 Block diagram of the computer controlled transient capacitance measurement setup.

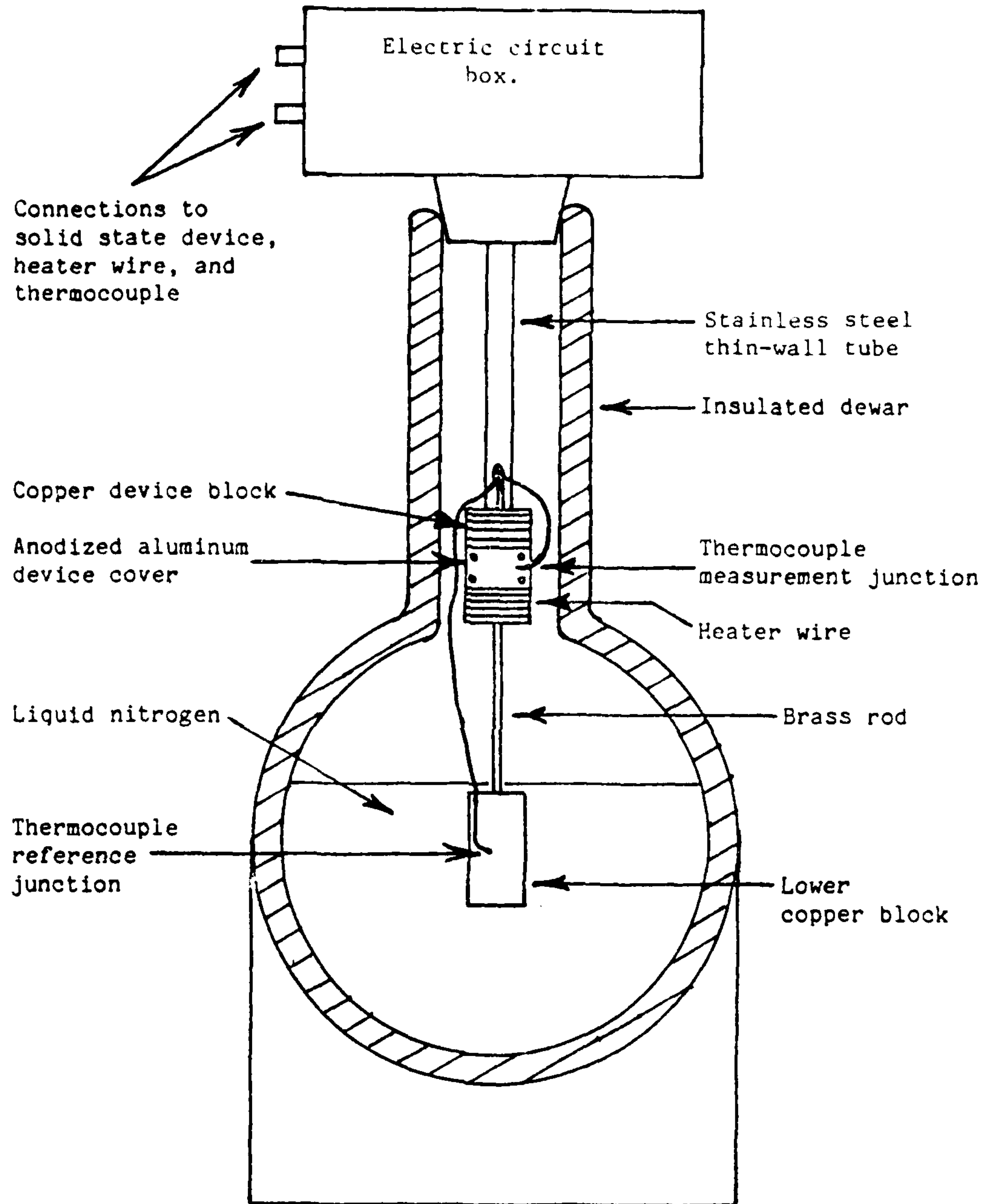


Figure 6.2 The liquid nitrogen dewar, the device sample holder, and the thermocouples of the computer controlled transient capacitance measurement setup.

real-time clock in the minicomputer. The capacitance, time and the temperature of each data point are stored in a disk file for plotting and further analysis. A typical capacitance versus time plot is shown in Figure 6-3. The temperature during the experiment is shown on the upper part of the plot. The small random variation in temperature comes from electrical noise picked up by the thermocouple wire which shows that the device temperature was kept constant to better than ± 0.1 K.

6.3 Measurement of Bulk Trap Parameters

Thermal emission rate is obtained by least-square fitting the C-t (capacitance versus time) data in Figure 6.3 to

$$C(t) = C_\infty - \Delta C \cdot e^{-t/\tau_e}. \qquad (6.3)$$

The thermal emission rates or the emission time constants τ_e determined at many temperatures are then fitted to the equation

$$\tau_e^{-1} = e^t = A_m (T/300)^m \exp(-E_A/k_B T). \qquad (6.4)$$

Equation (6.4) is identical to Equation (6.1) except that the temperature dependence of the pre-exponential factor is explicitly displayed in (6.4). In general, the fitted thermal activation energy or the energy level of the bulk traps depends on the choice of m in Equation (6.4). The total capacitance change, ΔC, during the entire transient is related to the ratio of the bulk trap density to majority impurity dopant or majority carrier concentration as follows [42]

$$\Delta C/C_\infty = N_{TT}/2(N_{DD} - N_{AA}). \qquad (6.5)$$

Equation (6.5) is valid if $\Delta C \ll C_\infty$ or $N_{TT} \ll (N_{DD} - N_{AA})$. Thus, the approximate density of bulk traps can be obtained from C-t data and Equation (6.5).

It is usually desirable to make a quick survey to determine if there are bulk traps present in a given sample. This survey, which we denote VSCTS (Voltage Stimulated Capacitance Transient Spectroscopy), can be performed using the computer controlled data acquisition system shown in Figure 6.1. In the VSCTS measurements, the device temperature is raised from 77K to 300K either by a programmed slow linear or nonlinear temperature ramp (known as the DLTS method [44]) or by programmed small temperature steps (VSCTS). Instead of sampling the entire capacitance transient at each constant temperature, the capacitance is sampled at two preselected and fixed times, t_1 and t_2. This is illustrated in the inset of Figure 6.4. The capacitance difference at these two times, C_2-C_1, is then stored and plotted as a function of temperature. Its magnitude is a function of temperature or the emission time constant, τ_e, and the sampling times t_1 and t_2. A typical example from a gold-doped silicon n+/p diode is shown in Figure 6.4. The occurence of the capacitance-difference-signal peak at a particular temperature (in this case 140K for the large peak) can be understood from Figure 6.4. Consider a fixed pair of sampling times, t_1 and t_2, for all temperatures between 77K and 300K. At low temperatures when the thermal emission time constant, τ_e, is large compared with the sampling time interval, t_2-t_1, the capacitance transient decay is slow and C_2-C_1 is small. As temperature rises and τ_e decreases, the capacitance transient decay rate increases and C_2-C_1 will increase. However, at still higher temperatures, τ_e becomes so short that the transient is nearly over at t_1, so that C_2-C_1 would again be small. If the capacitance transient is truly exponential, it can be easily shown that the thermal emission rate is

given by [44]

$$e^t = (t_2 - t_1)^{-1} \cdot \ln(t_2/t_1) \quad (6.6)$$

Figure 6.4 shows two peaks at 140K and 230K due to the two gold levels in silicon. The 140K is due to hole emission from the lower donor level, E_V+355 mV. The higher temperature and smaller peak at 230K is due to electron emission, even though the silicon substrate is p-type. This is due to the fact that the emission time constant depends on the emission rate of both electrons and holes trapped at a given level [42]

$$\tau_e = 1/e^t = 1/(e_n + e_p) \approx 1/e_n \quad (6.7)$$

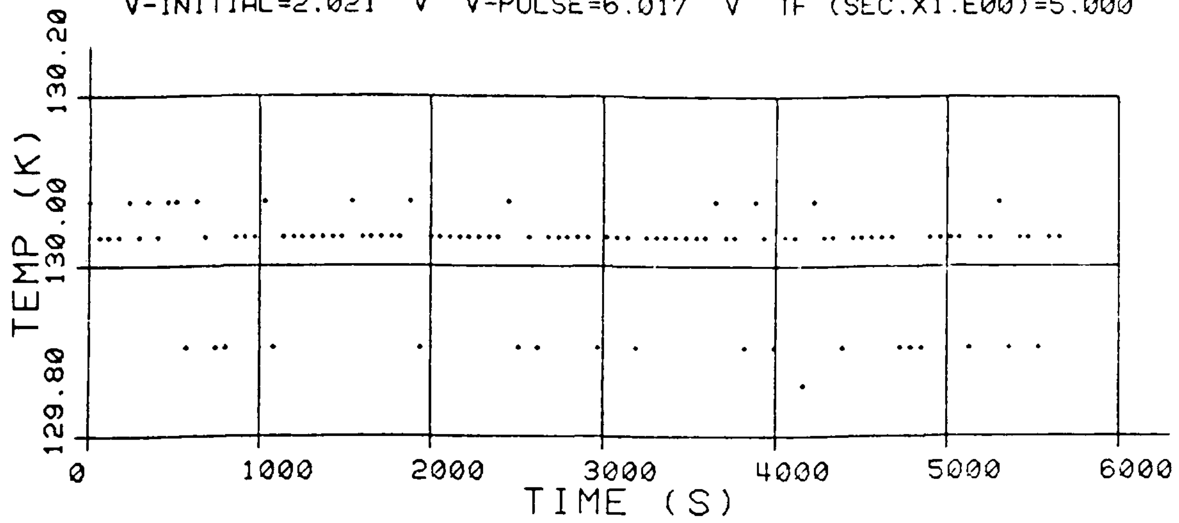
since at this gold acceptor level near the midgap of silicon, the electron emission rate is much higher than hole emission rate, i.e. $e_n >> e_p$.

The smaller amplitude of the 230K peak compared with the 140K peak is due to the fact that most of this midgap level is occupied by holes in a p-type silicon and the trapped electron density is very small compared with the gold density. It is approximately given by

$$N_T = N_{TT} e_p/(e_n + e_p) \approx N_{Au}(e_p/e_n) << N_{Au} \quad (6.8)$$

The larger amplitude of the 140K peak corresponds to the trapped hole concentration at the lower donor level and it is almost equal to the gold concentration, N_{TT} or N_{Au}.

The difference in capacitance signal at the two levels provides another means of determining the minority carrier as well as the majority carrier emission rates in one experimental transient capacitance run.



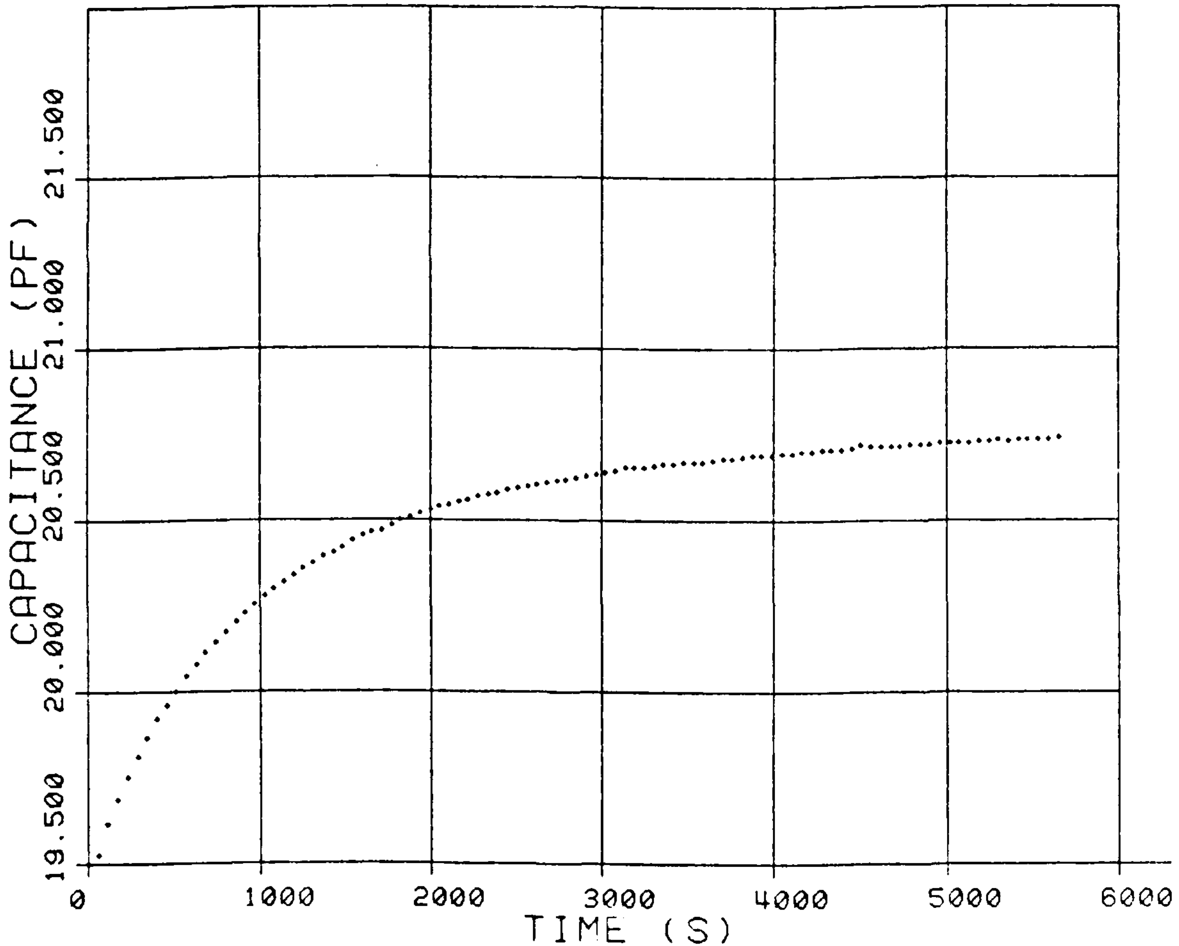


Figure 6.3 A typical computer output of the capacitance transient. The upper figure is the device temperature and the lower figure is the capacitance transient.

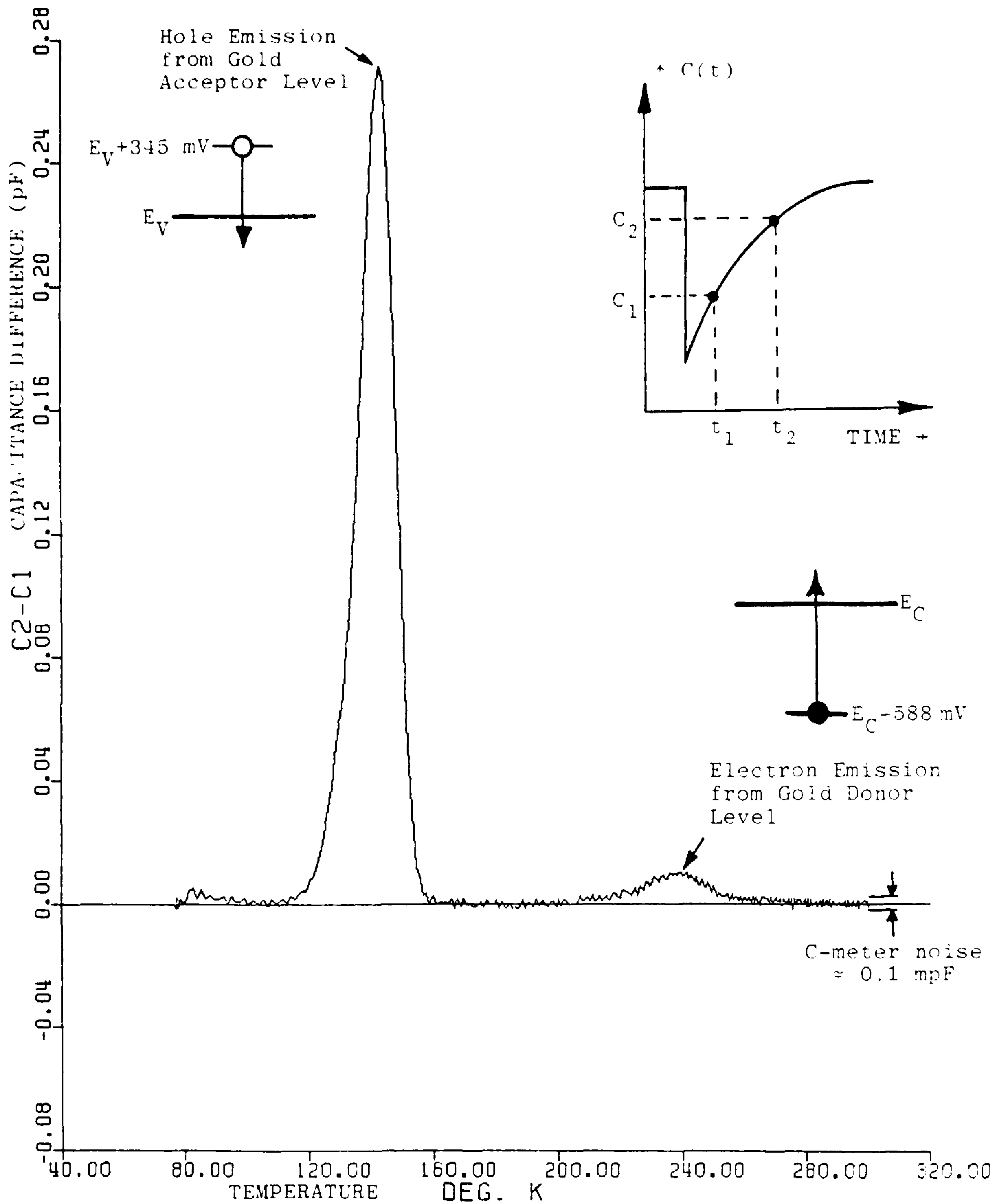


Figure 6.4 Voltage Stimulated Capacitance Transient Spectroscopy (VSCTS) of a gold diffused n+/p silicon diode. The inset shows the two-point sampling of the capacitance transient. The capacitance meter noise is about 0.1 mpF.

6.4 Spurious DLTS (VSCTS) Signals from Surface Recombination

In interpreting VSCTS data, it is necessary to eliminate signal from trapping in a surface channel. One example of this is shown in Figure 6.5. This data is taken from the same device from which data in Figure 6.4 is taken except that a MOS guard ring around the n+ contact is floated in Figure 6.5 while Figure 6.4 is obtained with a negative voltage applied to the MOS guard ring to pinch off the surface channel. The extra peak in Figure 6.5 comes from the surface channel which is pinched off in Figure 6.4.

Another example of a surface effect is observed in an aluminum on n-type silicon Schottky barrier diode. The VSCTS data taken shortly after fabrication is shown in Figure 6.6. There are two peaks at 120 and 300K as well as large noise. The 300K (midgap level) peak and the noise are related to the high reverse leakage current of the device which is 6 μA at -10 volts at room temperature. Since the n-type surface area surrounding the 30 mil diameter circular diode is not passivated, it is likely that the large leakage current is caused by water vapor around the edge of the diode [45]. This is confirmed by baking the diode at 200C for 15 minutes in dry nitrogen ambient. The room temperature leakage current after bakeout was reduced to less than 0.5 μA at -10 volts. The VSCTS was then taken and is shown in Figure 6.7 where the 300K peak is eliminated and the noise is reduced to 0.1 mpF which is the instrument noise from the Boonton 72A one MHz capacitance meter.

6.5 Recombination Centers in Ion Implanted Silicon

Some preliminary results using the computer controlled capacitance transient measurement setup have been obtained from an

oxygen implanted n+/p diode (implanted at AFCRL) previously fabricated in our laboratory [40]. The implant was done at high energy (2MeV) and high dose (10^{13} ions/cm^2). The VSCTS data for three different filling pulse amplitudes are shown in Figure 6.8. The d.c. bias voltage was 10V. Seven peaks are identified. They are labelled P1 through P7. The relative change in the size of peaks at different pulse amplitudes indicates that the bulk traps species have quite different spatial distributions. The spatial distribution of each bulk trap species can be measured using the differential bias voltage technique [46]. The VSCTS data of another ion implanted diode from the same wafer but annealed at 400C for 30 seconds in forming gas ambient is shown in Figure 6.9. Peaks P2, P3 and P6 are eliminated; P5 is barely detectable. P1 decreases in size while P4 and P7 increase quite substantially. This result shows a reverse anneal effect in which P4 (160K) and P7 (290K) have increased their concentration during heating at 400C.

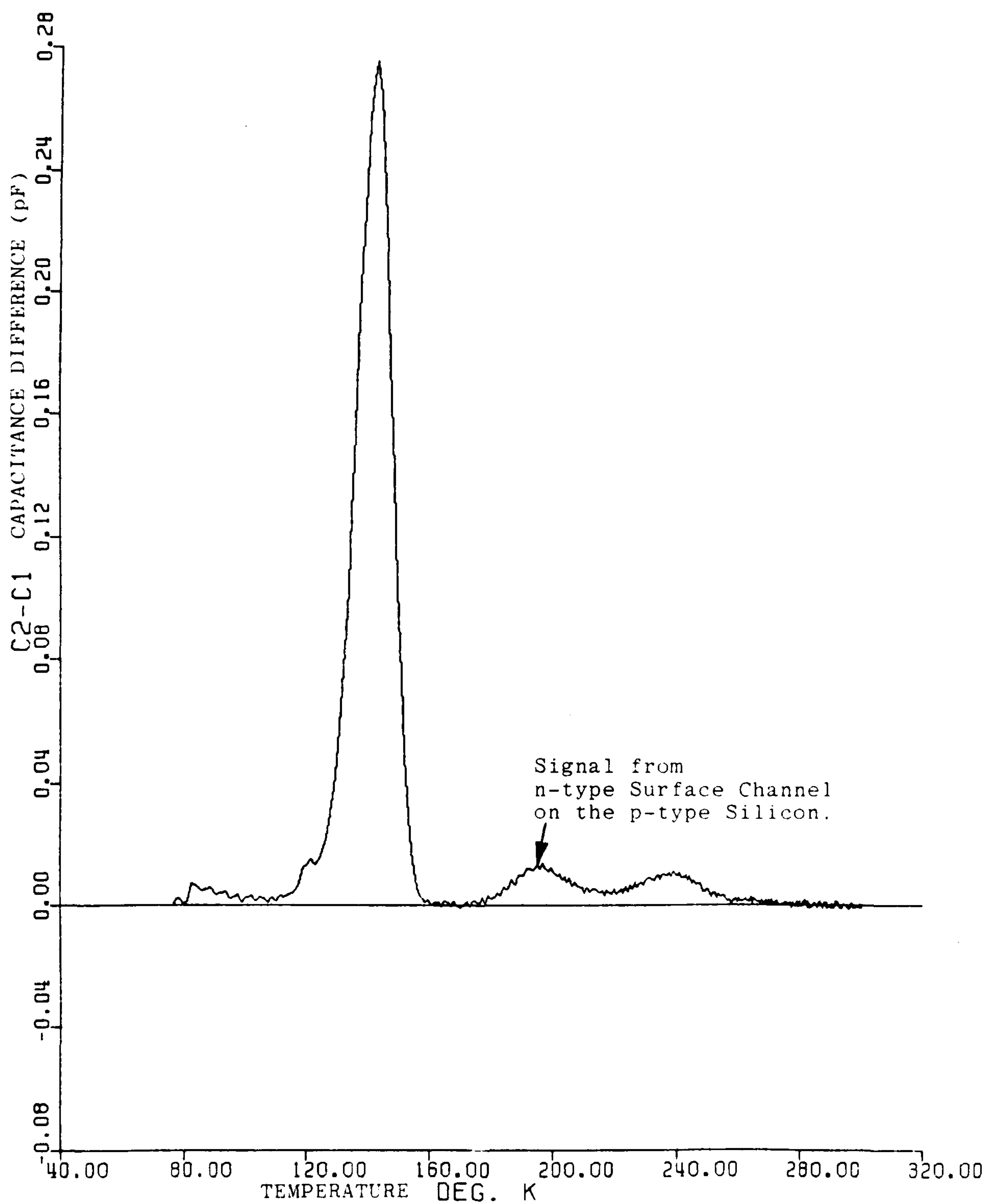


Figure 6.5 VSCTS of the same n+/p gold-diffused silicon diode as that in Figure 6.4 but with the MOS guard ring floated. The MOS guard ring in Figure 6.4 was biased to -10 V to cut off the surface channel

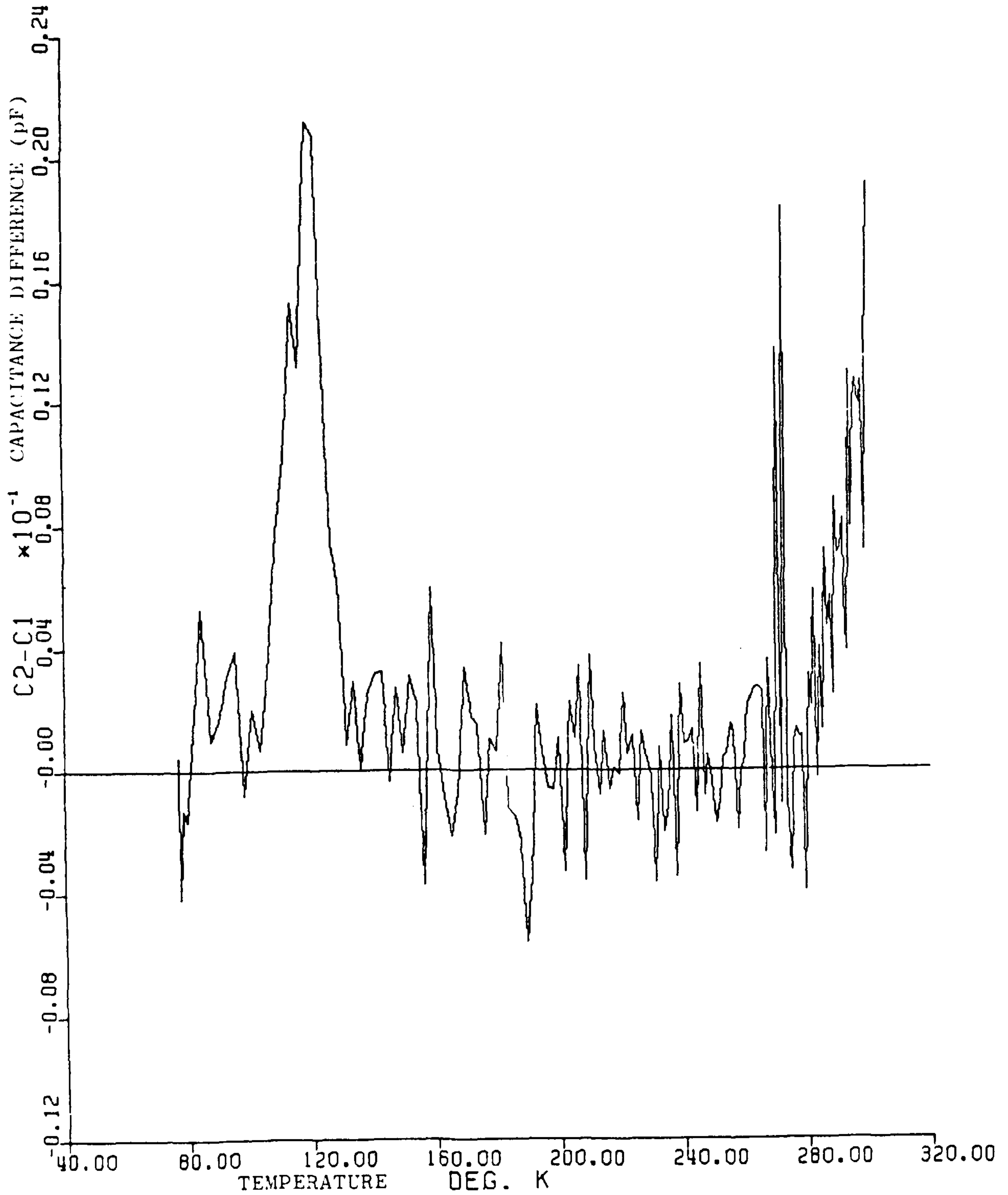


Figure 6.6 VSCTS (Voltage Stimulated Capacitance Transient Spectra) of an aluminum on n-Si Schottky barrier diode before bakeout.

AL ON N-SILICON SCHOTTKY BARRIER
AFTER BAKEOUT AT 200 C FOR 15 MINUTES

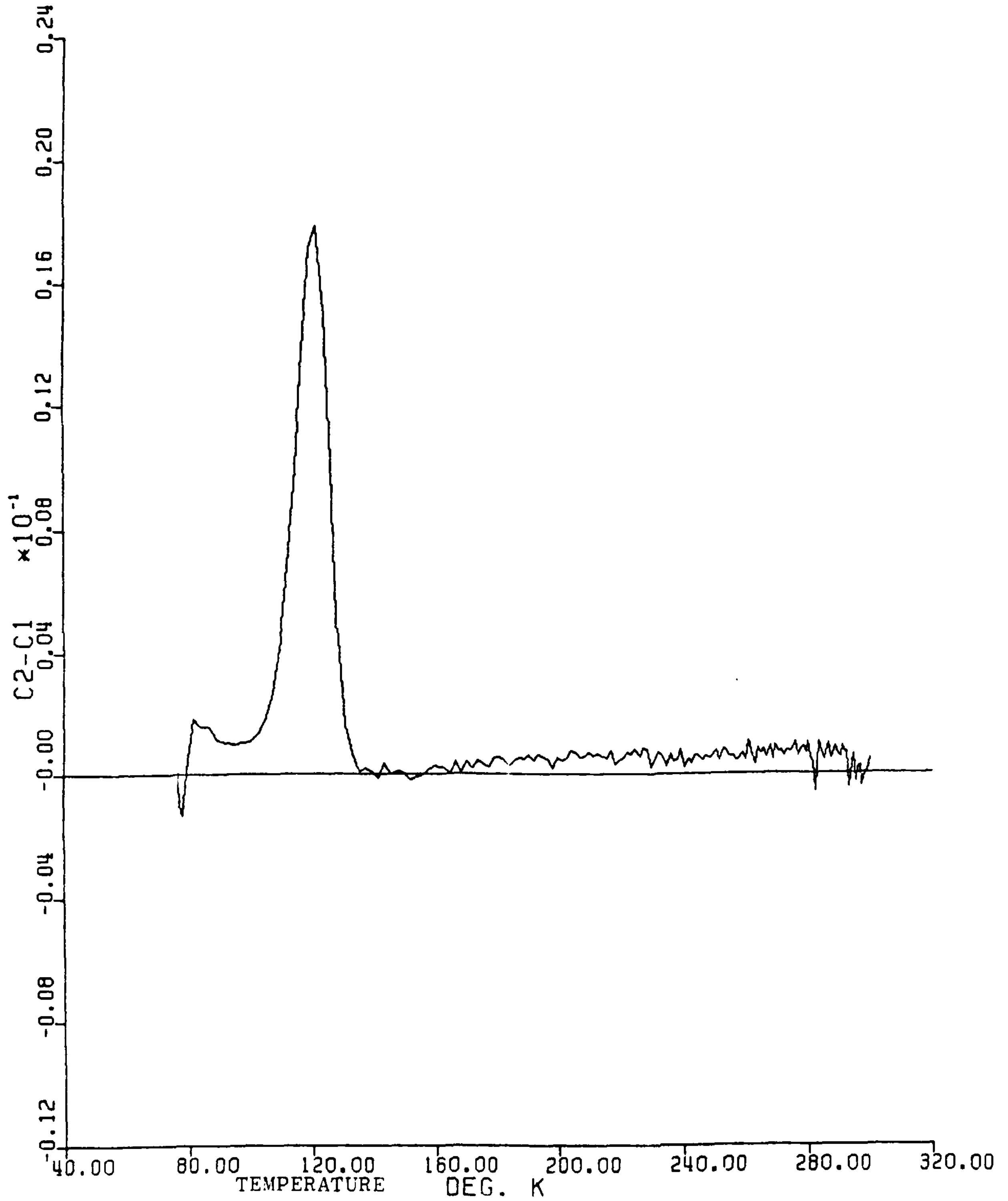


Figure 6.7 VSCTS of the Al/n-Si Schottky barrier diode shown in Fig.6.6 after bakeout at 200C for 15 min. in dry nitrogen.

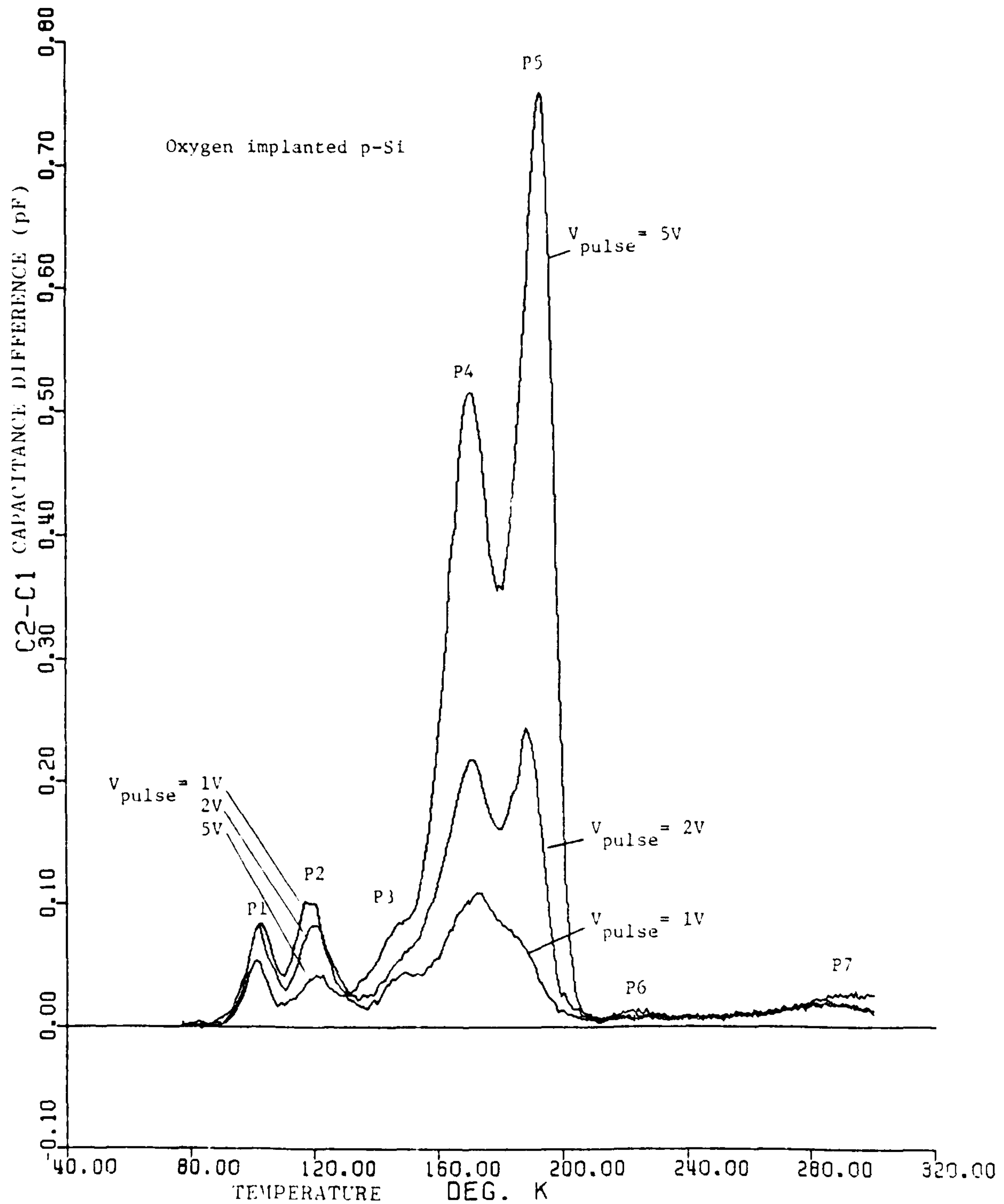


Figure 6.8 Voltage Stimulated Capacitance Transient Spectra of an oxygen (2 MeV) implanted n+/p Si diode after heated at 70C for 30 sec during soldering of the device dice to an 8-pin TO-5 header.

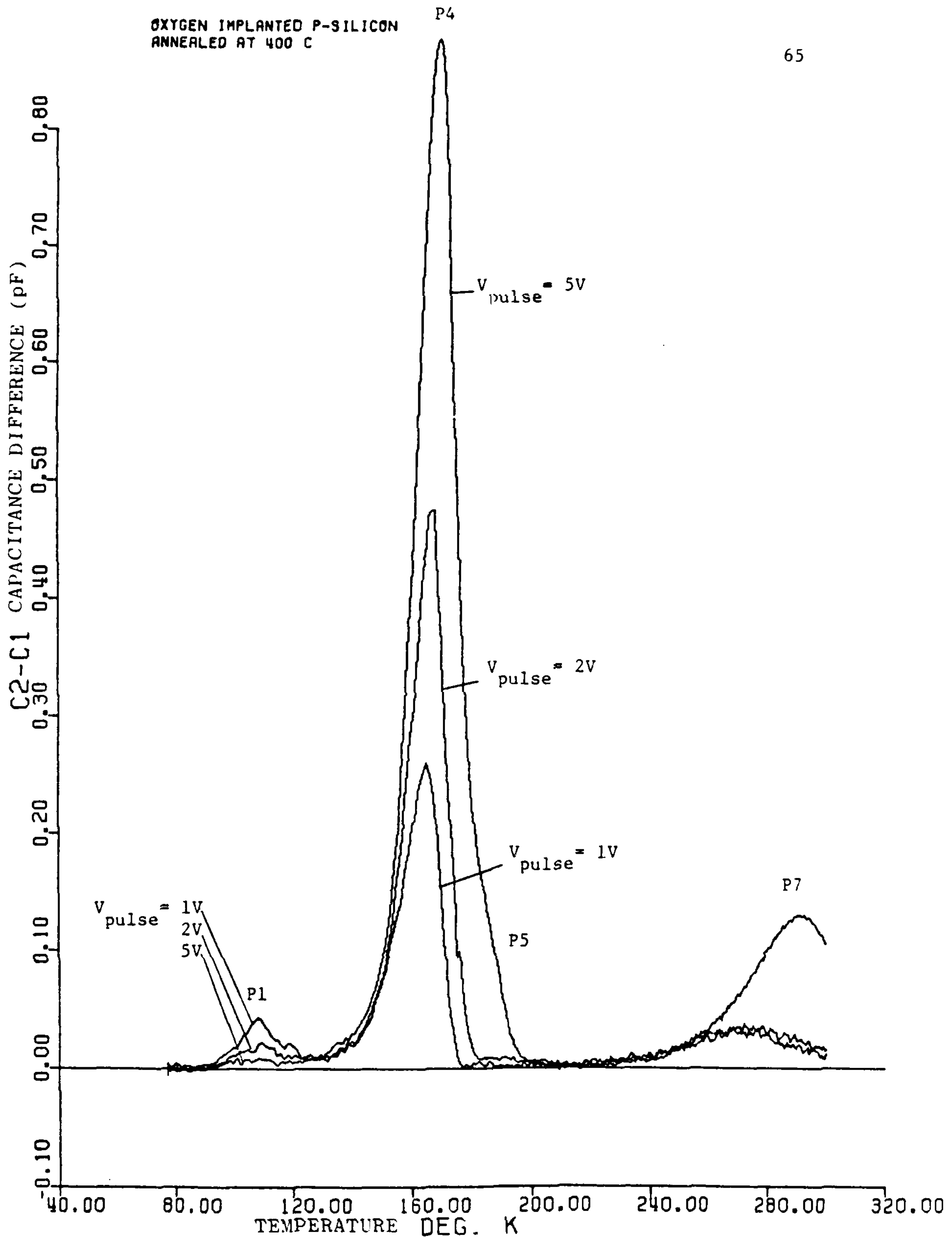


Figure 6.9 Voltage Stimulated Capacitance Transient Spectra of the oxygen implanted n+/p Si diode shown in Fig.6.8 after annealing at 400C for 30 secs in forming gas.

VII. PERFORMANCE LIMITED BY INTERBAND IMPACT IONZATION

The longitudinal electric field (longitudinal is the direction along which the charges are transferred, i.e. the direction parallel to the oxide-silicon interface) in a CCD varies from a minimum at the center of a gate to a maximum at the center of a gap. For this discussion, the magnitude of these electric fields are denoted by E_{min} and E_{Max}.

In order to achieve the highest possible charge transfer speed, E_{min} should be made as large as possible since the charge trasfer time under the gate is approximately given by the gate length divided by the drift velocity:

$$t_{gate} \approx L/v_d \approx L/\mu E_{min} \tag{7.1}$$

where $\mu = \mu(E_{min})$ is the field dependent drift mobility. A similar estimate can be made for the charge transfer time across the gap,

$$t_{gap} \approx d/v_d = d/\mu E_{Max} \tag{7.2}$$

where d is the length of the gap and $\mu = \mu(E_{Max})$. If the gate length is large, the transfer time under the gate may become diffusion limited instead of drift limited as given by Equation (7.1). The gate transit time for the diffusion limited condition is

$$t'_{gate} \approx L^2/D = (L/\mu E)(ELq/k_BT) \equiv (L/\mu E)\cdot F_{gate} \tag{7.3}$$

which is larger than the drift limited case, Equation (7.1), by a factor

$$EL/(k_BT/q) \equiv F_{gate} \tag{7.4}$$

before velocity saturation sets in at high electric field.

It is evident that the minimum electric field under the gate should be made as high as possible to obtain high transfer speed. E_{min}

has been estimated and was given by [47]

$$E_{min} \simeq 5(z_{ox}V/L^2) \tag{7.5}$$

where V is the d.c. voltage difference between two adjacent gates. For a CCD with overlapping gate or zero gap width, the maximum gap field is approximately given by

$$E_{Max} \simeq V/5z_{ox} \tag{7.6}$$

which must be smaller than the breakdown field of silicon, E_{BS}. Thus, the minimum field must be less than

$$E_{min} < 25(z_{ox}/L)^2 E_{BS} \tag{7.7}$$

The gate transfer time from Equation (7.1) using Equation (7.7) is then

$$t_{gate} > L^3/(25z_{ox}^2 \mu E_{BS}) \qquad L > L_{sat} \tag{7.8}$$

$$> L/v_{sat} \qquad L < L_{sat} \tag{7.9}$$

Here, L_{sat} is the gate length below which drift velocity saturation occurs due to hot electron effect while the gate voltage difference, V, is kept as high as possible but just below the silicon breakdown field, E_{BS}. Thus, using $v_{sat}=\mu E_{min}$, L_{sat} is then

$$L_{sat} = 5z_{ox}\sqrt{\mu E_{BS}/v_{sat}} \tag{7.10}$$

The adjacent gate voltage difference required to get the highest E_{min} under the gate before Si bulk breakdown occurs from Equations (7.5) and (7.7) is

$$V \simeq 5z_{ox}E_{BS} \tag{7.11}$$

These simple physical considerations give us the necessary design equations to determine the ultimate transfer time, which is limited by the transfer time under the gate. As a numerical example, let us assume that $E_{BS}=10^5$ V/cm above which excessive interband electron-hole pair generation would destroy the zeros. Let us take $z_{ox}=0.1\ \mu m$,

an electron surface mobility of μ=700 cm^2/Vs and a saturation velocity of v_{sat}=4x10^6 V/cm. Then,

$$L_{sat} = 2.09\ \mu m \tag{7.12}$$

For wide gate, such as L=10 μm, we have the following results.

E_{min} = 250 V/cm

V = 5 V

t_{gate} = 5.71x10^{-9} s drift limited

t'_{gate} = 5.52x10^{-8} s diffusion limited

For narrow gate, such as L=1 μm, drift velocity saturation sets in so that the gate transfer time decreases with L rather than L^3. Thus, Equation (7.9) must be used to estimate the transfer time. The results are given below.

E_{min} = 25 KV/cm

V = 5 V

t_{gate} = 2.5x10^{-11} s drift limited

t'_{gate} = 5.5x10^{-10} s diffusion limited

In both of these case, the E_{min} under the gate is sufficiently high that the charge transfer time under the gate is limited by drift rather than by diffusion.

The total charge transfer time is the sum of the gate and gap transfer times. However, for overlapping gates, the gap transfer time is quite small compared with the gate transfer time and can be neglected as a first estimate.

The gate transfer time given by Equation (7.8) shows that the ultimate limit is affected by the maximum tolerable electric field in the silicon, E_{BS}. The value we used for the numerical example, 10^5 V/cm,

is a rather high field which will give a electron-hole pair production rate of about 100 cm^{-1} per electron or an increase of electron density of 0.01 in a gate of 10^{-4} cm length. This 1% increase will become significant after passing through 100 charge transfer gates. In addition, the noise associated with the random pair production will also limited dynamic range. Thus, a smaller value of E_{BS} or applied voltage between adjacent gates may have to be used which would reduce the frequency response or increase the transfer time of the device.

Reliable interband impact ionization rate data at low electric field are not available. Some measurements have been obtained at low fields using junction gate field effect transistors [48]. Charge coupled devices offer alternative structures to get the low field data. A carousel or racetrack three-phase structure has been designed and fabricated with two-micron gap and relatively large gate length. The top view of a device is shown in Figure 7.1. The circulating charge packets will generate electron-hole pairs. The generated holes will flow into the p-type silicon substrate and produce a substrate current from which the hole ionization rate can be obtained. Since there is essentially no substrate current without electron-hole pair production, the substrate current measurement can detect very low hole currents at low impact ionization rates and low electric field. In addition, the CCD structure gives the impact ionization rate at the $Si\text{-}SiO_2$ interface where additional surface scattering mechanisms may influence the electric field dependence of the ionization rate. This project has just begun and will continue in a new contract.

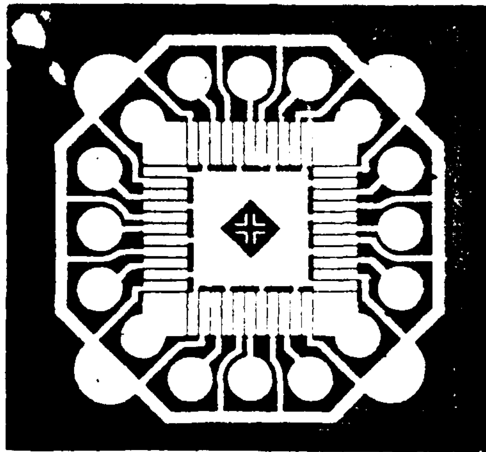


Figure 7.1 The top view of a three-phase silicon charge coupled device. The gap is 2 μm.

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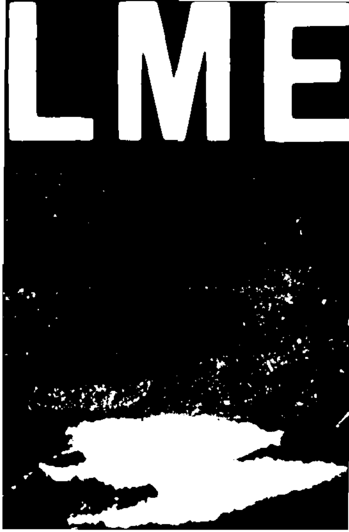
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