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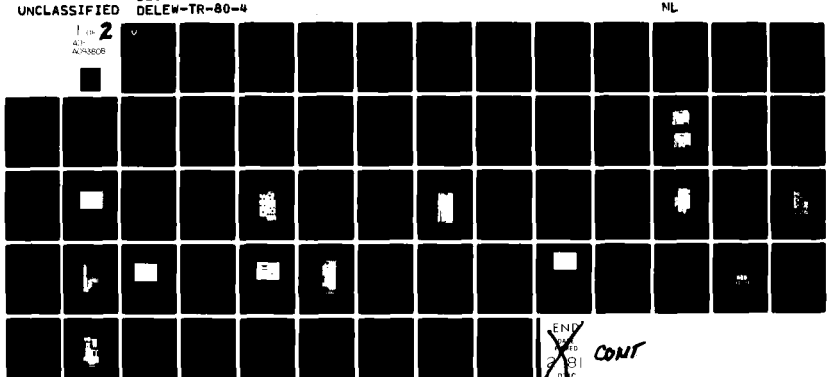

LEVEL II

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RESEARCH AND DEVELOPMENT TECHNICAL REPORT

DELEW-TR-80-4

# DIGITAL PHASE MEASUREMENT TECHNIQUES

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ELECTRONIC WARFARE LABORATORY



DECEMBER 1980



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This report describes the techniques and circuit designs necessary to implement the interface requirements to the (MASS) processor. A phase interferometer system is described which provides the frequency and a phase information which are then converted to digital data words. Then, specific digital processing techniques are used to obtain the angles-of-arrival which are then available for display and for transferring to the MASS processor.

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# DIGITAL PHASE MEASUREMENT TECHNIQUES

## INTRODUCTION

The thrust behind the work described in this report is to design a special purpose preprocessing unit that will interface to a Modular Adaptive Signal Sorter (MASS) signal processor.

The long development cycle for military systems, combined with the highly dynamic environment in which they must operate, present a major challenge to an electronic warfare system designer - to design a system which can evolve after deployment to meet future operational requirements. The specific architecture of the MASS electronic support measures (ESM) signal processor[1] is designed to meet this challenge. It features a completely modular organization in which the types and numbers of modules can be selected to match the specific application. Growth capability is provided by adding modules for increased throughput or developing new modules for increased functional capability. The internal control of the processor adaptively monitors the status of all processing modules as part of a dynamic resource allocation function.

The MASS processor is organized as a distributed microprocessor architecture in which each microprocessor-based processing module is configured for a portion of the overall ESM signal processing function. Typical modules are a frequency/azimuth pulse sorter, deinterleaver, "exotic" signal processor, pulse train tracker, librarian, and supervisor. Modules operate with two data buses. One is a very high speed pulse data bus carrying monopulse parameters, the other is a lower capacity control bus. Incoming data must be in digital form, and represent frequency, angle of arrival and time of arrival, as well as other information.

This report describes the techniques and circuit designs necessary to implement the interface requirements to the MASS processor. A phase interferometer system is described which provides frequency and phase information which are then converted to digital data words. Specific digital processing techniques are then used to obtain the angles of arrival (AOA) which become available for display and for transfering to the MASS processor. A system block diagram is shown in Figure 1.

## DISCUSSION

a. Phase Interferometer Techniques. Many electronic warfare applications require line-of-bearing (LOB) information on a particular emitter or on a number of emitters. One of the most widely used techniques for obtaining AOA data to compute LOB's is phase interferometry. Figure 2 illustrates the basic geometric relationships governing a simple phase interferometer. The operating bandwidth of an interferometer is usually restricted to one octave or at most, a two-to-one ratio between the upper and lower frequency band. This frequency range limitation is related to the system performance and is dependent on the phase error budget and wavelength. From Figure 2,

[1] Contract DAAK20-79-C-0516, RCA Corporation, Camden, NJ

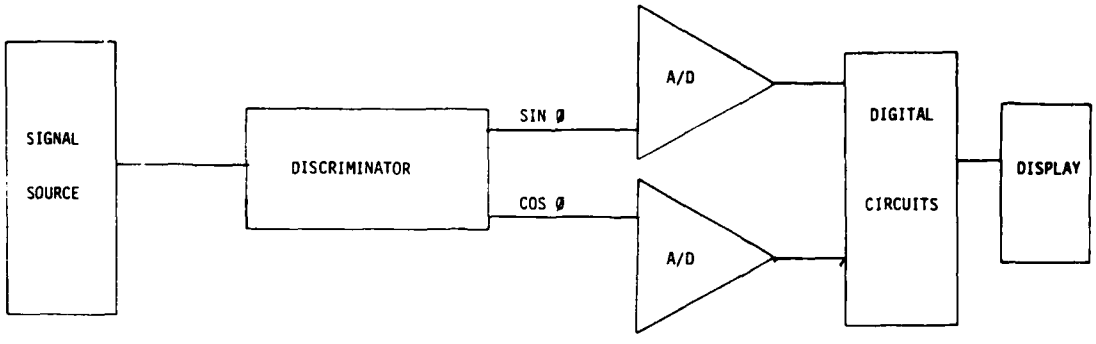



Figure 1. System Block Diagram

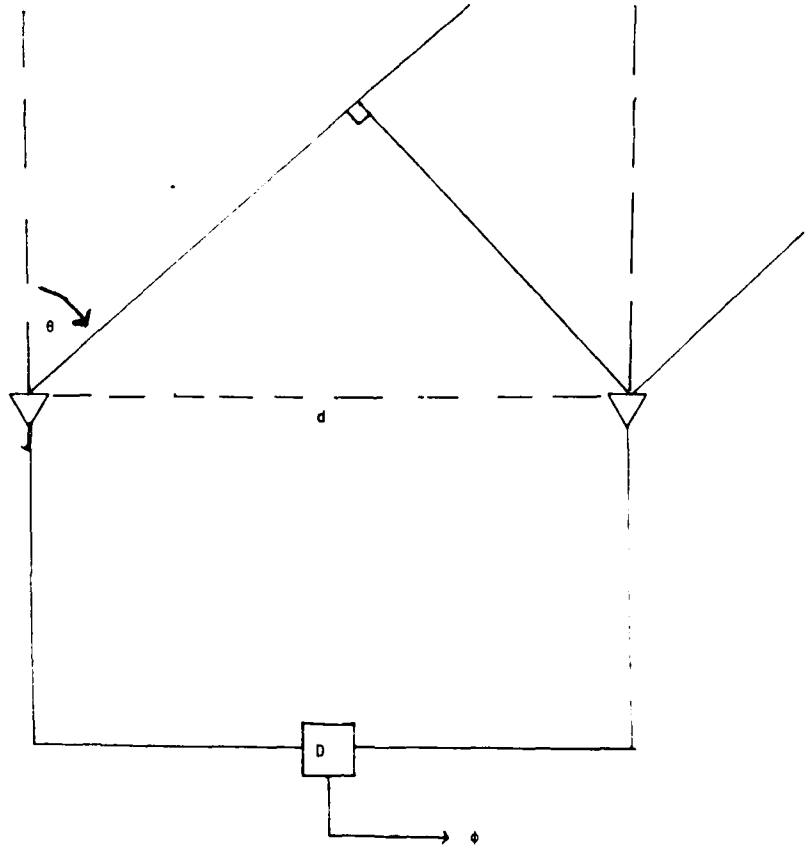



Figure 2. Phase Interferometer Baseline

$$\phi = \frac{2\pi d}{\lambda} \sin \qquad (1)$$

$$\Delta\phi = \frac{2\pi d}{\lambda} \cos \qquad (2)$$

$\theta$ = incident AOA, and $\phi$ = electrical phase angle. Therefore, for a nominally constant phase error budget, the direction finding (DF) error is:

$$\Delta\theta = \frac{\Delta\phi}{\frac{2\pi d}{\lambda} \cos\theta} \qquad (3)$$

for the case where $\cos\theta \simeq 1$, $\Delta\theta$ will vary by a factor of two over an octave band.

An electrical versus mechanical angle amplification factor ($\alpha$) exists for $d > \lambda/6$. Mechanical AOA measurement accuracy is determined by the selected antenna separation (amplification factor) and the electrical measurement resolution. For example:

$$\text{Gain} = \alpha = \frac{2\pi d}{\lambda} \cos\theta \qquad (4)$$

Accurate AOA measurements are achievable for moderate antenna baselines, i.e., $\lambda < d < \lambda/2$. The amplification factor ($\alpha$) also reduces the effects of electrical phase measurement noise, thus yielding a DF system signal-to-noise (S/N) sensitivity improvement of $(1/\alpha)$.

Ambiguities exist for antenna baseline separations (d) that are greater than $\lambda/2$, or if $d/\lambda > 1/2$. To resolve ambiguities, a baseline less than the half wavelength of the highest frequency in the band of interest must be available. The controlling factor for ambiguity performance is the number of antennas used for a given DF accuracy. Figure 3 shows a multiple antenna baseline configuration. For this particular baseline,

$$\phi_1 = \frac{2\ d_1}{\lambda} \sin\theta \qquad (5)$$

$$\phi_2 = \frac{2\pi\ d_2}{\lambda} \sin\theta \qquad (6)$$

and;

$$\phi_{2-1} = \phi_2 - \phi_1 = \frac{2\pi(d_2 - d_1)}{\lambda} \sin\theta \qquad (7)$$

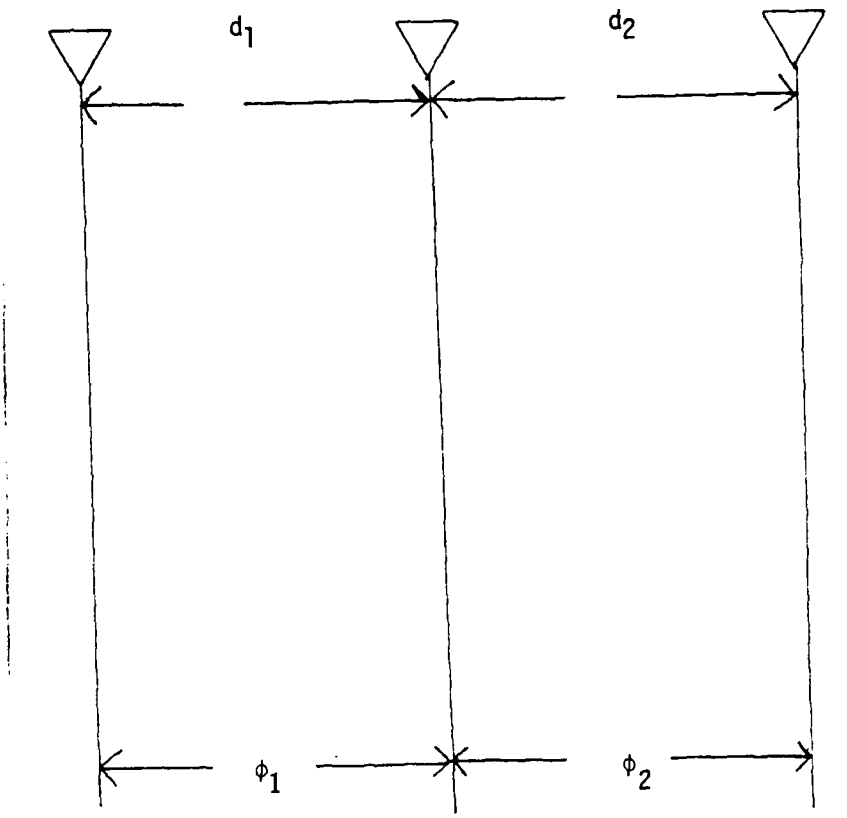



Figure 3. Multiple Antenna Baseline

The phase difference between two measurements $d_2$ and $d_1$ to determine $\phi_2 - \phi_1$ corresponds to a phase measurement that could be achieved if an antenna pair is spaced a distance $d_2$ and $d_1$ apart. An unambiguous condition exists for this baseline when

$$\frac{d_2 - d_1}{\lambda} < \frac{1}{2} \qquad (8)$$

The probability of an ambiguity error can be reduced when operating against fixed frequency emitters by averaging a number of phase measurements prior to performing the AOA computation.

The phase interferometer configuration provides us with the geometry for ultimately obtaining emitter AOA. The next step is to transform the energy impinging on the antennas into an electrical phase angle measurement. That is, the electromagentic wavefront of an incoming signal will reach each antenna of the interferometer at a slightly different time, resulting in a phase difference which can be measured.

b. Electrical Phase Angle Measurement

Mixers

A technique for measuring the phase angle of a signal is to use mixers in a discriminator configuration. A phase discriminator accepts two radio frequency (RF) input signals of the same frequency, and provides an output which contains relative phase and amplitude information. In a typical discriminator configuration, identical frequencies are fed to the mixer local oscillator (LO) and RF ports, and a dc output, proportional to the phase difference between the two signals, will appear at the IF port (Fig. 4).

A $90^{o}$ hybrid mixer (Fig. 5) produces an output voltage proportional to the sine of the phase difference between the two identical input frequencies:

$$V_0 \text{ (DC)} = K_1 \sin (\phi_I - \phi_R) \qquad (9)$$

where $K_1$ depends on the input power and diode characteristics, and $(\phi_I - \phi_R)$ is the phase angle difference between the two inputs. A typical value of $K_1$ at $\phi$ dBm input power is 500 MV/MW.[2] This is the voltage sensitivity when loaded into 1k ohm.

A $180^{o}$ hybrid mixer (Fig. 6) and a double-balanced mixer produce a dc output proportional to the cosine of the phase difference between two identical frequencies:

$$V_0 \text{ (DC)} = K_1 \text{ cosine } (\phi_L - \phi_R) \qquad (10)$$

The $90^{o}$ hybrid mixer produces a dc null when the input signal phases are equal. The $180^{o}$ hybrid, and the double-balanced mixers produce a maximum negative output when the input phases are equal.

[2] Anaren Data Catalog Publication 1976

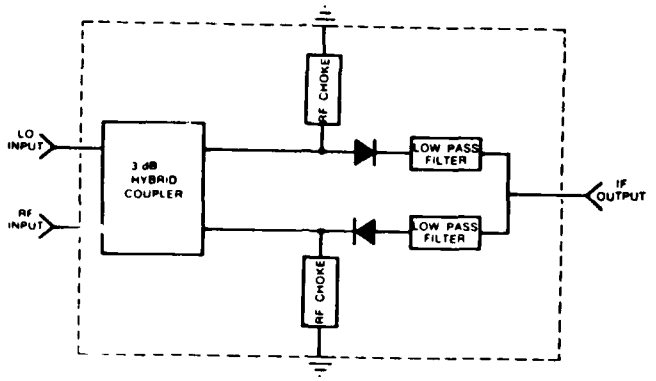



Figure 4. Typical Discriminator Circuit

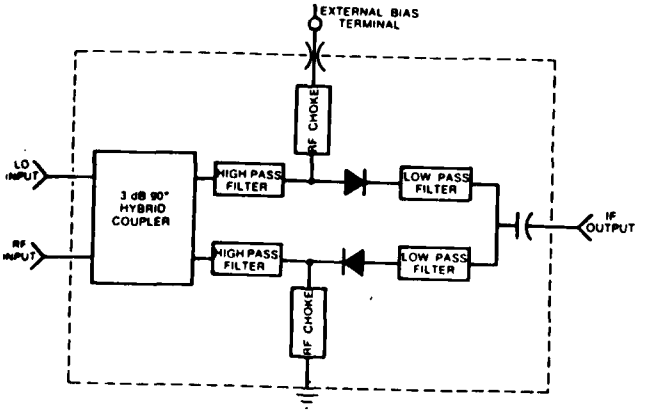



Figure 5. A $90^{O}$ Hybrid Mixer

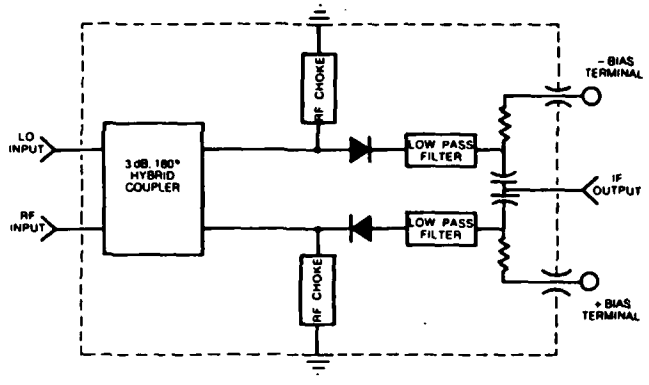



Figure 6. A 180° Hybrid Mixer

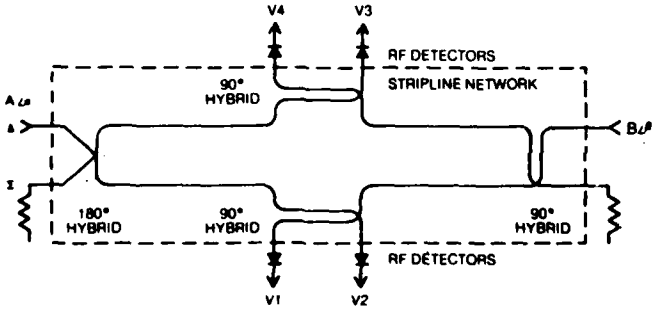



Figure 7. A Phase Discriminator (Correlator) Network

The real-world requirements of modern electronic warfare receivers have placed considerable stress on mixer requirements. Specific critical areas are: biasing of the mixer (which bears on the LO dynamic range and spurious performance); rejection of spurious signals (important for dynamic range requirements); LO to radio frequency (RF) isolation (important to reradiated LO power requirements); voltage standing-wave ratio (VSWR) (influences phase and amplitude tracking); and focusing of image signal energy (which is critical to phase and amplitude tracking requirements).

The passive RF portion of Figure 7 is a two-channel processing network. Two RF input signals (A and B) are divided to the four output ports. The resultant output are "square" detected and have the amplitude and phase relationships shown in Figure 8. These video voltages are a function of the relative phase between inputs A and B ($\phi = \delta - B$) and are proportional to:

$$V_1 = (A^2 + B^2) + 2\,AB \cos \phi \tag{11}$$

$$V_2 = (A^2 + B^2) - 2\,AB \cos \phi \tag{12}$$

$$V_3 = (A^2 + B^2) + 2\,AB \sin \phi \tag{13}$$

$$V_4 = (A^2 + B^2) - 2\,AB \sin \phi \tag{14}$$

Outputs $V_1$ through $V_4$ can be combined in differential amplifiers as shown in Figure 9. These two resulting bipolar voltages are of the form:

$$I - k\,AB \cos \phi \tag{15}$$

$$Q = k\,AB \sin \phi \tag{16}$$

These two outputs are, in fact, the in-phase (I) and quadrature (Q) components of the correlation of the two RF signals over a time period corresponding to the video bandwidth (30 ns for a 15 MHz video bandwidth). To increase the correlation time, reduce the bandwidth.

From equations (15) and (16) we can form

$$\frac{Q}{I} = \frac{k\,AB \sin \phi}{k\,AB \cos \phi} \tag{17}$$

and,

$$\text{TAN } \phi = Q/I \tag{18}$$

therefore,

$$\phi = \text{TAN}^{-1} \left(\frac{Q}{I}\right) \tag{19}$$

or,

$$\phi = \text{COTAN}^{-1} \left(\frac{I}{Q}\right) \tag{20}$$

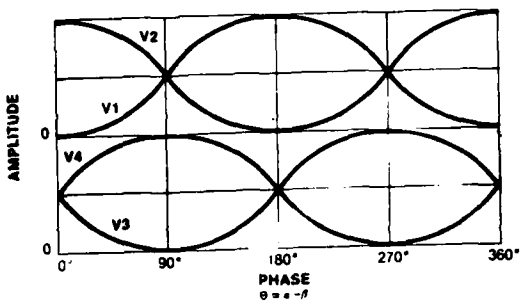



Figure 8. Instantaneous Video Amplitude Versus Phase

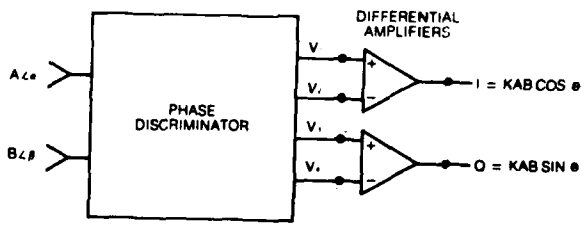



Figure 9. Phase Discriminator Video/Amplifier Block Diagram

For constant frequency signals and equations (15) and (16),

$$\phi = \text{TAN}^{-1} \frac{(\sin \phi)}{(\cos \phi)} \qquad (21)$$

and,

$$\phi = \text{COTAN}^{-1} \frac{(\cos \phi)}{(\sin \phi)} \qquad (22)$$

Equations (21) and (22) are graphically illustrated in the complex plane representation of Figure 10.

SAW Devices

Another method for implementing a phase interferometer system is via use of surface-acoustic-wave (SAW) devices to implement Chirp transforms and preserve the electrical phase angle measurement.

SAW devices consist of piezoelectric crystal substrates (quartz or lithium niobate), with metalized interdigital transducers applied to a highly polished surface. A SAW's physical size is largely a function of the frequency of operation, bandwidth or delay requirements. In Figure 11, electromagnetic energy, applied to the injection transducer, is transformed to acoustic energy. The acoustic signal propagates primarily along the surface of the crystal and is transformed back to an electromagnetic signal at the detection transducer. Since the conventional interdigital transducer radiates acoustic energy equally well in either direction along the axis of propagation, end absorbers are required to suppress acoustic signals that do not travel directly from the input to the output transducer.

The frequency of operation of a SAW device is a function of the electrode spacing and the bandwidth is inversely related to the overall length of the transducers. SAW devices are currently being used as bandpass filters, delay lines, and compression filters; and are readily reproducible due to their fabrication, which consists of thin film and application of photolithographic techniques.[3]

A SAW Chirp form[4] is an analog signal processing technique for producing Fourier transforms in real time. The transform algorithm (Fig. 12) begins with the multiplication of the input signal by a linear FM (Chirp) waveform. The product signal is then filtered through a linear FM compression filter having the same Chirp slope as the premultiply waveform. This process produces an output signal that corresponds in both amplitude and phase to the Fourier transform of the input signal. The linear frequency modulation may be removed when necessary through the final multiplication by the linear FM waveform.

[3] Skudera, W.J. et al, "Acoustic Surface Wave Fabrication Techniques and Results," ECOM-TR-4333, Aug 75.

[4] Rabiner, E.R. et al, "Chirp Z-Transform and Its Applications," Bell System Tech Jl., Vol 48, 1979, PP 1249 - 1293

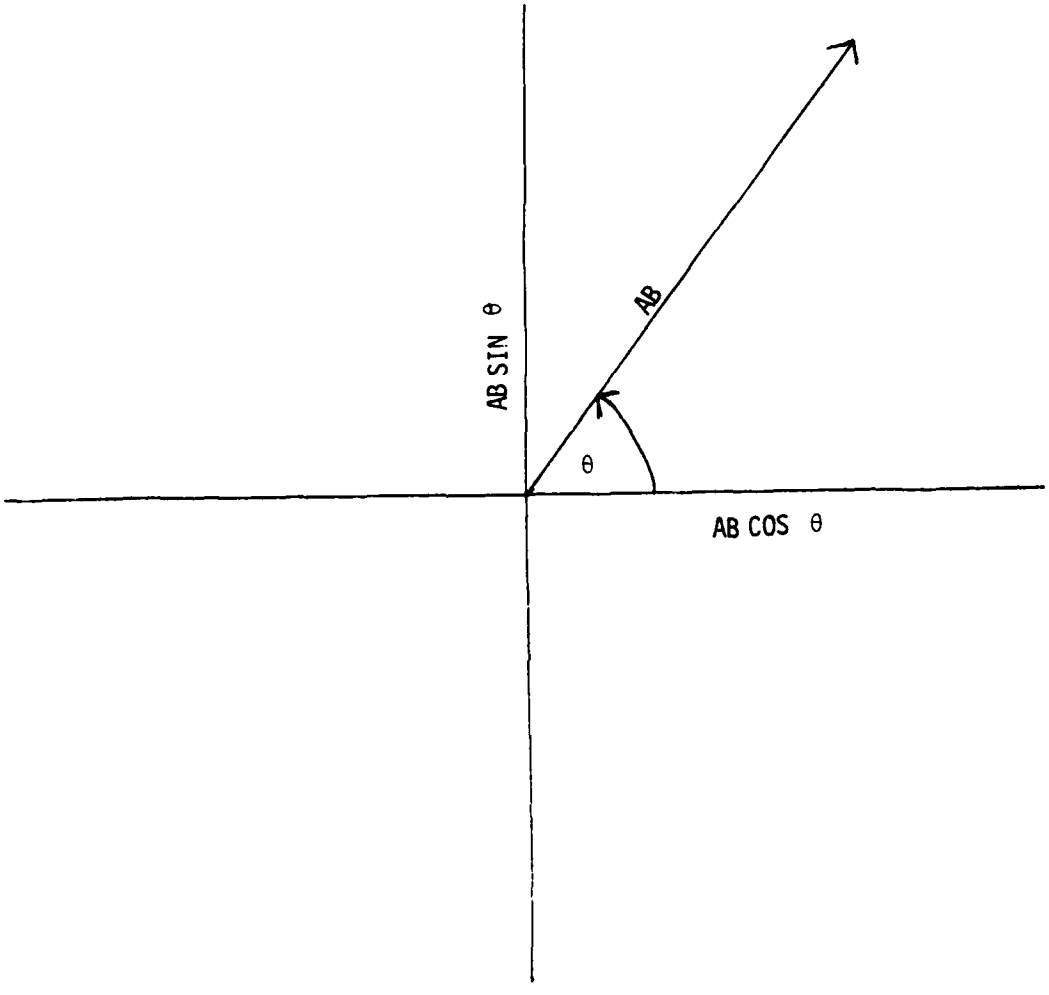



Figure 10. Phase Angle Representation in Complex Plane

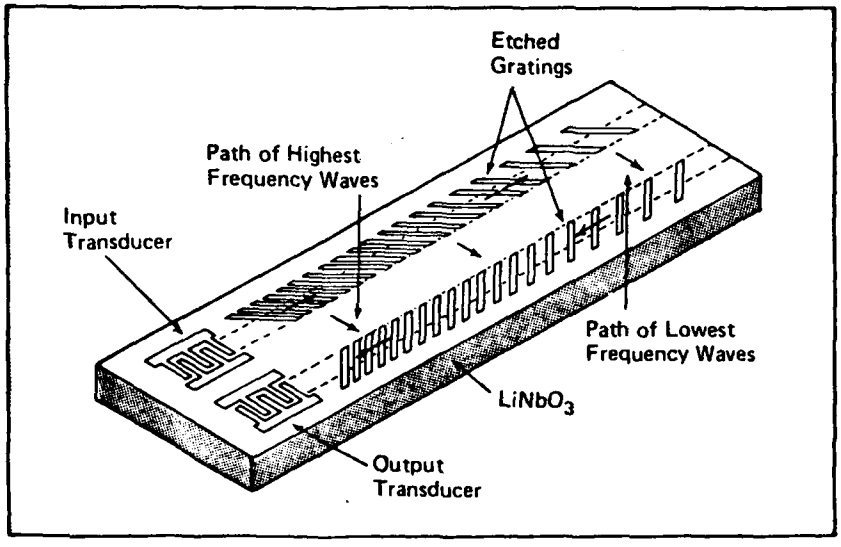
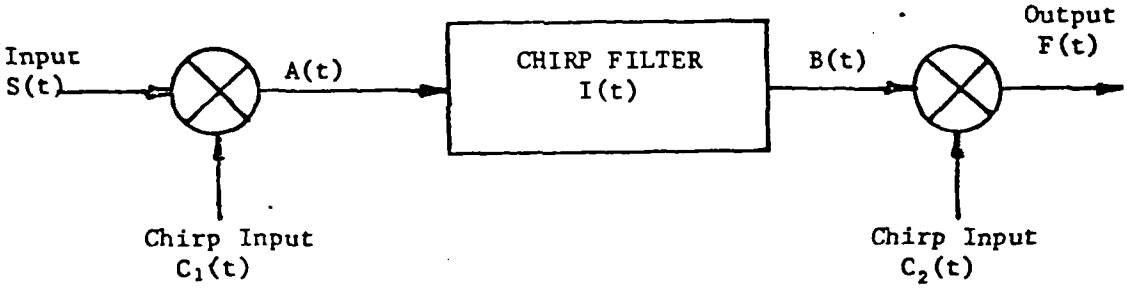



Figure 11. Surface Acoustic Wave (SAW) Device




where

$$C_1(t) = \begin{cases} \exp\left(j2\pi\left[f_1 t - \frac{\Delta F t^2}{2\Delta T}\right]\right), & |t|<\Delta T/2 \\ 0, & |t|>\Delta T/2 \end{cases}$$

$$I(t) = \begin{cases} \exp\left(j2\pi\left[(f_1 + f_0)t + \frac{\Delta F T^2}{2\Delta T}\right]\right), & |t|<\Delta T \\ 0, & |t|>\Delta T \end{cases}$$

$$C_2(t) = C_1(t).$$

Figure 12. Basic Chirp-Z Transform

The premultiplied Chirp and the matched compression filter can be implemented very effectively using SAW reflective array compressor (RAC) filter technology.[5]

Klose and Skudera[6] recently described a novel method for using SAW devices in a compressive interferometer system. They also implement a Chirp-Z transform and maintain the phase information (Fig. 13). Channels 1 and 2 are fed with identical phase-shifted signals similar to those obtained by connecting the channels to individual, spatially separated antennas. The Chirp waveform required to multiply the input signals is generated by impulsing an up-Chirping SAW pulse compression line (PCL). Chirp, PCL 1, expands the impulse source into a linear FM sweeping signal, which multiplies the input signals on both processor channels. The PCL 2, matched filters, perform the actual transform processing, and output the signal spectrum components as a series of RF pulses of different nominal center frequencies. The output pulse time-ordering, relative to the start of the Chirp period, is linearly related, in reverse order, to the frequency of the input component signals. Basic energy detection on either channel permits determination of relative signal frequency, amplitude, time-of-intercept, and limited modulation from one Chirp period to another.

For the phase interferometer implementation, the undetected RF signal pulses are passed to a linear, wideband, phase discriminator or correlator. The output in-phase ($\Delta I$) and quadrature ($\Delta Q$) signals are video detected. The relative amplitude and polarity of the detected $\Delta I$ and $\Delta Q$ signal pulses are a complex vector representation of the phase difference between the component input signal being processed. The output of the phase discriminator is signal-amplitude dependent, and the phase-difference angle is determined by computing the arc tan ($\Delta Q/\Delta I$).

Digital Techniques

Since phase discriminators were not physically available for this task, a Hewlett-Packard 203A Phase Generator was used to simulate the outputs of the discriminator. Figure 14 is a system block diagram of the brassboard for the digital phase measurement. Two signals, in phase and quadrature, are digitized and translated into the required binary code. These two signals are magnitude compared and checked for sign. The binary information is stored in a Random Access Memory (RAM) buffer. The smaller number is digitally divided by the larger number, the resultant quotient forms the address of a look-up table in which the base information is stored in Read Only Memory (ROM). The electrical phase angle is then displayed on a Dot Matrix display.

c. Analog-to-Digital Conversion Technique. One of the main problems facing the designer of a fast signal processor is the choice of analog-to-digital (A/D) converter. Counting, dual slope, and successive-approximation conversion techniques are all too slow for a high speed sampling rate application such as this.

[5] Webb, D.C., "SAW Filters Simplify Signal Sorting," Microwave System News, Sep 1978, P 75.

[6] Klose, D.R. and Skudera, W., "Dual Channel SAW Compressive DF Techniques," Army Science Conference, West Point, NY, June 1980.

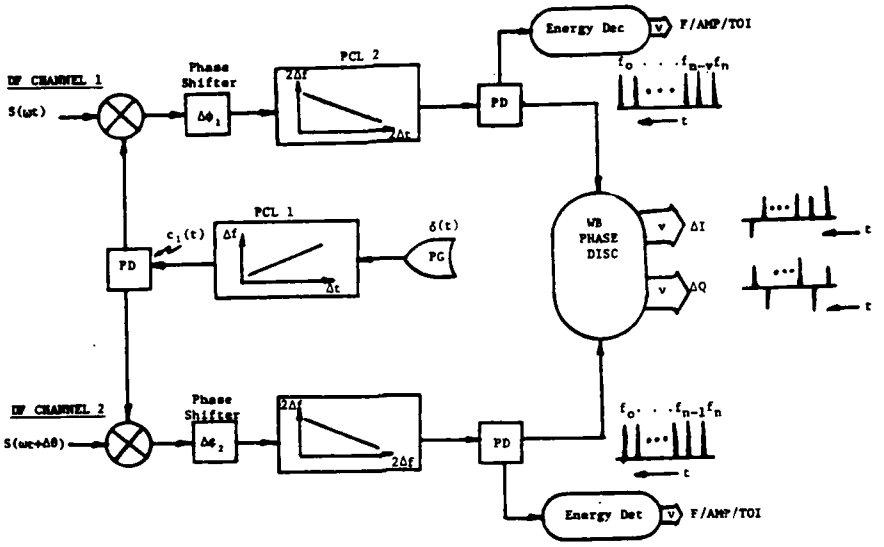



Figure 13. Compressive Interferometer

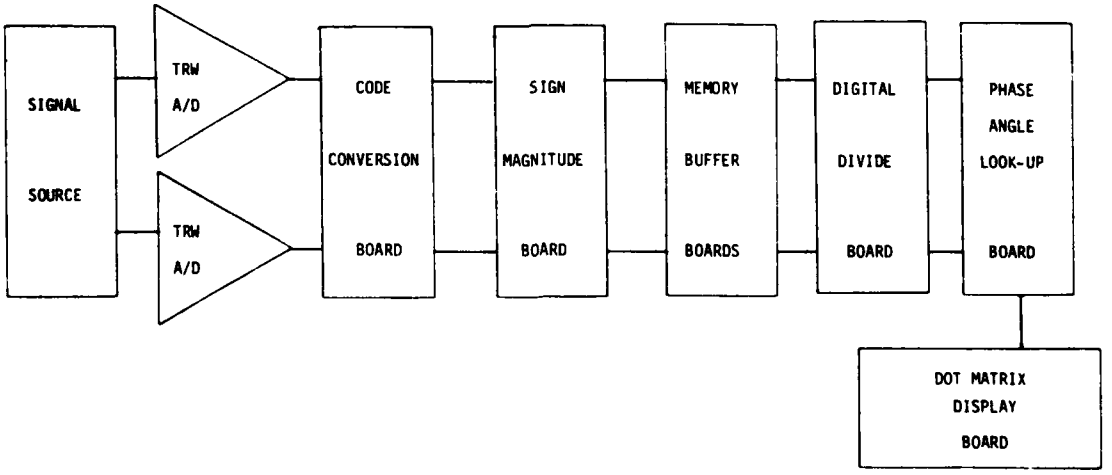



Figure 14. System Expanded Block Diagram

The parallel-comparator analog to digital-converter is the fastest of all converters; its operation is easily understood if one refers to the A/D converter of Figure 15. The analog voltage $V_a$ is applied simultaneously to a bank of comparators with equally spaced thresholds. This type of processing is called bin conversion, because the analog input is sorted into a given voltage range of $V_0$ voltage bin, determined by the thresholds of two adjacent comparators. Note that the comparator outputs, W, take on a very distinctive pattern; logic 0 for all comparators with thresholds above the input voltage, and logic 1 for each comparator whose threshold is below the analog input. The truth table is given in Table 1. Conversion time is limited only by the speed of the comparator and the priority encoder. Using an Advanced Microdevices AMD686A Comparator and a TI-147 Priority Encoder, conversion delays on the order of 20 ns can be obtained.

TABLE 1. TRUTH TABLE FOR A/D CONVERTER OF FIGURE 15.

| Inputs | | | | | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|
| $W_7$ | $W_6$ | $W_5$ | $W_4$ | $W_3$ | $W_2$ | $W_1$ | $Y_2$ | $Y_1$ | $Y_0$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The speed requirements of our phase interferometer processor dictated that we use the TRW TDC 1007J 8-bit flash A/D converter, which has a 33 ns conversion time. The converter can be purchased with its own interface printed circuit (PC) board. Two A/D converter boards were used in this processor (Fig. 16), one for the in-phase analog signal, and the other for the quadrature signal. The PC board contains all the circuitry necessary for connecting the A/D converters to any system (Figs. 16, 17, 18). The converters can accurately sample, without an external sample and hold circuit; input signals with frequency components up to 7 MHz. A single convert pulse controls the unit operation, consisting of 255 sampling comparators combining logic and a output buffer register (Fig. 19). Recovery from scale input occurs within 20 ns. Controls are provided for straight binary or offset two's complement output coding, in true or inverted sense. Figure 20 shows the inverted, offset two's complement outputs for the TRW A/D converters. The bottom trace is the sample or convert signal input. This signal starts the conversion process.

d. Code Conversion. The binary output of both A/D converters is in an inverted, offset two's complement format. This binary output was not desirable for further processing in our system; therefore, we designed a circuit that would translate the offset two's complement binary outputs of the converters into a normal format.

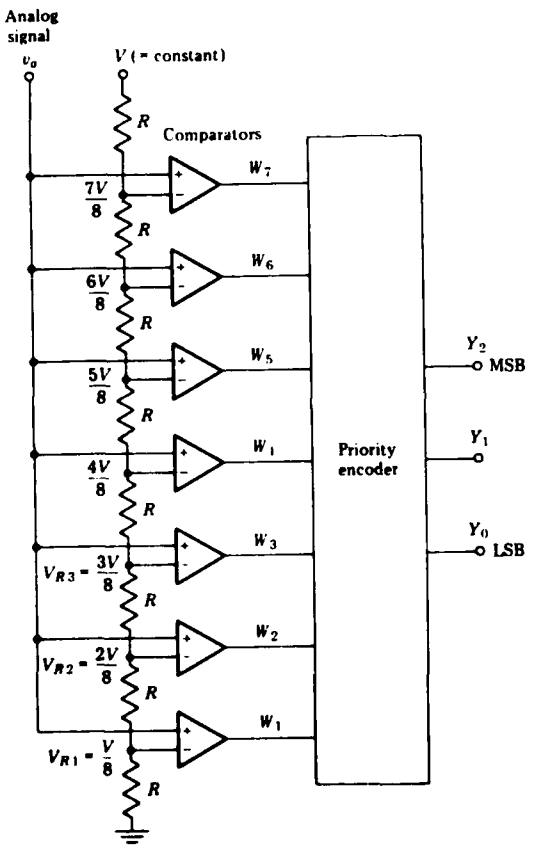



Figure 15. A 3-Bit Parallel Comparator A/D Converter

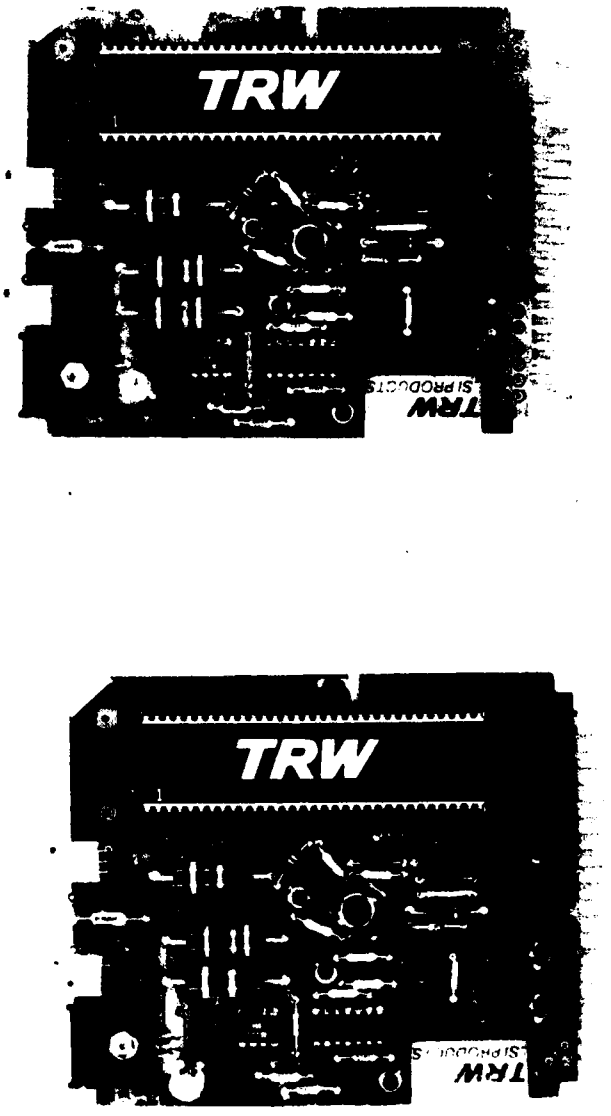



Figure 16. Two A/D Flash Converter Boards

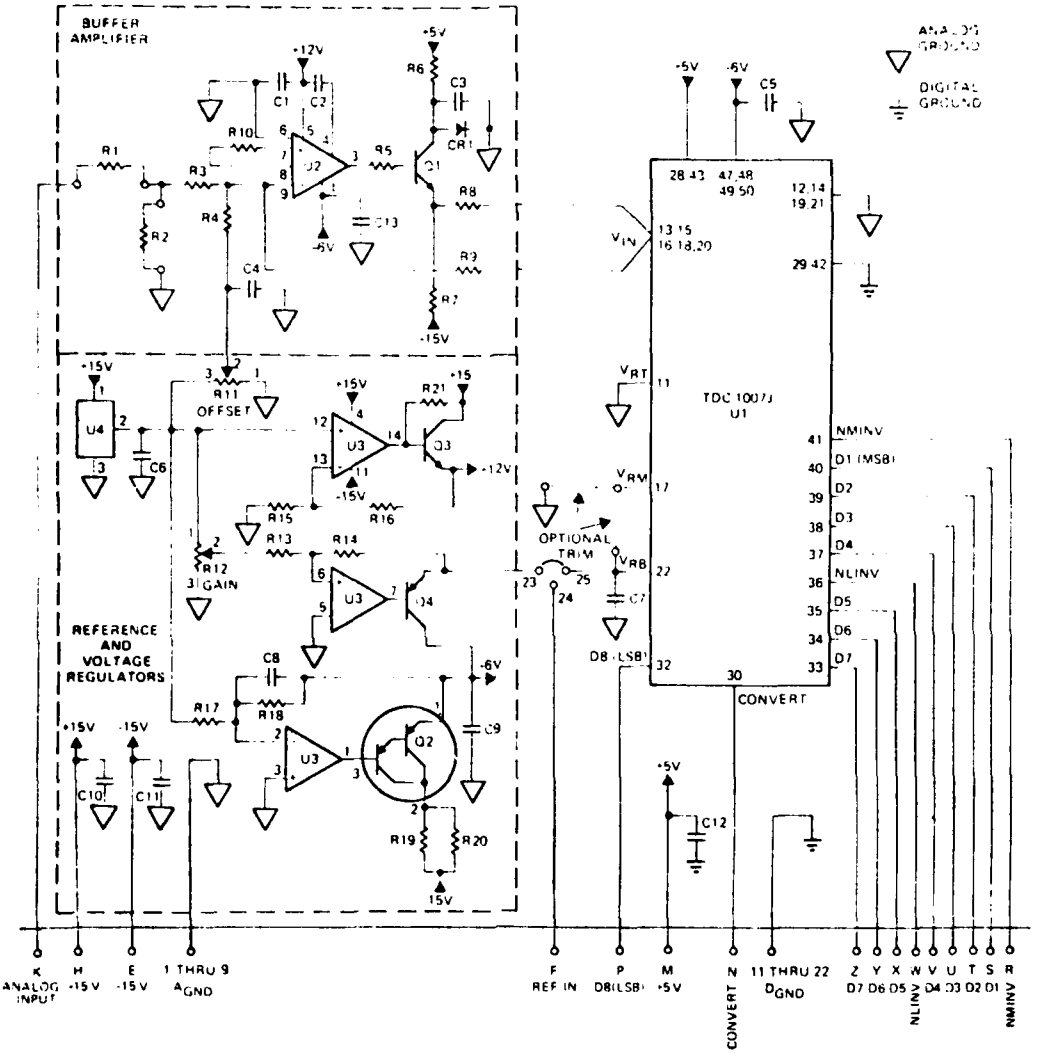



Figure 17. TDC1007 PCB Schematic

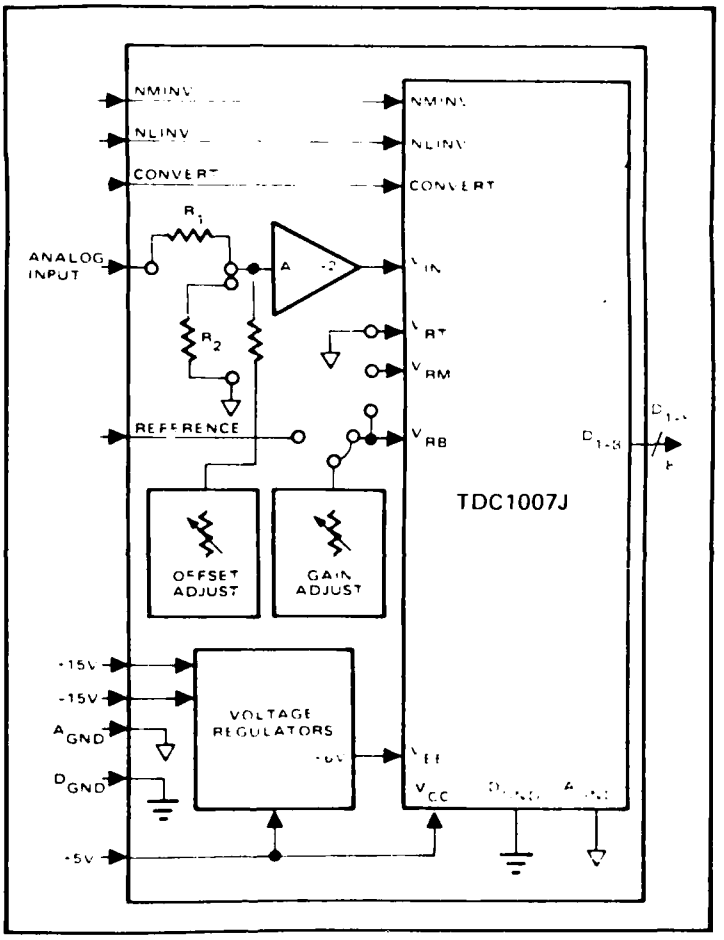



Figure 18. PC Board Block Diagram

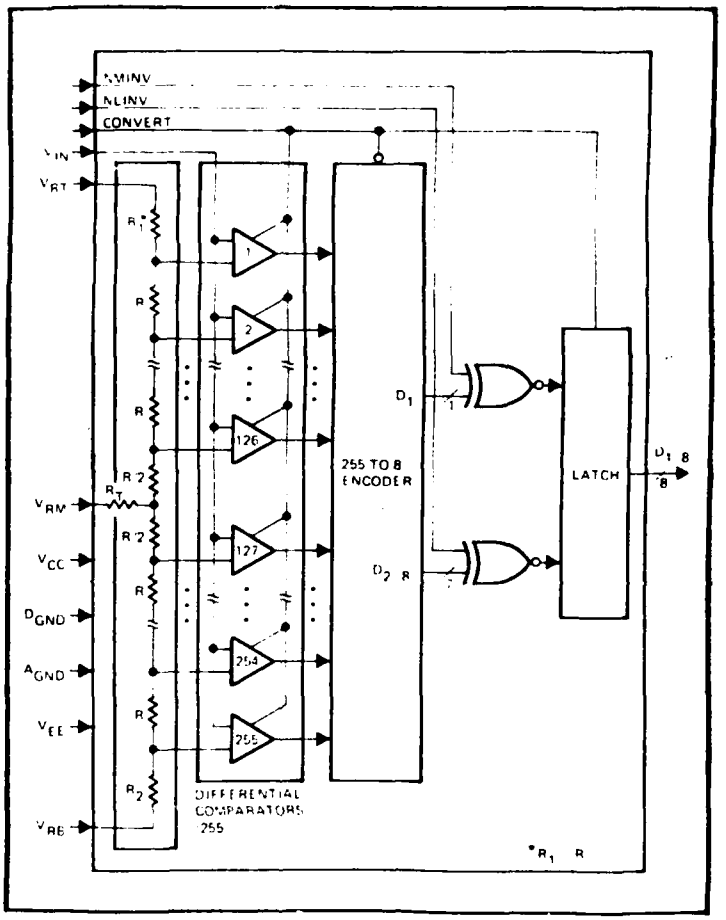



Figure 19. TRW Monolithic 8-bit A/D Converter

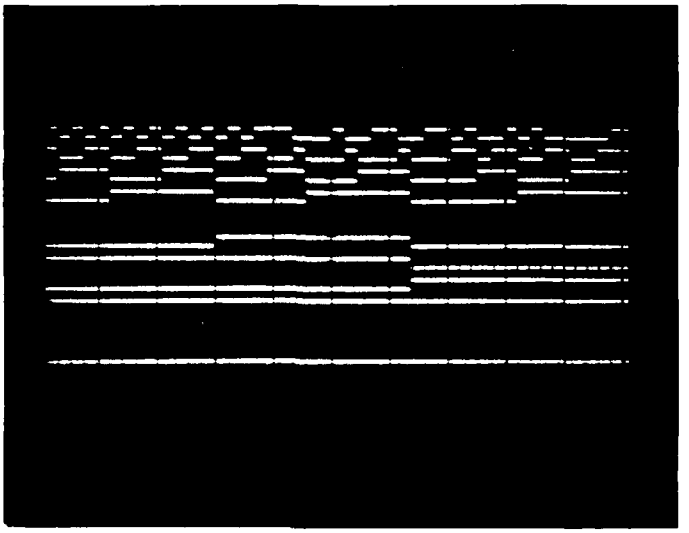



Figure 20. A/D Converter Binary Outputs and Sample Pulse

The normal two's complement numbering system is a technique for describing positive and negative numbers in a convenient notation and has the advantage of only having one representation for the number "zero." Two's complement numbers can also be added or subtracted without concern for the sign of each number since the result will be correct in two's complement notation. In this format, the sign bit, which is tne most significant bit (MSB), is a logical "0" for positive numbers and logical "1" for negative numbers.

A block diagram of the code conversion circuit is illustrated in Figure 21, and the actual circuit board is shown in Figure 22. The circuit is designed to add a constant 8-bit value to each of the digitized outputs of the A/D converters. Recall, that the A/D outputs represent the digitized values of the in-phase and quadrature signals of the phase interferometer.

The heart of the code conversion board is an AM25LS181 4-bit Arithmetic Logic Unit (ALU) function generator integrated circuit. This circuit is a 4-bit high-speed parallel device and the schematic is illustrated in Figure 23. When the mode control (M) is LOW, sixteen arithmetic operations can be performed under the control of the four select inputs. For an ADD operation, the select lines S0, S1, S2, and S3 have the pattern 1001. An internal full look-ahead carry scheme is used for high-speed arithmetic operations, and provision is made for further look-ahead by including both carry propagate (P) and carry generate (G) outputs. An open collector output, A = B, is used to signal the equivalence of the two parallel words. The open collector feature allows for the equivalence function to be expanded as a wire-AND connection for larger word lengths.

In many systems, the carry output, $C_{n+4}$, is connected to the next higher $C_n$ to provide ripple block arithmetic. Figure 24 is an illustration of the 8-bit adder circuit used to convert the outputs of each of the A/D converters. The A-inputs are tied to the A/D outputs, and the B-inputs have the constant value to be added.

The ALU can be used with either active HIGH or active LOW inputs and can be ripple expanded or full look-ahead expanded in either mode. The connection pattern is identical for either logic representation.

The code conversion circuitry (Fig. 21) examines the 8-bits of the A/D converters. If the MSB is a logical zero, nothing is done and all 8-bits are passed on to the next board. If the MSB is a logical one, the seven least significant bits (LSB) are inverted and a binary one (00000001) is added to the number to complete the conversion. The multiplexers are enabled by the MSB and both the inputs and outputs are buffered on the board.

e. Magnitude Test. The 8-bit words in two's complement form, representing the electrical phase difference of the interferometer, are next sent from the code conversion board to a circuit that will perform a magnitude comparison. This is done to condition the digital data so that it can be handled by the divide board.

A block diagram of the magnitude test circuits for the in-phase and quadrature data are shown in Figure 25 and the wire-wrap circuit board in Figure 26. Each of the 8-bit data words comes off the bus and is buffered to provide the necessary drive characteristics. The status of the MSB is checked

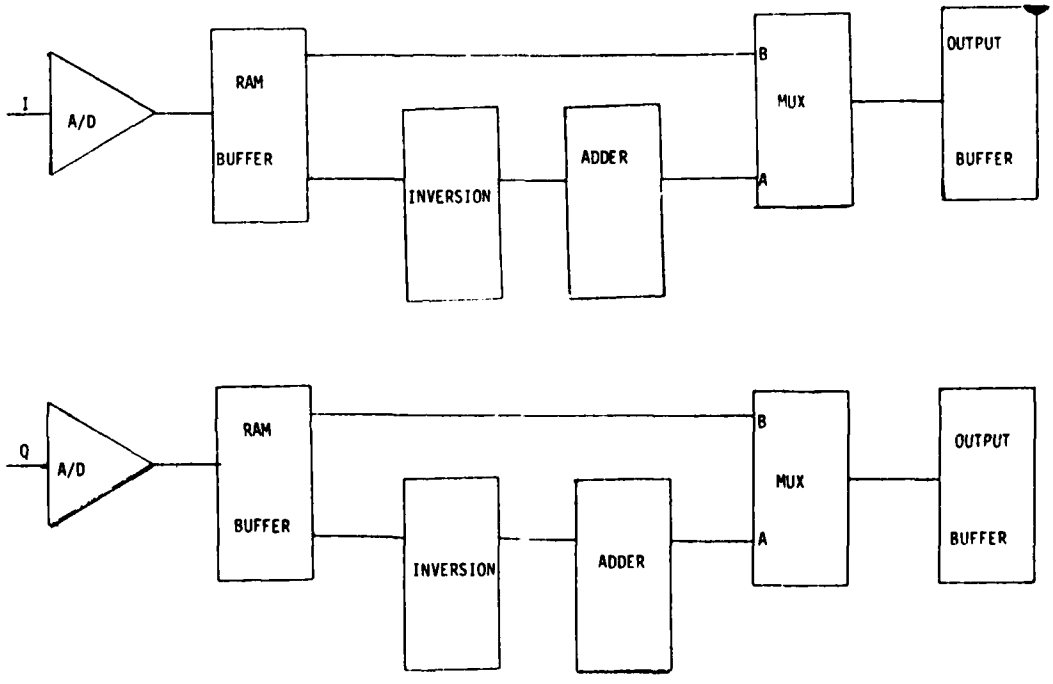



Figure 21. Code Conversion Block Diagram

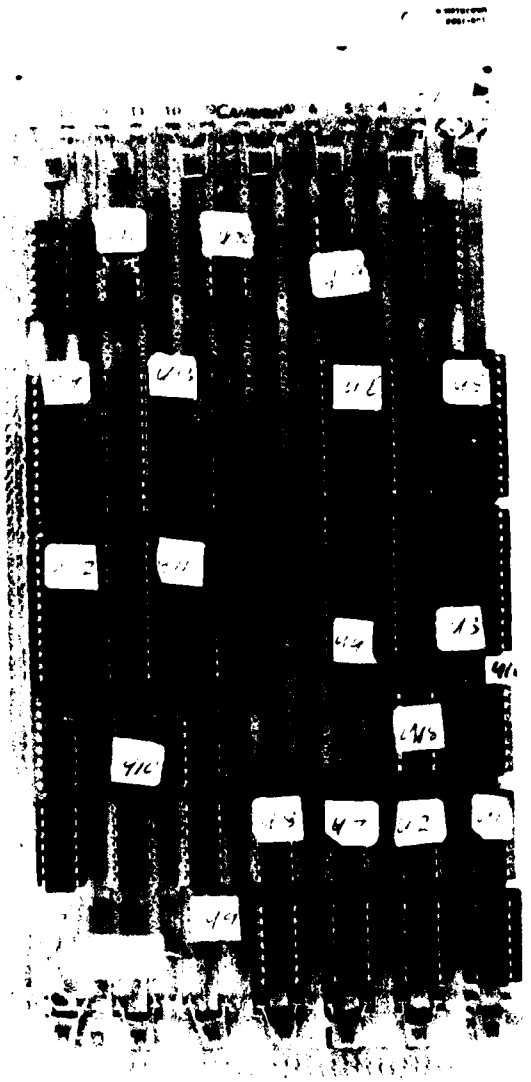


Figure 22. Code Conversion Circuit Board

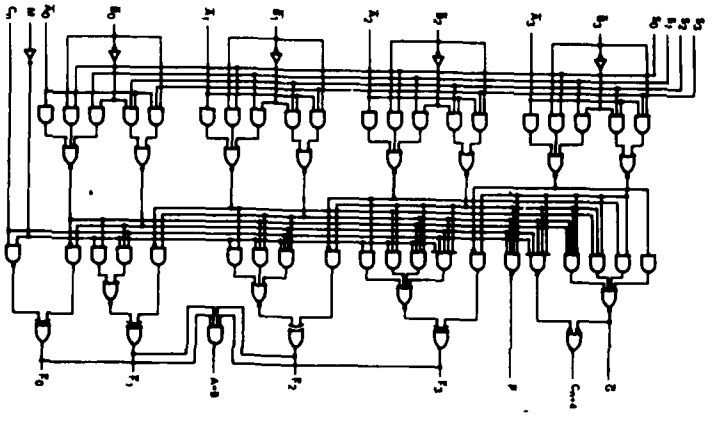


Figure 23. AM25LS181 4-bit ALU/Function Generator

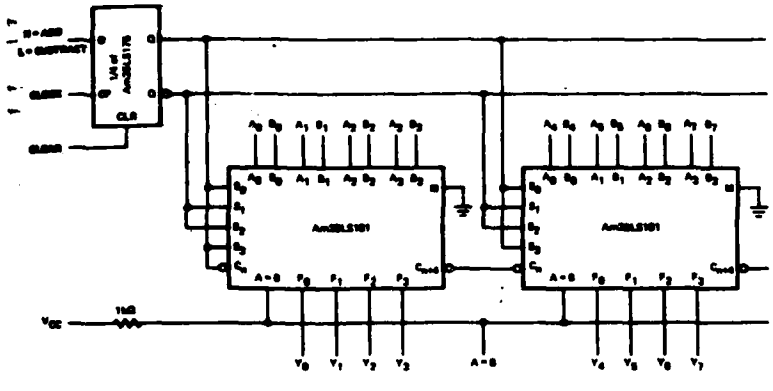


Figure 24. 8-bit Adder/Subtractor (Two's Complement)

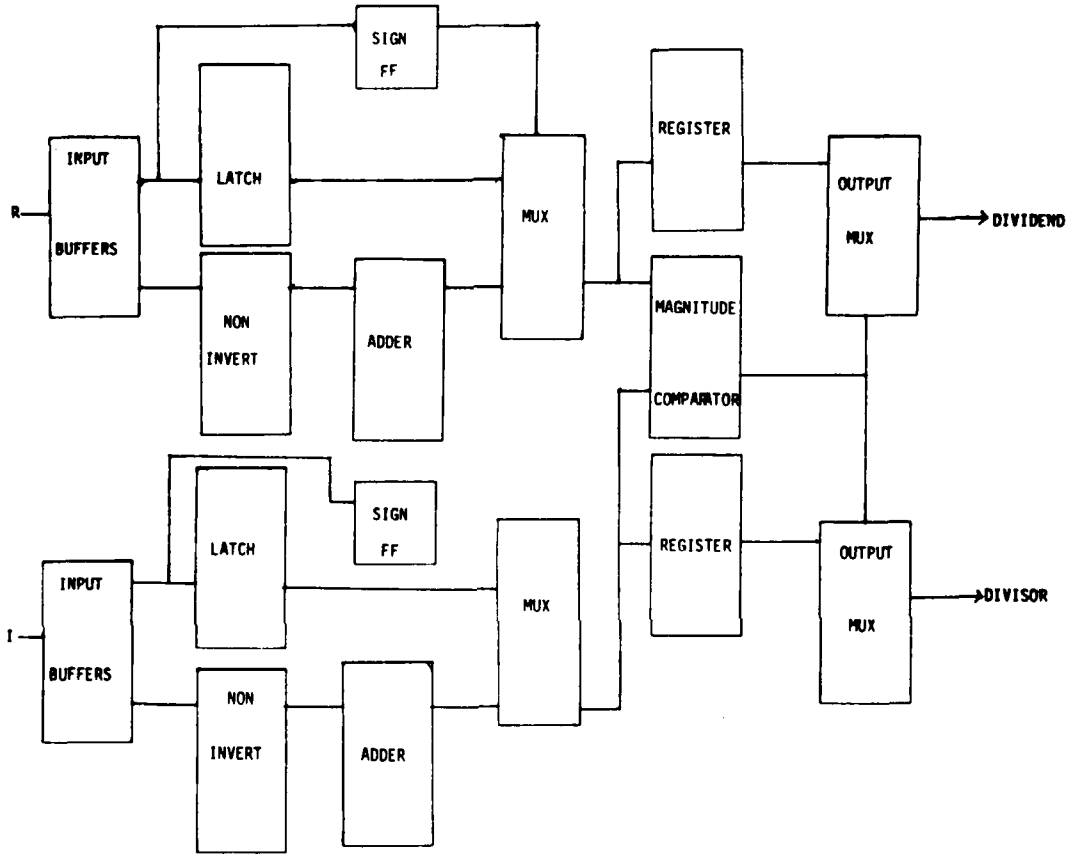



Figure 25. Sign Magnitude Board

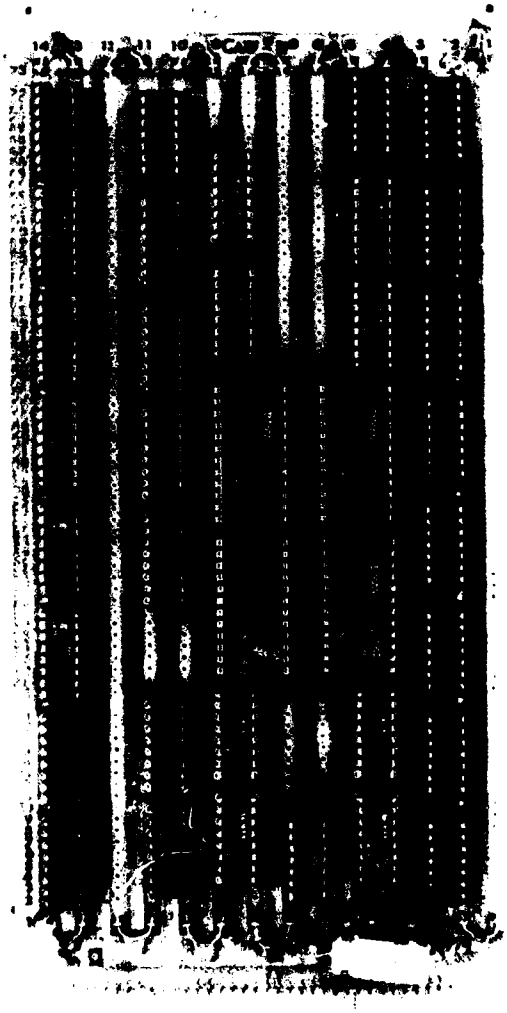


Figure 26. Sign Magnitude Board

by the sign flip flop, which controls the multiplexer, and the data are passed through the MUX to a register if it is Ø. If the MSB is a 1, the value (1 000 0000) is added to the data word before it is passed onto the register.

The digital I and R words stored in the registers are then compared by a pair of cascaded 4-bit magnitude comparator ICs (see Table 2 and Figs. 27 and 28). These ICs perform comparison of straight binary and straight binary code decimal (BCD) (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length are compared by connecting comparators in cascade.

TABLE 2. COMPARATOR LOGIC LEVELS

| COMPARING INPUTS | | | | CASCADING INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A > B | A < B | A = B | A > B | A < B | A = B |
| A3 > B3 | X | X | X | X | X | X | H | L | L |
| A3 < B3 | X | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 > B2 | X | X | X | X | X | H | L | L |
| A3 = B3 | A2 < B2 | X | X | X | X | X | L | H | L |
| A3 = B2 | A2 = B2 | A1 > B1 | X | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 < B1 | X | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 > B0 | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 < B0 | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | L | L | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | H | L | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | L | H | L | L | H |

The A < B, A > B, and A - B outputs of a stage handling less significant bits are connected to the corresponding A < B, A > B, and A = B inputs of the next stage handling more significant bits. The stage handling the least significant bits must have a high level voltage applied to the A = B input.

The comparison is done to insure that the larger number is always sent to the divisor of the divide board, and the smaller number is always sent to the dividend. The results of the comparators are gated to the respective dividend or divisor multiplexers.

f. Memory Buffers. Data transfer rate problems can arise due to the different speed requirements of various portions of the processor. The 8-bit A/D conversions can take place as fast as 33 ns, but the divide function will take more than seven times longer to implement; therefore, memory buffers were designed into the system to hold data in transit between the various boards.

After the magnitude comparison of the data is made, the larger of the 8-bit words is sent to memory buffer A, shown in Figure 29. The wire wrap board for buffer A can be seen in Figure 30. The smaller of the 8-bit words is sent to memory buffer B (Figs. 31 and 32). Both buffers contain eight 2147 static RAM, each arranged as 4KX1 bits. These RAM memory chips are fabricated in the H-metal oxide semiconductor (MOS) technology and feature a 55 ns access time. They have a power down feature in which de-selecting a

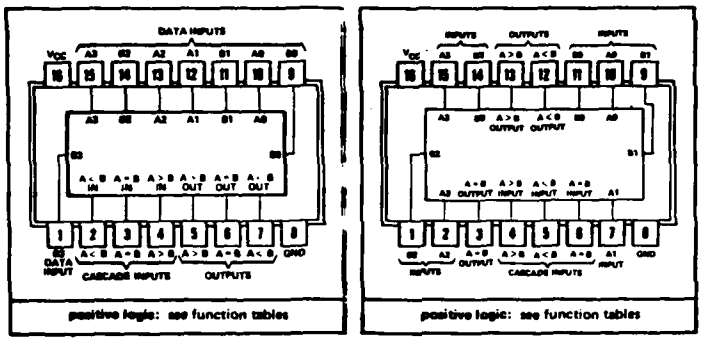



Figure 27. 4-bit Magnitude Comparator and Logic

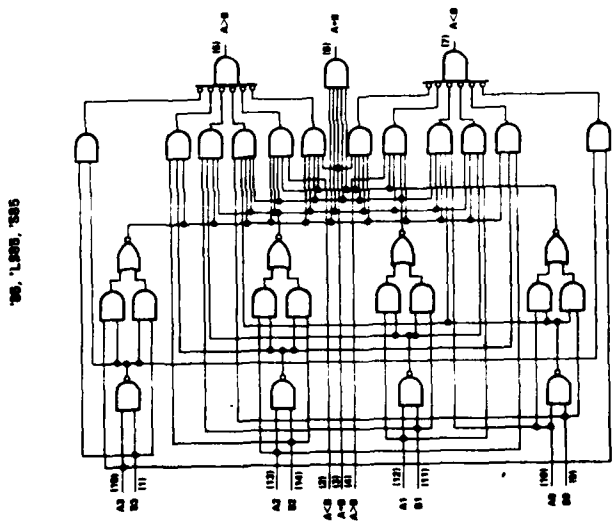


Figure 28. 4-bit Magnitude Comparator Schematic

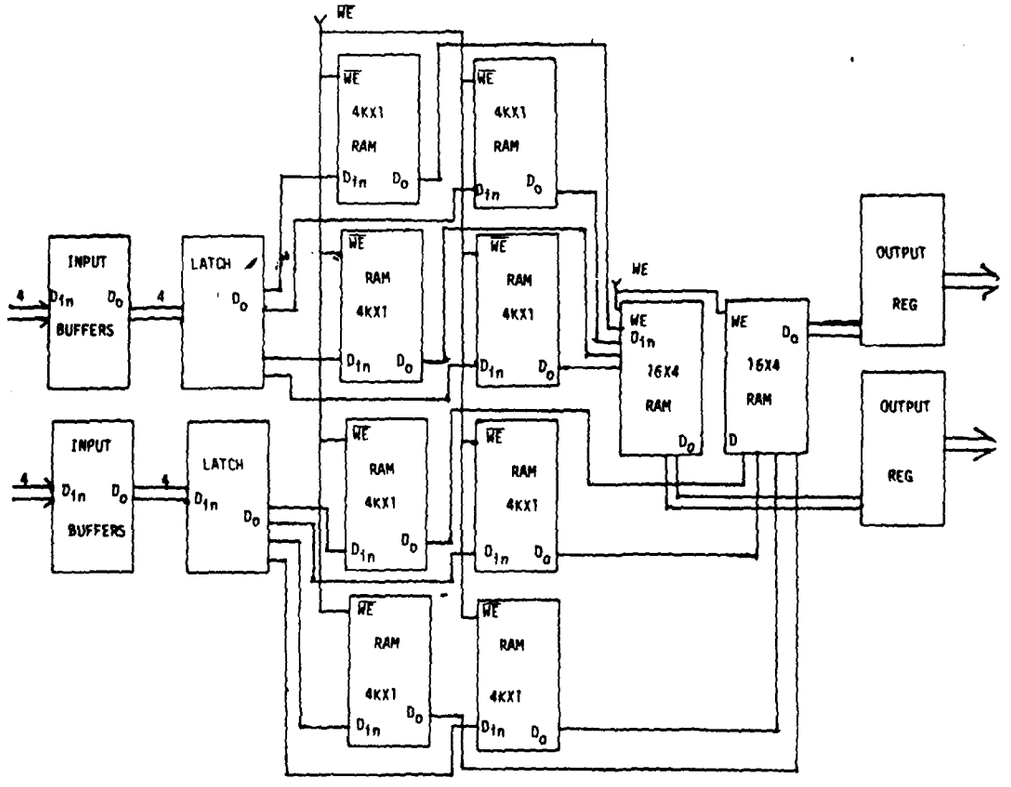



Figure 29. Memory Buffer A Block Diagram

Figure 30. Buffer A Memory Board

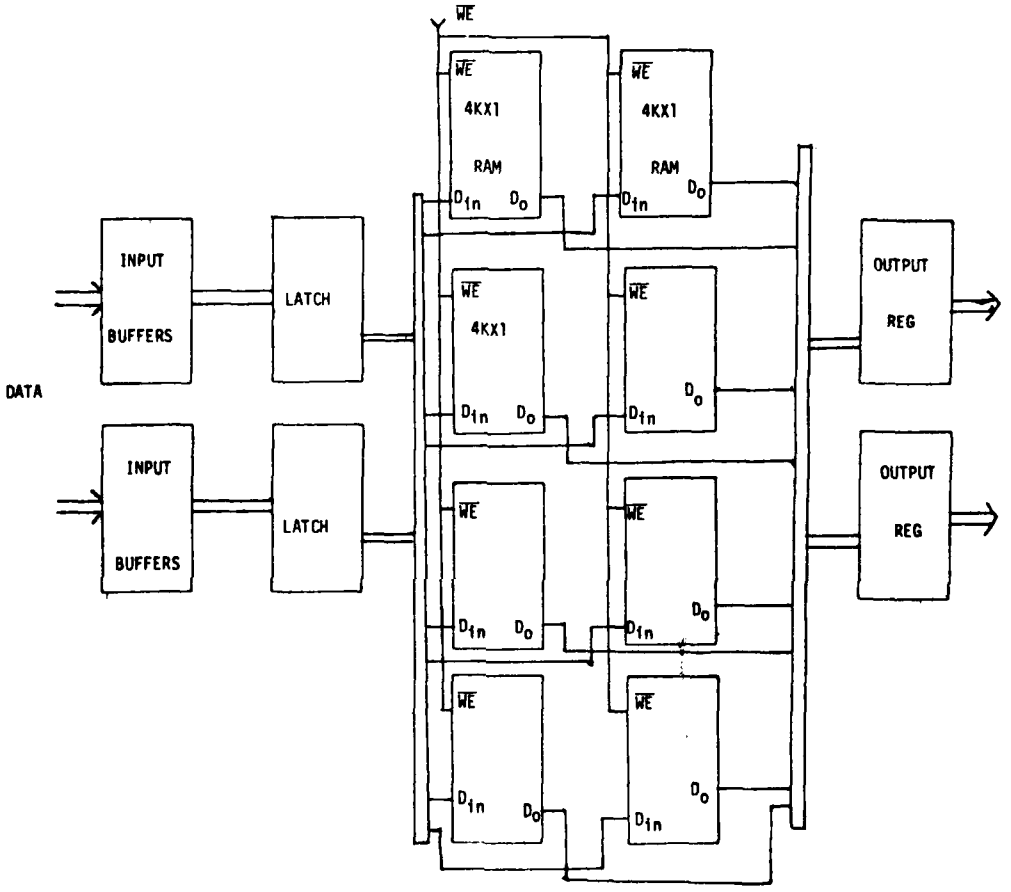



Figure 31. Memory Buffer B Block Diagram

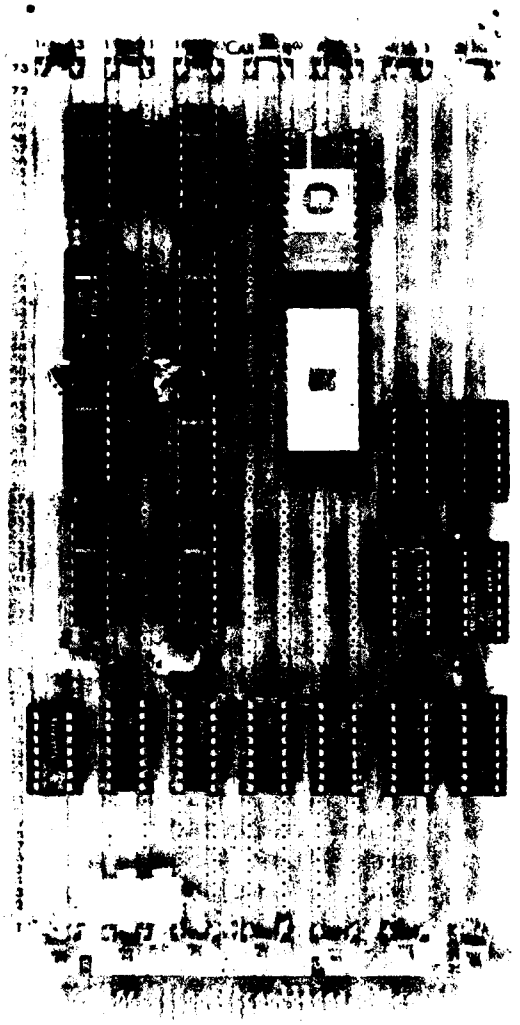


Figure 32. Buffer B Memory Board

particular device reduces its power requirements by 85%. The buffers are organized so that eight RAMs, connected in parallel, form a 4KX8 location map.

The incoming data words are latched by the tri-state D flip flops. These devices are used because of their high current-sinking capability. Each output can drive up to twenty transistor-transistor logic (TTL) device loads. The data are clocked into the buffers at one rate, and read-out at a different rate of speed. The addresses for the memory locations of both buffers are generated on a separate board (Fig. 33). Additionally, the timing and control signals (Fig. 34) of the buffers can also be found on this board. Address generation takes place mainly through the use of 4-bit binary counters (Fig. 35), cascaded to form a 12-bit address word (Fig. 36). The digital I and Q data are then read-out of the buffers and sent to the divide board.

Two's Complement Division

The output of the memory buffers are sent to the divide board (Fig. 37) for two's complement operation. Fixed point hardware division can be accomplished by using the comparison or trial and error method. In this method a trail quotient is formed and the product of the trail quotient and division is tested against the actual dividend and the resulting sign noted. If the sign is positive, the MSB quotient is set to a one, if not, a zero is stored. This procedure is repeated for all bits of the desired quotient, MSB first, LSB last. The output of this divide is available in parallel form.

g. Digital Divider. The digital divider hardware consists of the following: eight AM25S05 Multipliers; one AM2503 Successive Approximation Register (SAR); and four AM9324 Comparators (Fig. 38). The 25S05 is a 2X4 bit multiplier and performs the arithmetic functions $S = XY + K$, which is used as the iterative cell in multiplication and division schemes.[7] In Figure 38, the 25S05 is wired in an 8X8 multiplication array; a parallelogram type structure. When the multiplier array is expanded in the Y direction, it is expanded on a row-by-row basis. The S-outputs of one row are connected to the K-inputs of the following row that are shifted up by two bits in the X direction. (A weight of $2^2 = 4$.) The two least significant output bits ($S_0$ and $S_1$) are not connected and provide two of the array outputs. The AM25S05 can be used to multiply signed or unsigned numbers in various number representations and performs multiplications in either positive or negative logic. The logic diagram of AM25S05 is shown in Figures 39 and 40 and consists of five parts: a multiplier decoder, a shifting array, a complementer, a high speed adder, and an overflow and sign control.

The multiplier decoder generates the required control signals for the shifting array and complementer. First, it decodes whether ØX, 1X, or 2X of the multiplicand is to be added to the coming partial product. Second, the multiplier decoder generates the ADD/SUBTRACT command.

The "zero" times the multiplicand is obtained by AB. The P-input controls the ADD/SUBTRACT sequence so that the multiplier can work in either the positive or negative logic representation. The shifting array generates the 0, 1, or 2 times the multiplicand and applies this to the complementer. "X"

[7] "Schottky and Low Power Schottky Handbook," AMD 2nd Edition 1977, Sunnyvale, California

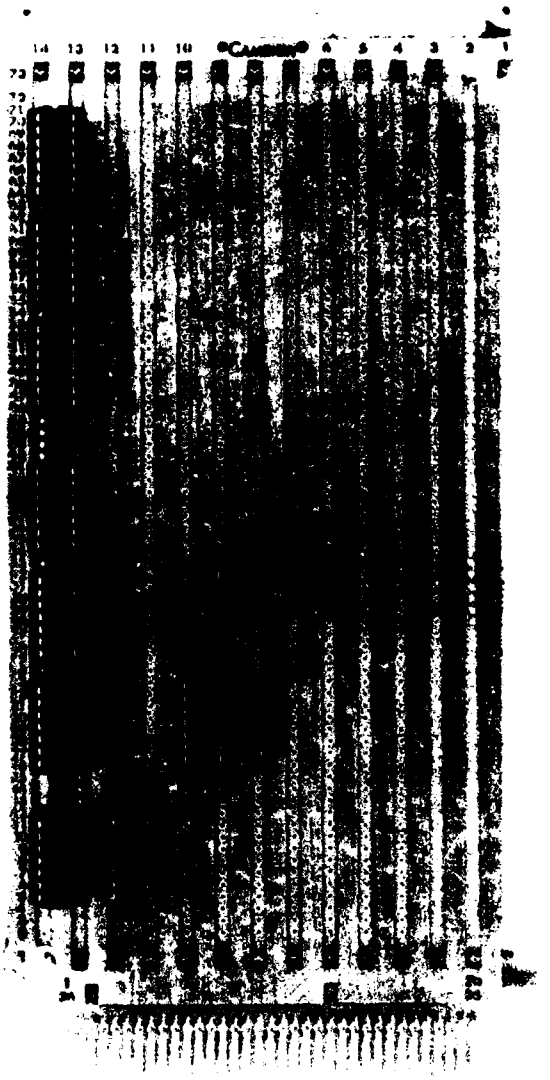


Figure 33. Timing and Address Generation
For Memory Boards

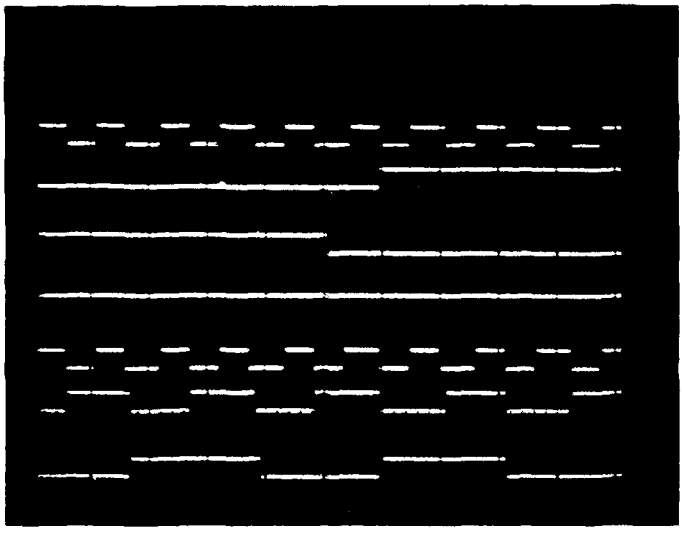



Figure 34. Memory Buffer Timing and Control Signals

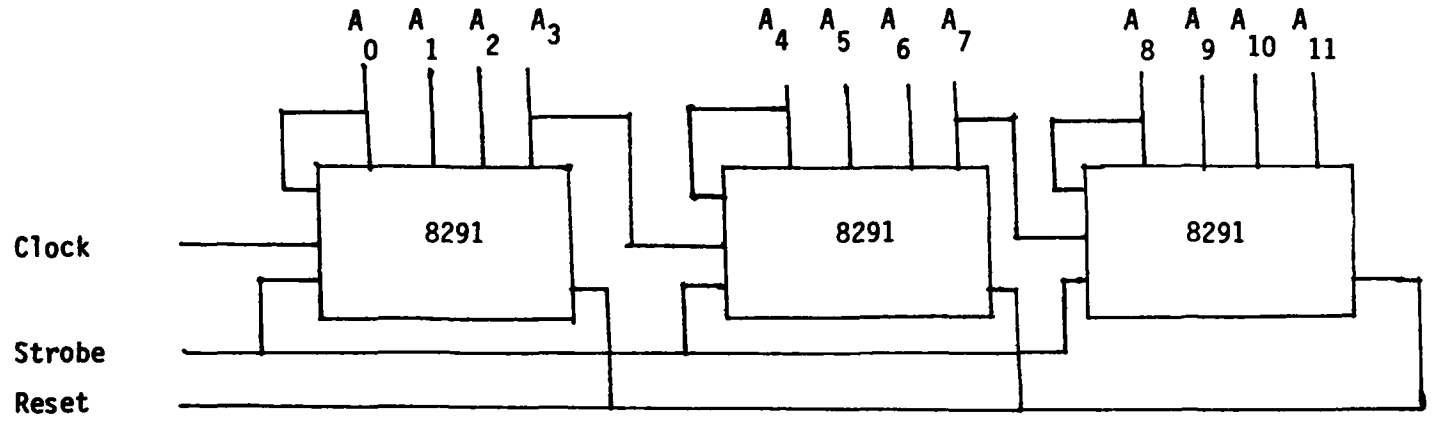



Figure 35. Memory Boards Address Schematic

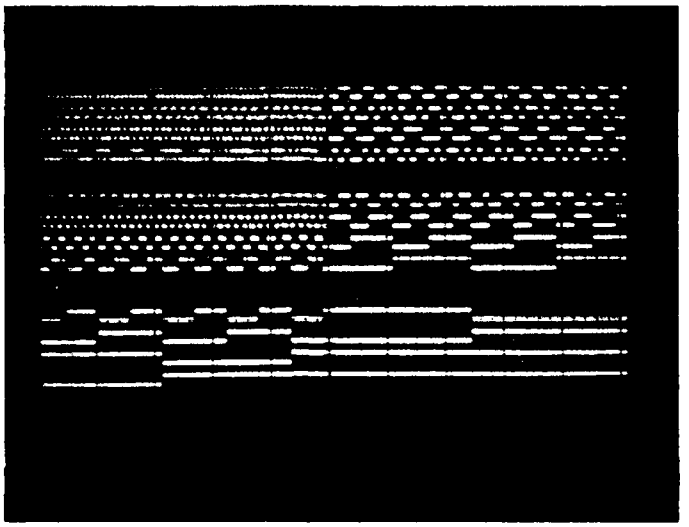



Figure 36. Memory Buffer Address Values

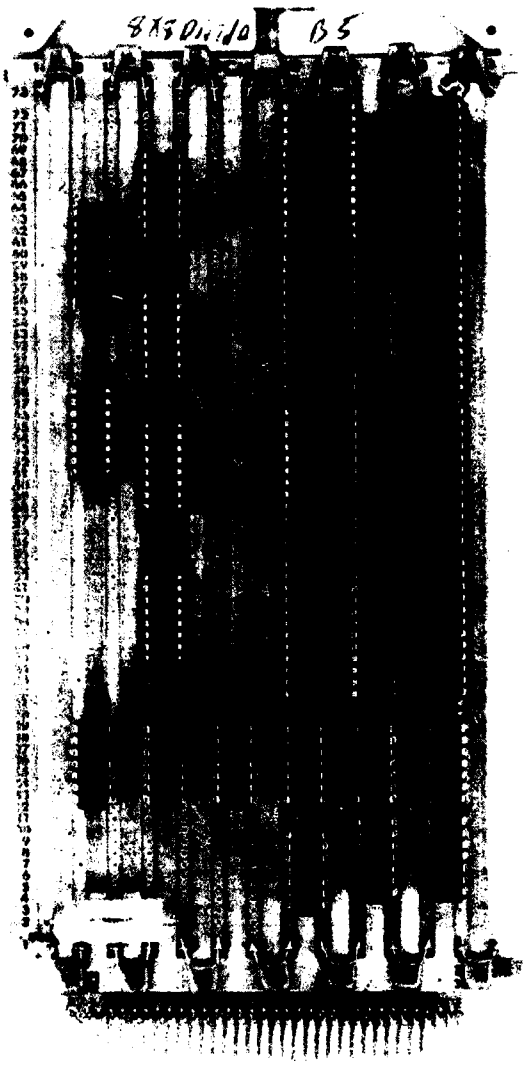


Figure 37. Two's Complement Hardware Divide Board

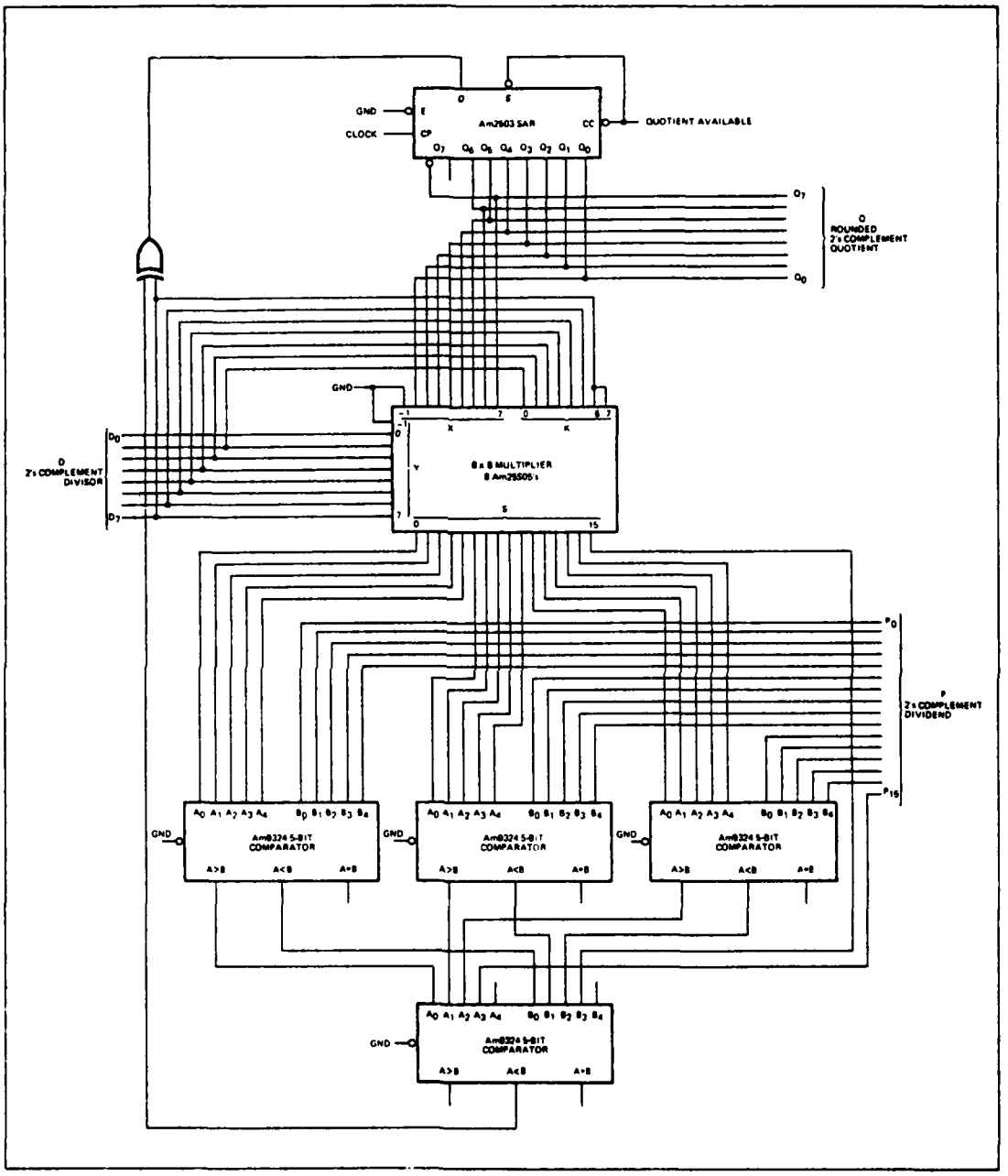



Figure 38. Fixed Point Division Schematic

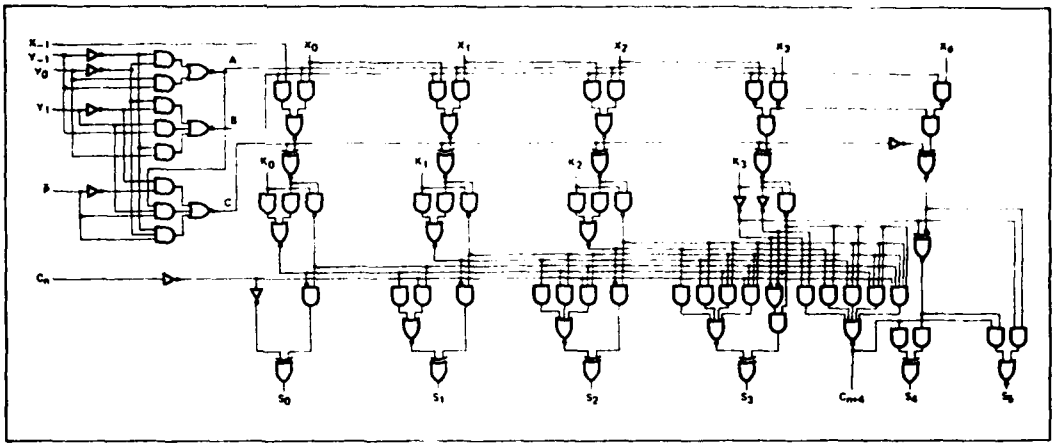


Figure 39. Logic Diagram for the AM25S05

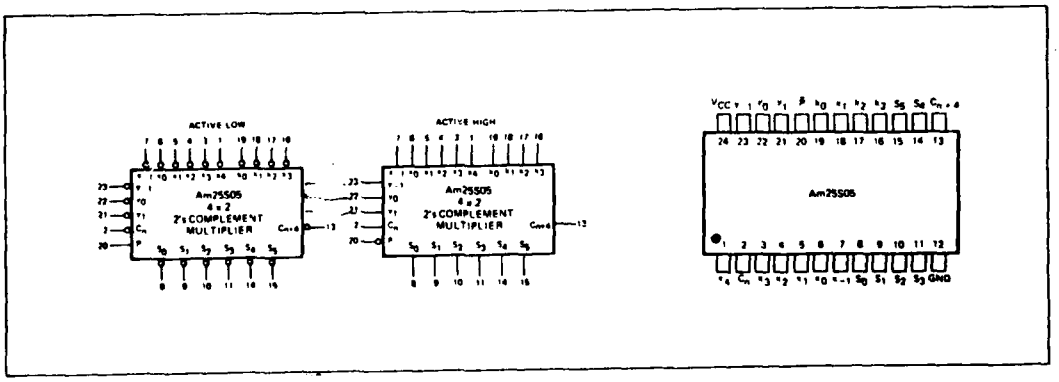



Figure 40. Logic Symbol and Connection Diagram for the AM25S05

is inverted through the shifting array and "0" is implemented as all highs out of the array. The X-1 input is used to shift up the next lower order bit for the 2X function. The complementer consists of a set of exclusive-NOR circuits controlled by the ADD/SUBTRACT function. The ADD command applies a "0" to each exclusive-NOR. The ADD command thereby causes each output of the shifting array to be inverted. Thus the X inputs are applied noninverted to the high speed adder in the ADD mode, and applied inverted in the SUBTRACT mode. The high speed adder is a 9-bit high speed parallel carry look-ahead adder that adds the selected function of the multiplicand $X_1$ to the partial product presented at the K inputs. The adder also has a carry input $C_n$, a carry output $C_n + 4$ and four sum outputs, S0 to S3.

At the most significant end of the array, i.e., where the sign bits are processed, a problem arises when an overflow occurs as a result of an addition or subtraction, or the need to use 2X in the adder. To overcome these overflow situations, the sign digits of the multiplicand and partial product must be repeated twice. Some logic minimize flow is possible and the S4 and S5 outputs, which are the MSB of the 6-bit signed product, can be generated easily. These two outputs are required only at the MSB end of each iterative step of a multiplication. In order to reduce input loading on $X_3$, an additional input is provided which is a part of this overflow circuitry. The $X_4$ input must be connected to $X_3$ at the MSB end of the array only, and can be left unconnected elsewhere.

Simply stated, the division operation can be performed by multiplying the trial value n by the divisor and comparing the result against the dividend. If the dividend is larger, then the trail value has to be increased. If the dividend is smaller, then the trial value has to be reduced. The operation is fairly straightforward for unsigned division. The first trial value is (-1) which is all 1's in two's complement form.

Since the complement of the MSB of the register is used rather than the true output, so that resetting the register presents -1 to the multiplier array, the change in algorithm between the sign bit and the rest of the bits is automatically taken care of. A double length dividend is assumed. The comparator is wired for a two's complement comparison with the sign digit of the product and dividend crossed over; the dividend sign bit forming part of the multiplier word and the product bit forming part of the dividend word.

The results of divisions using this circuitry can be seen in Figure 41. The top traces are the 8-bits of the quotient of the division, and the bottom trace is the conversion complete signal, signifying the end of the conversion. At this point the result of the division is a fractional number which represents $\Delta$ I/$\Delta$ Q, or $\Delta$ Q/$\Delta$ I. The next step is to convert the result of the division to the actual electrical phase angle difference it represents. This is readily done with a look-up table.

h. Phase Angle Look-Up and Display. The quotient from the divide circuit forms an address which is then used to point to a specific value in a table. The table is resident in a programmable read-only memory (PROM), and represents the values of the arc tangent or arc cotangent functions of the electrical phase angle.

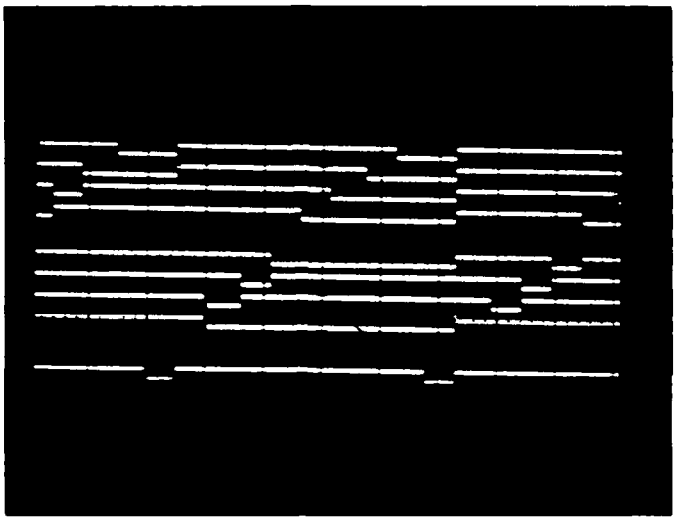



Figure 41. Divide Board Output Signals

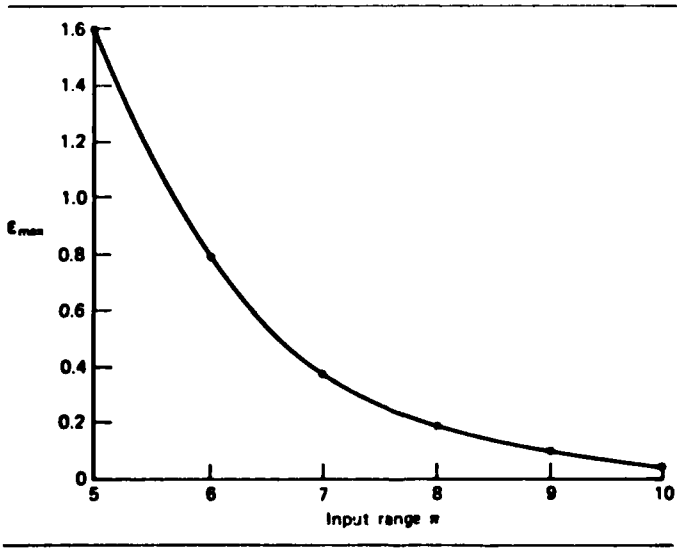



Figure 42. Maximal Error Curve for Rounded Products as a Percentage of the Input-Range n

The availability of inexpensive and widely used PROMs have made the table look-up approach a viable means for producing the product or quotient of any two binary numbers. The multiplication and division table stored in a PROM contains the results of all possible combinations of the input operands. The primary difficulty is the number of bits required in the PROM. For direct multiplication, the combined m-bit multiplicand and n-bit multiplier define a unique address in the memory. The contents of the addressed word, out of the $2^{m+n}$ possible words, form the (m+n) bit product, if no rounding is allowed.

The total bit capacity required in the PROM is

$$N = 2^{m+n} \times (m+n) \tag{23}$$

Even for moderate values of m and n, say m = n = 8, one may need a PROM memory with a capacity of $2^{8+8} \times 16 = 1{,}048{,}576$ bits to store the whole table. Therefore, in many practical applications, the product is rounded to P-bits, for P < m+n with the understanding that a scaling factor has to be imposed to the LSB of the rounded result. The bit capacity needed can thus be reduced to $N_r = 2^{m+n} \times P$. This rounding may introduce an error E which is bounded by

$$-\frac{g}{2} < \varepsilon > \frac{g}{2} \tag{24}$$

where g represents the value of the LSB of the rounded result. The bit capacities needed in a PROM for various values of g, p, and m = n, are enumerated in Table 3. In the case of m = n = p, the least significant n bits are rounded. The maximum error as a percentage of the range of the input quantities is given by

$$\varepsilon \text{ max} = \frac{0.5}{2^{n-1}} \times 100 \tag{25}$$

plot of ε max is given in Figure 42 as a function of the input range n.

The look-up table circuit (Figs. 43 and 44) is composed of High-speed Drivers, AM25LS243; RAM Buffers, 82S112, Octal Latches, AM25LS273; and an 8K Ultraviolet Erasable PROM, 2758. The INTEL PROM features a single 5v power requirement, simple programming, 525 mw power dissipation, and 450 ns access time.

The quotient output of the divider becomes the address of the look-up table. It is first buffered and latched, then gated to the PROM, which contains the angular function data. When the control signals, chip enable and output enable, go low, and the latched address is stable for at least 450 ns, then a valid table look-up operation can take place.

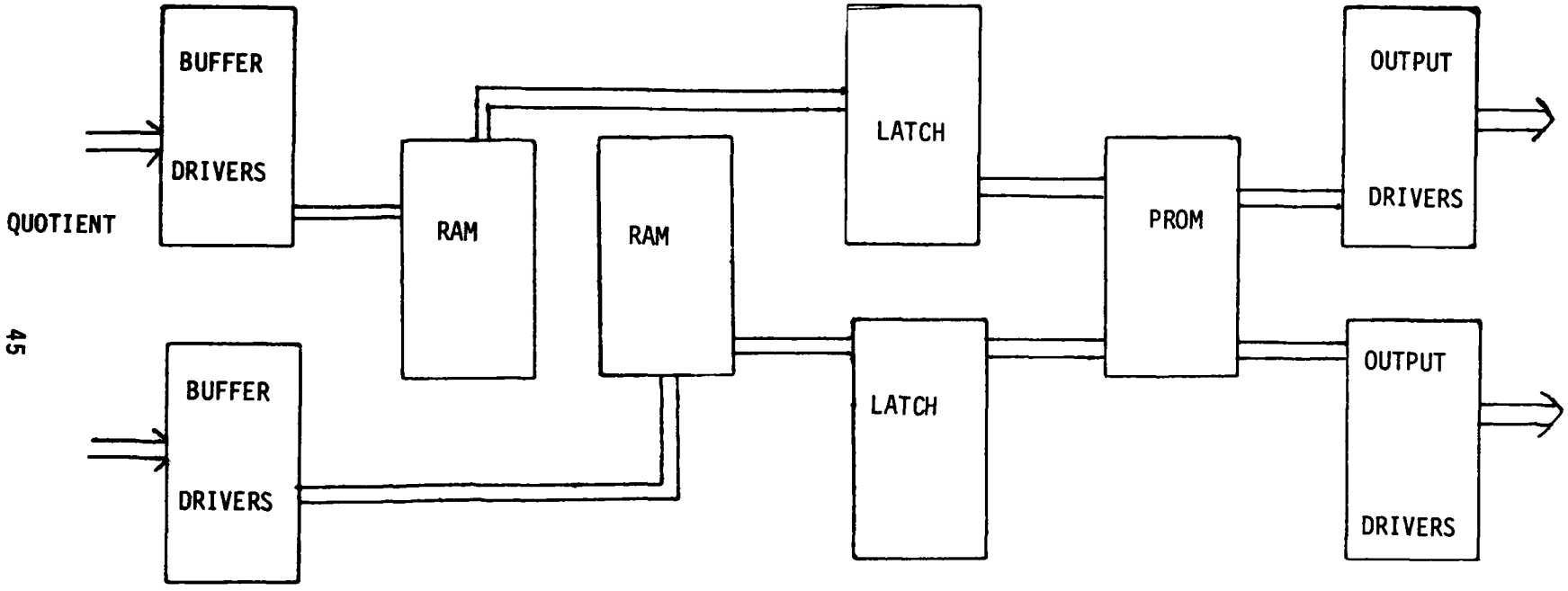



Figure 43. Phase Angle Look-Up

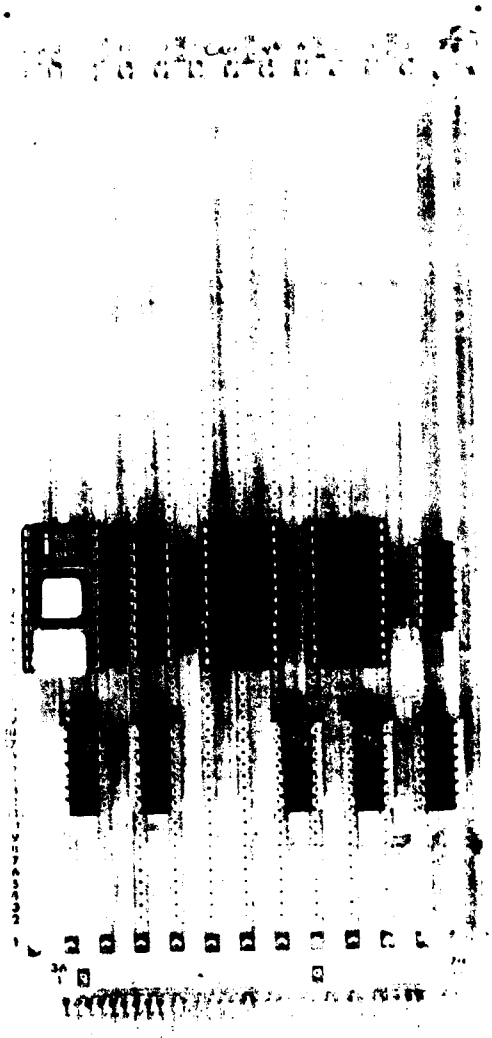


Figure 44. Angle Look-Up Board

TABLE 3. WORD LENGTH VERSUS BIT-CAPACITY FOR DIRECT MULTIPLICATION USING ROMs

| Input Range $m = n$ | Word Length $p$ | Value of the l.s.b. in the Rounded Product $q$ | The Reduced Bit Capacity $N_r = 2^{2n} \times p$ |
|---|---|---|---|
| 4 | 8 | 0 | 2,048 |
| 4 | 4 | $2^4$ | 1,024 |
| 8 | 16 | 0 | 1,048,576 |
| 8 | 14 | $2^2$ | 917,504 |
| 8 | 12 | $2^4$ | 786,432 |
| 8 | 8 | $2^8$ | 524,288 |
| 10 | 20 | 0 | 20,971,520 |
| 10 | 16 | $2^4$ | 16,777,216 |
| 10 | 10 | $2^{10}$ | 10,485,759 |

The table contains the arc tangent and the arc cotangent function information in binary form. Each table contains 128 distinct entries; the values for the tangent function can be found in Appendix A. The range of the electrical phase angle is limited to 0 - 45 degress for the tangent function, and 45 - 90 degrees for the cotangent. This forced limitation is extended to the baseline configuration to insure that the functions will remain in this range. This is done to keep the look-up table down to a reasonable number of entries.

Display

The output of the table look-up circuitry consists of an 8-bit binary data word which represents the electrical phase angle difference between channels. The angle at this point was viewed in order to verify correct operation of the processor. Two alphanumeric dot matrix displays were used to indicate the two-digit electrical phase angle, which had a range of 0 - 90 degrees.

The circuit which accomplishes this can be seen in Figures 45 and 46. The heart of the display board is a binary to BCD converter which translates the single 8-bit binary word into two 4-bit digits with values from 0 - 9. The converter circuit shown in Figure 47, contains a binary counter and a decimal counter which count the same number of clock pulses.

The 8-bit data word is buffered and latched into a register and presented to the input side of the 74LS193 Binary Counter at the start of conversion pulse. The conversion pulse also clears the decade counters (74LS-192). When the binary number is preset, the borrow line at the binary counter's output goes high, enabling the AND gate (7408) to send clock pulses to both chains. As the binary counter counts down from the preset number, the BCD counter counts up from zero. When a count equal to the incoming binary number is accumulated, the borrow line to the AND gate goes high, inhibiting further counting. The BCD counter now contains the BCD equivalent of the original binary number, which is strobed into two alphanumeric dot matirx displays.

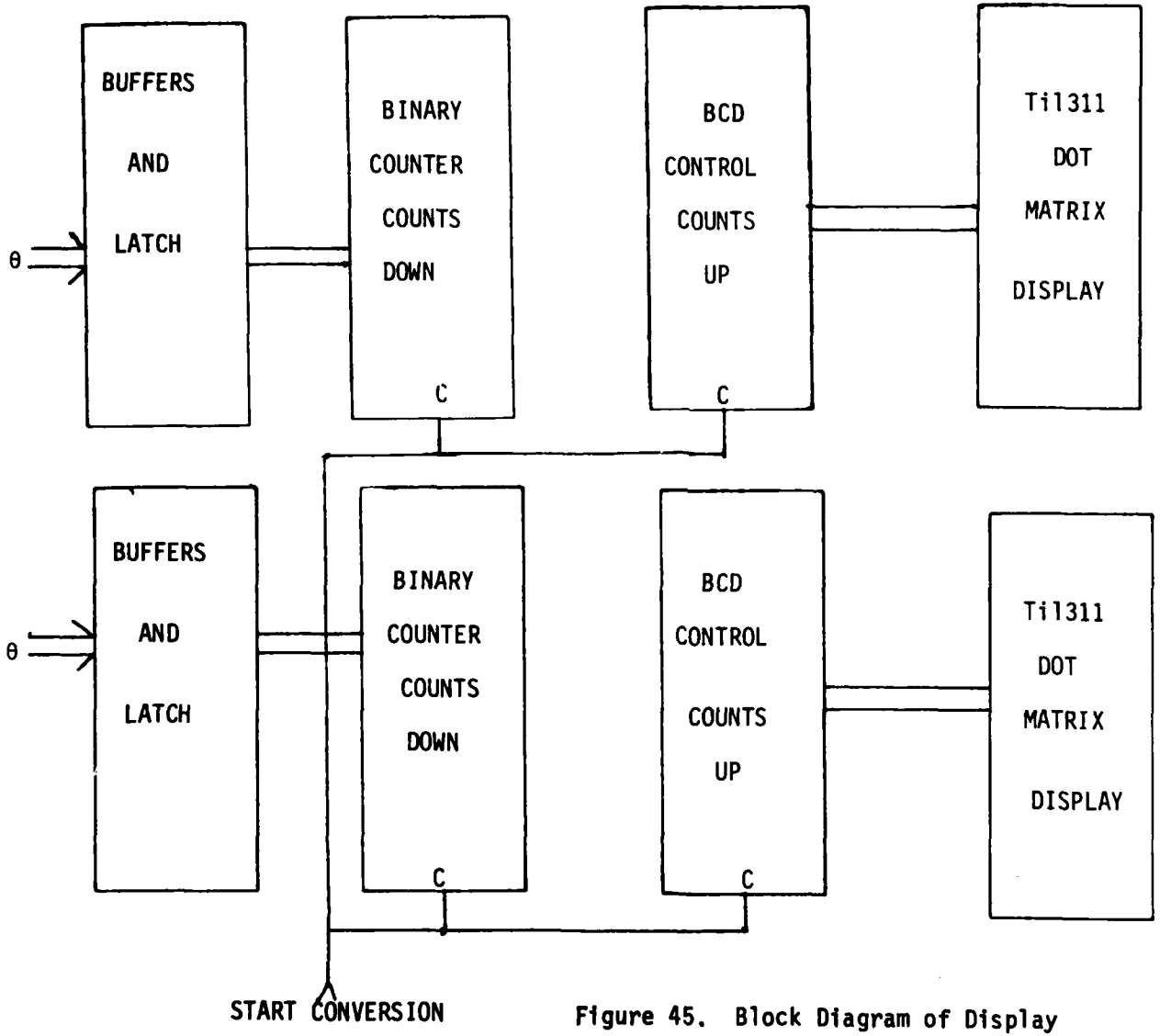



Figure 45. Block Diagram of Display

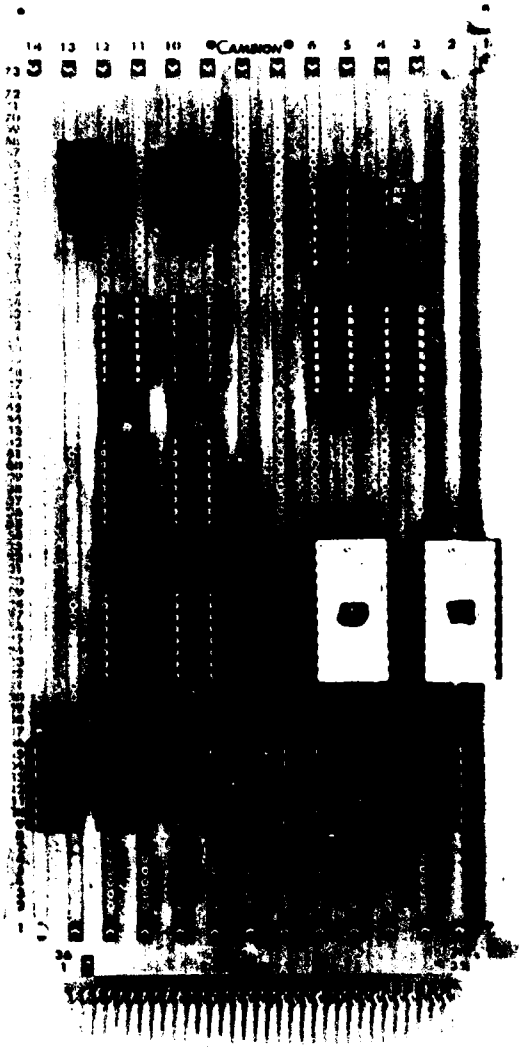


Figure 46. Display Board

Test Circuit

In order to check out the timing and control functions of the processor, and to trace signal levels between PC boards, a test circuit for trouble-shooting was designed (Fig. 48). Direct current (dc) voltages were applied to the inputs of both A/D converters to simulate an incoming pulse at a specific time, $t_1$. In this way, the converters are constantly sampling the same signal and; therefore, the same electrical phase difference will occur, resulting in a constant phase angle being calculated and displayed.

One benefit of this testing configuration is that timing pulses and data transfer between boards can be easily checked. Also, the input/output (I/O) states for the combinational and sequential logic functions on each board can be verified. A logic analyzer was used in conjunction with an oscilliscope as the primary debugging tool for the processor (Fig. 49).

CONCLUSIONS/RECOMMENDATIONS

The use of digital techniques in the measurement of electrical phase angle data results in significant speed and computational improvements in electronic warfare collection systems.

The processor described in this report illustrates a major portion of the digital circuitry needed to implement real-time monopulse AOA measurement. A real-world phase interferometer system has a number of baseline corrections built into it to account for errors across the frequency bands of operation. The antenna spacing is designed in such a way that all the ambiguities can be resolved in the processor. Total calibration of the system is needed throughout the frequency band, and it is a function of the RF front-end components and the final baseline configuration.

The next phase of the program will be to determine the azimuthal AOA from the electrical phase angles measured by this portion of the processor. The AOA can only be obtained after the baseline corrections are made, the ambiguities are resolved, and the entire phase interferometer is calibrated across the frequency band.

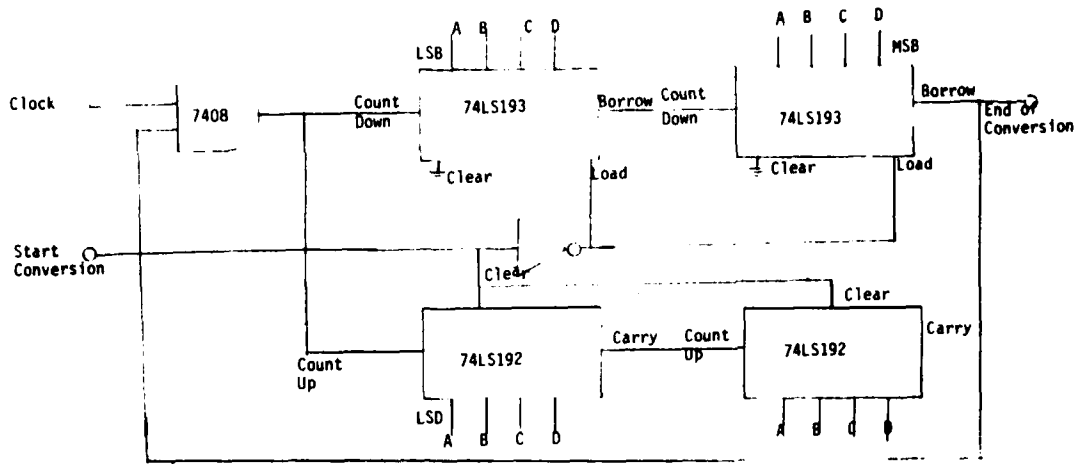



Figure 47. Binary to BCD Converter Schematic

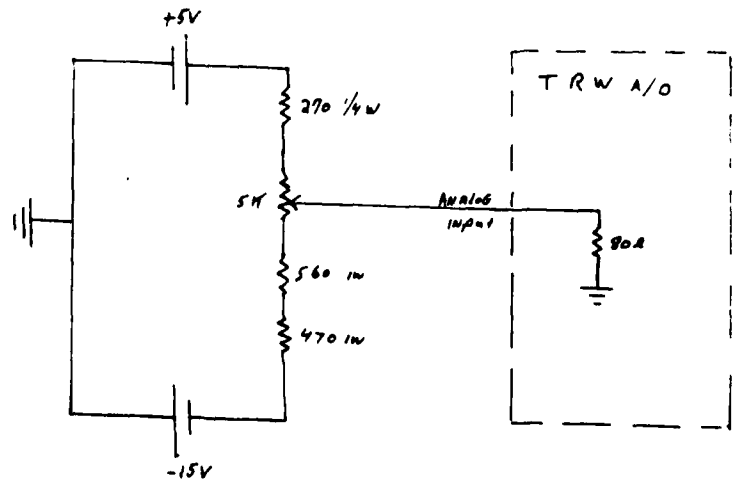



Figure 48. Test Circuit

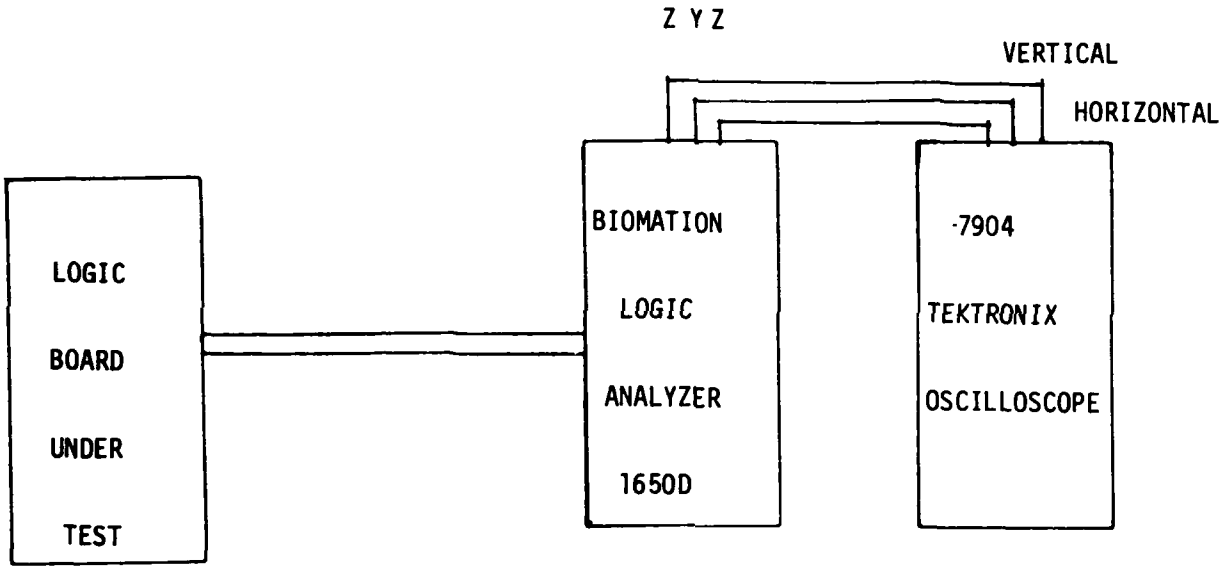



Figure 49. Trouble Shooting Test Set Up

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# APPENDIX A

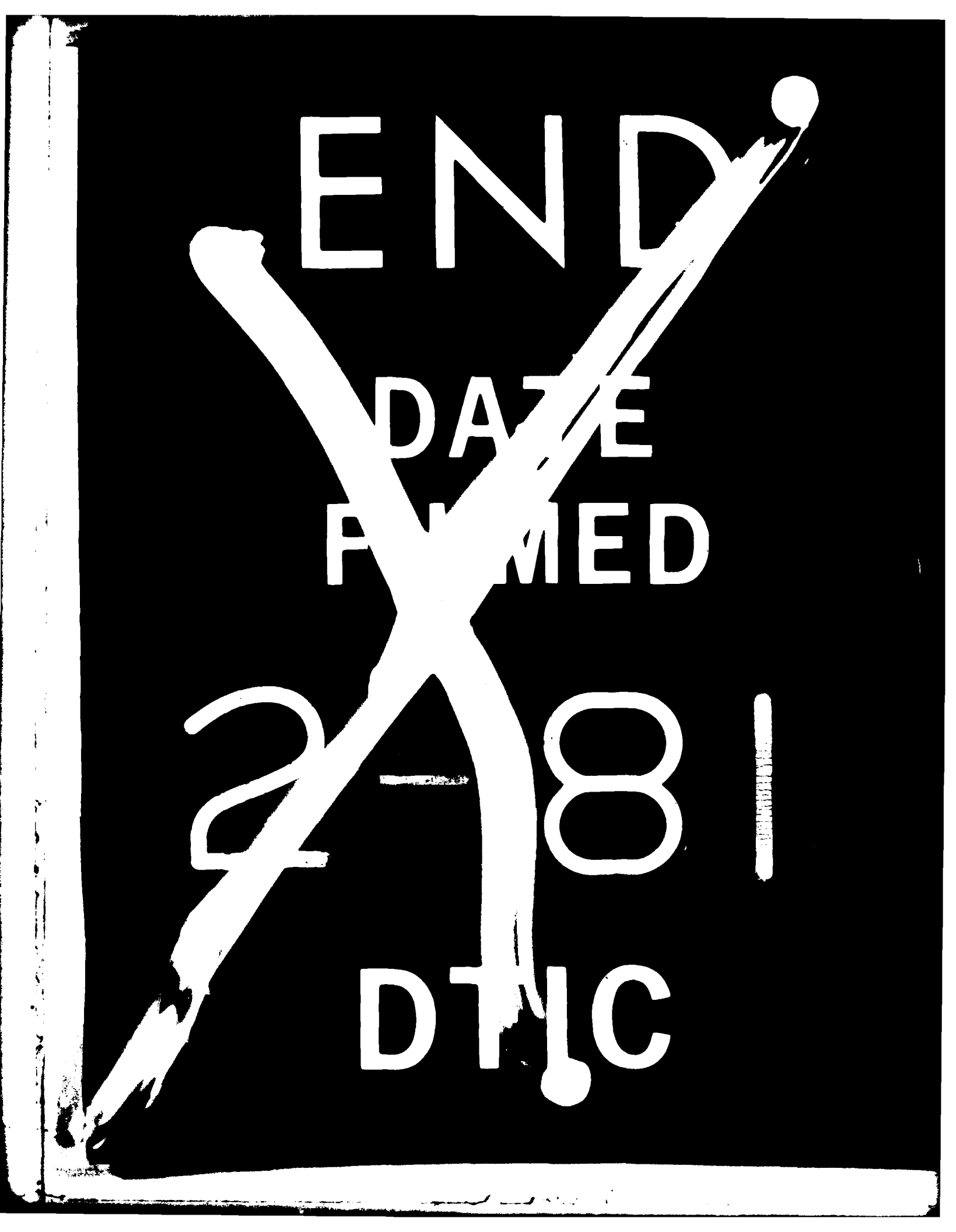
## PROM LOOK-UP TABLE

| RAM LOCATION | LOCATION DATA (HEX) | PHASE ANGLE (DEGREES) |
|---|---|---|
| 0 | 00 | 0 |
| 1 | 00 | 0 |
| 2 | 01 | 1 |
| 3 | 01 | 1 |
| 4 | 02 | 2 |
| 5 | 02 | 2 |
| 6 | 03 | 3 |
| 7 | 03 | 3 |
| 8 | 04 | 4 |
| 9 | 04 | 4 |
| 10 | 04 | 4 |
| 11 | 05 | 5 |
| 12 | 05 | 5 |
| 13 | 06 | 6 |
| 14 | 06 | 6 |
| 15 | 07 | 7 |
| 16 | 07 | 7 |
| 17 | 08 | 8 |
| 18 | 08 | 8 |
| 19 | 08 | 8 |
| 20 | 09 | 9 |
| 21 | 09 | 9 |
| 22 | 0A | 10 |
| 23 | 0A | 10 |
| 24 | 0B | 11 |
| 25 | 0B | 11 |
| 26 | 0B | 11 |
| 27 | 0C | 12 |
| 28 | 0C | 12 |
| 29 | 0D | 13 |
| 30 | 0D | 13 |
| 31 | 0E | 14 |
| 32 | 0E | 14 |
| 33 | 0E | 14 |
| 34 | 0F | 15 |
| 35 | 0F | 15 |
| 36 | 10 | 16 |
| 37 | 10 | 16 |
| 38 | 11 | 17 |
| 39 | 11 | 17 |
| 40 | 11 | 17 |

APPENDIX A (CONTD)

| RAM LOCATION | LOCATION DATA (HEX) | PHASE ANGLE (DEGREES) |
|---|---|---|
| 41 | 12 | 18 |
| 42 | 12 | 18 |
| 43 | 13 | 19 |
| 44 | 13 | 19 |
| 45 | 13 | 19 |
| 46 | 14 | 20 |
| 47 | 14 | 20 |
| 48 | 15 | 21 |
| 49 | 15 | 21 |
| 50 | 15 | 21 |
| 51 | 16 | 22 |
| 52 | 16 | 22 |
| 53 | 16 | 22 |
| 54 | 17 | 23 |
| 55 | 17 | 23 |
| 56 | 18 | 24 |
| 57 | 18 | 24 |
| 58 | 18 | 24 |
| 59 | 19 | 25 |
| 60 | 19 | 25 |
| 61 | 19 | 25 |
| 62 | 1A | 26 |
| 63 | 1A | 26 |
| 64 | 1B | 27 |
| 65 | 1B | 27 |
| 66 | 1B | 27 |
| 67 | 1C | 28 |
| 68 | 1C | 28 |
| 69 | 1C | 28 |
| 70 | 1D | 29 |
| 71 | 1D | 29 |
| 72 | 1D | 29 |
| 73 | 1E | 30 |
| 74 | 1E | 30 |
| 75 | 1E | 30 |
| 76 | 1F | 31 |
| 77 | 1F | 31 |
| 78 | 1F | 31 |
| 79 | 20 | 32 |
| 80 | 20 | 32 |
| 81 | 20 | 32 |
| 82 | 21 | 33 |
| 83 | 21 | 33 |

| RAM LOCATION | LOCATION DATA (HEX) | PHASE ANGLE (DEGREES) |
|---|---|---|
| 84 | 21 | 33 |
| 85 | 22 | 34 |
| 86 | 22 | 34 |
| 87 | 22 | 34 |
| 88 | 23 | 35 |
| 89 | 23 | 35 |
| 90 | 23 | 35 |
| 91 | 23 | 35 |
| 92 | 24 | 36 |
| 93 | 24 | 36 |
| 94 | 24 | 36 |
| 95 | 25 | 37 |
| 96 | 25 | 37 |
| 97 | 25 | 37 |
| 98 | 26 | 38 |
| 99 | 26 | 38 |
| 100 | 26 | 38 |
| 101 | 27 | 39 |
| 102 | 27 | 39 |
| 103 | 27 | 39 |
| 104 | 27 | 39 |
| 105 | 28 | 40 |
| 106 | 28 | 40 |
| 107 | 28 | 40 |
| 108 | 28 | 40 |
| 109 | 29 | 41 |
| 110 | 29 | 41 |
| 111 | 29 | 41 |
| 112 | 29 | 41 |
| 113 | 2A | 42 |
| 114 | 2A | 42 |
| 115 | 2A | 42 |
| 116 | 2A | 42 |
| 117 | 2B | 43 |
| 118 | 2B | 43 |
| 119 | 2B | 43 |
| 120 | 2B | 43 |
| 121 | 2C | 44 |
| 122 | 2C | 44 |
| 123 | 2C | 44 |
| 124 | 2C | 44 |
| 125 | 2D | 45 |
| 126 | 2D | 45 |
| 127 | 2D | 45 |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# SUPPLEMENTARY

# INFORMATION

AD-A093 808

ERRATA SHEET FOR

REPORT DELEW-TR-80-4
DIGITAL PHASE MEASUREMENT TECHNIQUES
DECEMBER 1980

The following corrections should be made:

Page 3:

$$\phi = \frac{2\pi d}{\lambda} \sin\theta \qquad (1)$$

$$\Delta\phi = \frac{2\pi d}{\lambda} \cos\theta\,\Delta\theta \qquad (2)$$

$$\phi_1 = \frac{2\pi d_1}{\lambda} \sin\theta \qquad (5)$$

$$\phi_2 - \phi_1 = \frac{2\pi(d_2 - d_1)}{\lambda} \sin\theta \qquad (7)$$

Page 5:

$$V_0\ (DC) = K_1 \text{ cosine } (\phi_I - \phi_R) \qquad (10)$$

Page 8:

$$I = K\,AB\cos\phi \qquad (15)$$

Page 8, 2nd paragraph, last line:

A and B ($\phi = \alpha - \beta$)

Page 42, 1st paragraph, last line:

$C_{n+4}$

Page 44:

$$-\frac{g}{2} < \varepsilon < \frac{g}{2} \qquad (24)$$