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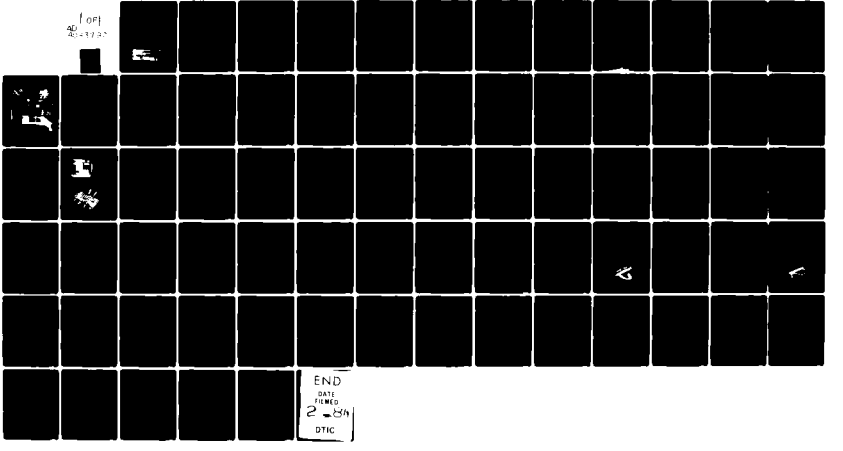

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HUGHES AIRCRAFT COMPANY
GROUND SYSTEMS GROUP

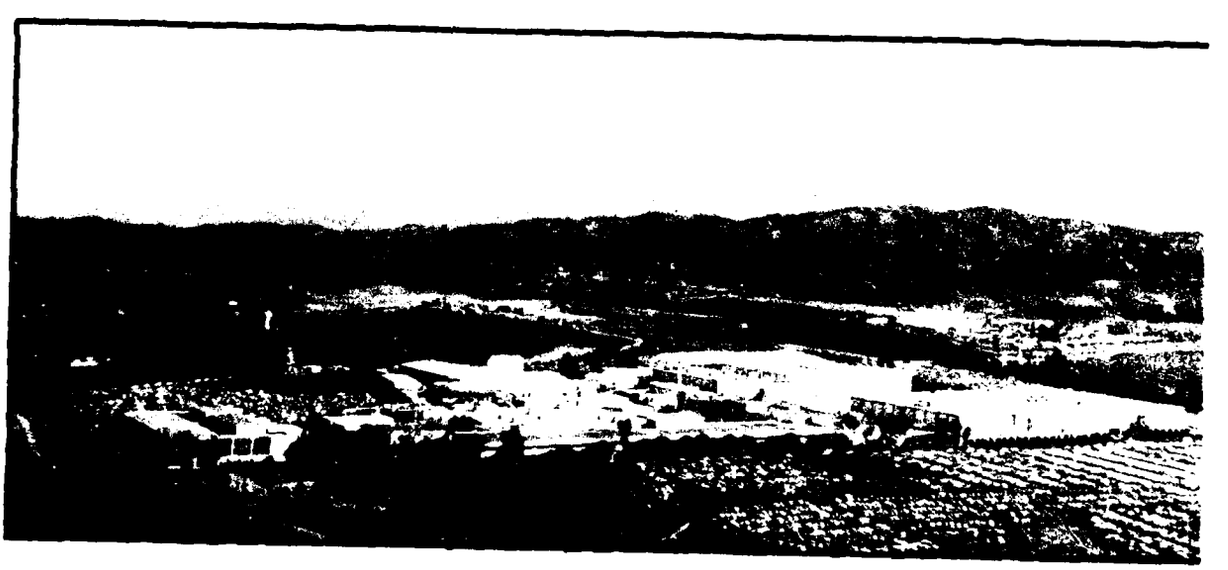
Final Report

LEVEL II (2)

Manufacturing Methods And Technology For Digital Fault Isolation Of Printed Circuit Boards

Project No. R783242

15 NOVEMBER 1980
CONTRACT NO. DAAK 40-78-C-0290



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20 Abstract

This report presents the final recommendations and conclusions, with supporting data, resulting from the contract option phase of contract DAAK 40-78-C-0290. It describes the manufacturing technology and test system that will enable detection, identification, and location of digital faults in the advanced missile electronic systems that will be used in the 1980's. Emphasis is placed on the fault diagnosis of large printed circuit boards containing complex hybrid digital microelectronic circuits.

The Basic Effort included an industry survey for digital printed circuit board test requirements and available test system capabilities, the D/PCB testability investigation and resulting design guide, the development of digital fault isolation methodology and the comprehensive selection of the optimum ATE that recommended the DTS-70 system.

The contract option phase of this project involved the purchase and installation of the DTS-70 system, the selection of the PN-1635972 and the PN-1646178 D/PCBs for testing, the development of generalized test software and the development of the specific hardware and software needed to test these worst-case boards. It also included a successful demonstration of the project's results for interested Department of Defense and industry personnel.

The Hughes-enhanced, state-of-the-art, DTS-70 automatic test system installed at Redstone Arsenal as a result of this contract provides the capability to isolate digital faults in such circuit boards to the component level with a test comprehensiveness of 90% or better.

The report concludes with recommendation for the improvement of the DTS-70 System to increase its utility, with recommendations for improving the testability of digital printed circuit boards, and with recommendation for future digital fault isolation studies.

FINAL REPORT

Manufacturing Methods and Technology for Digital Fault Isolation of Printed Circuit Boards

Project No. R783242

Prepared for

U.S. Army Missile Command

Redstone Arsenal, Alabama 35809

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Contract No. DAAK 40-78-C-0290
CDRL A004

Prepared by

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Report Date: 15 November 1980
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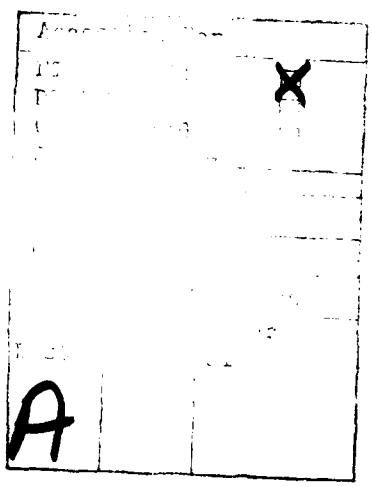

FOREWORD

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The contract option phase of this project involved the purchase and installation of the DTS-70 system, the selection of the PN-1635972 and the PN-1646178 D/PCBs for testing, the development of generalized test software and the development of the specific hardware and software needed to test these worst-case boards. It also included a successful demonstration of the project's results for interested Department of Defense and industry personnel.

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CONTENTS

SECTION 1
DFI PROGRAM OVERVIEW

1. PROGRAM OBJECTIVES OF THE BASIC STUDY AND HARDWARE OPTION TASKS

In progressive efforts of a Basic Study and Hardware Option, the DFI program accomplished the MICOM MM&T objectives to select a commercial ATE system providing cost-effective production test and fault isolation for complex digital PCBs during the 1980's.

Objectives – Efficient automatic test and fault isolation of digital PCBs for production and field installations, is presently a vital requirement of the military and of industry. To meet current D/PCB test requirements, MICOM initiated the DFI program with the following objectives:

- To select an optimum commercial automatic test equipment (ATE) system to test advanced D/PCBs during the 1980's.
- To establish manufacturing methods and technology (MM&T) for production test of D/PCBs having
  - mixed or multifamily logic
  - hybrid microelectronics
  - LSIs or microprocessors
- To test and fault isolate to an IC pin or component.
- To procure and implement the selected ATE system with test enhancements.
- To demonstrate the ATE system's D/PCB testing and install it at MICOM.

The results of the Basic Study, which selected the Hewlett-Packard DTS-70 ATE system, appear in the Interim Report,[1] Project No. -R783242 (Hughes FR 79-12-669A), dated 25 August, 1979.

Basic Study – The six major tasks performed in the Basic Study were initially structured into milestones for an approved task plan (CDRL A008) and were identified as:

- D/PCB Survey
- FI Test System Survey
- Performance Evaluation
- Testability Investigation
- DFI Methodology
- Test System (ATE) Selection

The baseline equipment for the study rapidly evolved into a set of 21 D/PCBs (derived from 6 prime military systems), and 7 primary test system candidates.

A simplified three stage process used to select the optimum ATE system for DFI, is shown in Figure A. The initial tester evaluation resulted from a combination of the computer-aided and manual data reduction of 186 data items for each D/PCB and of 275 data items for each tester. Tester evaluation in the second stage combined the initial result with the relative D/PCB test program cost and a derived cost-performance figure from the supplier quoted system. The final evaluation combined the initial and secondary results with a practical system performance test, provided by a 5 IC test circuit, that measured system simulator software and fault diagnostic capability.

As a result of this comprehensive evaluation, and the DTS-70 ATE system's high score, the Basic Study selected the DTS-70 ATE system for production test application.

1. The Interim Report is available for distribution from: Defense Documentation Center, Cameron Station, Alexandria, Va. 22314

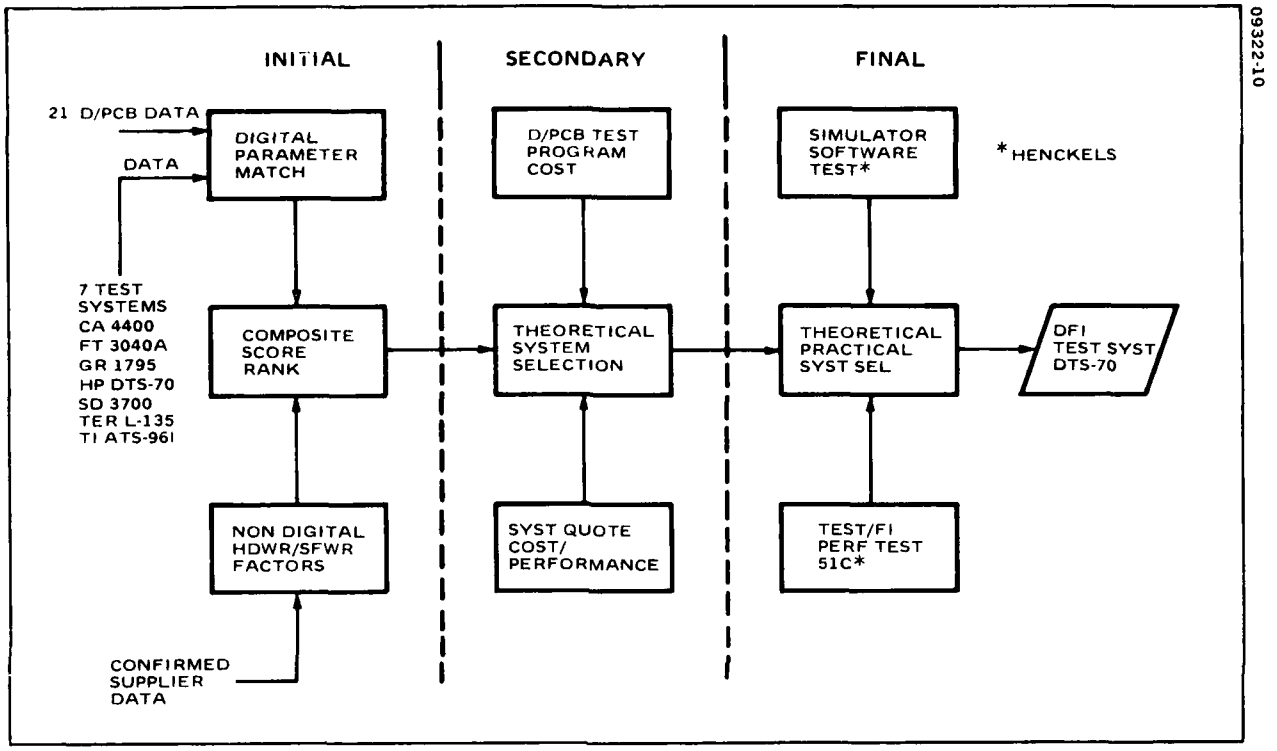


Figure A. Test System Selection Process. The six milestones for the approved task plan (CDRL A008) evolved into the three stage system selection process illustrated here.

1. PROGRAM OBJECTIVES OF THE BASIC STUDY AND HARDWARE OPTION TASKS (Continued)

Hardware Option – The Hardware Option, or ATE implementation, consisting of major tasks and resultant outputs to MICOM, was also included in the milestone task plan of CDRL A008. Major tasks and program outputs shown in Figure B include:

- Hardware Procurement
- D/PCB Test Candidate
- ATE Integration
- Software Development
- Performance Analysis
- Industry Demonstration
- Final Report
- Implementation Plan
- Support Facilities
- Improved Software
- ATE Installation

Hardware Procurement was initiated early in October, 1979, for all necessary ATE hardware, software and operator training. System hardware included test enhancement equipment.

Following the first quarterly program review in December, 1979, two complex microprocessor D/PCBs, selected from the PCB survey and available from Hughes' production, were approved as test candidates.

Software Development concentrated effort on creating the test program for each D/PCB candidate. Concurrently, the Performance Analysis task progressively improved the D/PCB test software towards the 95 percent test comprehensiveness level (ability to detect all possible faults).

The DTS-70 ATE system was fully integrated and operating early in April, 1980, and had logged over 2500 hours by August, 1980, with less than 2.5 hours required for maintenance service.

In early September, 1980, a total of 45 persons attended the Industry Demonstration (CDRL A005) at Hughes. Interested representatives of various military, government, industry, and Hughes organizations witnessed the ATE test and fault isolate the two microprocessor D/PCBs.

As a separate part of this Final Report (CDRL A004), the DTS-70 Implementation Plan (CDRL A006) was submitted during the latter part of July, 1980. This plan outlined ATE system acquisition costs, facilities, production test applications, and D/PCB through-put test costs relative to a baseline comparison system.

Improved Software outputs included 5 elements of the system executive and test software, and the two D/PCB candidate's application test software. These are contained on the system's fixed and movable discs.

Support Facilities cost data for the maintenance of the ATE system hardware and software are supplied by a support maintenance application program report operating through the IMAGE/1000 software.

To conclude the DFI program, installation of the DTS-70 ATE system for MICOM at Redstone Arsenal was successfully completed by Hughes during the latter part of September, 1980.

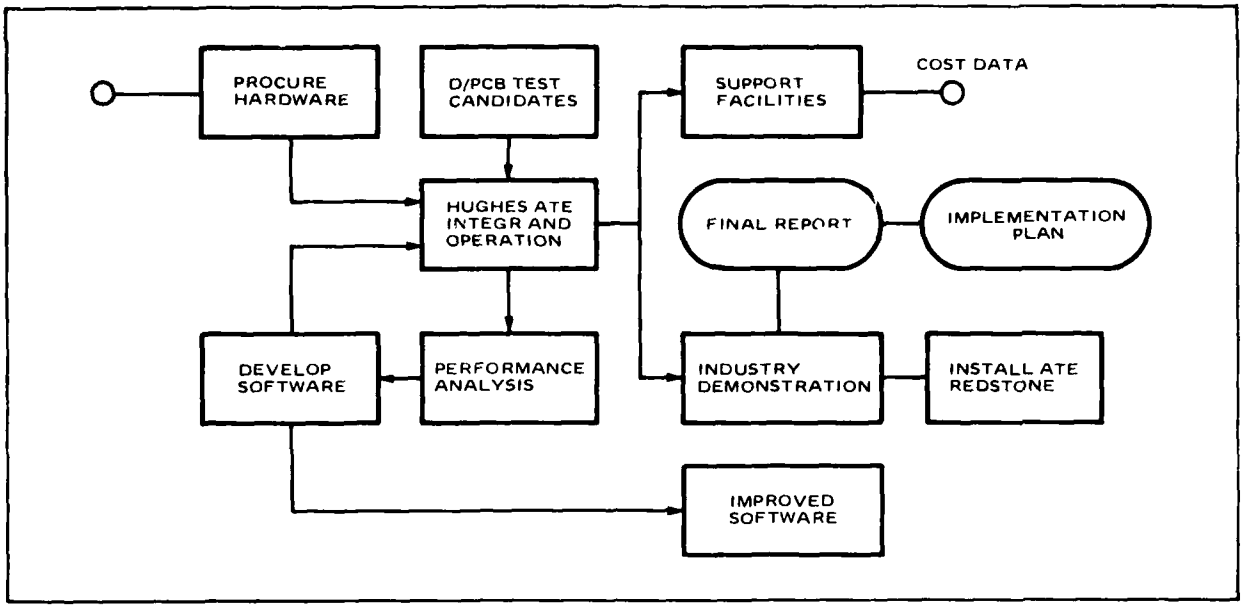


Figure B. ATE Implementation Task Development and Outputs to MICOM. Once the DTS-70 ATE System had been selected, eleven months were required to procure system hardware, develop and refine its software, and install the test system at Redstone Arsenal.

2. DTS-70 SYSTEM CONFIGURATION AND CIRCUIT BOARD TEST CANDIDATES

In addition to multiple-station capability, the DFI-configured DTS-70 features hardware and software test enhancements, including Signature Analysis. It can effectively test two complex microprocessor D/PCB test candidates – the first containing a 8080 A/B, and the second an AM 2901 device.

Hardware – The results of the D/PCB Survey test requirements and the stated program objectives were used to establish the implemented ATE system requirements prior to its procurement.

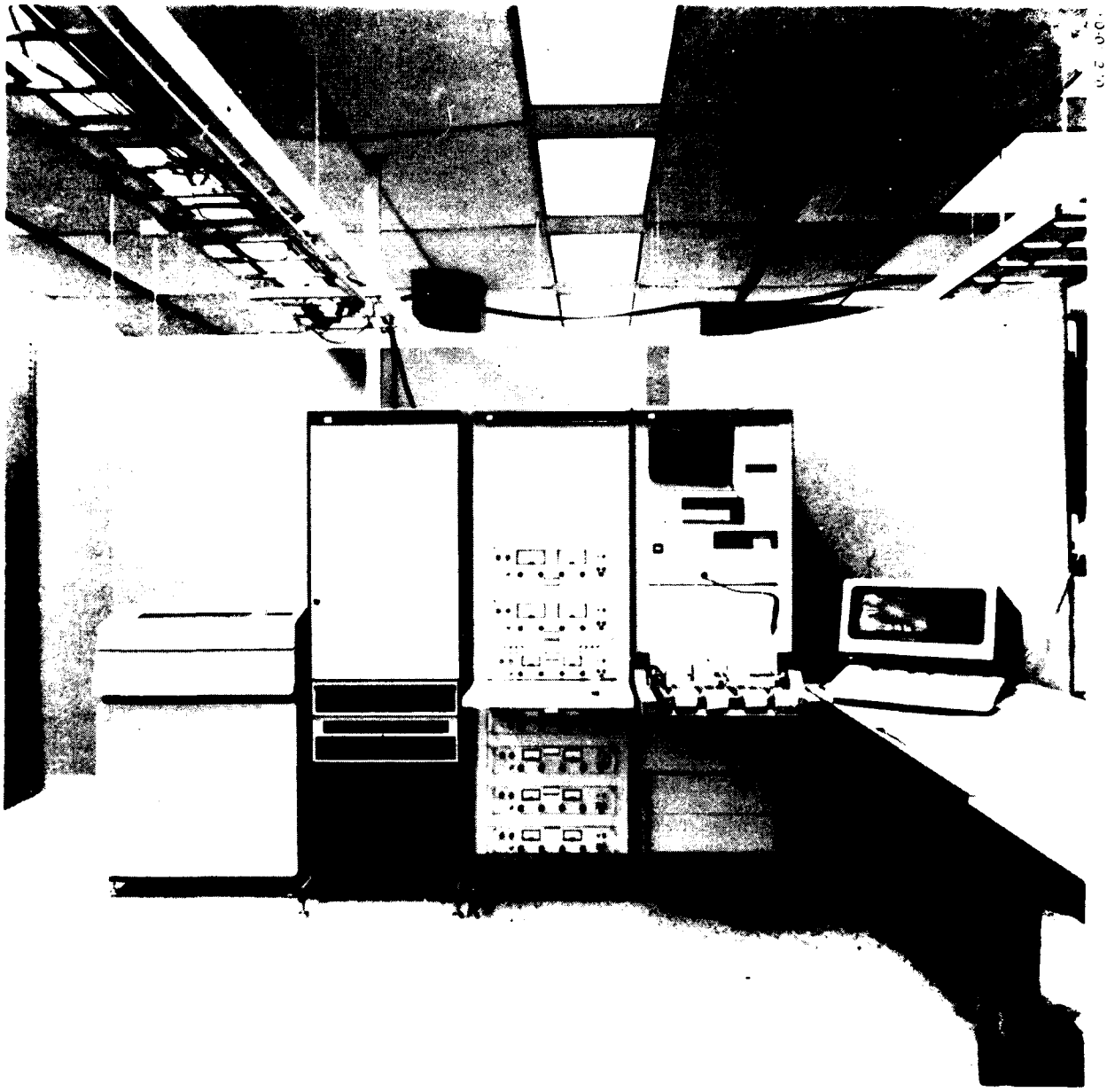
As implemented for the DFI program, a standard DTS-70 system was supplemented with test equipment features enabling it to test and fault isolate, to the component level, D/PCBs having mixed logic, LSI, and microprocessor devices. The facing figure illustrates the resulting DTS-70 system configuration. Its major equipment groups are:

- 400 LPM Printer (2608 A/210)
- HP 1000/40 Computer and 20 M Byte Disc Drive (7906/020)
- UUT Bus Programmable Power Supplies, (7)
- Digital Test Unit with
  - 270 I/O Test Pins
  - Computer Guided Probe
  - Programmable Driver/Comparators
  - Repair Ticket Printer
- Keyboard/CRT Terminal

The modular ATE system design permits economical expansion as needed for production. To increase D/PCB test through-put, programming capacity, and production management reports, one HP 1000/40 computer can operate three test stations with operator terminals and three additional terminals on a time sharing basis.

The equipment selected to enhance D/PCB automatic testing and to extend fault diagnostic capability from the circuit node level to the component level includes:

- Signature Analyzer (SA) – bus controlled through Hughes-originated FORTRAN software for LSI and microprocessor tests.
- HP-IB-(IEE-488) – bus control the data transfer of the SA unit or of 14 additional bus controlled instruments.
- HP Digital Probes/Gen Rad Fault Probe – to isolate a node fault to the component level.
- Seven UUT Power Supplies – bus programmable for wide voltage and current range PCB requirements.



DTS-70 System Configuration for the DFI Program. The modular design of the DTS-70 system permits additional growth without requiring extensive modification of the existing system.

2. DTS-70 SYSTEM CONFIGURATION AND CIRCUIT BOARD TEST CANDIDATES (Continued)

To quantitatively measure ATE system performance for D/PCB test and fault isolation, data were recorded for specific D/PCB test objectives as indicated:

- Functional Test – to 95% comprehension
- Simulated D/PCB Faults
  - SA0, SA1, Solder Bridge (SB)
  - 2 Simultaneous (introduced) faults
- Fault Isolation – to the pin level of a hybrid module or LSI device

Two complex microprocessor D/PCB test candidates, surveyed in the Basic Study, were selected and mutually approved by Hughes and the MICOM project officer. The test candidates are part of respective military systems currently in production. They include:

- Army AN/TPQ-36 Radar
  Part number – 1635972 Microprocessor (8080 A/B)
- HMD-22, Air Defense Ground Environment (ADGE) Radar Display
  Part number – 1646178, 16 Bit Microprocessor (AM 2901)

Both D/PCBs contain ROM, RAM, LSI, microprocessor, and a large variety of digital ICs.

Although the -972 PCB contains 28 ICs, its testing complexity resides in its Intel 8080 A/B microprocessor and multiport 8 Bit bidirectional LSI devices. Signature Analysis and FORTRAN software are used in combination with conventional digital techniques to test this D/PCB candidate.

At the other extreme, the -178 PCB contains 142 ICs including four AM 2901 microprocessors. Its test complexity originates with bidirectional bus circuits and large variety of digital functions. Testing of the -178 PCB uses AM 2901 functional models in combination with conventional digital techniques described later.

To apply Signature Analysis and LSI modeling, the two D/PCB candidates required advanced test software techniques. Furthermore, their combined complexity stressed the test capability of the DTS-70 system.

Software – Five elements of system executive software combined with Hughes-originated FORTRAN test or application software achieve effective D/PCB testing, data base management (DBM) of production records and reports, ATE system maintenance reports, and system diagnostic or performance self-testing. The system software element features, and their use or application are summarized in the following table and discussed in more detail later in this report.

Test Candidates – A paramount objective of the industry demonstration, identified by CDRL A005, was to effectively demonstrate a D/PCB test with Signature Analysis as well as to provide fault isolation performance data for the DFI configured DTS-70 system.

DTS-70 EXECUTIVE AND DFI APPLICATION SOFTWARE

Software Type	Identifier	System Disc Residency Fixed (F) Movable (M)	Principal Language	Interface Language	End Use
System					
Real Time Executive	RTE IVB 92067 A/031	(F) LU 2,3	HP 1000 Assembly	FORTRAN	Controls all system operations
TESTAID/FASTRACE III	91075 B, IVB	(F) LU 2,3	HP 1000 Assembly	NONE	PCB test simulation and fault isolation
IMAGE 1000/(IVB)	92063 A/020	(F) LU 2,3	HP 1000 Assembly	FORTRAN	Data Base Management
Functional/Test		(F) LU 2,3	HP 1000 Assembly	NONE	System Functional Test
Application					
Signature Analysis	SACMPR	(M) LU 18	FORTRAN	-	- 972 PCB Test, 8080 A/B
μProcessor Initialization	INIT/NOOP	(M) LU 18	FORTRAN	NONE	- 972 PCB Test, 8080 A/B
Line Deleter - Make Undetectable	LNDEL/ MKUND (SPEDUP)	(M) LU 18	FORTRAN	NONE	Produces TEST-AID simulator source file to remove previously detected faults
Fault Isolation - 972 PCB	FIF 972	(M) LU 18	HP 1000 Assembly	NONE	- 972 PCB Test Post Processor Files
Fault Isolation - 178 PCB	RHFAIN RHFFLG RHFABO RHFBIN	(M) LU 15 (M) LU 15 (M) LU 15 (M) LU 20	HP 1000 Assembly HP 1000 Assembly HP 1000 Assembly HP 1000 Assembly	NONE	- 178 PCB Test Post Processor
Support Facilities	DFISML, SMRPT	(F) LU 19	HP-Image, Query	FORTRAN	DFI System Support Maintenance Log and Report

3. SUMMARY OF PROGRAM RESULTS

As determined by hardware and software performance with the D/PCB test candidates, by a successful Industry Demonstration, and by the development of a system supportive Implementation Plan, the MICOM program objectives were realized by the implemented DTS-70 system.

System test and fault isolation performance data applicable to this Final Report (CDRL-A004) and to the Industry Demonstration (CDRL-A005) were recorded for the two D/PCB test candidates. Results of the GO/NO-GO test and fault isolation for SA0, SA1, and SB simulated PCB faults were established with test software verified through respective production PCBs. Table I summarizes the D/PCB candidate test results.

In the -972 PCB Signature Analysis testing, manual probing of the 40 pins on the 8080 A/B microprocessor accounts for 8 minutes of total test time shown. By using a 40 pin multiplexer in the test adapter, total test time may be reduced to the order of 1 to 2 minutes.

Industry Demonstration – The DTS-70 Industry Demonstration (CDRL-A005) was scheduled on 8, 9, 10 September 1980 and over 100 guests were invited from MICOM, military, government, and industry organizations. A total of 45 guests observed the test and fault isolation of the -972 and -178 D/PCBs in three separate conferences.

There were requests for copies of the Interim (CDRL-A003) and Final (CDRL-A004) reports, and questions were asked by several guests covering such items as:

- Basic Study – System selection, computer and manual technique
- ATE Implementation -972, -178 test software
  - Signature Analysis, FORTRAN software
  - LSI device logic modeling
  - D/PCB test programming time
  - Logic probe fault isolation
  - D/PCB multiple fault isolation
  - Production D/PCB test throughput and cost

Guest comments indicated that the demonstration was successfully carried out.

Implementation Plan – As a separate part of the final report the DTS-70 production test Implementation Plan (CDRL-A006) was submitted during the latter part of July 1980. The Implementation Plan identified DTS-70 implementation items with specific results, where applicable, as:

- ATE Implementation – 72 square feet; less than 5 days
  – 8.4 KVA power; 120v, 60 Hz
- Acquisition Cost – $K for DFI configuration
- Test Applications – 218 PCB types in 5 Hughes military production systems; 10 OEM contractors external to Hughes
- Test Programming Time – 2.4 HR/IC, predominantly MSI
  – 3.7 HR/IC, AM 2901, LSI
  – 1:2, Signature Analysis vs. LSI functional model
- Test Throughput – $/PCB, 1 to 3 test stations

Improved Software – Salient characteristics of the test software used during the development and Industry Demonstration for the -972, and -178 D/PCB test candidates, are summarized in Table II.

TABLE I. DTS-70 TEST AND FAULT ISOLATION PERFORMANCE FOR MICROPROCESSOR D/PCBS

D/PCB Test Candidates	Number of ICA	GO/NO-GO Test Minutes	Fault Isolation Mean Time-Minutes		
			SA0	SA1	SB
1635972 (8080 A/B)	28	8.3*	1.2	1.7	1.1
1646178 (AM2901)	142	1.5	5.9	2.0	3.2

*Uses manual probing of 40 pins on the 8080 A/B.

TABLE II. DTS-70 D/PCB CANDIDATE TEST SOFTWARE CHARACTERISTICS

D/PCB Test Candidate	Software	Application or Subdivisions	Pattern Generation	Total Number of Patterns	Test Comprehensiveness, %
1635972 (8080 A/B)	SACMPR*	8080 A/B	Manual	175	98
	TESTAID/ FASTRACE	IC Level Substitutes for 8080 A/B	Manual		
1646178 (AM2901)	TESTAID/ FASTRACE	4	Manual	2586	90

*Signature Analysis and FORTRAN – Test compares 8080 A/B UUT pin signatures to known good signatures stored in a disc file.

3. SUMMARY OF PROGRAM RESULTS (Continued)

Testing of the -972 PCB is achieved by test software comprised of two major parts. First TESTAID/FASTRACE is used to test the entire PCB with the 8080 A/B removed from its socket and replaced by a 40 pin umbilical test line supplied with digital test patterns through the DTS-70. Second the 8080 A/B microprocessor is placed in its socket and is allowed to free run through an adapter ROM. SACMPR, a Hughes originated FORTRAN program using Signature Analysis then compares 8080 A/B UUT pin signatures with known good signatures stored in a file.

In either part of the test, the test terminates on a failed step, and either FASTRACE or the SACMPR directs the operator probe to the faulty node.

The 175 test patterns used were manually generated and provide an overall test comprehensiveness of 98 percent. The automatic test pattern generation feature in the DTS-70 TESTAID was not used because of a 10 fold, or one order of magnitude, increase in test patterns and a consequent increase in simulation time.

Test software for the -178 PCB consists of four major parts utilizing 2586 test patterns for an overall test comprehensiveness of 90 percent. TESTAID/FASTRACE is used for the entire test and includes logic models for LSI and AM2901 devices. Specific operating requirements, of the system automatic pattern generator were not workable with the PCB sequential logic operation and therefore manual test patterns were generated.

Test software for the -972 and -178 PCBs proved highly effective during the test demonstrations as determined by the tabulated test results.

Support Facilities – A program for system support and maintenance (SM) records operating through IMAGE/1000 and QUERY was entered in the system. This program is identified by DFISML, and resides in the system fixed disc on LU19.

The DFISML data base (DB) consists of a Schema which defines all data base items and files. The Schema contains a detailed data file (SMFILE) and two master type files – one for part number (PART) and the other for service date or DATEF.

Command procedure files operating within the system QUERY are used to enter new data or update the DB. Similarly a 30 step report program, SMRPT, is used to print an SM report.

Any hardware or software item requiring SM action in the system would be printed in a report which includes part or serial number, maintenance action, labor or material cost, and date of occurrence.

The Industry Demonstration, and D/PCB test software priority on the system did not permit sufficient time to verify the SM program and report print out. The SM software is otherwise complete in form.

However, the only items requiring maintenance on the system in over 2500 hours of operation were a 94151A Programmable Driver/Comparator Card, and a TESTAID Fault Isolation Probe. Both items were serviced so that system operation was interrupted no more than 2.5 hours. Also, a spare 94151A card was ordered for the system.

With regard to the MICOM MM&T objectives for the DFI program, the foregoing overview discussions are summarized by Table III.

TABLE III. ATE IMPLEMENTED SATISFIES PROGRAM OBJECTIVES

HARDWARE	Tests Complex LSI D/PCBS
	Fault Isolates to Component
	High Reliability: 2 Faults/2500 Hr.
	Fast Maintenance, <2.5 Hr.
SOFTWARE	Test Program Time
	– MSI ≤ 2.5 Hr/IC
	– Modeled LSI ≤ 3.7 Hr/IC
	SA Functional Test Time (8080 μP)
	vs. Functional Model Test, 1:2 Ratio
	IMAGE/1000 for Production Records and Reports
	System Functional Test allows Fast Fault Isolation
PERFORMANCE	GO/NO-GO Test, $1<T<9$ Minutes
	Fault Isolation, $0.2<FI<12$ Minutes
	Test Throughput, (Implementation Plan CDRL-A006)
GROWTH	One Controller, 3 Test Stations, 6 Terminals
ECONOMIC FACTOR	High Value Return/$ Invested

SECTION 2
WORK ACCOMPLISHED

1. TEST SYSTEM CONTROLLER AND EXECUTIVE SOFTWARE

The System Controller combined with its Executive Software enables the DTS-70 to operate 3 different production test stations simultaneously with as many as 6 different engineers developing new test software at the same time.

The hardware and software breakdown of the test System Controller is shown in the table opposite. The hardware block diagram is shown in the facing figure.

The System Controller (SC) uses the HP 1000 computer system (HP 2113A) as its central core of operations. It has been supplied with 256 KBytes of high performance memory and a 16 channel I/O. With this SC, the DTS-70 can support high-level languages (such as FORTRAN, COBOL, BASIC, and ATLAS...). It has the capability of controlling 3 Test Stations, reducing the need for test software to one set of software for every 3 Test Stations. The SC, by allowing additional peripherals to be easily integrated with the system, is conducive to system expansion. The SC hardware consists of four major elements.

HP Interface Bus (HP-IB) – HP's implementation of IEEE Standard 488-1975, Digital Interface for Programmable Instrumentation. The HP-IB is capable of linking up to 15 devices at one time.

Disc Drive – HP 7906/20 is a 20 MByte master disc drive with a disc controller for interface with the HP 1000. It has an upper (removable) and lower (fixed) disc, each having a 10 MByte capacity. Each disc is subdivided further into:

- 4 Logic Units (LU)
- 203 Tracks (TRK)/LU
- 12.2 KBytes/TRK

Line Printer – The HP 2608A/210 is a 132-column, 400 LPM printer. It has a 128 ASCII character set with the option of other language sets. It also provides graphic and double sized printing.

Keyboard/CRT Terminal – The HP 2645A is a keyboard/display terminal with 4096 bytes of RAM memory. The keyboard is full ASCII code with 8 function keys and 12 editing/control keys. The CRT screen is 24 lines by 80 columns with video and inverse video display modes. The terminal also is equipped with 2 mini-cartridge tape transports (cassettes).

For the DFI program, five elements of HP system executive software were provided.

RTE IVB – The Real Time Executive (RTE), version IVB is the operating system software. It programs in FORTRAN and HP Assembler with expansion capability for other languages. RTE manages operations of the computer, main memory, disc memory storage, and all I/O devices.

IMAGE/1000 – This is a user-oriented data base management system, that is interactive with BASIC, FORTRAN, and HP Assembler. It can be operated from multi-terminals and has provisions for protecting the data base from unauthorized users. IMAGE may be used for production inventory control or production test reports.

TESTAID – This software supplies simulator-based test program generation for D/PCB's. It can be used to both manually and automatically generate test patterns for fault isolation, while simultaneously keeping track of the percent fault detection. TESTAID is made up of the following subprograms:

- SGLST – Topology generation.
- SMSET – Fault directory generation.
- SIMUL – Simulator and test pattern generation.
- PATDK – Post processor program, creates the Preliminary Test File for FASTRACE.

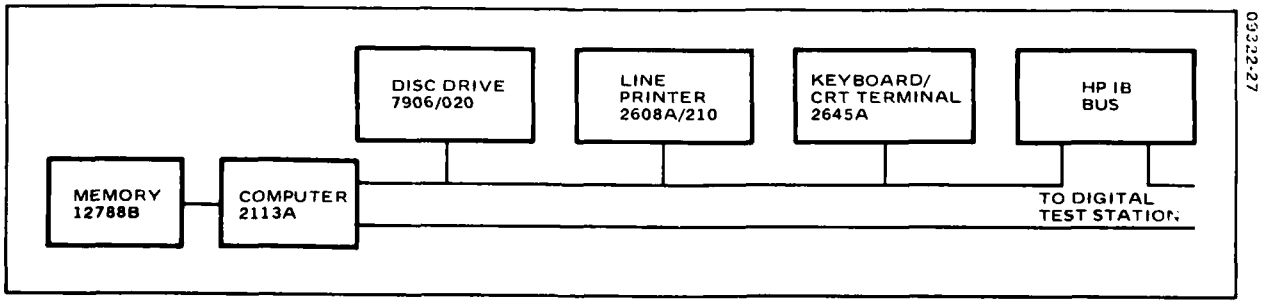
FASTRACE – This software provides test program execution for D/PCBs. It performs pass/fail testing and the computer-guided probing if a failure is found. FASTRACE is made up of the following subprograms:

- SETUP – adds hardware setup data to the Test file.
- CHECK – performs hardware confirmation of values specified in SETUP.
- PONOF – applies and removes power from the UUT.
- GONO – performs the pass/fail test on the UUT.
- PROB – performs fault isolation to the node on a failed UUT.

Diagnostic Self Test – Software for two tests is provided to verify test station operation. These are the System Functional Test (SFT) and the System Performance Test (SPT). The SFT is a comprehensive test which verifies that the various stimulus, response, measurement, and switching functions of the Digital Test Unit (DTU) are working correctly. It serves as a good test for checking system integrity before actual production testing begins. The SPT serves as an excellent overall system calibration test and is used for maintaining functions to the required specifications.

DFI TEST SYSTEM CONTROLLER

Hardware	Software
Computer - 2113A - 16 I/O Channels	RTE IVB - Operating System, 92067A/031
Memory - 12788B - 256 KByte	IMAGE/1000 - DBM, 92063/020
Peripherals - Disc Drive - 7906/020, 20 MByte - Line Printer - 2608A/210, 400 LPM - Keyboard/CRT Terminal; 2645A	TESTAID - Simulator, 91075B FASTRACE - Fault Isolation Diagnostic Self Test, Tape CT
Interface - HP-IB	



Hardware Block Diagram of Test System Controller. The easy integration of additional peripherals makes the test system controller conducive to expansion.

2. DESCRIPTION OF THE DIGITAL TEST SYSTEM

The HP 9571A Digital Test Station can handle the testing of D/PCBs containing multi-power requirements and mixed family logic. It is well-suited to meet the challenges of the '80s in D/PCB testing requirements.

The HP 9571A Digital Test Station block diagram is shown in the figure opposite. The following describes features of the test station's major hardware.

Digital Test Unit (DTU) – The DTU is an integral part of the digital test station. It is computer controlled through user programs to generate stimulus signals to the unit under test (UUT), to check the expected responses, and to interrupt the controller in case of a test failure. The DTU is capable of testing TTL, CMOS or mixed logic PCB. For mixed logic testing, the DTU contains 18 programmable driver/comparator (PDC) cards with a capacity expandable to 24 cards. Since each card operates with 15 DTU I/O pins, the 18 cards provide a total of 270 I/O pins for the DFI system configuration.

To accommodate mixed logic or frequent changes in board logic types tested, the PDC card can operate under program control. Logic high or low voltage circuits (2 each) may be programmed over a range of -16V to +16V with ±80mV accuracy. The programmed voltage is common to all 15 I/O pins in any one set. Each driver can supply a maximum of 20mA up to 14V. The PDC card can operate with any one of four voltage reference sets supplied by the DTU.

Programmable Rate Generator (PRG) – The PRG is an option that provides a digital waveform signal on a coaxial connector at the system interface. It is used whenever high-speed clocking is required to clock counters, shift registers, or to provide high-speed refresh clocks for dynamic devices. PRG output is controlled by a user test program. Its waveform can be a continuous pulse train or a specific number of pulses from 1 to a maximum of 32,767. Pulse width and pulse delay are both programmable from a minimum of 100 nsec to maximum of 100 sec at a resolution of 0.1%, thus allowing a maximum repetition rate of 5 MHz.

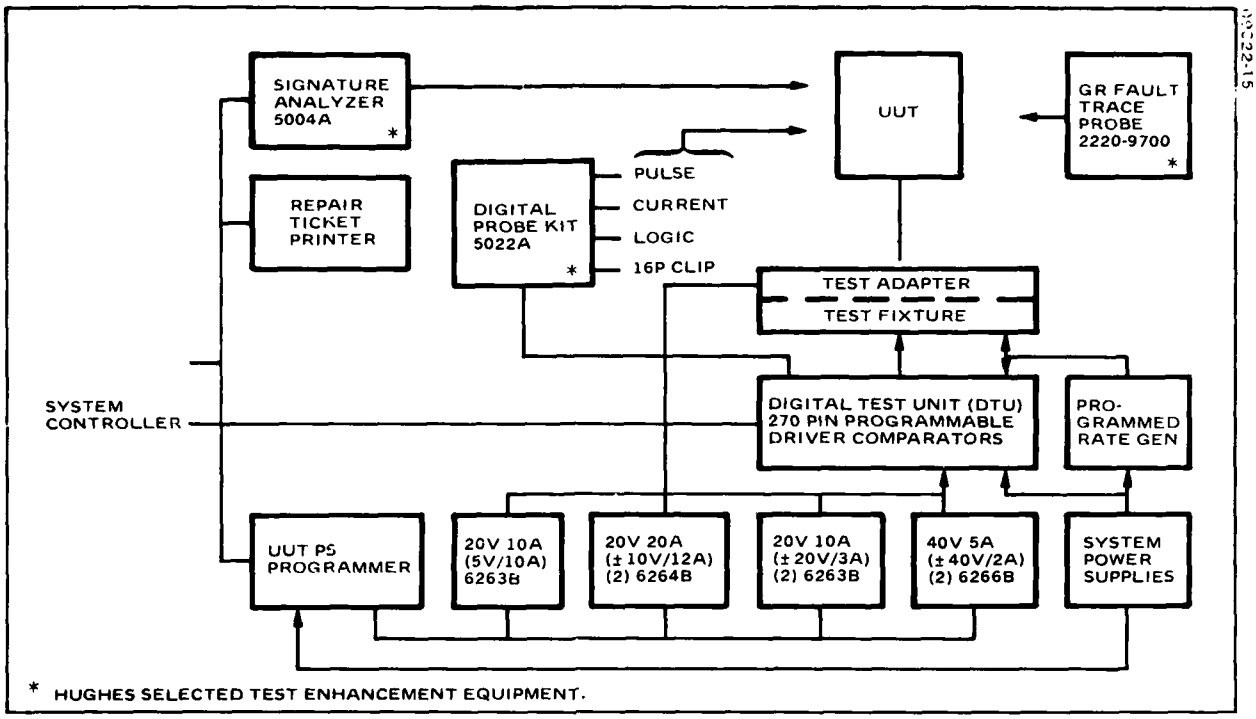
Repair Ticket Printer – The HP 5150A Thermal Printer provides a hard copy of the test failure report. The printer outputs the test result at 6 lines per inch on a 2-1/4 inch wide strip of paper. The report can be conveniently torn off and attached to the failed D/PCB for repair station action. It is controlled via the HP-IB.

System Power Supplies (SPS) – The SPSs furnish all the operating power required by the DTU. There are four SPSs used by the DTU: +5V, ±20V, and +12V. The +5V power supply provides VCC power to all the printed circuit assembly logic circuits used in the DTU. The ±20V supplies are used in the voltage reference probe, and the driver comparator circuits. The +12V supply is for controlling the thermal cutoff assembly, which protects the DTU from excessive room ambient heat.

Power Supply Programmer (PSP) – Through software the PSP fully controls the UUT power supplies. It is activated by the proper data command on the HP-IB. The PSP controls the voltage and current settings of the power being supplied to the UUT.

UUT Power Supplies – The DC power to the D/PCBs under test is provided by 7 programmable power supplies in the HP 9571A. These supplies are directly controlled by the PSP. Further, they feature high-performance constant-current, constant-voltage operation with built-in over-voltage protection. The HP power supplies supplied with the DFI system are:

- 6263B (3 each) - 0-20V, 0-10A for low current applications
- 6264B (2 each) - 0-20V, 0-20A power for high current logic applications



HP-9571A Digital Test Station Block Diagram. The diagram shows digital test station plus additional test enhancement equipment selected by Hughes to resolve a PCB circuit node fault to the individual component level.

2. DESCRIPTION OF THE DIGITAL TEST SYSTEM (Continued)

- 6266B (2 each) - 0-40V, 0-5A used for D/PCBs containing +28VDC logic families.

This set of power supplies was selected based on the power requirements needed to test the 21 D/PCBs surveyed in the basic study.

Test Fixture/Test Adapter – The test fixture (PN 09570-60018) provides the mechanical holding apparatus for securing the board-under-test and serves as the electrical port through which all test signals pass between UUT and DTU.

Used with the test fixture is the test adapter. The test adapter is specially designed to mate with the test fixture and each test adapter accepts passive or active circuitry to suit the test requirements of the individual UUT. Together the test fixture and the test adapter form the interface between the UUT and the DTU.

As shown in the figure, the following test enhancements were added to the system to increase its testing capabilities:

Signature Analyzer – The signature analyzer (SA) is a data compression device that takes data from an IC node and serially feeds it into a 16-bit feedback register. It then takes the contents of the register and encodes them into a hexadecimal signature. The data are sampled during a specific time interval so that the "good" signatures taken are repeatable. The SA unit detects 99.998% of erroneous data and 100% if the error involves a single bit or a mid cycle misplaced bit.

For microprocessor or LSI testing, the measured UUT pin signatures of a known good device are located in a system file and serve as a test standard for other ICs of the same type.

Digital Probe Kit – The HP 5022A Digital Probe Kit contains 4 troubleshooting aids for fault isolation to the component level. The kit contains the HP 547A Digital Current Tracer, the HP 545A Logic Probe, and the HP 548A 16-Pin Logic Clip.

GenRad Fault Probe – As is shown in the table opposite the GenRad 2220 Fault Probe is an instrument used to resolve a board node fault and locate the faulty component. It can be used to find faulty ICs, shorts and open circuits. The GenRad Probe has 3 modes of operation: the Signal Trace mode, the Connectivity mode, and the Microvoltmeter mode.

The Signal Trace mode works by injecting a 600 kHz trace current between the 2 shorted nodes and following the etch with the current-tracing probe to the fault location.

In the Connectivity mode two probes are used, one placed on a known node, while the other is swept across the board until the unidentified faulty node is found. This mode is also used to locate open circuits.

The Microvoltmeter Mode requires that the two shorted nodes be identified. A 10mA DC current source is then connected between nodes to provide a potential gradient along the etch carrying current. The small IR drop is sensed by the microvoltmeter as an increasing or decreasing potential as one probe is moved away from the other along the track. When the meter reading no longer changes the short has been found.

GenRad 2220 FAULT PROBE CAPABILITIES AND MODES OF OPERATION

- **Capable of Finding**
  - Shorts/opens between IC pin and VCC or ground.
  - Shorts/opens between adjacent IC pins.
  - Faulty ICs
  - Shorts between etch on a board.
- **Modes of Operation**
  - Signal Trace. Used for locating a short between 2 nodes when both nodes are known.
  - Connectivity. Used to physically locate the second node, if fault is diagnosed as one node shorted to another unidentified node.
  - Microvoltmeter. Useful in finding shorts between power bus and ground tracks.

1. SELECTION OF THE AN/TPQ-36 CIRCUIT BOARD PN-1635972 AND THE HMD-22 CIRCUIT BOARD PN-1646178

In the DFI Basic Study, a D/PCB survey was conducted to find the most complex D/PCBs available in today's industry. From the resulting list of 21 D/PCBs (representing the worst cases any ATE system would have to test) the 1635972 and the 1646178 D/PCBs were chosen as the final test candidates to be used in the ATE Implementation phase of the DFI project.

The 1635972 D/PCB is a microprocessor board used in the Signal Processor of the AN/TPQ-36 Firefinder Radar. Among the 64 circuit board types found in the radar Signal Processor, the 1635972 board is the most complex. It was selected from the list of 21 D/PCBs surveyed because it is a Hughes production board with the complexity necessary to completely exercise the capabilities of the DTS-70 system. A photograph of the 1635972 board is shown in Figure A.

Being a Hughes production board, the 1635972 D/PCB was an ideal test candidate because of its easy accessibility for the test development stage of the DFI project. This also enabled speedy board replacement from Hughes Manufacturing should any damage be incurred on the board during hardware verification. So one of the criteria used in selecting the board for testing was its production availability.

The 1635972 D/PCB's complexity is due to the LSI devices found on the board and not necessarily to the number of IC's – of which there are only 28. The 1635972 board contains the following LSI devices:

- Intel 8080-microprocessor
- 8228-system controller data bus driver
- 8255-programmable peripheral interface

These devices in conjunction with the bidirectional bus capabilities of the board make the 1635972 D/PCB an excellent test candidate for the project.

The 1646178 D/PCB is the HMD-22 display microprocessor used for air defense and air traffic control. The board's large size and complicated logic make it a prime test candidate for the DFI project.

As in the case of the 1635972 board, the 1464178 D/PCB was chosen because it is a Hughes production board of sufficient complexity to give the DTS-70 a thorough testing. A photograph of the board with the 1646178 board mounting test hardware still attached, is shown in Figure B.

The 1646178 board is difficult to test because it contains:

- LSI devices – Four AM2901 microprocessors. The AM2901 is a four-bit microprocessor slice which is cascadable to any word length. With four AM2901s mounted on the card, the 1646178 board becomes a 16-bit microprocessor.
- Sequential Logic – Having 142 IC devices mounted on it, the board has the fault visibility problems associated with sequential logic.

The 1646178 D/PCB was chosen as the second test candidate because its LSIs and sequential logic made it a complex board to test.

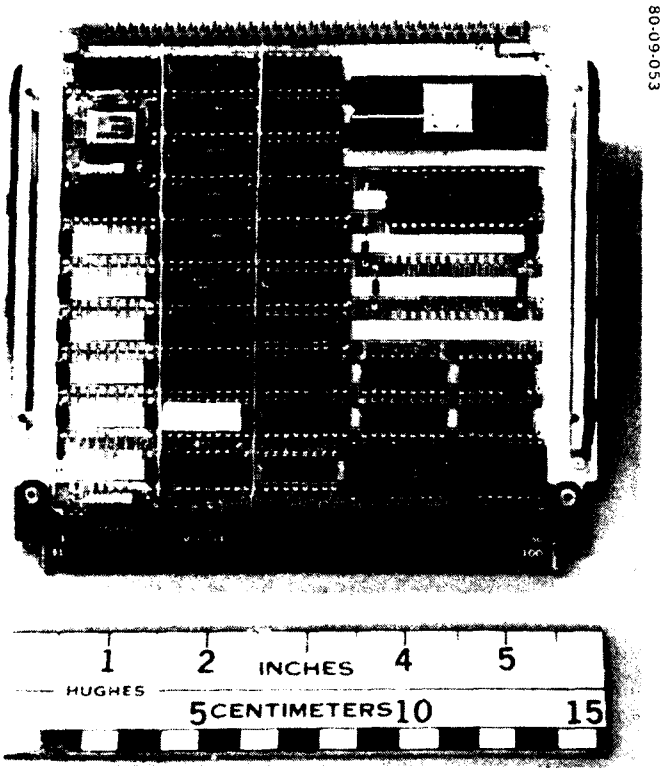


Figure A. 1635972 D/PCB. The 1635972 D/PCB provides a complex test candidate with 3 LSI and 8080 A/B microprocessor able to stress the DTS-70 test and fault isolation capabilities.

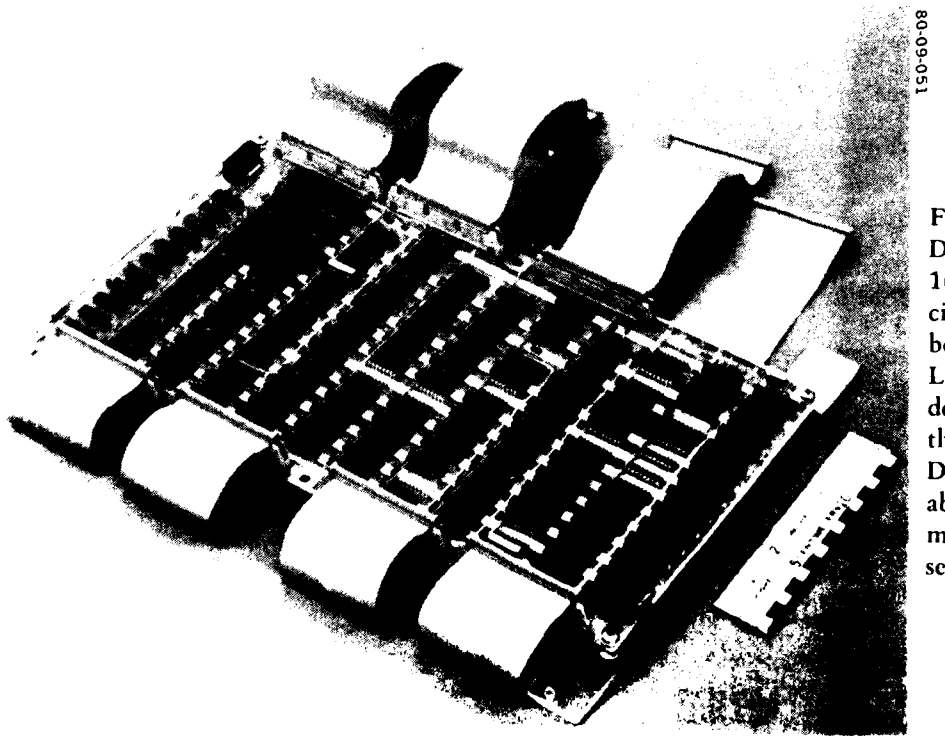


Figure B. 164178 D/PCB. This 9" x 16", HMD-22 printed circuit microprocessor board, with its four LSIs and 142 IC devices, provides a thorough test of the DTS-70 system's ability to detect both microprocessor and sequential logic faults.

Section 2 – Work Accomplished
Subsection C – Test Software for the P/N-1635972 D/PCB

1. D/PCB CHARACTERISTICS AND TEST METHOD

Two independent test processes are required to test the complete state-of-the-art, microprocessor-based, 1635972 D/PCB within 8.3 minutes. The board's complexity requires that Signature Analysis be used to test its 8080 A/B microprocessor, while HPs TESTAID/FASTRACE software can be used to test the rest of the components on the board.

The 1635972 microprocessor digital board was selected from among the 64 digital circuit board types used in the Signal Processor unit of the AN/TPQ-36 Firefinder radar system because it provided a 'worst case' test of the DTS-70 system.

Architecture, P/N-1635972 D/PCB – The -972 board, contains a total of 28 Integrated Circuits. Its hardware and functional characteristics are shown in Table I and in the facing figure.

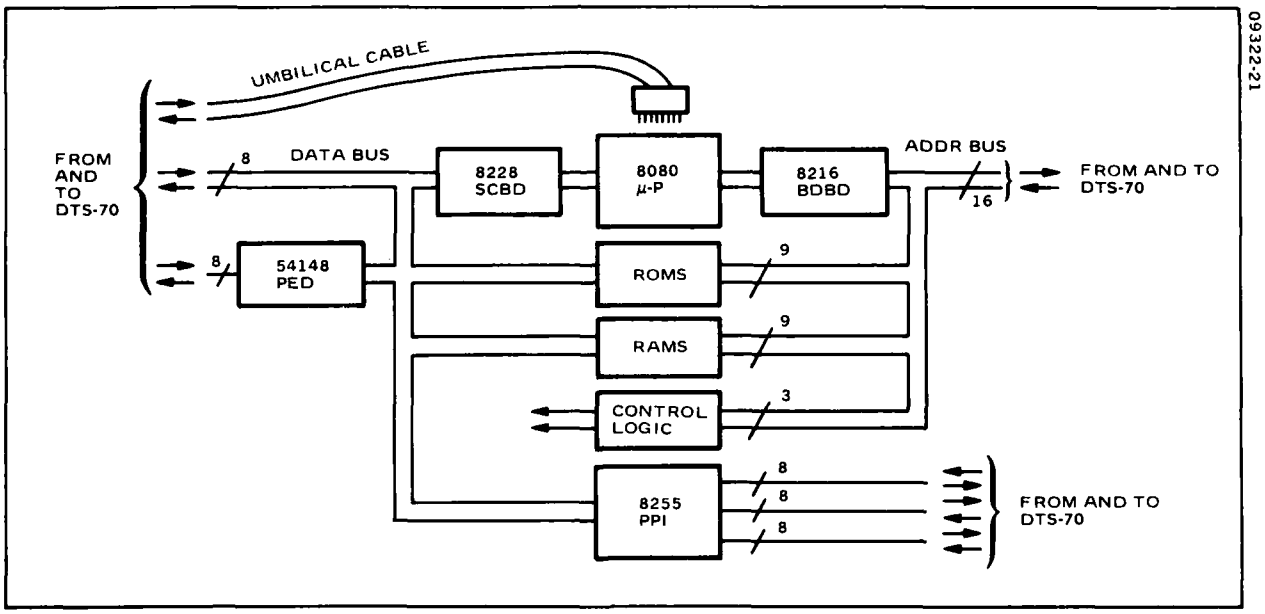
The Intel 8080 microprocessor, the heart of the entire -972 board, communicates directly to an external computer through the eight bit data bus and the 16 bit address bus (see the figure opposite). It sends or receives 8 bit data to or from three external peripheral devices through the 8255, programmable peripheral interface. The ROM contains AN/TPQ-36 system operational programs and the system self-test programs. The RAM stores temporary system programs. The 54148, Priority Encoder receives command words from an external board and generates signals to interrupt the 8080 microprocessor. An internal Clock Generator provides a 2 MHz clock in two phases for the 8080 microprocessor. The 8228, System Controller interfaces between the 8 bit data bus and the 8080 microprocessor. The 8216 Bi-Directional Bus Driver increases 8080 microprocessor output drive capacity for the data and address buses interface.

Test Method – The 1635972 board test requires two test processes. The first process uses DTS-70 system TESTAID/FASTRACE software and the second uses Signature Analysis. The vital reason for using two test processes is that the -972 board contains the 8080 microprocessor, which is not modeled in the TESTAID device library. Furthermore, it was not feasible to develop a functional model of the 8080 within the given time schedule.

Test 1, TESTAID/FASTRACE – The test program written and executed through the TESTAID/FASTRACE software is used to test the entire -972 board with the 8080 microprocessor removed from its socket and replaced by a 40 pin umbilical cable and connector (see figure opposite). The umbilical cable is connected to the DTS-70 driver comparator through the test adapter. The static test input patterns originated in the DTS-70 pass through the umbilical cable and simulate operation as if the 8080 microprocessor were providing static output patterns. The output of circuits connected to the 8080 microprocessor passes through the umbilical cable to the DTS-70 comparator. Since the test system DTU has 270 I/O pins, 102 driver comparator pins could be used to interface the 51 bidirectional pins of the -972 PCB. The system pin capacity for the PCB bi-directional pins realized an important saving in that only one specific test program had to be developed for the bi-directional case instead of two.

TABLE I. 1635972 D/PCB HARDWARE CHARACTERISTICS

Hardware Item	Quantity (ea)
Power Supply, +12 VDC (<50 mA)	1
Power Supply, +5VDC (2.5 amp)	1
Power Supply, -5VDC (<50 mA)	1
Total I/O Pins	80
Microprocessor, Intel 8080	1
System Controller Data Bus Driver, 8228	1
Programmable Peripheral Interface, 8255	1
ROM (512 word x 4 bit)	3
RAM (1024 word x 1 bit)	8
Clock Generator, 8224	1
Bidirectional Bus Driver, 8216	10
Decoder, 54138	1
Encoder, 54148	1
NAND, 54LS00	1



1635972 Functional Block Diagram and Test Operations. The board complexity and the presence of the 8080 A/B microprocessor stresses the test capabilities of the DTS-70 system.

1. D/PCB CHARACTERISTICS AND TEST METHOD (Continued)

The FASTRACE software package is used to isolate fault nodes on the board. Once the -972 board has been connected to the DTS-70 system through the test adapter and the umbilical cable has been inserted to replace the 8080 microprocessor, the operator logs into the system with the command TECH and the name of the circuit board to be tested (i.e., 1635972). Table II shows the procedure for testing the 1635972 D/PCB with the 8080 microprocessor removed using TESTAID/FASTRACE software. All statements underlined in the table are user input. The computer automatically tests the board using TESTFILE, a program generated using HPs TESTAID/FASTRACE software, and determines whether the board fails or passes. If the board fails, the computer executes PROB, which directs the operator through a backtrace process in which the fault isolation probe is used to locate the faulty node. The fault isolation time varies depending upon where the fault is located in the PCB or UUT.

The number of probe steps required to isolate a fault is a function of the number of output signals connected to a node which must be probed and also of the number of input signals controlling that output. In order to isolate a fault the operator must test these signals as directed by the computer. After this procedure has been performed, the thermo printer produces a Repair ticket, which the test operator will use to isolate the exact location of a fault on the D/PCB. To do this he uses the DTS-70 test enhancement, i.e., current tracer or Gen Rad 2220-9700 Fault Trace Probe.

Test 2, Signature Analysis of the 8080 Microprocessor – Once the -972 board is tested successfully the next step is to remove the umbilical cable and replace the microprocessor.

To test the 8080 microprocessor, the operator must connect four lines from the Signature Analyzer to -972 board test points (TP) as follows: CLK to TP2, START & STOP to TP18, and GND to TP33. Then the SACMPR program (see Topic 2.C-4) is executed to test the 8080 microprocessor. Table III shows how the test is implemented. SACMPR directs the operator to manually probe IC pins as directed by the computer. SACMPR is a Hughes developed FORTRAN software package which enables automatic comparison of stored signatures in the data table of the computer's disc memory with unknown UUT signatures probed through the signature probe and passed through the HP-IB bus. SACMPR software was developed so that it can be used universally for the Signature Analysis testing of D/PCBs once the correct reference signatures for the D/PCBs have been entered into the program's data table (see Topic 2.C-4).

TABLE II. 1635972 BOARD TEST PROCEDURE

Computer's Instructions	User's Response
PLEASE LOGON:	TECH
ENTER SELECTION:	1635972C

TABLE III. 8080 MICROPROCESSOR TEST PROCEDURE

Computer's Instruction	User's Response
PLEASE LOGON:	FMGR
:RU	NOOP (initialization)
:RU	SACMPR
:ENTER FILE NAME	T8080

2. TESTAID/FASTRACE TEST DEVELOPMENT PROCEDURES

The development of the TESTAID/FASTRACE test software for the -972 board was accomplished in three major tasks: modeling, test pattern generation, and establishing the bi-directional I/O data bus interface.

The development of the TESTAID/FASTRACE software for the -972 board required the completion of three major tasks (see table opposite). The first task was modeling the LSIs and MSIs which were not included in the TESTAID device library. The second task was generating test patterns to simulate the board. The third task was interfacing the bi-directional data bus of the -972 board to the DTS-70 programmable driver comparator card. After the completion of these three major tasks, the remaining work was to execute sub-programs (SGLST, SMSET, SIMUL, PATDK) following the procedures specified in the test generation manual (HP-91075B Vol 1B).

Task 1, Modeling – The -972 board contains the 8228, System Controller and Bus Driver, the 8255, Programmable Peripheral Interface (PPI), and the 8216, four bit parallel bi-directional bus drivers all of which required functional modeling. Of the three LSI devices, modeling the 8255 required nearly one third of the -972 board test program generation time. The detailed development of functional models is further described in Section 2.C.4.

Task 2, Test Pattern Generation – The entire test pattern of the -972 board was developed by manually analyzing individual IC functions. This manual test pattern development was a time consuming task, but it provided comprehensive test results and reduced the number of test patterns required. Consequently, the fault simulation time required per SIMUL run was substantially reduced.

The primary reason for using manual pattern generation instead of the TESTAID automatic pattern generation program, PGEN, was the requirement for LSI modeling. Since the development of LSI modeling required separate functional testing of each device and the creation of its own test patterns, the same test patterns could in turn be used as the board test patterns.

The overall test pattern generation strategy for the -972 board was to concentrate testing at the individual IC level test in lieu of testing groups of related IC's. The advantages of IC level test pattern generation are two fold. First, it takes less time to develop test patterns since the test can be restricted to one IC at a time. Second, it is very easy to debug the test programs since each faulty test number corresponds to a specific IC fault.

Task 3, Establishing the Bi-Directional I/O Data Bus Interface – The third major task was handling the bi-directional I/O data bus interface. The -972 board has 51 bi-directional I/O pins and the DTS-70 has 270 I/O pins. There were two interface options available. The first involved connecting every -972 board bi-directional pin to two DTS-70 I/O pins while providing an interface circuit between the three pins on the test adapter. The second option involved establishing a one to one connection between the DTS-70 and the -972 board. The advantage of this option is that it does not require creating an interface logic circuit. Its disadvantage is that it requires developing two separate test programs and simulations – one to test driver logic function, and the other to test the comparator logic function. We chose the first option, since the DTS-70 had enough driver comparators to interface with the 972 board's 51 bi-directional pins, and this eliminated the creation of a second test program.

TESTAID/FASTRACE TEST DEVELOPMENT PROCEDURES

Functional Modeling of LSI Devices	– 8228 system controller and bus driver – 8255 programmable peripheral interface – 8216 four bit parallel bi-directional bus driver
Test Pattern Generation	– Manual generation of test patterns – Patterns generated at IC rather than board level. This permitted the use of test patterns developed for LSI functional modeling
Bi-Directional Bus Interface	– Test adapter interface circuit connects two DTS-70 pins to each -972 board bi-directional pin

3. TESTAID/FASTRACE SOFTWARE AND MODELING OF LSI DEVICES

Through operator interaction, the TESTAID/FASTRACE software, supplied with the DTS-70 system, generates and executes the PN-1635972 D/PCB test program. To fully satisfy the TESTAID simulator software requirements, functional models were developed for three LSI devices and one MSI device on the -972 board.

TESTAID and FASTRACE are standard test software supplied with the DTS-70 system. The overall test process using TESTAID and FASTRACE is diagrammed in Figure A.

Basically, TESTAID generates the test program and FASTRACE executes the test program generated by TESTAID. TESTAID consists of four major subprograms, SGLST, SMSET, SIMUL, and PATDK, which are used during the software preparation phase. For each PC board to be tested, the four programs are used to generate a Preliminary Test File. The Preliminary Test File (PTF) contains a description of the circuit's topology and test patterns, node state information for each test pattern, and fault signatures.

FASTRACE consists of five subprograms, SETUP, CHECK, PONOF, GONO, and PROB which are used during the hardware verification phase. System dependent information, such as power supply setup, the types of boards contained in the Digital Test Unit, and the Test Adapter number are added to the PTF by FASTRACE software. FASTRACE then uses this PTF information to perform GO/NO-GO testing on real boards and to guide the operator in probing to locate suspected faults.

As seen in Figure A, the user has to generate the PC board Topology File (also called the SGLST source file) in the beginning of the TESTAID software preparation phase. This Topology File contains a coded description of the unit under test (UUT), the -972 board, in terms of logic devices. The DTS-70 system IC library supplies over 1500 devices modeled in the format required by the TESTAID/FASTRACE software. The user must therefore functionally model any UUT device not in the TESTAID device library.

For the -972 board, the 8216, 8228, and 8255 devices had to be modeled before the board could be tested. The TESTAID modeling process for these devices involves the use of TESTAID recognizable primitive gates and flip-flops already modeled in the device library. The Intel 8080 microprocessor was not modeled since the estimated modeling time was prohibitive for the DFI program. The functional test of this device is performed by a Signature Analysis method described in Section 2.C-4.

The Intel 8216 is a four bit bi-directional driver specifically designed to buffer microcomputer system components. As seen in Figure B, the 8216 has four tri-state buffered drivers and is able to achieve direct bus interface and bi-directional capability. To model the 8216, eight tri-state drivers are converted by eight primitive logic OR gates as shown in Appendix B.1.2.

The Intel 8228 is a 40 pin LSI device operating as the System Controller and Bus Driver for the 8080 microcomputer system. The 8228 generates all control signals required to directly interface RAM, ROM and I/O components.

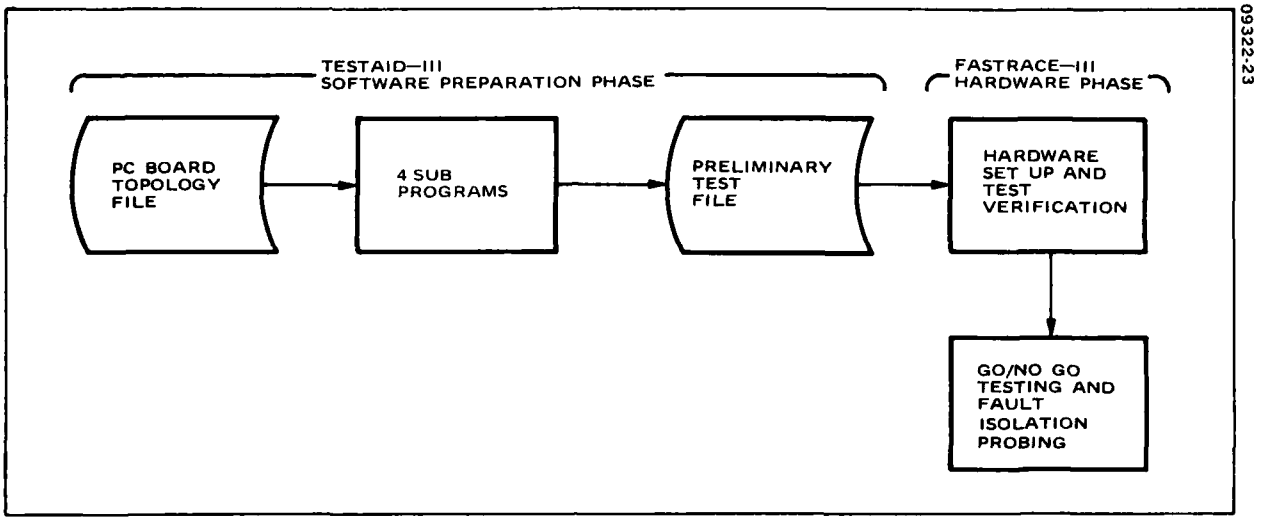


Figure A. TESTAID/FASTRACE Functional Block Diagram. TESTAID/FASTRACE is the HP test generation and fault isolation software supplied with the DTS-70 system. Hughes implementation of this software for the 163572 D/PCB required extensive effort to model the LSI and MSI devices on the D/PCB.

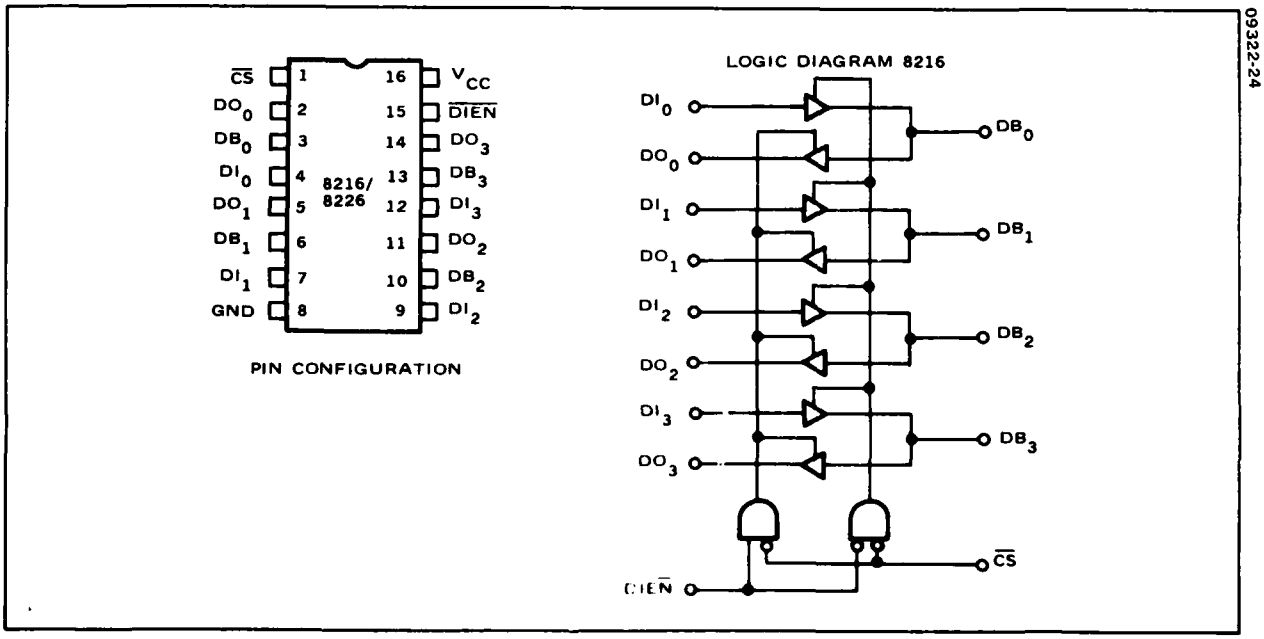


Figure B. Intel 8216 Functional Block Diagram. Additional test adapter circuitry was provided by Hughes to successfully model the 8216 device.

3. TESTAID/FASTRACE SOFTWARE AND MODELING OF LSI DEVICES (Continued)

As seen in the 8228 functional block diagram, Figure C, the 8228 has three functional blocks: the bi-directional bus driver, the status latch, and the gating array. The Bi-directional Bus Drivers are modeled using 16 OR gates (R1 through R15 in Appendix B.1.4). The Status Latch functions are modeled by using 6 D-F/F registers (M1 through M6) found in the TESTAID device library. Since data bits 2 and 3 do not contribute decoding logic for the control signal, only 6 D-F/F registers are used. Finally, the Gating Array functional blocks are modeled using 5 NAND gates (N1 through N5), and 4 AND gates (A1 through A4). Refer to Appendix B.1.4 for the complete schematic drawings of the model.

The Intel 8255 is a 40 pin LSI, eight channel, four port Programmable Peripheral Interface (PPI) device. As seen in Figure D, the INTEL 8255 has 24 I/O pins which may be individually programmed in two groups of 12 and is used in three modes of operation. Reference to the Intel User's Manual (MCS-80) will provide further details of operation.

Upon analyzing the three modes, it is found that all three modes commonly use the READ/WRITE control, Bi-Directional Data Bus, 8-bit internal Data Bus, Group A Control, and Group B control logic functions. The differences between the three modes involve Group A and Group B I/O ports and their associated decoding logic, which provide less than one third of the device's operations. After a series of trade-off studies, considering both the program schedule and test comprehensiveness requirements, it was decided to model the 8255 PPI for mode 0 operation only.

As is shown in Appendix B.1.1., the READ/WRITE control block of the PPI is modeled using seven 4 input NAND gates, U165 through U170, and five inverters, U121 through U125. The output of control blocks, $\overline{PAW}$, $\overline{PBW}$, $\overline{PCW}$, $\overline{PAR}$, $\overline{PBR}$, and $\overline{PCR}$ control ports A, B, and C for READ and WRITE operation. The delay lines, D10 through D13, are used to prevent a race condition during the READ/WRITE and port select operation. Port A, B, and C functional blocks are modeled using OR gates for the bi-directional data bus and D-F/F registers to latch the outputs during the WRITE operation.

The detailed description of each port follows. The port A functional blocks are modeled using 16 OR gates, U64 through U79, for the bi-directional data bus; 8 D-F/F registers, FF14 through FF17, for output data latching during the WRITE operation; and 16 OR gates, U48 through U63, for internal data bus communication.

The port B functional blocks are modeled using 16 OR gates, U96 through U111, for bi-directional data bus; 8 D-F/F registers, FF22 through FF25, for output data latch; and 16 OR gates, U80 through U95, for internal data bus communication.

The port C functional blocks are also modeled using 16 OR gates, U32 through U47, for bi-directional data bus; 8 D-F/F registers, FF6 through FF9, for output data latch; and 16 OR gates, U24A through U31B, for internal data bus communication.

The Data Bus Buffer functional block is also modeled using eight pairs of OR gates, U1 through U16, which interface between the 8 bit internal data bus and the 8 bit external data bus.

The group A and group B control functional blocks are created by using 8 D-F/F registers, FF1 through FF4. The output of the group A and group B registers are decoded using INVERTERS (U126, U127, U128, U131, U132), AND gates (U148 through U150, U152, U153) and OR gates (U151, U154) to control the ports A, B, and C for mode 0 operation.

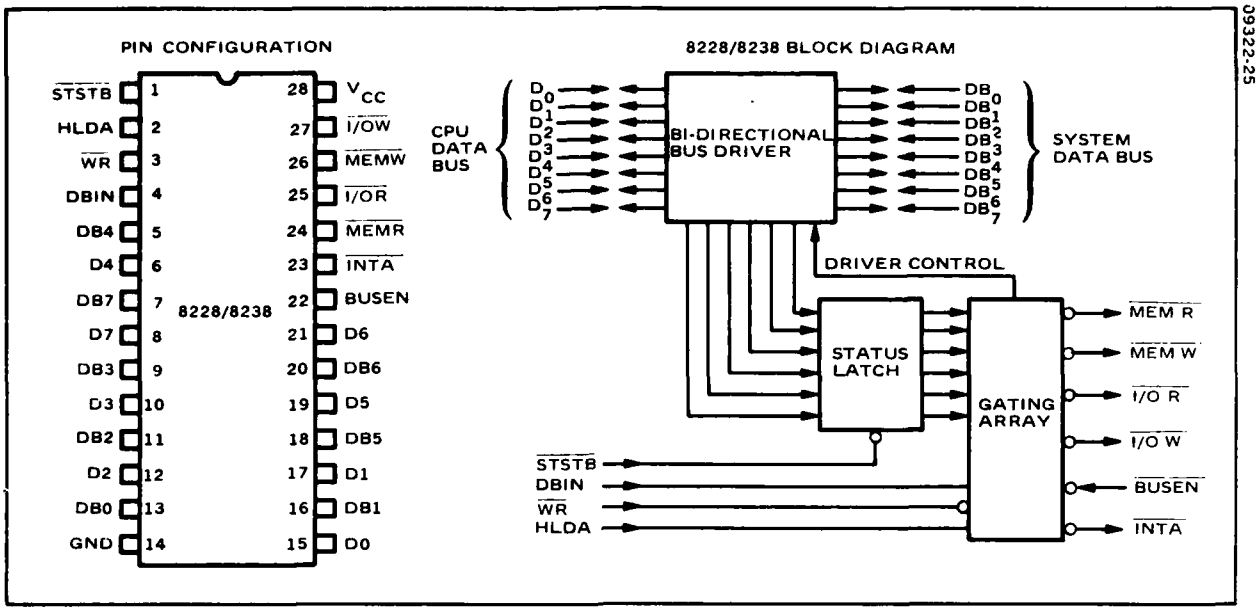


Figure C. Intel 8228 Functional Block Diagram. The Intel 8228 System Controller has three functional blocks requiring modeling, the bi-directional bus driver, the status latch, and the gating array. Each of these required different modeling techniques.

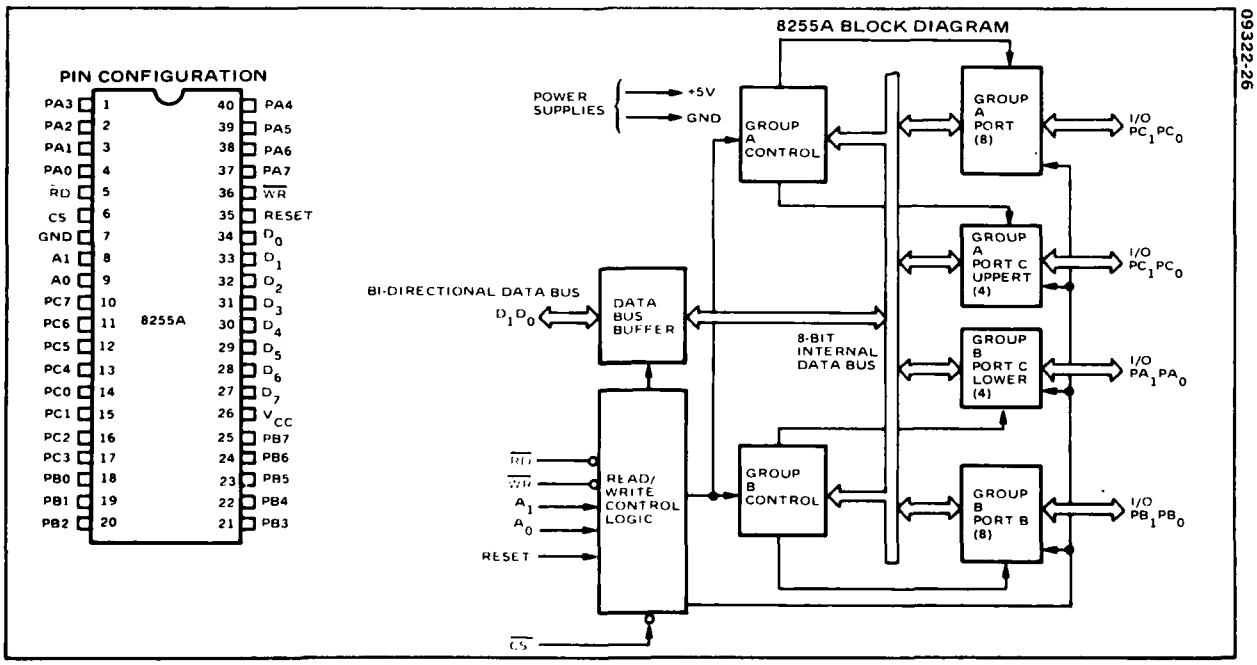


Figure D. Intel 8255 Functional Block Diagram. Most of the 1635972 D/PCB modeling time was spent on the Intel 8255A Programmable Peripheral Interface.

4. FORTRAN SIGNATURE ANALYSIS FOR THE INTEL 8080 A/B MICROPROCESSOR

Modeling microprocessors is a time consuming process, and in some cases is not feasible. Signature Analysis (SA),* to be used with the DTS-70, provides a cost-effective and work-saving alternative approach in testing microprocessors on a D/PCB.

To use the HP 5004A Signature Analyzer with the DTS-70, software programs called No-Operation (NOOP), Initialization (INIT) and Signature Analysis Comparator (SACMPR) were developed by Hughes for testing the 8080 A/B microprocessor on the -972 D/PCB. The functions of each program are identified in Table I. Since the DTS-70 includes a FORTRAN IV compiler and the HP-IB interface option, the NOOP, INIT, and SACMPR software package were written in FORTRAN.

Using these programs, the following signature analysis procedure was developed for testing the -972 board's 8080 A/B.

Step 1 – The external program NOOP or INIT is used to free run the 8080 A/B on the board. The NOOP program initiates the HP computer to send the 8080 microprocessor the NOP instruction (all seven data bits in a low state). This enables the 8080 program computer to cycle continuously and provides a specific signature at every address output. Unfortunately, the simple NOOP program does not provide valid signatures at the data lines. The data line signatures, being all zeros, are ambiguous since they are indistinguishable from a data fault condition. To alleviate this condition, the INIT program was developed. It operates through the external test adapter ROM and toggles all the control, address, and data lines. The toggling of the control, address, and and data lines provides the unique signatures needed for each node on the microprocessor to be tested by Signature Analysis. Because the INIT program was developed to be compatible with Intel assembly language, it can execute the 8080 microprocessor's 72 instructions during the SA test. Therefore, INIT provides a potentially complete SA test approach for 72 instructions of the 8080 microprocessor. However, during the industry demonstration, the INIT program was developed for only 11 instructions.

Step 2, SACMPR Data Table – By inserting a known good board into the Test Adapter and probing signatures at preselected nodes, a good board data table was created (see Table II) which contains a listing of the nodes to be tested, identifies the correct signatures for each node, and provides testing instructions to the operator.

The following discussion explains the entries in Table II. Appendix A.1.6 has a complete listing of the table for further reference. Words one through three (columns one through six) contain the six character node name in a right-justified format. Words four and five (columns seven through ten) contain the four character correct signature for that node. Words six and seven (columns eleven through fourteen) are left blank, as SACMPR will create a good or bad flag indication during run-time. Word eight (columns fifteen and sixteen) contains the two character "GOOD GOTO" row pointer. Word nine (columns seventeen and eighteen) contains the two character "BAD GOTO" row pointer. Word ten (columns nineteen and twenty) contains the two character "FROM" row pointer. To indicate the end of data table, the word STOPST and ENDEND should be entered into the node name field.

*See Hewlett-Packard Application Note #222, A Designers' Guide to Signature Analysis.

TABLE I. SIGNATURE ANALYSIS PROGRAM FUNCTIONS

NOOP	• Turns on the power supply for the -972 board • Applies NOP instruction to the 8080 microprocessor by applying DB 0 thru DB 7 all to logic zero • Resets momentarily the 8080 microprocessor • Enables the System Controller and Address Buffer • Toggles all address lines on the microprocessor continuously.
INIT	• Turns on the power supply for the -972 board • Enables the external ROMs in the Test Adapter • Resets momentarily the 8080 microprocessor • Enables the System Controller and Address Buffer • Toggles all address and data lines on the microprocessor continuously.
SACMPR	• Compares known good signature with an unknown signature or a probed signature • Directs user for forward or backward probing or re-probing.

TABLE II. SAMPLE SIGNATURE FILE FOR 8080 MICROPROCESSOR USING NOOP

	Node Name			Correct Signature	Good Flag	Bad Flag	Good GoTo	Bad GoTo	From
Row #	1	2	3	4 5	6	7	8	9	10
	1 2 3 4 5 6			7 8 9 10	11 12	13 14	15 16	17 18	19 20
1	U 4 5 . 2 0			7 5 5 U			2	0	0
2	U 4 5 . 2			0 0 0 0			3	0	0
3	U 4 5 . 1			H H 8 6			4	0	0
⋮	⋮			⋮			⋮	⋮	⋮
28	S T O P S T								
29	E N D E N D								

NOTE: The data are taken for the NOOP program with the START and CLOCK switches IN, and STOP switch OUT position at the HP5004A Signature Analyzer front panel.

4. FORTRAN SIGNATURE ANALYSIS FOR THE INTEL 8080 A/B MICROPROCESSOR (Continued)

The two characters allotted to the various pointers in the SACMPR data table allow the addressing of up to 99 nodes. The data table mapping of the PCB used in the test is stored under a file name of the test engineer's choice.

In creating the data table, it is recommended that the points at which the nodes can actually be probed be identified. If, for example, a node is not directly accessible on the board connector, its equivalent point on the test adapter should be listed. It should be kept in mind in the adapter design, that all pins carrying signals which may require probing be kept in accessible locations.

Step 3, Execution of Signature Analysis Testing — To execute a Signature Analysis test the 8080 microprocessor being tested is inserted in its socket. Next the Signature Analyzer connections are made to the -972 board as indicated: CLOCK to TP2, START & STOP to TP18, GND to TP33. The UUT is then probed manually at the indicated nodes as directed by the DFI system computer. Signatures from test nodes will be compared with the reference signatures automatically. The SACMPR program can direct the user to probe forward or backward or to re-probe when the reference signature and the probed signature do not match. The SACMPR development and testing procedure is diagrammed in the facing figure.

Advantages and Disadvantages of Signature Analysis — The advantages of using Signature Analysis for testing microprocessor based boards include the following:

- The microprocessor does not have to be modeled, which reduces test program development time considerably.
- Simulation time is reduced since the D/PCB is tested without the microprocessor using TESTAID.
- Similar microprocessors can be tested by using the SACMPR program.

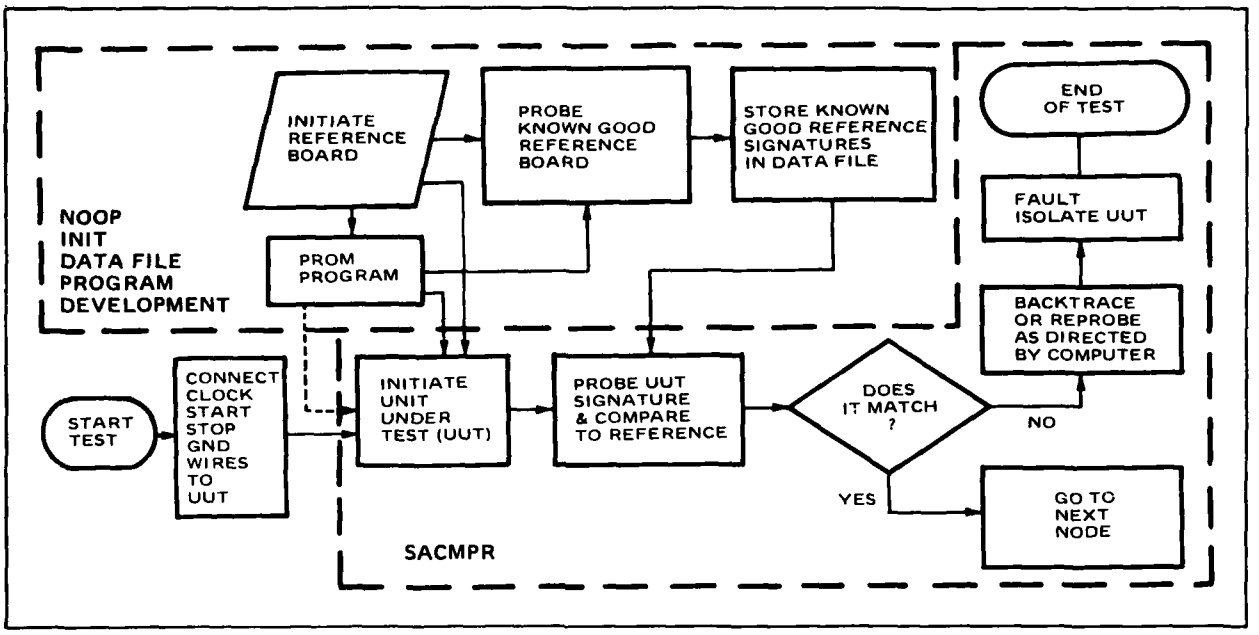
The disadvantages of Signature Analysis testing include:

- It requires a known good board to acquire reference signatures.
- It requires a program to free run the microprocessor.

Since the basic SACMPR software has already been developed by Hughes, the development of a Signature Analysis procedure for other microprocessor based boards would require anywhere from one to three man weeks.

SIGANL and SAFILS Support Programs — Two additional programs, SIGANL and SAFILS were required to support the SACMPR software. The SIGANL program minimizes the user's input when using Signature Analysis. SIGANL is a transfer file containing commands necessary to run SACMPR. The SAFILS program is a file created by the user's data table as described in Step 2. The file name(s), along with a 50-character description of the PCB test, are stored in this file. The file is scanned and listed at the beginning of every execution of SACMPR. The user then enters his choice from the list and SACMPR does the rest.

Appendix A-1 includes the NOOP, INIT, SIGANL, SAFILS, and SACMPR programs.



Signature Analysis Software Development and Testing. Signature Analysis is an effective test technique that eliminates the modeling of microprocessors.

1. D/PCB CHARACTERISTICS AND TEST METHOD

The 1646178 D/PCB test software, based entirely on TESTAID/FASTRACE, successfully applies a software model for the board's 16 bit microprocessor and executes the complete test in 4 subdivisions. It achieves a 90% test comprehensiveness.

Developed after considering alternative test methods and software techniques, the 1646178 D/PCB test software (within TESTAID/FASTRACE) has two prominent features. The first is that it uses functional modeling techniques to test the AM2901 microprocessor. Modeling was feasible since the AM2901 is a 4 bit bipolar microprocessor slice. Since four AM2901s comprise the 16 bit device for the 1646178 D/PCB, overall board modeling effort was reduced.

The second is that, because the 1646178 D/PCB contains 142 various SSI, MSI, and LSI devices, a large number of test patterns (2586) is required to test the board. The number of test patterns, combined with practical simulator limitations, required the PCB test to be subdivided in four parts (or elements).

There are two reasons for the subdivision into 4 TESTAID/FASTRACE test simulations. First, 2586 test patterns are needed to test the board. In the TESTAID program SIMUL, a certain area of the statefile is allocated for the Pattern File. This Pattern File is finite and if the number of input patterns exceeds its maximum limit, the statefile corrupts and the present SIMUL test run is lost. For the 1646178 board, a maximum of approximately 750 patterns can be entered into the Pattern File before an overflow occurs. Since 2586 patterns were required for the 1646178 D/PCB test, the patterns had to be separated into 4 tests. Second, the complete board test also required different I/O configurations to accommodate bidirectional buses found on the 1646178 board. The bidirectional buses had to be utilized as both inputs and outputs. With the DTS-70 system this could only be done by running separate tests, each with a different arrangement of inputs and outputs for the bidirectional parts. For these reasons, 4 subtests were required on the 1646178 D/PCB.

Before discussing the test further, an overview of the D/PCB characteristics is necessary. The 1646178 D/PCB is a general purpose 16-bit microprocessor containing a Data Manipulation Function, a Microsequencer Function, an External Communication Control Function, and a Clock Generation Function. The board is functionally depicted in Figure A. Its hardware characteristics are shown in Table I below.

TABLE I. 1646178 D/PCB HARDWARE CHARACTERISTICS

Item	Quantity
Power Supply, +5 VDC (8 amp)	1
Total I/O Pins	255
Microprocessor (AM2901)	4
ROM (256 word x 8 bit)	2
ROM (2048 word x 4 bit)	3
Generator, Look Ahead Carry	1
Counter	4
Latch, Addressable	2
Decoder	5
Multiplexer	21
Flip-Flops	29
Other (AND, OR, EX-OR, etc.)	71

The test pattern generation strategy used was to manually develop individual test patterns for each group of related logic functions such as the RDR or the ALU. This approach would guarantee a more comprehensive test. Unfortunately this manual process was very slow. It was necessary because it was not possible to use the TESTAID Automatic Pattern Generator (PGEN) due to the amount of sequential logic found on the 1646178 D/PCB.

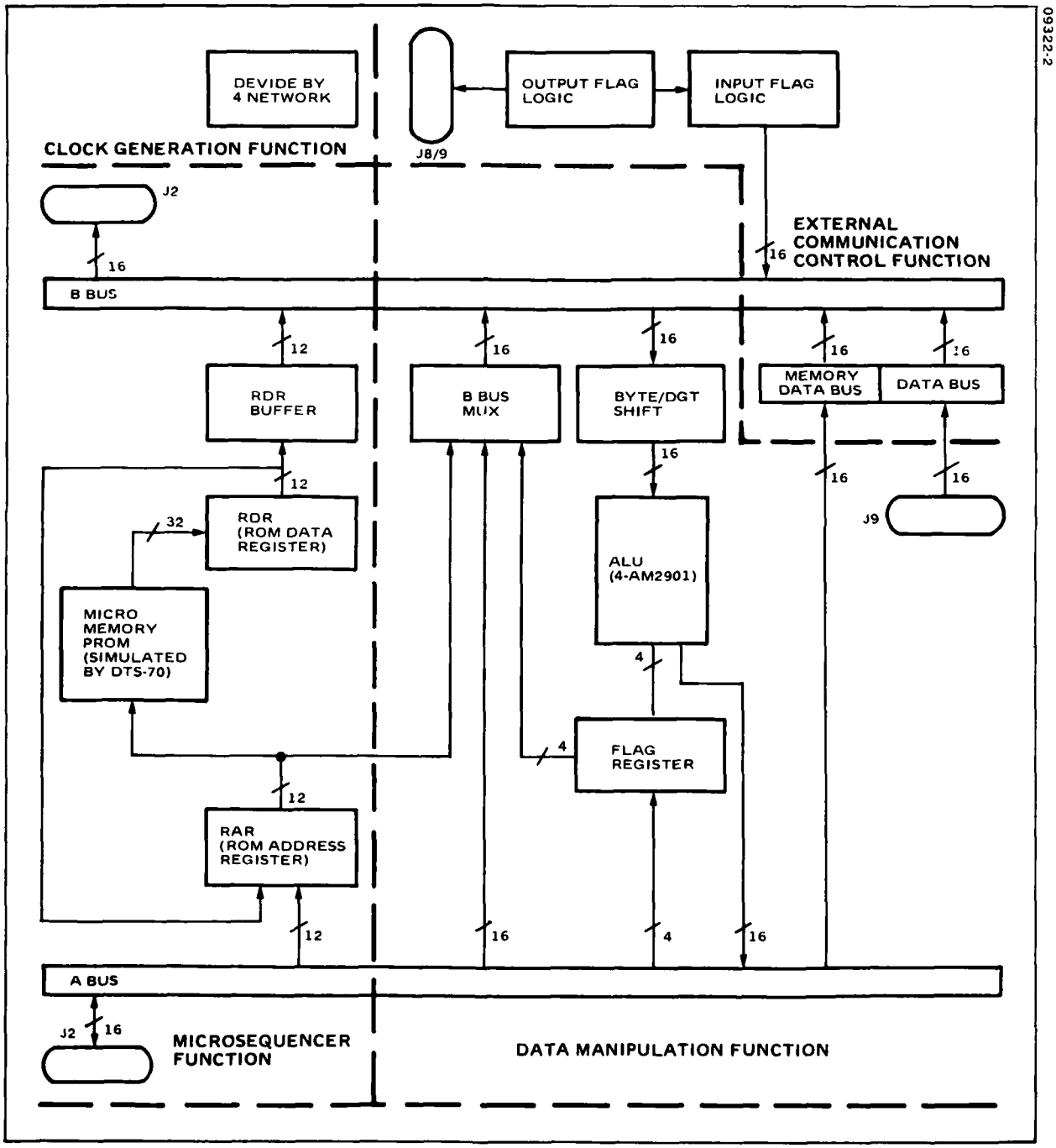


Figure A. Architecture of 1646178 D/PCB. Test partitioning (Figure B) is independent of the system architecture shown here.

1. D/PCB CHARACTERISTICS AND TEST METHOD (Continued)

A diagram of how the four tests were partitioned is found in Figure B.

Test 1 (RHFAIN) — The primary emphasis here is the testing of the Microsequencer Function of the 1646178 D/PCB. This includes tests for the RDR, RAR, and associated logic. Also tested is the B Bus Multiplexer and the RDR Buffer. The I/O configuration assigns the A bus and the Data Bus as inputs, and the B bus an output.

Test 2 (RHFFLG) — The primary emphasis here is the testing of the Flag Register, the Memory Data Bus and associated logic. The I/O configuration is the same as in Test 1.

Test 3 (RHFABO) — The primary emphasis here is the testing of the Data Manipulation Function. This includes the Byte/Digital Shift MUX and the ALU. Also tested is the Input Flag Logic associated with the External Communication Controller. The I/O configuration utilizes the Data Bus as an input and the A Bus and B Bus as outputs.

Test 4 (RHFBIN) — The primary emphasis here is the testing of the OUTPUT Flag Logic and the Clock Generator Function. The I/O configuration assigns the A Bus as an input and both the B Bus and Data Bus as outputs.

The total SOFTWARE effort can be found in Table II below. This table gives a TESTAID breakdown of the total number of program statements required for each test. Table III shows the procedure for running the 1646178 D/PCB Test itself. All statements underlined in the table are user input.

TABLE II. BREAKDOWN OF THE NUMBER OF PROGRAM STATEMENTS REQUIRED FOR EACH TEST

Testaid	Test 1	Test 2	Test 3	Test 4
SGLST (# statements)	2390	2390	2390	2390
SMSET	-	-	-	-
SIMUL (# patterns)	721	694	778	393
PATDK (# statements)	19	19	19	20

TABLE III. 1646178 BOARD TEST PROCEDURE

Computer's Instructions	User's Response
PLEASE LOGON:	TECH
ENTER SELECTION:	1646178 TEST1
ENTER SELECTION:	1646178 TEST2
ENTER SELECTION:	1646178 TEST3
ENTER SELECTION:	1646178 TEST4

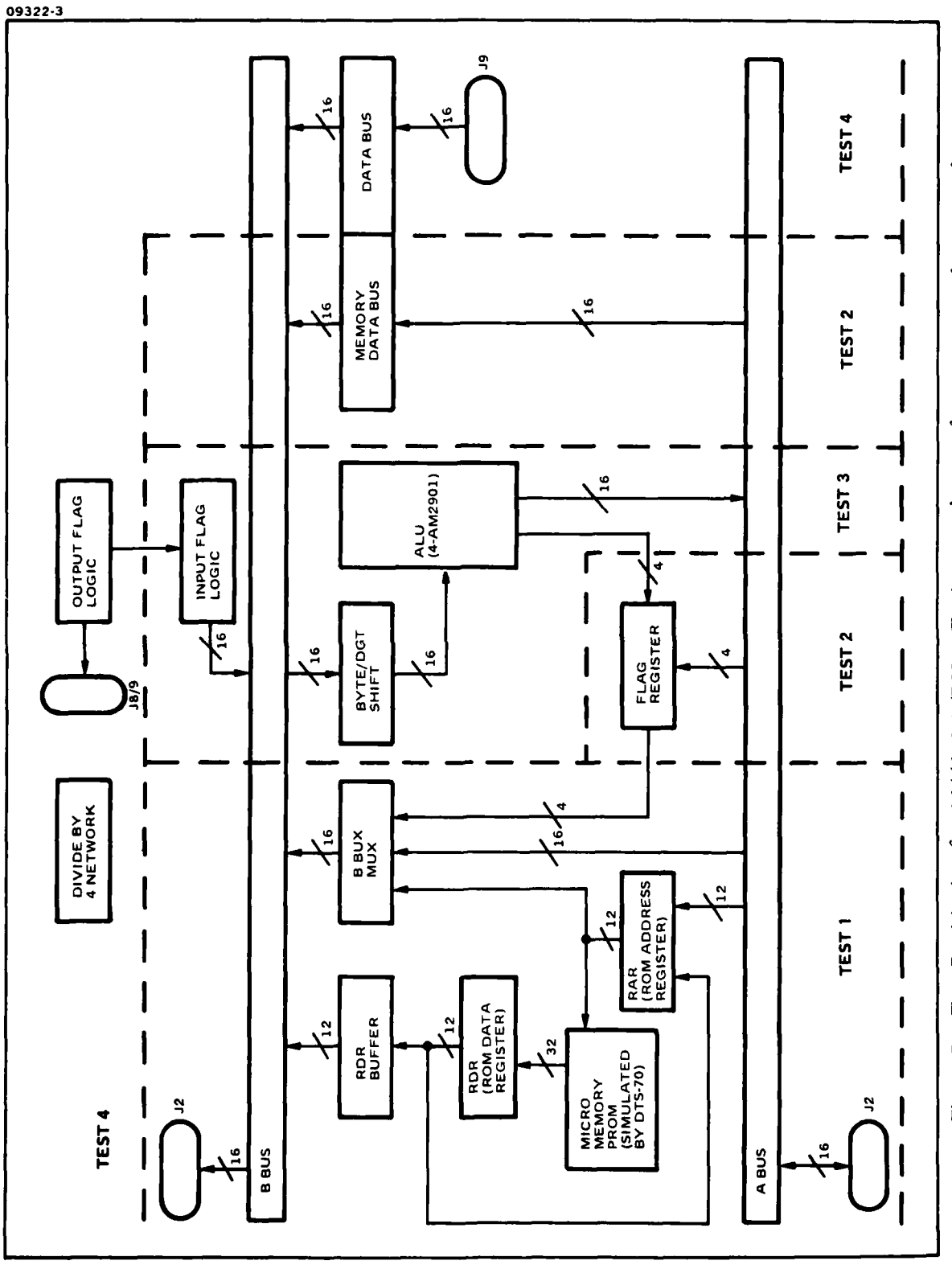


Figure B. Test Partitioning for 1646178 D/PCB. Testing was done in four parts in order to avoid overflow of test system Pattern File, and in order to perform the bidirectional bus test on the board.

2. SOFTWARE MODELING OF THE AM 2901 LSI DEVICE

The AM2901 LSI device was not in the test system library and had to be modeled for the 1646178 D/PCB. The development of the model for this device was enhanced by the use of the MSI models developed by HP.

It was shown previously that the 1646178 D/PCB could be broken into 9 basic IC categories. Of these 9 categories, the ROMs and the microprocessors were the only ones that required Hughes modeling. The other 7 IC categories contained MSIs already HP modeled in the TESTAID Device Library (see TESTAID-III, Integrated Circuit Device Library (91075-93016)). Since 93% of the ICs found on the 1646178 D/PCB were already modeled, the total modeling time and effort was reduced substantially (see Implementation Plan — CDRL A006).

The ROMs were modeled using Hewlett-Packard TESTAID Primitives (see TESTAID-III, Programming and Operating Manual (91075-93018)). These models were made using the direct application of the ROM and Decoder Primitive.

The AM2901 model is a hierarchy of submodels as shown in the figure opposite. Separate models had to be developed for the RAM, ALU, Q-Register and the Microinstruction Decoder. These submodels were then combined with TESTAID device models and Primitives to produce the functioning microprocessor model.

The following is a brief discussion of each Hughes device model.

RAM — (Refer to RAM schematic, Appendix B.3.2). The AM 2901 uses a 16-word by 4-bit 2-port RAM. During a read operation, the RAM 'A' port is controlled by the A address field and the 'B' port is similarly controlled by the B address field. When in the write mode, data is written only into the RAM file specified by the B address field. Modeling this device required setting up two 16-word by 4-bit RAMs using the TESTAID Primitives. The data inputs to the two RAMs were then made common. During a read operation, the separate 'A' RAM AND 'B' RAM act independently. In a write mode, the 'B' RAM address field is forced into the 'A' RAM address field so that identical data can be stored into the parallel RAMs. The AM2901 RAM device was modeled using the RAM and Decoder Primitives plus library devices 74157 and 5477.

ALU — (Refer to ALU schematic, Appendix B.3.3.) The ALU (arithmetic logic unit) for the AM2901 performs 8 arithmetic logic operations. The Hughes model of this ALU is centered around the TESTAID model for the 74181, an arithmetic logic unit function generator. The Hughes model of the AM2901 takes the ALU Function OP code at the Microinstruction Decoder and translates it into a code that produces the same function in a 74181. This enables the Hughes model to emulate the real operations of the AM2901.

Q-Register — (Refer to AM2901 model schematic, Appendix B.3.1.) The Q-Register is used for shift multiplication, division operations. The Hughes model of this Register was only partially successful due to an inherent feedback condition. During a Q-Register multiplication, division shift operation, the Q-Register becomes the data source and the data destination, simultaneously. The TESTAID simulator interprets such a condition as indeterminable and loads the Q-Register with Xs, which represent the unknown states. To try and break this race condition, an unsuccessful double latch model was devised for the Q-Register. It was then decided to postpone further effort on the Q-Register to continue with the total board test. Due to time constraints this problem was never resolved. Since this model was not completely successful, further details of its operations will be omitted. The present Hughes Q-Register model can only store external data

and RAM data. The two latches used for this model were the 74363 and the 5477 both available in the TESTAID device library.

Microinstruction Decoder – (Refer to Microinstruction Decoder, Appendix B.3.4.) The AM2901 has an 8-bit microinstruction that controls ALU Function, ALU Source, and the destination of the ALU's resultant data, F. The microinstruction Decoder was modeled using 3 ROM decoder networks which output the control signals needed to implement the correct microinstruction operation.

It is important to note that this present AM2901 model can perform all the functions necessary to completely test all of the 1646178 D/PCB except for its Q-Register shift operations. The Q-Register Shift operations constitute only 6% of the total AM2901 functions. This indicates that 99% of the AM2901 is functionally tested by the present mode. Therefore, although the actual AM2901 logic test is compromised, the total board test comprehensiveness is not compromised.

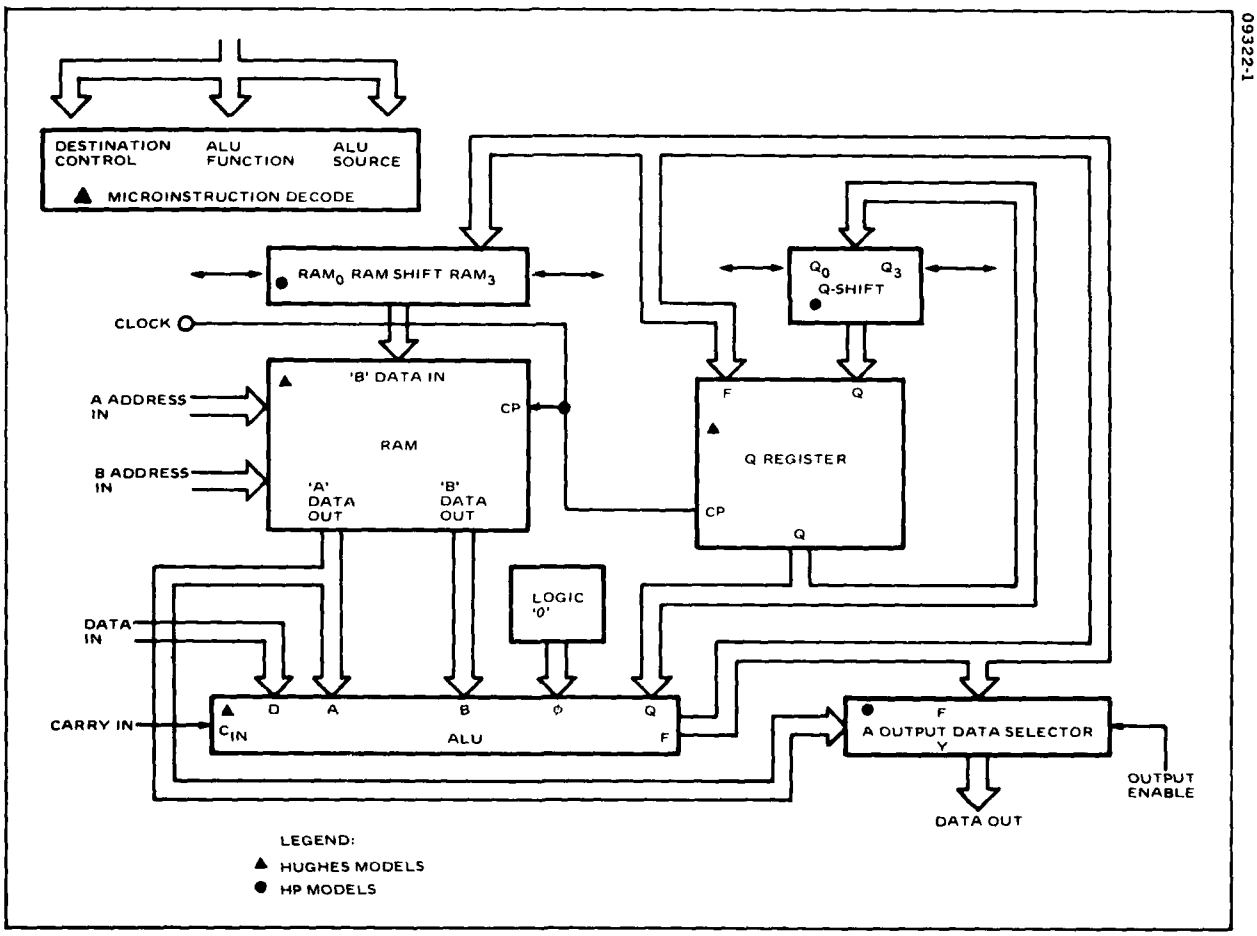


Figure A. Block Diagram of AM2901 Model. As is indicated by the legend, the AM2901 model is a composite of submodels developed by Hughes and HP.

3. ENHANCING SIMULATION RUNNING TIME THROUGH USE OF A FORTRAN PACKAGE

Because of the large quantity of test patterns (over 2500) required to test the 1646178 D/PCB, a Hughes developed software package, SPEDUP, was used to reduce the TESTAID simulation time. SPEDUP can be used to reduce testing time for other D/PCBs as well.

The SPEDUP software package, written in FORTRAN, reduces simulation time by removing all previously detected faults. A SPEDUP flow diagram appears in the figure on the facing page. To understand how SPEDUP works, a brief description of the following programs is given:

- HP TESTAID software, which includes:
  - SIMUL, the Digital Simulator Program that simulates the static and dynamic response of the PCB to test patterns and detects faults.
  - SMLST, a utility program which generates an easily readable listing similar to SIMUL
- HUGHES SPEDUP software (see Appendix A.2 and A.3 for flow charts and detailed listings) consist of:
  - LNDEL, a program used to remove all detected fault lines from a SMLST output file
  - MKUND, a program that enables SIMUL to execute faster and more efficiently after its initial run

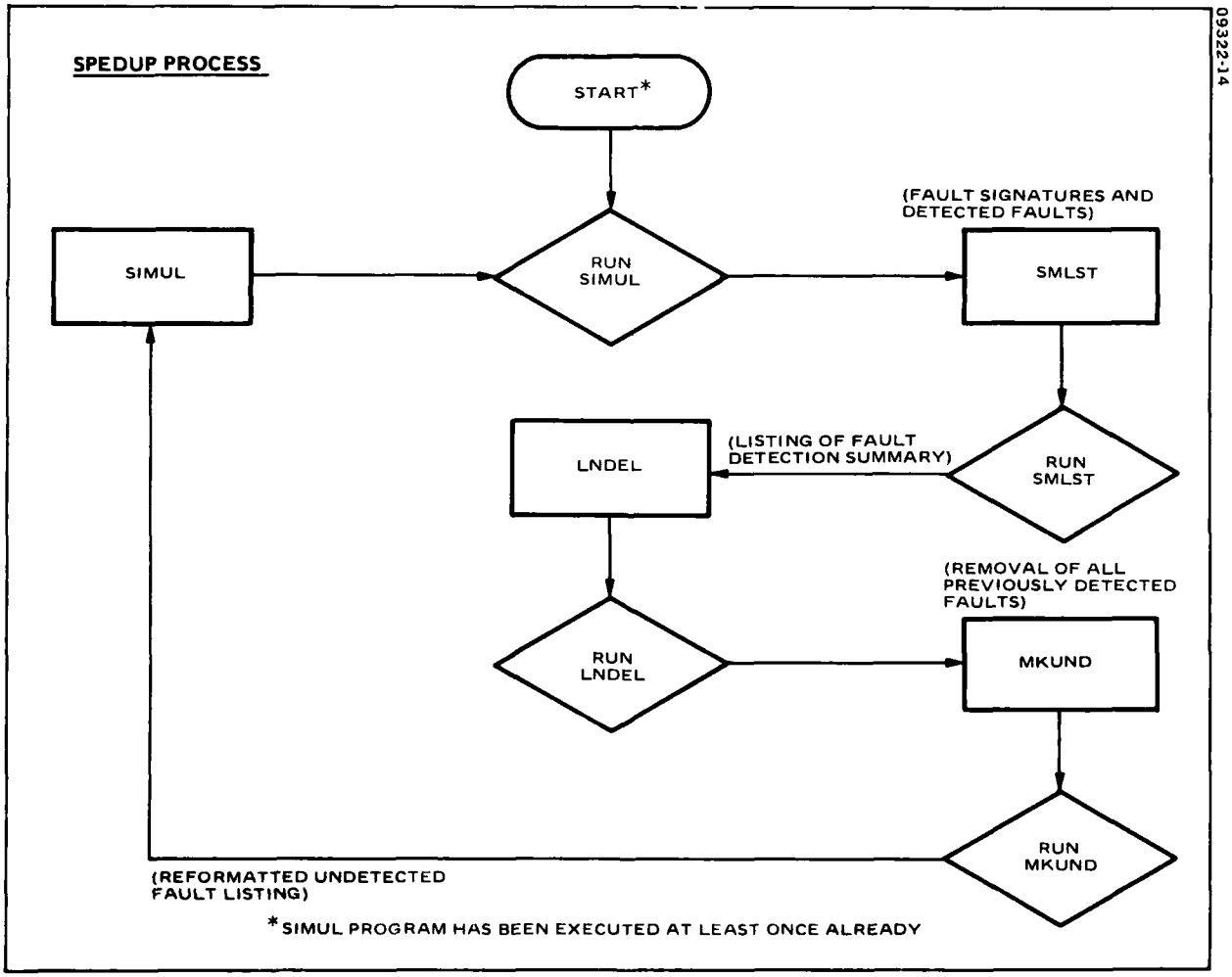
After executing the SIMUL program for the first time and before the next run is made, SMLST should be run, routing its output listing to a disc file of the user's choice. This file is then used as input to the program LNDEL, which deletes lines in the file not containing detected faults, and writes these detected fault lines on to cartridge tapes. The user then copies these tapes into another disc file and deletes the original SMLST file. The program MKUND is executed with this new disc file as its input, reformatting the faults into a form acceptable to SIMUL so it can remove them as previously detected faults. The MKUND program writes its output to the cartridge tape, which the user copies to disc and uses as input for the next SIMUL run. This procedure can be repeated as often as necessary.

The SPEDUP process, although used for simulating the 1646178 D/PCB, can be used whenever there is a requirement for multiple SIMUL runs on a digital printed circuit board.

Run times on three different 1646178 D/PCB simulation runs were recorded, and appear in the facing table. The results showed that the average run time was reduced almost a third when SPEDUP was used. Also, three more different simulation runs (cases 4 thru 6) were recorded to determine the amount of disc storage space saved by using SPEDUP. As shown in the table, over half of the disc storage space was saved after SPEDUP was executed.

SPEDUP IMPROVEMENT DATA

	Case	Before SPEDUP (Hrs)	After SPEDUP (Hrs)
SIMUL Run Time or Simulation Time	1	151	59
	2	45	14
	3	106	35
		Before SPEDUP (Blocks)	After SPEDUP (Blocks)
Disc Storage Required	4	897	433
	5	760	312
	6	450	211



SPEDUP Process Flow Diagram. The use of SPEDUP eliminates repeated detection of identical faults as new test simulations are run, and thus saves both computer run time and disc storage.

1. ROLE AND DESCRIPTION OF TEST ADAPTERS FOR THE CANDIDATE CIRCUIT BOARDS

The test adapters provide the electrical and mechanical interface required to test the two LSI-based printed circuit board candidates on the DTS-70.

Photographs of the 1635972 Test Adapter and the 1646178 Test Adapter are shown in Figures A and C. The development of these adapters, began with the mechanical interface to the DTS-70 provided by Hewlett-Packard with its HP91071A Test Adapter Kit. From this starter kit, additional electrical and mechanical features were added to fit the requirements of the two test candidates.

The electrical functions of the 1635972 Test Adapter are shown in Figure B.

(1) Input /Output Circuit – The input circuit provides the electrical connection between a DTS -70 driver and a 1635972 input pin. The output circuit provides the connection between a DTS-70 comparator and a 1635972 output pin. These types of connections are used for the address and control signals found on the 1635972 board.

(2) The Bidirectional Pin Circuit – The 1635972 board has 43 bidirectional data pins. To provide a bidirectional signal the DTS-70 must tie two of its pins, a driver and a comparator, together and connect them to the 1635972 bidirectional board pin, as shown in Figure B. The open collector buffer (7417) and the pullup resistor were added to isolate the DTS-70 driver from the 1635972 board driver. This prevents the DTS-70 driver from masking the operation of the 1635972 board driver.

(3) Adapter ROM Circuit – This ROM circuit is used to repetitively cycle the 8080 A/B microprocessor instructions and to toggle its eight data input and sixteen address output lines.

(4) Time Delay Circuit – This circuit delays the status strobe signal to the 8228 system controller for a duration long enough to allow information on the 8228 data lines settling time. Then the status strobe signal latches the STATUS information on its data bus.

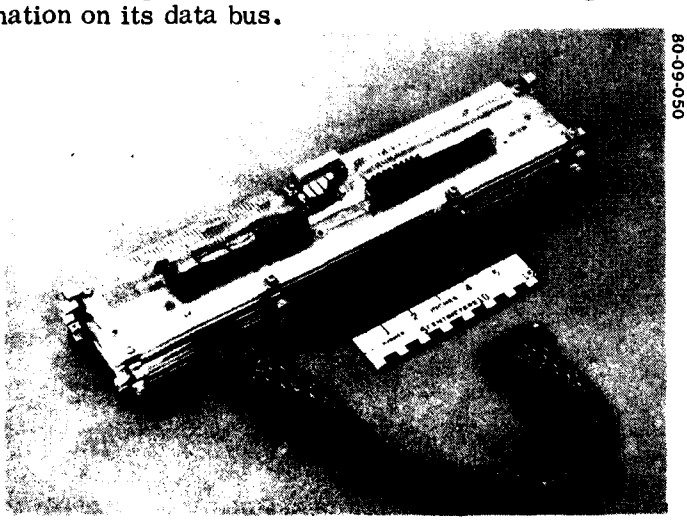


Figure A. 1635972 Test Adapter. An important feature of the 1635972 test adapter is a ROM circuit used to test the microprocessor through signature analysis.

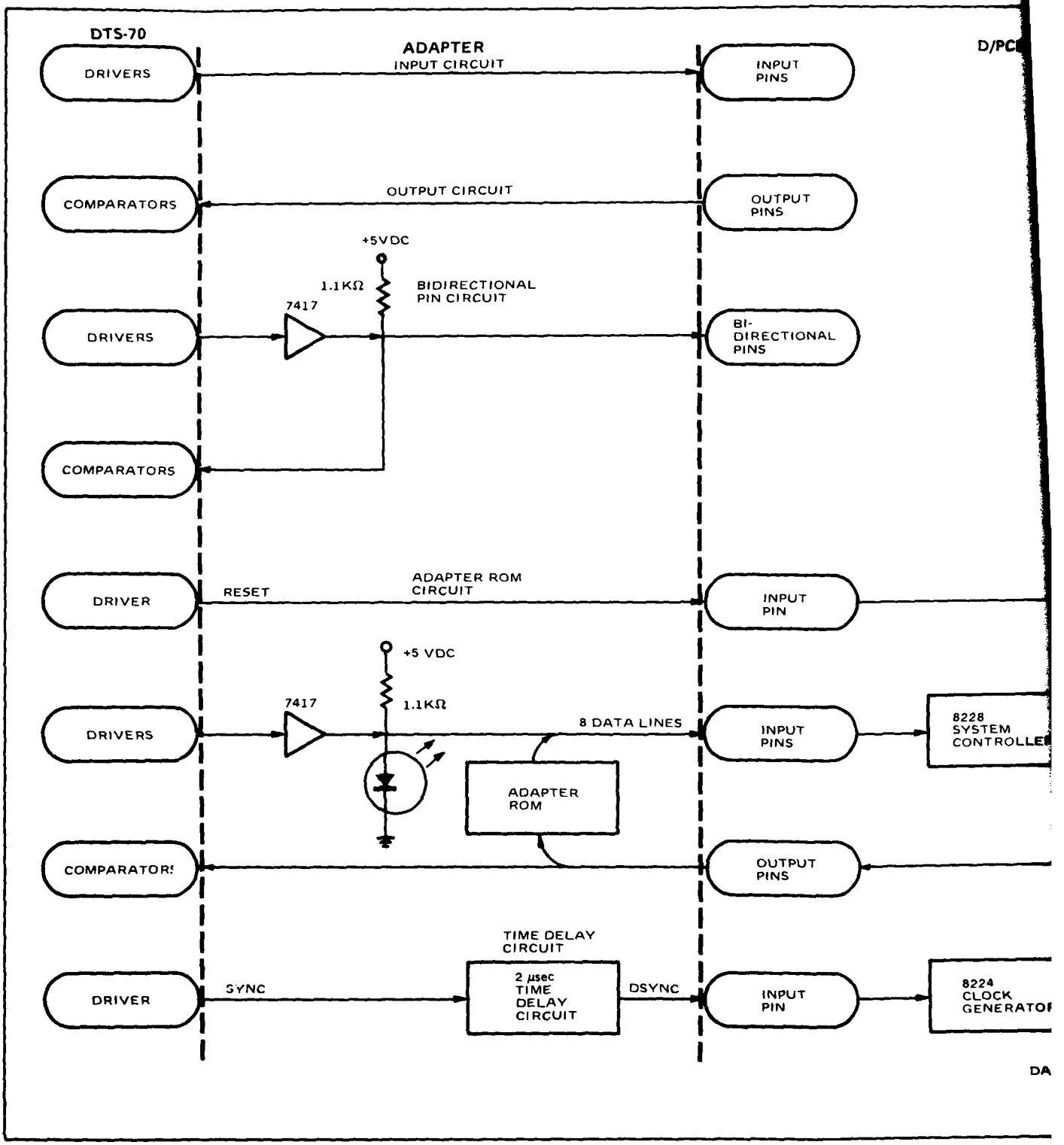
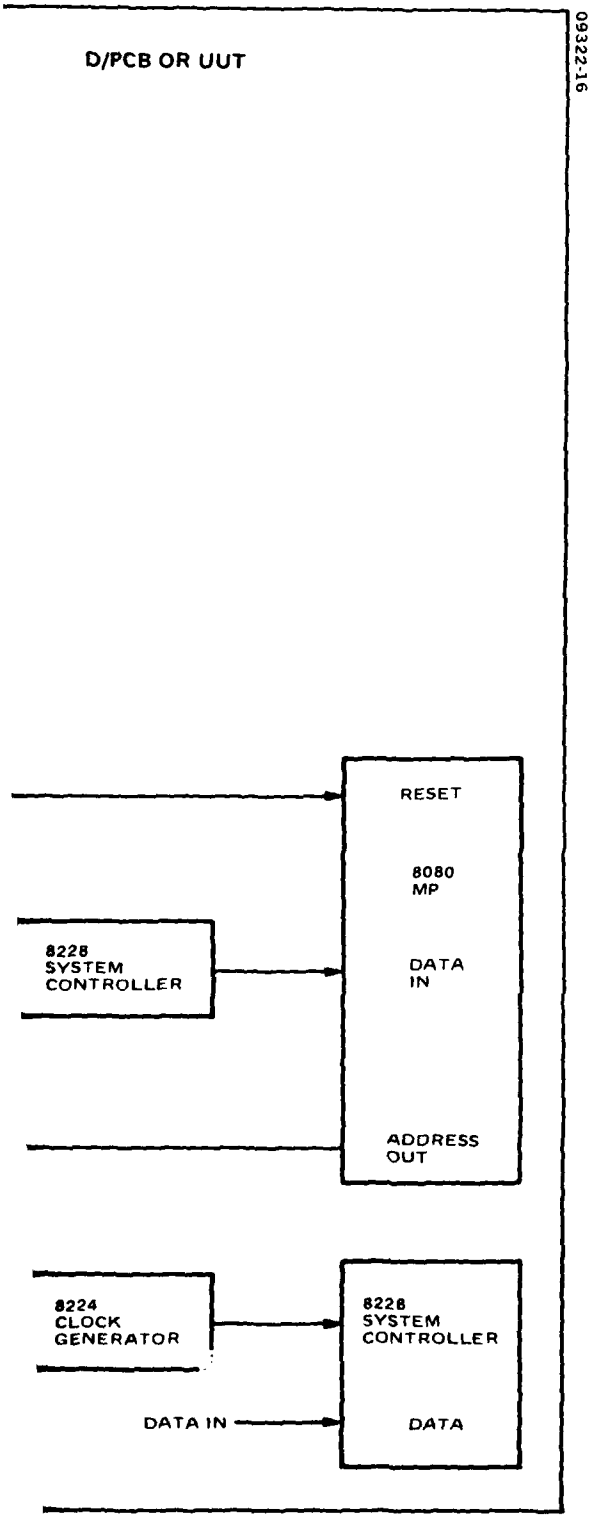


Figure B. 1635972 D/PCB Test Adapter Electrical Functional Block I
the test adapter, the -972 board is tested in two parts, using Signatur
microprocessor and conventional TESTAID/FASTRACE for the remair



nal Block Diagram. By interfacing through
g Signature Analysis for the 8080A/B
the remainder of the board.

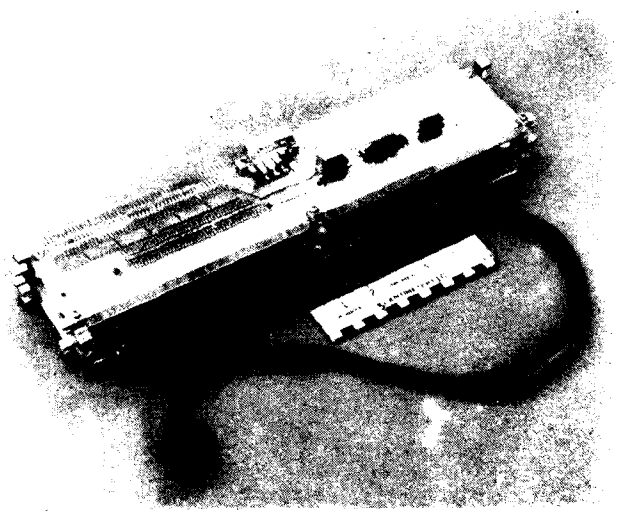
1. ROLE AND DESCRIPTION OF TEST ADAPTERS FOR THE CANDIDATE CIRCUIT BOARDS (Continued)

The 1646178 Test Adapter functional diagram is shown in Figure D.

(1) Input/Output Circuit – The input circuit provides the electrical connection between a DTS-70 driver and a 1646178 input pin. The output circuit provides the interface connection between a DTS-70 comparator and a 1646178 output pin.

(2) Bidirectional Pin Circuit – This circuit was required to produce valid logic levels on all bidirectional pins. The reason for this is that a logic probe cannot sense a passive node. The output of any disabled tri-state element found on all bidirectional pins is passive logic '1's, which means the outputs float to a value that the board hardware will interpret as a logic '1'. But because such a node state is passive, it cannot force a logic probe to a valid logic state and is flagged as a faulty node by the test system. The problem was solved by the addition of pullup resistors on all the bidirectional I/O pins. This produced an active logic '1' on the pins when the tri-state elements were disabled.

(3) Initialization Circuit – The initialization circuit initializes the 1646178 D/PCB before each test run. It accomplishes this by forcing the Divide-by-Four Network found on the 1646178 board to a known state. The initialization circuit is a clock that toggles signal $\overline{C}$16MC until $\overline{C}$LKM2 goes to zero. When CLKM2 goes low the initialization circuit is shut off and at this point the whole circuit is disabled by the DTS-70 control line.



80-09-052

Figure C. 1646178 Test Adapter. The 1646178 test adapter contains an initialization circuit needed to force the D/PCB into a known state so as to enable testing and pull-up resistors needed to detect disabled tri-state logic elements.

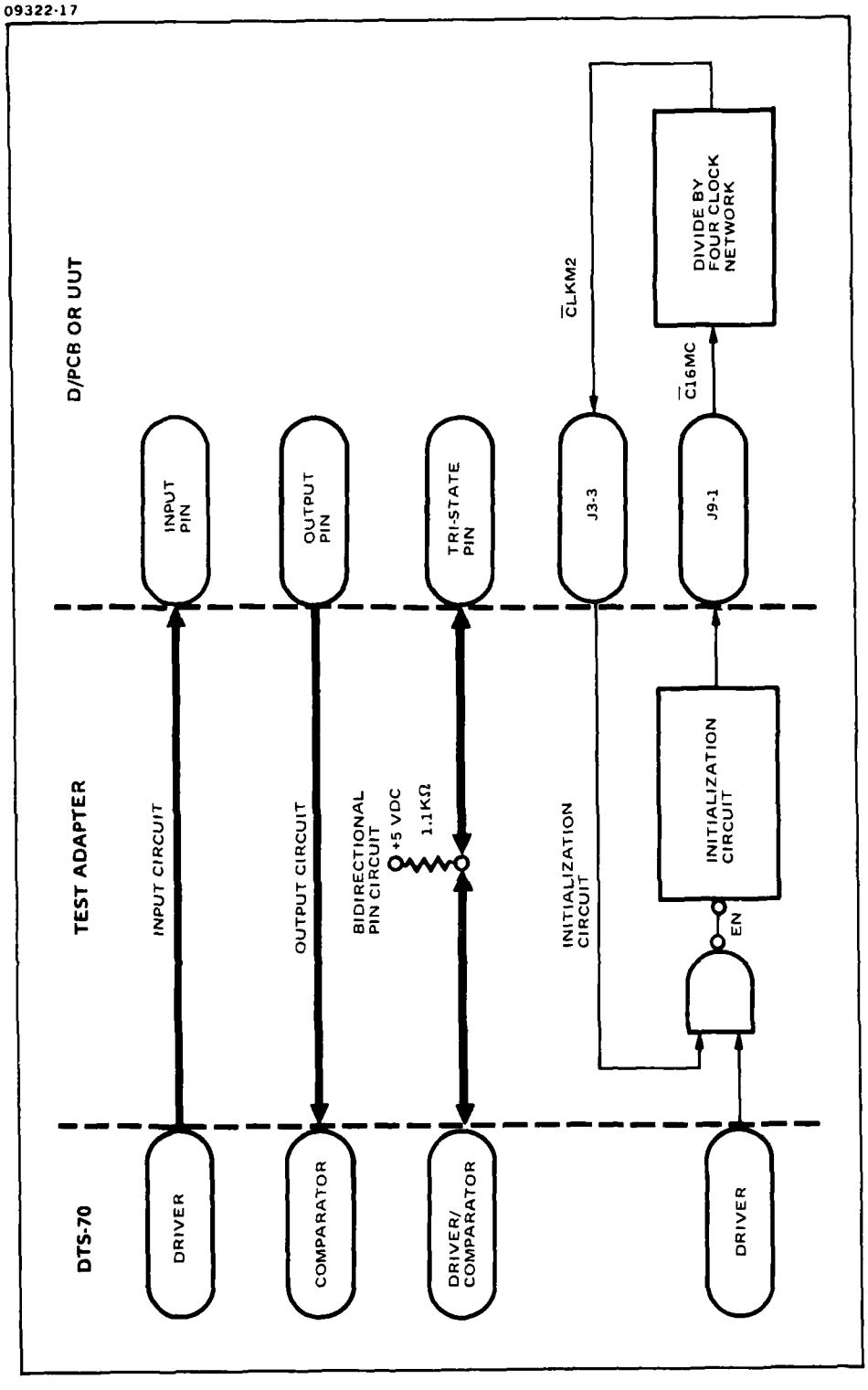


Figure D. 1646178 Test Adapter Electrical Functional Block Diagram. Enabling the initialization of testing, and the testing of bidirectional pins required the construction of special test adapter circuit.

1. PN-1635972 CIRCUIT BOARD FINDINGS AND RESULTS

The development of the -972 test program required 46.1 man-weeks (with learn factor) and resulted in a fault isolation time for any fault of between 0.2 minutes and 5.9 minutes. During the test program development phase four major difficulties were encountered and resolved successfully.

The manpower distribution for the TESTAID/FASTRACE and SIGNATURE ANALYSIS programming development is shown in Tables I and II respectively. The left hand column of both tables contains itemized job names and the right hand side shows the detailed breakdown of work.

In Table I, the hardware/software verification column provides the process time needed for accommodating the test program to the -972 board functions. This verification process required many iterations of corrections for both software (i.e. circuit topology, test patterns, resimulation) and hardware (i.e., test adapter). The total time devoted to TESTAID/FASTRACE test programming is 1344 hours (33.6 weeks) and to SIGNATURE ANALYSIS is 500 hours (12.5 weeks). The total -972 board test program generation time was 46.1 weeks (with learn factor).

Fault isolation performance data are shown in Table III. This table shows the length of time needed to isolate the different faults. Three different types of faults, stuck at zero (SA0), stuck at one (SA1) and Solder Bridge (SB), are inserted manually at the indicated IC pins on the -972 board and the fault isolation time measured. The time required to isolate SA0 faults is between 0.2 minutes and 5.9 minutes. For SA1 faults, isolation time is between 0.2 minutes and 3.1 minutes, and for SBs it is between 0.4 minutes and 3.6 minutes.

The GO/NO-GO test performance data for the 972 board is shown in Table IV. The testing of the 972 board involves, first, a complete logic circuit test without 8080 microprocessor using TESTAID/FASTRACE, and second, the 8080 microprocessor test using the SIGNATURE ANALYSIS method. As seen in the table, the time required for testing the 972 board without the microprocessor is 0.3 minutes, and 8080 microprocessor test itself takes 8.0 minutes. The total time required for the -972 board GO/NO-GO test is 8.3 minutes. However, the GO/NO-GO time for the 8080 microprocessor test can be improved by using multiplexing techniques rather than manual probing of its 40 pins.

During the hardware verification phase of the program, the following problems were encountered and satisfactorily resolved.

The first problem involved the -972 board power supplies, which default to their maximum voltage whenever a test programmer enters a wrong command sequence. SETUP, CHECK and PONOF are subprograms of the FASTRACE software package in the DTS-70 system. The system power turn on procedure requires that the SETUP and CHECK programs be executed in series prior to the PONOF program, which turns on the system power. When the PONOF program is executed alone, the power supplies selected by the SETUP program default to the maximum voltages causing component failure on the -972 board. In most cases, the damaged components are ROMs, the Clock Generator, and the Microprocessor.

Power supply default problems were encountered in other cases also. When the preliminary test file Logical Unit (LU) number in the SETUP run string is different from the PATDK preliminary test file LU number, then power supply defaulting occurs. For example, if a test programmer enters the following PATDK and SETUP run strings on the terminal:

```
:RU, PATDK, TASF, 1, &PA972, *TFI, FIF::-18
:RU, SETUP, FIF::-17, 1, &SETUP,
```

TABLE I. MANPOWER DISTRIBUTION FOR TESTAID/FASTRACE TEST PROGRAM

						Time-Hours	
Items	Design	Topology Editing	SGLIST	SMSET	Simul	Hdwr/Sfwr Verification	Total
LSIS, ROMs, RAMs	200	88	56	40	200	200	784
1635972 Board	0	40	80	40	120	280	560
Total	200	128	136	80	320	480	1344

TABLE II. MANPOWER DISTRIBUTION FOR SIGNATURE ANALYSIS TEST PROGRAM

					Time-Hours	
Items	Concept	Algorithm	Coding	Edit	Debug	Total
FORTRAN	48	148	88	64	88	436
Adapter ROM	16	16	8	8	16	64
Total	64	164	96	72	104	500

TABLE III. FAULT ISOLATION PERFORMANCE

Fault Type	Probe Time	Fault Type	Probe Time	Fault Type	Probe Time
SA0	Minutes	SA1	Minutes	Solder Bridge	Minutes
U31.13	0.8	U31.13	3.1	U31(5,6)	0.4
U31.5	0.5	U31.5	2.1	U31(9,10)	3.6
U31.9	5.9	U31.9	2.4	U18(4,5)	0.8
U18.12	1.2	U28.13	1.3	U48(3,6)	0.4
U28.1	2.5	U47.19	1.3	U47(1,2)	0.5
U46.2	0.2	U48.13	0.2	U47(14,15)	0.9
SA0	Minutes	SA1	Minutes	Solder Bridge	Minutes
Min	0.2	Min	0.2	Min	0.4
Mean	1.2	Mean	1.7	Mean	1.1
Max	5.9	Max	3.1	Max	3.6

TABLE IV. GO/NO-GO TEST PERFORMANCE

D/PCB = TESTAID/FASTRACE	0.3 Minutes
Signature Analysis – μP (Manual Probing)	8.0 Minutes
Total GO/NO-GO Test Time	8.3 Minutes

1. PN-1635972 CIRCUIT BOARD FINDINGS AND RESULTS (Continued)

where

FIF::-18 is the preliminary test file name created by PATDK in LU 18

and

FIF::-17 is the preliminary test file name in LU17,

then the power supplies will be defaulted, since the LU number of the SETUP Test File name is 17 instead of 18.

To prevent Power supply default problems, the following conditional command strings are entered just after the SETUP and CHECK run string:

```
:IF, 1P,EQ,0,2
:RU, OPGET,,CORRECT SETUP AND CHECK AND TRY AGAIN
```

These conditional commands check the LU numbers of the preliminary test file between PATDK, SETUP, and CHECK programs. If they are different, then the program halts and displays a "CORRECT SETUP AND CHECK, AND TRY AGAIN <ENTER CARRIAGE RETURN>" message to alert the test programmer for corrections.

The second problem involved testing a bi-directional data bus driver for the -972 board. During the hardware verification phase, it was discovered that the bi-directional driver output attained a logic low (less than 0.8v) during tri-state condition. However, a logic high (greater than 2.4v) was expected, since the bi-directional bus driver (8216) circuit is modeled such that the output goes to a logic high during the tri-state condition. To resolve this problem, pull up resistors (1.1K ohm) are provided on the test adapter.

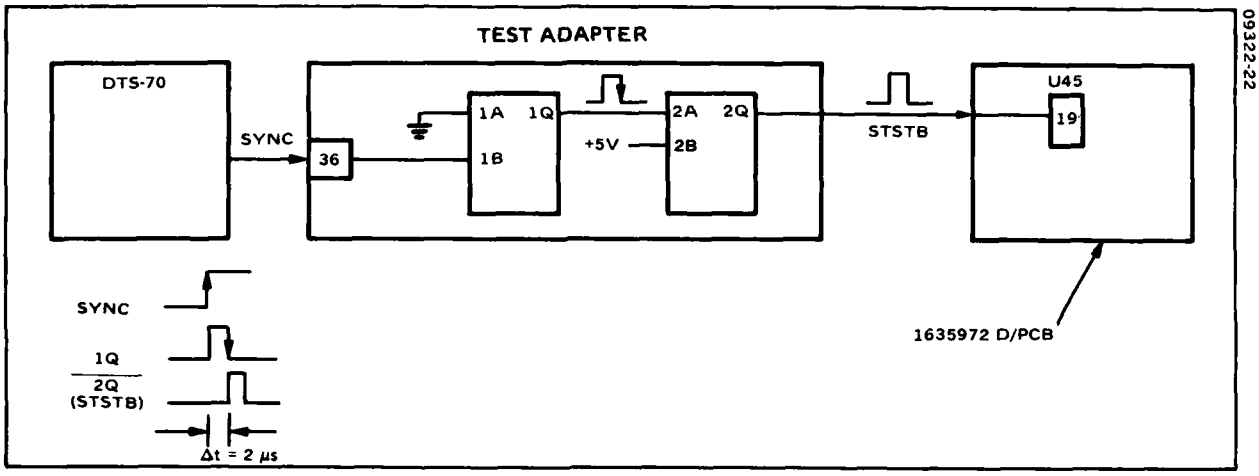
Another problem related to the bi-directional data bus involved the overload of the DTS-70 driver during a logic HIGH state. For instance, when the -972 board bi-directional driver outputs a logic LOW state, the DTS-70 comparator monitors an intermediate level 1.2v during the first 12 seconds; the voltage then shifts to logic LOW. This problem was resolved by adding an open collector buffer (7417) at the output of the DTS-70 driver. This buffer can reduce the output current of the DTS-70 when it is in logic HIGH state, thereby eliminating the sinking current problem. Test requirements for the -972 board driver were thus satisfied and the interaction problems resolved.

The third problem involved tri-state logic definition between two bi-directional bus drivers inside the board (for example, between pins U14 and U15, or U13 and U15 on the 972 board). As mentioned earlier, the tri-state output was modeled as a logic 1, but in the actual board, the voltage was about 0.5v or logic LOW. If the bi-directional bus driver had been connected to the external connector pins, then adding a pull up resistor at the test adapter would have resolved the problem. But this was not the case. The problem was resolved by remodeling U9, U10, U13 and U14, all of which are 8216 bi-directional bus drivers. This forced a "don't care" state during the tri-state mode (see Appendix B.2 for schematics).

The fourth problem involved a timing delay between the data bus and the status strobe signal for the system controller logic circuit. The 8228 system controller requires a delayed (8n sec min) status strobe pulse to latch the 8 bit status data into the status register. Unfortunately, the DTS-70 does not have the capability to provide a time delay for individual signals with respect to

other data signals. This problem was resolved by adding a time delay circuit (74123) in the test adapter. The time delay circuit (see the figure below) operates in the following manner:

The SYNC signal along with the other 8 data signals are initiated by the DTS-70 simultaneously. The positive edge of the SYNC signal triggers a one-shot "A" signal which has a "RC" time constant of 2 μs. Since the one-shot "A" output is connected to the inverted input of the other one shot circuit, the negative edge of the one-shot "A" output triggers a one-shot "B" output. As a result, the SYNC signal creates a single 2 μs pulse with a 2 μs delay from the positive edge of the SYNC signal. This delayed 2 μs pulse satisfies the 8228 status strobe requirement.



Time Delay Circuit. The time delay circuit provides a time delayed strobe pulse to the 8228 system controller.

2. PN-1646178 CIRCUIT BOARD FINDINGS AND RESULTS

With the successful completion of any project, the results and the process of getting to those results are an important output. For the DFI Project, these outputs are the fault isolation performance data, the D/PCB programming summary, and the test verification process.

The final test results for the 1646178 D/PCB can be seen in Tables I and II. Table I, the 1646178 D/PCB Programming Summary, shows the total programming effort in manhours required for the 1646178 D/PCB. Table II is the Fault Isolation Performance Data taken during test verification. It shows the length of time it took to isolate manually induced faults (SA0, SA1, and solder bridges) on the 1646178 board.

Test verification is the process of merging the test software to the board hardware operations. This merging process required many iterations of corrections to the software/hardware and many retests. The following is a complete account of the problems encountered and how they were resolved during the test verification stage of this project.

The first major problem in test verification was errors found on the 1646178 board schematic. These schematic errors had to be corrected in the software topology so that the physical hardware and the software model of the 1646178 D/PCB would match. At first glance, this type of problem would seem easily corrected. But, since any changes to the software topology require over 350 hours to resimulate the complete test, the problem of topology errors on the 1646178 board is not trival.

Another hardware related problem resulted in the Initialization Circuit modification made to the 1646178 test adapter. This adapter modification was required to initialize the 1646178 D/PCB which was not possible using software techniques. Initialization Circuit operation details can be found in Topic 2.E.1.

During fault isolation, it was discovered that the AM2901 RAM and Q-Register tri-state shift lines were not floating to a logic '1' when in the high-impedance state. Instead, the shift lines were sitting at a passive logic '0'. Because the nodes were passive, they could not force the FASTRACE Probe to a valid logic state and were always flagged as faulty nodes. To eliminate this problem without having to resimulate the entire 1646178 D/PCB test, the RAM and Q-Register shift lines were marked inaccessible to the FASTRACE Probe. This marking technique, made in preparation for the Industry Demonstration, was only a temporary solution to the problem. It compromises the total board test comprehensiveness by 1.6%.

TABLE I. 1646178 D/PCB PROGRAMMING SUMMARY

Items	Design	Topology Editing	SGLST	SMSET	SIMUL	Hardware Verification	Total Hours
AM2901	80 hrs	120 hrs	8 hrs	4 hrs	40 hrs	24 hrs	276 hrs
ROMS	8 hrs	16 hrs	8 hrs	4 hrs	8 hrs	8 hrs	52 hrs
Complete 1646178 PCB	0 hrs	80 hrs	40 hrs	8 hrs	600 hrs	80 hrs	808 hrs
Total	88 hrs	216 hrs	56 hrs	16 hrs	648 hrs	112 hrs	1136 hrs

Gross Time = 28.4 weeks (with learn factor)

Fault Type SA0	Probe Time Minutes
U101.1	1.45
U101.4	0.5
U101.9	0.75
U101.13	0.2
U101.14	0.2
U103.2	1.5
U103.15	2.0
U812.9	1.75
U204.1	1.84
U204.2	1.0
U204.5	1.25
U204.9	1.84
U204.13	11.84
U304.11	1.16
U104.1	1.84
U104.6	10.0
U1205.1	2.0
U1205.2	2.22
U1205.13	2.22
U306.1	1.65
U306.2	9.43
U306.6	1.5
U306.15	1.7
U107.9	1.92
U107.14	8.84
U205.1	1.15
U205.15	1.15
U305.4	0.68
U105.1	0.8
U106.6	0.67
U1207.3	1.0
U710.10	3.3
U110.13	2.55
U110.14	2.55
U607.3	2.88
U607.12	1.22

Fault Type SA0	Probe Time Minutes
U908.6	1.93
U908.15	0.6
U907.3	8.0
U907.4	0.93
U907.9	8.85
U907.12	8.85
U1007.3	0.73
U1007.11	3.33
U1010.1	0.63
U1010.5	0.62
U1010.6	6.05
U190.15	1.63
U1006.7	3.84
U906.2	3.84
U906.13	2.13
U911.1	1.84
U911.4	10.1
U911.5	2.25
U911.6	1.72
U911.9	0.65
U911.10	1.27
U911.12	1.93
U409.1	3.16
U409.5	0.62
U509.10	1.84
U807.8	4.63
U814.10	3.27
U1103.1	2.77
U514.6	4.43
U514.11	2.43
U514.14	2.88
U403.5	9.43
U403.12	1.05
U607.1	1.23
U607.2	2.24
U607.4	1.95

Fault Type SA0	Prob Mi
U607.11	1.
U1211.10	2.
U111.3	8.
U111.12	0.
U111.13	0.
U207.7	1.
U207.9	0.
U108.7	0.
U108.11	2.
U307.9	0.
U208.4	0.
U208.6	1.
U308.12	0.
U410.1	3.
U410.2	0.
U410.3	0.
U410.4	0.
U410.10	0.
U410.11	1.
U410.14	3.
U603.4	5.
U603.12	6.
U604.9	5.
U601.1	4.
U601.6	5.
U701.2	3.
U702.14	3.
U704.5	4.
U704.6	2.
U805.1	0.
U401.1	0.
U401.2	2.
U401.4	2.
U401.6	2.
U401.10	2.
U401.12	2.
U401.14	2.

TABLE II. FAULT ISOLATION PERFORMANCE DATA

be Time inutes
1.32
2.55
8.22
0.75
0.50
1.0
0.92
0.76
2.04
0.51
0.63
1.97
0.51
3.63
0.73
0.63
0.82
0.83
1.86
3.55
5.00
6.47
5.15
4.21
5.76
3.22
3.94
4.62
2.1
0.92
0.67
.5
.0
.0
.08
.01
.05

Fault Type SA0	Probe Time Minutes
U505.2	1.80
U505.4	4.92
U505.6	1.92
U505.10	2.27
U505.12	1.92
U505.14	1.92
U501.2	1.27
U501.4	1.27
U501.6	2.0
U501.10	1.51
U402.2	3.17
U402.4	2.08
U402.6	3.00
U402.10	1.95
U504.1	4.47
U504.12	1.75
U502.2	1.87
U502.10	1.62
U407.1	1.05
U407.2	0.53
U407.3	0.73
U407.5	0.5
U407.6	0.83
U407.7	0.83
U407.9	0.28
U407.10	0.43
U407.12	0.48
U407.15	0.43
U507.2	0.48
U507.4	0.68
U507.15	0.43
U510.2	2.07
U510.10	1.7
U406.1	1.45
U406.11	0.65
U904.5	0.67
U904.6	1.63

Fault Type SA0	Probe Time Minutes
U904.11	0.33
U904.12	1.78
U904.14	1.10
U905.4	1.0
U905.9	0.62
U905.14	0.9
U902.9	1.35
U803.8	0.3
U803.9	0.5
U201.3	1.87
U201.4	0.4
U201.6	0.45
U201.13	0.4
U202.6	0.45
U202.13	0.48
U303.1	2.13
U303.5	0.4
U302.13	1.72

Fault Type SA1	Probe Time Minutes
U1001.4	4.16
U1006.15	4.00
U214.29	0.65
U906.6	2.50
U410.1	0.34
U207.14	1.25
U1001.4	4.16
U1001.1	0.66
U207.1	0.83
U308.15	1.00
U307.15	1.00
U1007.7	1.83
U1007.10	2.67
U906.10	8.5
U906.12	8.51
U907.10	7.16
U1006.9	1.87
U1006.10	1.80
U909.2	1.73
U201.11	2.90

GO/NO-GO TEST TIME	1.5 MINUTES

›be Time inutes
.16
.00
.65
.50
.34
.25
.16
.66
.83
.00
.00
.83
.67
.5
.51
.16
.87
.80
.73
.90

Fault Type Solder Bridge	Probe Time Minutes
U204(4,5)	0.55
U104(9,10)	7.07
U201(4,5)	1.50
U1210(8,10)	1.34
U214(2,3)	2.08
U604(6,7)	6.92

1. USE OF THE IMAGE/1000 SYSTEM FOR SUPPORT MAINTENANCE REPORTS

In order to provide readily available support maintenance data on the DFI Test System and its performance, Hughes developed an application of HP's IMAGE/1000 Data Base Management Program called DFISML. This will provide the necessary maintenance and support cost data.

Support Facilities – During the DFI program ATE implementation, the Support Facilities output required by MICOM sought to establish the operating support cost data (SCD) of the DTS-70 system hardware and software. To meet the SCD objectives by computerized methods, the system was supplied with IMAGE/1000 software. This decision provided a ready and cost effective solution to the requirements SCD and additional varied capability for other data base management (DBM) operations such as:

- Manufacturing inventory
- D/PCB test records, reports
- Test failure trend analysis
- Production, field reports

IMAGE/1000 software is designed to operate with the test system HP 1000/40 general purpose computer.

Applying IMAGE/1000 – To apply IMAGE/1000 a format must first be defined to create the required system Support and Maintenance (SM) Log records or data base (DB) structure. The format in IMAGE is known as a SCHEMA, and it is this SCHEMA that IMAGE/1000 uses as its DB defining algorithm.

IMAGE/1000 is interactive and operates through specified commands, with alphanumeric character strings. It can also perform a simple arithmetic average or algebraic addition, check syntax, and provide operator error messages and remedial reference aids. For data base flexibility IMAGE can use automatic masters, manual masters, keys, and indexes in the DB structure and software operations.

To provide system support and maintenance (SM) records an application program was written to operate through IMAGE/1000 and QUERY, an IMAGE subprogram. This program is identified by DFI SML and resides in the system fixed disc on LU19.

The DFI SML Data Base – This consists of a SCHEMA which defines all data base items and files as shown in the figure opposite. A copy of the SCHEMA program is included in Appendix A.5.1 for reference. The DB structure is indexed by two key items – one for part number (PART) and the other for service data or DATEF. PART and DATEF operate as automatic master files and are linked directly to the detail data file (SMFILE). Each record in the DB is broken down into the elements or quantities shown directly below the SMFILE. To indicate the type of system maintenance service performed, Support Activity or SACTV is further subdivided into the generic name of an activity and a verb representing the action, for example: "Printer Installed." Auxiliary FORTRAN software is also required to supply a time quantity as ELTIME.

QUERY – Command procedure files, operating within the system QUERY are used to enter new data or update the DB record. Alternately an operator, having proper security level to access the DB, can interactively perform those operations. In addition to its DB update function, QUERY also executes a 30 step application program SMRPT which was written to print the support maintenance report. A reference copy of the SMRPT program is included in Appendix A.5.2. The SM report print-out, the objective of the SMRPT program, with a sample record, is shown in the facing table. After being entered in the DFISML

data base, any hardware or software item requiring SM action would be printed in the report on request.

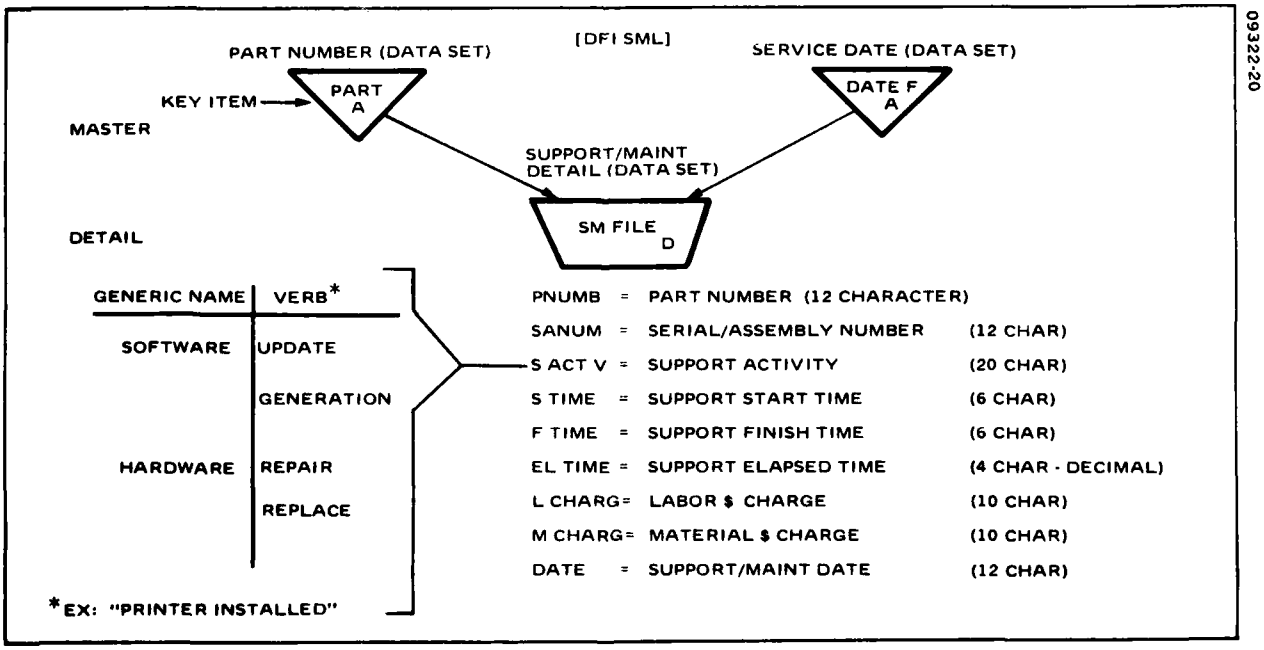
Although the DFISML application software is complete in form, the D/PCB candidate test software priority and the industry Demonstration did not permit sufficient time to verify the programs or to provide a report printout. To establish the true system support cost data would require continual system operation over a much longer period of time than was afforded during the ATE implementation period.

Because of the system's excellent reliability, the only items requiring maintenance action in over 2500 hours operation were a 94151A Programmable Driver Comparator card, and a TESTAID – Fault Isolation Probe. Both items were serviced so that system operation was interrupted no more than 2.5 hours. A spare 94151A card was also ordered for the system.

The two maintenance actions in 2500 hours operation are highly favorable, but are not sufficient to establish system support cost. Continued system operation and application of the DIF SML data base can, over a period of time, provide the Support Cost data.

DFI SUPPORT MAINTENANCE REPORT – DTS-70 SYSTEM

Part Number	Serial/ Assembly Number	Support Activity	Support Time Hr	Labor $	Material $	Date
HP94151A		Replace driver/ comparator card		90.00	1,150.00	8-15-80



DFI DTS-70 Support Maintenance SCHEMA. The IMAGE/1000 software uses this SCHEMA to produce the maintenance support cost data reports which will provide a hardcopy system upkeep record.

1. DTS-70 INDUSTRY DEMONSTRATION

The purpose of the Industry Demonstration was to show DoD and Industry that the DFI Test System has met its primary program objectives, that is, to test and fault isolate complex microprocessor or LSI based digital printed circuit boards. According to comments made by those who attended the demonstration, it did so.

The Industry Demonstration showed that the DTS-70 test system, as implemented by Hughes, met all test system criteria and fulfilled the DoD's 90% test comprehensiveness requirements.

In many ways, the demonstration was beneficial to all who attended the conference, especially to those (both DoD and Industry) who already possessed a DTS-70 Test System. Improvements similar to those made to the DFI System by Hughes, can be incorporated in their systems. Secondly, Hughes' analysis of the problems associated with D/PCB testing, and their solutions, were of benefit to those who are considering a digital PCB Test System in their own manufacturing test facilities. Finally, the results of this program were also beneficial within Hughes.

The Demonstration created an atmosphere of learning for people having problems testing microprocessor or LSI based D/PCBs in a production environment. The testing objectives were common among the invited guests and Hughes solution of D/PCB test problems presented them with a method for meeting test objectives. An exchange of information and ideas on manufacturing methods and technology was also accomplished during the three separate conferences.

From over 100 invitations, 45 guests attended the Industry Demonstration at Hughes Aircraft Co. Those industry groups represented are identifed in the facing table.

GROUPS ATTENDING THE HUGHES INDUSTRY DEMONSTRATION

Group Name/Location(s)	Group Name/Location(s)
ATE Associates Northridge, CA	Northrop Electro-Mechanical Division Anaheim, CA
Ford-Aerospace & Commercial Corp. Newport Beach, CA	NUWES Keyport, WA
General Dynamics Pomona, CA	RCA ATE Systems Division Burlington, MA
General Electric Co. Syracuse, NY	Teledyne Systems Northridge, CA
Hewlett-Packard Fullerton, CA	Texas Instruments Co. Dallas, TX
Hughes Aircraft O. Canoga Park, CA El Segundo, CA Fullerton, CA Irvine, CA Tucson, AZ	TRW Systems Redondo Beach, CA
IBM Corporation Owego, NW	U.S. Army Missile Command Redstone Arsenal, AL
Lockheed Missile & Space Co. Sunnyvale, CA	Vought Corp. Dallas, TX
Magnavox Fort Wayne, IN	
McDonnell Douglas Huntington Beach, CA	
Naval Avionics Center Indianapolis, IN	

SECTION 3
RECOMMENDATIONS

Section 3 – Recommendations

1. USER AUGMENTATION OF THE DTS-70 SYSTEM

The DTS-70 system was purchased with certain enhancement features which complement the systems' fault isolation capabilities. With the completion of the DFI project, the experience gained has led to additional recommendations for system enhancement features.

During the test development stage, the DTS-70 was observed to have a number of shortcomings which inconvenienced the user. If the DTS-70 system were to be purchased today, it would be acquired with the same enhancement features purchased for the DFI project plus the following additional features:

(1) Power Fail Interrupt Package – HP provides a power fail recovery system which protects memory should there be a fluctuation or failure in the system AC power line. There were a few cases during the course of this project in which software simulations over 20 hours long were lost due to power line fluctuations.

(2) 2nd Disc Drive – The addition of another disc drive to the system would facilitate the programming effort. With three users on the system for this project, the disc working area shrank to the point where much of the information had to be stored on cassettes in order to make room for the other users. This wasted valuable time that could have been better spent on the board testing effort. The second disc drive would also make the software backup procedure faster. Software backup was performed on a weekly basis to protect the programming software from being completely lost should a disc crash occur. With the second disc drive, backup could be done more frequently thereby reducing the amount of information lost should there ever be a disc failure.

(3) Utility Outlet – A 120V, 60Hz outlet mounted on the front of the DTS-70 for powering the auxiliary equipment used with the system would be very convenient to the user.

With the addition of these features, the test development stage could have been greatly expedited.

2. POTENTIAL CIRCUIT BOARD IMPROVEMENTS TO ENHANCE TESTABILITY

Unless designers devote sufficient consideration to the testability of their product, many hours may be wasted at the testing stage resolving a problem that would have taken seconds in the initial design. Design practices must be upgraded to adequately incorporate testability.

Considering the fact that each D/PCB must be tested at some point in production before it reaches its destination in the field, it seems logical that the design effort should be conducted with testability in mind. An example of not designing for testability was encountered during the DFI implementation phase when test engineers had to overcome many testability hurdles in the two candidate D/PCBs. Based on problems encountered in this project, several general recommendations for D/PCB design improvements which would greatly facilitate the development of tests for any PCB are presented in the following paragraphs. Specific change recommendations to the test candidates can be found in the facing table.

One of the most difficult tasks for the test engineer is the initialization of the D/PCB. In many cases the initialization can be accomplished with a few extra test patterns added to the beginning of the test sequence to bring the board to a known state. But in some cases, the D/PCB can never be initialized using conventional software techniques, and requires special hardware modifications to be initialized. This time and effort could be completely eliminated if more attention were focused on the D/PCB's initialization at the design development stage.

Another recommendation for the design of digital PCBs is the use of sockets with all microprocessors and ROMs. The use of sockets for microprocessors and ROMs would widen the scope of possible test strategies for any PCB and therefore improve the PCBs' overall testability.

Feedback loops are another source of problems for the test engineer. When such loops exist it is difficult to locate a fault's origin within the feedback loop. If special logic were added to externally break these loops, a fault could be isolated down to a single node without the use of additional equipment (i.e., GR 2220-Fault-Probe.)

The final recommendation involves putting pullup resistors on all tri-state nodes because a logic probe cannot sense a passive node. The output of a disabled tri-state element is a passive logic '1', which means the output floats to a value that the board hardware will interpret as a logic '1'. Because such a node is passive, it cannot force a logic probe to a valid logic state and is flagged as a faulty node when it is tested. In the case of the DTS-70, tri-state elements could not be handled without the addition of pullup resistors unless special modifications were made to the tri-state models from the HP library.

SPECIFIC DESIGN IMPROVEMENTS RECOMMENDATIONS
FOR TEST CANDIDATE D/PCBs

Ckt Brd Part No.	Recommended Change	Benefit of Change
1646178	U1214 pin 14 & 15 tied to external input pin.	Enables complete board initialization without hardware adapter modifications (initialization circuit).
	Pullup resistors on all tri-state element outputs.	Pullup resistors had to be placed on adapter in order to test the board. Special complications resulted when the tri-states were not accessible to edge connector pins. This required modeling the unknown "X" state which was not available in the device model library.
	Special logic to the divide-by-four counter which disables feedback and passes external data.	This would eliminate feedback in the divide-by-four network and allow fault isolation to the node level.
	Logic to disable feedback throughout FLG REG circuit.	Allows fault isolation to the node level.
1635972	Provide an external pin to connect U28 pin 13.	Can control CHIP-SELECT of ROM (U28).
	Provide an external pin to connect U28 pin 10.	Enables ROM testing in IC level test, also controls CHIP-SELECT of U14 & U15.
	Provide a Test point at U35 pin 1.	Provides CLOCK input to the SIGNATURE ANALYZER.
	Install socket at U45.	Enables the use of DTS-70 8080 A/B simulation through umbilical cable.
	Install sockets at U2, U28, U31.	Permits a ROM substitution if test program requires a ROM modification.

3. RECOMMENDATIONS FOR FURTHER MM&T STUDY

The objective of the Hybrid Test and Fault Isolation program is to improve the manufacturing technology for test and fault isolation of complex digital hybrid modules. To improve the signature analysis technique and to improve digital hybrid testing on the DFI system, the following recommendations should be considered.

There are two recommended methods for improving the manufacturing technology for test and fault isolation. They are:

- Improve on the signature analysis technique.
- Improve the digital hybrid testing on the DFI System.

Improving the Signature Analysis Technique – The present method of signature analysis requires the test system operator to probe each microprocessor pin under the direction of the system computer. This method can account for an increased total test time as demonstrated on the 1635972 D/PCB.

The recommended method calls for a 40-pin clip and adapter cable to interface the microprocessor. A 40-pin multiplexer in the test adapter will then monitor the microprocessor via the probe on the front panel of the signature analyzer. By using a 40-pin multiplexer, the total test time may be reduced to the order of 1 to 2 minutes.

Improving the Digital Hybrid Testing on the DFI System – The complexity of the hybrid microelectronic circuits used in advanced digital electronic and missile systems is increasing at an exponential rate. Present and future use of custom designed hybrid modules causes a high production test and rework cost. Production and electronic manufacturing experience indicates two primary reasons for the high rework cost: 1) the large amount of time required to develop a test program for the complex digital hybrid modules, and 2) developing the technique necessary to fault isolate a hybrid module of high logic density.

To highlight the technology or economic factors investigated, five major tasks for the recommended Hybrid program are identified and a brief description of each is given in the following paragraphs.

Probing Technique Development – Under the direction of the system computer, the test system operator isolates faults by probing the guided probe to a specific node. For Hybrid test, an appropriate probing technique is required to locate a fault without damaging the hybrid circuit chip. A fixed point probe card (up to 300 probe points) will reduce setup time and supply uniform probe pressure with minimum scrubbing.

Operational Software Development for RAMs – Due to the internal complexity of the RAMs, a significant number of faults caused by internal failures may not be manifested on the external pins. To cover all the gate level faults, so many test patterns are required that they will overflow the capability of the Automatic Test System's simulator. This problem can be solved by developing system software to bypass the software of the test system's logic simulator. With the new software control, large RAM patterns could be generated by the test engineer.

Test Program Development – This task seeks to develop new logic primitives that would effectively aid in developing LSI or VLSI models. The new circuit logic models would then be added to the existing Automatic Test System's IC library.

By utilizing the multi-terminal capability of the DTS-70 ATE, for example, alternative hybrid modeling methods may be developed concurrently and evaluated for software requirements as well as for testing and fault isolation

effectiveness. The concurrent modeling can therefore be carried out without an adverse effect on programming time.

Another method could be progressive testing, that is, the testing all individual chips prior to inserting them into the hybrid module.

Test Fixture/Adapter – Hybrid modules usually do not have standard pin or size configurations. Therefore, the Unit Under Test (UUT) and the Automatic Test System need an interface solution. An economical approach would be the TEXTOOL Socket/Receptacle (up to 64 pins) which has 12 different sizes and has a typical life of 25,000 to 50,000 insertions.

A costlier alternative would be a probe fixture featuring rapid load and unload, automatic vacuum valve to vacuum chuck, an output connector, and an individual X-Y-Z adjustment. This would be ideal for use with the fixed point probe card.

Hybrid Cost Analysis – An important factor for MM&T concerning hybrids is repair cost. A cost analysis should be performed to determine the break-even point for hybrid repair/rework costs versus the cost of replacing a faulty hybrid module. The results of these cost analysis comparisons would be a valuable guideline in determining when to throw away a faulty unit.

In performing the cost study, a number of parameters would be considered in evaluating the relative costs for repair and discard. These parameters should include the complexity of the device (number of equivalent gates), the production quantities of the device and the system it is used in, and the type of technology used in developing the hybrids (thin film, thick film, etc).