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Bubble Memory Module

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1. INTRODUCTION AND PROGRAM ACCOMPLISHMENTS

Most space missions require data storage equipment onboard for spacecraft control and to retain data for delayed telemetry. It has been recognized that implementation of bubble domain technology as a data recorder offers advantages in versatility, potential reliability, and cost.

Future spacecraft missions and Shuttle-transported experiments impose considerable variability in high reliability data recorder needs. Capacity requirements vary from less than 10 M bits upward. Data format may be either serial, as primarily used in tape recording, or parallel for interfacing to microprocessor and computer controllers. Controls may vary from simple on/off lines to multiple commands with various command word formats. Desired memory performance includes single and multiple channel configurations, command reconfiguration, ability to record specific events, simultaneous read and write, asynchronous data rates, access to large memory blocks containing data or computer programs, and graceful failure via omission of failed memory cells. To simultaneously satisfy these needs in a manner which does not impose one user's requirements on another, a Bubble Memory Module (BMM) concept has been developed which separates bubble related technology from application oriented technology, thus permitting the user to tailor the memory module's organization to suit a specific experiment.

A two board prototype of a BMM which utilizes unique characteristics of bubble domain memory was designed, built, and tested on this program. The prototype development managed by NASA-Langley Research Center and jointly funded by NASA-OAST and the Air Force Space Division, is aimed at maturation of bubble domain technology for space applications. [Ref 1, 2, 3]

Accomplishments of the program not only include design and testing of a prototype but also development of processes and verification of design innovations. Perhaps the most important accomplishment from the viewpoint of future mass memory using bubble domain is demonstration of a sense multiplexer which greatly reduces power and circuitry dedicated to bubble detection. A second is the development of a small rugged multichip hermetic memory cell which is driven with an expandable coil matrix. This approach reduces power and circuitry and allows memory expansion without correspondingly increasing circuitry. A few problems occurred during the program. Several hermetic sealing methods which were costly in terms of development effort were attempted before a suitable method was found. The manufacturing yield run had to be aborted in order to conserve program funds after processing problems occurred. Performance of the timing PROM circuit, although adequate for the prototype, is deficient for full scale development. But overall the program has demonstrated a manufacturable Bubble Memory Module which can be put into production with a minimum of effort.

Use of commercial products or names of manufacturers in this report does not constitute official endorsement of such products or manufacturers, either expressed or implied, by the National Aeronautics and Space Administration. This report was prepared by Autonetics Strategic Systems Division, Electronic Systems Group, Electronics Operations of Rockwell International at Anaheim, CA under NASA Contract Number NAS1-14174. It summarizes work performed on this contract covering the period 1 May 1978 to 1 June 1980.

Use of standard international units (SI) as the primary unit of measure has been waived for this report. Table 1-1 is provided for converting the U.S. customary units used in this report to SI units.

Table 1-1. Conversion Table

To convert from	to	Multiply by
	ACCELERATION	
free fall, standard (g)	metre per second squared (m/s^2)	9.806 650*E+00
	ANGLE	
degree (angle)	*radian (rad)*	1.745 329 E-02
	AREA	
circular mil	square metre (m^2)	5.067 075 E-10
in^2	square metre (m^2)	6.451 600*E-04
ft^2	square metre (m^2)	9.290 304*E-02
	ELECTRICITY AND MAGNETISM	
gamma	tesla (T)	1.000 000*E-09
gauss	tesla (T)	1.000 000*E-04
oersted	ampere per metre (A/m)	7.957 747 E+01
	ENERGY (Includes Work)	
calorie (mean)	joule (J)	4.910 02 E+00
	LENGTH	
angstrom	metre (m)	1.000 000*E-10
micron	*metre (m)*	1.000 000*E-06
mil	metre (m)	2.540 000*E-05
	MASS	
gram	kilogram (kg)	1.000 000*E-03
ounce	kilogram (kg)	2.834 952 E-02
pound (lb avoirdupois)	kilogram (kg)	4.535 924 E-01
	PRESSURE OR STRESS (Force per Unit Area)	
atmosphere (standard)	pascal (Pa)	1.013 250*E+05
inch of mercury (32^oF)	pascal (Pa)	3.386 38 E+03
psi	pascal (Pa)	6.894 757 E+03
torr (mmHg, 0^oC)	pascal (Pa)	1.333 22 E+02
	TIME	
hour	second (s)	3.600 000*E+03
minute	second (s)	6.000 000*E+01
year (365 days)	second (s)	3.153 600*E+07
	VOLUME (Includes Capacity)	
ft^3	cubic metre (m^3)	2.831 685 E-02
in^3	cubic metre (m^3)	1.638 706 E-05

2. MEMORY MODULE REQUIREMENTS AND GOALS

2.1 GENERAL

This section summarizes requirements for the Bubble Memory Module given in the Statement of Work. Design approaches developed in subsequent sections are based on these design requirements.

Requirements are for a memory system (Figure 2-1) which is nonvolatile, versatile, adaptable to both serial and parallel data applications, highly reliable and cost effective. The memory affords reasonable radiation hardness to meet the bulk of potential applications. The design employs a module concept to maximize utility in a broad range of applications.

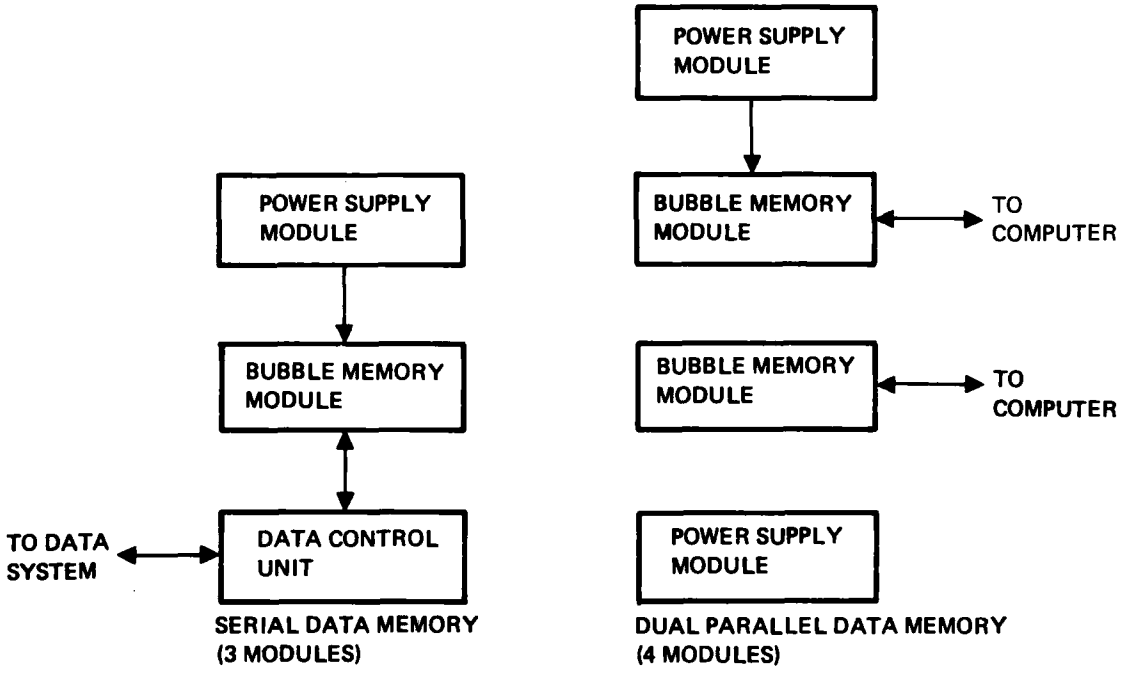


Figure 2-1. Two applications of the BMM.

2.2 DATA INTERFACE

The memory module has two independent control and data buses each with the signals listed below. Interface is TTL compatible with the ability of operating reliably with cable lengths of six feet in length.

Power Strobe - This signal powers up and initializes the module in preparation for the receipt of the user clock (UCLK).

Cell Address. - This is a parallel binary coded signal of three bits used to select the cell for the next operation. Block size is 51,200 words of 16-bits each. Retrieval time for the block is 0.61 seconds with a first bit access time of 10 microseconds.

Board Address. - This is a set of 3-bits used to select one of potentially eight boards for the next operation.

Address Ready. - This signal is an output signal to the user which acknowledges that the module is busy. Input address is latched in the memory module just prior to "address ready" high to low transition.

Data Ready. - This is another output signal to the user which acknowledges receipt of data on write or which provides an indication of valid data on read.

Mode. - This is a single line which indicates whether a read or write operation is required for the next operation.

User Clock. - This signal begins execution of the next data cycle. Cell address and mode control must have been previously set up.

Data input and output (I/O) interface is 16-bits wide parallel. The interface is a bidirectional bus used either for read or write. Data interface is isolated from the bus when the memory module is unpowered. Data rate of the memory module depends on the type of access, burst or incremental. In incremental access, average data rate is user dependent and can vary from 0 to 55K 16-bit words per second. A start and stop cycle is associated with each word accessed. In burst access; a block of sequential words is a fixed instantaneous rate of 83.3K 16-bit words per second. Average data rate is user dependent up to the instantaneous rate. In burst access, a start and stop cycle is associated with each block, thus burst access provides for a lower power mode of operation for a given number of accesses.

2.3 ENVIRONMENTAL REQUIREMENTS

Environmental requirements of the memory module covered in this section were verified to some extent by subassembly testing and by testing of the prototype. Qualification of the memory module prototype under these requirements was not part of this contract.

The weight of a fully populated 10^7 bit memory module is 3.3 kilograms (7.32 lbs). This weight doesn't include cover plates or other mounting hardware which would be required in a stand-alone application nor does it include a power supply.

Power required of the memory module is a function of frequency as shown in Figure 7-26. Test results of the module indicate 26.6 watts maximum power dissipation compared to the required 30 watts. Projections during the program ranged from 18 to 24 watts. Minor modifications to the design will reduce power dissipation to about 23 watts.

The memory module must operate over a range of -10C to 60C and retain data over a non-operating range of -40C to 85C. These limits also apply to the module in a vacuum environment. Cells were tested from -10C to + 75C while the module was tested from -10C to 60C.

To ensure that the memory module withstands shock and vibration during spacecraft launch, separation, and deployment, it is designed to pass a number of mechanical tests during qualification. Sinusoidal vibration levels for qualification and flight acceptance testing are given in Tables 2-1 and 2-2 respectively. Gaussian random vibration levels for qualification and flight acceptance correspond to the spectrum analyses of Tables 2-3 and 2-4, respectively.

TABLE 2-1. DESIGN QUALIFICATION SINUSOIDAL VIBRATION REQUIREMENTS

Axis	Frequency	Level
All	5 – 28 28 – 100 100 – 200	0.50 in DA 20 G 15 G

Sweep Rate: 2 octaves/minute

TABLE 2-2. FLIGHT ACCEPTANCE SINUSOIDAL VIBRATION REQUIREMENTS

Axis	Frequency	Level
All	5 – 28 28 – 100 100 – 200	0.33 in DA 13.3 G 10 G

Sweep Rate: 4 octaves/minute

TABLE 2-3. DESIGN QUALIFICATION RANDOM VIBRATION REQUIREMENTS

Axis	Bandwidth	PSD	Grms
All	20 – 200 200 – 400 400 – 600 600 – 1200 1200 – 2000	0.17 g^2/Hz +6 dB/oct. 0.70 g^2/Hz -6 dB/oct. 0.17 g^2/Hz	24.4 G

Duration: 2 min/axis

TABLE 2-4. FLIGHT ACCEPTANCE RANDOM VIBRATION REQUIREMENTS

Axis	Bandwidth	PSD	Grms
All	20 – 200 200 – 400 400 – 600 600 – 1200 1200 – 2000	0.075 g^2/Hz +6 dB/oct. 0.31 g^2/Hz -6 dB/oct. 0.075 g^2/Hz	13.2 G

Duration: 2 min/axis

A shock transient where positive and negative acceleration shock response spectra satisfy the requirements of Figure 2-2 for qualification tests and Figure 2-3 for flight acceptance tests will be applied to the memory module. Acceleration tolerance is designed to be ±33g.

The memory module is expected to pass mechanical tests applied along each of three orthogonal axes and system functional tests during pre-test, test, and post-test periods.

Memory module design provides no more than 0.5 gram per square centimeter aluminum shielding while system components were selected to provide a minimum radiation susceptibility of 100K rad (Si) total dose of 1 mev electrons.

It is recognized that these minimum dose levels restrict some potential users.Therefore it was a goal of the module development program to increase the radiation hardness as far as practical, consistent with performance requirements and system goals stated previously.

The memory module is expected to demonstrate that its performance is not degraded during exposures to ±10 Oe d.c. magnetic field applied along any axes with one axis being the direction of the cell bias field (six exposures).

Magnetic field from the memory module is expected to be less than 10 n tesla and 3 n tesla, respectively at a distance of one meter.

An electromagnetic compatibility (EMC) requirement will be imposed on the memory module using the requirements and limits of MIL-STD-461/462.

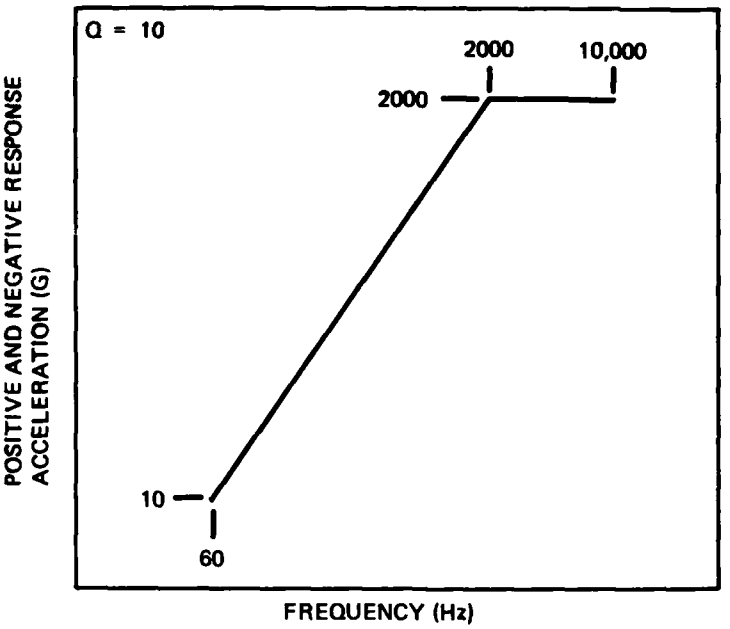


Figure 2-2. Design qualification mechanical shock requirements.

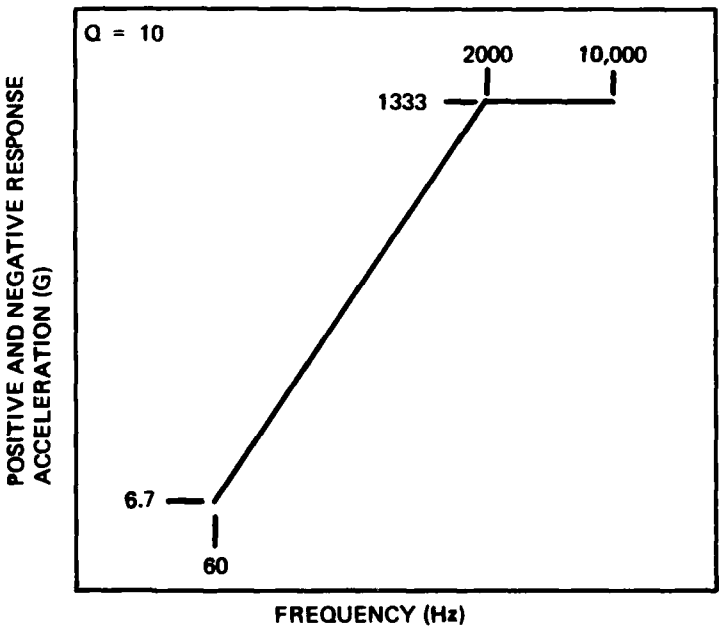


Figure 2-3. Flight acceptance mechanical shock requirements.

3. SYSTEM CONFIGURATION AND ORGANIZATION

3.1 BUBBLE MEMORY MODULE CONCEPT

The BMM concept employs a basic building block defined as a "bubble memory module" for generation of a variety of memory systems. A bubble memory module exemplified in Figure 3-1 contains a bank of bubble memory cells (a cell is a group of chips simultaneously accessed in parallel to attain desired operational data rates) and appropriate circuitry for equal access to each cell, but provides no functional organization of the cells. Functional organization and housekeeping tasks are left to a user-designed controller. Ultimate system characteristics and limitations are determined by bubble chip architecture and the number of chips per cell.

Figure 3-2 depicts memory system organizations available with a parallel-data memory module. Capacity expansion is provided by adding BMMs to a user interface bus, by adding storage boards to BMMs or by combinations of the two. Maximum system data rates are determined by the size of the user-designed power supply and the number of memory modules operated simultaneously. The simplest memory system is the parallel data system shown in Figure 3-2(B), where the user controller or computer can directly access each cell.

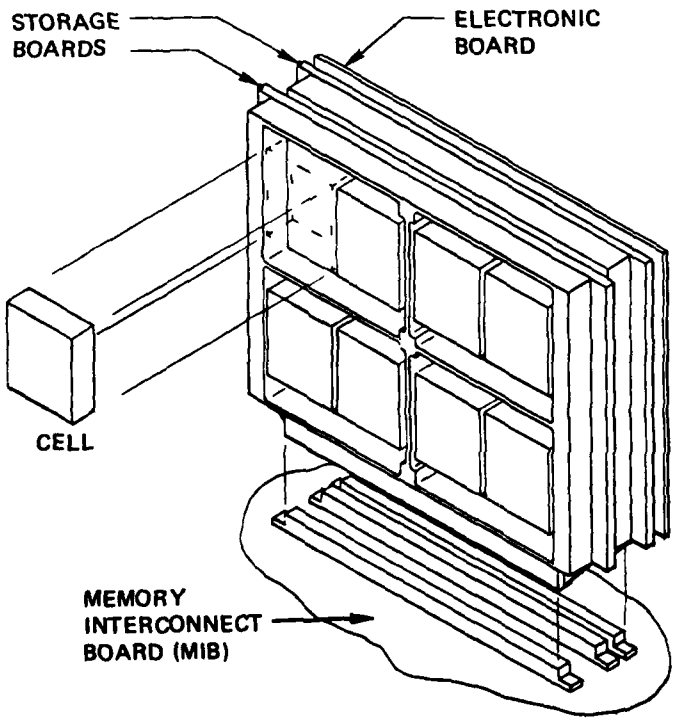


Figure 3-1. Bubble Memory Module example.

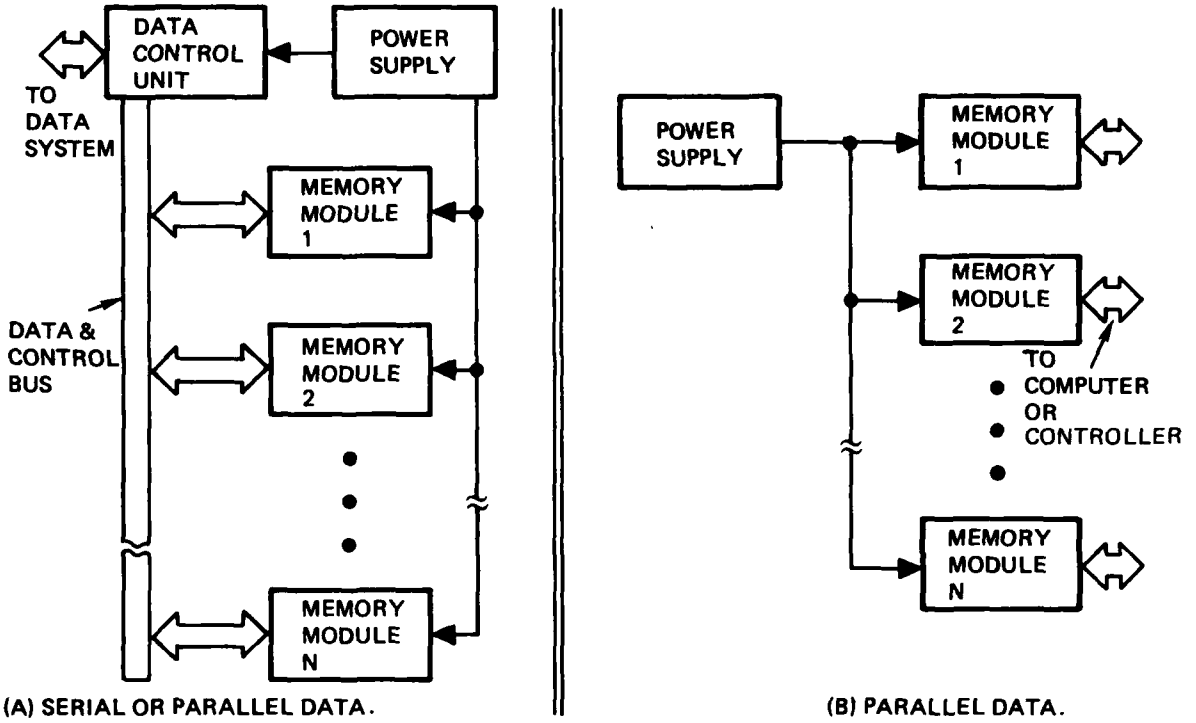


Figure 3-2. Memory system concepts.

The memory system shown in Figure 3-2(A) contains a user-designated Data Control Unit (DCU) which determines the organization of the memory system. The DCU can be so simple as to route data to and from the appropriate memory modules by a predetermined schedule, or it can provide a high degree of in-flight commandable configuration control with complete housekeeping of memory status. Both serial and parallel data may be accommodated in this scheme with the DCU providing the serial/parallel conversion.

Mechanical design is based on requirements for modularity wherein the bubble memory module may be combined with other modules to form a serial data memory (SDM), dual parallel data memory (DPDM), and other system configurations. Modularity is achieved by having standardized mechanical and electrical interfaces for the BMM and all other modules which are to be packaged along with the BMM. These modules are mechanically fixed and electrically interconnected to a chassis/MIB assembly which is unique to the particular system configuration required. Physical characteristics of several memory configurations shown in Figure 3-3 are given in Table 3-1. A basic stand-alone 10^7 recorder including a power supply is shown in Figure 3-4. When the system contains a few boards as in these configurations, mechanical and thermal considerations dictate a housing arrangement where the master interconnect board is perpendicular to the cold plate. Interface connectors from the MIB would be placed on the rear wall of the housing.

Another case style shown in Figure 3-5 is required for a large number of modules in order to minimize thermal path length and center of gravity. The concept shown is an example of packaging bubble memory modules in a high reliabilty configuration. A single failure will degrade capacity by no more than 14 percent.

TABLE 3-1. BMM PHYSICAL CHARACTERISTICS

Configuration Storage Capacity		BMM 1.3×10^7	SDM 1.3×10^7	SDM 2.6×10^7	DPDM $6.6 \times 10^6 \times 2$	PDM 6.6×10^6
Storage Module						
Quantity	Ea	2	2	4	2	1
Weight Kg	(Lb)	2.96 (6.52)	2.96 (6.52)	5.9 (13.04)	2.96 (6.52)	1.5 (3.26)
Volume Cm^3	(In^3)	2070 (126)	2070 (126)	4130 (252)	2070 (126)	1030 (63)
Electronics Module						
Quantity	Ea	1	1	1	2	1
Weight Kg	(Lb)	0.34 (0.75)	0.34 (0.75)	0.34 (0.75)	0.68 (1.50)	0.34 (0.75)
Volume Cm^3	(In^3)	361 (22)	361 (22)	361 (22)	722 (44)	361 (22)
Controller Module						
Quantity	Ea	0	1	1	0	0
Weight Kg	(Lb)	–	0.45 (1.00)	0.45 (1.00)	–	–
Volume Cm^3	(In^3)	–	672 (41)	672 (41)	–	–
Power Supply Module						
Quantity	Ea	0	1	1	2	1
Weight Kg	(Lb)	–	1.8 (4.00)	1.8 (4.00)	3.6 (8.00)	1.8 (4.00)
Volume Cm^3	(In^3)	–	1345 (82)	1345 (82)	2690 (164)	1345 (82)
Chassis – MIB						
Weight Kg	(Lb)	–	2.95 (6.50)	3.81 (8.40)	3.68 (8.10)	2.22 (4.90)
Volume	(In^3)	–	7810 (476)	10690 (652)	9380 (572)	5080 (310)
System Total						
Weight Kg	(Lb)	3.3 (7.3)	8.5 (18.8)	12.3 (27.2)	10.9 (24.1)	5.9 (12.9)
Volume Cm^3	(In^3)	2930 (148)	7810 (476)	10690 (652)	9380 (57.2)	5080 (310)

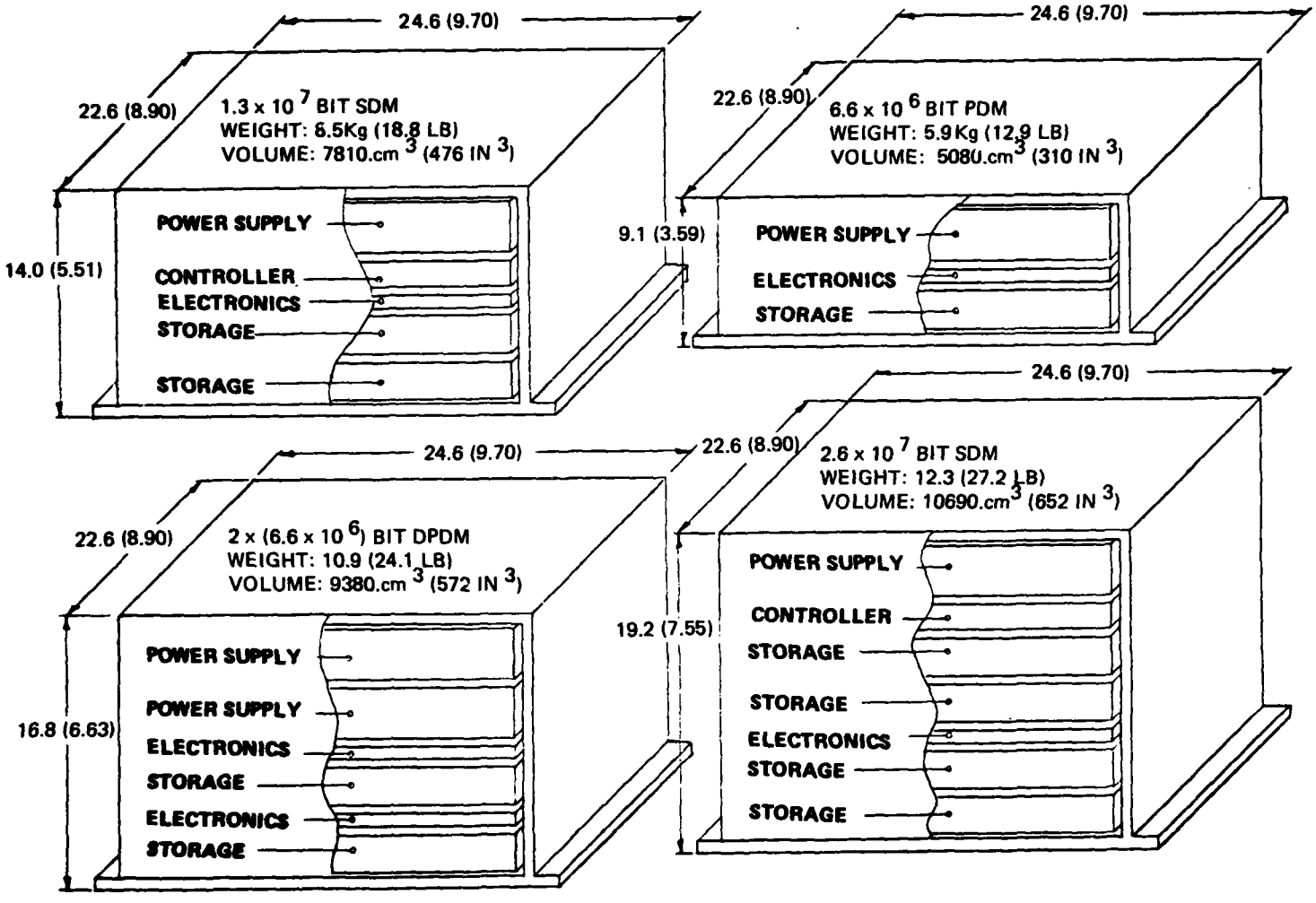


Figure 3-3. BMM configurations.

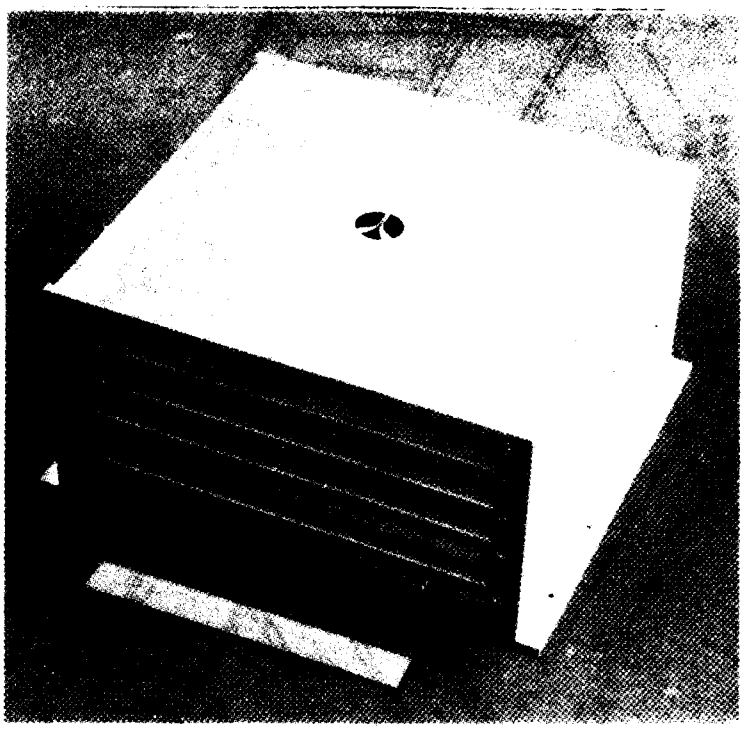


Figure 3-4. 10^7 recorder mockup.

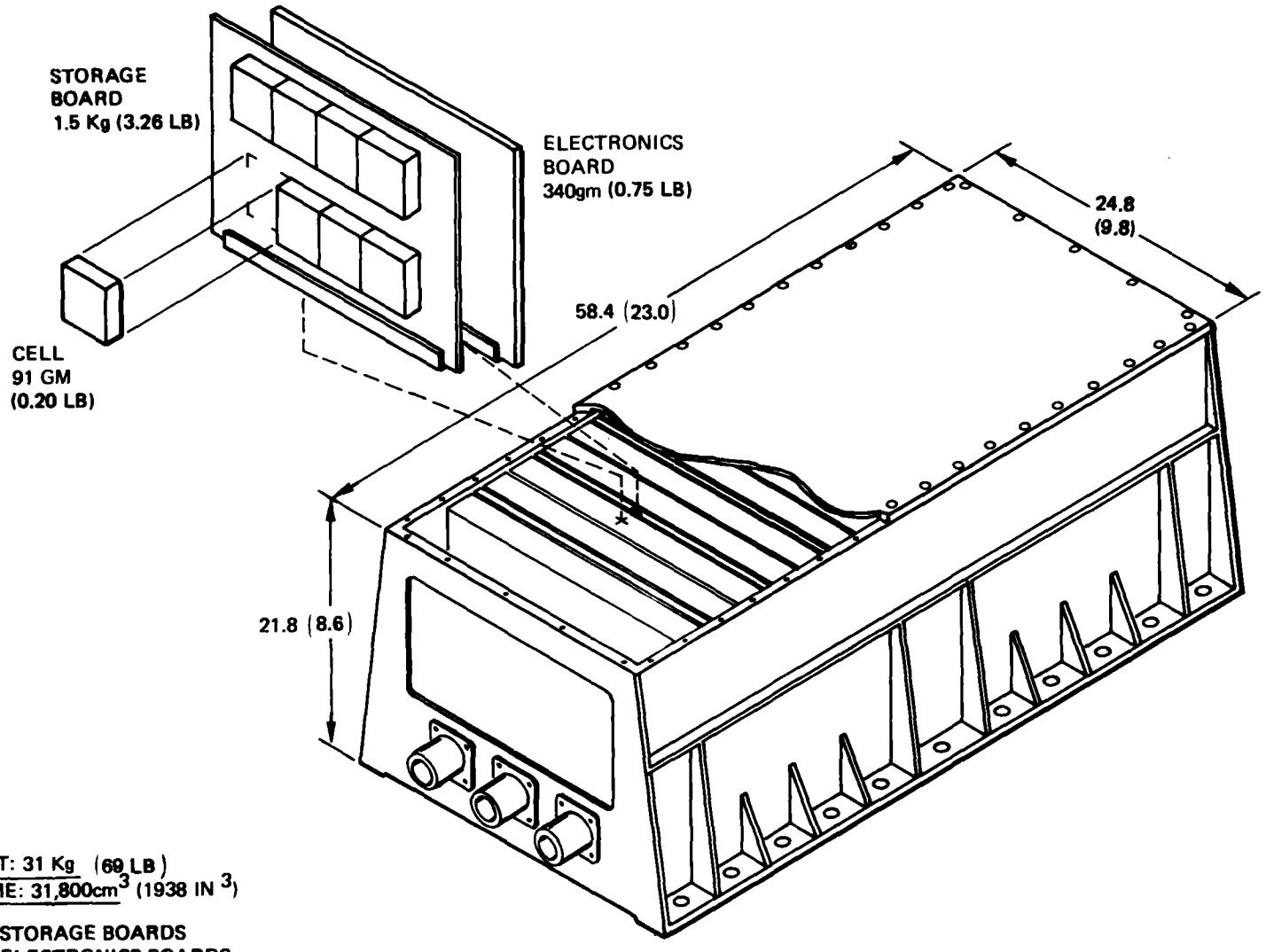
TABLE 3-2. PREDICTION SUMMARY FOR 10^7 BMM

Module	Quantity	Each FPMH*	Total FPMH*
Storage Module	2	2.49	4.98
Electronics Module	1	1.32	1.32
Power Supply	1	1.59	1.59
MIB	1	0.20	0.20
			8.09

*FPMH = Failures per Million Hours

The prediction is based on these ground rules:

Environment – Space
Average Component Case Temperature – 50°C
100% Operational
Class S Integrated Circuit
JANS Transistors/Diodes
ER Passive Devices
Failure Rates per MIL-HDBK-217B, Notice 2



WEIGHT: 31 Kg (69 LB)
VOLUME: 31,800cm^3 (1938 IN ^{3})

14 STORAGE BOARDS
7 ELECTRONICS BOARDS
DUAL POWER SUPPLY

Figure 3-5. 0.9 x 10^8 mass memory system.

3.1.1 Reliability Considerations

Because of its modularity, the Bubble Memory Module concept can be tailored to meet reliability requirements. For example, the concept in Figure 3-5 is configured to eliminate single point failures by using redundant 10^7 BMMs, each with its dedicated electronics board. Figure 3-6 is the reliability model of such a system. Based on analysis of the parts list for the prototype BMM, an MTBF of 120,000 hrs (14 yrs) is projected for the basic 10^7 module with power supply. A breakdown of failure rates and assumptions are given in Table 3-2.

For applications where reliability is secondary to cost considerations such as those where maintenance is possible the BMM can be expanded in capacity by adding up to eight storage boards per electronics board. Support electronics doesn't increase linearly with storage thereby reducing cost per bit but at the same time decreasing MTBF to 40,000 hours under Table 3-2 assumptions.

3.2 BUBBLE MEMORY MODULE DESCRIPTION

A memory module has been designed and a Prototype fabricated consistent with the BMM concept. To minimize component count, weight, and volume, the field coils are arranged in a matrix, and the bubble chip operators and detectors are multiplexed. This memory module is primarily aimed toward memory module applications in the 7 to 52 megabit range with minimum operational power at data rates from zero up to 1.33 Mbits/sec. These goals have led to the choice of a 100K bit serial bubble chip (actually 102,400 bits) and a cell containing eight chips in a common bias and field coil assembly. In addition to a detector designed for multiplexing, the 100K bit serial chip has first-bit-detection capability and is physically a relatively small chip. First-bit-detection enables access to a single data word, thus permitting very low data rates without additional data buffering. The small physical size of the chip offers low power by minimizing field coil volume. Table 3-3 is a summary of overall features of the memory module.

TABLE 3-3. BUBBLE MEMORY MODULE CHARACTERISTICS

Characteristic	Value
Module Capacity	6.55M to 52.4M bits
Data Rate	Asynchronous, DC to 1.33 Mbs
Word Size	16 bits (parallel)
Error Rate	1 in 10^8 bits
Average Power	Standby – 0 watts
	100 Kbs – 3 watts
	1 Mbs – 22 watts
Operate Range	-10°C to +60°C
Data Retention	-40°C to +85°C
Power Sources	+5, ±12, +27 volts
Radiation	100K Rad (Si)
MTBF for 13M bits	100,000 hours
Weight for 13M bits	3.31 KG (7.3 lbs)
Volume for 13M bits	2770 cm^3 (169 in^3)

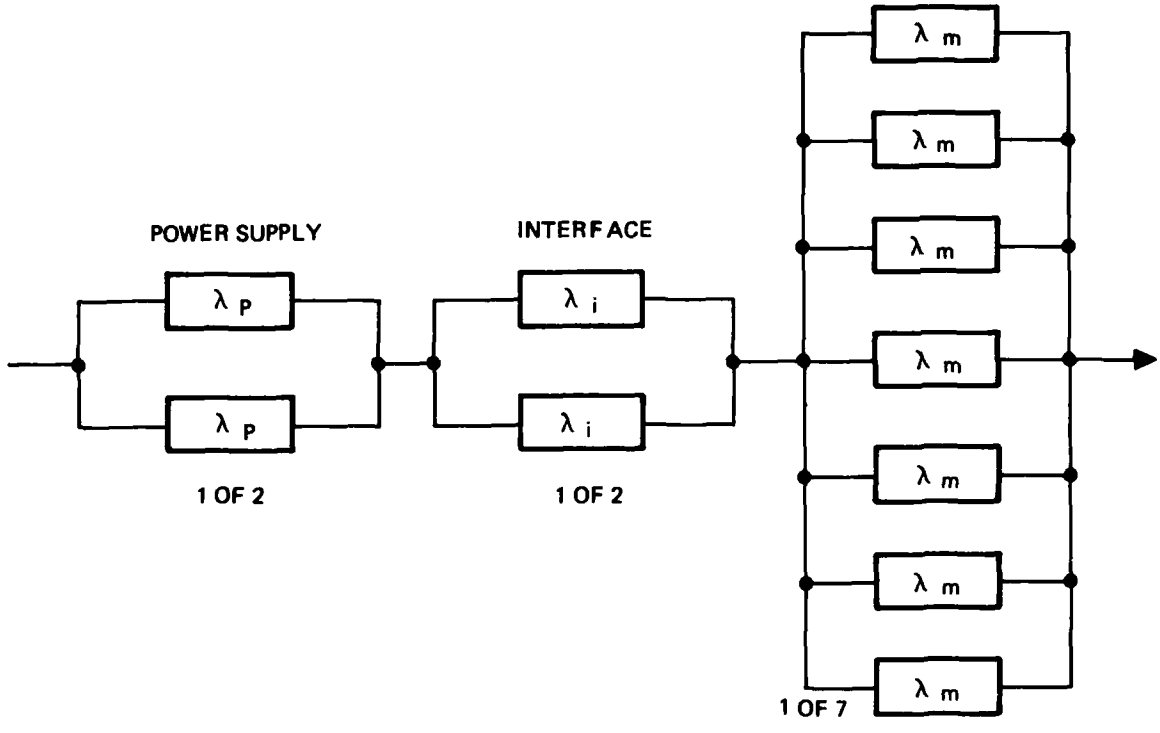


Figure 3-6. Reliability model of mass memory system.

The memory module consists of one electronics board and from one to eight storage boards, as shown in Figure 3-7. With the eight-chip cell (819,200-bits/cell), the memory module capacity is expandable in 6.55 M bit increments. Detector noise is minimized by locating sense circuits, cell select switches, and memory cells on the same board. Thus, only high level data signals are transmitted between the two boards. The division of other functional blocks on the electronic and storage boards is less critical but results in two equal-area circuit boards and nearly equal power distribution. Bubble chip operator current sources are located on the electronics board. Eight generator current sources (GEN) provide the signals to write independent data simultaneously into the eight chips of a cell. For erasing, each of two transfer-out (TRO) sources simultaneously drive the transfer-out loops for eight chips in the selected cell. Similarly, each of the two replicator sources (REPL) simultaneously drives the replicator switches on all chips in the cell. The TRO sources are de-energized in Read for nondestructive readout. REPL sources are energized in both Read and Write mode so that data are always available in the detector.

Bubble memory module building blocks partitioned analogous to major design tasks are given in Figure 3-8. Interface (data, command, and address) to the BMM is through either of two buses. Signals are active low logic. Power switching is used to ensure zero standby power and low operating power. The four voltages required and the status lines shown are single line functions. Over temperature and coil driver over current are the status indicators provided. The erase function allows erasing of all cells of a selected board.

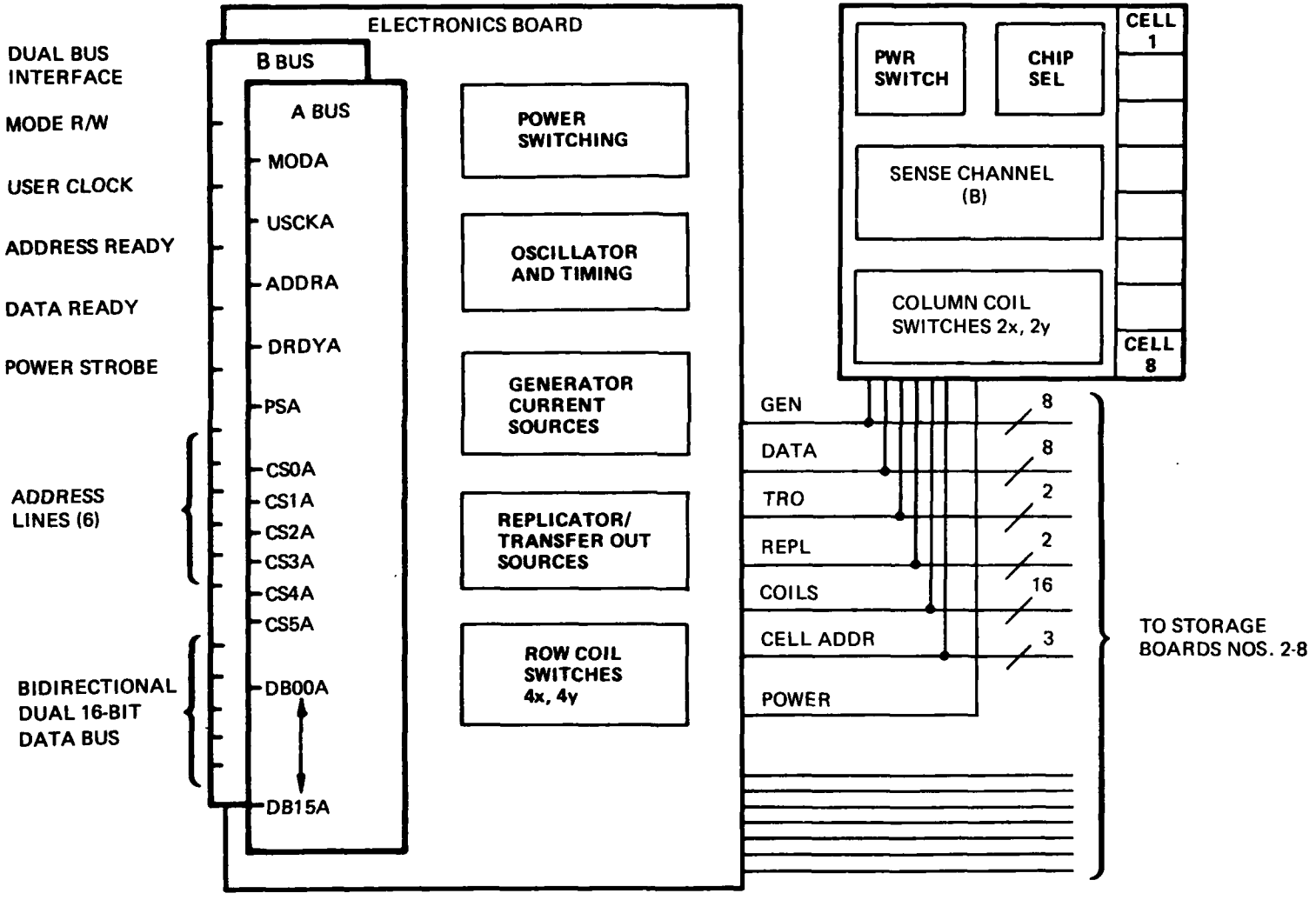


Figure 3-7. Memory module function partitioning.

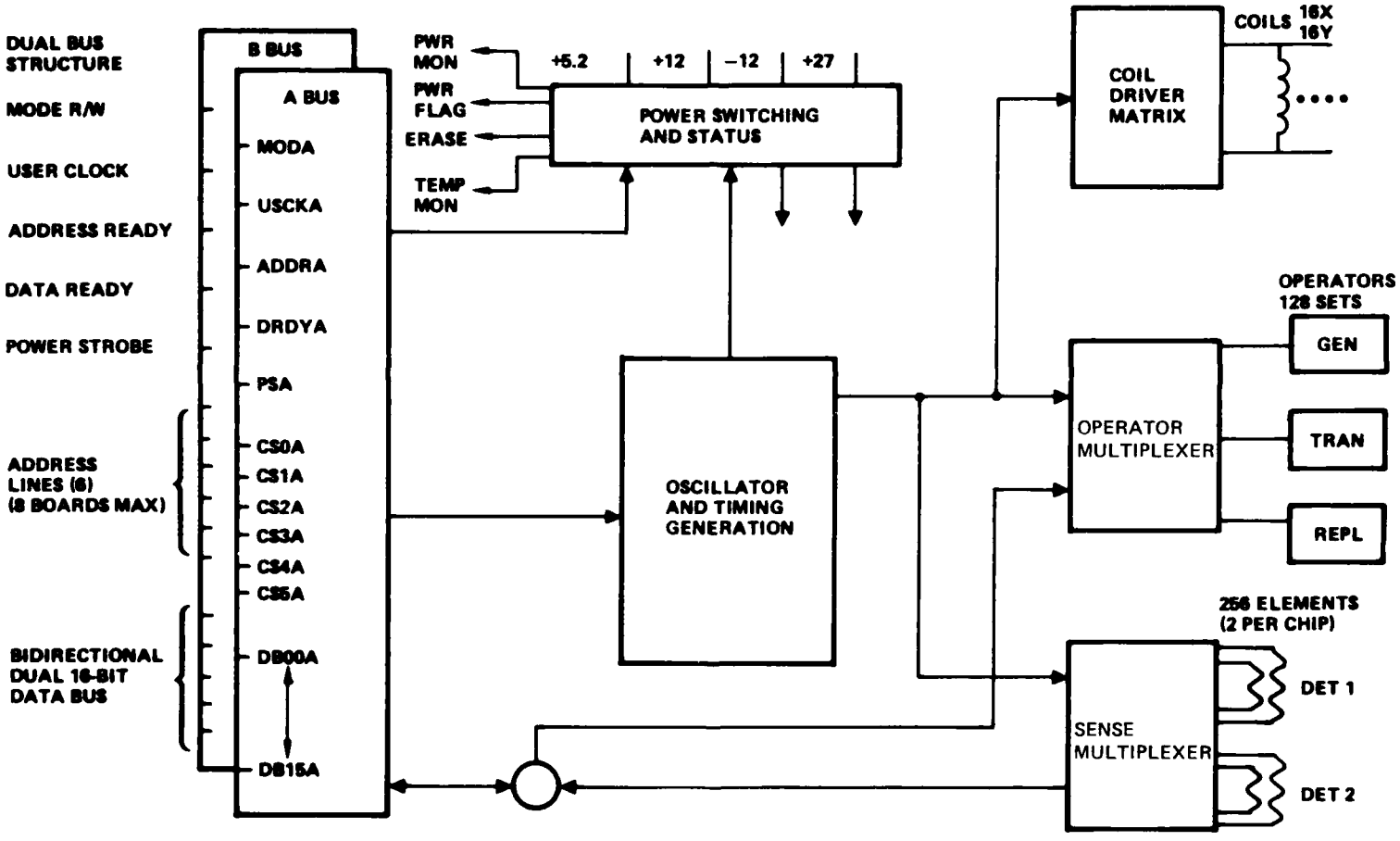


Figure 3-8. Electrical block diagram.

Memory timing is derived from a crystal oscillator which is divided down and counted to provide PROM address. The PROM controls 28 functions with 187 nanosecond minimum resolution and pulse width. The sense multiplexer (lower right) is the most critical design task because of the detector's low input signal and its susceptibility to digital noise. Detector current from the circuit generates a voltage at the detector which is discriminated as either a "1" or "0" by the circuit. Bubble control (generation, replicator and transfer out) is provided by the operator multiplexer. The Coil Drive matrix applies digital timing to the selected memory cell.

Figure 3-9 shows allocation of power, weight, and components of each block. Allocation of components and power is heavily weighted to the coil driver function. In reviewing the SSDR design at the beginning of this program the same conclusion was reached about the SSDR driver matrix. Alternate designs such as a sine wave resonant driver were found to be less acceptable from a components viewpoint. Despite considerable improvements in the basic design the trapezoidal driver still requires a considerable number of baluns and steering diodes. Reconfiguring the coil for higher voltage and lower current will reduce driver power and relax requirements on diodes. Generally the lower the current, the smaller the devices can become.

3.2.1 Interface Modes

Two types of data access are provided by variation in the User Clock timing - incremental and burst. The operation of the memory module is best described by considering each access type separately, assuming only one data bus is energized. Incremental access, with timing depicted in Figure 3-10, causes the selected cell to make two 6-μsec field rotations and shut down, transferring one word on the 16 parallel data lines. When the Power Strobe logic line is logic low, interface is energized. Two microseconds time lapse is required after the Power Strobe goes low to allow interface logic circuitry to stabilize. The Power Strobe line must be maintained low by the user for the duration of the cycle, as indicated by the Address Ready line going low and then returning to its original high state. At the user's option, the Power Strobe may either be returned to its high state at the conclusion of the cycle (power strobing) to save standby power, or it may be held low continuously. The User Clock pulse must occur when the Address Ready line is in the high state and must be at least one microsecond wide (glitch protection) to cause any response. The width of the negative pulse of the User Clock determines whether the memory module operates in burst or incremental access. For incremental access this pulse width must be greater than 7.5 μsec. After the Address Ready returns to its high state, a second User Clock pulse of at least 7.5 μsec duration will provide access to the next 16 bit parallel data word. This arrangement not only allows user access to single 16-bit words but also accommodates simple square wave clocking. The purpose of the Address Ready line is to indicate by a low state that the memory module has received the User Clock pulse, has latched the Mode (Read or Write) and Address (cell select), and is in the process of execution. During this low state the memory module does not recognize any signals for the User Clock, Mode, and Address lines. The Data Valid line is to provide clocking for data setup and to indicate by a high state when data are valid on the data bus interface.Data validity is ensured by the user in the Write mode and by the memory module in the Read mode. In the Write mode the user must actually maintain data validity only throughout the Data Ready transition from high to low, since data are latched at that time. A positive-going transition on the Data Ready line indicates the next word may be established on the data bus lines. In the Read mode, data are valid on the data bus lines near the end of the cycle. Incremental access provides asynchronous data rates from zero to 695K bits/s as determined by the minimum time to start, rotate two field cycles, and stop.

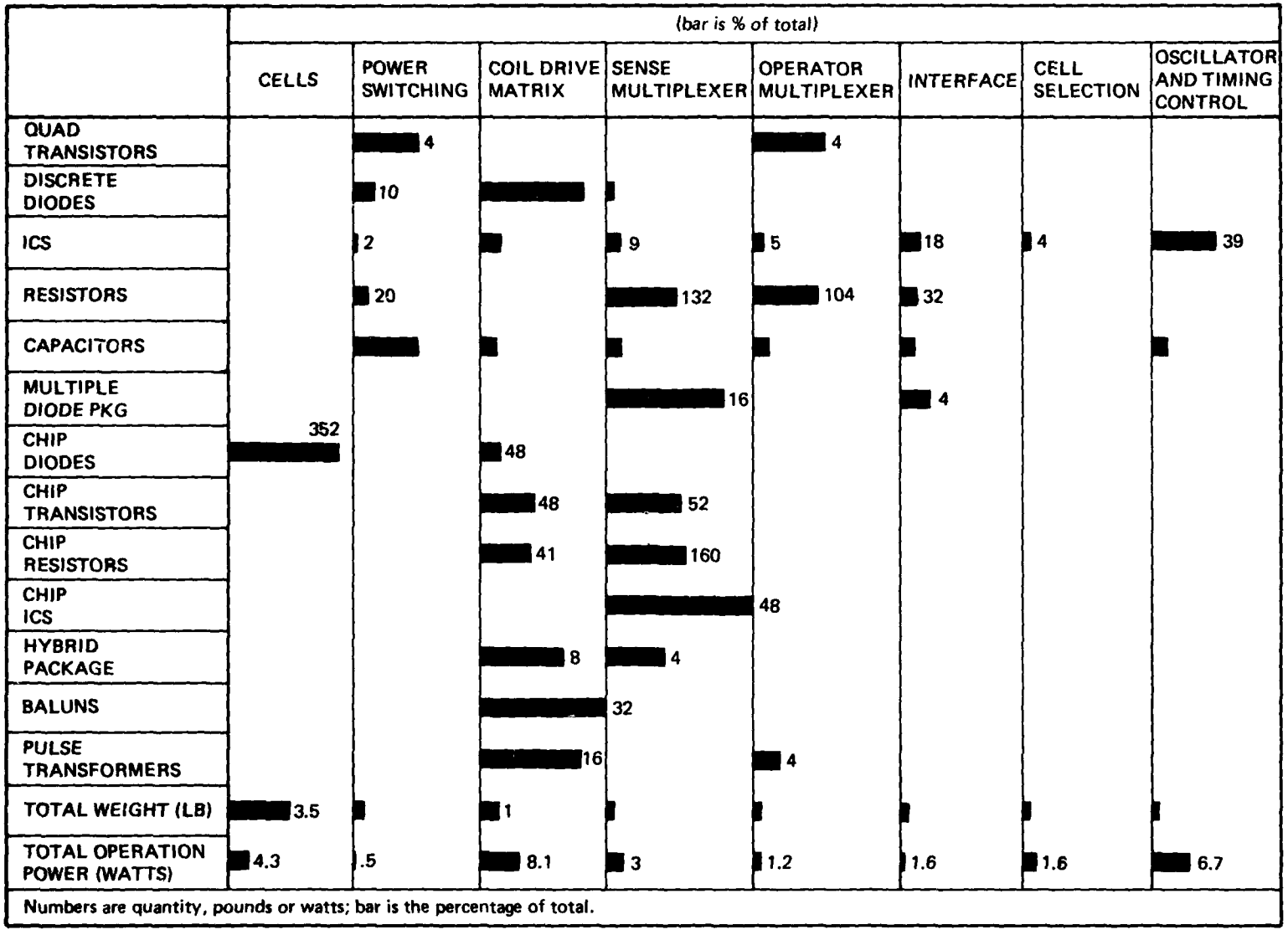


Figure 3-9. Allocation of parts, weight and power by function (1.3 Mbit BMM).

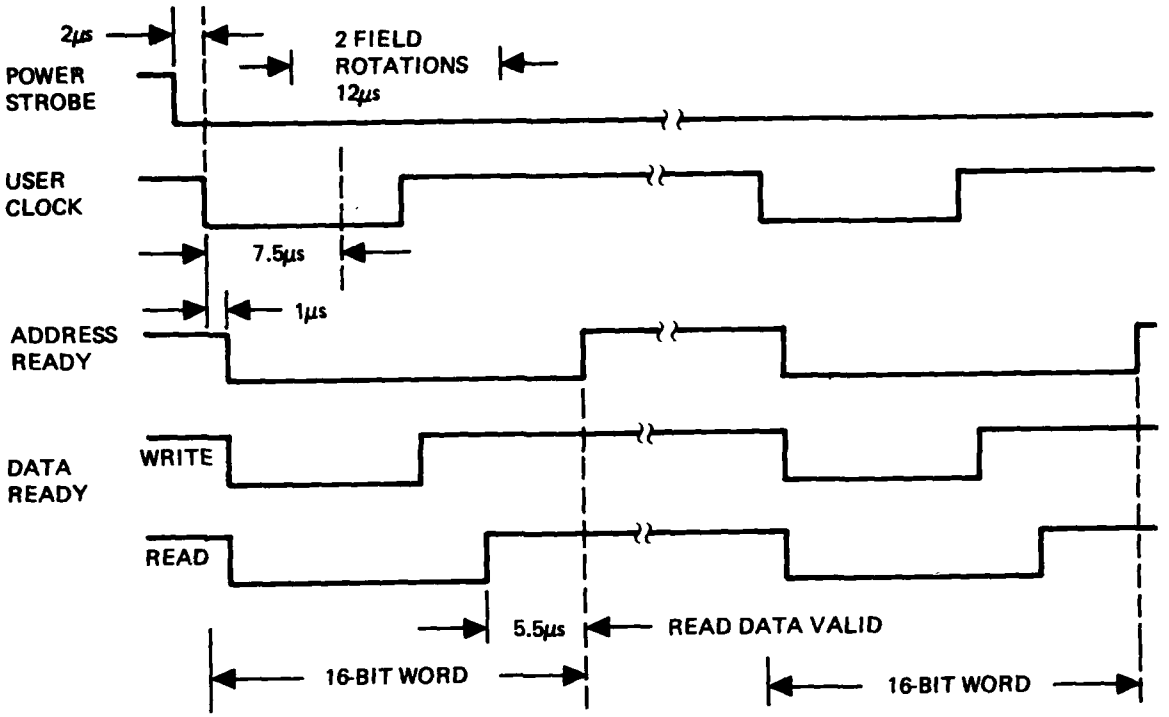


Figure 3-10. Incremental access timing.

Burst access is accomplished by accessing blocks of data through the application of an initial pulse and a stop pulse on the User Clock line. As shown in Figure 3-11, burst access is initiated when the initial User Clock pulse is less than 7.5 μsec wide. Thereafter, the times during which the Data Ready line is low represent windows for stopping memory module operation. The user may count the negative going transitions of the Data Ready line until the desired number of words are accessed and apply the stop pulse during the appropriate window. The stop pulse must be at least 1.0 μsec wide. In burst access the instantaneous data rate is 1.33 Mbits/μsec as determined by the memory module's internal drive field rate of 166.6 kHz. Thus, asynchronous average data rates vary from zero to greater than 1 Mbit/sec by the user's choice of a burst repetition rate. Since internal timing controls the instantaneous data rate during a burst, the user must synchronize to the Data Ready line not only for proper data timing but also for stopping the burst at the desired data count. Mode, Address, Power Strobe, and Address Ready serve the same functions as for incremental access.

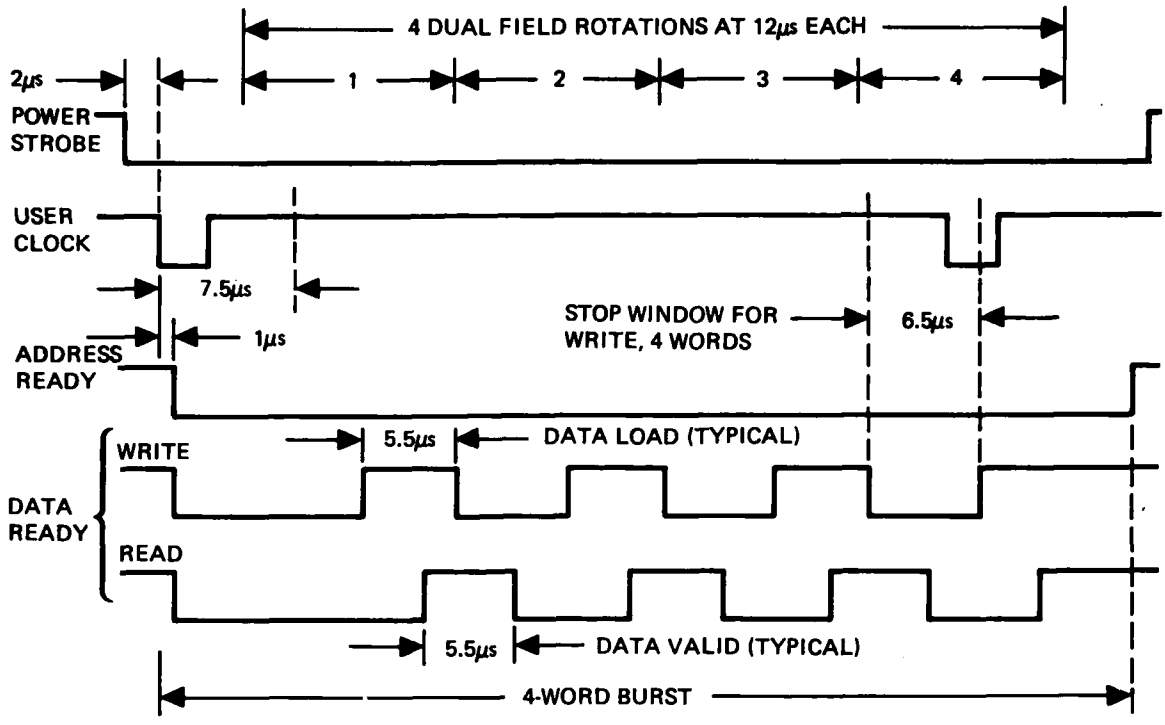


Figure 3-11. Burst access timing for a 4-word burst.

3.2.2 Dual Bus Structure

Two identical command and data interface buses facilitate simplified connection of the memory module to more than one user while providing an alternate communications path to the memory module in case one link becomes incapacitated. The approach is useful in large fault tolerant systems of which the memory module or modules may be a part. An example of an application facilitated by the dual bus structure is the use of one bus by spacecraft experiments or a data source and the other bus by telemetry. The experiment package controls filling of memory cells with data while the telemetry package controls dumping at an optimum time.

In operation a request on either bus gains dedicated control of the module if it is not busy. A later request on the free bus must wait for availability as indicated by Address Ready. The new user has 7.5 microseconds of priority, after which time the priority reverts to equality. If the dual bus feature is not required it can be unpopulated, saving approximately 8 ICS since it is an independent function.

4. D1106 CHIP DESIGN AND TEST

4.1 INTRODUCTION

The D1106 chip design shown in Figure 4-1 is a serial loop FIFO register with 102,400 bits of storage. Data are written into the loop with the "generator" which is the leftmost operator and are removed from the loop with the "transfer out" which is the second operator. Bubbles thus generated are transported along a periodic arrangement of permalloy elements having a period of 16 μm. They are driven by a uniform in-plane magnetic rotating field at a rate on the order of 150 kHz. A static bias field normal to memory element is required to stabilize the magnetic domains into cylindrical domains or bubbles.

Bubbles on the main track are "replicated" into the detector using the six element replicator which is the third operator. Conductors for operators are AL-CU and are placed close to the garnet under the permalloy. Bubbles in the replicator tracks are stretched along the detector chevrons in six strips of 50 elements each or about 0.3 mm in length. The domain strips are detected in a back-to-back full shorted detector configuration where the first detector bar is monocyclic with the generator and transfer out components. A dual detector arrangement is used so that adjacent bits can be alternated between the two thereby reducing adjacent bit overlap. Each detector is split into three sections reducing the amount of stretch which is especially important for the first bit detection. Conductors for detectors are permalloy.

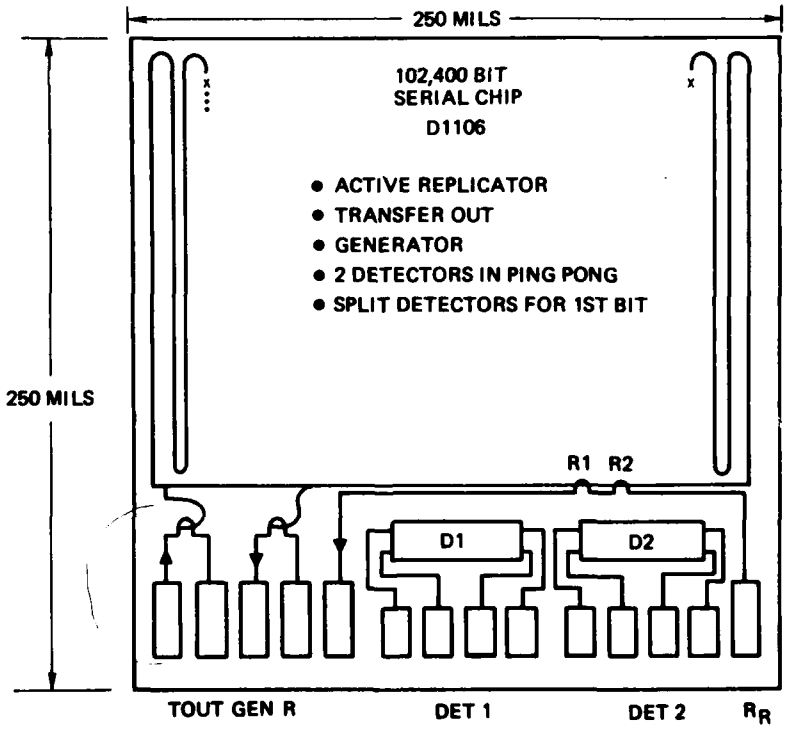


Figure 4-1. Bubble chip layout.

The D1106 chip design is a considerable improvement over the D1067 design used on the previous SSDR program [Ref 2]. The new design which has gap tolerant permalloy elements and a CaGe garnet material provides a wide bias margin over temperature and requires lower drive field. A comparison in bias margin and temperature performance for typical chips is shown in Figure 4-2. Operator phase and amplitude margin are more than sufficient for system applications. Evaluation of detector performance verified that detector redesign provides greater sense margin than its predecessor. Bubble signal has about the same amplitude but adjacent bubble overlap and zero signal balance have improved significantly.

4.2 CHIP DESCRIPTION

Fabrication of the D1106 is done using a two level process on garnet wafers. The fabrication sequence involves LPE growth of magnetic garnet film, deposition of an SiO_2 spacer which is then covered with a Al-Cu conductor layer. This conductor layer is etched to form generator and annihilator components of the memory element. After these conductor paths have been formed, another spacer layer is deposited followed by a layer of permalloy. The permalloy is masked and etched to form the propagation pattern and detector of the memory element. As a final step, the chip is masked to allow the second SiO_2 layer to be removed from the conductor layer at the bonding pad sites. Table 4-1 summarizes these various process steps used to form the memory element.

Memory elements used to generate, propagate, replicate, and transfer bubbles are shown in Figure 4-3. Asymmetrical chevrons are the main elements used to propagate bubbles through the register. Asymmetrical chevrons allow considerable gap tolerance which enhances yield and performance compared to the "H/I" pattern used previously. Furthermore, only one gap is required per bit of memory capacity whereas the "H/I" pattern requires two.

Generation of a bubble is done by nucleating with a pulse of current a magnetic domain which expands to a full sized bubble within a fraction of a cycle. Replication is accomplished by stretching a bubble into a strip around the curved element shown and then "cutting" it into two bubbles with a pulse of current. Cut pulse phasing is fairly critical because the strip must be aligned geometrically with the conductor at cut time. Otherwise bubbles fail to replicate, they may retard into the next bit time, or they may leave the path and enter the register somewhere else. Annihilation is done by transferring bubbles to an auxiliary path which leads to the guard rail where it merges with the edge domain structure. A low current of approximately 30 milliamps is enough to produce a field sufficient to attract bubbles to the auxiliary track.

Field directions and approximate operator and detection phasings are shown in Figure 4-4. Field rotates in the clockwise direction when looking into the chip's surface. Element design is optimized for best operation with the current fields directed as shown in the figure.

4.2.1 Fast Access Ping Pong Detector Design

Incremental read and write capability with fast access is desirable in systems designed for low power data logging or sequential control applications. An objective of this program was to achieve bubble detection during the first field cycle of a read operation whereas most bubble memory devices require several cycles of operation prior to detection. Data on conventional

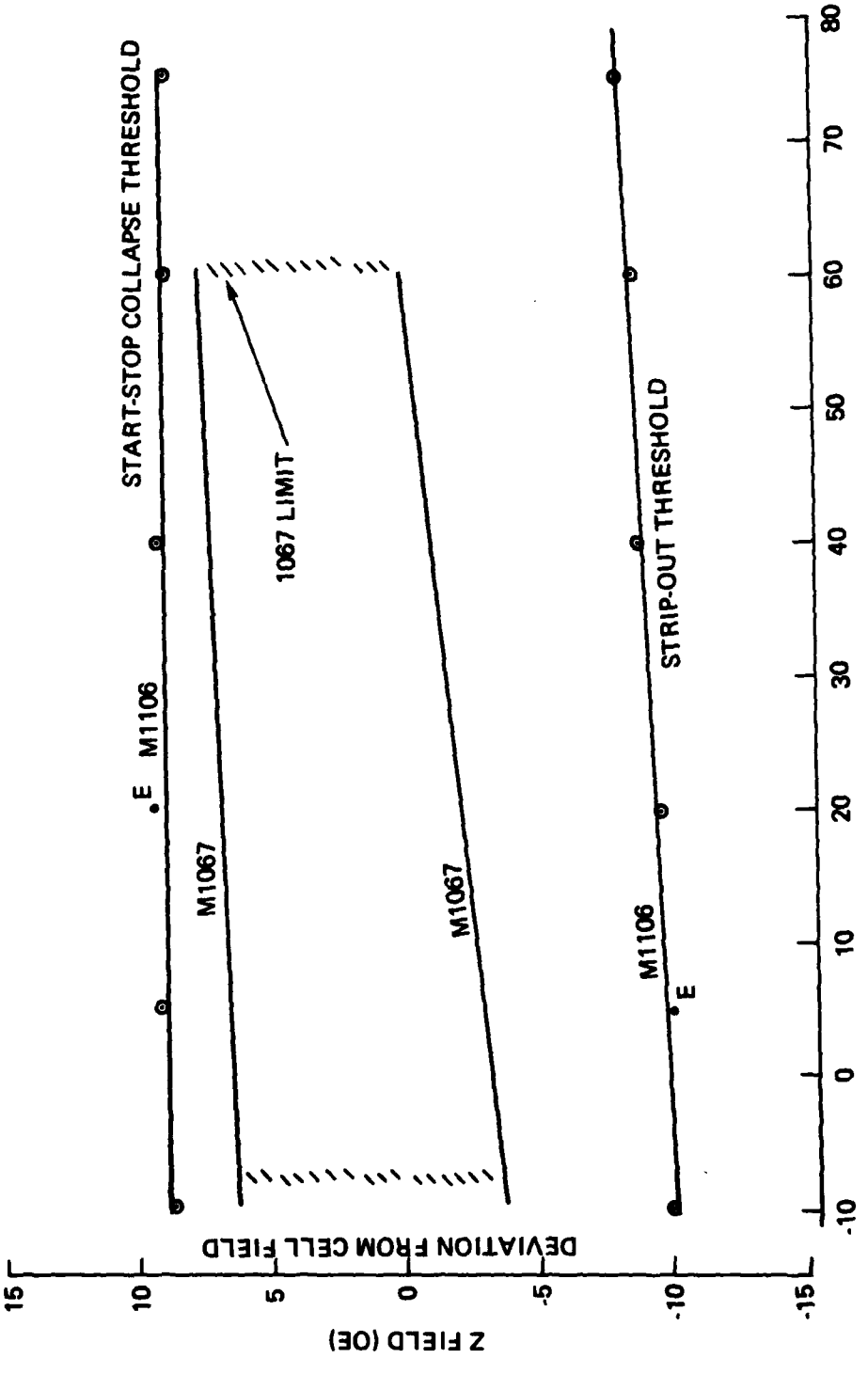


Figure 4-2. Device comparison.

TABLE 4-1. DEVICE PROCESSING SEQUENCE

Step No.	Thickness A	Material/Function	Technique
1	900	SiO_2 Spacer	RF Sputter
2	4,250	Aℓ-Cu Conductor	Electron Beam Evaporation
3	–	Conductor Pattern	Photolithography
4	–	Chemical Etch Aℓ-Cu	Immersion
5	6,000	SiO_2 Spacer	RF Sputter
6	4,000	Permalloy Propagate	RF Sputter
7	–	Propagate Pattern	Photolithography
8	–	Ion-Etch Permalloy	VEECO Microetch
9	–	Oxide Pattern	Photolithography
10	–	Chemical Etch SiO_2	Immersion

detectors of the type used for Rockwell's RBM256 four micron bubble devices shown in the lower set of curves of Figure 4-5 indicate that three or more cycles of coil precharge are required at 25C before reliable bubble detection can occur. Improvements were obtained by reducing stretcher length (middle curve) and by using a fast risetime precharge where coil resistance limits risetime. The split detector of Figure 4-6 was tested and found satisfactory in meeting fast turn-on requirements.

In this detector design three separate replicators feed each 50 element stretcher section so that each detector produces a signal identically timed with other sections. Test results show that the split detector design with enhanced coil precharge requires less than one half a cycle of precharge to achieve full signal amplitude at high Z bias and low temperature.

Other features of the detector design include an even and odd set of detectors (ping pong detection). The two sets which sense alternate bubbles replicated every other cycle reduce detection of bubble field from adjacent chevron stacks (bubble overlap). This reduces overlap from about 20% to less than 10% of peak bubble signal.

4.3 TEST RESULTS

Development of the D1106 design evolved from the D1067 design used on the SSDR. A partially populated chip (D1100) with gap tolerant elements was first designed and processed for evaluation. This chip has several small capacity tracks each with a different "handgun" corner and two versions of detector. Evaluation of this design uncovered a mask defect, a first bit detection problem, and established the back-back full shorted detector as the more desirable configuration. The D1106, incorporating design improvements, was processed by the Electronic Research Division in enough quantity for evaluation, to establish yield performance, and to populate four cells. A manufacturing yield run then followed. This section primarily covers evaluation results on the D1106 chip with pertinent results on the D1100 test chip.

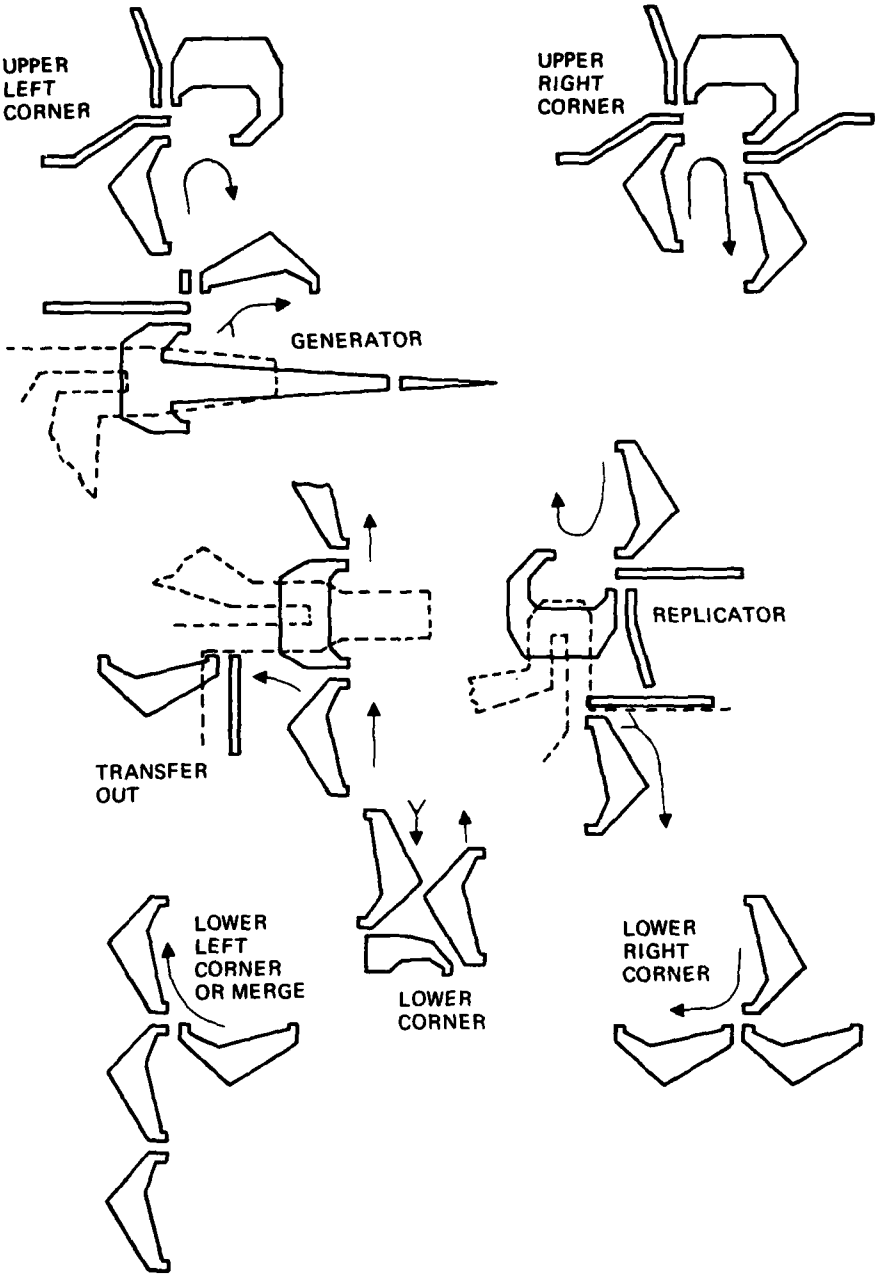


Figure 4-3. Memory elements.

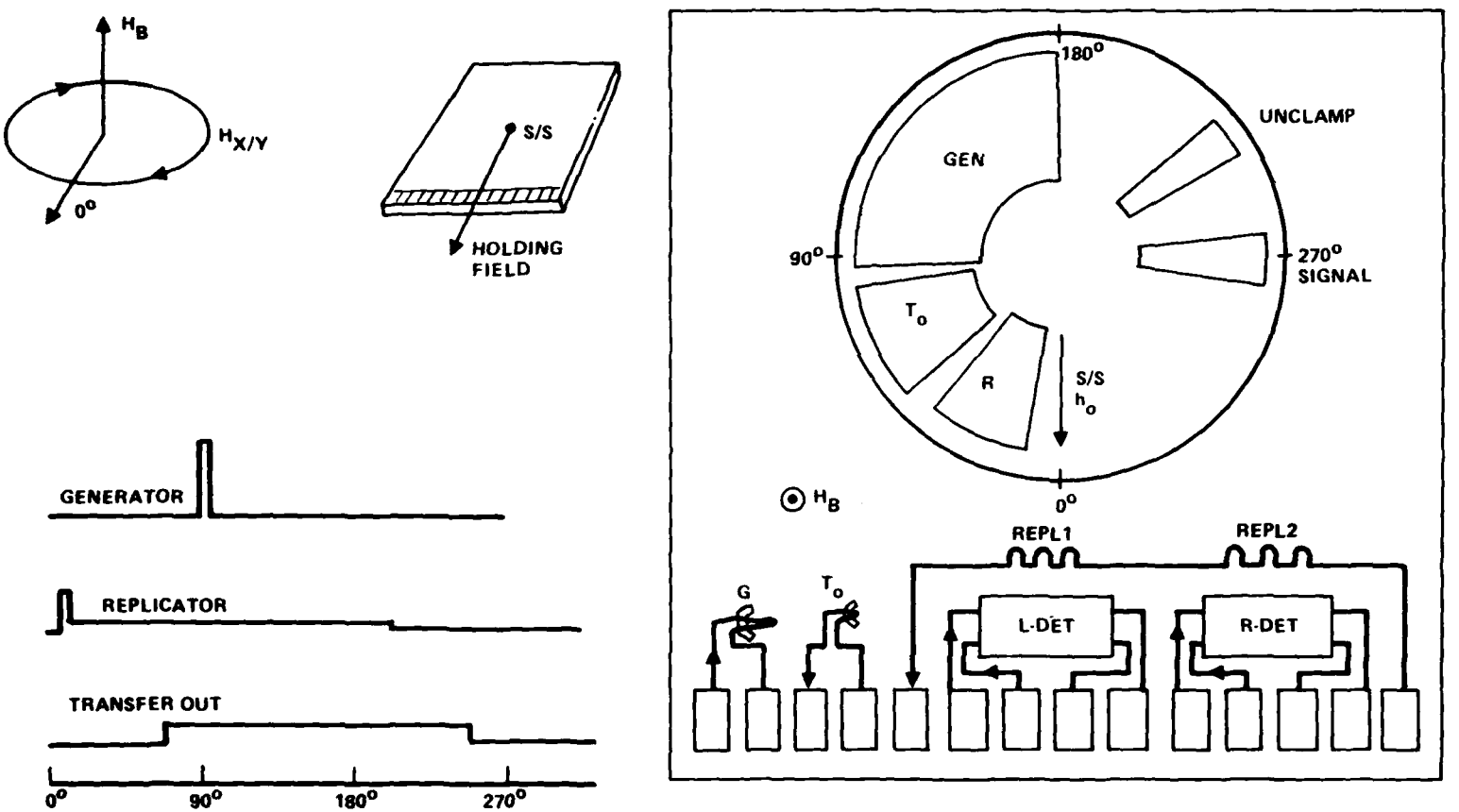


Figure 4-4. Chip timing and polarity definition.

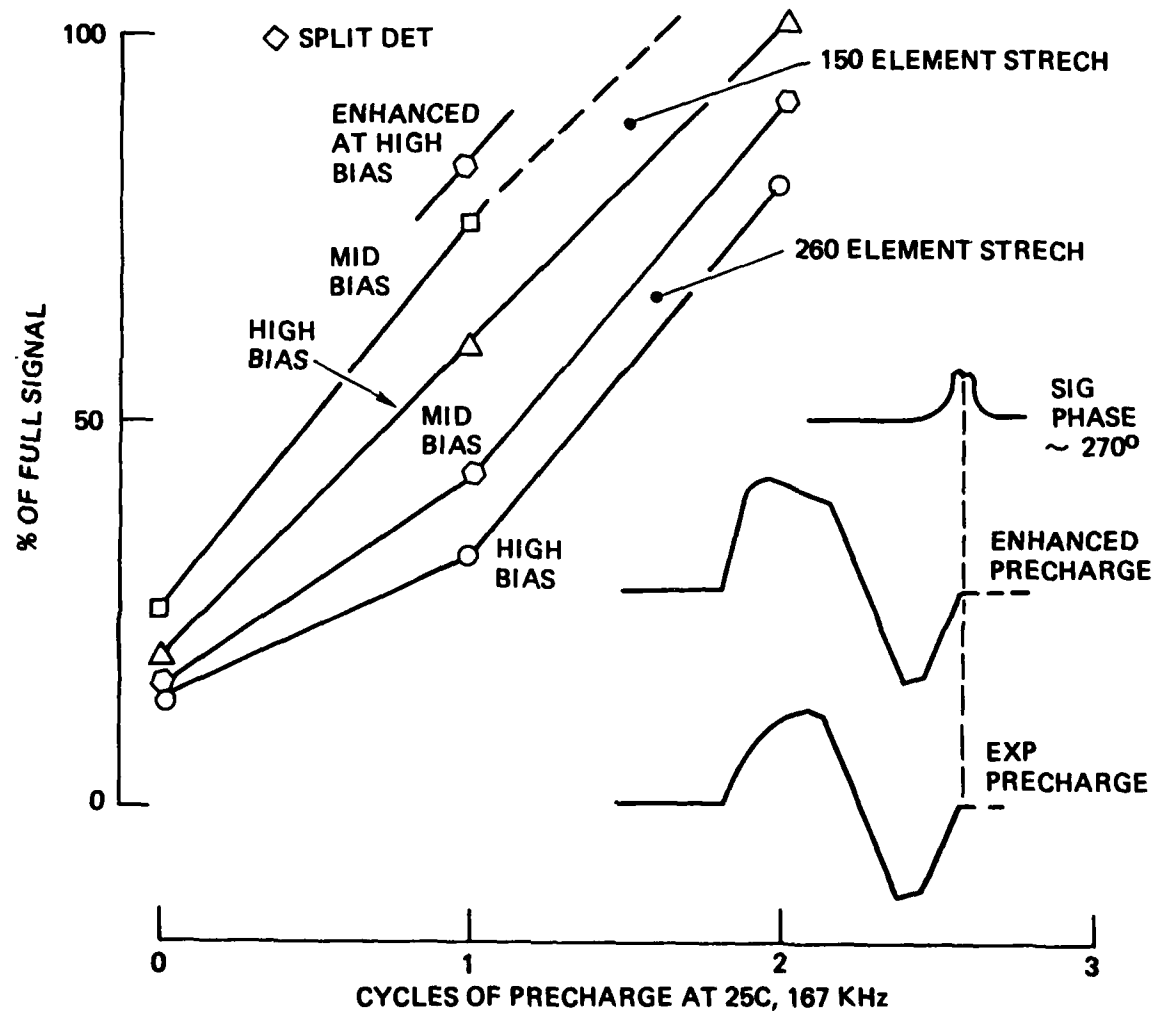


Figure 4-5. Stretcher detector performance.

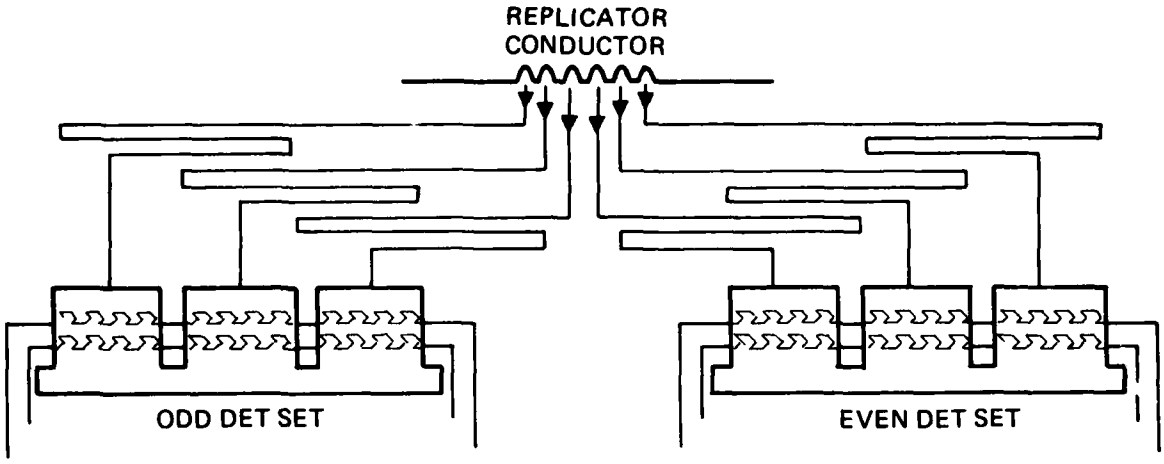


Figure 4-6. Fast access ping pong detection.

4.3.1 Propagation Test Results

Propagation margin is given in Figure 4-7. It was obtained under start-stop gated conditions where the full register was written with a data pattern and then read continuously in 15 or 16 bit words. The margin was found under these conditions by raising or lowering the Z bias from no error condition until hard errors occurred. The margins thus obtained are representative of the storage register and a few connecting elements but exclude detection, generation, and transfer out.

Several features are significant. Curl up of lower margin at high drive and decrease of upper margin at low temperature and low drive bracket the drive field margin for system application. The optimum drive appears to be between 40 and 50 oersteds or a nominal of 45 Oe ± 10 percent for system design. For extended temperature applications (<-10C), temperature compensated drive amplitudes or tighter drive tolerance will be of value. These margins were obtained using a trapezoidial drive waveform and a SSDR cell. Results are sensitive to the locus of the rotating field which depends both on coil characteristics (L/R ratio) and on applied waveform. Tracking of margin with cell bias is satsfactory with both having a variance of -0.19 ± 0.01 percent per °C.

Lower margin can be characterized a number of ways as shown in Figure 4-8. Stripout of an empty register gives slightly lower values than for gated margin of mixed "ones" and "zeros." A more conservative margin limit is where erasure of a register of striped out bubbles depends solely on the transfer out operator (upper curve). This presupposes that stripout occurs during abnormal operation of the memory and that the event must be anticipated either by incorporating Z axis erase hardware or by maintaining Z bias above the operator erase margin.

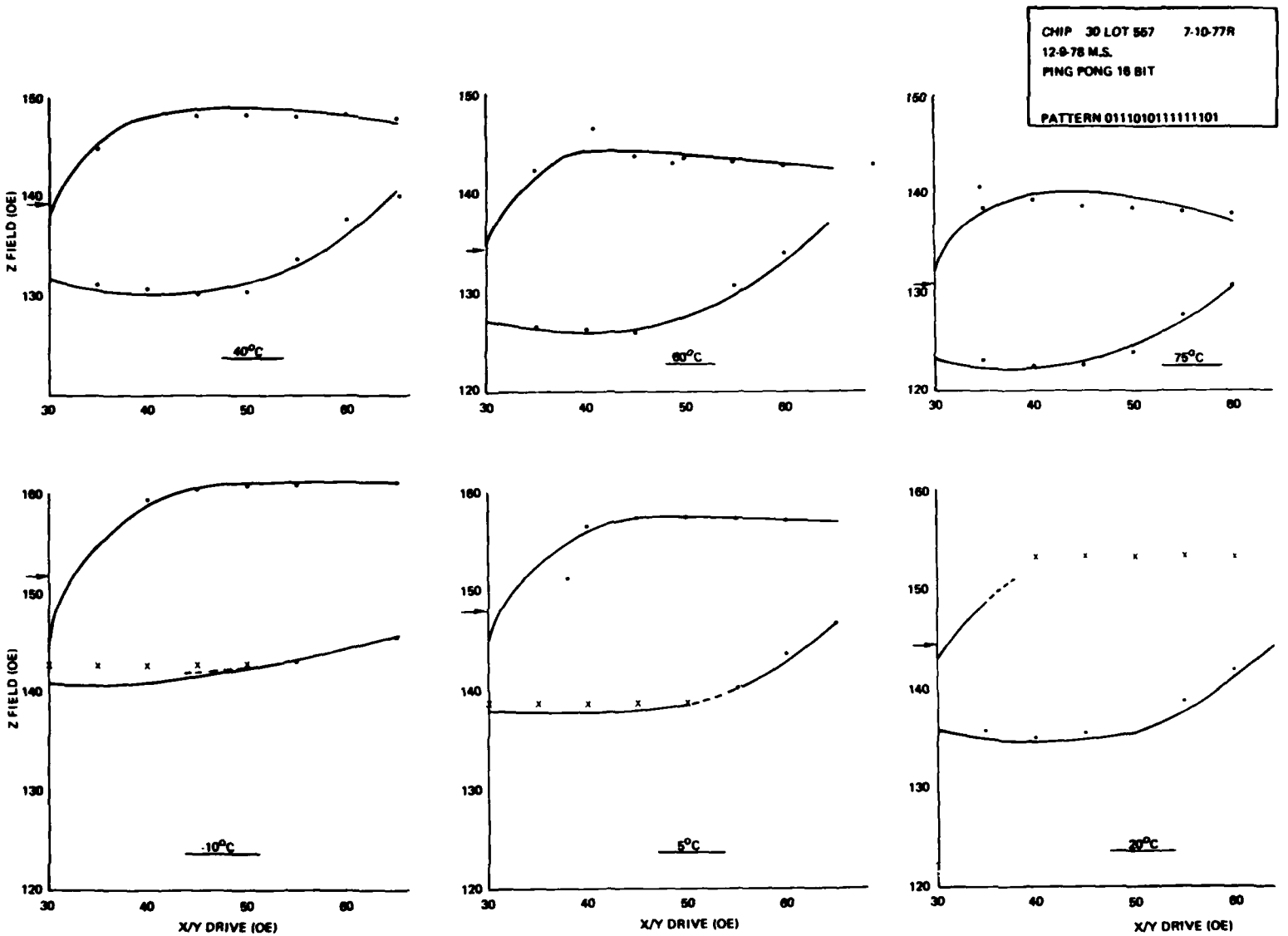


Figure 4-7. Propagation margin vs temperature.

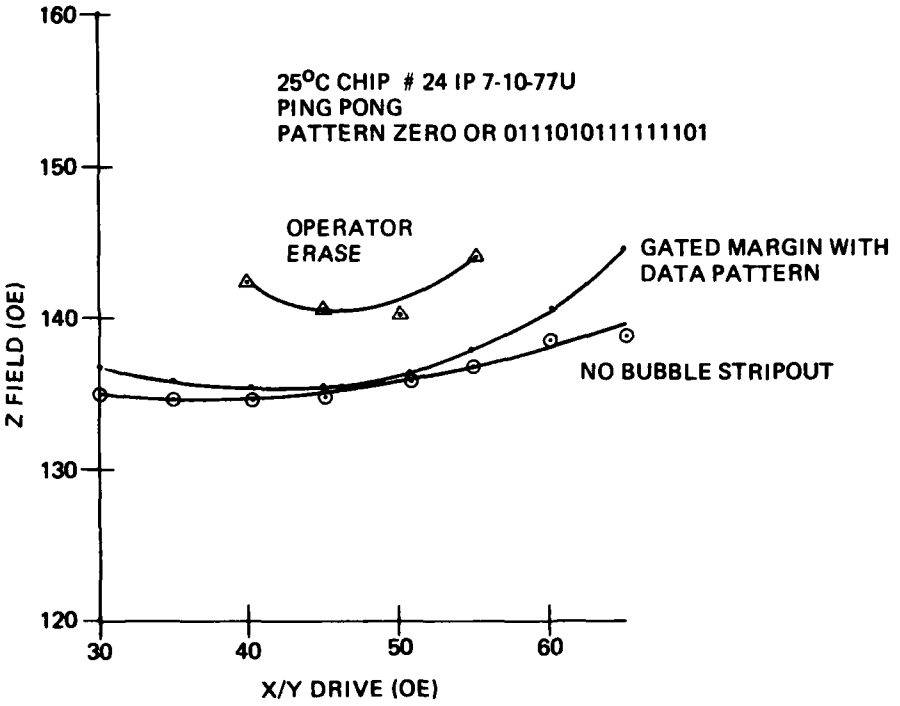


Figure 4-8. Lower margins.

4.3.2 Operator Margins

Bubble generation (Figure 4-9) has excellent margin in amplitude and in phase. Results indicate that compensation of amplitude is not required because 280 ma of current was applied without nucleation of spurious bubbles at 75C and only 195 ma is required at -10C, giving a comfortable margin for system operation. Statistical data obtained at the field runs (Section 6) show considerable variation in device generator amplitude requirements, which suggests compensation would be beneficial. Based on characterization results and the yield study, generator amplitude of 220 milliamp ± 10 percent with a temperature coefficient (tempco) of -0.4 percent/°C should be specified for system operation.

Transfer out operation is not critical in amplitude or in phase (± 10 deg) for a 180 deg pulsewidth. A wider pulsewidth (270 deg) provides improved phase margin.

Replicator amplitude and phase as given in the lower curves of Figure 4-9 are both satisfactory but need compensation for wider temperature operation and device to device variability. Cut pulse amplitude at high temperatures causes spurious bubble nucleation above 200 milliamp. A 25C value of 120 ma ± 10 percent with a tempco of -0.4 percent °C should be specified.

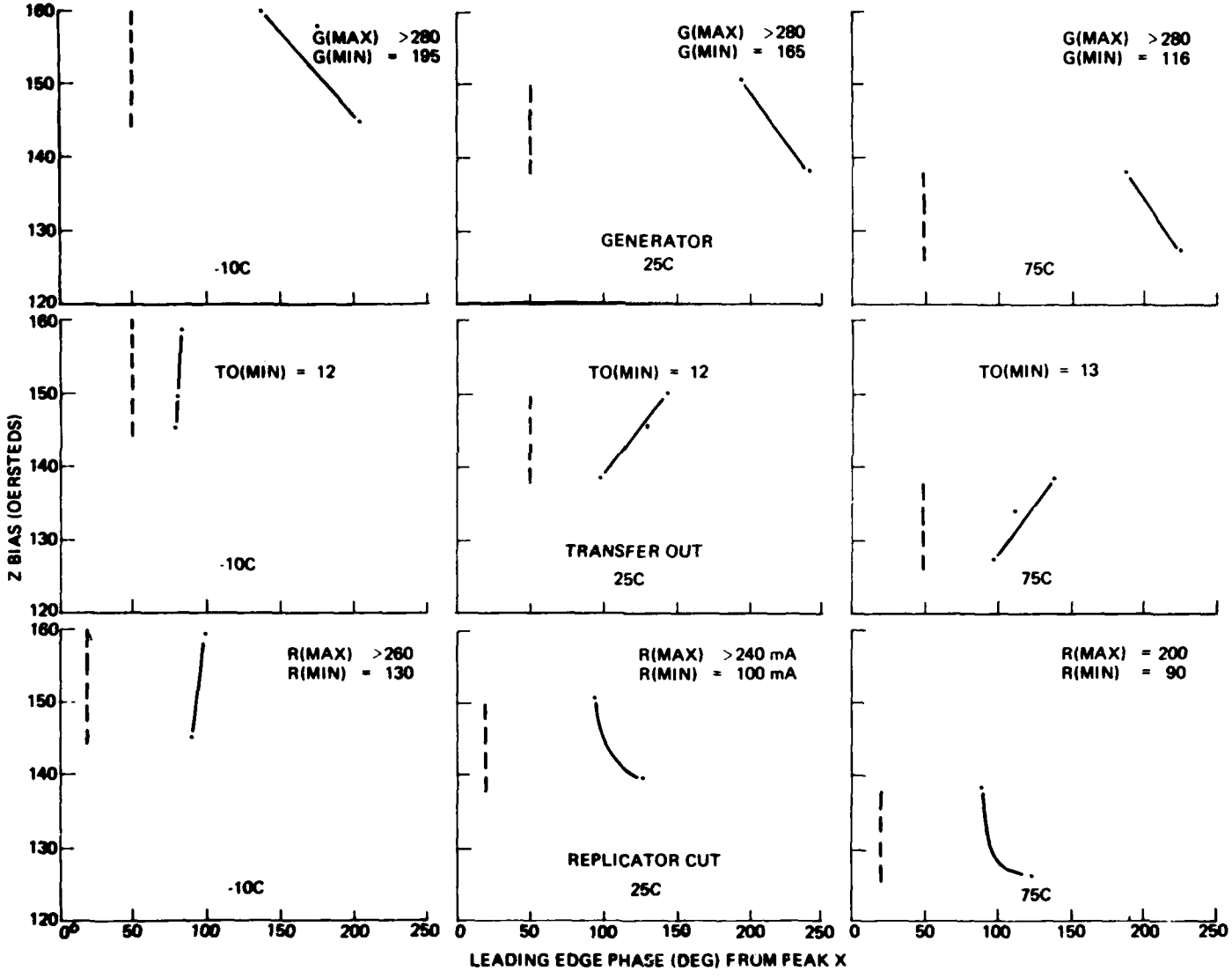


Figure 4-9. Operator margins.

TABLE 4-2 . OPERATOR CHARACTERISTICS

Function	Current Density	Pulse Width	Duty Cycle
Generate	9.66×10^6 A/cm^2	200 nsec	0.032
Transfer Out	1.13×10^6 A/cm^2	3.125 μsec	0.5
Replicate Cut	9.05×10^6 A/cm^2	200 nsec	0.032
Replicate Transfer	1.51×10^6 A/cm^2	3.125 μsec	0.5

Conductors used for the operator are aluminum with about 4 percent copper added for improved electromigration resistance. Table 4-2 summarizes current density, pulsewidth and duty cycle for the D1106 design. A simple lifetime test of 4 months was conducted on the replicators of nonoperating die at 25C to determine if a hazard exists. Eight chips were tested with a range of current from 80 mA to 195 mA at 100 kHz. No failures or changes in resistance occurred for the 10^{12} pulses even for the chips with 195 mA of current (10^7A/cm^2). Published data [Ref 4] on electromigration effects in bubble memory devices indicate generate and replicate cut operators should have lifetime greater than 10^{15} operations or 10^7 hours.

4.4 DETECTOR CHARACTERIZATION

Detection for the D1106 design uses a full shorted back-to-back chevron detector chosen for its stability and convenient signal phasing. As shown in Figure 4-10, two detectors are used for alternate bit detection which reduces overlap signal. Each detector has three sections to improve first bit detection. Figure 4-11 is the signal signature of the detector. The bubble strip and its signal influence can be traced through the detector as follows. On the left, the bubble is at the chevrons in the start/stop direction at 0 deg just prior to entering the active detector. There is no change in strip position until about 135 deg into the cycle when it moves to the first detector. At 180 deg magnetoresistance change for a bubble strip is greatest because the strip is directly under a shorting bar where bubble field and detector current is mostly orthogonal. As the bubble strip moves across the detector, output decreases partly because bubble field and detector current are more aligned with each other and partly because of retardation of local fields by the bubble strip. Another peak occurs when the bubble strip is at the output shorting bar. Exactly the same process occurs in the dummy detector except that signal polarity is reversed because of differential sensing.

Magnetoresistance signal pickup of the bubble strip after leaving the dummy detector (overlap) still occurs but with less impact than the previous 1067 design. Cycle three has a signal at 180 deg which will subtract from an adjacent bubble strip signal. This can be avoided in redesign by choosing the second detector as the active detector. Figure 4-11 was obtained using sine wave drive at 50 Oe at room temperature.

Signal stabilty versus drive field for a trapezoidal drive waveform is shown in Figure 4-12. Noise is excluded as a variable by plotting the difference between a baseline without bubbles and a baseline with bubbles to obtain only bubble influence. Notice that signal signature of the trapwave has significantly higher frequency component and a subdued 0 deg peak compared to sine wave drive. Stability of peaks for drive field variation is important in system application. These are plotted in Figure 4-13. Phase stability for peaks "a" and "c" appears satisfactory for

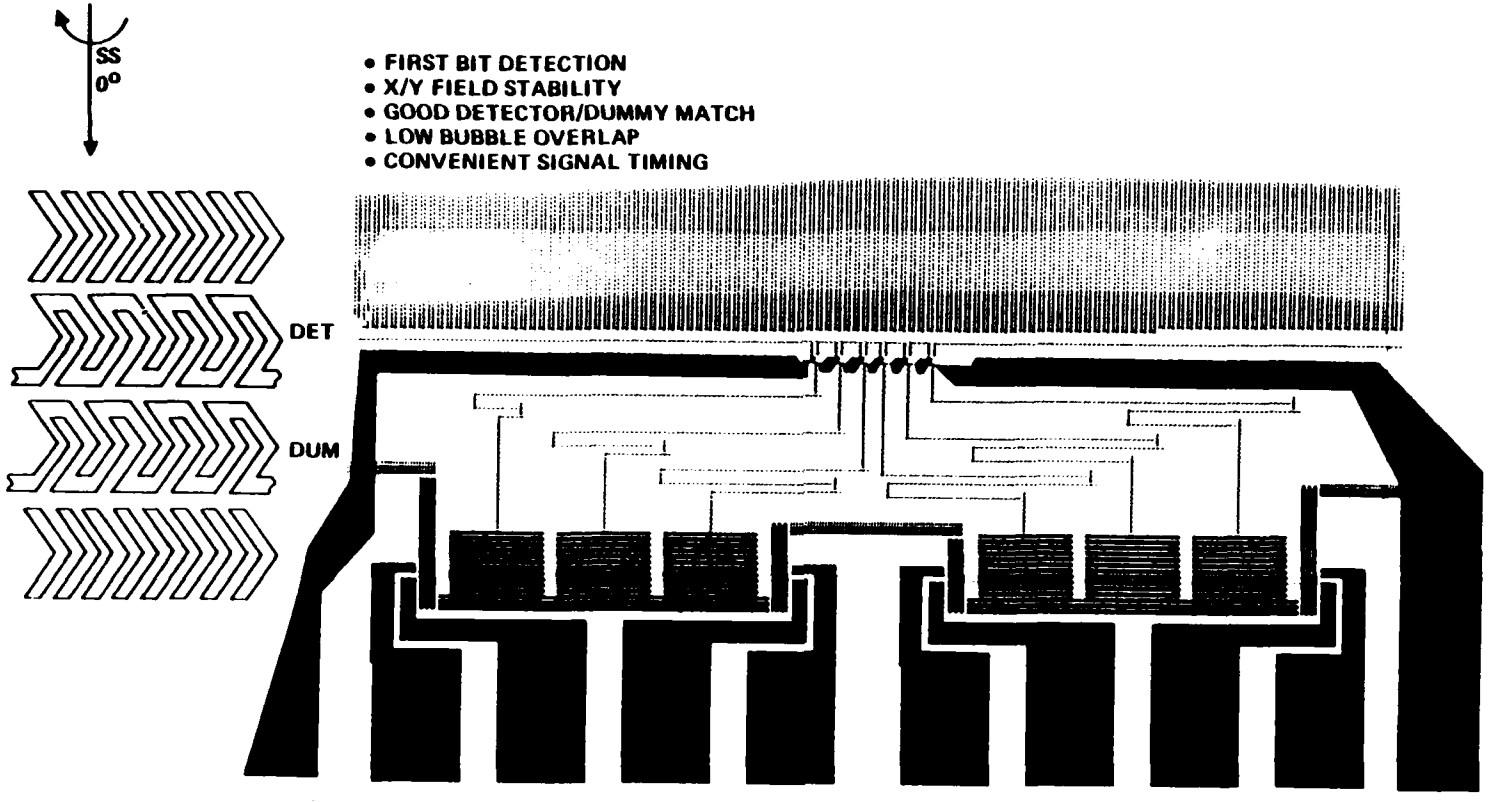


Figure 4-10. Back-to-back detector design.

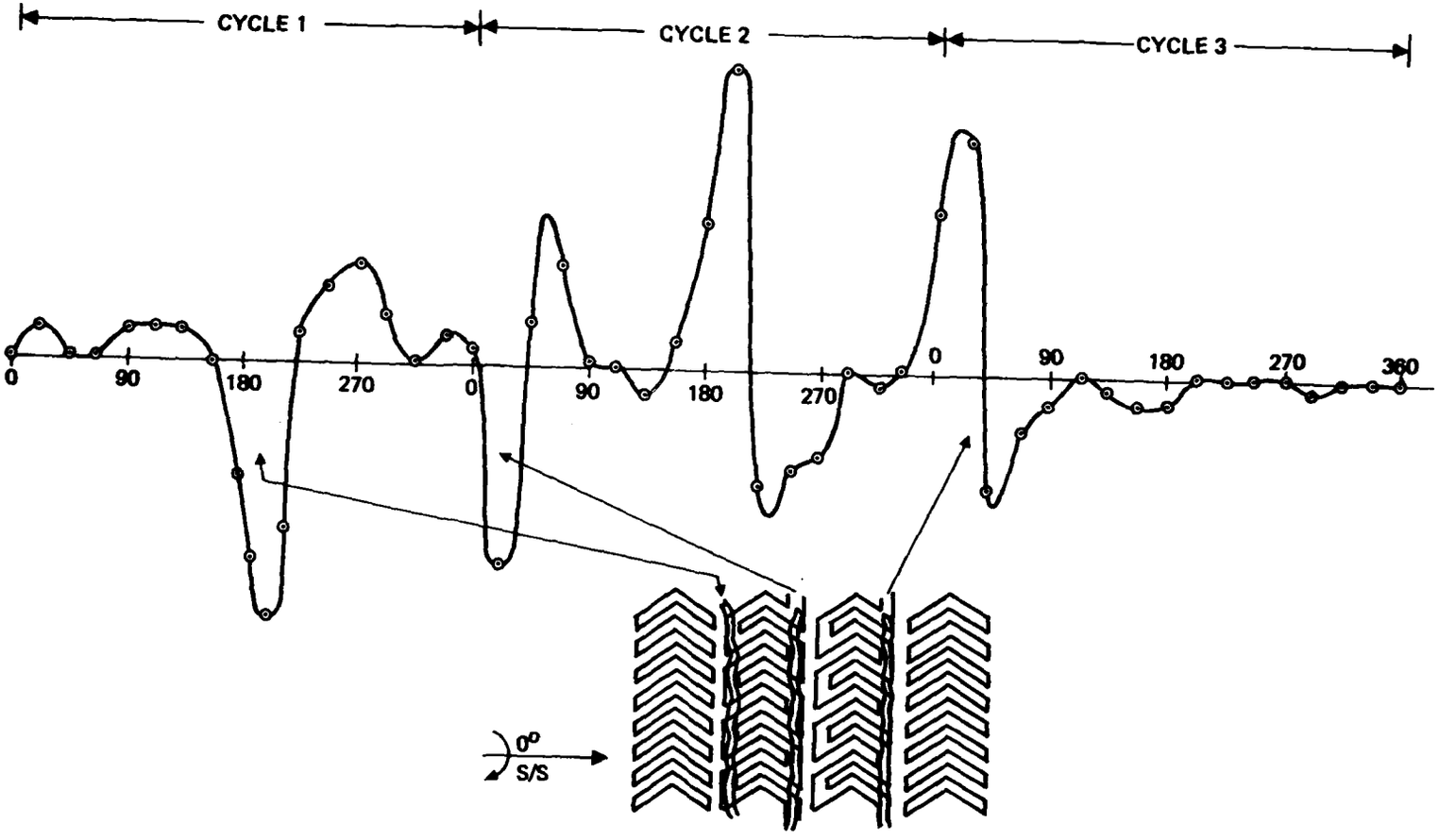


Figure 4-11. Bubble influence on the detector (50 OE sinewave drive).

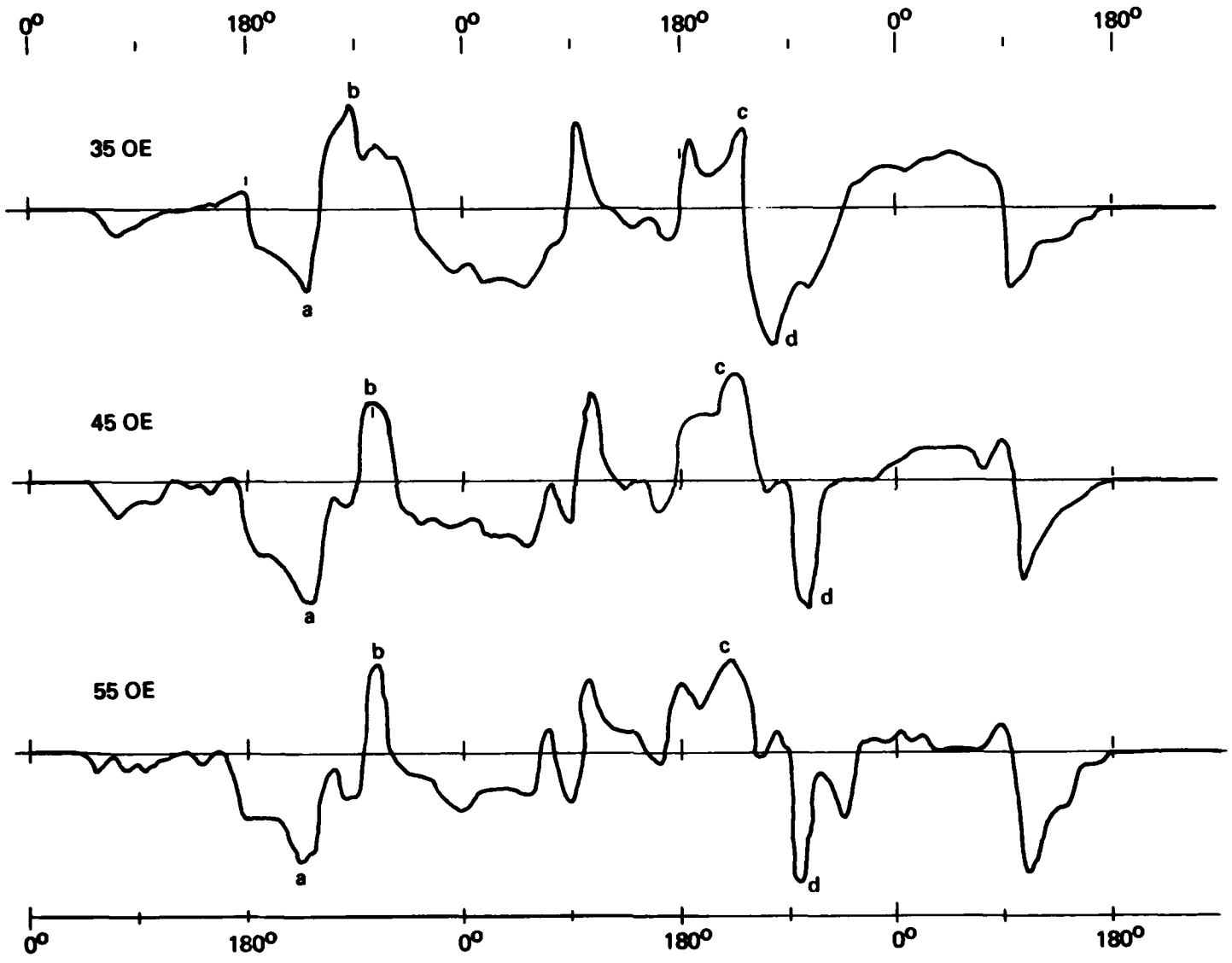


Figure 4-12. Bubble signal waveform vs drive (25°C) 1106 chip.

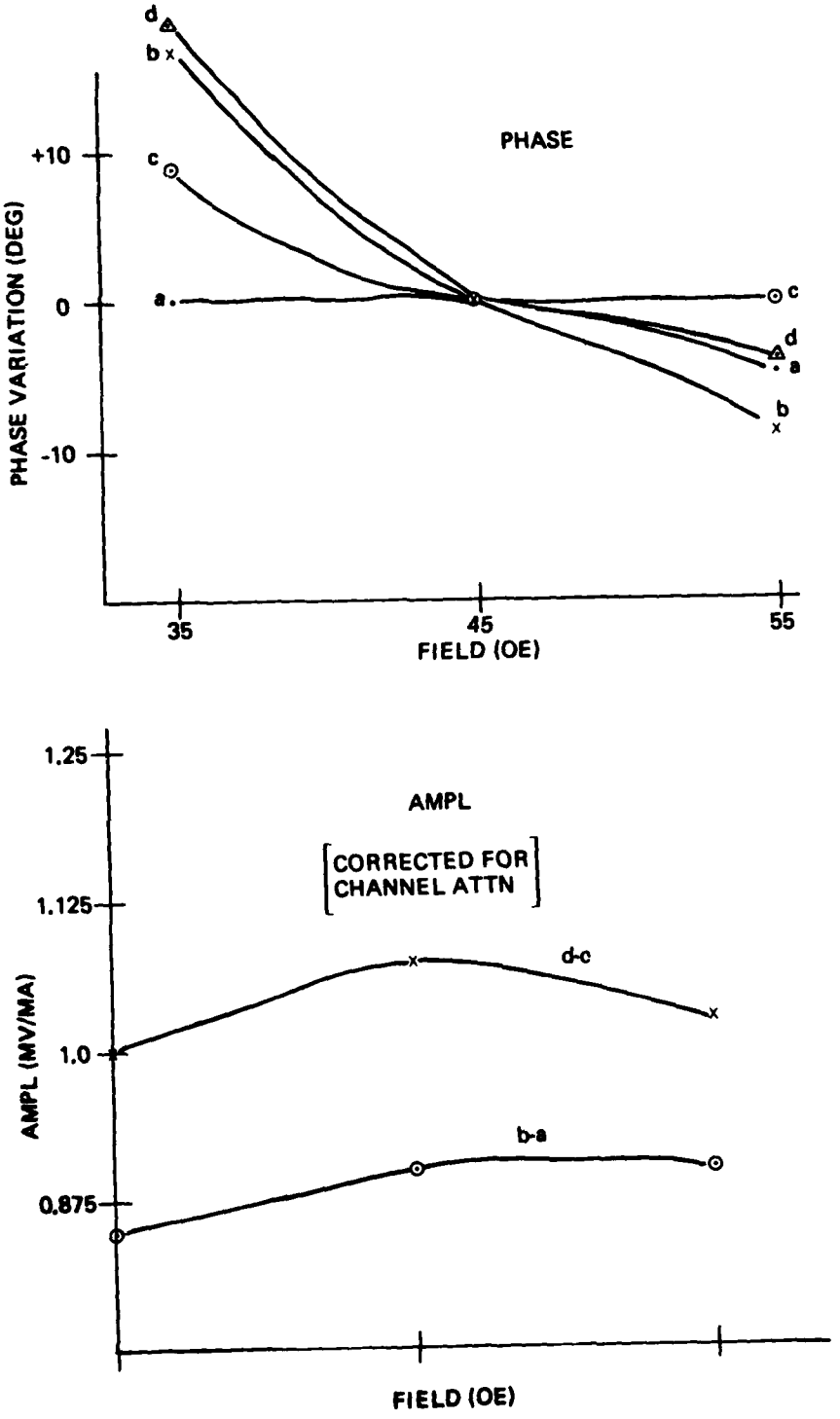


Figure 4-13. Signal stability vs drive.

drive field tolerance of ± 10 percent while peaks "b" and "d" vary excessively particularly for low drive field. A peak detector is desirable in system application. Amplitude stability appears excellent.

Other detector configurations such as the "F" detector and the "half shorted" detector were evaluated for implementation in the design. Although the F detector had greater signal amplitude, its stability (especially amplitude stability) was found inadequate. Overall the full shorted back-back detector seemed to be the best choice of detector designs for the D1106 chip.

Another property of interest is detector sensitivity versus detector current for pulsed bridge detection which is shown in Figure 4-14. A number of detectors were tested using both current polarities. For current amplitude below 18 milliamps and 30 percent duty cycle sensitivity is roughly constant. Above this value which corresponds to approximately 30 milliwatts of dissipation, detector sensitivity begins to drop significantly. A 10 to 13 mA specification limit provides a safe margin for temperature and production variations.

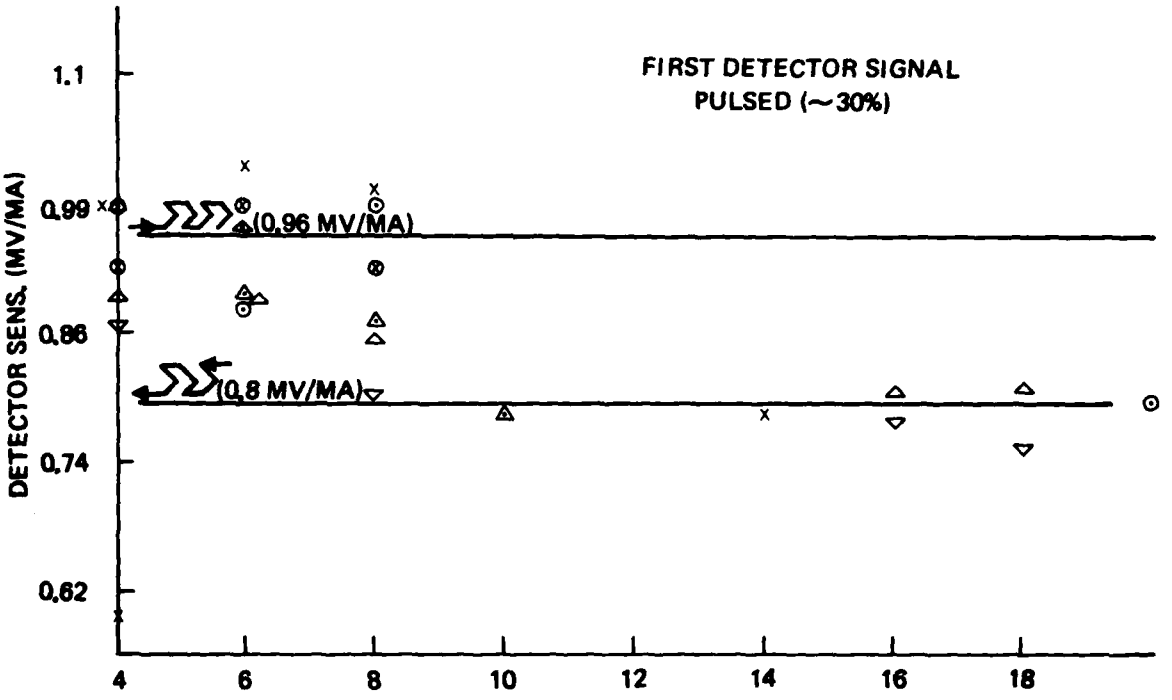


Figure 4-14. Detector ampl vs detector current and direction.

5. MEMORY CELL DESIGN AND TEST

5.1 CELL DESCRIPTION

Basic bubble memory storage is provided by the memory cell shown in Figure 5-1. The memory cell contains eight 100K bit bubble memory chips and the magnetic circuits elements required to operate them.

The eight chips are mounted on two ceramic hermetically sealed chip carriers, stacked and inserted into the cell. The memory cell contains two orthogonal coils to generate the rotating field and a permanent magnet assembly to generate the bias field. The photographs, Figures 5-2 and 5-3 illustrate the principal components of the carrier and cell assemblies.

The cell is operated such that all chips are accessed in parallel. With a rotating field rate of 166 kHz, the cell can be read or written at 1.33 Mb/s.

Principal components of this cell include eight bubble chips, hermetic chip carriers, X-Y coils, ferrite field spreader plates, ceramic bias magnets, and a permalloy shield keeper. The overall physical and electrical characteristics of the cell are summarized in Table 5-1.

The 8 x 10^5 bit cell magnetics assembly as shown in Figure 5-4 utilizes a double open-ended X coil which is unique in that it is a wound assembly and has rectangular magnet wire to minimize dc resistance. Details of this coil assembly are shown in the photograph, of Figure 5-5.

The carrier assembly provides total environmental protection for the chips as they are enclosed in a ceramic hermetic cavity which is sealed by glass and indium interfaces. Details of the various seal interfaces are shown in Figure 5-6. Interconnect to the carriers is from both ends to facilitate minimum noise circuit geometry at the memory module level.

The two carriers are precisely located and locked into the cell by end cap hardware which is part of the magnetics assembly, as shown in Figure 5-1.

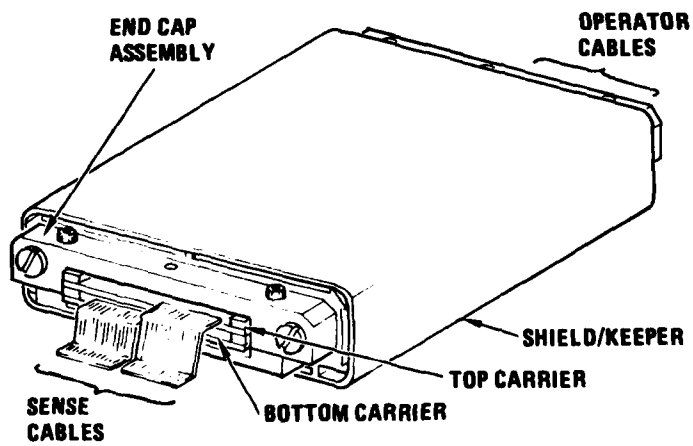


Figure 5-1. 8 x 10^5 bit cell assembly.

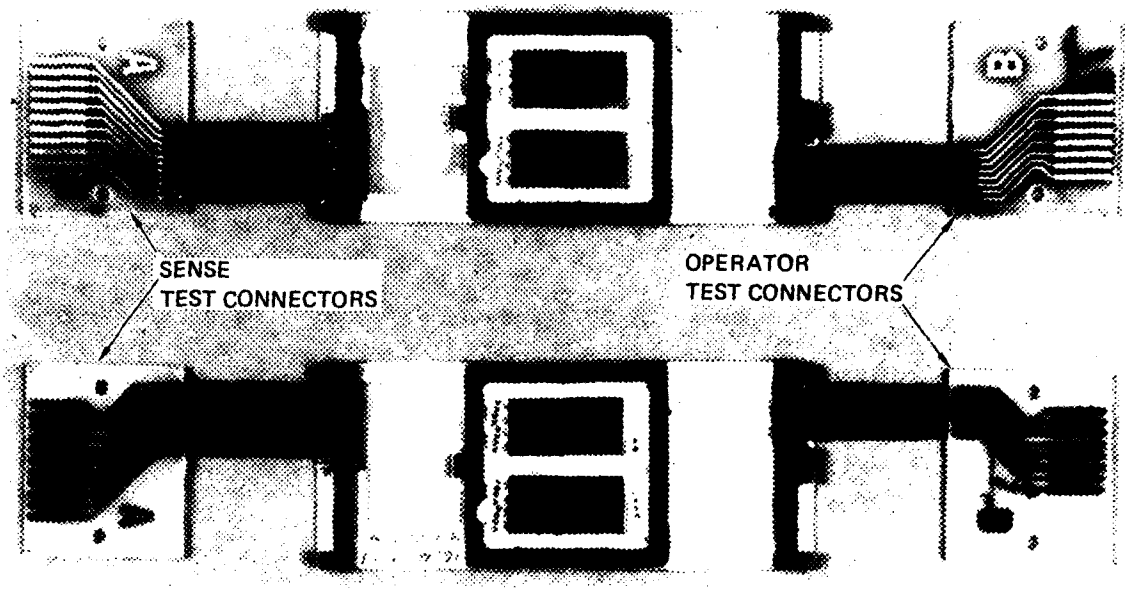


Figure 5-2. Upper and lower chip carrier assemblies

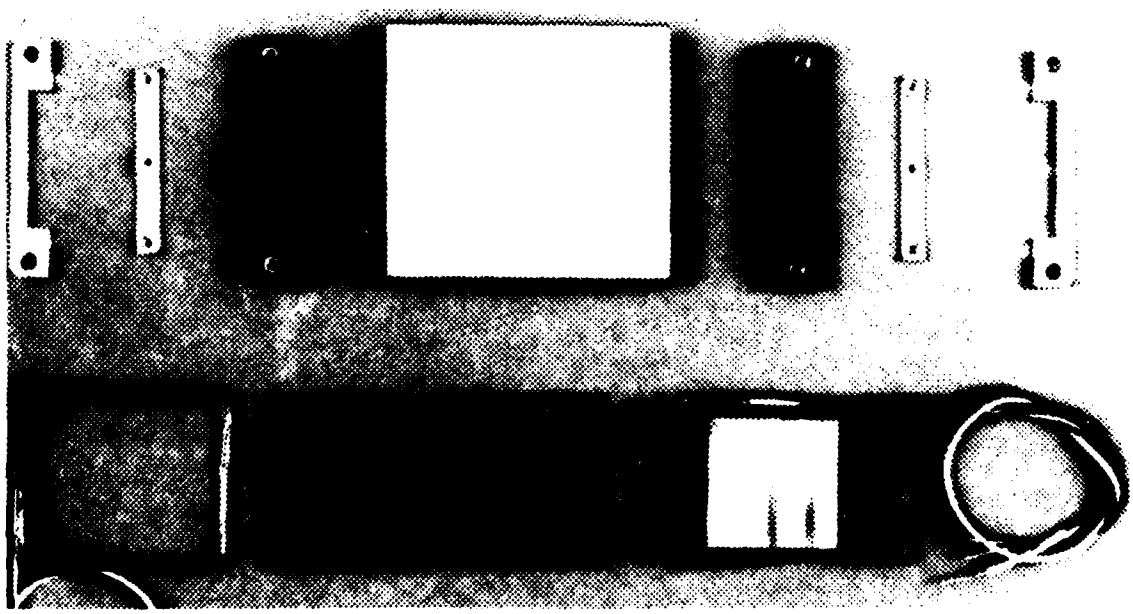


Figure 5-3. Cell magnetics components and carrier alignment end cap hardware.

TABLE 5-1. CELL CHARACTERISTIC AND PERFORMANCE SUMMARY

CELL ASSEMBLY		
Storage Capacity	8.2×10^5	Bits
Number of Chips	8	ea
Drive Frequency	166.6	kHz
Data Rate	1.3×10^6	Bits/sec
Power Dissipation	6.2	watts
Weight	100 (0.22)	GM (lb)
Size	5.6 x 4.3 x 1.3 (2.2 x 1.7 x 0.51)	CM (in)
Volume	31 (1.9)	CM^3 $(in)^3$
ENVIRONMENTAL PERFORMANCE		
Operating Temperature	-10 to +75	C°
Survival Temperature	-40 to +85	C°
Sine Vibration	50	G
Random Vibration	1.0	G^2/Hz
Shock at Q = 10, F = 2000 Hz	2000	G
Acceleration	33	G

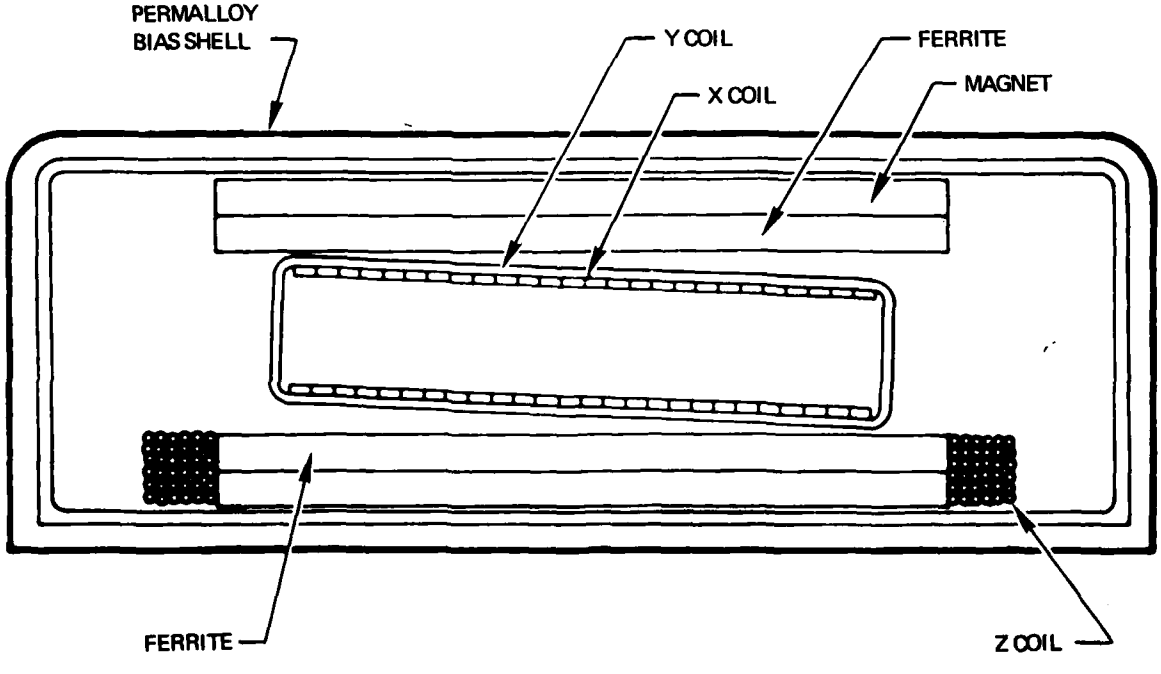


Figure 5-4. Magnetic assembly configuration.

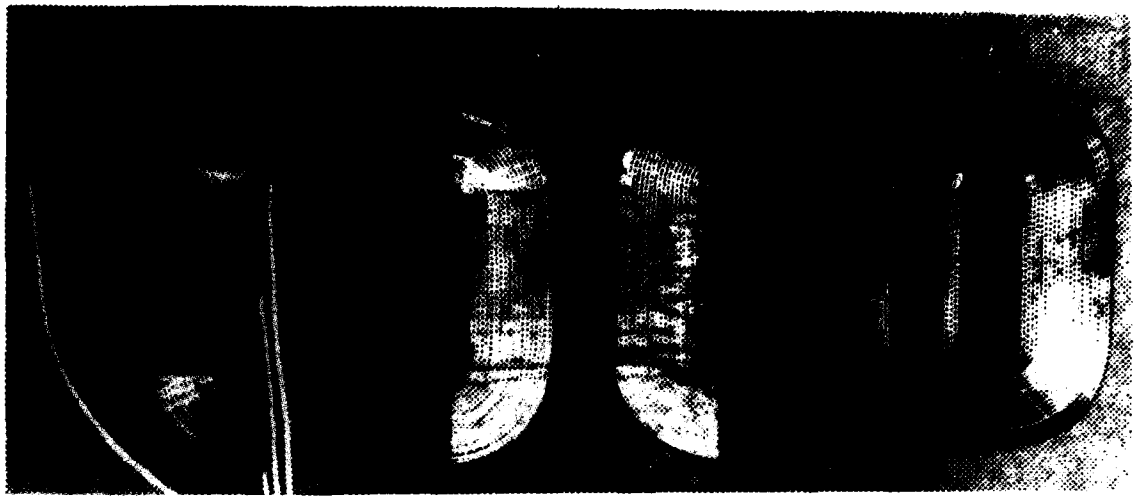


Figure 5-5. X-Y coil assembly and open X coil details.

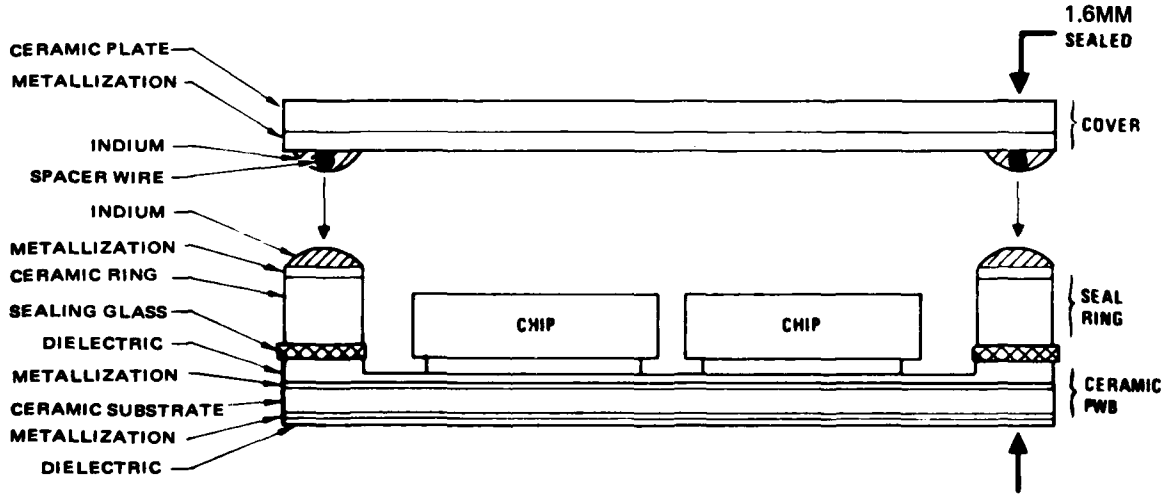


Figure 5-6. Hermetic carrier section.

5.2 CARRIER DESIGN

An exploded view of the dual carrier assembly is shown in Figure 5-7. Four 100 kilobit serial chips are mounted face down on each carrier as illustrated. Principal components of each carrier include the aluminum oxide thick film metallized printed wiring board (PWB), front and rear epoxy glass spacers, 22 beam leaded selection diodes, aluminum oxide seal ring, solder preform and an aluminum oxide cover. Chips are adhesively bonded active surface down on the ceramic PWB. Interconnect from the chip to the PWB is through 0.7 x 3 mil beam bonds. This interconnect geometry is highly planar minimizing inductive pickup of rotating field noise into sensitive detector circuits.

The aluminum oxide PWB has two layers of gold thick film metallized circuit conductors on the front side and a gold thick film metallized ground plane on the back side. Interconnect to the PWB is from both ends to implement physical isolation of the detector and operator functions at the carrier and system level.

Detector conductors are 5 mils wide on 10 mil centers and are routed under the chips, to beam lead diodes which connect to terminations on one end of the PWB. These conductors are laid out as differential pairs and are flanked by 5 mil wide guard lines along most of their length. All detector lines are on the first metallization layer and are shielded by the back side ground plane.

Detector line paths from the edge of the chip field to the PWB terminations have additional shielding implemented by a second ground plane which is part of the second level front side metallization. The operator circuit conductors are laid out along the outside perimeter of the chip field and are terminated to pads on the opposite end of the PWB away from the detectors.

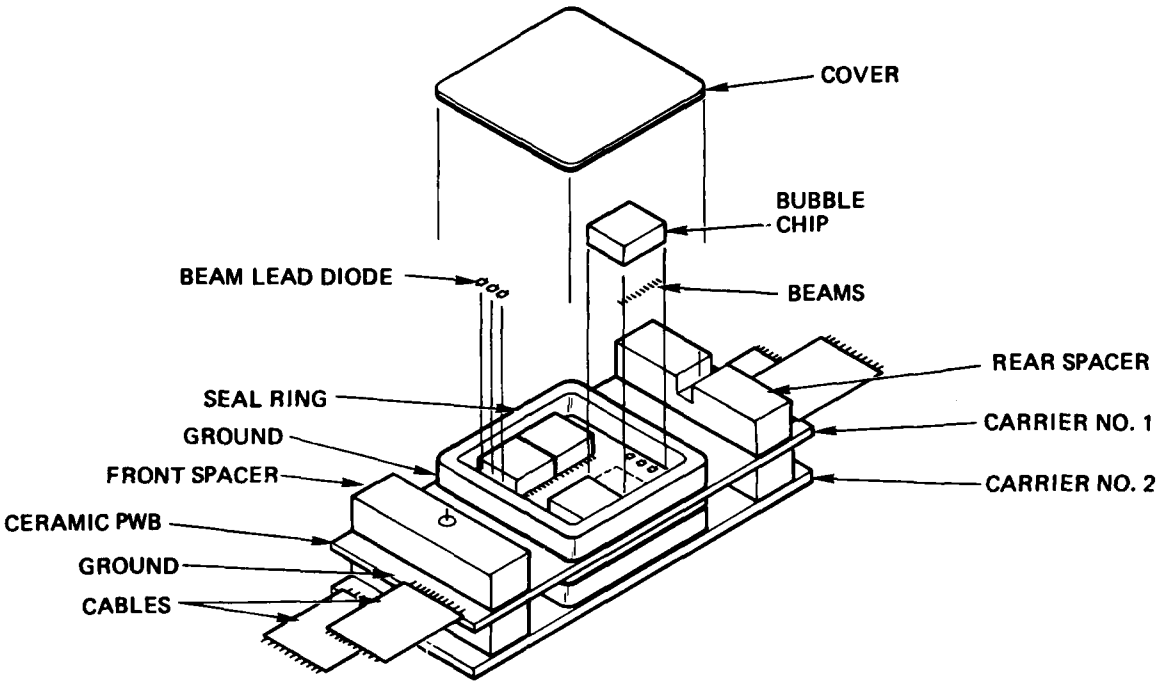


Figure 5-7. NASA 8 x 10^5 bit dual carrier assembly.

This conductor/ground plane layout geometry effectively separates the detector circuits from the operator circuits and minimizes reception of cross coupled noise.

The two PWB's required have identical layouts in the chip field area; however the termination pads are offset to the right of center on the top and the left of center on the bottom PWB. This offset is implemented to eliminate interconnect cable crossover and simplify fan out geometry to the multi-layer board.

An aluminum oxide ring is glass sealed to the ring dielectric on the PWB. Once chips have been mounted and have passed acceptance testing, a metallized cover is solder reflowed to the seal ring as shown in Figure 5-6 to provide a hermetic chamber for the bubble chips.

Major considerations in the design of the carrier include a hermeticity requirement (described in Section 5.6), Power dissipation, and noise. As far as carrier design is concerned, power dissipation in minimized (also the volt amp product) by minimizing volume of active chip area by reducing space between chips and space for covers and PWBs.

Inductive and capacitively coupled noise is a major concern in bubble chip packaging. Sources of inductive coupling ($d\phi/dt$) are the chip bond leads, PWB surface sense conductors inside the coil, and the conductors as they egress from the coil. Area between differential conductors exposed to the rotating field vector produce a sense line voltage proportional to frequency and to field magnitude. Face down bonding of beam leaded bubble chips ensure low and consistent pickup while minimum area between sense conductors inside the coil virtually eliminates $d\phi/dt$ pickup except from the leads as they egress from the coil. At the coil egress a Z component of the rotating field creates $d\phi/dt$ pickup of one polarity above center plane and of opposite polarity below center plane. The two carriers in the cell are well balanced so that $d\phi/dt$ pickup is on the order of 0.2 millivolts during signal time but opposite in polarity between carriers.

Capacitively coupled noise (cross coupling) is a rate of voltage change pickup from the coil to the sense leads. Very small currents flow into detectors to produce unbalanced or differential voltage at the sense amplifier input. Control of the currents involves electrostatically guarding the differential sense conductors. Since the noise is proportional to the second derivative of the coil current, the noise becomes a severe aggravation as coil operating frequency is increased and for trapezoidal or triangle wave forms which have high frequency components. Placement of the electrostatic guard relative to the coil and conductors and impedance control to system ground are important factors in the design.

Establishing the number of carriers for eight chips is relatively straightforward. A single chip carrier has minimum total parts and associated assembly costs but requires a chip mounting area which is large enough for eight chips. This requires a drive coil and bias structure large enough to provide a uniform field over the eight chip area. Driven area can be reduced by 50% when the chips are packaged on two carriers, each having four chips. Four or more carriers could also be used but, the combined carrier thickness and increased interconnect difficulty would offset the efficiency gained by using two carriers. Based on this a two carrier design was adopted for the cell.

To reduce the number of carrier interconnects, the two detectors of each chip are multiplexed at the carrier level with an array of diodes. As these diodes are in the rotating field it is necessary that noise pick up be minimized and thus planar beam lead diodes are used as in the earlier SSDR design.

In terms of the total package, hermetic sealing is required to assure reliable operation after exposure to high humidity with condensation. Such condensation may result in damage to both lead bonds and the memory chip if the cell interior is not protected. Options available include sealing the entire cell in a hermetic enclosure or sealing at the bias shell level. Sealing at the carrier level was ultimately adopted in order to complement the final interconnect design and minimize polymeric material constraints.

An epoxy glass laminate plate having a central rectangular aperture is adhesively bonded to the PWB and serves to space the two carriers apart and increase the strength of each individual carrier. A small hole in one end of the plate (and PWB) is provided for pin alignment (Y axis) of the carrier to the cell magnetics.

Polyimide insulated etched and gold plate copper flexible cables are solder-terminated to each end of the carrier PWB.

5.3 CELL MECHANICAL CHARACTERIZATION

Experience with the earlier solid state data recorder (SSDR) 1.64×10^6 bit cell pointed to the necessity for improvement of operating margin, reduction of coil power, volt amp product, parts count and complexity. The number of memory elements to be packaged in a memory cell is a function of a number of considerations. Included in these are weight, volume, power, data rate and device yield. At a minimum, a cell must contain sufficient memory elements to allow delivery of the required data rate. Although two or more cells may be operated in parallel to obtain a given data rate, it would require additional coil drive components and is undesirable from that standpoint. The system requirement on data rate is 1.33 Mb/s (instantaneous). The minimum allowable number of chips per cell is established by this requirement in combination with the drive field frequency at which the cell runs. A drive field of 166.6 kHz was selected as being consistent with good bubble chip operating margins, efficient drive circuit operation, and low thermal gradients. With this field rate, the data rate requirements are met with eight or more chips per cell.

The greater the number of chips in a cell, the more difficult it is to obtain well matched bias margins from a given chip population. Increased chips per cell will result in reduced composite cell bias margin as compared to the individual die.

To illustrate this trade off, wafer level test data taken on 128 memory elements was used to establish how composite cell bias margin varies with number of chips/cell. Measured bias margin of the die was used as a sorting criteria to divide the 128 memory element into groups representing cell populations ranging in size from one to 16. This sorting was done in a manner to obtain best possible overlapping bias margin for each of the groups. Average overlapping bias margin of all the groups for each cell population was calculated and is illustrated by the graph of Figure 5-8. In addition, the weight and volumetric efficiency (normalized to a sixteen chip cell) was calculated for each cell chip population. This data is also presented in Figure 5-8. Obviously, to obtain best possible bias margins, a single chip cell would be used. However, this would result in a cell weight and volume more than three times that obtained with a 16 chip cell.

Conversely a sixteen chip cell while very efficient in packaging terms has overlapping bias margins 44% less than a single chip cell. Clearly some compromise between these extremes is required. An eight chip cell was selected as this compromise, providing a 60% reduction in cell weight and volume at the expense of a 27 percent reduction in bias margin when compared to a single chip cell. Based on an analysis of the required overlapping cell bias margin, this was selected as an acceptable compromise between bias margin and packaging efficiency.

An additional reason for maintaining the number of chips per cell at close to the minimum required for the 1.33 Mb/s data rate has to do with cell volt-amp product, cell power dissipation and power supply weight and volume. In terms of driving the cell, the coil volt-amp product is approximately proportional to coil volume at a given frequency and drive field. As the number of chips in a cell is increased, the volume and thus volt-amp product is also increased which in turn increases the energy required to be supplied from the coil drive transistors. As shown in Figure 5-9, the volt-amp product for an eight chip cell is 30% less than that for a 16 chip cell and is within a region of capability for readily available single power transistors.

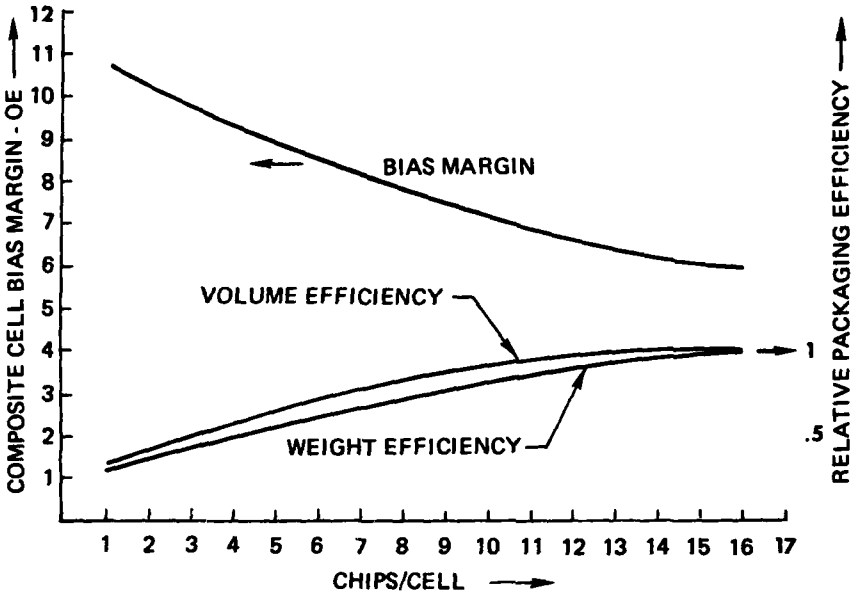


Figure 5-8. Cell margin and packaging efficiency vs population.

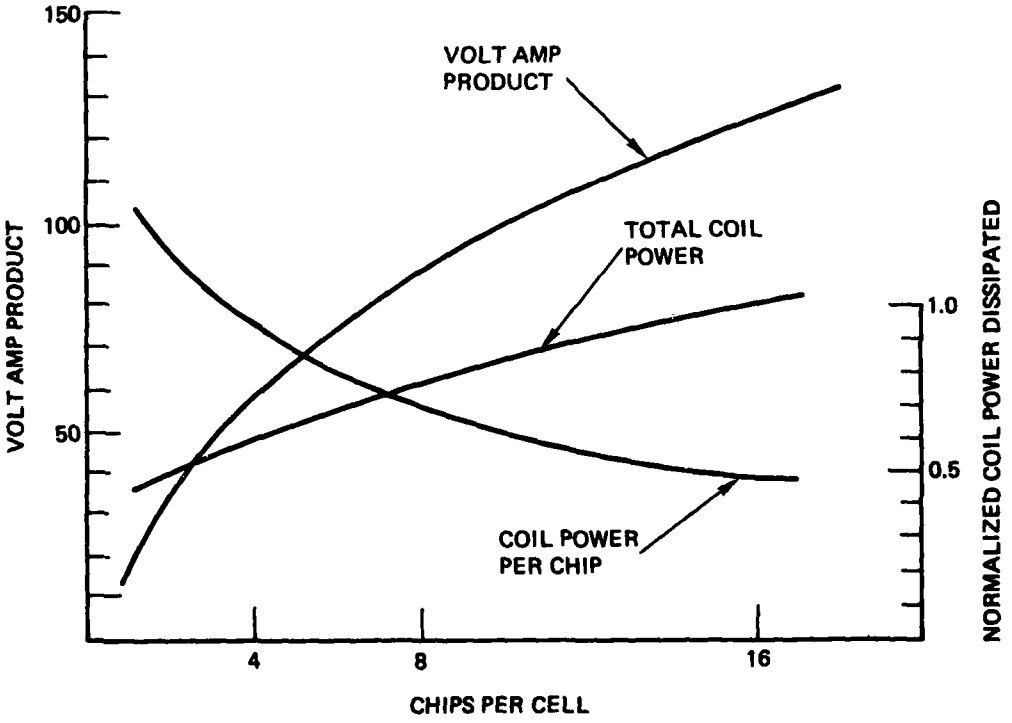


Figure 5-9. Volt-amp product and coil power vs chips per cell.

Drive coil power dissipation is proportional to the coil surface area at a given frequency and drive field. As shown in Figure 5-9, this power also increases with number of chips per cell but the power per chip decreases significantly. From a cell standpoint, maximizing the number of chips per cell produces the greatest power efficiency but from a system power basis this efficiency is maximized at the minimum number of chips in a cell necessary to provide the required data rate. This arises because the typical switching power supply has a small energy storage capacity and thus must be designed for peak load which increases with the number of chips and results in an increase in power supply standby dissipation, weight and volume.

Required holding field is obtained by tilting the drive coils within the bias structure rather than tilting the chips. Such an approach has two potential advantages. First it minimizes coil volume and results in a corresponding decrease in coil drive power. This is particularly important since the tilt direction is normal to the pad edge of the chips, resulting in an increased coil dimension in the tilt direction which would greatly increase cell volume if the chips were tilted in the coil. Secondly, it reduces any components of the drive field normal to this memory element surface caused by tilting the memory elements within the coil. The only concern with this approach is the asymmetry of the coil with respect to the ferrite bias plates which could cause some distortion of the drive field.

The cell magnetics assembly as shown in Figure 5-4 utilizes a tilted X-Y drive coil assembly having a unique X coil which is open at both ends. The open ended feature allows the X coil to be adhesively bonded to the Y coil for maximum heat transfer and because the open ends allow ready removal of the chip carriers when required. Referring to Figure 5-5 the X coil is fabricated by winding two edge wound rectangular spirals which are subsequently formed into a channel shape around which the Y coil is wound and adhesively bonded. The penalty paid for the open end feature is 20% increase in total coil surface area and power dissipation. The coils are wound with a single layer of solid copper rectangular wire 1.55 skin depths thick (0.25 mm) which is calculated as the optimum thickness for minimum ac resistance of a solid conductor single layer coil at the 167 kHz rotating field frequency. The particular coil fabrication processes developed were not compatible with litz conductors which would have reduced the ac resistance.

Bias field for memory element operation is generated by the two permanent magnets in a series circuit consisting of the permalloy shield/keeper, ferrite bias plates and the airgap which contains the drive coils. Permanent magnets have a temperature coefficient that tracks the variation of memory element center bias value with temperature. A Magnet Materials Producers Association (MMPA) ceramic type 1 magnet was used which has a temperature coefficient (tempco) of -0.18% per °C. The ferrite plates serve the dual purpose of ensuring bias field uniformity and acting as a keeper for the rotating magnetic field generated by the drive coils. Permalloy shield/keepers also serve a dual function of providing a return path for the bias field and shielding the memory cell from external magnetic fields. The thickness (30 mils) and length of the permalloy shield is sufficient to attenuate a 20 Oe. external field to operationally acceptable levels in the cell interior. The shield also operates inversely in that it keeps the fields interior to the cell from fringing outside the coil.

5.3.1 Cell Thermal Analysis

A prime consideration in this cell design is to minimize the cell temperature rise above ambient in order to maximize the upper memory operating temperature limit. It is also very important to minimize the temperature differential between the chips and magnets in order to not limit the operating bias margin by an offset between the field supplied by the magnets and the field required by the chips. Conduction heat transfer is the principal mode for distribution and removal of thermal energy dissipations in the cell. The principal significant heat to be conducted is the 4.3 watts being dissipated by the X and Y coils when they are running at the required data rate.

Heat transfer to the carriers is by conduction through air and radiation when the cell is operated in a ground based environment and by radiation only when operated in space (vacuum) environment. Both of these conditions are analyzed. The analysis is based on the cell being adhesively bonded to a heat rail as in the BMM configuration thus the principal conduction heat flow path is through the bottom of the cell. The various internal paths are as follows and listed in order of magnitude.

1. From the bottom of the coils through the bottom magnetics, shield keeper wall and adhesive interface to the heat rail. Referring to Figure 5-10, these paths are between nodes 3, 4, 8, 9, and S.
2. From the top of the coils, through the top magnetics, around the shield keeper and through the adhesive interface to the heat rail. As shown in Figure 5-10 these paths are between nodes, 1, 2, 6, 9, and S.
3. From the top of the coils to the bottom of the coils by the Y coil windings. This is the node 2, 4 path shown in Figure 5-10.
4. From the top and bottom of the coils to the chip carriers as represented by paths through nodes 2, 1, 5 and 4, 3, 5 in Figure 5-10.
5. From the carrier covers through the carrier and flex cables to the MLB surface as represented by the path through nodes 5, S shown in Figure 5-10.

A critical path for balance of magnet temperatures is around the permalloy shell as described above. A high efficiency path is also analyzed wherein a 10 mil thick copper liner is adhesively bonded to the 30 mil thick shield keeper.

The results of these analyses are summarized in Table 5-5.

The method of analysis was to develop an electrical analog model of the cell and calculate thermal resistances (and conductance) of the paths between the selected nodes. Conduction was assumed as the only mode of heat transfer except in the case of the carrier/coil interface previously described. The heat flow from the cell is assumed to be symmetrical about a vertical centerline, thus the analog circuit and dissipations are for 1/2 of the cell. Two dimensional heat flow with line sources was assumed for most paths. The node equations were set up in matrix form (8 x 8) and processed on a T159 calculator using software programs ML02 and ML03.

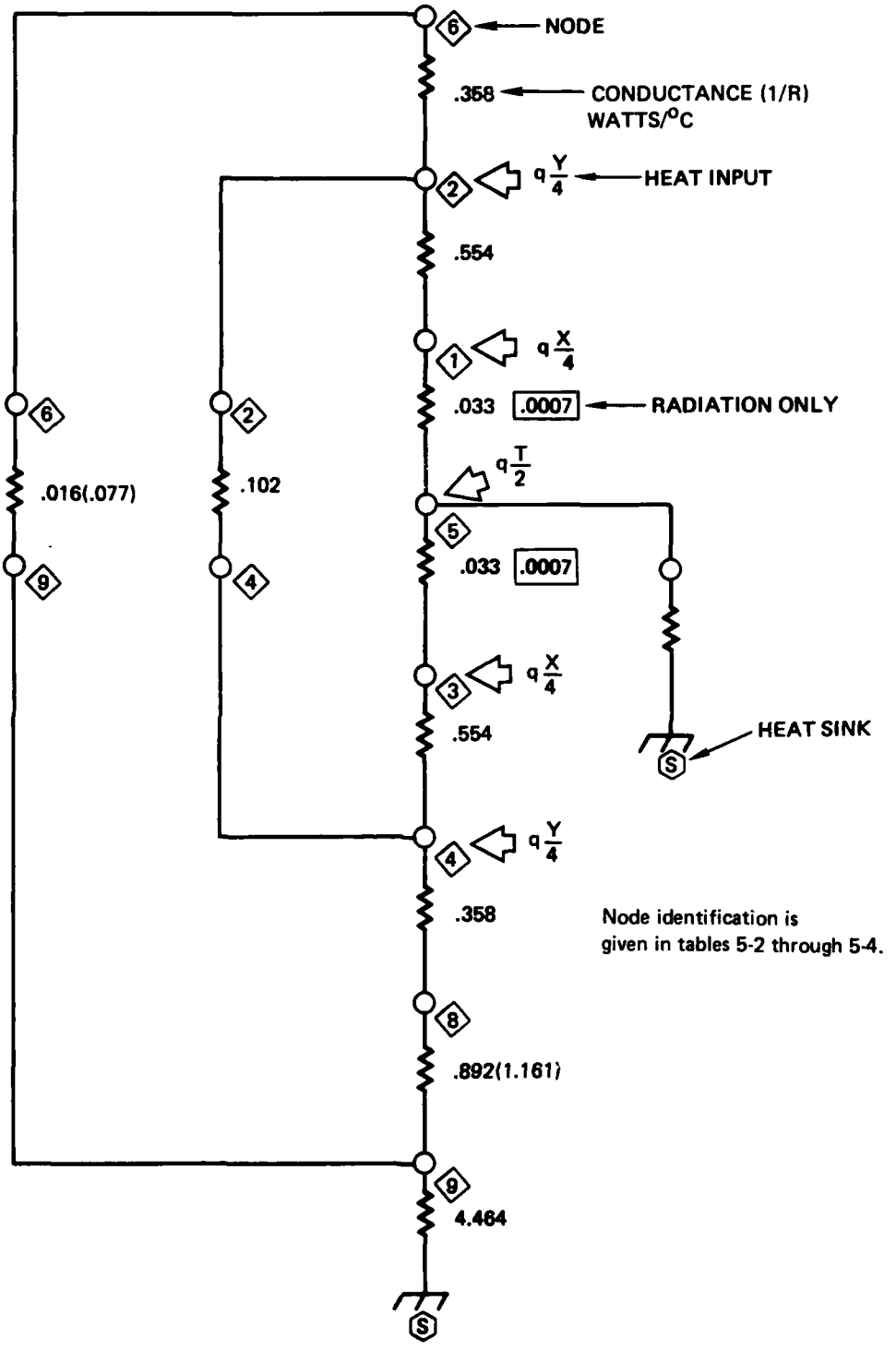


Figure 5-10. NASA 8 x 10^5 bit cell conduction heat flow schematic.

Referring to Figures 5-10 through 5-13 and Tables 5-2 through 5-5, it is shown that the copper liner significantly reduces the top magnet temperature and is particularly effective at the 6 watt 100 percent duty cycle power level. A weight penalty of .025 lb cell is effected if the copper is used. Copper plating was not implemented in the design because it was felt that the cell power would be close to 4 watts and because of added cost of the process step.

Based on these calculations, which generally are considered conservative compared to actual measurements, the chips must be tested at more than 12C above specified mounting surface temperature in order to validate operation for worst case temperature excursions. Cell evaluation conducted at the yield run (Sec. 6) was done at 75C to validate a 60C cell temperature maximum. Another consequence of the analysis is that the upper magnet temperature rises above chip temperature while the lower magnet remains below chip temperature. For transient cell operations, the effect on Z field compensation should nearly cancel between top and bottom magnets.

TABLE 5-2. NASA 8 x 10^5 BIT CELL TEMPERATURE IN VACUUM WITH CARRIER DISSIPATION

Node Temperature Above Heat Rail – °C					
		Permalloy Shield Only		Permalloy Shield With Copper Liner	
Node	Description	6 Watts	4 Watts	6 Watts	4 Watts
1	X Coil Top	23.3	15.3	15.6	10.2
2	Y Coil Top	21.7	14.2	14.0	9.2
3	X Coil Bottom	12.3	8.1	9.7	6.4
4	Y Coil Bottom	10.7	7.0	8.1	5.3
5	Chip (Carriers) (2)	12.0	11.2	11.3	10.7
6	Top Magnet	20.8	13.7	11.6	7.7
8	Bottom Magnet	3.5	2.3	2.4	1.6
9	Bottom Shield	0.6	0.4	0.6	0.4

Notes:

1. All power dissipations are at 100% duty cycle

(2) Dissipations within chip carriers = 0.2 watt

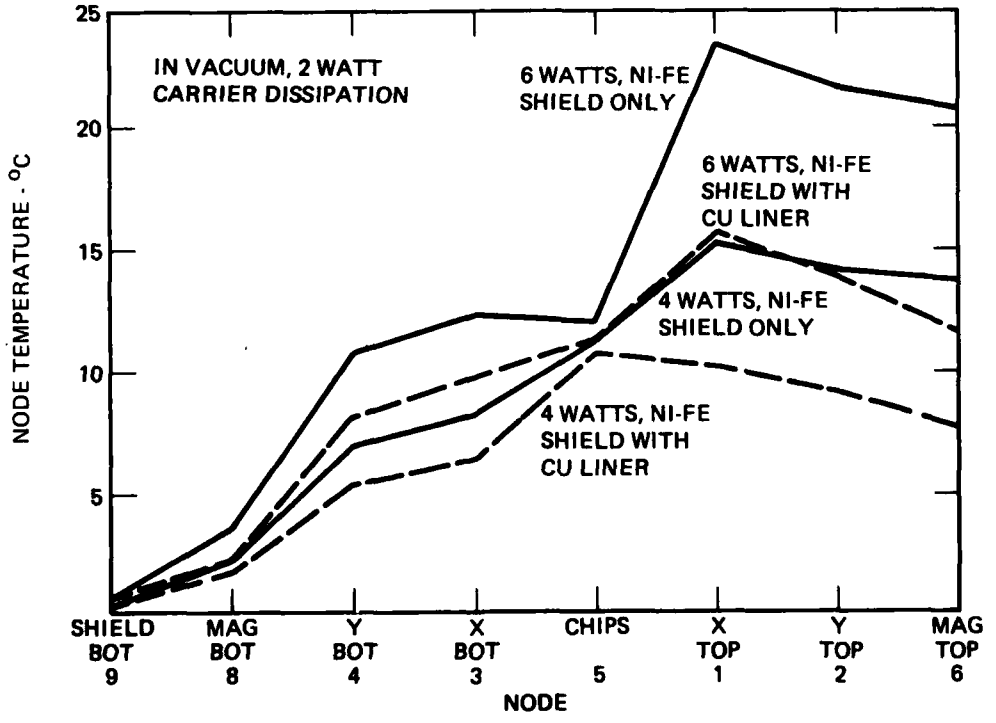


Figure 5-11. NASA 8 x 105 bit cell steady state temperature distribution-100% duty cycle.

TABLE 5-3. NASA 8 x 10^5 BIT CELL TEMPERATURE IN AIR WITH CARRIER DISSIPATION

Node Temperature Above Heat Rail – °C					
		Permalloy Shield Only		Permalloy Shield With Copper Liner	
Node	Description	6 Watts	4 Watts	6 Watts	4 Watts
1	X Coil Top	21.5	14.4	15.0	10.0
2	Y Coil Top	20.3	13.5	13.6	9.1
3	X Coil Bottom	12.5	8.3	9.9	6.6
4	Y Coil Bottom	10.7	7.1	8.3	5.5
5	Chips (Carriers) (2)	15.0	10.0	11.0	7.3
6	Top Magnet	19.5	13.0	11.3	7.5
8	Bottom Magnet	3.5	2.3	2.4	1.6
9	Bottom Shield	0.6	0.4	0.6	0.4

Notes:

1. All power dissipations are at 100% duty cycle

(2) Dissipations within chip carriers = 0.00

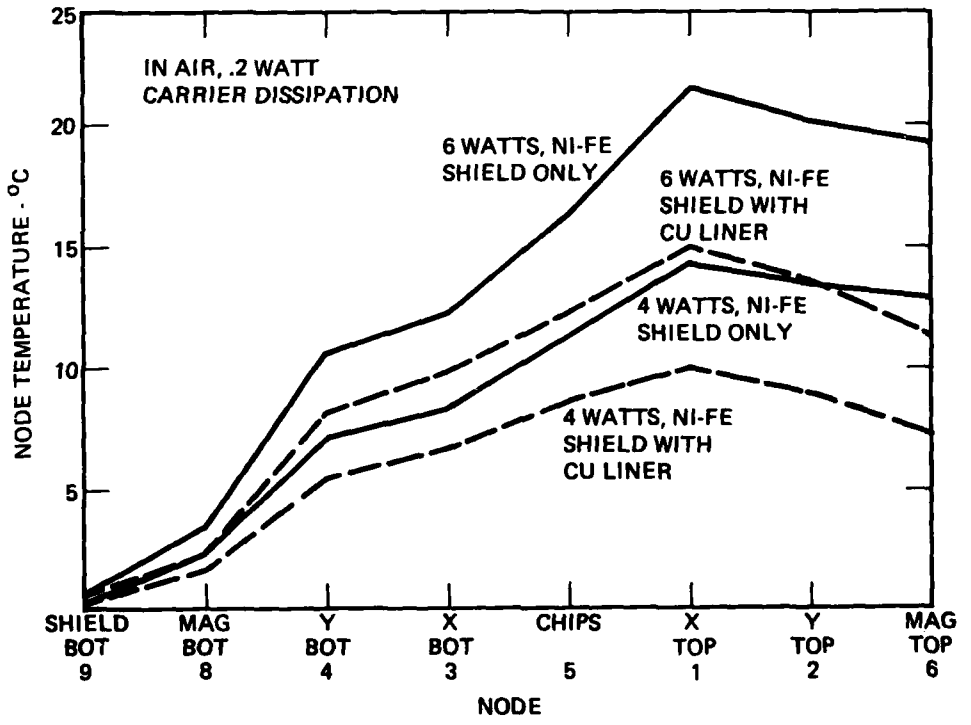


Figure 5-12. NASA 8 x 10^5 bit cell steady state temperature distribution - 100% duty cycle.

TABLE 5-4. NASA 8 x 10^5 BIT CELL TEMPERATURE IN AIR WITH NO CARRIER DISSIPATION

Node Temperature Above Heat Rail – °C					
		Permalloy Shield Only		Permalloy Shield With Copper Liner	
Node	Description	6 Watts	4 Watts	6 Watts	4 Watts
1	X Coil Top	21.5	14.3	15.0	10.0
2	Y Coil Top	20.2	13.5	13.6	9.0
3	X Coil Bottom	12.4	8.3	9.9	6.6
4	Y Coil Bottom	10.6	7.1	8.2	5.5
5	Chips (Carriers) (2)	16.3	11.3	12.3	8.6
6	Top Magnet	19.4	12.9	11.3	7.5
8	Bottom Magnet	3.5	2.3	2.4	1.6
9	Bottom Shield	0.6	0.4	0.6	0.4

Notes:

1. All power dissipations are at 100% duty cycle

(2) Dissipations within chip carriers = 0.2 watt

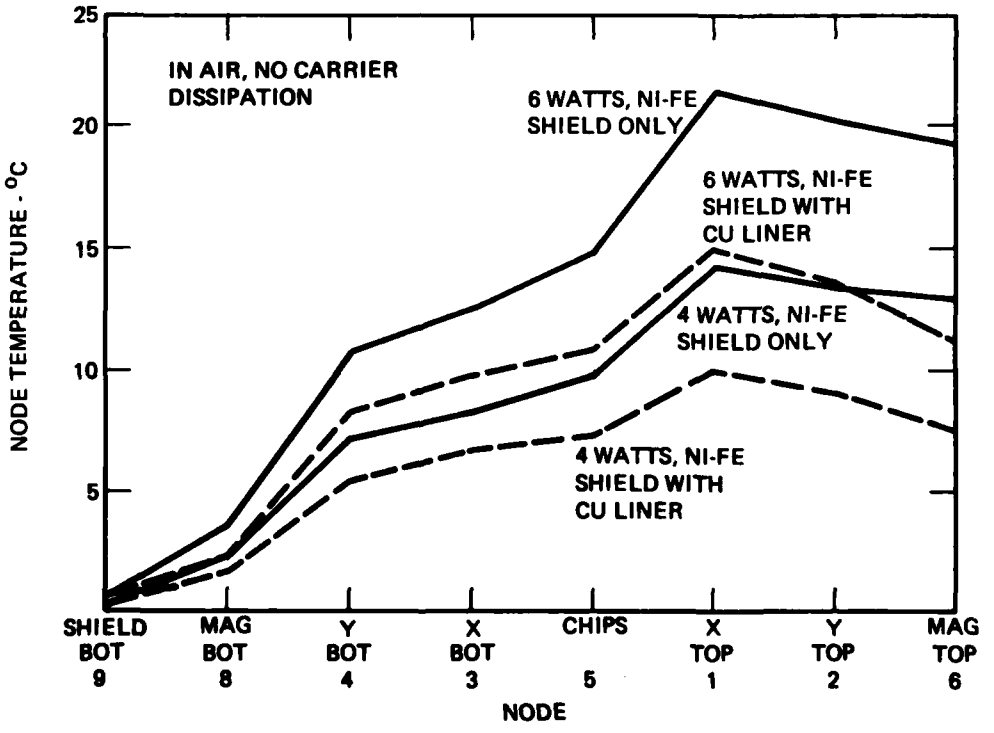


Figure 5-13. NASA 8 x 10^5 bit cell steady state temperature distribution - 100% duty cycle.

TABLE 5-5. ANALYSIS SUMMARY

Environment	Dissipation –Watts– Total	Carrier	See Table	See Figure
Cell in vacuum	6/4	0.2/0.2	5-2	5-11
Cell in air	6/4	0.2/0.2	5-3	5-12
Cell in air	6/4	0/0	5-4	5-13

TABLE 5-6. CELL ELECTRICAL CHARACTERISTICS

$UI_{product}$			
DC Resistance	X	0.68	Ω
	Y	0.96	Ω
	Z	3.87	Ω
AC Resistance at 160 kHz	X	1.35/1.06*	Ω
	Y	2.8/1.93*	Ω
Inductance	X	17.0	μh
	Y	25.8	μh
Field Sens	X	23.8/26.6*	Oe/A
	Y	32.5/37.5*	Oe/A
	Z	73.6	Oe/A
Cell Power at +45 Oe	X	2.9/1.9*	watts
	Y	3.3/1.7*	watts
	Total	6.2/3.6*	watts

*Without tantalum.

5.4 ELECTRICAL CHARACTERIZATION

Three fields are produced by the cell assembly. A rotating field is produced by the X/Y orthogonal coils. Main electrical factors in their design include field uniformity, impedance, and inductance. Coil configuration and size are dictated by mechanical tolerance requirements and by electrical requirements. Bias field as produced by the magnetic circuit of the shell is required to be set for each cell's specific chip bias range requirements. The field is expected to be accurate over the chip's surface and to track the chip's thermal coefficient. Holding field which is provided for by tilting the coil in the bias assembly, is required for maintaining a strong attraction between permalloy elements and bubbles when rotating field is turned off. Table 5-6 summarizes characterization results given in more detail in the following sections.

5.4.1 Coil Field Uniformity

Field uniformity is a factor in cell design and operation. The lowest value of field in the chip area determines minimum drive requirements while the highest field in the area determines noise and conversion in worst case. An AC probe was used to determine field shape and conversion into other directions. It is a three axis movable probe with micrometer adjustment which is capabable of profiling individual coils, completed cells or partial assemblies. Figure 5-14 defines directions of the probe relative to the coil assembly and chips.

Sensitivity measurements were made by exciting the Y or X coil with a sinewave current at 160 kHz and measuring the coil field with calibrated probe. The probe which is a miniature wire coil was calibrated using a standard helmholtz coil. Geometric referencing of the probe was done from the coil center. For Figure 5-15 and Figure 5-16 the probe was centered vertically in the coil which is worst case as far as edge uniformity because of fringing at the open ends of the coils. Actual chip active surface is 15 mils above center for the upper chips and 30 mils below center for the lower chips. Curves of Figures 5-15 through 5-17 were obtained by moving the probe mounted on a micrometer controlled platform through the coil opening in parallel with the coil's center line (Figure 5-14). Results are expressed as Oesteds of field produced per ampere of current in the coil.

A major concern during cell development was higher than anticipated power dissipation of the coil due to carrier covers of tantalum and due to X coil conductor loss in the Y field. Some improvements were obtained by reducing cover thickness and by using a lower power drive waveform. During hermetic sealing development it was found that seam sealing of tantalum covers resulted in poor packaging yield compared to the indium seal. As these results show, an added benefit of the indium seal is a 25 percent reduction of cell power.

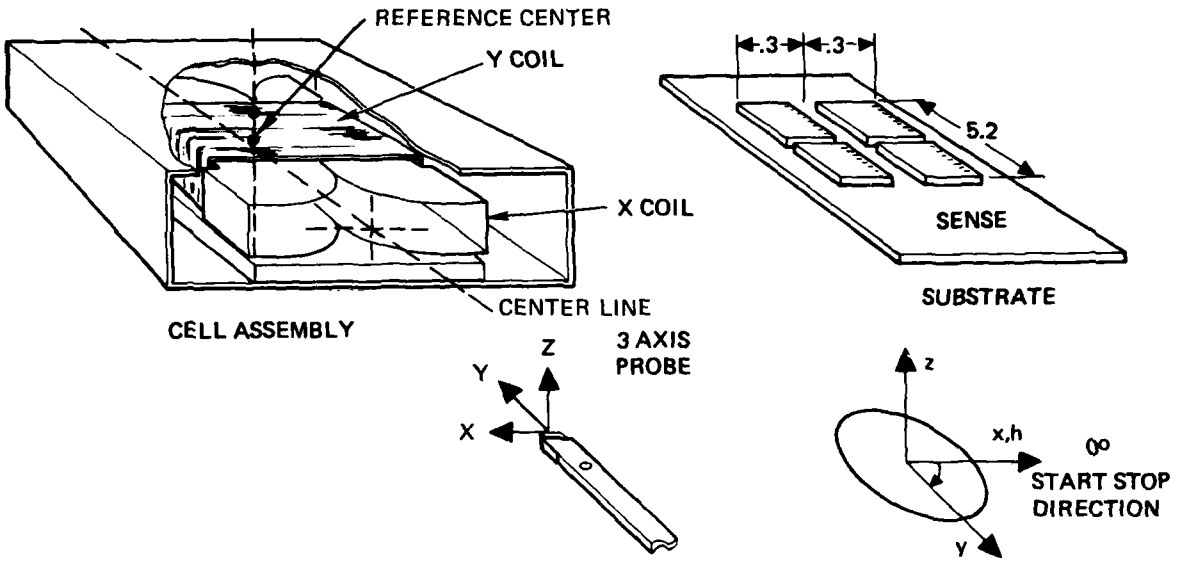


Figure 5-14. Field direction definitions.

Figure 5-15 gives the field uniformity of the Y coil with and without tantalum covers. Covers require about 4 percent higher field at the edge of the chip area and they produce some asymmetry due to plating variability. Variability can be overcome by stamping from plated tantalum sheets. An extra tantalum cover was placed below the lower carrier in order to maintain field symmetry around center plane of the coil assembly. Field uniformity for the X coil is shown in Figure 5-16. In this case, covers reduce field by about 8 percent while making the field more uniform. The center line of the coil (curve 1 and 2) is less uniform than the chip area edge field because the joint between the two halves of the coil spreads at the open ends.

Conversion of rotating field from Y into Z as shown in Figure 5-17 affects Z margin and noise pickup. At vertical center, conversion is zero but at 30 mils below or above the center plane at the chip edge, pickup is about 0.7 Oe/A as shown in Figure 5-17.

5.4.2 Cell Bias Field Evaluation

Two bias magnet configurations were evaluated over a temperature range from -20 to +60C. Magnet 1 consisted of a single magnet the same size as the cell ferrite. Magnet 2 consisted of 4 separate magnets with a total size slightly smaller than that of the cell ferrite. Both magnets 1 and 2 were of the same MMPA ceramic type 1 material.

Test procedure for determining cell coefficient involved measuring the gauss level of the cell as a function of temperature using a gauss probe inserted in the cell. Zero field drift and probe gain were measured vs temperature and used to correct probe data. Figures 5-18 and 5-19 are graphs of corrected cell measurements normalized to 25°C. This procedure gives a cell coefficient value of -0.178%/°C for the large magnet and -0.174%/°C for the 4 small magnets.

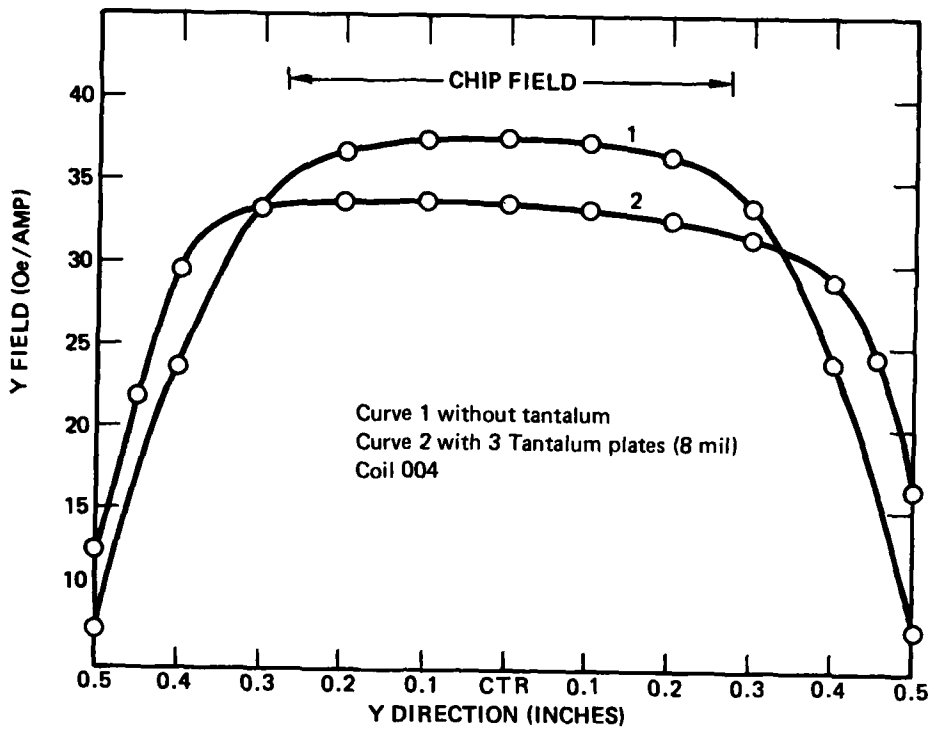


Figure 5-15. Y field from Y coil.

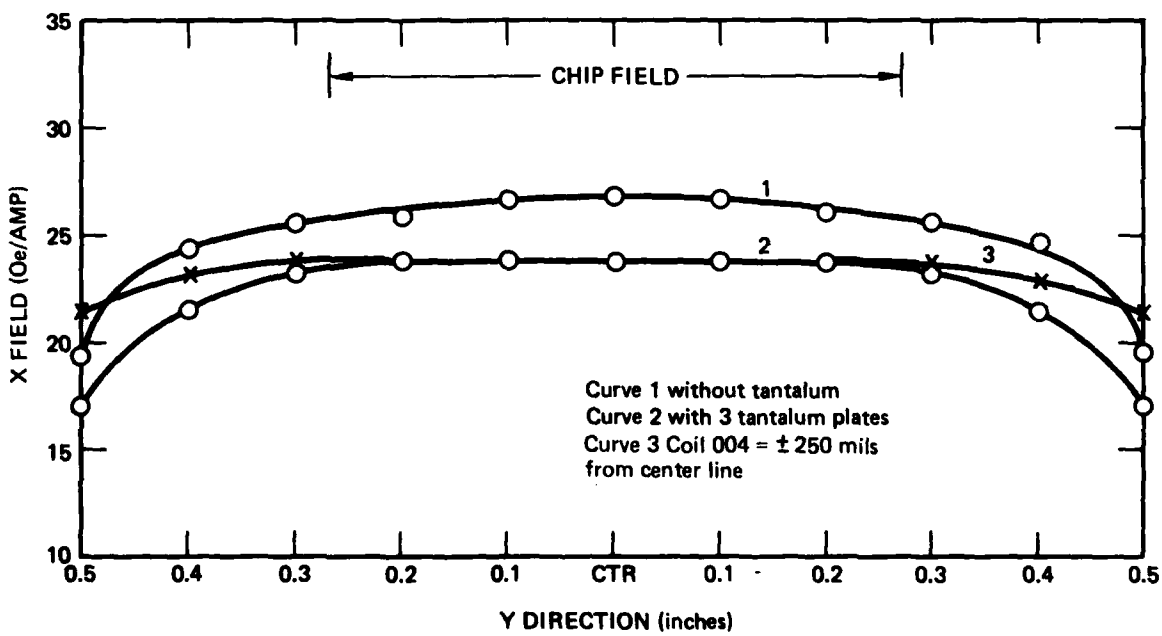


Figure 5-16. X field from X coil.

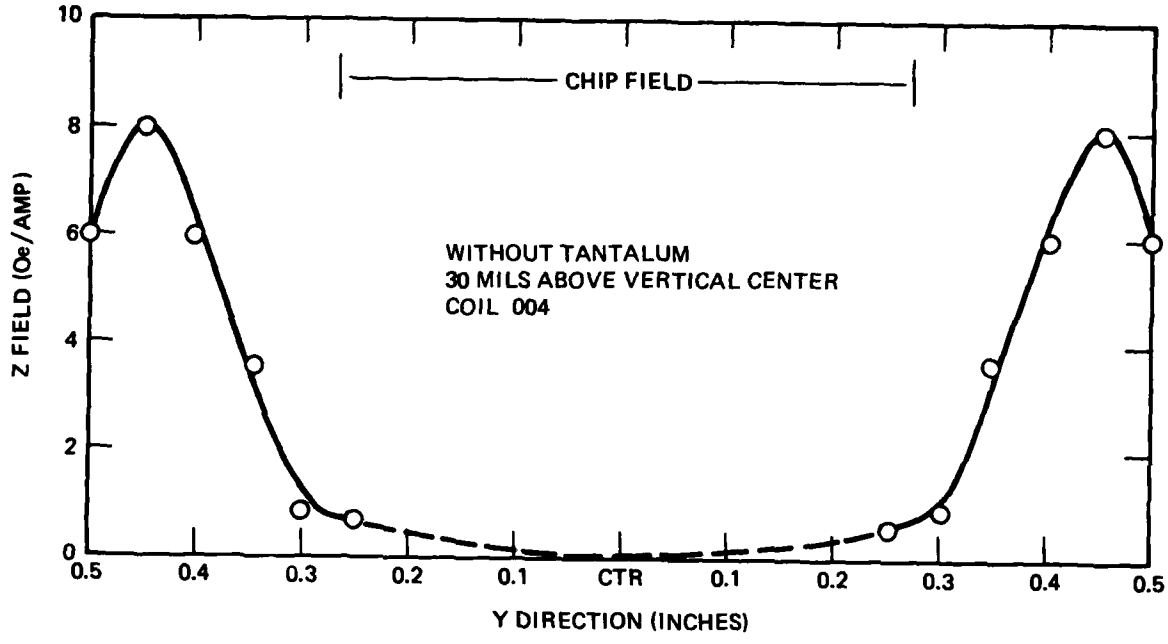


Figure 5-17. Z field from Y coil.

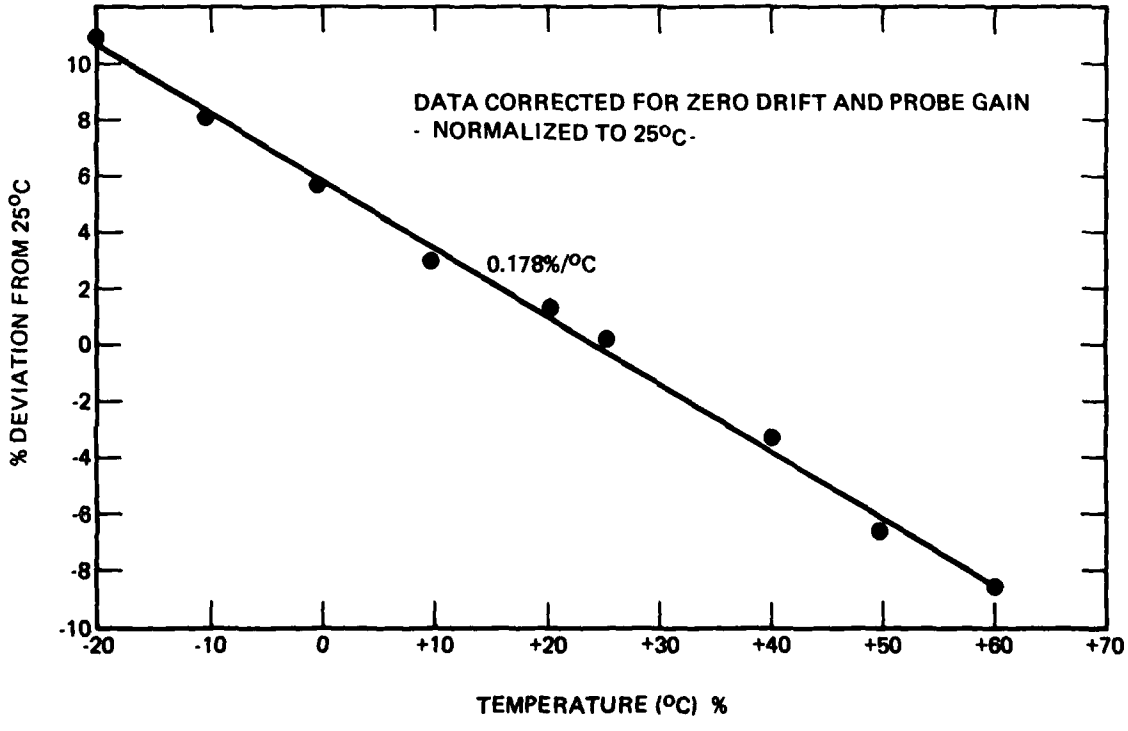


Figure 5-18. Bias field variance with temperature.
(1 LARGE MAGNET)

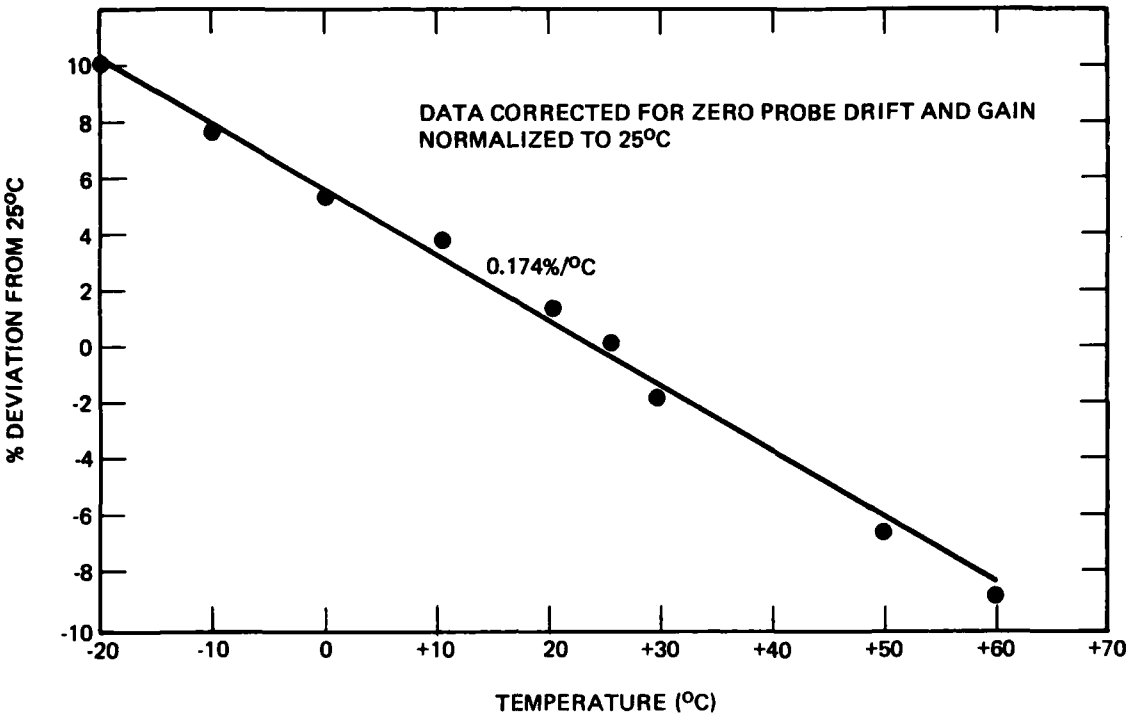


Figure 5-19. Bias field variance with temperature.
(4 SMALL MAGNETS)

5.4.3 Coil Impedance Measurements

A Boonton Inductance Bridge was used to measure inductance and AC resistance. To identify component losses, individual coils were tested first alone and then again at stages in assembly. Design equations used at the beginning of the program predicted lower than measured Y coil losses for the case of metallics inside such as the X coil or metal covers. Consequently power dissipation will tend to be higher than predicted at the preliminary design review except that other design strategies were used to reduce power. Overall, cell power dissipation will remain in the 5 watt range with tantalum covers and in the 4 watt range without tantalum covers.

Figure 5-20 is a plot of coil resistance for a completed cell including carriers with 3 tantalum covers. Slightly lower resistance is obtained (Figure 5-21) without tantalum covers. Inductance was given in Table 5-6. Resistances listed in the table are averages of three final cell configurations.

5.5 CELL ENVIRONMENTAL TESTS

One memory cell identified as the engineering cell was subjected to a series of environmental tests (figure 5-22) to demonstrate that the design is suitable for qualification programs to NASA Specifications.

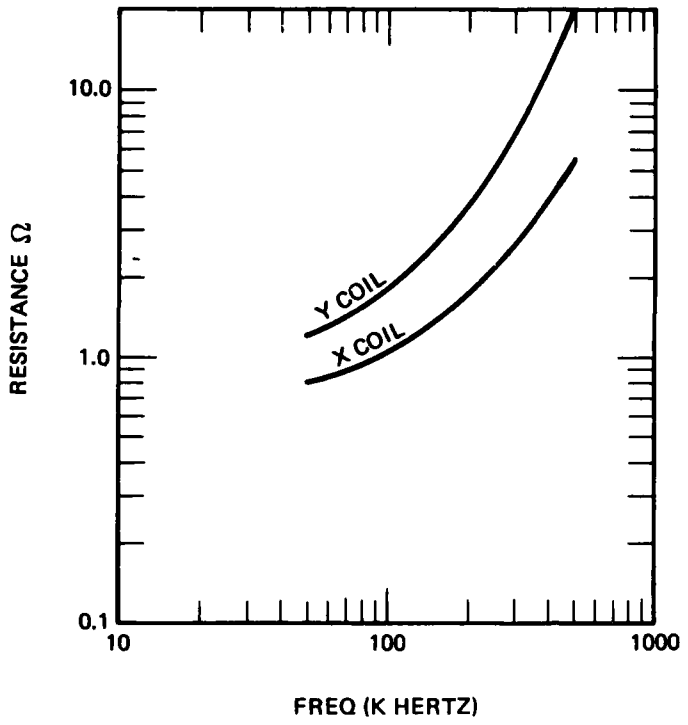


Figure 5-20. AC coil resistance vs freq with tantalum covers.

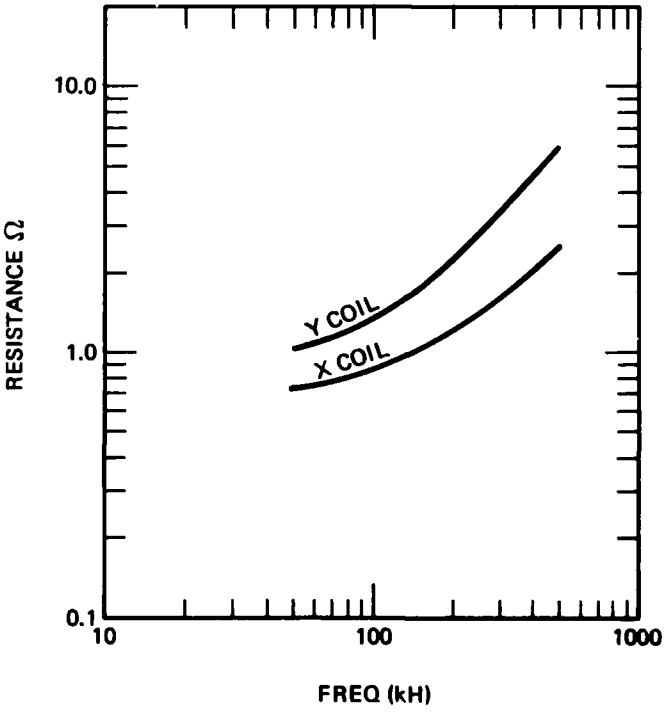


Figure 5-21. AC coil resistance vs freq w/o covers.

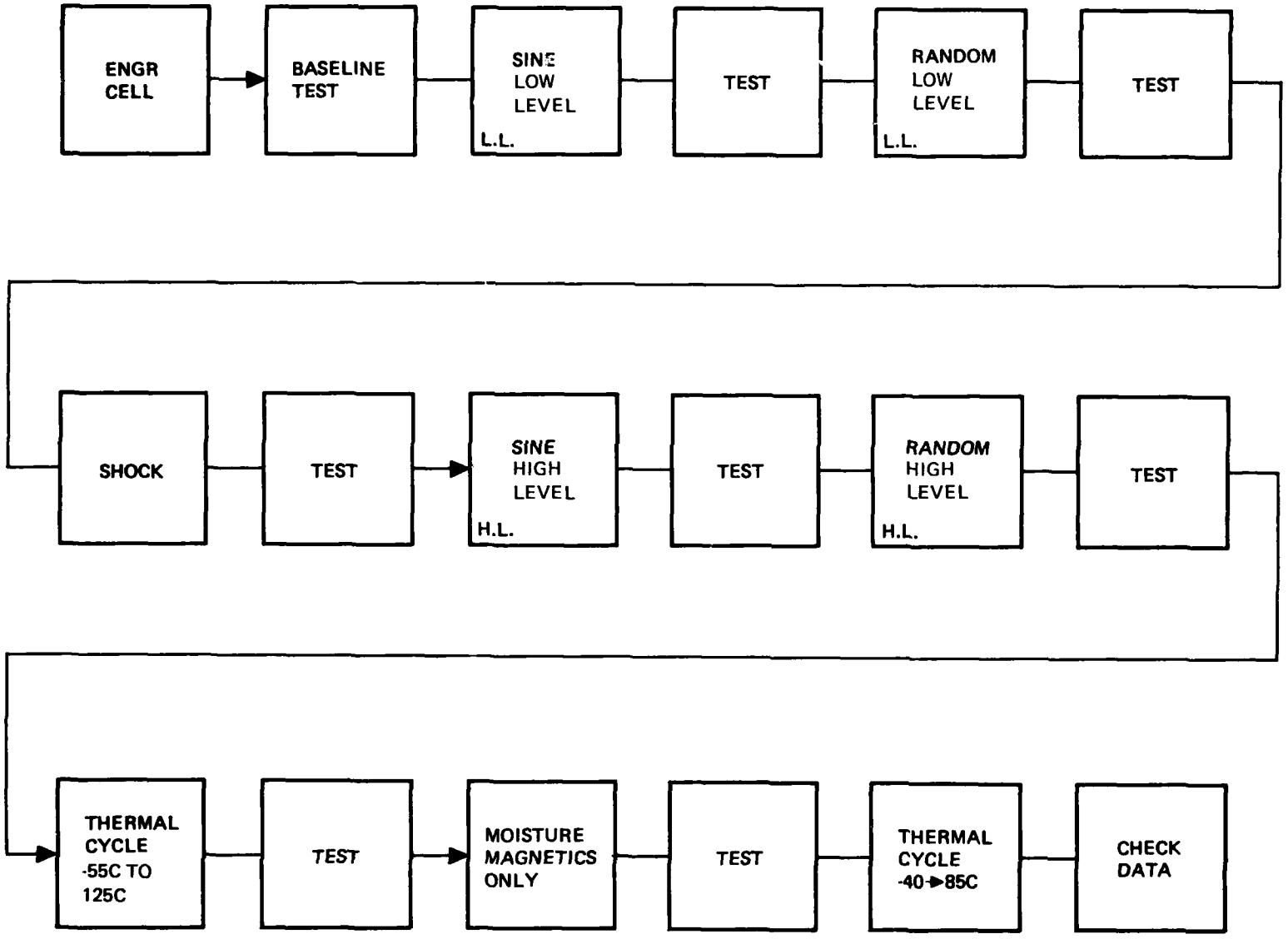


Figure 5-22. Environmental test sequence.

Performance tests consisted of measurements at 25C which are most sensitive and effective in identifying electrically defective devices. The tests include, but were not limited to, sense window, Z bias margin, coil drive, operator drive, data pattern, start/stop, variable data rate operation and data retention. These tests, as applicable, were conducted prior to and after each environment exposure. Environmental tests were conducted as SSD's environmental test lab.

Prior to mechanical testing, cell hardware was secured according to assembly procedures and the cell tested for baseline results. Cell bias was set close to the top of the margin for two chips as shown in Figure 5-23 in order to uncover vibration related data loss. Then the test sequence of Section 5.5.1 was started.

5.5.1 Order of Environmental Test and Test Results

1. **Sinusoidal Vibration**

   Test was in accordance with MIL-STD-883, Method 2007, Condition A, (20G peak 3 axis).

   Post test results indicate no loss of data or margin shift.

2. **Random Vibration**

   Test was in accordance with MIL-STD-810, Method 514, curve AM

   Post test results indicate no loss of data or margin shift.

3. **Shock**

   Test was in accordance with NASA spec, exhibit 5, Para 4.2.2, Figure 4 (500G 3 axis).

   Post test results indicate no loss of data or margin shift.

4. **Sinusoidal Vibration**

   Test was in accordance with MIL-STD-883, Method 2007, Condition B (50G 3 axis).

   Post test results indicate no loss of data or no margin shift.

5. **Random Vibration**

   Test was in accordance with MIL-STD-810, Method 514, curve AN.

   Post Test results indicate no loss of data, no margin shift.

6. **Thermal Cycle**

   Test was in accordance with MIL-STD-883, Method 1010, Condition B Temperature from -55 to +125C

   Post test results disclosed several anomalies.

   a. Unable to operate chip U3 top substrate.
   b. Unable to operate lower substrate chips.
   c. Stored data scrambled in a tested chip. The cell was not expected to retain stored data at the temperature limits of this test.

Failure analysis indicated that the cable conductors cracked at the carrier interface probably because of extreme handling and the taped back position they were in during the series of tests. It is probable that vibration and handling for testing deformed the conductors at the bond interface so that work hardening caused conductors to crack. In addition a bond failure of a beam leaded diode occurred. Analysis of the failure indicated a probable cause of failure due to adhesive which was inadvertently permitted to flow under the diode. Repeated expansion and contraction of the adhesive stressed the bond to the point where it opened. Normally polymetric coating is avoided since the problem is well known. After repair of the cell the test was repeated without incident.

7. Humidity Test

Magnetics assembly only was tested in accordance with MIL-STD-202, Method 103, Condition B.

After each environmental test Z bias margin was measured for the seven operating die of the cell. Except for one measurement point which was probably an error (chip 02 at baseline), Z bias margin was repeatable within experimental error as shown by the tight clustering of the cell profile curves of Figure 5-23 for post tests, one through five.

Following cell repair after thermal cycling and after humidity testing of the magnetics assembly, the cell was assembled and retested. All chips exhibited higher lower bias threshold than previous tests by about 1 oe (Figure 5-23). Because of rework it is difficult to precisely identify the cause of the shift without another series of tests.

8. Data Retention

The cell was subjected to thermal cycling according to Method 1010 except that the temperature range was reduced to -40 to 85C. Data loss occurred on chips 02, 03, and 05. These were shifting errors and are typical of upper margin failure (see Figure 5-23). Lowering cell bias to 146 oe (by 3 oe guard band) is required to provide data retention over the specification range.

Conclusions

This series of tests provide considerable confidence that the memory cell design is adequate for space qualified programs which require wider scoped qualification testing. Qualification testing should include vibration, shock, thermal cycling, data retention as above but also thermal vacuum and humidity of completed cells.

5.6 CARRIER HERMETIC SEALING STUDY

Principal features of the developed carrier include a thick film metallized ceramic substrate which is glass sealed to a refractory metallized seal ring which forms a hermetic cavity into which the chips are secured. Figure 5-6 illustrates the build-up of the chip cavity. A thin film metallized ceramic cover is indium reflow soldered to the metallized seal ring forming the final hermetic package seal.

The basic substrate is fabricated from 96% aluminum oxide plate stock which is ground to a .015 in (.38 mm) thickness. This ground substrate is metallized and insulated with standard thick film materials and processes. Hermetic testing at the thick film level shows that some dielectric materials are porous and were avoided for implementation in the final design.

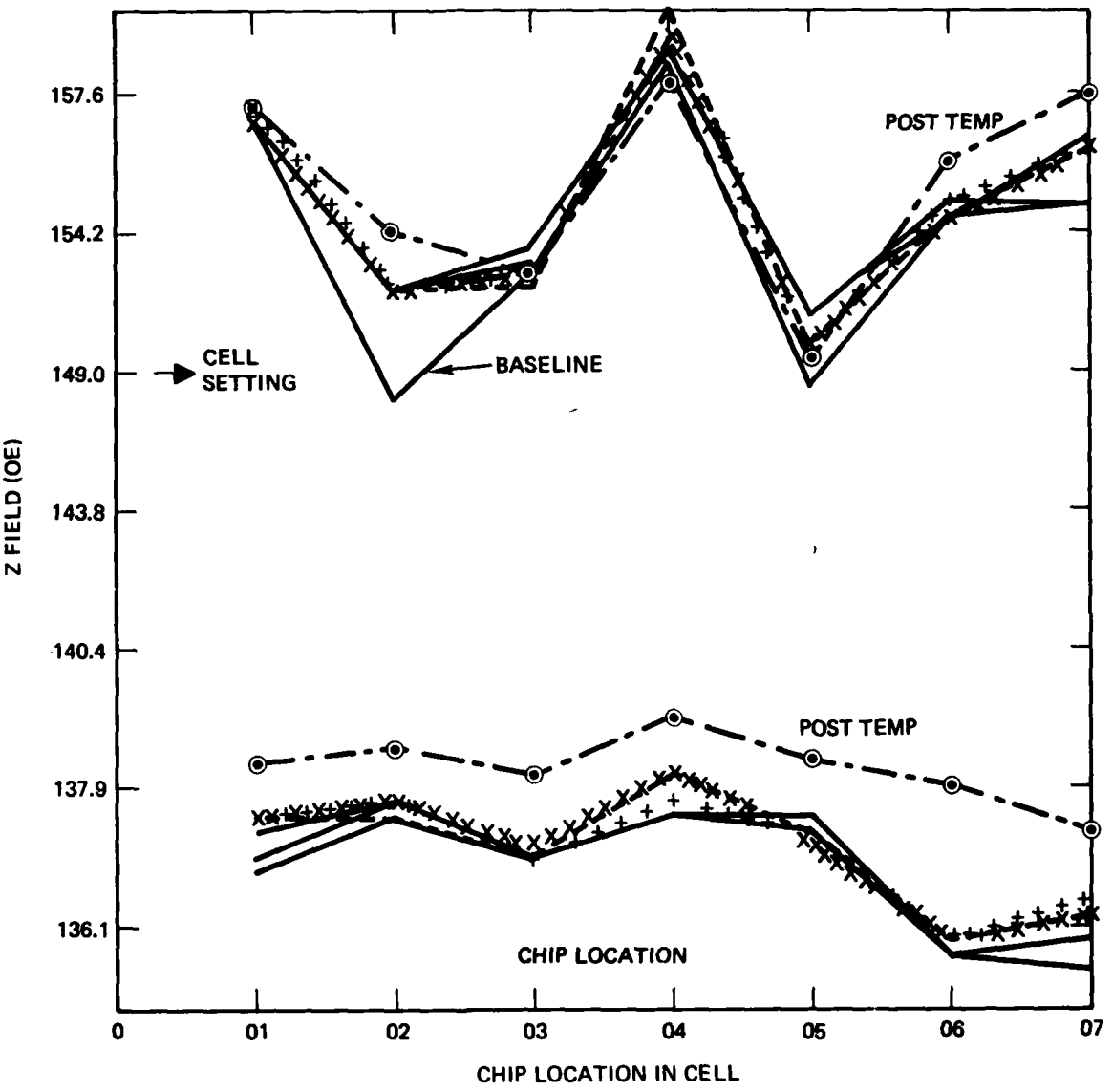


Figure 5-23. Z bias margin for engr. cell at X/Y ~ 40 Oe,25°C.

The 96 percent aluminum oxide seal ring is formed by stamping from un-fired green ceramic and subsequently tungsten metallized on one side and fired at high temperature. The resultant ring is flattened by a vendor proprietary process and plated with nickel which is fused into the tungsten for improved adhesion. The nickel is overplated with high purity gold which forms the final seal solder interface. A crystallizing glass was selected to provide the hermetic seal between the unmetallized seal ring surface and the thick film metallized substrate. This glass material is screened onto both parts which are then subjected to two drying and one prefuse furnace cycles in an air environment. The two parts are subsequently aligned, clamped and fused together at 410C in an air atmosphere. Processing yield of test and design parts was nearly 100 percent upon completion of the process development. Gross leak testing was performed on all parts by pressurizing the seal cavity which was closed off with a gasketed metal plate. Helium tracer gas fine leak testing was also performed at this assembly level.

Both tantalum and metallized ceramic covers were evaluated during the seal development. Tantalum was initially selected as it is nonmagnetic, has a coefficient of expansion matching the ceramic carrier and is compatible with progressive resistance heating seam reflow soldering. The covers were fabricated from .008 in.(.20mm) thick sheet which was nickel plated, vacuum baked and over plated with gold by a proprietary high adhesion process.

Sealing process development and coil loss testing ultimately resulted in the use of a .010 in.(.25 mm) thick 99.5 percent aluminum oxide cover having thin film metallization on one side which was overplated with .0005 in.(.013 mm) of copper. The 99.5 percent aluminum oxide was selected because of its high elastic modulus (very stiff), strength, compatibility with thin film metallization, and flatness after processing. The thin copper plating provides the necessary electrostatic shielding for the bubble chip interconnect and reduces eddy current loss for minimum coil power dissipation. The copper is also compatible with the sealing material ultimately used.

Three cover sealing processes were investigated during carrier development and are as follows.

1. Progressive resistance heating seam reflow soldering (seam sealing) of gold-tin alloy preform
2. Progressive electron beam reflow soldering of a gold-tin alloy preform
3. Mass reflow soldering using pure indium

Development started with the progressive flexure reflow of gold gold-tin solder as this process was currently in use for the seam sealing of all metal hybrid packages. The majority of the development sealing was conducted using ceramic hybrid package bases and the tantalum covers discussed. After extensive development efforts on sealing schedule the initial sealing yield on fifty packages was 50 percent and rework proved to be difficult. The very high adhesion of the gold-tin alloy to the metallized ceramic resulted in loss of metallization and ceramic chipping on most attempted rework. The low initial sealing yield was attributed to lack of flatness of the thin tantalum covers.

A limited investigation into the use of electron beam technology for reflow of the gold tin was initiated and it was found that the progressive localized heating caused cracking in the glass seal interface of the design carriers.

The third and most promising fluxless process investigated involved mass reflow sealing of the metallized ceramic cover to the metallized seal ring surface using pure indium. Numerous packages were sealed successfully by a belt furnace bulk reflow of indium tinned interfaces in an inert atmosphere at a peak temperature of 180C. The process as developed has an initial seal yield in excess of 75 percent and multiple seals of reprocessed covers and rings were very successful. Leak rates (helium bomb) meeting the requirements of MIL-883A are typical. Some seal degradation from stress induced cracking was observed after thermocycle (-55 to + 125C) and may be eliminated by copper plating the seal ring surface to minimize brittle gold-indium intermetallics.

5.7 POLYIMIDE CHIP PASSIVATION

During the SSDR program it was discovered that magnetic particles from dicing would degrade or inhibit chip performance if the particle fell on the chip's active surface. A demonstration showed that vibration would cause loose particles to move within the cell thereby randomly changing chip operation. A mylar spacer of about 1 mil glued to the chip's surface was found to eliminate sensitivity to vibration and to eliminate the effect of further particle contamination. The mylar spacer which was applied to chips individually after cleaning was found to be cumbersome for large quantities of chips and of inconsistent quality because of the difficult handling operation.

A wafer coating of polyimide was therefore introduced as a combination passivation and spacer layer. Basically it is a thick coating of about .7 mils which is spun on and then pattern etched to expose bonding pads. Two wafers of the first yield run and four wafers of the manufacturing yield run were coated, etched, and evaluated for mechanical integrity. No significant mechanical degradation was observed after the humidity exposure for the test of Figure 5-24.

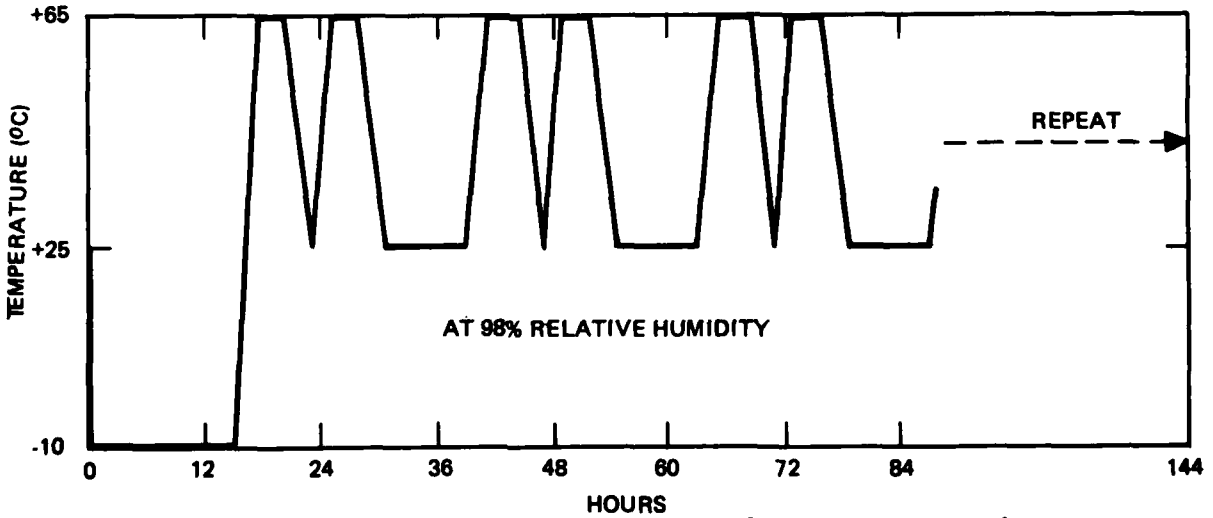


Figure 5-24. Humidity and thermal exposure of polyimide coated wafer.

6. CHIP YIELD RUN

Two yield runs were planned for the program, the first in a research environment followed by a yield run in manufacturing. Most of the data collected covers chips of the first run and a subsequent evaluation of preliminary cells. Because of process and equipment difficulties and because of funding limitations, the second yield run was concluded without obtaining sufficient die for further cell assembly and with little additional information.

6.1 FIRST YIELD RUN DESCRIPTION

Eighteen 2-inch CaGe garnet wafers were chosen for the first yield run and processed in lots of four wafers each at the Electronics Research Center. Wafers were chosen with a collapse field range of from 160 to 164 oersteds. Figure 6-1 is a process flow diagram which describes sequential steps in the process and probe testing. Table 6-1 shows vacuum depositions, layer thickness, and tolerances which were targeted for device fabrication. Resisitivity and circuitry measurements were made on monitor samples included with each run. Table 6-2 shows the various lithography steps in the process.Permalloy and conductor layers are high resolution steps requiring critical alignment while the oxide layer is noncritical because it blankets the register area.

6.1.1 Yield Summary

Yield can be calculated a number of ways. Table 6-3 gives the assumptions on the chosen method which was based on the number of wafers which were diced or which were consumed in process. Remaining wafers can be reprocessed so they were omitted although effort is expended in partial processing and in preparation for reprocessing.

Wafer probe testing was done in two phases. The first phase was a screen to identify die acceptable for further testing while the second phase was the characterization of die at two temperatures and two drive fields.

During the yield run extra mechanical, magnetic, and electrical tests were conducted than normal production practice in order to obtain statistical data for design and as background data for anticipated production runs. Good die were found to be distributed on the wafers as shown in Figure 6-2. Except for the edge die only one location is void of good die which probably is caused by a mask defect.

6.1.2 Wafer Probe and Cell Test Results

Propagation margins were measured at wafer probe and with the cell tester. Comparisons are given in Figures 6-3 and 6-6 as profiles according to the installed location within a cell. Probe data was obtained at 60 and 25C for conditions of 50 Oe of sinewave drive at 60C, and 40, and 50 Oe at 30C. Probe Resistance data was measured at 60C but was extrapolated at 25C for comparison purposes. Prober conditions were start/stop propagation with asynchronous data shift applied between write and read and complemented data for a second pass. Cell propagation data was obtained from -10C to 60C for conditions of trapezoidal drive roughly analogous to 40 and 50 Oe of sinewave drive and for start/stop conditions. Testing involved writing once and reading continuously while Z field was varied until errors occurred.

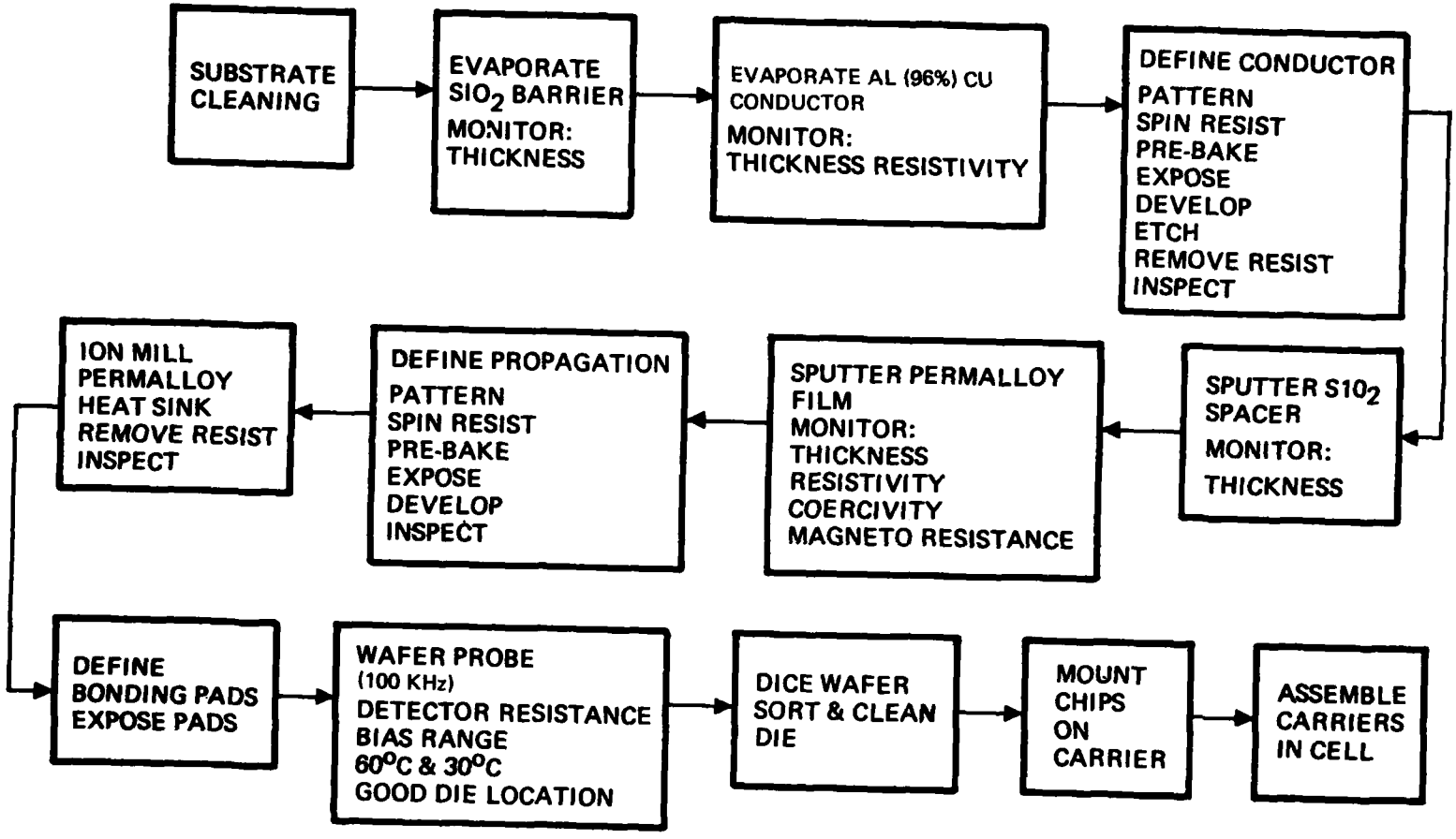


Figure 6-1. Two-level process sequence for 100K bit devices.

TABLE 6-1. PROCESS FLOW CHART

Vacuum Deposition	Film Thickness	Process Control Parameter
Schott Glass Barrier[1]	900 ± 100Å	–
Al/Cu Conductor[1]	4250 ± 250Å	*Resistivity – 3-6 μΩ/cm Adhesion – Tape Test
SiO_2 Spacer[2]	6000 ± 300Å	–
NiFe Propagation[2]	4000 ± 300Å	*Resistivity – 17-21 μΩ/cm **Coercivity – <1.5/Oe

[1]Schott glass and Al/Cu deposited by E-beam in the same pump down.

[2]SiO_2 and NiFe rf sputter deposited in the same pump down.

*Resistivity measurements are made on a glass sample using a 4-point probe.
**Coercivity measurements are made on the same glass sample using the B-H loop.

Composition	YSmLuCaGe	Q	4.5-5
Thickness	3.41	L	0.398
4 π M	295-315	Stripwidth	3.39-3.46
K μ	18,000	H_{COL}	160-164

TABLE 6-2. PHOTO LITHOGRAPHY PARAMETERS

Photolithography	Resist Thickness	Process Control Parameter
Conductor (c-layer)	1.5μ	*Replicator Linewidth – 3.9μ
Propagation (p-layer)	1.5μ	*Detector Gap – 2.2μ
Passivation (O-layer)	2.5μ	Noncritical
P and C Layer Alignment	–	*±1.5 μm

*These measurements were made on a sample basis.

Comparison between wafer probe and cell is imperfect. Upper margin averages about the same or both but differs for individual die. Lower margin averages consistently lower for cell test than for probe test by about 3 Oe, which provides a greater margin than would be indicated by the probe station. Data scatter is apparent in prober results because of the discrete Z step size of the prober and because of testing error of about ± 1 Oe. The reason for the consistent 3 Oe lower margin was not identified.

Most of the yield decline (from 20 to 16 percent) in going from wafer probing to carrier installation was because of propagation failure (Table 6-4). About 10 die which failed propagation at cell test were not identified by the wafer prober, suggesting that a 15 percent fallout occurs due to dicing or due to handling. Previous testing indicates that garnet flecks (as obtained from dicing) affect propagation when they fall on critical locations, as discussed in section 5.7.

Compilation of detector resistance statistics provides insight into process uniformity and information for matching bubble chips. A large factor in the sense budget for multiplexed systems has been variability in bubble output signal which is correlatable to detector resistance. Some of the variability is removable without yield impact by selective placement of die in a cell based on detector resistance matching. A histogram of detector resistance for chips from the 1st yield run which were incorporated in preliminary cells is given in Figure 6-7.

TABLE 6-3. CALCULATION OF YIELD

Basis of Yield			Total Dice: 37 Die Wafer	Total Dice: 33 Die Wafer
1	On started wafers	28	1036	924
2	On accepted wafers	11	407	363
3	On accepted wafers plus another wafer consumed in process	12	444	396

Garnet Area consumed in process . . . . . 37.7 in^2

Yield on a Basis of 400 Die

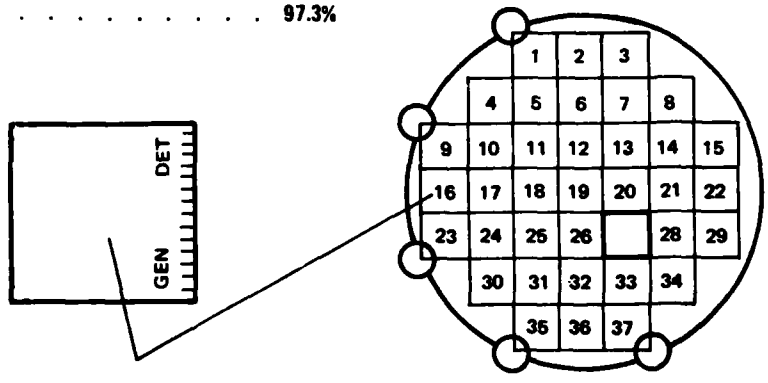
Initial 60C screen yield 30.7%

Two Temperature operating die yield (>1 Oe) 20.2%

Two temp criteria (60C (>6 Oe) 16.2%

Maximum Wafer Yield 32.3%

Mask Yield 97.3%



Circled die always failed most probably because of edge proximity. Number 27 also failed all the time suggesting a mask failure.

A 20 percent spread in resistance is indicated. The next four figures (6-8 to 6-11) show comparison between detector resistance as measured with a digital volt meter and cell tester sensitivity. A reasonable but not perfect correlation exists between detector resistance and detector sensitivity. Correlation is less perfect between resistance and matrix breadboard output measurements. Imprecise clamp release setting, amplitude measurement, and variable

zero noise are attributed as the cause of differences. Results suggest that detector outputs which are difficult to measure at wafer probe can be best matched using detector resistance which is easy to measure and fairly accurate.

The main factor in detector resistance variation is permalloy thickness variation due to sputtering process control and to analomies within the sputtering chamber. Figure 6-12 shows

TABLE 6-4. CHIP FAILURES

Die available from wafer probe	65
Installed Die	38
Broken Die	4
Unstable Propagation	5
No Propagation	3
Inadequate Z Margin	1
Marginal for Low Drive Field	4
Burned Out (Electronics Failure)	2
Pattern Sensitivity (Async Test)	2
Untested Die in Inventory	4
Unaccounted	2

the lot permalloy thickness measured from a coupon at the center of the lot wafers. There appears to be a slight inverse relationship between reported permalloy thickness and detector resistance. Measurements are single point measurements and tend to ignore wafer and lot gradients.

6.1.3 Operator Amplitude Statistics

Generator current amplitude and replicator current amplitude margins were measured at the cell tester to determine best set values for the module and to determine optimum amplitude compensation. Temperature compensation reduces the potential hazards at high temperature of spurious bubble nucleation and the potential for reduced lifetime due to localized heating of electromigration. Figures 6-13 and 6-14 are the minimum amplitudes required for replication and generation. Each dot is a measurement.

A lifetime test on replicators was started in October of 1979 to determine if a hazard exists due to high amplitude and continuous operation such as could exist in some applications. No failures or shifts in resistance were observed in the 1500 hours (5×10^{12} pulses) of continuous testing for the eight chips tested. Current ranged from 80 milliamps on several chips to 195 milliamps (10^7 amps per cm^2) on 2 chips.

6.1.4 Detector Performance (Sense Budget)

Figure 6-15 shows critical chip and cell sense factors as a sense budget. Primary budget factor is the average of 32 bubble signals from the four cells, each measured as the instantaneous difference between baseline and a single isolated bubble signal at strobe time.

As the memory module design developed, the module was changed to include peak detection which provides about 10 percent more signal than shown in this budget.

Considerable variations (about ± 10 percent) as shown in Figures 6-8 to 6-11 occurred in signal amplitude on the production run because of detector resistance variation due to permalloy thickness or linewidth variations.

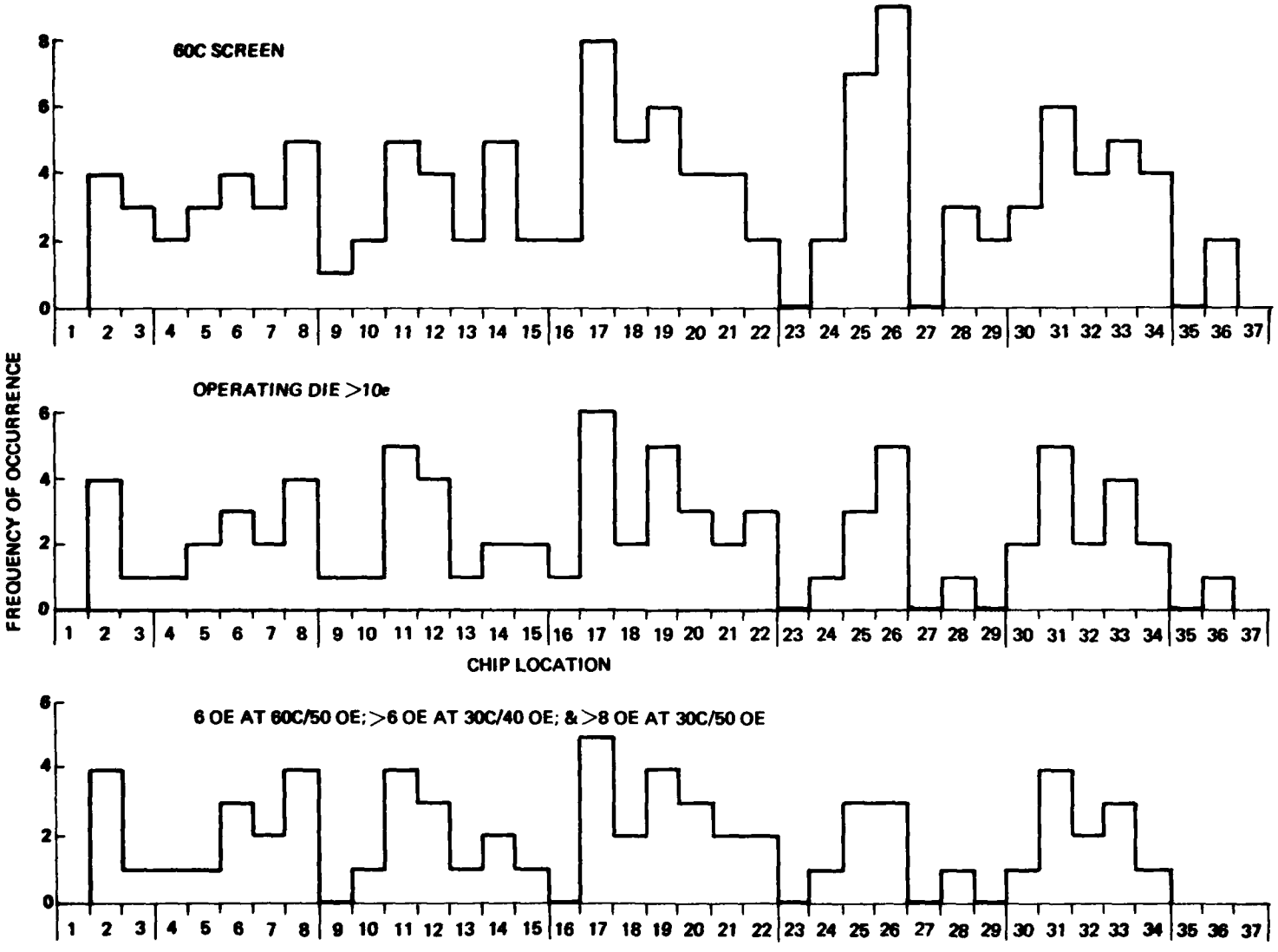


Figure 6-2. Good die versus wafer location.

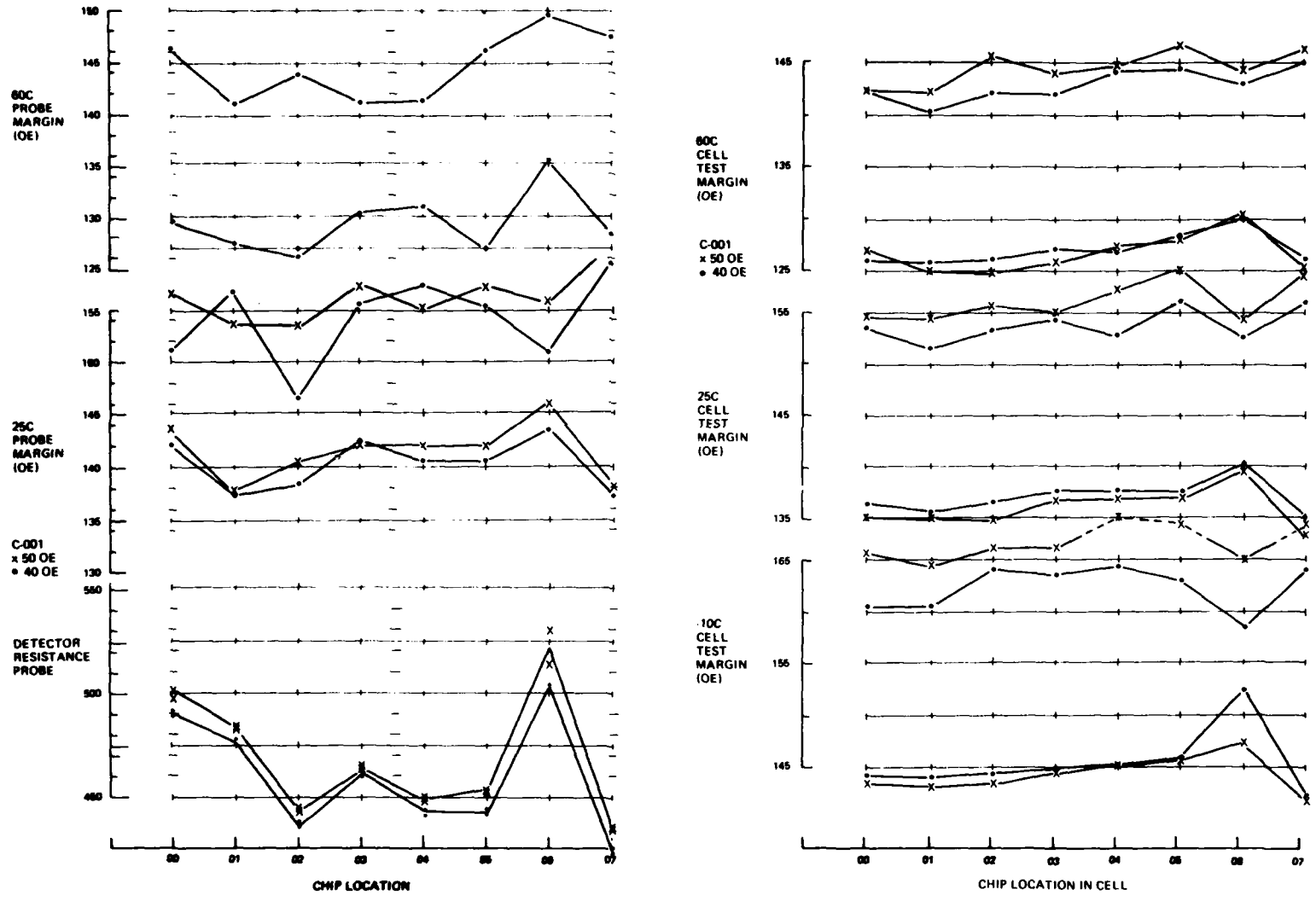


Figure 6-3. Probe station of cell test comparison of C-001.

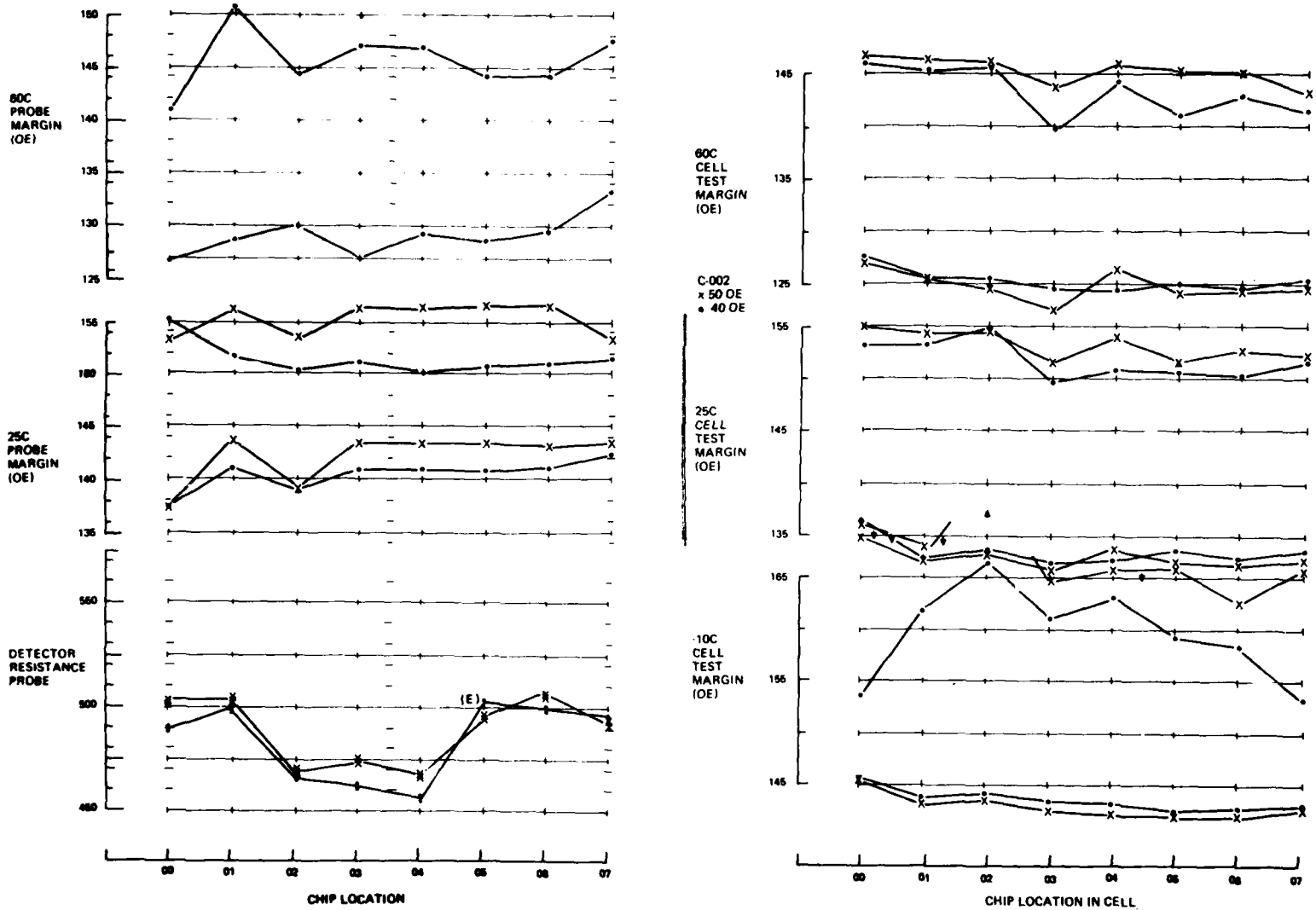


Figure 6-4. Probe station of cell test comparison of C-002.

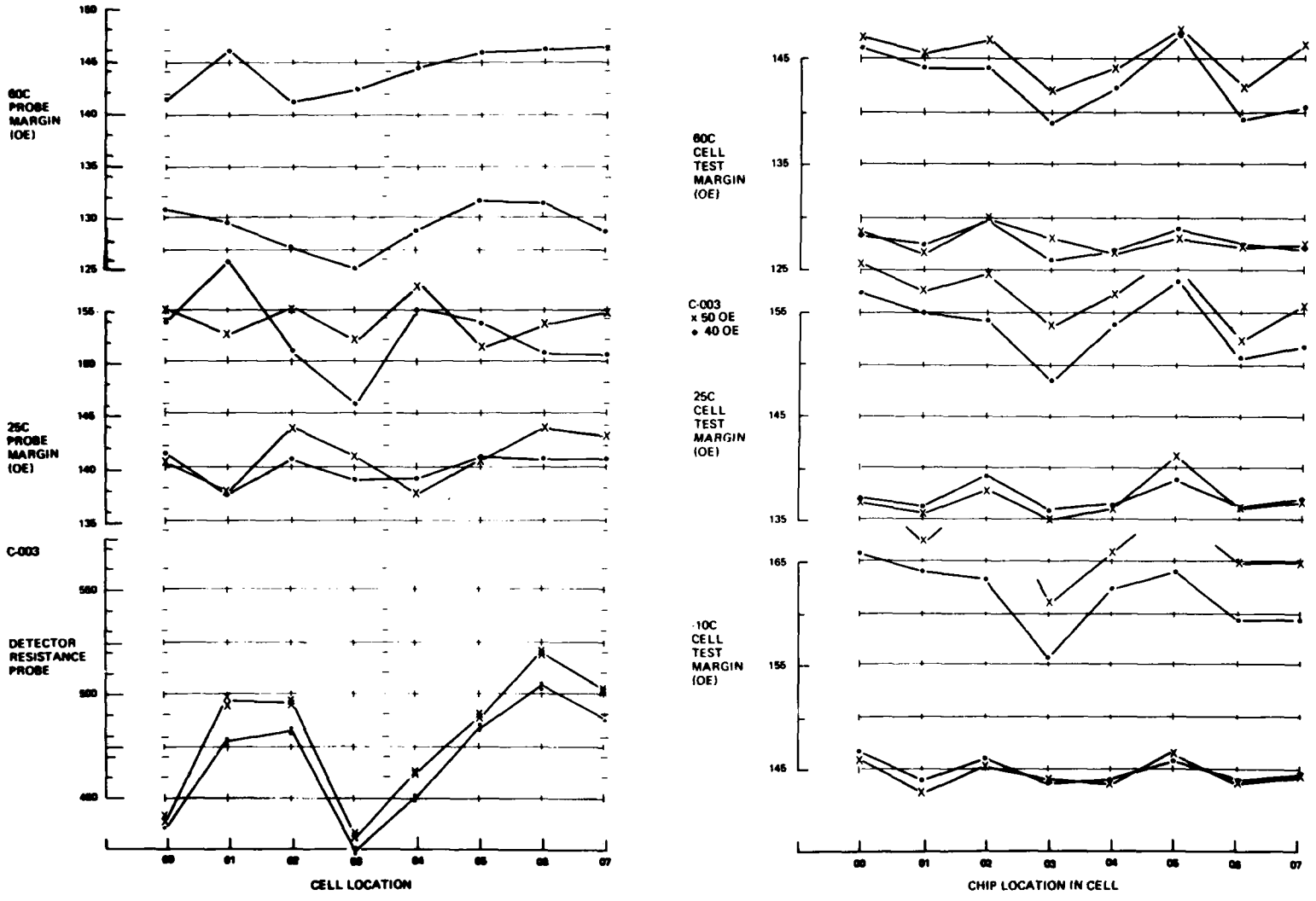


Figure 6-5. Probe station of cell test comparison of C-003.

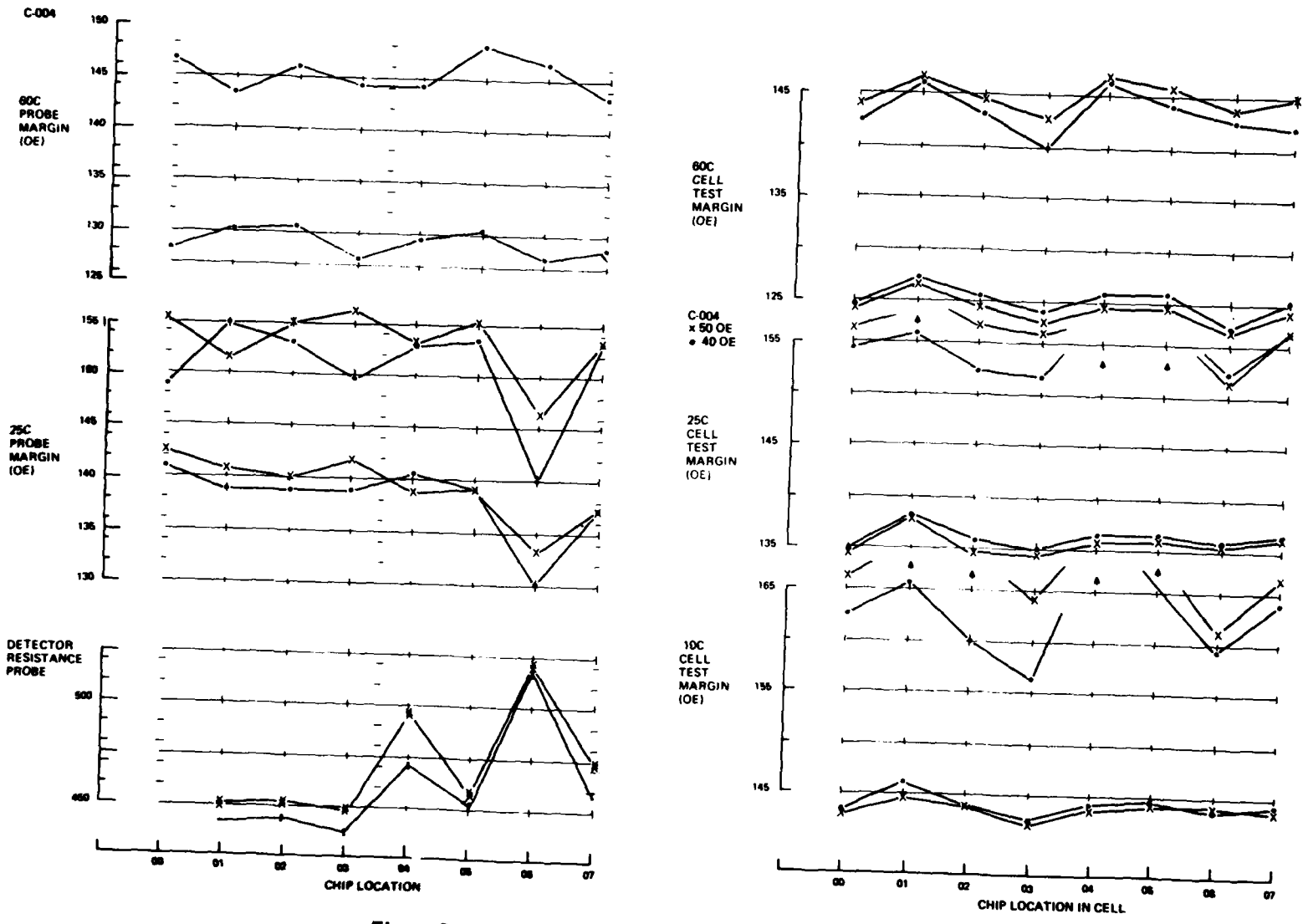


Figure 6-6. Probe station of cell test comparison of C-004.

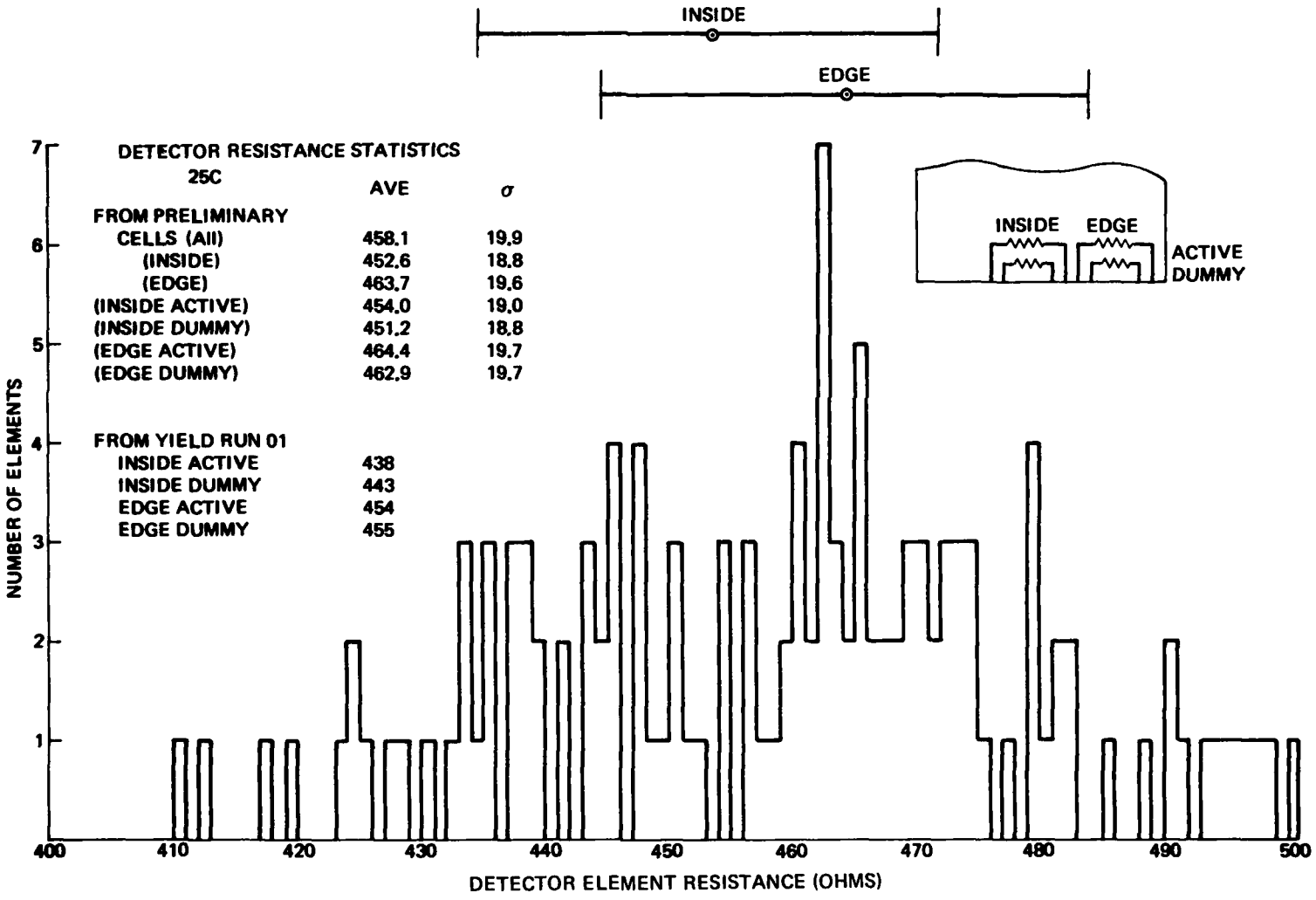
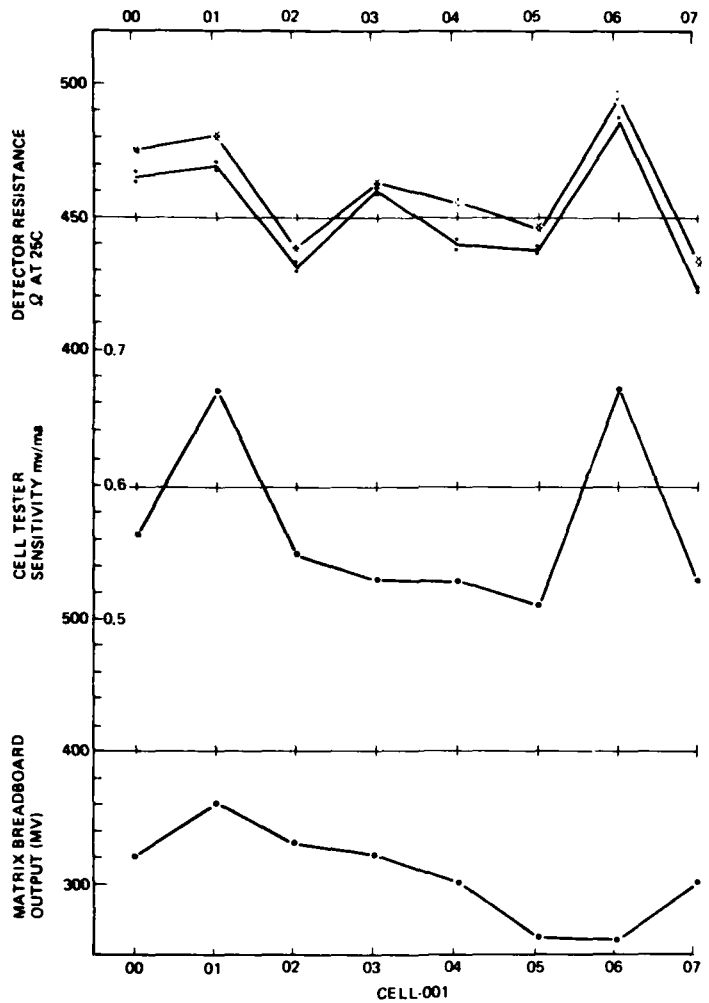
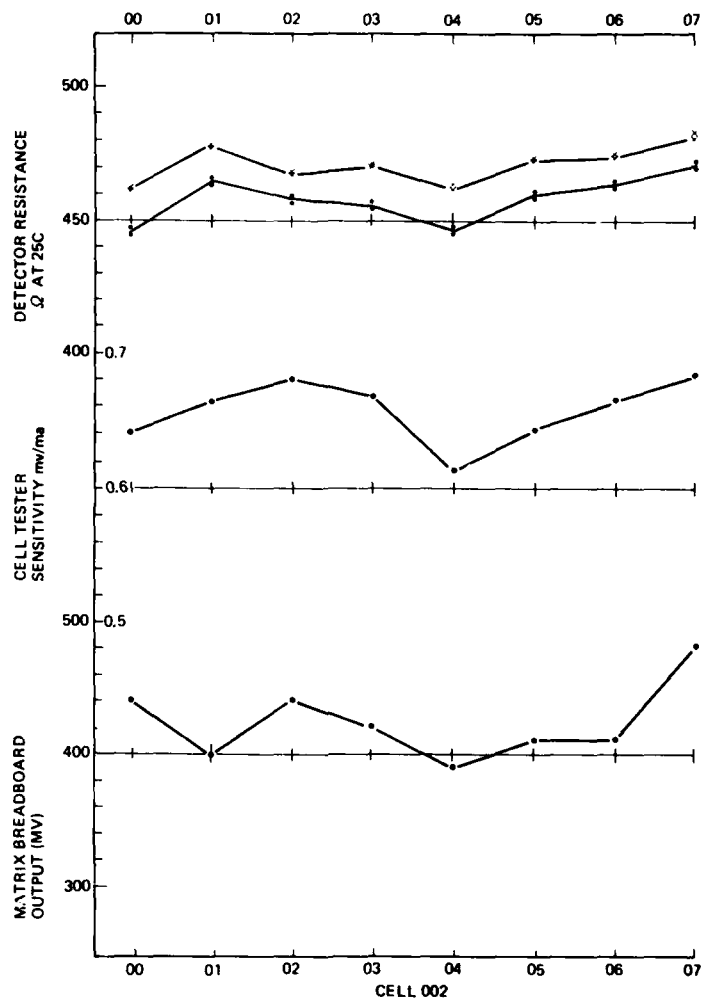


Figure 6-7. Detector resistance statistics.



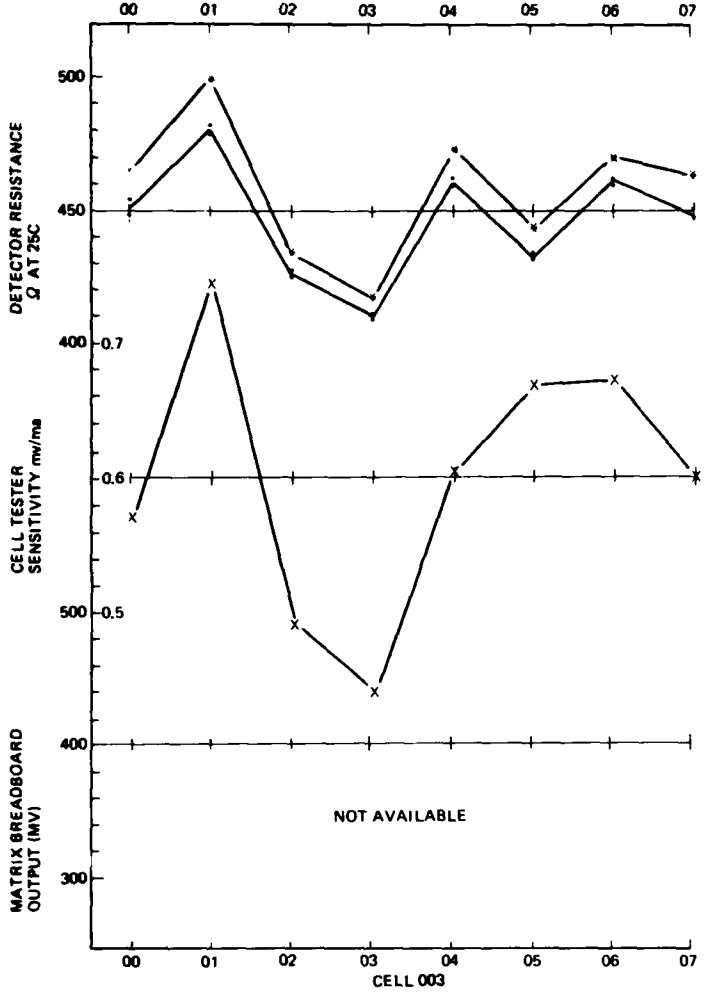
TOP: RESISTANCE • INNER DETECTOR
x EDGE DETECTOR
MIDDLE: CELL TESTER SENSITIVITY
BOTTOM: MATRIX OUTPUT A=40

Figure 6-8. Comparison between signal and resistance.



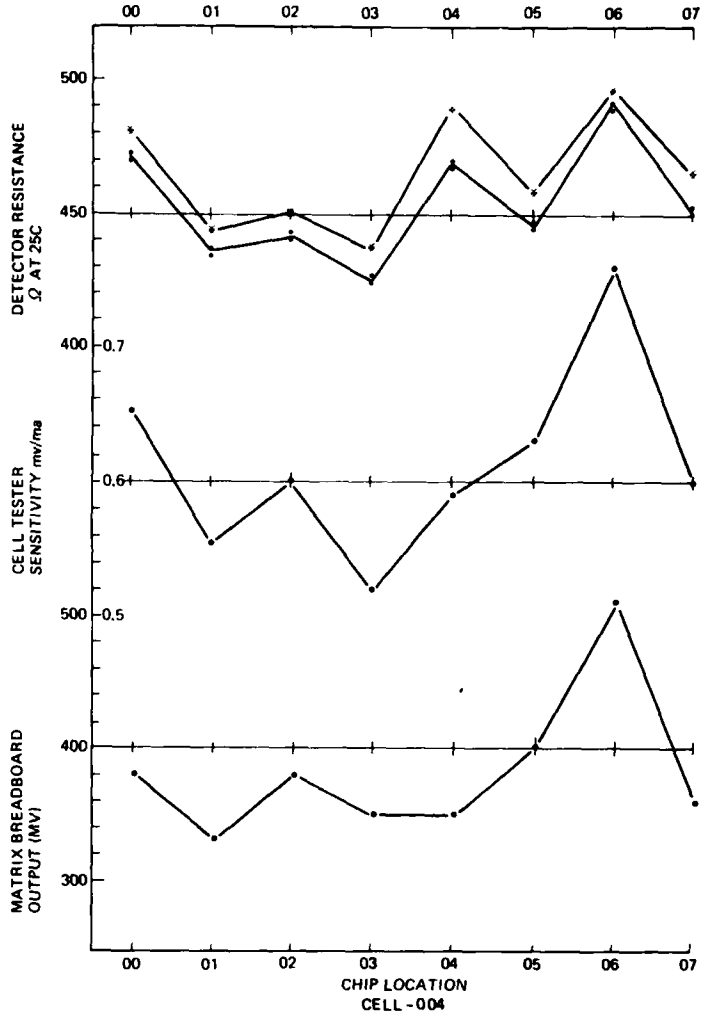
TOP: RESISTANCE • INNER DETECTOR
x EDGE DETECTOR
MIDDLE: CELL TESTER SENSITIVITY
BOTTOM: MATRIX OUTPUT A=40

Figure 6-9. Comparison between signal and resistance.



TOP: RESISTANCE • INNER DETECTOR x EDGE DETECTOR
MIDDLE: CELL TESTER SENSITIVITY
BOTTOM: MATRIX OUTPUT A=40

Figure 6-10. Comparison between signal and resistance.



TOP: RESISTANCE • INNER DETECTOR x EDGE DETECTOR
MIDDLE: CELL TESTER SENSITIVITY
BOTTOM: MATRIX OUTPUT A=40

Figure 6-11. Comparison between signal and resistance.

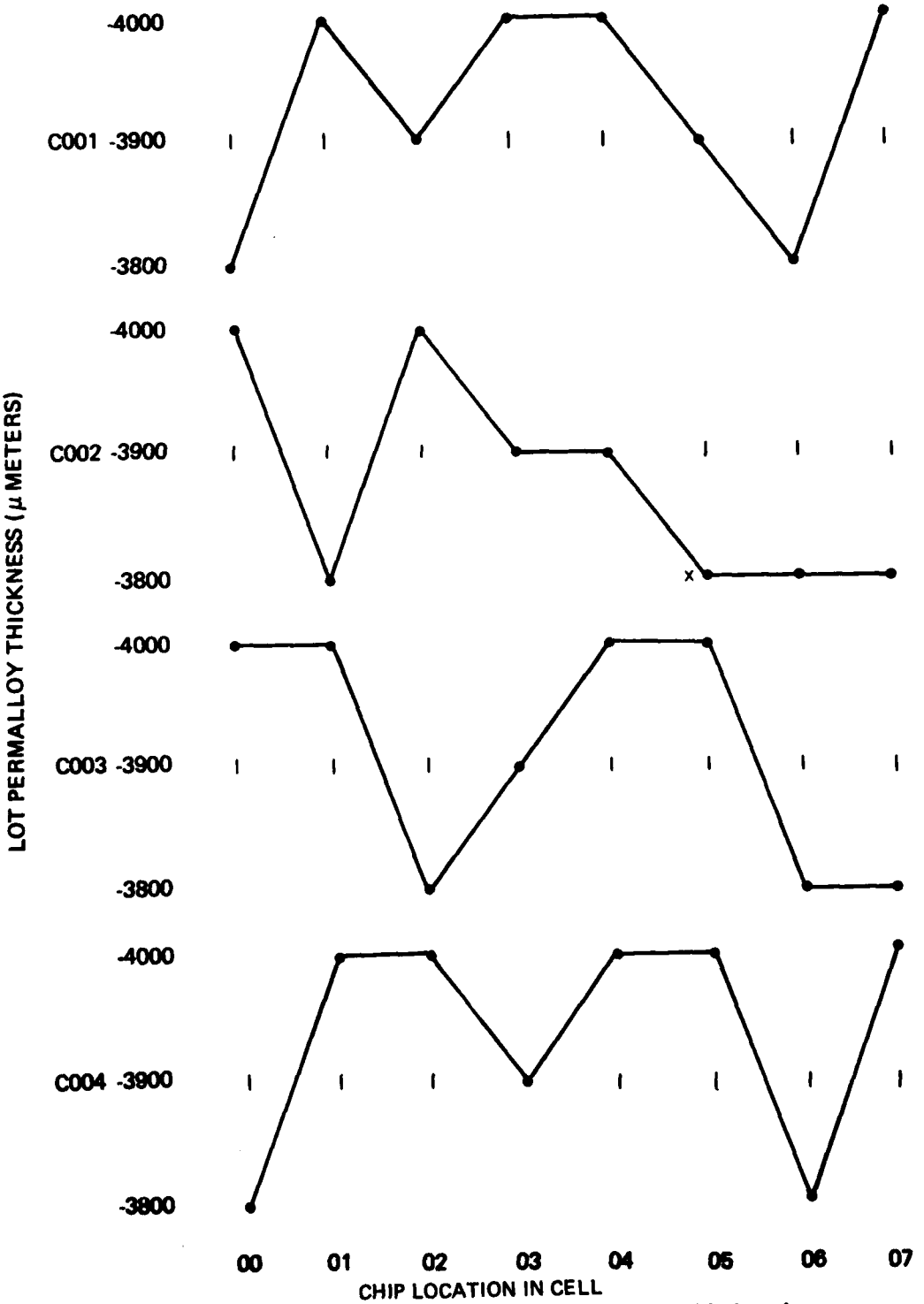


Figure 6-12. First yield run permalloy thickness vs cell chip location.

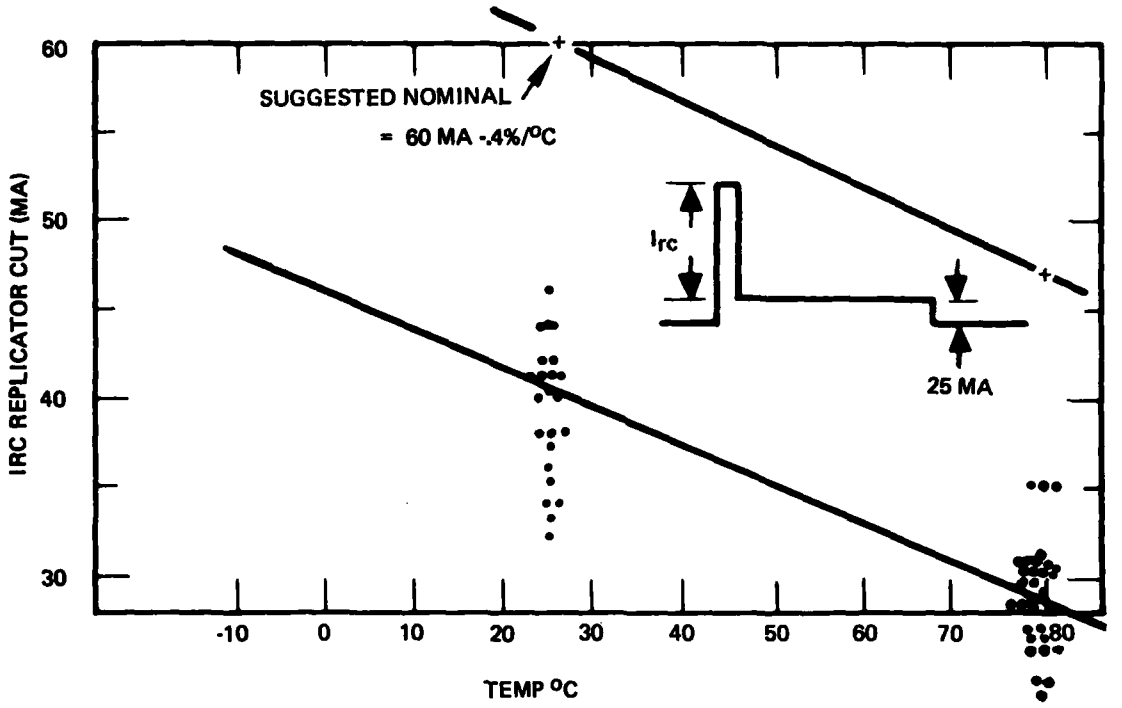


Figure 6-13. Replicator cut pulse.

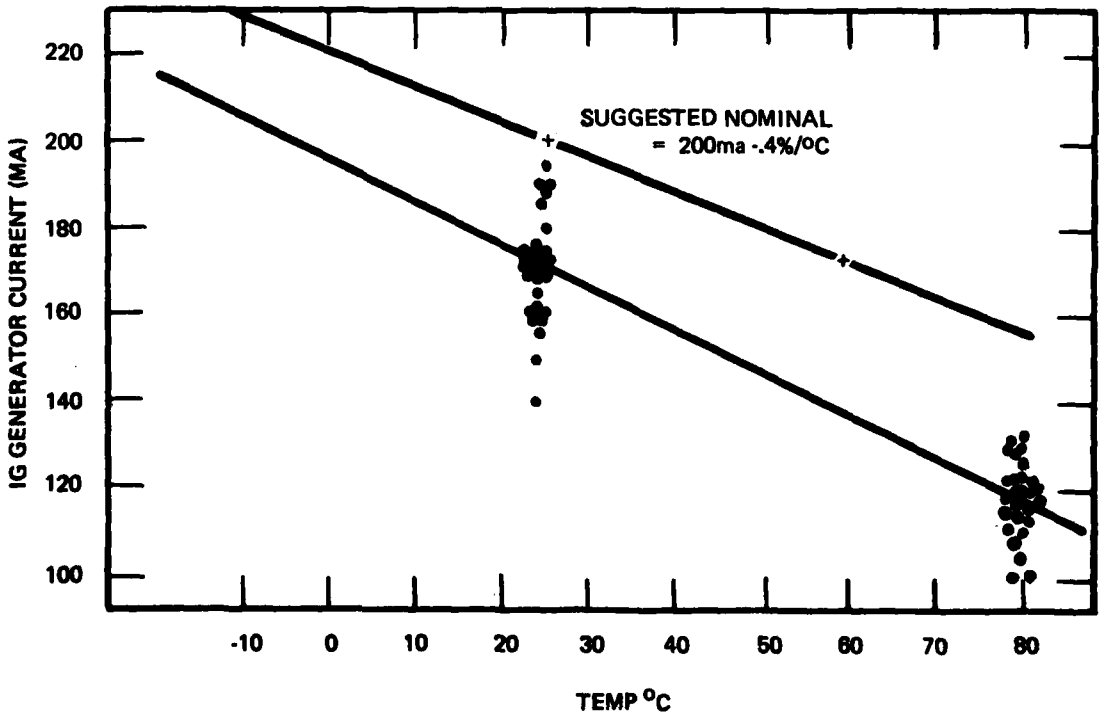


Figure 6-14. Generator min amplitude.

Factors listed to the right of the nominal signal of Figure 6-15 are factors which shift signal amplitude and baseline thereby reducing composite 1-0 window in worst case. Detector mismatch is a statistical variation in detector sensitivity between active and dummy detectors. The back-to-back configuration of the D1106 chip provides significantly reduced mismatch over the 1067 chip used on the SSDR program. Rotating field sensitivity is a change in bubble influence on the detector from a preceding or a trailing bubble. $D\phi/DT$ is voltage induced in the cell by coil current.

A guard band for random detector noise is included in the budget for the 10^{-8} soft bit error requirement of the contract. In evaluating the error rate of a number of individual chips on the multiplexer of the prototype memory module it was found that the sense budget will shrink approximately 20 percent of nominal signal for a 10^{-8} error rate guarantee.

The 1.5 millivolts remaining on the budget times amplifier gain provides 60 millivolts of signal to cover system noise, threshold set uncertainty and gain variability. Because chip and cell measurements indicate a potentially marginal situation relative to contract goals, an optional threshold per chip circuit was designed into the memory module.

Measurements of the module sense performance indicate that the circuit is not required for most applications. The circuit can be used in those applications requiring temperature extremes or low error rates.

6.1.5 Statistical Summary

Wafer probe data were fed into Rockwell's time share computer for compilation. Summary results are given in Table 6-5. Data is for chips which passed a 6 Oe window criteria as opposed to data given in para 6.1.2 which is for installed die. Notice that bias deviation is excellent for the run, which made bias matching a simple process during cell assembly. The tight matching of the cells is attributable to a wafer selection criteria on collapse field of from 160 to 164 Oersteds.

Detector resistance measurements made on the probe station at the beginning of the run were found to be inaccurate as confirmed by DVM measurements (See para 6.1.2) which exaggerated variation.

6.2 MANUFACTURING YIELD RUN

Two 8-wafer lots were started by manufacturing in mid-September of 1979. Seven wafers of the first lot were completed and found to have excessive missing permalloy elements caused by poor adhesion of the permalloy. No electrical tests were perfomed. Six wafers of the second lot were completed in November. A major problem occurred during ion milling when the wafer temperature rose excessively which burned the photo resist. These wafers were probed to obtain 33 die (2 cells) for further cell tests. Table 6-6 gives results of the tests in terms of yield. Cost considerations forced discontinuation of further processing and testing as part of this contract.

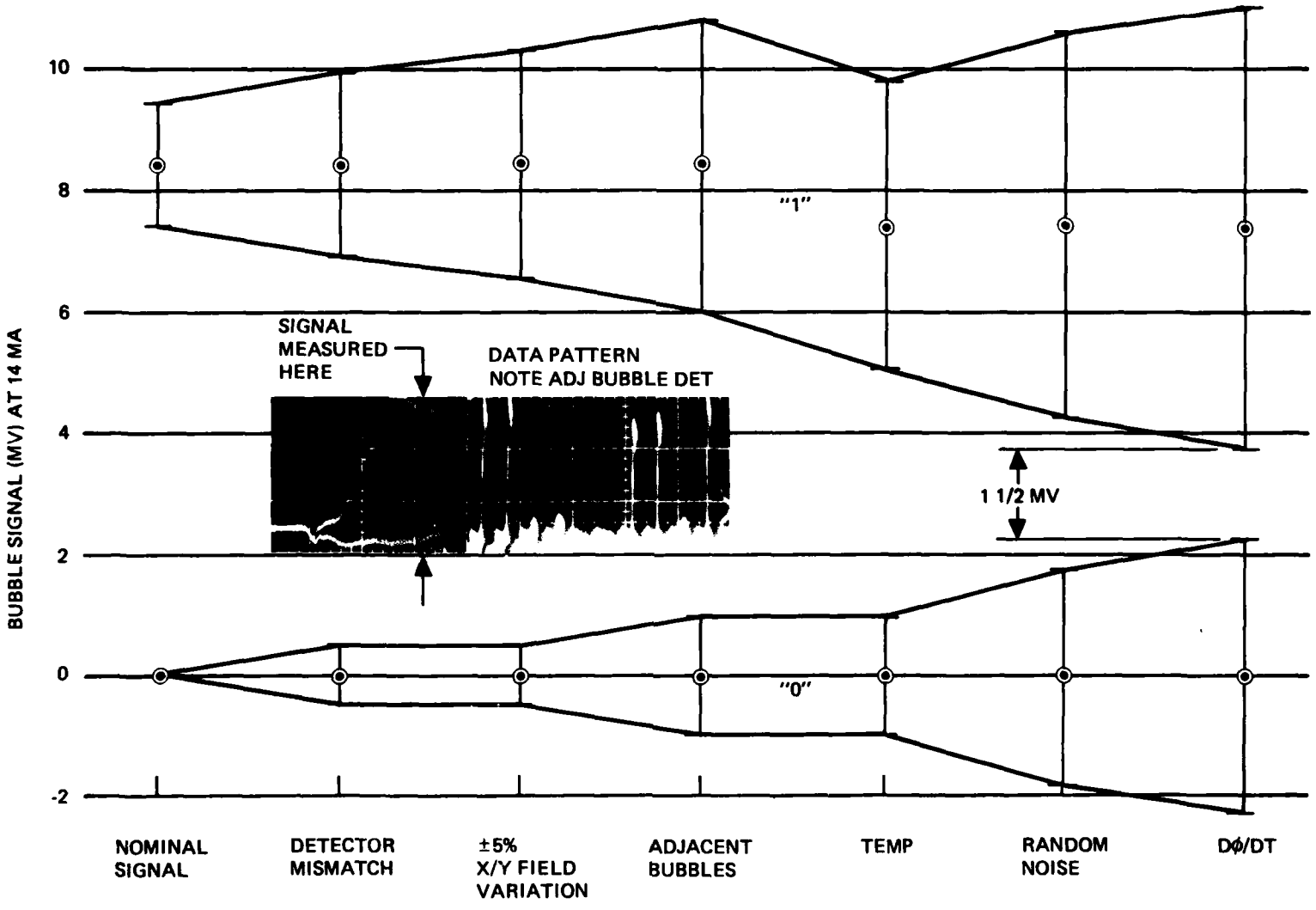


Figure 6-15. Cell test sense budget.

TABLE 6-5. WAFER PROBE TEST DATA STATISTICS FIRST YIELD RUN

	30C; 40 Oe Bias		30C; 50 Oe Bias		60C; 50 Oe Bias		Temp. Coeff.	DET Resistance Ω			
	Lower	Upper	Lower	Upper	Lower	Upper	%/°C	DET 1	DUM 1	DET 2	DUM 2
Ave	139.6	151.1	141.1	154.5	129.3	144.9	-0.206	499.0	504.8	517.4	518.4
Sigma	3.1	4.1	3.5	3.0	2.9	2.7	0.087	93.3	69.2	71.6	71.7

TABLE 6-6. PROBE YIELD VERSUS INSPECTION YIELD MANUFACTURING YIELD RUN

Wafer	Wafer Probe Yield	Visual Inspection Yield	Accepted Die
705-2-2B	17%	44%	10
705-2-2D	19%	56%	16
704-1-2F	0	18%	–
705-2-3H	7.9%	31%	7
703-2-3B	0	23%	–
704-2-2F	0	14%	–
		Total Die available for cell test	33

7. PROTOTYPE MODULE DESIGN AND TEST

A prototype of a memory module was built and tested in order to provide a model for evaluation of circuit and system design, and user interface concepts. The completed module is shown in Figure 7-1. An electronics board containing interface, power switching, timing, operator current sources, and part of the coil drive matrix is a wire wrap board with plug-in integrated circuits. A wire wrap board was chosen over a multilayer board because of program fund availability. This was a fortuitous choice because a number of circuits required modifications which were easily implemented during evaluation. A few circuits which will be identified in the following sections require more development in order to improve dependability and manufacturability of the basic module.

A single storage board was built and populated with five memory cells. Four circuit layers were required in the board plus a voltage and ground layer. Few problems were found during checkout of the board as compared to the electronic board. Isolated improvements to the basic layout would be beneficial in order to eliminate jumpers from the board.

7.1 ELECTRICAL BLOCK DIAGRAM

A block diagram of the prototype for the minimum system is shown in Figure 7-2. A fully populated system of eight boards requires expansion of the coil driver to a 4 by 16 matrix, seven additional sense multiplexers, and additional selection circuitry.

Basic function control is provided by a 20 MHz clock which sequences a PROM to provide a 28 function by 256 step sequence. Sixteen data bits, board address, cell address, and memory control are provided by two interface sections which can be operated independent of one another. Power switching and status monitors are provided by the power control section.

A separate sense multiplexer is used on each storage board in order to provide detection of the low level signals. Outputs are high level TTL open collector logic at the board interface. Operator current sources are on the electronics board with the current flowing to the selected board via the cell selection switches. Four coil drive hybrids are provided on the electronics board with two on each storage board. In this way additional capacity can be added without adding a commensurate amount of electronics.

7.2 SENSE MULTIPLEXER DESIGN

Although multiplexed sensing involves careful engineering of chip magnetic assembly and printed circuit board, the approach results in at least an order of magnitude reduction in power consumption and components devoted to detection. Multiplexing permits a complex circuit to be shared by using a simple switch per cell.

One of eight chips in each of eight cells is connected on a sense bus as shown in Figure 7-3. Each chip has two detector pairs for alternate bit detection which are connected through steering diodes during alternate cycles. Two cell select switches (half an IC) energize an addressed cell for both operator and sensing functions. A common cell select switch is used to economize circuitry since little noise is added to the sense bus because the switch is a small impedance to coupled noise relative to detector impedance.

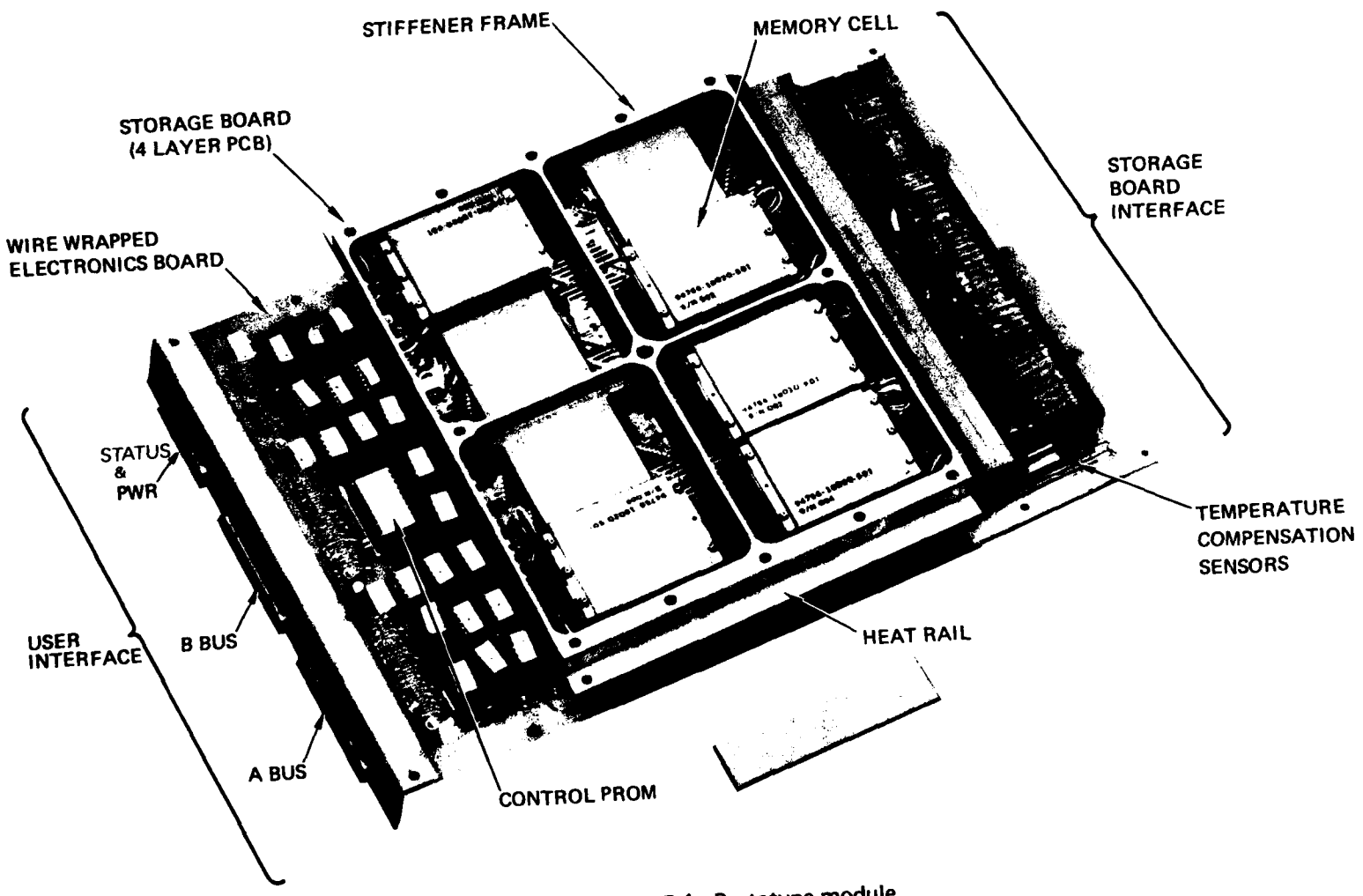


Figure 7-1. Prototype module.

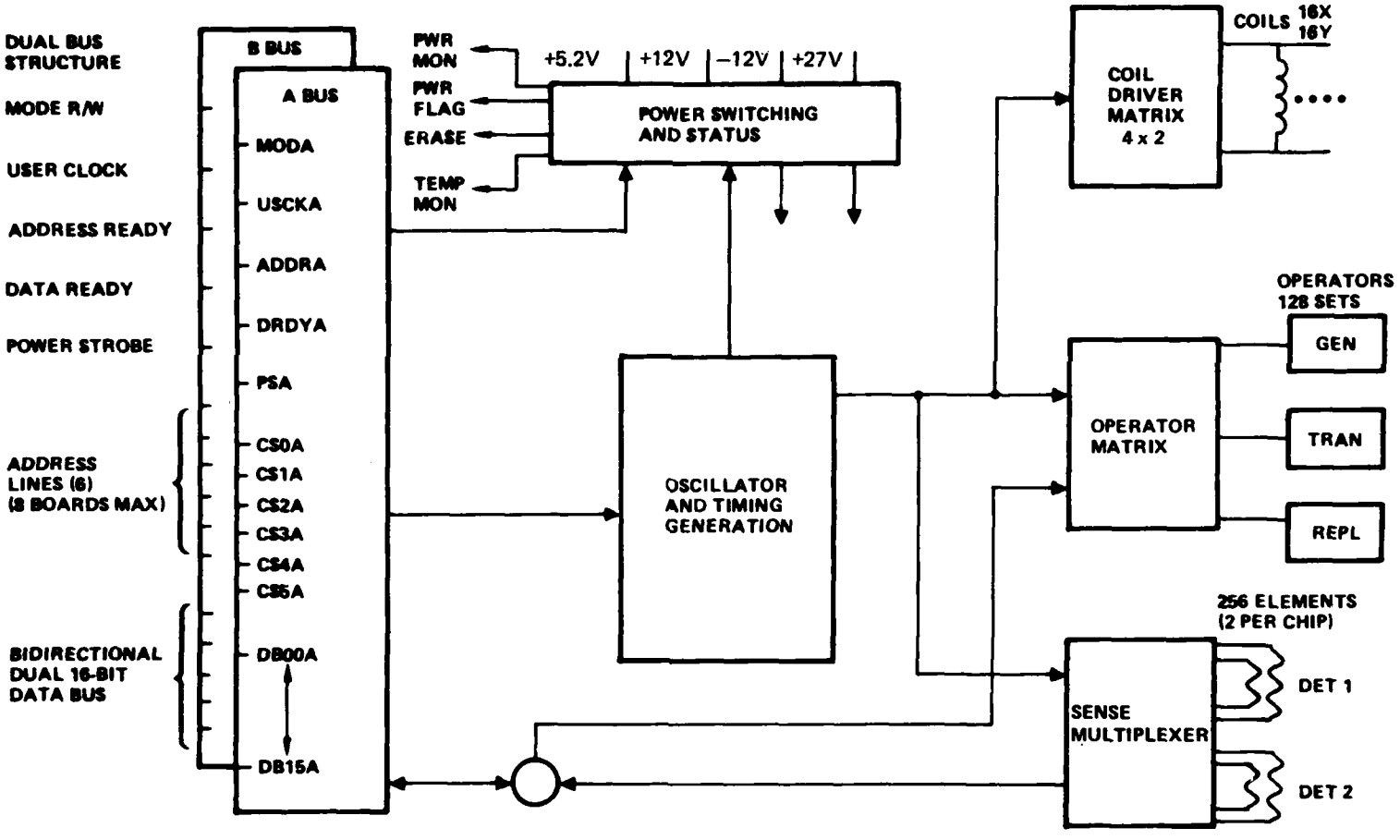


Figure 7-2. Electrical block diagram.

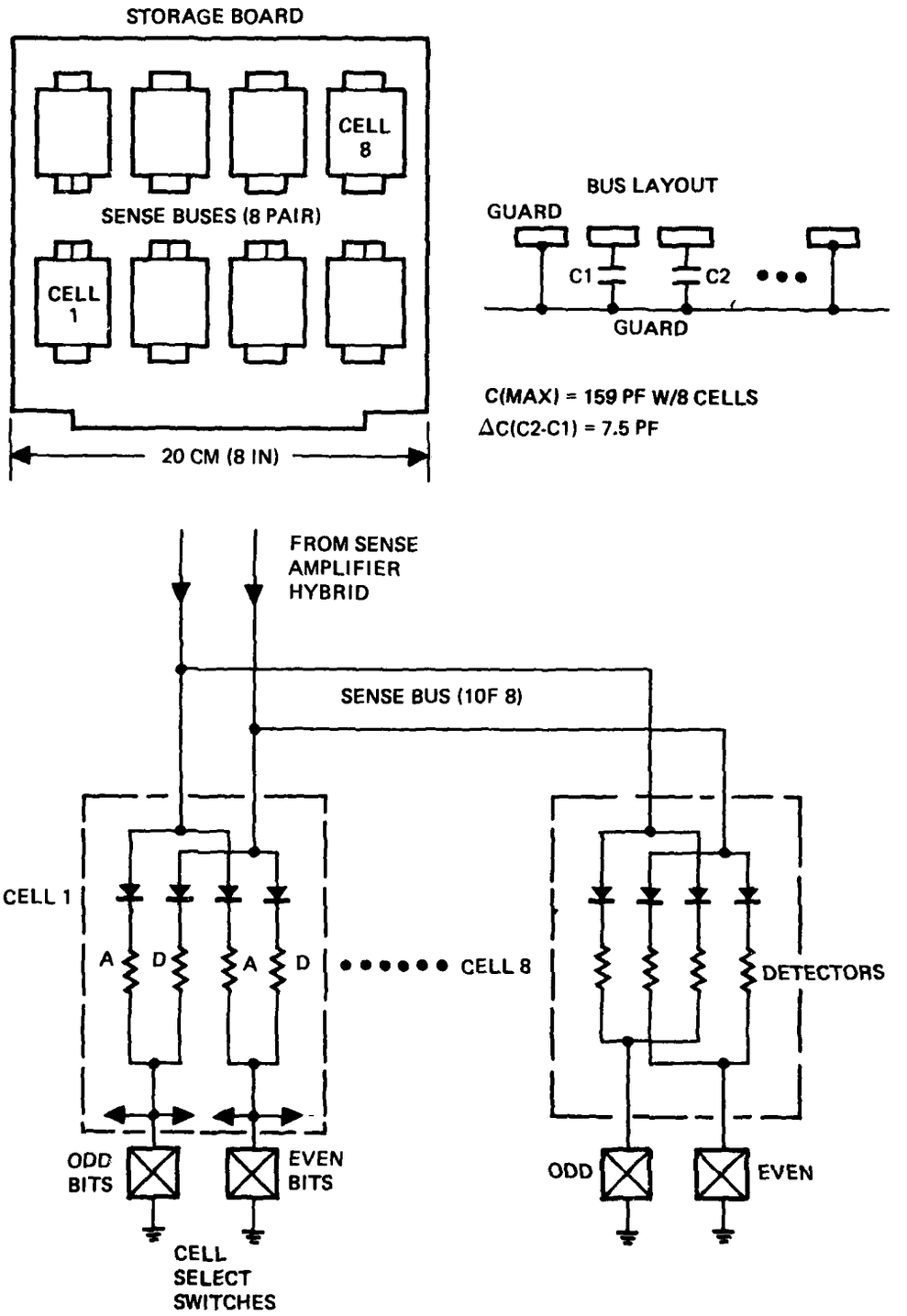


Figure 7-3. Sense multiplexer configuration.

AD-A093 642 ROCKWELL INTERNATIONAL ANAHEIM CA AUTONETICS STRATEG--ETC F/6 9/2
BUBBLE MEMORY MODULE.(U)
DEC 80 O D BOHNING, F J BECKER NAS1-14174
UNCLASSIFIED C80-569/201 NASA-CR-3380 NL

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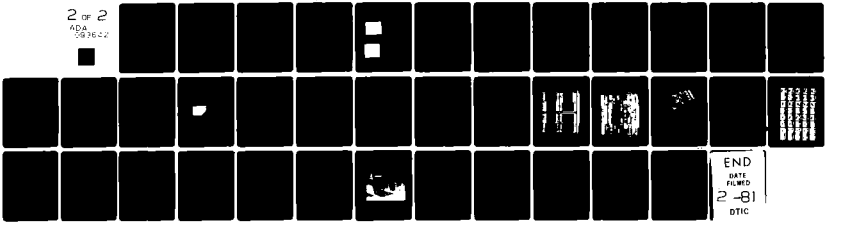
AD A093642



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Main considerations in the design include maintaining a tight differential pair, guarding against external noise, and producing a low and balanced line capacitance. Cells are placed on the storage board so that sense cables connect onto the sense bus to an isolated, completely guarded center section of the multilayer board as shown in Figure 7-4. Minimum practical line to line spacing and line width (both 7 mils) are used so that line capacitance for a fully populated board is less than 160 picofarads and differential unbalance is less than 7.5 picofarads. Results of breadboard demonstration of the simulated multiplexer indicate that cells can be interchanged and that bus loading can be varied with barely perceptible changes in signal shape or threshold. Breadboard tests demonstrated the feasibility of removable cells. Table 7-1 gives the measured values of capacitance for both the storage board and the carrier conductors. Unbalance of approximately seven picofarads on two of the differential sense lines can be reduced to less than two pf by slightly modifying the artwork. Bridge current pulse recovery is affected by both unbalanced bus capacitance and unbalanced detector resistance. The difference between recovery exponentials of the detectors using measured circuit elements as shown in Figure 7-5 can be minimized best by tight control of bus and carrier capacitance.

7.2.1 Sense Circuit Design

An operational amplifier based approach was chosen as a detection circuit (Figure 7-6) because of its lower power and for its ability to handle higher input voltages than most differential amplifiers. Common mode voltage at the amplifier's input range from seven to ten volts due to the bridge current in the detector and semiconductor voltage drop. Input offset can be as high as 100 millivolts due to detector resistance unbalance and accumulated semiconductor tolerances.

Control of offset is accomplished by amplifying the bubble signal of about 8 millivolts to the maximum safe amplifier limit and by AC coupling the single ended amplifier output to a comparator. AC coupling the amplifier output instead of the input eliminates criticality of restoring dual capacitors having low level signals and eliminates some parts.

Performance of the amplifier circuit with a pulsed input in the presence of offset is shown in Figure 7-7. Offset at (A) of Figure 7-6 is plotted against the "one" and "zero" signal at comparator input (B). Offset rejection is about 200 to 1 with an amplifier input offset range of $\pm$ 200 millivolts.

Driving detectors with pulsed current rather than direct current increases signal amplitude while minimizing detector power dissipation. Detector current of 10 to 14 milliamps is pulsed on for 2.5 microseconds in every other cycle (12 microseconds) for each detector in order to minimize detector temperature. Recovery of the sense bus after bridge current turn on plus time for signal detection establishes minimum bridge current pulse width.

Offset at the amplifier input establishes maximum gain relative to supply voltage. Table 7-2 lists offset of each contributor based on this data. An amplifier gain of 40 was chosen as the safe maximum.

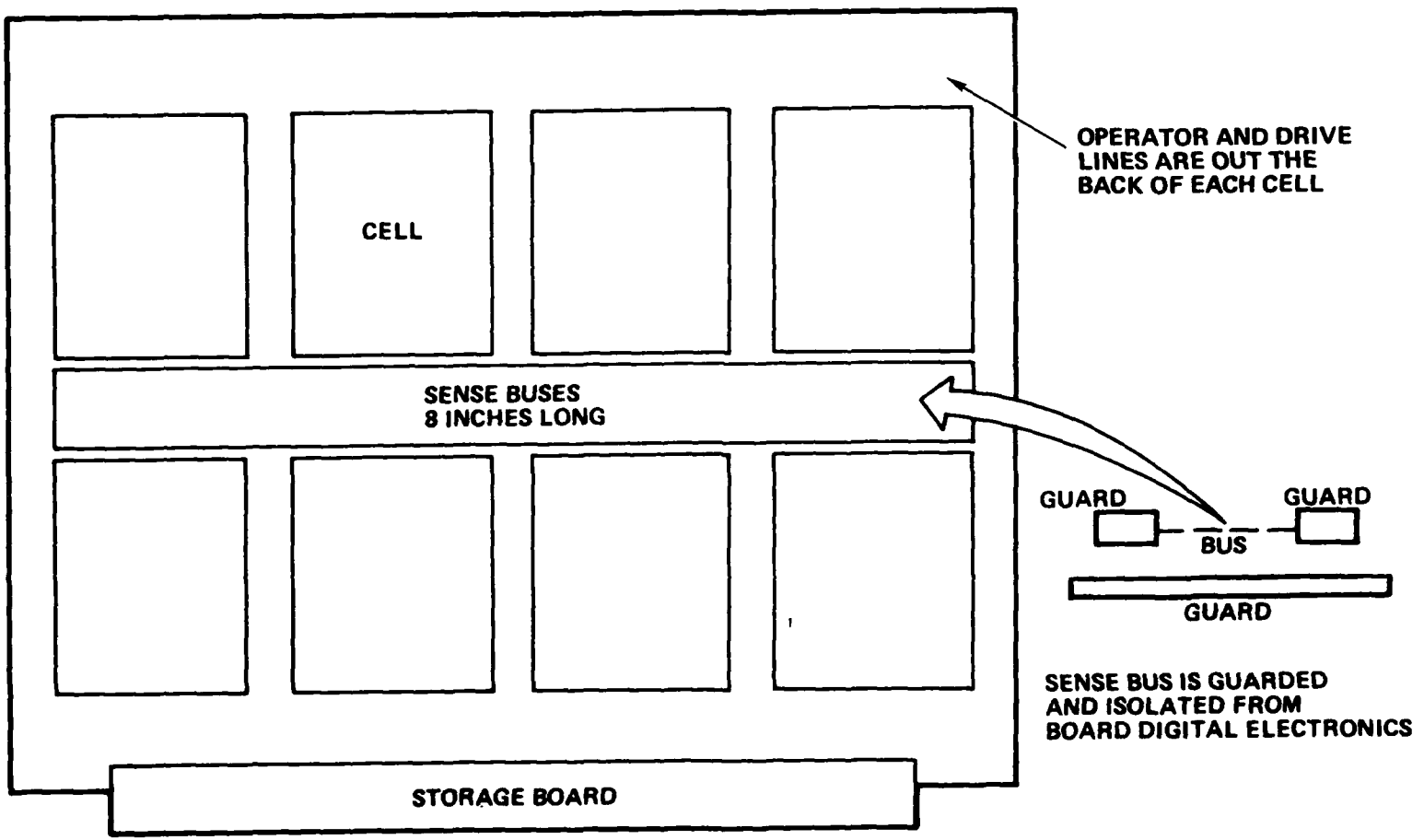
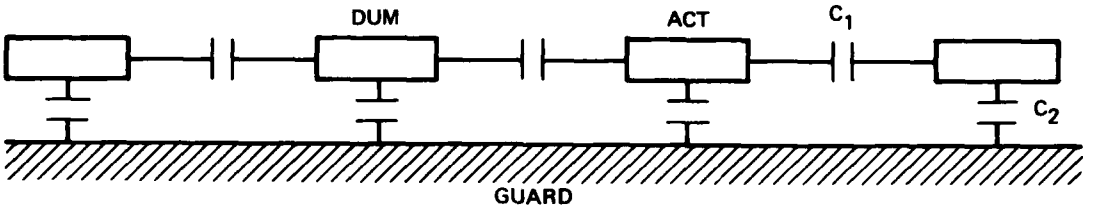


Figure 7-4. Sense bus layout strategy.

TABLE 7-1. BOARD AND CELL BUS CAPACITANCE



	Dummy to Guard	Active to Guard	Dummy to Active	C_1 DUM–ACT Guard "Guarded"	Δ DUM–ACT	Approximate C_2
SA1	35.5	34.5	29	6.5	1	29
SA2	42	35.5	30	7	6.5	33
SA3	44	41.5	34.0	7.5	2.5	36
SA4	45	42.5	34.0	7.8	2.5	38
SA5	35.5	36.0	30.0	7.0	0.5	30
SA6	37	44.5	30.4	7.0	7.5	35
SA7	45	44	35.0	8.2	1	37
SA8	44	46.5	36.0	8.1	2.5	38
Cell Min	11.3	11.5				
Cell Max	14.6	14.5			0.2	

Typical bus capacitance with 8 cells = 136 pf
Maximum bus capacitance with 8 cells = 159 pf
Maximum bus unbalance = 7.5 pf

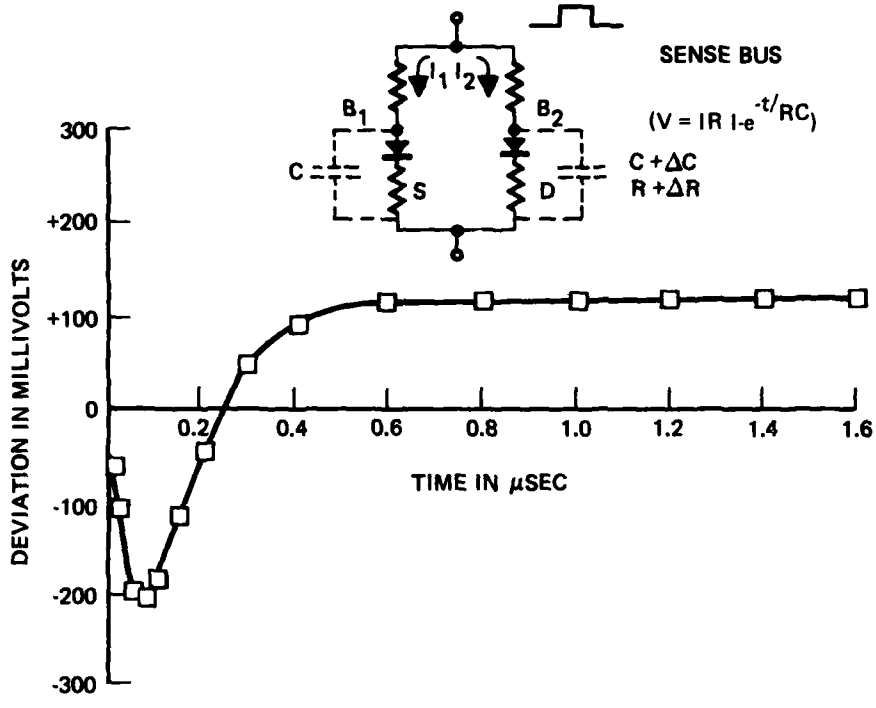


Figure 7-5. Bridge current recovery for DC = 15 pf, ΔR = 5Ω.

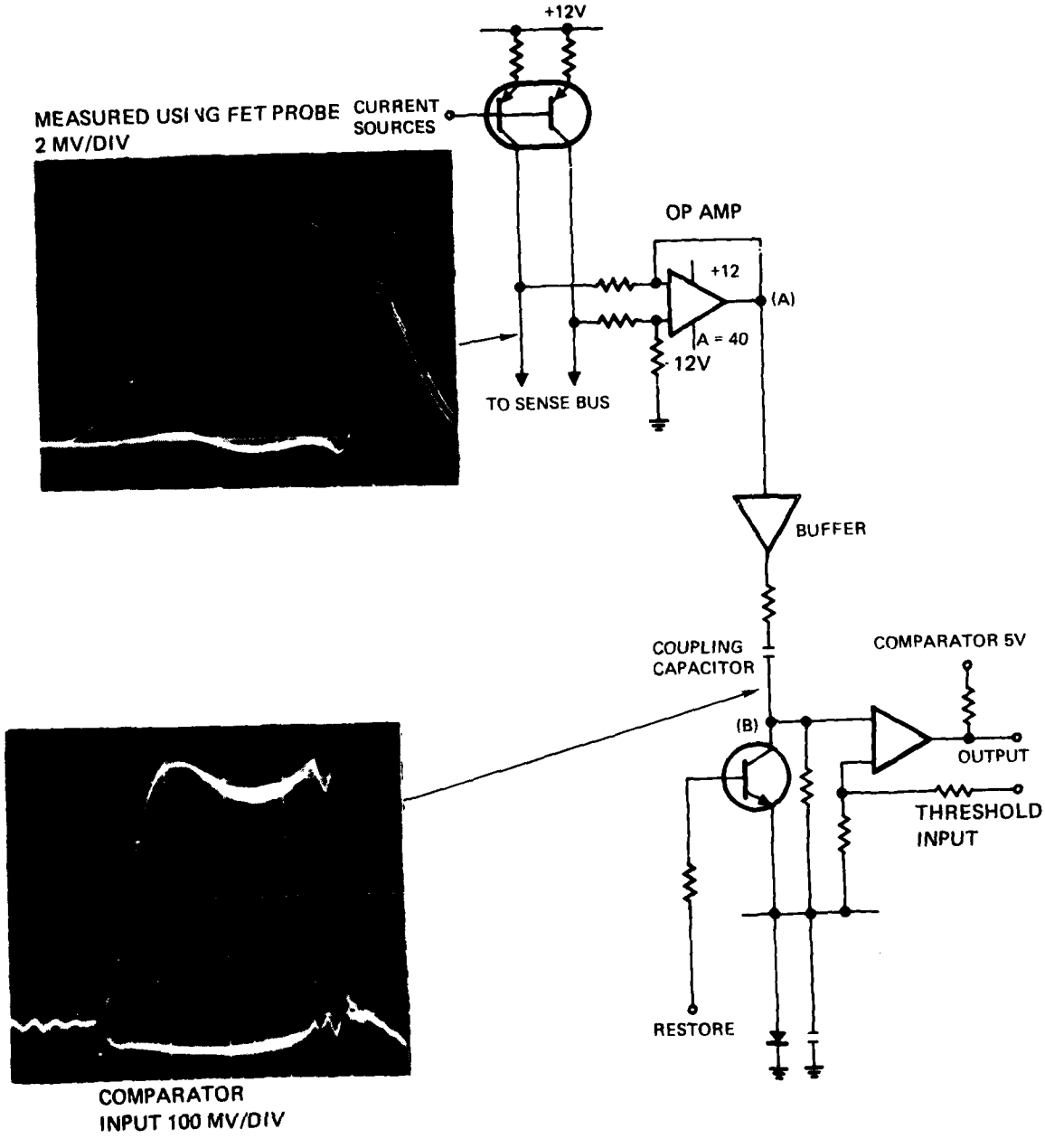


Figure 7-6. Bubble sense amplifier circuit.

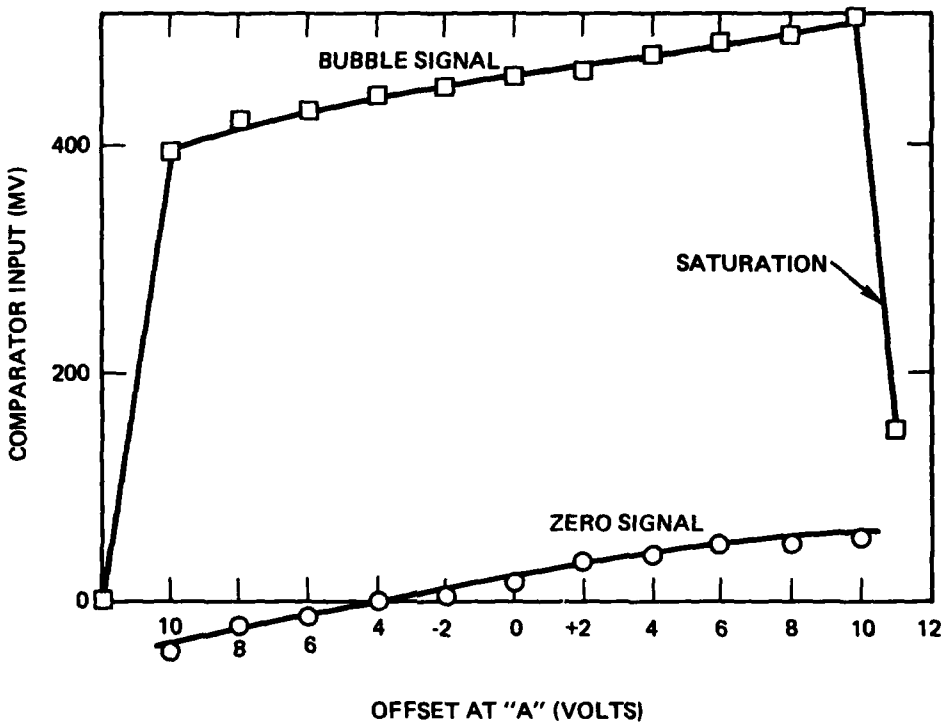
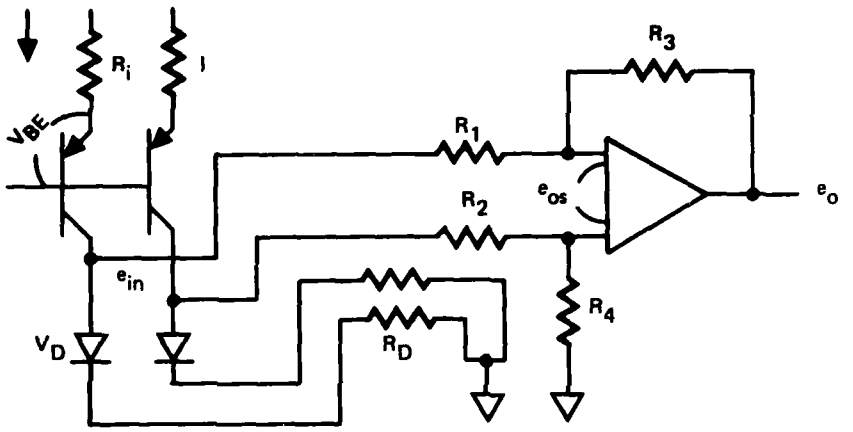


Figure 7-7. Amplifier offset rejection performance.

TABLE 7-2. OFFSET CALCULATION



ASSUME I = 12 MHz
$R_D \approx 600\Omega$
$e_{in} \approx 8V$
$A_{CL} \approx 40$

Maximum error in e_0 for above circuit:

Parameter	Δ	Δe_{in}	Δe_0	Rationale
ΔV_{BE}	0.005V	0.020	0.80	Spec
ΔV_D	0.050V	0.050	2.00	Est
R_D	3Ω	0.036	1.44	Data
R_1	0.1%	–	0.32	Spec
R_2	0.1%	–	0.32	Spec
R_3	0.1%	–	0.32	Spec
R_4	0.1%	–	0.32	Spec
ΔI	0.2%	0.0144	0.58	Spec (R_D is ± 0.17)
e_{os}	0.005V		0.80	Spec
		Total Offset	6.90 Volts	

7.2.2 Sense Hybrid Design

Two four channel sense amplifier hybrids are used on each memory module. Bridge reference, threshold level and timing signals are generated external to the hybrid. Four channels per ceramic substrate are hermetically sealed in a single package. A single conductor level substrate, noncritical parts alignment, and low power components are features of the design which permit conventional hybrid manufacture. An LSI version of the design could accommodate techniques such as matched resistor pairs and compensation to achieve improved performance. General description and pin identification of the part is given in Figure 7-8.

7.2.3 Programmable Sense Threshold Circuit

A circuit which provides a unique threshold for each chip was designed into the storage board as a precaution in the event sense channel noise exceeded expectations. It is a simple low power circuit (Figure 7-9) requiring two IC's, eight diode packages, and a resistor per chip (64). An address line energizes a threshold rail with the reference voltage which supplies the eight sense channels with threshold voltages. During checkout, module sensing of detection was found to be adequate without the full use of the circuit. Instead the reference voltage was connected at point A which provides a separate threshold per channel. Retaining the circuit as part of the design provides capability to improve margin for applications with stringent requirements.

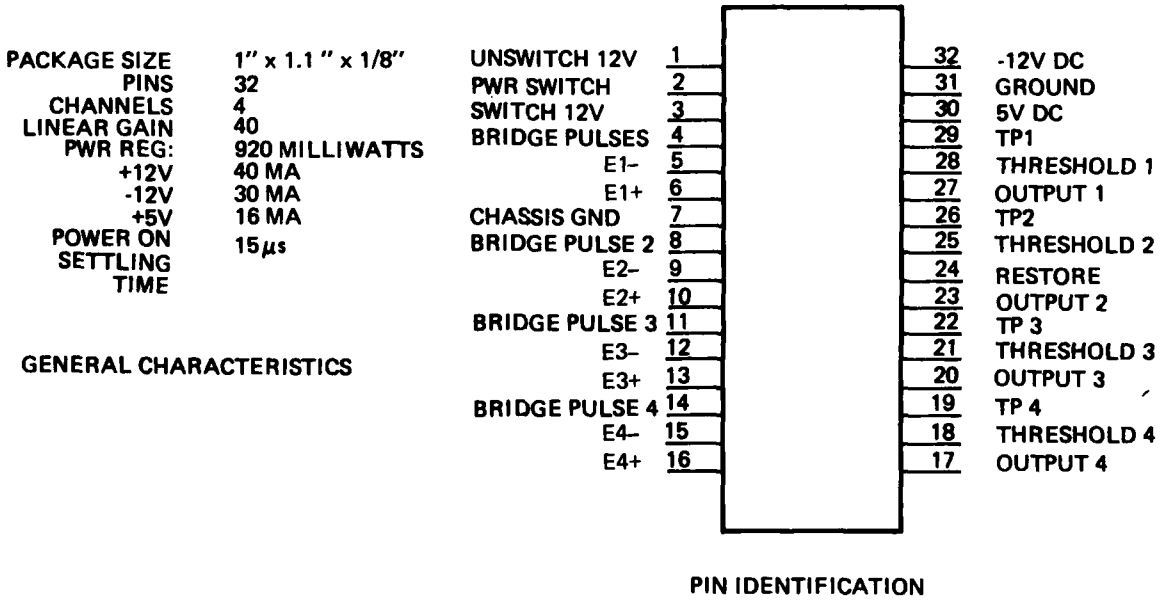


Figure 7-8. Four channel sense hybrid.

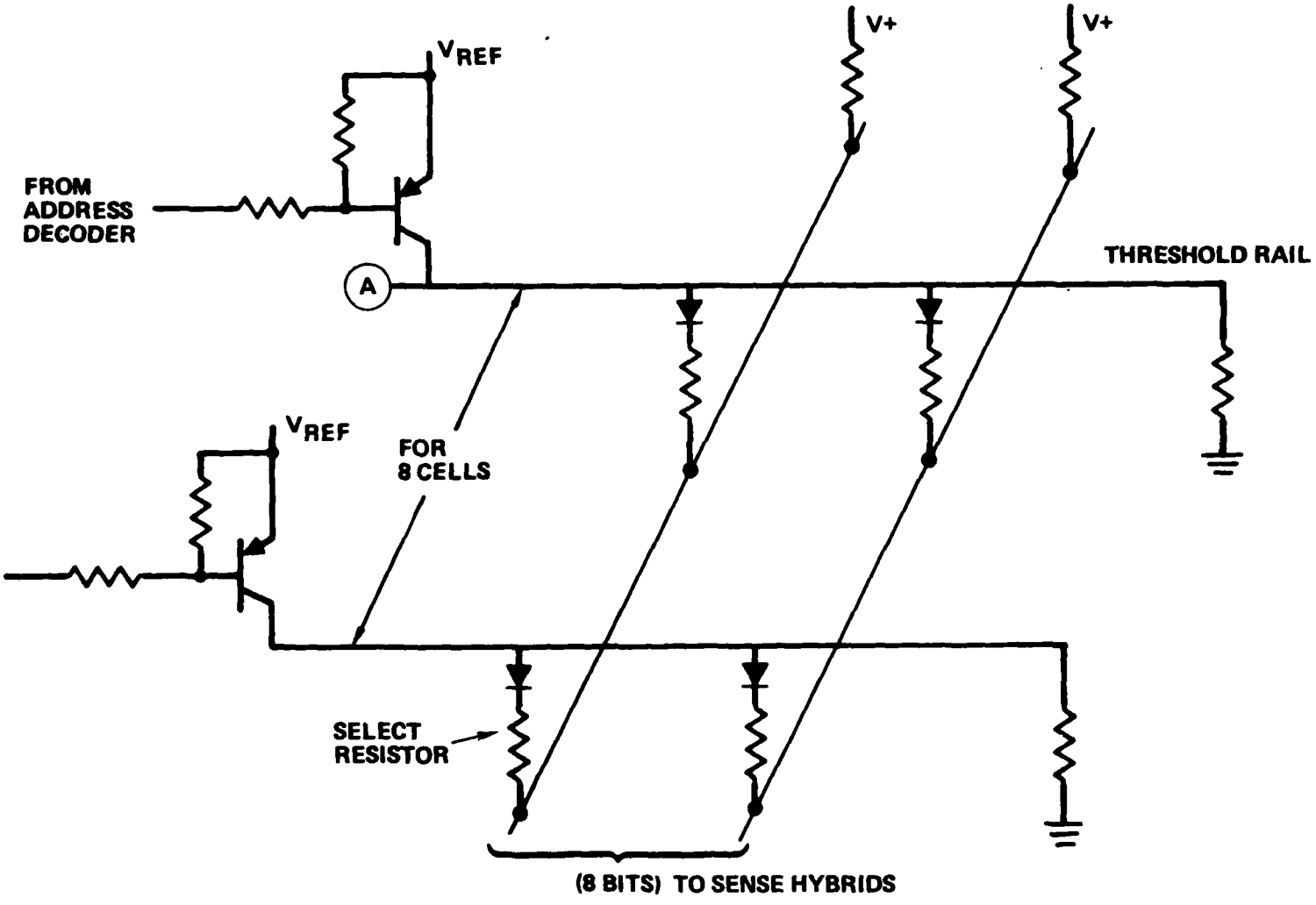


Figure 7-9. Programmable sense threshold circuit.

7.3 COIL DRIVE MATRIX DESIGN

Coil drivers provide current which flows through the coils to create a rotating field. Four switches are used to control current and phasing through each coil as illustrated in Figure 7-10. With switches X1 and X4 on, current rises exponentially in the coil with a (L/R) time constant to a final value of V/R. At about 60 deg into the cycle when the desired peak field is reached, X1 is turned off which forces coil current through D1 from ground through X4. This provides the characteristic shallow decay or flat top of the trapezoidal wave. After about 120 deg into the cycle, X4 is turned off which causes current to exponentially decay to a negative value (-V/R) until energy is dumped at about 180° into the cycle. The above process repeats for the negative half (180 - 360 deg) of the cycle using switches X2 and X3.

By using four timing signals per coil (8 total) a trapezoidal, triangle, or any general waveform combination can be provided which allows optimization of bubble chip operation for a particular cell design. Triangle waveforms require only two digital timing signals per coil but implementation of the triangle waveform is restrictive as related to amplitude and phasing combinations.

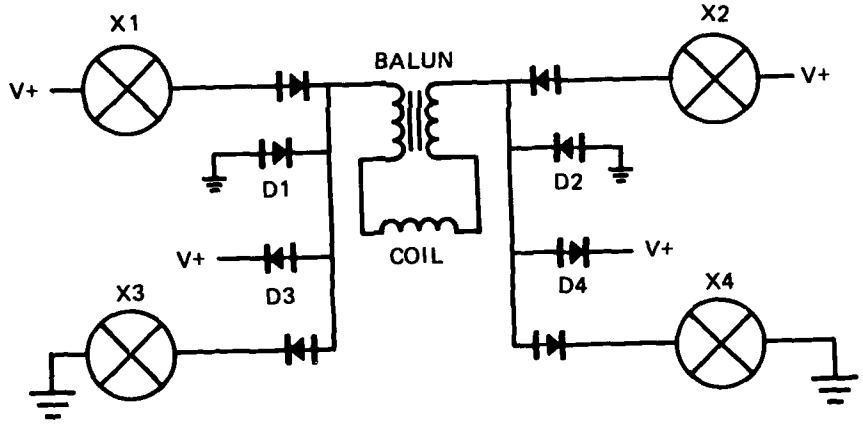


Figure 7-10. Coil Drive Concept.

A matrix design Figure 7-11 was chosen for driving the coils of the cells because of the low risk of the design and because of the lower component count than available alternatives especially for an expanded module of many boards. The design is essentially the SSDR design discussed in [Ref 2] except for modifications to reduce transistor storage time and some simplifications to the design.

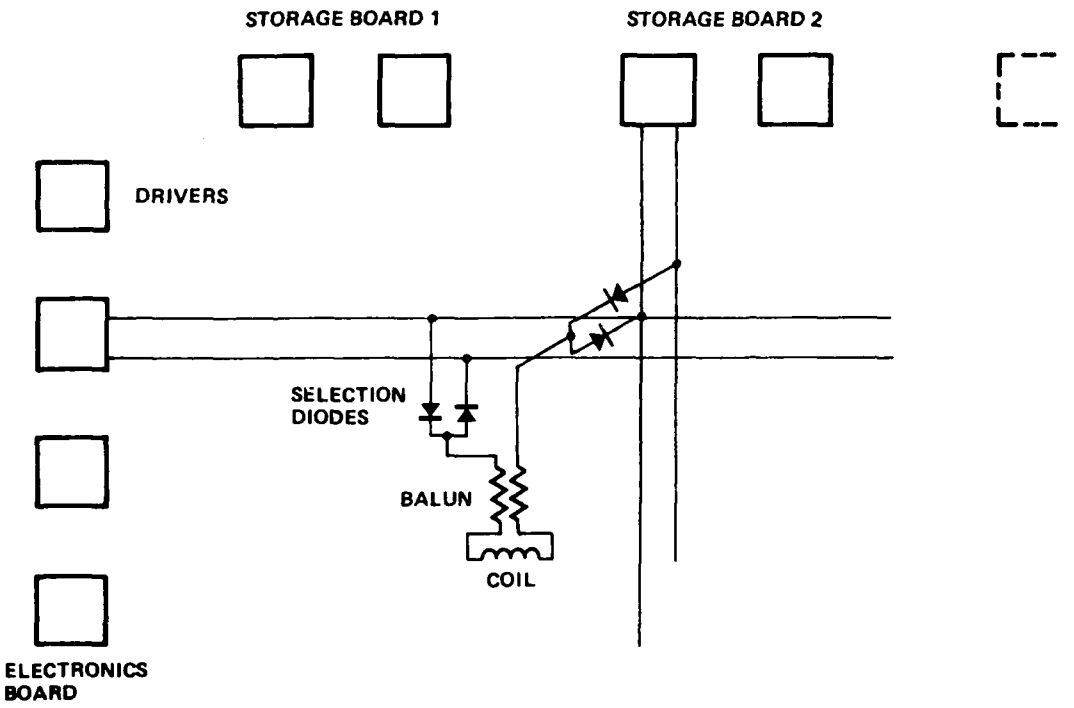


Figure 7-11. Coil driver matrix.

Four diodes and a balun are used with each coil for selection and for isolation between coils in a cell and for isolation of the common mode capacitance of the coils. Four drivers are on the electronics board and two drivers are on each storage board. A full system of eight boards requires 40 drivers (20 X; 20Y) whereas a nonmatrixed configuration would require 256 drivers.

The driver hybrid circuit is shown in Figure 7-12. The top switch is a floating switch which permits large voltage swings on the emitter while the bottom switch is direct coupled. A capacitor, diode, and resistor network is used on the clamp node of each switch to supply energy during switch transistors in order to reduce the potential of secondary breakdown. Physical characteristics of the hybrid and its pin out identification are given in Figure 7-13.

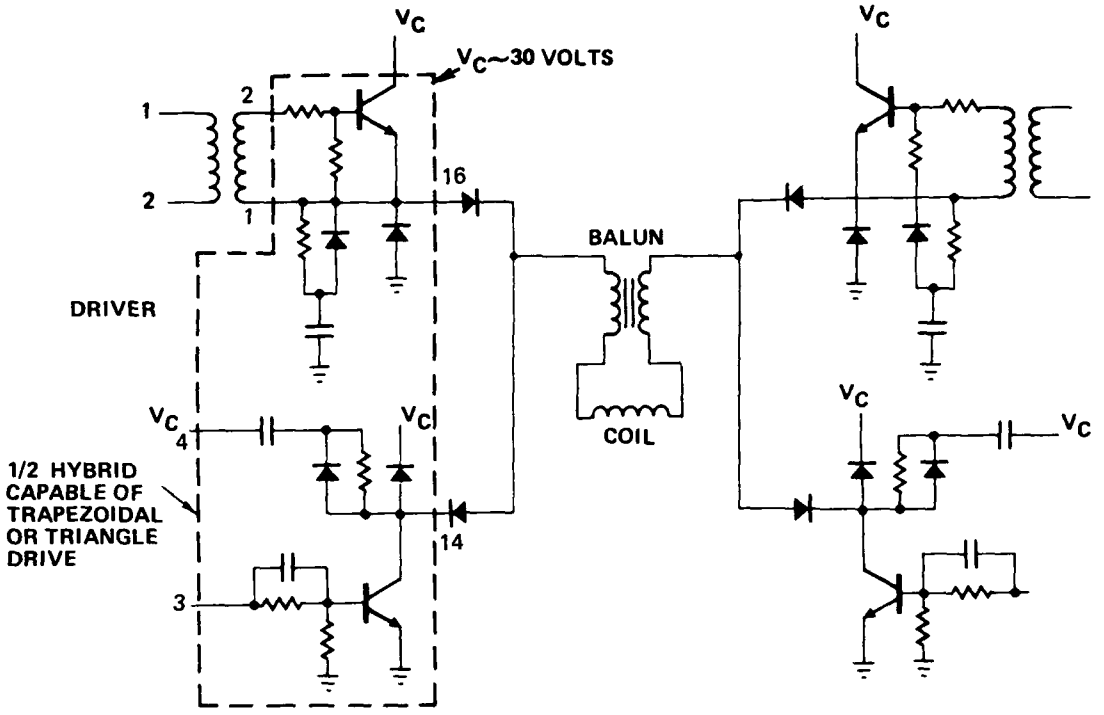
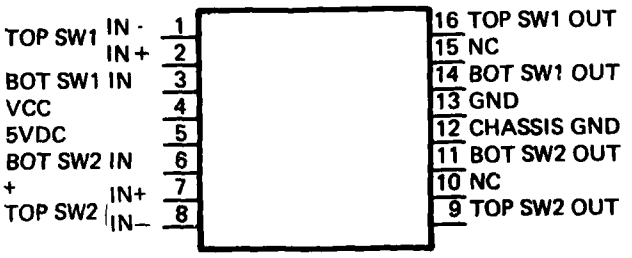


Figure 7-12. Coil driver circuit.

PACKAGE SIZE:	1 in. x 3/4 in. x 1/8 in.
NO. PINS	16
STANDBY PWR	100 MW
SUPPLIES REQ'D:	+5 VDC
	+27 VDC (VCC)
MAXIMUM DISSIPATION	2 WATTS

GENERAL CHARACTERISTICS



PIN IDENTIFICATION

Figure 7-13. Four switch drive hybrid.

7.3.1 Trapezoidal vs Sinewave Drive Tradeoff

During preliminary design of the memory module a tradeoff was made between sinewave drivers and trapezoidal drivers. A sinewave driver had been used on the small coils of the feasibility model [Ref 1] but circuits such as in Figure 7-14 had not been evaluated for larger capacity cells or for a matrix of cells. A trapezoidal drive matrix had been used successfully on the SSDR [Ref 2]. As is summarized in Table 7-3 the sinewave driver represented a riskier, more complex design approach but with potentially lower power than the trapezoidal matrixed drive. As a result of a design review of the tradeoffs, a trapezoidal driver with selected improvements became the chosen approach for the memory module. This choice has simplified implementation, precluded tuning, and allowed concentration on more critical aspects of module design.

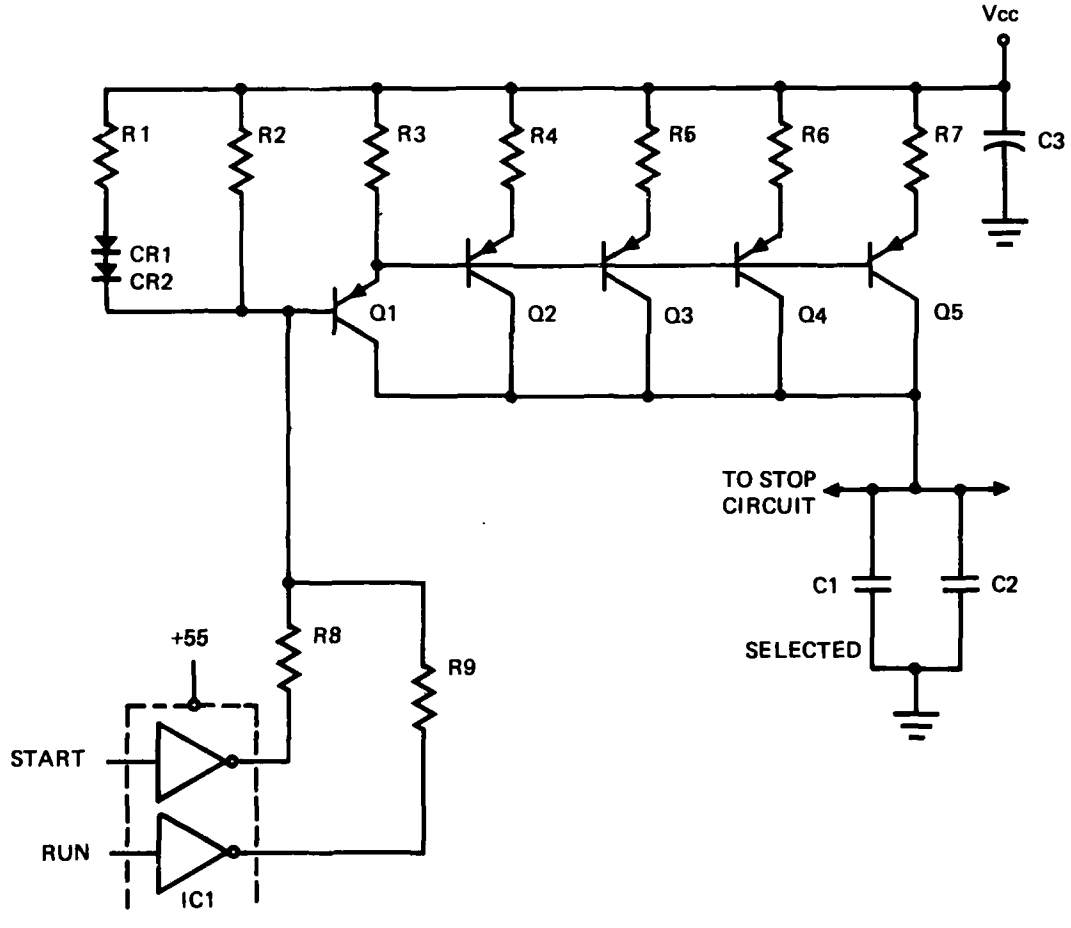


Figure 7-14. Typical start and run sinewave coil driver.

TABLE 7-3. TRADE OFF BETWEEN SINEWAVE AND TRAPWAVE DRIVER FOR 10^7 BIT MODULE.

PARAMETER	SINEWAVE DRIVER PER COIL	SINEWAVE DRIVER MULTIPLEXED (HYBRID SEL SWITCH)	TRAP WAVE DRIVER (HYBRID IZED DRIVER)
NUMBER OF COMPONENTS	EXTREMELY HIGH ~1000	HIGH 500	200
COMPONENT WEIGHT			HIGH BUT CELLS AND FRAME ARE MORE IMPORTANT
POWER - BURST - INCR.	~12 W ~19	11W 18	22W 22
SENSE NOISE			.3 - 1 MV
MEMORY LOSS DUE TO DRIVER FAILURE	6%	50%	28%
SET UP TUNING	TANK TUNED	TANK TUNED	NONE
TIMING ACCURACY			POTENTIALLY THE BEST
AMPLITUDE ACCURACY	PROBABLY THE BEST AFTER TUNING		
LSI APPLICABILITY	EXCELLENT WITH EXTERNAL POWER TRANSISTORS	SAME	POOR BECAUSE OF THE BALUNS AND TRANS-FORMERS
RISK	FEASIBILITY MODEL	NEW	ALREADY DEVELOPED SOME REDESIGN REQ'D
MAXIMUM INCREMENTAL DATA RATE	640 KILOBITS/SEC	640 KILOBITS/SEC	850 KILOBITS/SEC

7.3.2 Drive Field Waveform Investigation

During cell checkout the sense signal was found to vary drastically for low drive field conditions which disagreed with results obtained at the time of characterization of the D1106 chip. Two effects, holding field and intra cycle field uniformity, were found to affect signal for desired low drive field operation. The top two curves of Figure 7-15 show how reducing drive field from 50 to 40 oersteds affects bubble detector influence in a cell which has a five oersted holding field. A sinewave was used in the measurement because of its constant field amplitude locus which excludes drive variables from consideration. This holding field effect was not observed at chip characterization because characterization was done with a SSDR cell (3 Oe tilt) using a trapezoidal drive. The bottom curves show the result of reducing holding field to zero. Both signal peaks are affected similarly when drive field is reduced.

In order to retain necessary holding field and to minimize drive, a locus balanced trapezoidal drive waveform was adopted. Applied digital timing waveforms are unbalanced so that X coil current plus the equivalent holding field current provides a nearly constant field amplitide locus, especially prior to and during bubble strip detection.

Intra field uniformity which was the other aspect of the observed problem, is affected by cell inductance and resistance (L/R) as well as digital timing. Time constant (L/R) of the new cell increased 50 percent for X and decreased 250 percent for Y from the SSDR cell. Digital drive therefore had to be modified to provide a more uniform locus ($X^2 + Y^2$) as well as to provide a tilt corrected locus.

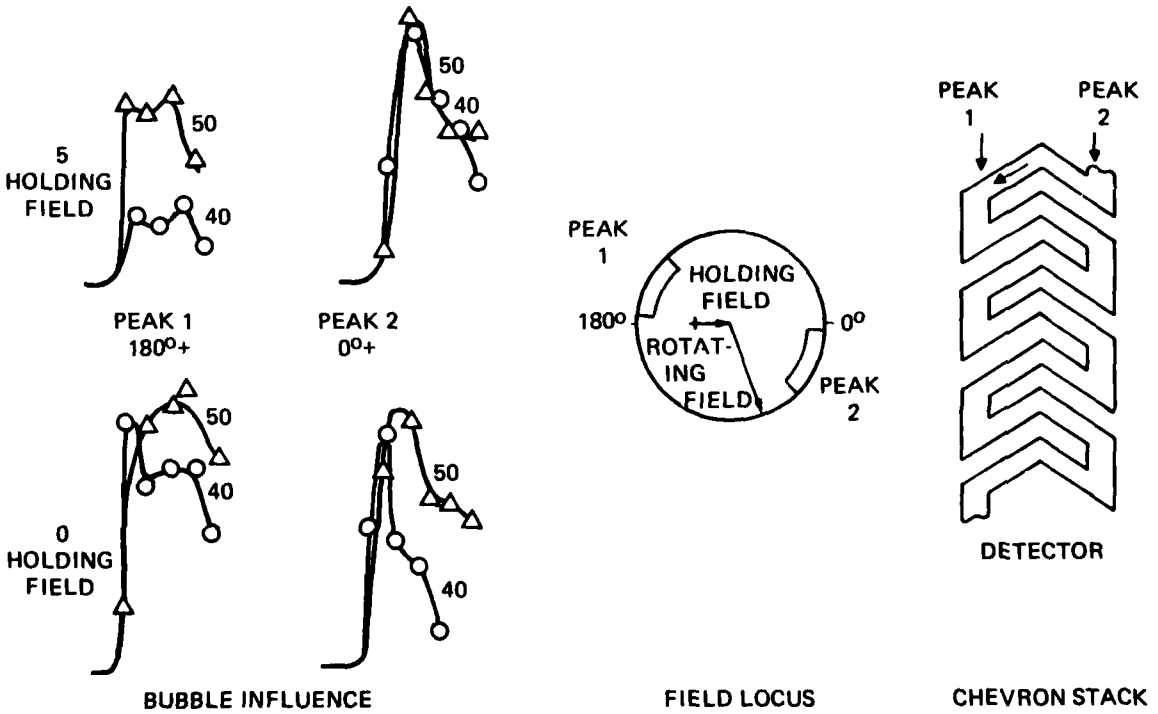


Figure 7-15. Holding field affect on bubble influence (sine drive).

Figure 7-16 is the Drive waveform chosen for the memory module. The plots are calculated values based on the digital switch timing and the (L/R) time constant of the coils, while the photo is actual coil current measured at the module for a single cycle with system voltage at 28 volts. Field Amplitude locus ($A = X^2 + Y^2$) is shown in Figure 7-17. Orthogonality between X and Y fields is excellent but absolute amplitude digresses about ± 15 percent from average. High points at A are desirable from a detection view-point but low points such as at B may limit performance at low drive field, particularly for replicator operation. Further evaluation is desirable. In any case the generalized trapezoidal waveform offers more flexibility in matching coil characteristics to system drive than does a triangle drive. This is because the flat top duration of the trapezoidal wave can be varied to compensate for unequal rise and fall time slopes of the two coils.

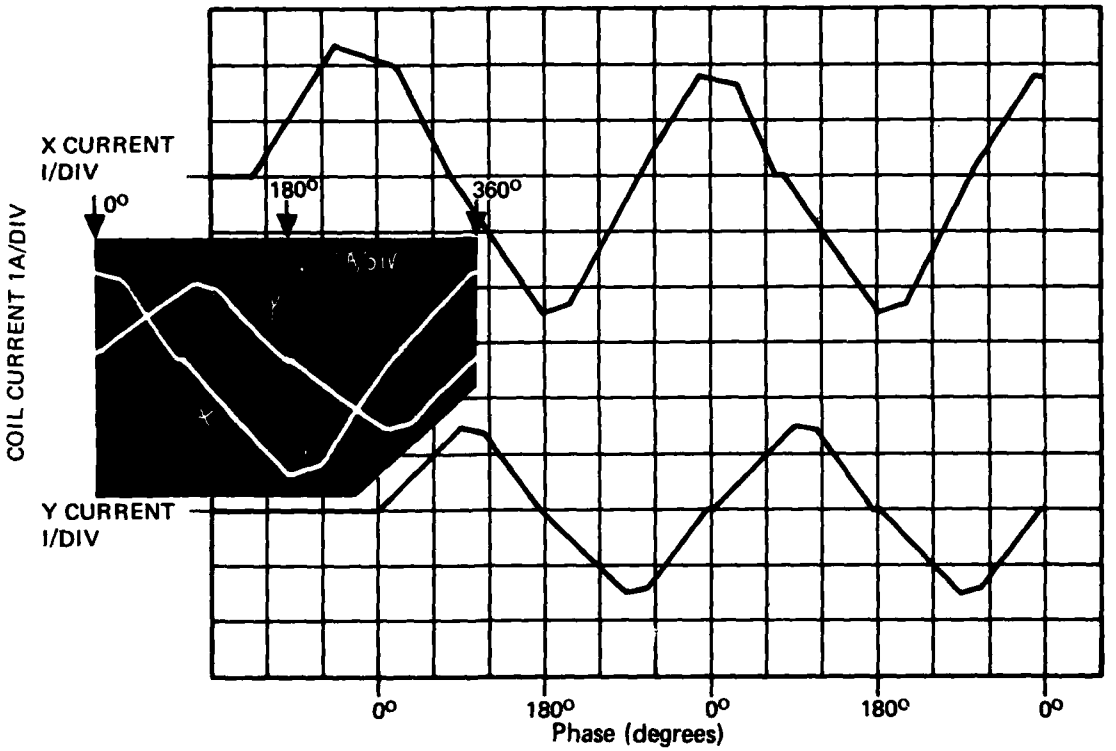


Figure 7-16. Memory module coil drive waveform.

7.4 CELL MULTIPLEXER CIRCUIT

A cell multiplexer (Figure 7-18) using beam diodes as selection elements controls the path of operator and detection currents into an addressed cell. During read, current from the replicator current sources and from the sense channel current sources flows to the energized cell through saturated switches to ground. Diodes of all unenergized cells are back biased by the pull up resistors (5K) in the selection switch IC. A common coil select switch for read and write is used to economize circuitry since little noise is added to the sense bus because the switch is a small impedance to coupled noise relative to detector impedance. During write, current from the transfer out current source and the generators flows to ground through the selection transistors. In order to keep peak current well within the 600 milliamp rating of the 55326 quad selection switch, only two generators' current sources are turned on at a time.

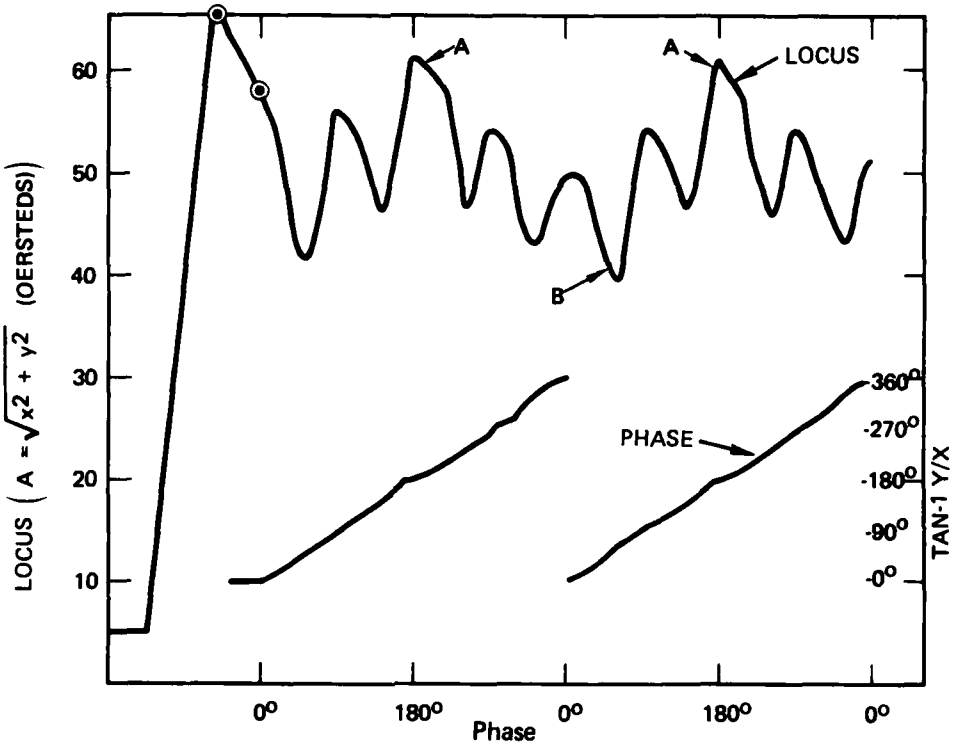


Figure 7-17. Field locus and phase between X and Y

Besides simplifying selection circuitry to only four IC's, the multiplexer approach reduces interface from 112 lines at the chips to 30 lines at the cell interface. Demonstration of the multiplex concept for bubble operation was one of the major accomplishments of the program.

7.5 TIMING AND CONTROL CIRCUITRY

Timing for the module is generated from a 21.33 MHz crystal oscillator (Figure 7-19). The oscillator operates an 8-bit binary counter and a four phase clock generator. After user clock (USCK) initiates an operation, the counter steps the 512 by 8-bit PROM through its addresses until a recycle command or an End of Count (EOC) is encountered. The PROM addresses are divided into four phases so that the control signals can be expanded into four sets of latches. This arrangement is more power conservative than a multiple PROM arrangement. Address zero is the wait state while address 66 is zero degrees. There are 128 states per rotating field cycle operating at 166.6 kHz, which gives theoretical resolution of 46.9 nanoseconds on pulse edge placement. Because of the 4 phase operation, minimum pulse width is 187.5 nanoseconds adjustable in increments of 187.5 nanoseconds.

Two problems were uncovered during evaluation of the design. The first is that the 21.33 MHz clock doesn't stabilize after power turn-on for at least 20 microseconds dependent on supply voltages. The problem appears to be basic to crystal oscillators. For zero standby operation a new approach such as a delay line circuit used typically on other magnetic memories should be evaluated. An example is a delay line square wave generator produced by Engineering Components Company for 0 to 70C operation. The other problem is that of switching time variations of the PROM. Outputs of the PROM do not switch constituently with each other. Minimum to maximum switching guard band over temperature and voltage uses

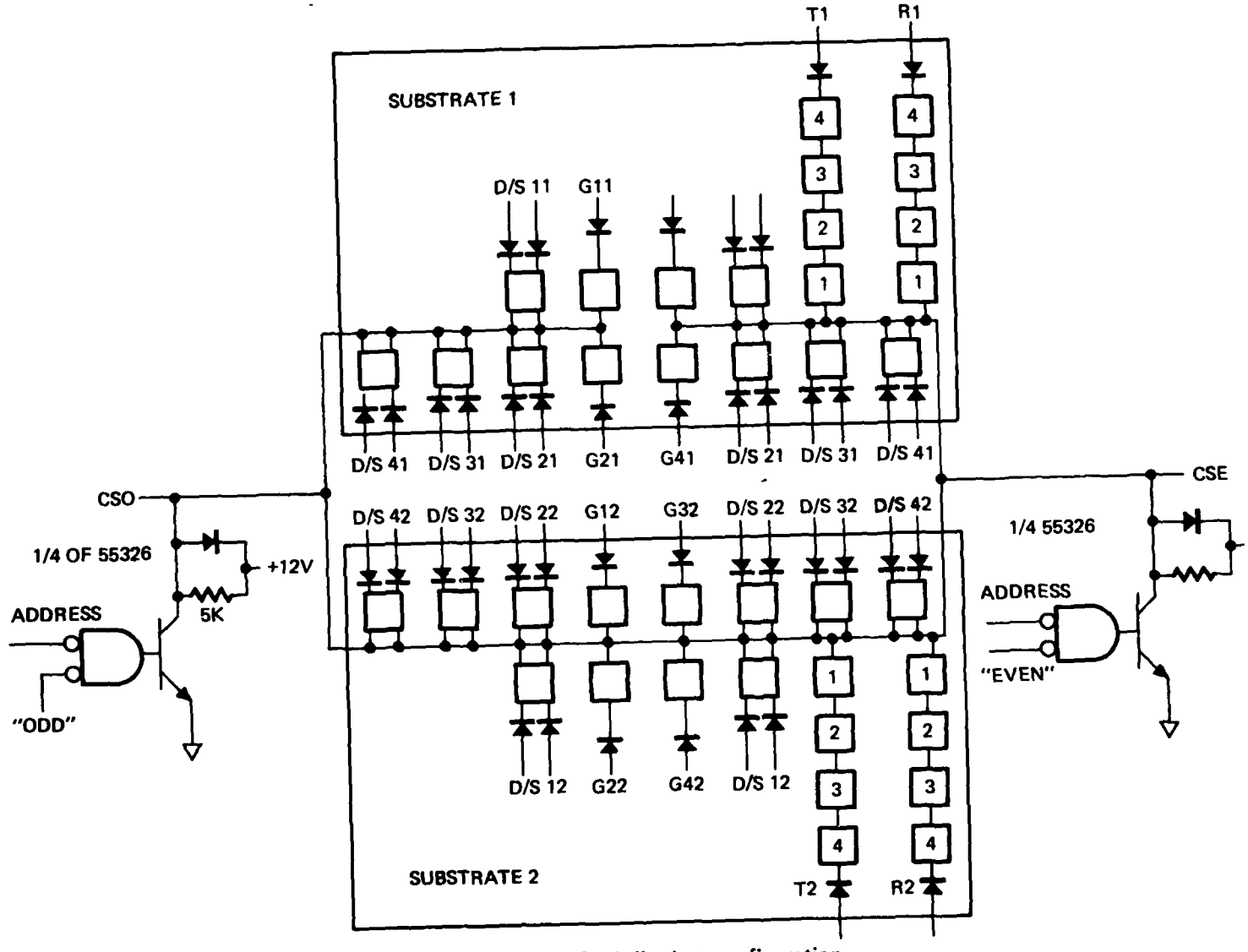


Figure 7-18. Cell select configuration.

most of the available margin. Breadboard operation is assured for a voltage of 5.4 ± 5 percent from -10 C to greater than 60 C but operation of production boards cannot be assured. For future development either the clock should be slower and more PROMS used, or a faster PROM which will operate dependably at the fast clock rate should be used.

A flow diagram of the operation of two modes is shown to the left of Figure 7-19. Once started in the burst mode the memory can operate by recycling timing until stopped. Incremental mode operation is committed to 2 timing cycles.

7.6 SAFETY CIRCUITS

A major hazard of bubble memory chips is fusing of operator conductor loops by inadvertently applying current to the device for extended periods of time. Coil drive current is limited only by limiting on-time of the driver transistors. To prevent hazards several circuit concepts were implemented in the module design. A power on and off protection circuit of Figure 7-20 is used which clamps critical gate inputs to ground during transitions of the five volt logic voltage. Gate type is selected so that a grounded input guarantees an open output when its supply voltage is being turned on or off. Another concept shown in Figure 7-21 is used to limit pulsewidths to a predetermined maximum by using a one shot. A 54LS221 one shot is more suitable than most because it is an edge triggered, nonretriggerable one shot with hysteresis which reduces the potential for oscillations on open inputs from creating a wide pulse.

7.7 PROTOTYPE MECHANICAL STRUCTURE

The storage board holds up to eight cells each with a capacity of 8.2×10^5 bits. Cells are adhesively bonded to the heatrail of the front surface (Figure 7-22) while board associated electronic components (Figure 7-23) are located on the opposite side. Cells and components with a few exceptions are adhesively fixed to surface aluminum heat rails which are also adhesively fixed to the six-layer control multilayer printed circuit board (MLB). All components are lap solder terminated to tinned pads of the MLB. This overall construction provides an environmentally resistant mounting for components and also provides a low thermal resistance conduction heat flow path from the components to the module perimeter.

Cells and components on the storage board are conduction cooled through the surface conductors to the side rails by means of the conduction locking mechanism shown in the photo.

A 6061-T6 aluminum frame is fixed to the cell side of the board to provide necessary stiffness to minimize board deflection during vibration and acceleration. The storage board is interconnected to other boards and systems modules by an Amp Mil qualified 180 pin connector set.

The electronics board (Figure 7-24) is a partially wire wrapped two-layer printed circuit board. The approach was chosen to allow circuit modifications during development. Coil drive hybrids are mounted on a heat rail to permit heat conduction to the side rails during evaluation. Instead of a master interconnect board as conceptualized, a flexible cable with an 180 pin socket is used for interface to a single storage board. System interface is through the three connectors on the left.

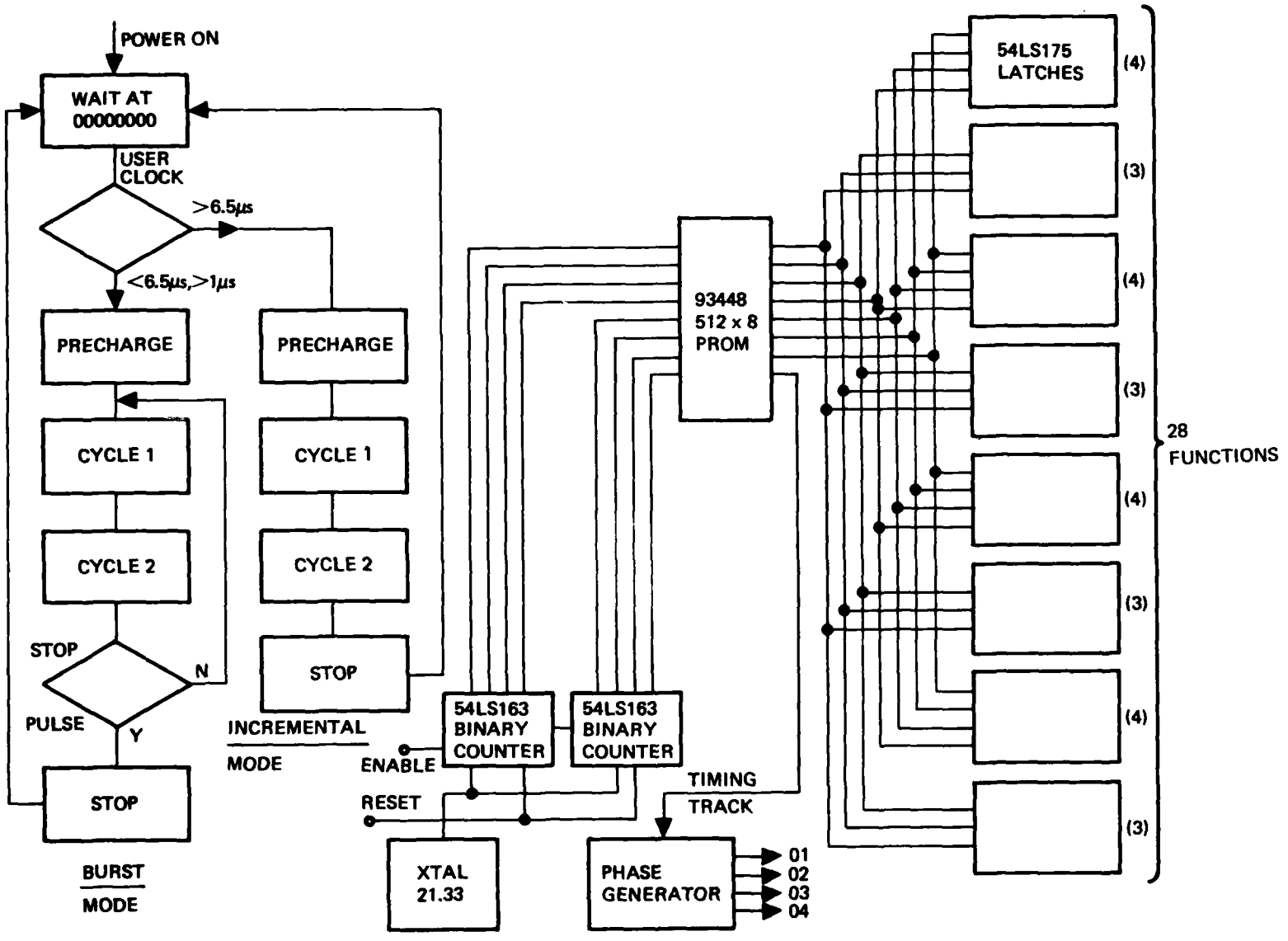


Figure 7-19. Module timing concept.

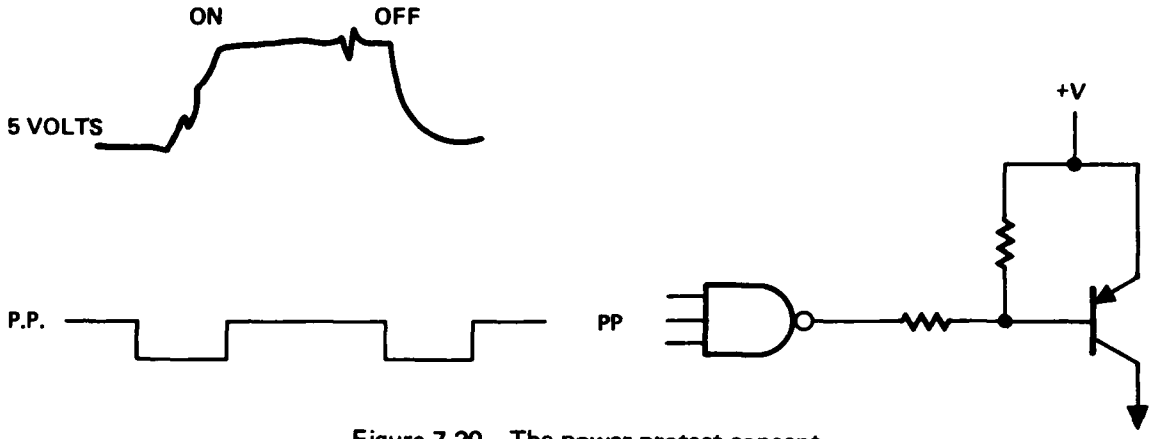


Figure 7-20. The power protect concept.

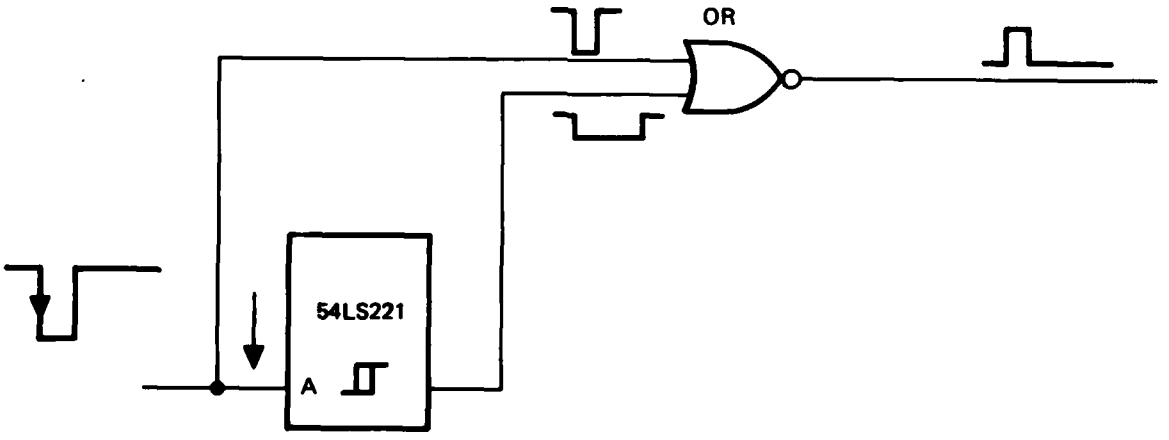


Figure 7-21. The redundant timing concept.

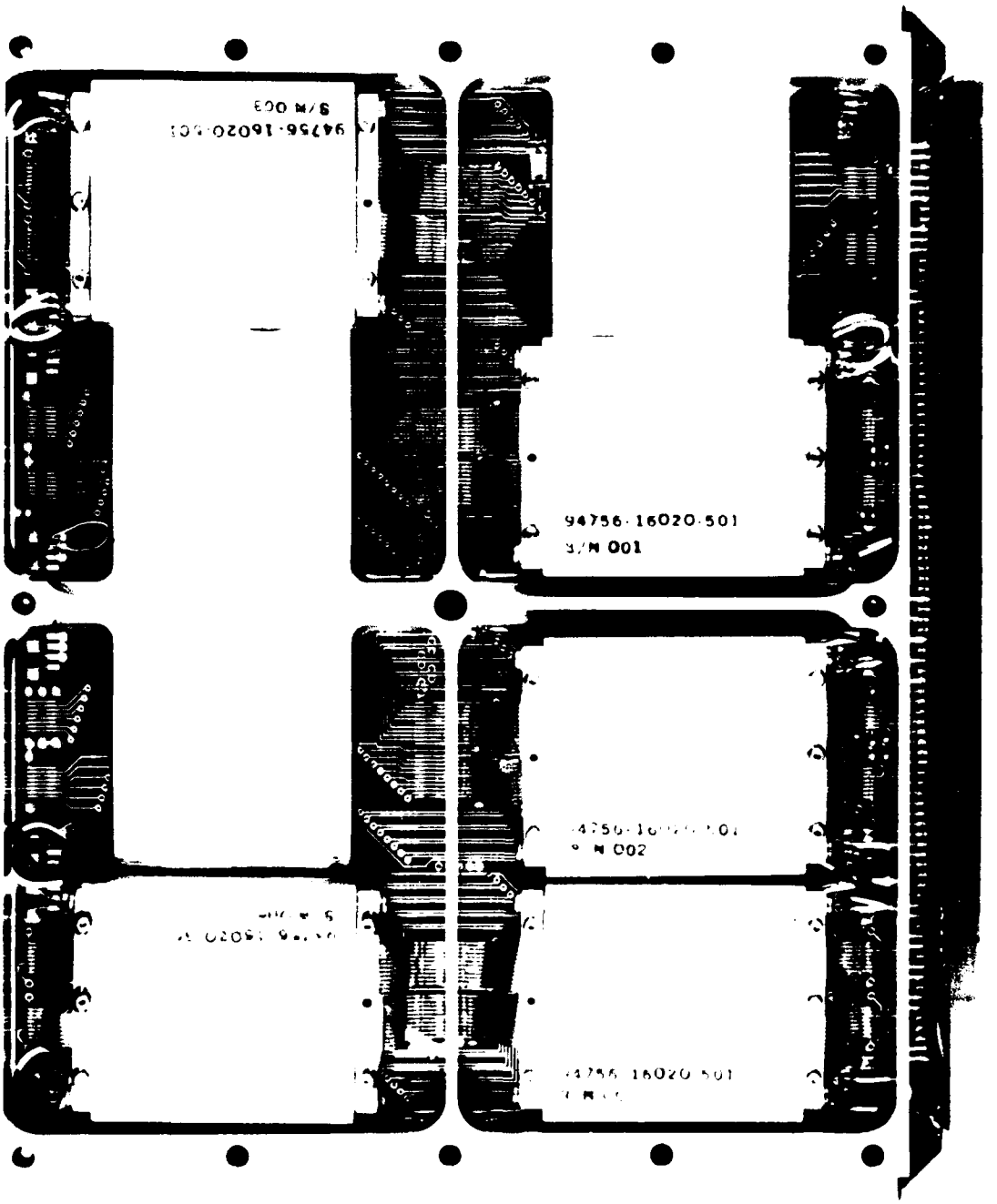


Figure 7-22. Cell side of storage board.

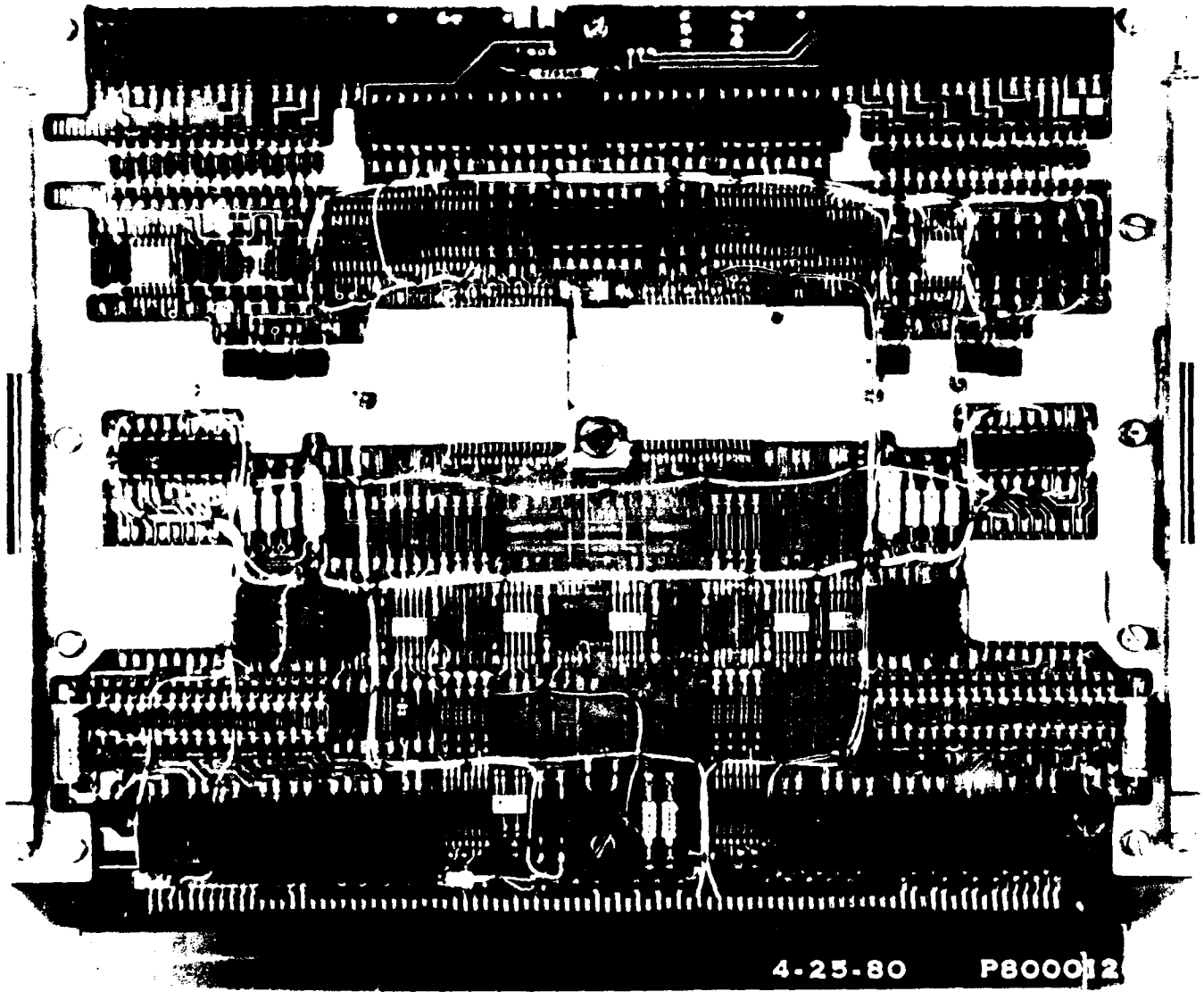


Figure 7-23. Component side of storage board.

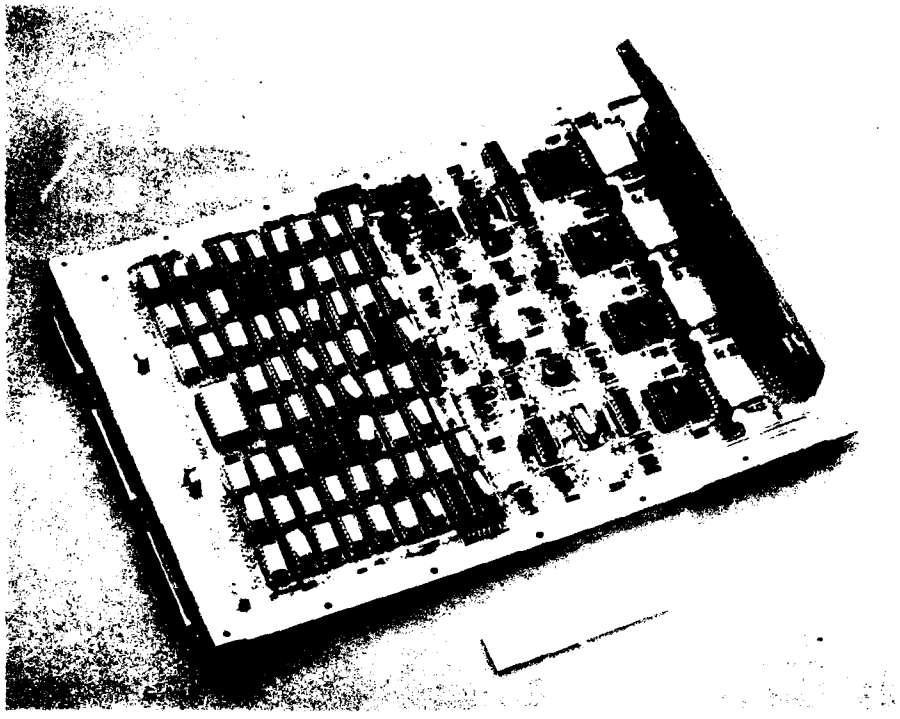


Figure 7-24. Electronic board.

7.8 MODULE TEST RESULTS

Checkout of the electronic board required considerably more effort than did the storage board because the electronics board is a wire wrapped brassboard with fairly complicated control logic for interface, timing, and control while the storage board is carefully designed as a finished multilayer board.

On the storage board the only problem of consequence turned out to be a few conductors with digital signals cross coupling into the sense channels directly under the sense amplifier hybrids despite careful planning during board design. The signals were rerouted with surface bonded wires. Major problems on the electronics board were with the timing PROM and the oscillator turn on as discussed in Section 7.5.

During checkout, three chips were lost by an inadvertent short between generator and coil drive voltage. The three were replaced with marginal chips in order to provide operative cells. Five additional chips were found to be marginal for the reasons identified in Table 7-4. In a conventional production program only three of the eight would have been allowed to reach module assembly.

Sense signals at the module are given in Figure 7-25. Most of the variations shown in outputs are due to chip detector variations as described in section 6. Line 3/1 shows a small cross coupled noise which doesn't affect margin but could be eliminated. Line 6/14 has a

TABLE 7-4. CHIP TEST SURVEY AT MODULE TEST

Require Replacement	Cell ID	Comments
Chip 0	A0; C005	This is the engineering cell assembled for evaluating system operation. The cell was not reworked or tested over temperature. *Chip 0 never worked.*
Chip 6 Chip 2	A3; Cell 003	Chip 6 is sensitive to some patterns. If bubble rests on critical location, data is scrambled when turned on. Chip 2 signal changes drastically at 25 volts drive.
Chip 1	A4; Cell 004	Chip 1 is a marginal replacement chip.
Chip 4	A5, Cell 002	Chip 4 has a trapped bubble problem. Operates okay unless pattern is scrambled. Then the cell must be cleared by erase. Problem was noted at the cell tester.
Chip 5 Chip 6 Chip 1	*A6; Cell 001*	*Chips 5 and 6 are sensitive to low drive field. This was noted at cell test.* Chip 1 is a replacement chip which doesn't operate properly.

baseline offset that reduces margin slightly. It is clear from this evaluation that the multiplexer concept for sensing multiple chip on a large bus is an acceptable method of sensing. Some improvement in sense margin can be obtained by reducing module and cell noise but more improvement can be realized by reducing signal variations by grading chips.

7.8.1 Memory Module Power Dissipation

Power dissipation versus data rate of the memory module is shown in Figure 7-26. Maximum dissipation is higher by about five watts compared to early program predictions while overhead or idle power is higher by about two watts but lower than the program goal. Part of the difference occurred because of the preliminary nature of an early estimate of coil driver power. Figure 7-27 gives aspects of an improved estimate that agrees with data. The coil circuit in the upper left is modeled on the right using manufacturer's V_{ce} and $V_{forward}$ curves to obtain equivalent source generators. Dissipation was calculated for the waveform of Figure 7-16 and for measured AC coil resistance.

Results are summarized at the bottom of Figure 7-27 and are plotted in Figure 7-28. Power in the coil and in the hybrids is consistent with early estimate while driver dissipation is higher. This includes dissipation in the diodes and balun. Several minor modifications can reduce dissipation by from 2 to 3 watts. The cell winding can be configured for higher voltage and lower current which potentially saves 30 percent or 2 watts. Another potential savings is in optimizing or eliminating the second breakdown circuit which is presently responsible for two watts.

Another potential area for reducing power dissipation is by reducing logic voltage to 4 volts which saves 1.6 watts. Logic voltage was increased during checkout to 5.4 volts in order to ensure operation of the timing PROM over a 10 percent voltage range. Modification of the circuit is recommended (Section 7.7), in order to improve model performance and margin.

Overall, minor changes in design should reduce power of the memory module to below 24 watts at maximum data rate.

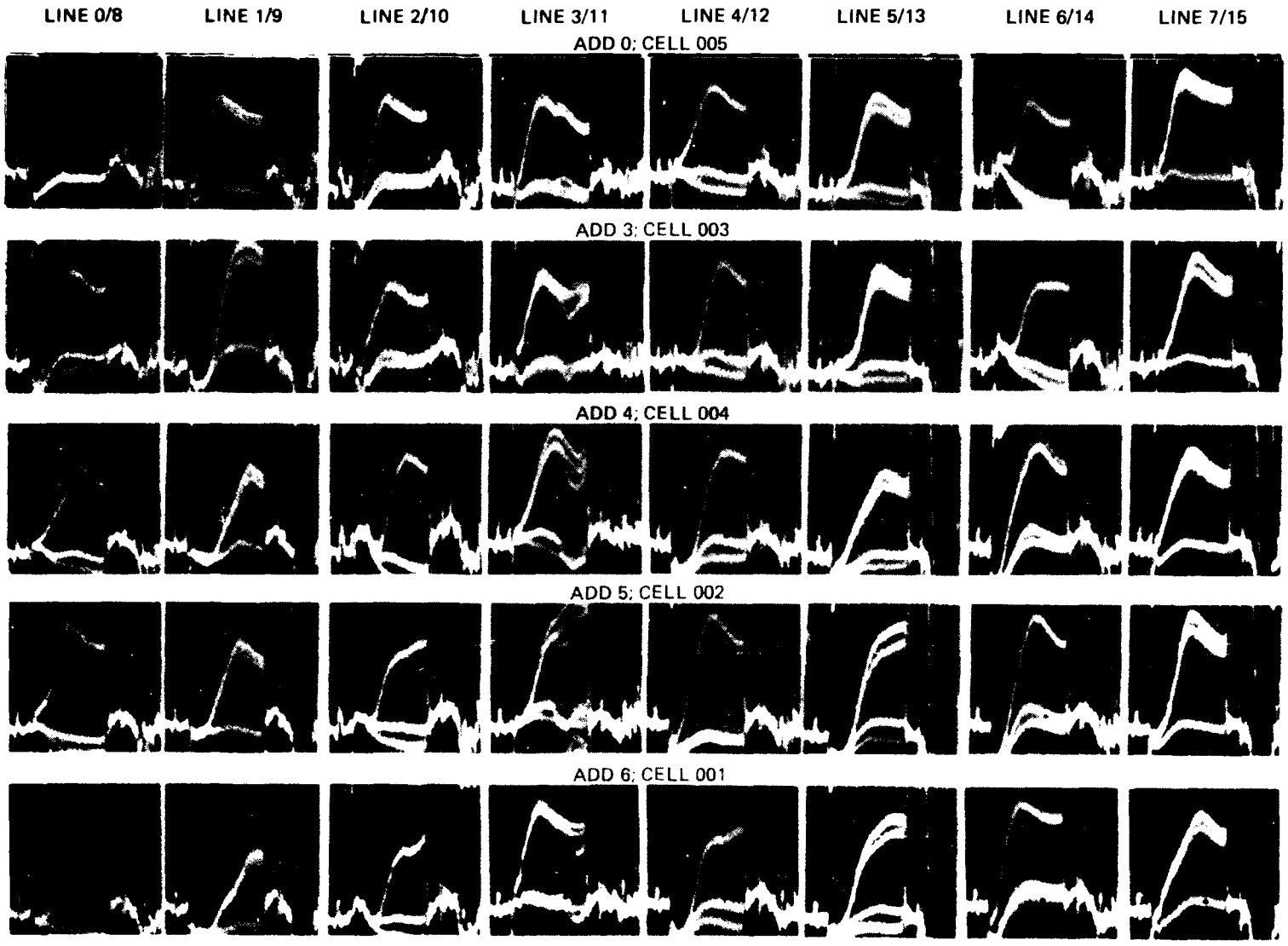


Figure 7-25. Sense amp linear outputs 200mv/div; 500 ns/div (Pattern No. 2).

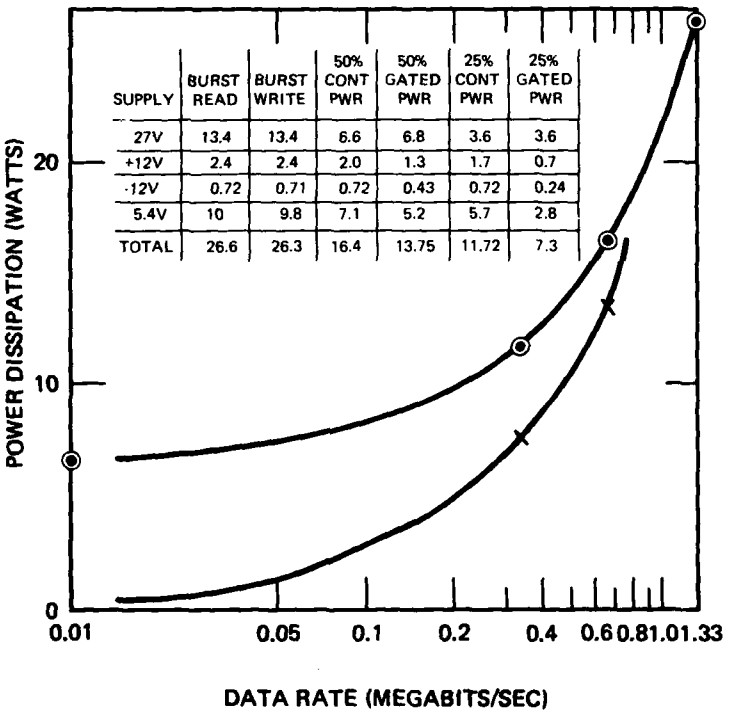
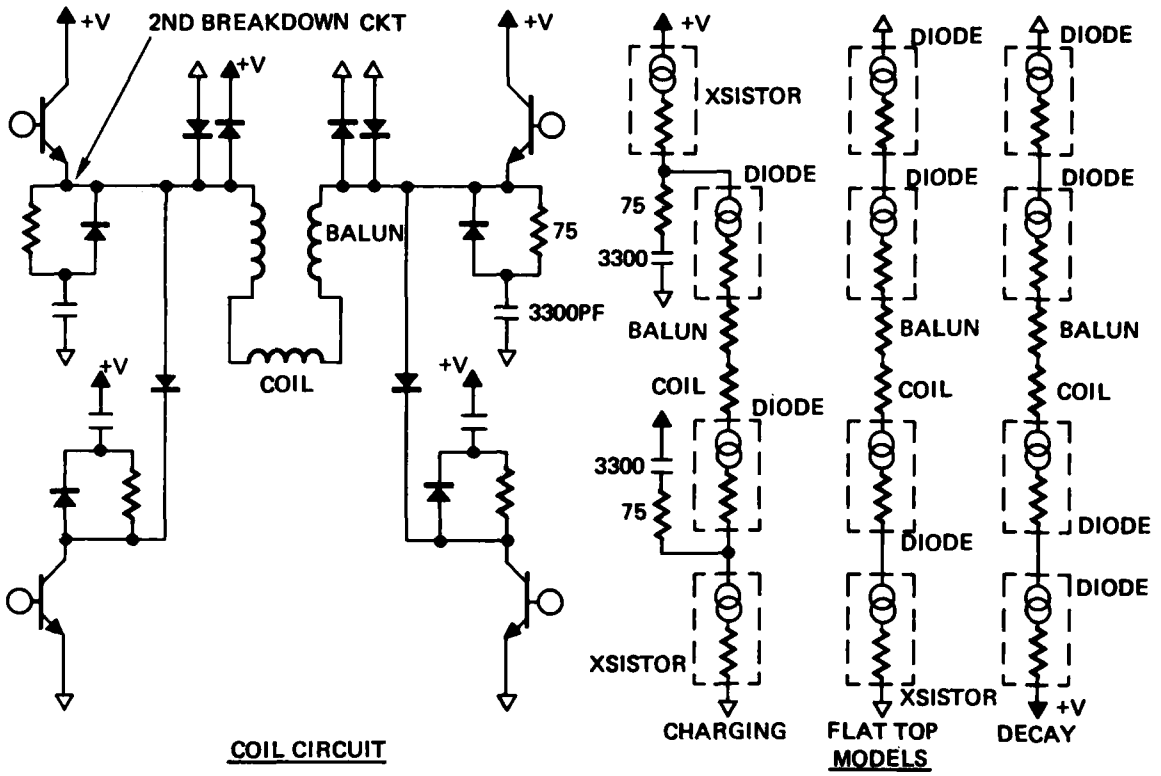
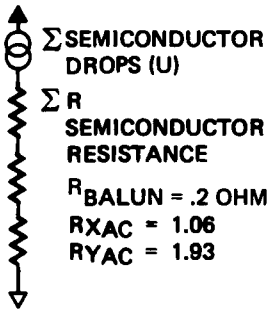


Figure 7-26. Memory module power dissipation.



COIL CIRCUIT

CONDITIONS	V	ΣR	R_{TOTAL}
CHARGING	1.84	0.7	(X) 1.96
			(Y) 2.83
FLATTOP	2.36	0.55	(X) 1.81
			(Y) 2.68
DECAY	2.88	0.4	(X) 1.66
			(Y) 2.53



SIMPLIFIED MODEL AND VALUES FROM MANUFACTURING DATA

TOTAL ESTIMATED POWER = 13.04W; TOTAL MEASURED POWER = 13.4 WATTS
X COIL PWR = 1.94W; Y COIL PWR = 2.37 WATTS
TOTAL COIL POWER = 4.31 WATTS
X COIL DRIVER POWER = 4.4 WATTS; Y COIL DRIVER POWER = 2.33 WATTS
TOTAL COIL DRIVER POWER = 6.73W; EFFICIENCY = 33%
SECOND BREAKDOWN CKT PWR = 2 WATTS; MAX HYBRID PWR = 1.2 WATTS

POWER DISSIPATION BREAKDOWN

Figure 7-27. Aspects of the coil power estimate.

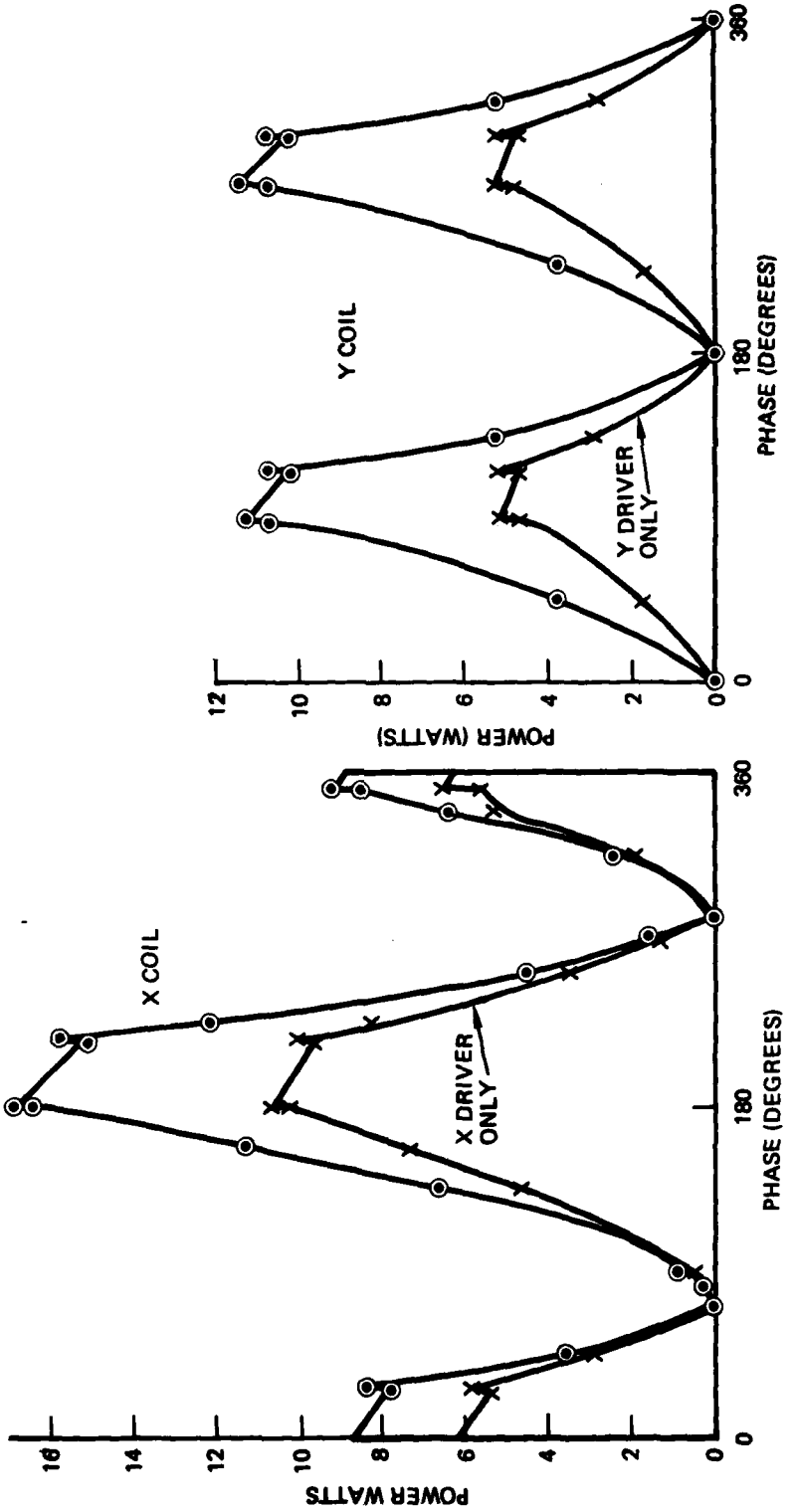


Figure 7-28. Instantaneous power dissipation.

7.8.2 Memory Module Error Rate

Measuring error rates of a 16-bit parallel data channel for each of the cells was not done because of the limited single-bit capability of the module exerciser. Instead, bit error rate was measured on a few bits at room temperature to obtain a percentage guard band to apply to the threshold setting of each sense channel. An estimate of the expected cell soft error rate can then be made for later comparison to data collected at NASA Langley with automatic equipment. Figure 7-29 shows measured error rate versus percentage of full output. If a single isolated bubble signal is 10 millivolts above baseline noise, then a 10^{-8} error rate or the number of errors per bits tested is expected at 8.2 milivolts for that bit. For an isolated no bubble signal a 10^{-8} error rate is expected at 1.3 millivolts above baseline noise. Each bit in a mixed pattern may have a different signal level where 10^{-8} error rate is expected. In considering a guarantee for 10^{-8} operation a guard band of 13 percent of full signal should be added to the maximum zero and a guard band of 16 percent subtracted from the lowest one. Based on threshold measurements described at the beginning of this section, an error rate of 10^{-8} can be guaranteed providing the eight marginal chips were replaced.

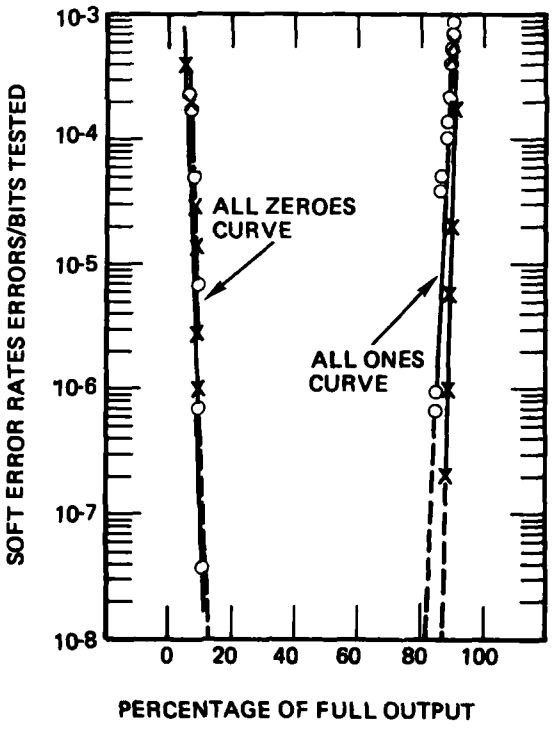


Figure 7-29. D1106 error rate.

8. SPECIAL TEST EQUIPMENT

Two pieces of equipment were built for program requirements. A cell tester (Figure 8-1) was built so that performance of the cell could be verified and so that chip faults could be analyzed. A digital controller supplied signals sequentially to operate the driver operators and sensing functions. These were under PROM control. Macro timing was controlled by either front panel switch, by six sets of PROMs, or by computer input. Cells were mounted on a cold plate which is cooled by refrigerant-cooled dry nitrogen and heated with cartridge heaters.

Figure 8-2 is a photo of the module tester operating the Bubble Memory Module prototype. The module tester is a simple digital tester capable of testing a single channel at a time. It uses most of the hardware, including the front panel and cabinet used earlier to test SSDR module (Ref 2).

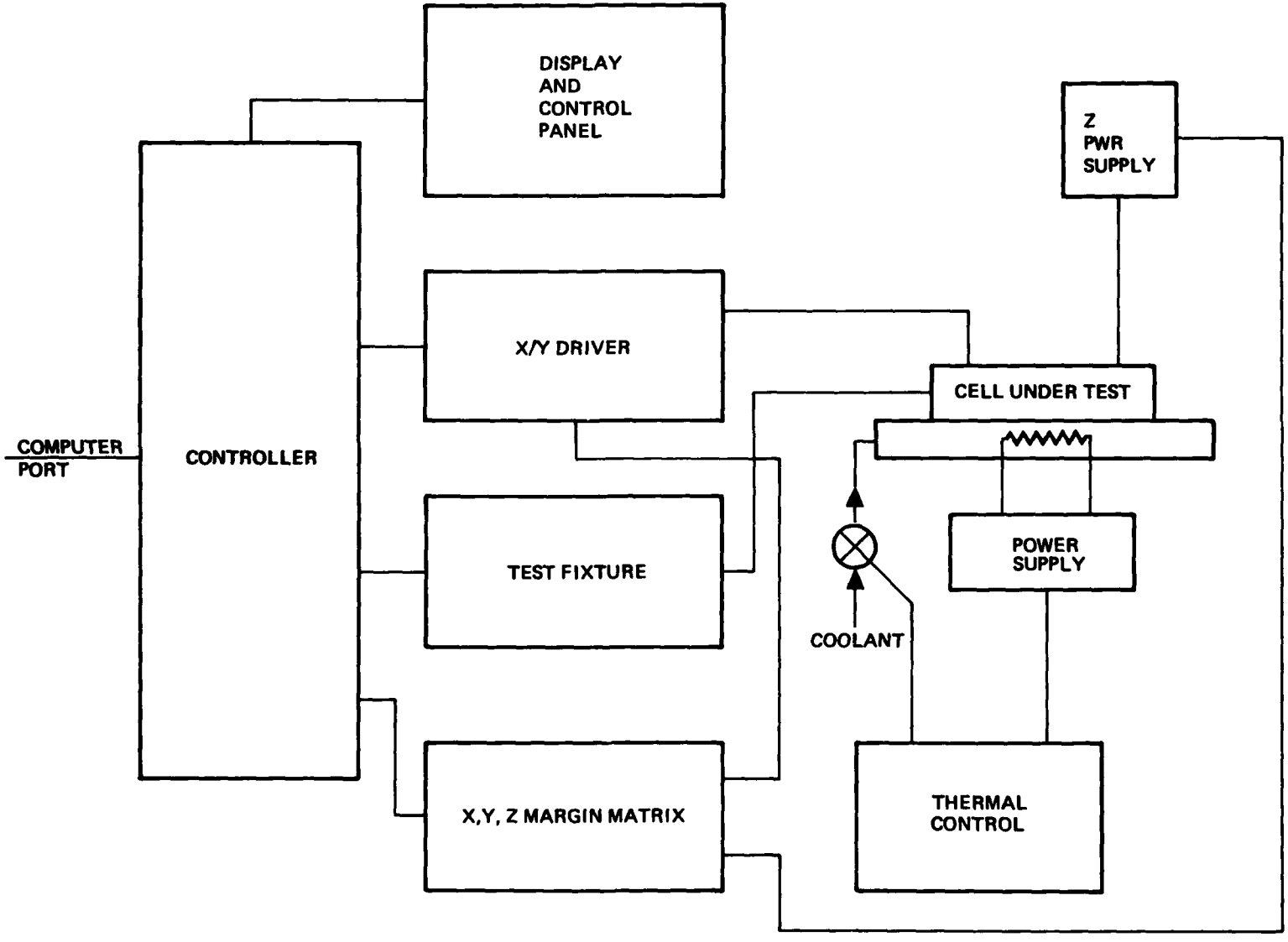


Figure 8-1. Cell tester block diagram.

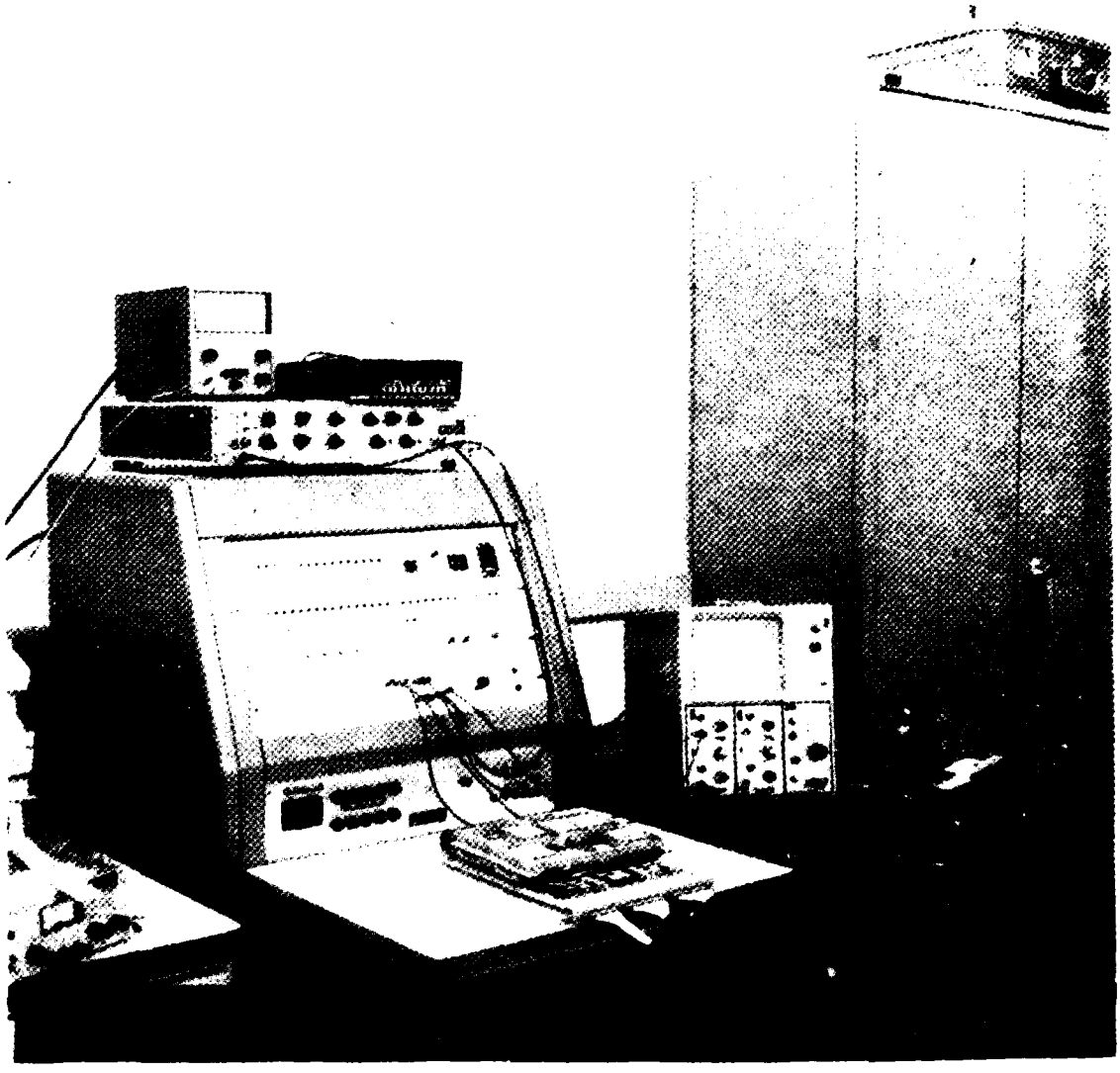


Figure 8-2. Module tester and memory module under test.

9. SUMMARY AND RECOMMENDATIONS

A memory module using bubble domain technology has been developed to meet a wide variety of spacecraft mission needs. This memory module is in a high state of design and evaluation and is believed suitable for flight qualification.

Objectives of the program have been achieved. The chip, cell and storage board have been optimized for multiplexed sensing with satisfactory results demonstrated at breadboard test and at module level test. A building block approach was adopted for the module providing flexibility in recorder and memory design for many applications. Finally power dissipation has been reduced from the SSDR module power of approximately 40 watts to 27 watts at 1.33 MHz.

The Bubble Memory Module program has validated a number of chip, circuit, and systems concepts suitable for spacecraft recorder design. However, selected areas of design should be improved before proceeding into a qualification or production mode.

At the memory element level, a detector resistance test should be used to allow grading and sorting of detector outputs. Longer term improvements in process uniformity especially of the detectors should be sought. Polyimide wafer coating for passificaton which was evaluated during the program should be adopted because the technique appears to be faster and more repeatable than the present technique of applying mylar performs to individual die. Although higher density bubble chips are obviously desirable to increase capacity, the parallel-chip method for attaining higher data rates suffers additional power losses when physically large area chips (corresponding to large capacities) are used. Implementing the 2 micron or smaller bubble technology as discussed in Section 9.1 can significantly increase capacity without increasing chip size.

At the cell level, the winding configuration should be re-explored to take advantage of recent developments which have the potential of reducing coil driver power and increasing data rate slightly without impacting other aspects of the design. Carrier hermeticity studies should be continued to involve a larger number of sample runs than was possible on the present program and to verify the design.

At the system level, the oscillator circuit must be redesigned and replaced with a recirculating delay line so that the timing can be turned on within 5 microseconds. The present method of timing generation cannot be worst-cased for device variation and should be redesigned. Additional minor improvements might be made to the coil driver and sense hybrids and to the storage board layout to improve performance and manufacturability.

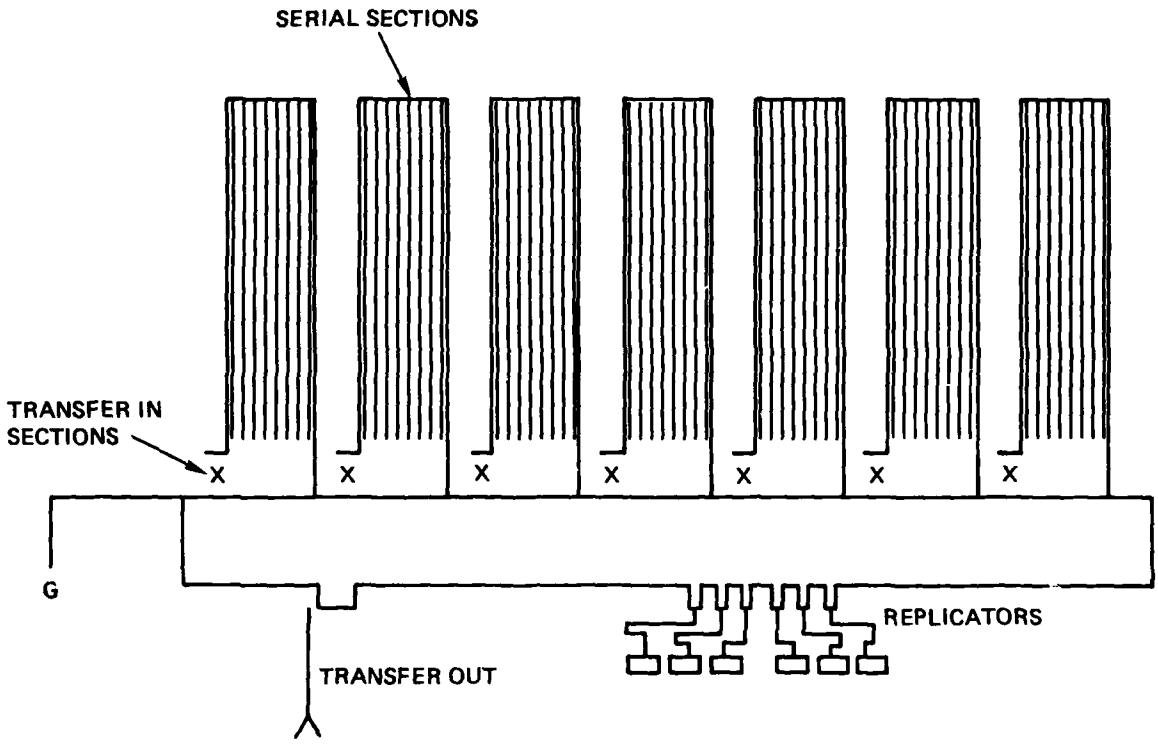
In the long run, attention should be directed to increasing capacity within the basic module design and to developing a production capability for a general-purpose recorder module.

9.1 SERIAL REDUNDANT CHIP

The ultimate yield limit of a serial chip design is the probability that all propagation elements are within geometric spacing limits. This implies that larger capacity serial chips using two micron or smaller bubbles becomes increasingly uneconomical unless a form of selective redundancy is used.

Rockwell's Electronics Research Center has explored a method of obtaining redundancy in serial chips [Ref 5]. The approach shown in Figure 9-1 uses a shorted transfer-in gate as a basic element. Except for the addition of the transfer-in gate, the chip is designed to perform identically with the present design. A 1/2-cm chip by 1/2-cm which is of the same physical size as the D1106 chip but using two-micron technology can contain approximately 400 kilobits.

To test specific serial sections for the first time, a pattern is generated which is timed to transfer into the selected sections using high current in the transfer loops. Once good sections are identified, each good section's transfer-in shunt is laser cut. To operate the device, a transfer-in pulse of low amplitude (25 milliamp) is applied every cycle. Data flows in a continuous stream, bypassing bad loops.



SERIAL REDUNDANT CHIP SCHEMATIC

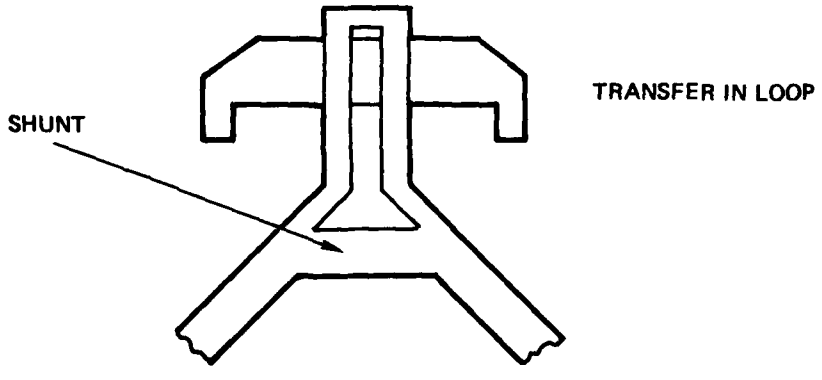


Figure 9-1. Redundant serial concept.

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16. Abstract

This report covers development of a Bubble Memory Module as a general purpose storage unit in recorders or mass memory for spacecraft applications. Design, fabrication and test of a partially populated prototype recorder using 100 kilobit serial chips is described. Electrical interface, operating modes, and mechanical design of several module configurations are discussed.

Fabrication and test of the module demonstrating the practicality of multiplexing and matrixing multiple bubble chip cells as a means of minimizing support circuitry resulting in lower power, weight, and volume.

This effort resulted in the completion of a module consisting of a fully engineered printed circuit storage board populated with 5 of 8 possible cells and a wire wrapped electronics board. Interface of the module is 16 bits parallel at a maximum of 1.33 megabits per second data rate on either of two interface buses.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
Magnet Bubble Memory Technology Data Recorder Mass Memory Memory System	Unclassified - Unlimited Subject Category 19

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