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STUDY OF THE PHYSICS OF INSULATING FILMS AS RELATED TO THE RELIABILITY OF METAL-OXIDE SEMICONDUCTOR DEVICES

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STUDY OF THE PHYSICS OF INSULATING FILMS AS RELATED TO THE RELIABILITY OF METAL-OXIDE SEMICONDUCTOR DEVICES

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This report covers the high current injection into SiO_2 using Si rich SiO_2, the use of Raman scattering to observe amorphous Si in Si rich SiO_2 and the crystallization of this amorphous Si at high temperatures. the use of attenuated total reflectance measurements to study Si rich SiO_2, measurements of physical characteristics of oxides grown using high pressure oxidation, and the description of an automatic tester developed for use in electron and hole trapping studies.

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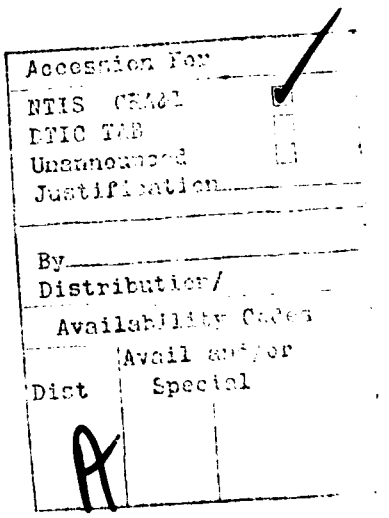

INTRODUCTION

Much of the previous work on this contract has been concerned with the development of means to reduce the electron trapping in SiO_2. The goal of this work has been to reduce drifts in device characteristics as a result of charge trapped in the SiO_2. In another class of devices, floating polysilicon gates are embedded into the SiO_2 to store charge indefinitely. This charge is used to control the behavior of the MOSFET device and thus controllably alter the function of the circuitry encorporating these devices. One of the major problems associated with the use of floating gates has been the need to change the stored charge. It is preferable if this can be done electronically "in situ". It is also preferable to use oxide conduction to change this charge instead of charge injection as a result of hot electrons generated in PN junctions in the silicon. The latter process is inefficient since a large current in the silicon is required to obtain a useable oxide current for use in charging or discharging the floating gate.

A new method for charging and discharging the floating gates has been developed by DiMaria and Dong that involves the use of thin silicon rich SiO_2 regions to enhance the injection of charge into the SiO_2. These Si rich SiO_2 regions are used above the floating gate (to remove the negative charge from the floating gate when desired) and under the top, control gate (to supply charge to the floating gate). At the relatively low electric fields normally applied for device operation, these regions are not effective and therefore act as insulators. At a well defined field, these regions inject charge into the SiO_2 and change the state of charge of the floating gate. The threshold field for this surprising effect is surprisingly reproducible even though the devices are made in different locations and in some cases by different processes. These structures have been labeled DEIS devices. The first paper by DiMaria and Dong included in this report "High Current Injection Into SiO_2 From Si Rich SiO_2 Films and Experimental Applications" discusses these devices. A novel technique has

been developed for using the Si rich charge injectors to study charge trapping in SiO_2, by DiMaria, Ghez and Dong and this work is described in a paper entitled "Charge Trapping Studies in SiO_2 Using High Current Injection From Si Rich SiO_2 Films."

The Si rich SiO_2 regions are two phase consisting of Si particle embedded in SiO_2. The silicon particles are very small and have a high density. The paper entitled "Observation of Amorphous Silicon Regions in Silicon Rich Silicon Dioxide Films" by Hartstein, Tsang, DiMaria and Dong discusses the use of Raman scattering and optical transmission measurements to study these Si particles and shows that they are initially amorphous but convert to crystalline silicon after heat treatment at temperatures above 1000°C. The two phase nature of this material leads to the enhanced electron injection that occurs. The alternated total reflectance technique has also been used to study the infra red absorption of these materials in a paper entitled "Attenuated Total Reflectance Study of Silicon Rich Silicon Dioxide Films" by Hartstein, DiMaria, Dong and Kuza.

SiO_2 grown at high pressure by R.J. Zeto of the U.S. Army Electronics Technology and Devices Laboratory (ERADCOM), Fort Monmouth, New Jersey have been evaluated by Irene, Dong and Zeto in a paper that is included, "Residual Stress, Chemical Etch Rate, Refractive Index, and Density Measurements on SiO_2 Films Prepared Using High Pressure Oxygen."

We have received several requests for a description of our Automatic Avalanche Injection Apparatus and this is described by John Calise, "Automatic Tester Used in Electron Trapping and Hole Trapping in SiO_2."

Invention Disclosures

Back Up Non Volatile Memory for Static Random Access Memory Array
D.R. Young

Storage Cell for EAROS Arrays Using DEIS Charge Injectors
D.R. Young

High Current Injection into SiO_2 Using Si Rich SiO_2 Films and Experimental Applications*

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ABSTRACT

Although silicon dioxide has a high mobility for electrons (~ 30 cm^2/V-sec), it forms large interfacial energy barriers (> 2 eV) with all contacting metals or semiconductors because of its large energy bandgap of ~ 9 eV which makes current injection into it very difficult. This results in the excellent insulating properties of SiO_2 capacitors. By depositing a thin layer of Si rich SiO_2 between SiO_2 and a contacting electrode, such as Al or Si, high electronic current injection at moderate applied voltages can be obtained. This "apparent" reduction of the interfacial energy barrier is believed to be obtained by "local" electric field distortion associated with the highly conducting, two-phase (Si and SiO_2) nature of the deposited Si rich SiO_2. This injection phenomena has been shown to be limited by the interface of the Si rich SiO_2 with the underlying oxide. The currents are Fowler-Nordheim-like and have weak temperature dependence. Internal photoemission has been used to show that uniform homogeneous grading of the energy bandgap of the Si rich SiO_2 layers does not account for the high current injection. Injection currents are not strongly effected by high temperature (> 1000°C) annealing which is shown, using Raman spectroscopy, to convert amorphous Si regions (< 50 Å in size) into Si crystallites in the Si rich SiO_2 layer.

Layered structures composed of Si rich SiO_2 and SiO_2 have been shown to have several applications, particularly in the area of non-volative semiconductor memory and can be used to improve voltage breakdown characteristics. Devices using Si rich SiO_2 injectors to charge up floating, polycrystalline-Si gate type memory structures are capable of being "written" or "erased" at low voltages in 5 msec at least 10^5 times with the excellent charge retention characteristic of a floating poly-Si structure. Low voltage breakdowns of SiO_2 layers, which are believed to be associated with the field at the cathode, are shown to be suppressed when a thin Si rich SiO_2 layer is present. Reversible space charge build up in this thin layer relaxes high electric fields at the metal or silicon contacts. This is believed to result in the observed dramatic increase in breakdown voltage. Also, current as a function of ramped gate voltage characteristics are shown to be a rapid, easy means for studying trapping

kinetics and centroid position of trapping sites in the SiO_2 layer of structures with Si-rich SiO_2 injecting layers.

I. INTRODUCTION

Silicon dioxide, SiO_2, is commonly used in the electronics industry for passivation because of its excellent insulating properties. These properties are due to the large energy barriers (> 2 eV) that SiO_2 forms at interfaces with contacting metal or silicon layers because of its large energy bandgap (≈ 9 eV [1]). However, once electrons have entered the SiO_2 layer from the contact at the lower potential, they rapidly move through this layer to the opposite contact with a rather high mobility, for an insulator, of ~ 30 cm^2/V-sec [1] with less than 1 out of every 10^5 carriers being captured by traps in the thermally grown SiO_2 [1,2]. These electronic trapping centers are believed by many researchers to be related to residual H_2O present in the SiO_2 layers [2,3]. Hole injection from the contacts into SiO_2 layers is much more difficult than electron injection due to an asymmetry of the interfacial energy barriers, with holes "seeing" a larger barrier [1]. Hole mobility is also typically ≈ 10^{-5} times less than the electronic mobility due to the presence of shallow traps in the SiO_2 forbidden bandgap near the top of the valence band [1]. In principle, the blocking effect of the contacts to SiO_2 could be overcome if an interfacial matching layer is inserted between the contact and the SiO_2. For example if the contact is Si, then a region with the bandgap graded from Si to SiO_2 should be appropriate; namely, a semiconductor to insulator heterojunction [4]. At low applied fields, this heterojunction would be blocking with a limiting energy barrier for electrons (holes) of ≈ 3 eV (5 eV) from the bottom of the Si conduction band to the bottom of the SiO_2 conduction band (top of the Si valence band to the top of the SiO_2 valence band) [1,5]. As the applied field is increased, the energy bands would be pulled down for electrons (up for holes) until the smaller energy barrier at the Si contact-graded insulator interface limits the injection process [5]. With this type of reasoning in mind, metal-oxide-semiconductor (MOS) structures, were initially fabricated with a thermal silicon dioxide layer grown on Si and various thin stepped or graded Si-rich SiO_2 layers [5] deposited on top of the SiO_2 before gate electrode deposition. Current as a function of gate voltage characteristics such as those in Fig. 1 indeed showed enhanced electron injection under negative gate voltage bias when compared to control structures without the stepped or graded Si-rich SiO_2 layers present. However as seen in Fig. 1, the current enhancement was not particularly sensitive to the nature of the grading as long as the last layer closest to the contacting electrode, which was Al

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for this case, was composed of the Si-rich SiO_2 material with the highest Si content used (46% atomic Si [5,6]). Also, no strongly enhanced hole injection under positive gate voltage bias was seen. These observations led to a questioning of whether or not the Si-rich SiO_2 layers were really graded in a homogeneous way, or whether the material was actually composed of separate phases (like Si and SiO_2).

This review will be concerned with experimental data correlating the material properties of the composite Si-rich SiO_2-SiO_2 structures with the observed electrical properties. In section II, several experiments showing a two phase nature (Si and SiO_2) for the Si-rich SiO_2 materials will be discussed. Then a model depending on this two phase nature will be used to explain the high electronic current injection phenomena shown in Fig. 1. The dependence of the injection process on temperature, Si-rich SiO_2 thickness, gate electrode area, annealing, and sensitivity to Si content of the Si-rich SiO_2 layers will be described. In section III, experimental applications involving various stacked layers of Si-rich SiO_2 and SiO_2 will be shown for electrically-alterable read-only-memory (EAROM). Also, low voltage breakdowns in MOS structures which are believed to be associated with contact-SiO_2 interfaces are shown to be dramatically improved with the presence of the intervening Si-rich SiO_2 layer. Finally, the current-ramped voltage characteristics of these structures will be discussed in terms of a rapid, easy way to study trapping kinetics and centroid position of sites in the SiO_2 layer which are either purposely or inadvertently introduced during fabrication.

II. PHYSICS AND MATERIAL CONSIDERATIONS

A. Two Phase Characteristics

Several laboratories have recently shown that Si-rich SiO_2 (also called semi-insulating polycrystalline silicon (SIPOS) [7]) has Si crystallites in an oxide matrix made up of mostly SiO_2 at least after annealing at high temperatures (1000°C) in an inert ambient such as nitrogen [8-12]. These films are usually prepared by chemical vapor deposition (CVD) at 700°C-800°C using SiH_4 and N_2O [6]. Figure 2 shows a dark-field high-resolution cross-section transmission-electron-micrograph (TEM) of stacked layers of 1000°C annealed Si-rich SiO_2, SiO_2, and Si-rich SiO_2 [12]. The bright white spots in these micrographs are crystallities in the Si-rich SiO_2 layers. The largest crystallities are approximately 50 Å in size. The intervening, chemically-vapor-deposited oxide layer does not show any crystallities.

Further studies initially by Goodman et al. [13] and more recently by Hartstein et al. [14] using Raman spectroscopy, have shown that the as-deposited unannealed Si-rich SiO_2

layers are also made up of at least two phases (Si and oxide) with the Si regions being amorphous. Figure 3 demonstrates how these amorphous Si regions are converted to Si crystallities with high temperature annealing. In this figure, the Raman spectrum of amorphous Si (α-Si) shows no sharp lines for frequency shifts above 200 cm^{-1} but rather a broad asymmetric continuum peaked near 480 cm^{-1}. This continuum arises from the relaxation of the normal Raman selection rules for scattering from a crystal due to the loss of translational symmetry in the amorphous state. As the Si-rich SiO_2 layer is progressively annealed at higher and higher temperatures, the continuum of the amorphous Si state disappears (completely by 1150°C) and the Raman spectrum of crystalline silicon with a single strong line at $\approx$ 525 cm^{-1} appears. Optical transmission measurements in the visible region show a similar behavior on comparing annealed and unannealed Si-rich SiO_2 layers [14].

Also measurements of the infrared absorption using the attenuated total reflection technique [15] of CVD Si-rich SiO_2 and control CVD SiO_2 films show absorption lines attributed to SiOH, H_2O, and SiH groups in as-deposited films [16]. The concentrations of the SiOH and H_2O impurities is in the low 10^{21} cm^{-3} range and the concentration of the SiH impurity is in the mid 10^{18} cm^{-3} range with the Si-rich SiO_2 films containing about an order of magnitude more SiH than the SiO_2 films [16]. After annealing at 1000°C in N_2, no absorption lines are observed, and the concentration limits for SiOH and H_2O are $\lesssim$ low 10^{19} cm^{-3} and for SiH $\lesssim$ 10^{16} cm^{-3} [16]).

B. Current-Voltage Characteristics

(i) Dark Currents

Electrical characterization of Si-rich SiO_2 films deposited on top of or underneath SiO_2 layers was performed by measuring the dark current using point-by-point or ramped gate voltage techniques [5,17]. Results from these measurements which will be discussed in this section together with the results from material characterization summarized in section II-A, will lead to the physical model proposed in section II-C.

Figure 1 shows the dark current as a function of negative gate voltage for various Si-rich SiO_2 layers stacked on top of a thermal SiO_2 layer incorporated into an MOS structure. These measurements were taken point by point, and they show a ledge in the low voltage region. This ledge is due to a reversible electronic space charge build-up in the Si-rich SiO_2 layer [5]. As the negative voltage is increased, the Al gate electrode injects electrons into the Si-rich SiO_2 layer which traps and holds this charge in the Si regions. This causes the

observed ledge which is terminated when injection from the Si-rich SiO_2 layer into the SiO_2 layer becomes dominant at ≈ -22 V. At higher negative voltages ($\gtrsim -22$ V), most of the applied voltage is dropped across the underlying SiO_2 layer due to the low resistivity of the Si-rich SiO_2 film compared to SiO_2 [6]. As seen in Fig. 1, the current is strongly dependent on voltage after dominant injection into the SiO_2 layer which is consistent with Fowler-Nordheim tunneling [18]. The remainder of this review will be concerned mostly with this high electron current injection into the SiO_2 layer. With the Si-rich SiO_2 layer present, the MOS shows essentially a switching action where electron injection from the Al electrode is blocked by a reversible space charge build-up in the Si-rich SiO_2 layer until a critical voltage is reached. Then injection (via Fowler-Nordheim tunneling) of some of the stored electrons in the Si-rich SiO_2 layer into the SiO_2 layer becomes dominant, and these electrons can rapidly flow through the SiO_2 to the opposite electrode which is the Si substrate for this case. This switching action is extremely useful for device applications as will be shown in section III-A.

MOS structures with Si-rich SiO_2 layers at either or both the Si substrate or gate electrode interfaces [19] can be fabricated using in situ CVD of Si-rich SiO_2 and of SiO_2 as opposed to using a thermal SiO_2 layer grown from the Si substrate. Annealed CVD SiO_2 and thermal SiO_2 are very similar in both their physical and electrical properties [1,17,19]. Such a stacked structure consisting of a Si substrate - CVD Si-rich SiO_2 - CVD SiO_2 - CVD Si-rich SiO_2 - metal or polycrystalline Si (poly-Si) gate electrode is called a dual electron injector structure (DEIS) [19], because enhanced electron injection can occur from either the Si substrate for positive gate voltage V_g^+ or from the gate electrode for negative gate voltage V_g^-. Figures 4 and 5 show enhanced electron injection from the Si substrate for a DEIS which was unannealed or annealed at 1000°C in N_2 for 30 min prior to Al gate metallization, respectively. These dark I-V measurements were taken under ramped gate voltage conditions with a constant ramp rate of .47 V/sec. The first low voltage ledge is due to a capacitive displacement current $C\ dV_g/dt$ where C is the total series capacitance of the stacked structure [17]. The second broad ledge at $\approx 10^{-7}$ A in Fig. 4 for the unannealed structure is due to trapping on certain H_2O related sites [17] in the intervening CVD SiO_2 layer which are removed with annealing as shown by Fig. 5. The study of these trapping ledges can give useful information on trapping kinetics, and it will be discussed in section III-B. For the annealed structure in Fig. 5, the I-V characteristics show only a slight dependence on the thickness of the Si-rich SiO_2 layers from 100 Å to 1000 Å. This is consistent with the low resistivity of this material with respect to SiO_2 and consistent with a physical model which suggests that the enhanced electron injection into the SiO_2 layer is controlled by the Si-rich SiO_2 interface with this oxide layer. The ledge at $\approx 10^{-6}$ A in Fig. 5 is not due to trapping. It is caused by depleting

minority carriers (electrons for the 2 Ωcm p-Si substrates used here) from the substrate Si-Si-rich SiO_2 interface faster than they can be generated thermally in the Si for enhanced injection into the SiO_2 layer. As this depletion occurs, any additional voltage is dropped across the Si substrate and the oxide fields are held approximately constant. On the unannealed structure in Fig. 4, there is a more pronounced dependence on Si-rich SiO_2 thickness. This again is probably due to H_2O in the oxide regions of the Si-rich SiO_2 layers which cause more trapped space charge build-up in this layer and make it appear more resistive to electronic carrier flow to the Si-rich SiO_2-SiO_2 interface.

The dark I-V dependence on contacting electrode material was studied in detail for Al, Au, planar Si, and Si with a rough surface (poly-Si surfaces [20]). For the case of a Si-rich SiO_2 injecting layer deposited on SiO_2, poly-Si and Al gate electrodes give similar results, but Au electrodes regardless of the deposition technique (resistance heated W boat or electron-beam deposition [5]), have less injected current for comparable negative gate voltages. However, these differences between Si, Al, and Au were not as large as observed on control structures without the Si-rich SiO_2 layer [5]. The differences in dark I-V characteristics on the control structures are adequately predicted by differences in the work functions of Al, Si and Au with Au being $\approx$ 1 eV larger than Al or Si [5,18]. Since the current injection is controlled by Fowler-Nordheim tunneling at the metal-SiO_2 interface [18], a 1 eV difference in work function gives a 1 eV larger energy barrier at this interface and a larger tunneling distance into the SiO_2. However when the injecting Si-rich SiO_2 layer is present, the Si islands and the space charge they build up tend to limit the electrode injection, as discussed previously. The energy barrier height differences are minimized further as the Si-rich SiO_2 layer is made thicker [5].

For structures (such as the DEIS) where the Si-rich SiO_2 injector is deposited on either a planar Si crystal surface or a rough poly-Si surface and then the SiO_2 layer is deposited on top of it, an asymmetry in the dark I-V characteristics between this bottom injector and a Si-rich SiO_2 injector deposited by CVD on top of the SiO_2 layer (top injector) is observed [19]. The bottom injector gives a larger electron current injection for positive gate voltages than the top injector for negative gate voltages of the same magnitude for structures which have supposedly equivalent injectors and contacts [19]. This asymmetry is thought to be due to observed (by high-resolution cross-section TEM [12]) differences in the Si islands at the Si-rich SiO_2-SiO_2 interface.

Dark current-voltage characteristics on composite Si-rich SiO_2-SiO_2 structures as a function of the following variables, were also investigated: area from 6×10^{-3} cm^2 to

8.4×10^{-6} cm^2; temperature in the range from 77°K to 473°K; annealing at 1000°C in various gaseous ambients such as N_2 and N_2-H_2 mixtures; and Si content of the Si-rich SiO_2 layers ranging from 33% to 46% atomic Si. No strong dependence of the conductivity of any of the composite structures was seen with variations in area [5,21], temperature [5], or annealing [5]; but a strong dependence with Si content of the Si-rich SiO_2 layers was observed [5]. However, it should be noted that Si-rich SiO_2 layers alone do show a strong dependence of their conductivity on thickness, temperature, and annealing conditions [22]. A lack of dependence of the conductivity on electrode area implies that the injection process is uniform over the scale of dimensions discussed here. The slight temperature dependence of the currents that was observed is consistent with Fowler-Nordheim tunneling at the Si-rich SiO_2-SiO_2 interface limiting the electron injection into the SiO_2 layer [18]. Although the Si islands in the two phase Si-rich SiO_2 layers are converted from an amorphous to crystalline state with high temperature annealing in N_2 or N_2-H_2 ambients, the electronic injection process remains essentially unchanged. This implies that if the Si-rich SiO_2-SiO_2 interface controls the injection into the SiO_2, at least the Si islands at this interface are not drastically changing in size, shape, or density.

A dependence on the Si content of the Si-rich SiO_2 layer of the composite structures was observed for $\lesssim$ 40% atomic Si. This is consistent with an increase in the resistivity of the Si-rich SiO_2 layer with more of the applied voltage being dropped across it rather than the intervening SiO_2 layer. However, once a Si content in the range of $\approx$ 46% atomic Si was reached, small changes (1% to 2%) in the Si content had very little effect on the I-V characteristics. This is shown in Fig. 6 where the ratio R_o of $[N_2O]$ to $[SiH_4]$ in the gas phase was varied from 2 to 5. Only for $R_o = 2$ is there a decrease in the injection efficiency. This was caused by the characteristic of the CVD reactor used here where less Si in the Si-rich SiO_2 layer is deposited at the wafer position in this reactor when $R_o = 3$ is exceeded.

(ii) Photocurrents

To investigate and measure interfacial energy barrier heights, photocurrent as a function of light energy was used [23]. Typical cube root of the photoresponse (photocurrent normalized to the incident photon flux) as a function of light energy is shown in Fig. 7 for an MOS structure with a Si-rich SiO_2 injector on top of SiO_2 and a control MOS structure, with just an SiO_2 layer present both with Al gate electrodes. These measurements were done using chopped light with a.c. detection techniques at voltages where high dark current electron injection from the Si-rich SiO_2 layer into the SiO_2 is occurring [5]. The photocurrent response from 1.5 eV to 3 eV is due to a 90° out of phase signal from the Si substrate while that from

3 eV to 5 eV is due to internal photoemission from the Si islands or Al gate electrode into the SiO_2 regions [5]. Both of these latter two processes have an $\approx$ 3 eV energy barrier [23], and the slight increase in photoresponse with voltage (comparing $V_g = -10$ V to -16 V) is consistent with ordinary Schottky barrier lowering [23]. Clearly no energy barriers $\lesssim$ 2 eV due to uniform homogeneous bandgap grading (as discussed in section I) which would be necessary to explain the dark current data are observed in Fig. 7. D.c. photocurrent measurements lead to the same conclusions and are very similar to Fig. 7. Differences in the photoresponse-energy characteristics were observed when the metal contact was changed from Al to Au. Au has an $\approx$ 1 eV greater work function and therefore an $\approx$ 1 eV greater energy barrier when in contact with SiO_2 [23]. However, these changes were not as large as on the control MOS structures with just an SiO_2 layer present due to the photoconductivity of the trapped space charges (electrons) on the Si islands in the Si-rich SiO_2 layer [5] as discussed in section II-B-i.

C. Physical Model

From the experimental observations discussed in sections II-A and II-B, the large electron current injection into SiO_2 appears to be controlled by the Si-rich SiO_2-SiO_2 interface. Since uniform bandgap grading or stepping seems unlikely from the two phase (Si and SiO_2) nature of the Si-rich SiO_2 and from the photocurrent measurements where no lowered energy barriers due to a homogeneous Si_xO_y material graded or stepped to SiO_2 are observed, a localized physical mechanism seems reasonable. Figure 8 schematically illustrates such a localized mechanism. For this physical model, electrons move easily through the Si-rich SiO_2 (because of its low resistivity) to its interface with the SiO_2 layer. At the Si-rich SiO_2-SiO_2 interface, electrons are injected from the last layer of Si islands into the SiO_2 at lower applied average fields than from a continuous planar surface due to distortion of the local electric field. This enhancement of the local fields occurs because of the size, shape, and density of the Si islands [24] which must have some curved surfaces since they are non-planar (see Fig. 2). To explain the dark I-V data reported here only a field enhancement of $\approx$ 1.5 to 2 [17,19] is necessary due to the strongly field dependent nature of Fowler-Nordheim tunneling from Si into SiO_2 [18]. Fowler-Nordheim tunneling at this interface is consistent with the weak temperature dependence and the strong electric field dependence observed for the dark currents. The photocurrent results, which are only weakly dependent on the electric field, would still yield results which are not drastically different than those of the control structures. The lack of dependence on electrode area is also consistent with this localized model because

the Si islands are much smaller than the electrode area and they are densely packed for the 46% atomic Si material.

The conductivity of the Si-rich SiO_2 layer itself is probably controlled by direct tunneling between the closely spaced Si islands for the 46% atomic Si material (see Fig. 8). For smaller percentages of Si in the Si-rich SiO_2 layer, the conductivity is probably controlled by Poole-Frenkel conduction [25] (field-assisted thermal-activation of carriers from the Si wells). For these lighter doped Si materials, more of the applied voltage is dropped across the Si-rich SiO_2 layer of composite structures and degradation of the current enhancement is seen on dark I-V characteristics. Of course, the density of the Si islands will decrease and possibly their size and shape might change in these lighter doped films which will also affect the injection efficiency at the Si-rich SiO_2-SiO_2 interface. For larger amounts of Si, the Si regions become connected and percolation [26] controls the conduction to the Si-rich SiO_2 interface. For nearly 100% atomic Si, the Si-rich SiO_2-SiO_2 interface would look planar and the electric field distortion would disappear.

There are other localized mechanisms at the Si-rich SiO_2-SiO_2 interface which might also be operating in addition to or instead of field-enhanced tunneling. One such mechanism could be localized energy bandgap grading or stepping occurring in the transition region from Si to SiO_2 surrounding each of the Si islands in the last layer at the Si-rich SiO_2-SiO_2 interface. In a similar fashion, many localized states across the SiO_2 bandgap might be introduced in this same transition region and lead to a localized mechanism involving trap-assisted tunneling [1].

III. EXPERIMENTAL APPLICATIONS

In this section, three experimental applications using structures containing stacked layers of Si-rich SiO_2 and SiO_2 are described. The first application discussed in section III-A uses a DEIS stack in a non-volatile memory device. In section III-B, the improved breakdown characteristics of MOS-type structures with Si-rich SiO_2 layers acting as buffers between the contacting electrode and the SiO_2 layer will be demonstrated. While the third application presented in section III-C involves using Si-rich SiO_2 injectors as a high electronic current source at moderate applied electric fields for charge trapping studies in SiO_2 layers.

A. DEIS EAROM

A novel non-volatile memory device using a DEIS stack for putting electrons on or taking them off a floating poly-Si storage layer is depicted schematically in Fig. 9 [19,21]. This device is essentially an MOS field effect transistor (MOSFET) [25,27] with an energetically deep storage well for electrons formed by the isolated poly-Si electrode. When electrons are put on this floating poly-Si layer, the internal electric field they generate affects the field at the substrate Si-SiO_2 interface. For the n-channel structure (electrons are the mobile charge carrier in the Si surface channel when the device is turned on) shown in Fig. 9, the charge state of the floating poly-Si layer is sensed when an electron current flows in the channel region between the source and drain contacts. The channel is turned on by putting a large enough positive voltage on the control gate to invert the Si surface by pulling minority carriers (electrons in this case) to the Si-SiO_2 interface. When electrons are trapped on the floating poly-Si layer, more positive gate voltage is required to invert the Si surface by overcoming the opposing electric field introduced by the trapped negative charge. This voltage at which the channel becomes conducting is called the turn-on or threshold voltage, V_T [25,27]. Determining the charge state of the floating poly-Si layer by sensing V_T is called the "read" operation of the non-volatile memory.

The difference between the memory described here and others using a similar floating poly-Si storage layer [28,29] is the way in which electrons are put on (called the "write" operation) or taken off (called the "erase" operation) the poly-Si. Here a DEIS stack is used to give write/erase operations at moderate gate voltages and low power because of the enhanced electron injection phenomena associated with the Si-rich SiO_2-SiO_2 interfaces. Most commercially available floating poly-Si gate non-volatile memories are written by avalanching a Si junction to get "hot" electrons over the highly blocking 3 eV barrier at the Si-SiO_2 interface [28,29]. This requires much more power consumption because the Si currents are $\gtrsim 10^5$ times the SiO_2 currents. These devices are typically very difficult to erase, usually requiring photo-discharge of the trapped electrons off the poly-Si with ultraviolet (UV) light which takes $\gtrsim$ 10 minutes [28,29]. The DEIS EAROMs described here can be written and erased at comparable voltages ($\lesssim$ 30 V) and speeds ($\lesssim$ 5 msec) at least 10^5 times.

Figure 10 demonstrates the write/erase cycling of the DEIS EAROM in Fig. 9. The turn-on voltage V_T is used as an indication of the charge state of the floating poly-Si where a positive value of V_T implies a written condition of stored electrons and a negative value of V_T implies an over-erased condition of ionized donors. A virgin as-fabricated device which is approximately in a neutral charge state initially, is cycled for the voltages indicated by similar symbols (solid characters for write and open characters for erase). A control structure with just an SiO_2 layer between the control gate and floating poly-Si layer could not be written for

similar voltages. However, the control structure can be over-erased somewhat because of the rough nature of the top surface of the poly-Si layer [20,30,31] which gives field-enhanced local injection near the tips of the asperities on this Si surface into the SiO_2 layer between the control and floating gates [30]. A collapse in the V_T window is observed to occur after $\approx 10^4$ to 10^5 write/erase cycles. This is due to a permanent trapped electronic space charge build-up in the intervening CVD SiO_2 layer due to H_2O related trapping sites [1,2,17,21]. This negative trapped charge generates an internal electric field which reduces the field at either Si-rich SiO_2-SiO_2 injecting interface, and therefore reduces the injected current from the control gate or off the floating poly-Si layer which in turn determines V_T. The effect of this trapped charge can be overcome by increasing the write/erase gate voltages so the electric fields at the injecting interfaces are returned to their initial values [21]. Also, the trapped electrons can be discharged thermally by heating the device to temperatures $\gtrsim 200°C$ [2,3,21]. Recently, write/erase voltages between 10 and 15 V have been obtained on DEIS EAROMs like those in Fig. 9 with thinner oxide layers between the single crystal Si substrate and the floating poly-Si layer [21].

Although the DEIS EAROM described here has excellent write/erase characteristics, it must also retain the stored electronic information for long periods of time (10-100 years) when no power is applied which gives it a "non-volatile" nature. Figure 11 shows that the DEIS EAROM for a grounded gate electrode condition has the same retention characteristics as a commercially available floating poly-Si gate device with an SiO_2 layer between the control and floating gates. The discharge rate for $\approx 5 \times 10^{12}$ stored electrons/cm^2 for temperatures between 25°C and 300°C is similar for a control device, DEIS EAROM, or a single electron injector structure (SEIS) EAROM with only a Si-rich SiO_2 injector under the control gate. The electron discharge which becomes significant after $\approx 10^5$ sec and 10^4 sec at 200°C and 300°C, respectively, can be shown to be thermally activated with a barrier energy of ≈ 3 eV for zero electric field [21]. This is consistent with electron discharge from a Si well surrounded by SiO_2 [23]. At normal device operating temperatures between 25°C and 80°C, this thermal activation process would give only 5% charge loss in $\gtrsim 3 \times 10^7$ years [21]. The DEIS structure in Fig. 11 shows a similar retention characteristic compared to the control structure because the local fields are not high enough to significantly cause charge loss for the times considered by the enhanced current injection mechanism via tunneling into the SiO_2 layer which is only weakly dependent on temperature [5].

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B. Low Voltage Breakdown

Numerous measurements on many large area (.006 cm^2) capacitors with DEIS or SEIS stacks have shown that low voltage breakdowns are drastically reduced compared to MOS controls with just an SiO_2 layer present. A low voltage breakdown is one that causes destructive shorting of the SiO_2 layer at average electric fields which are less than the "intrinsic" dielectric strength of SiO_2. This intrinsic value is regarded as usually between 8-12 MV/cm depending on oxide thickness [32]. Figure 12 demonstrates this for a DEIS structure which only shows 3 capacitors out of approximately 100 breaking down at low average fields after being sequentially ramped to current levels of 2×10^{-6} A and then 5×10^{-4} A, respectively. The portion of this histogram (in 0.5 MV/cm bins) between 8.5 and 10.5 MV/cm is simply a measure of the reproducibility across a wafer of the gate voltage needed to draw a dark current of 5×10^{-4} A ($\approx$ .1 A/cm^2). This scatter in the histogram is due to variations in the intervening CVD SiO_2 thickness which is on the order of 10% for the CVD reactor used. Ramping the voltage to the same current level again would produce essentially the same distribution shown in Fig. 12. The breakdown distribution on the control structure fabricated in an identical fashion except for the Si-rich SiO_2 injecting layers and subjected to the same ramped voltage sequence is shown in Fig. 13. Clearly most of the 100 capacitors of the control wafer have broken down at lower voltages than expected for a 5×10^{-4} A Fowler-Nordheim current from the Al gate electrode into the SiO_2 layer [18].

Low voltage breakdowns are usually associated with localized defects or asperities at the contacting electrode-SiO_2 interface where the injection current increases locally in a drastic manner compared to the remaining electrode area causing shorting of the Si substrate to the gate electrode [32]. The DEIS structure (or SEIS for the polarity favoring injection into SiO_2 via the Si-rich SiO_2 layer) minimizes these localized contact effects that occur at low average electric fields by building up a reversible space charge layer in the Si-rich SiO_2 layer opposite the defect or asperity at the contacting electrode-Si-rich SiO_2 interface. This field screening effect due to the trapped space charge has been demonstrated previously for minimizing injection from a rough poly-Si surface into SiO_2 [20,30,31] by using a "W" trapping layer which will build up a stable trapped electron distribution $\approx$ 70 Å from the injecting interface [31].

C. SiO_2 Trapping Characterization

Charge trapping ledges in dark current as a function of ramped gate voltage characteristics on DEIS or SEIS structures can yield useful information on trapping kinetics and trapped charge location. Examples of such ledges were seen in Fig. 4 at a current level of $\approx 10^{-7}$ A due to certain H_2O related sites in the intervening CVD SiO_2 layer. The ledge appears, during

a dark current – ramped gate voltage measurement, when a current level is reached at which the SiO_2 traps start to fill significantly and build up an internal electric field opposed to the increasing applied field [17,33]. The field near the injecting interface is held approximately constant until the traps are filled which therefore keeps the electron injection current nearly constant. The ledge is much more pronounced on the DEIS structures as compared to the control because of the lower average electric field in the bulk of the SiO_2 layer where the electrons are trapped [33]. This lower field minimizes field ionization of trapped charges and/or a reduction in the capture rate of the charge carriers [1]. Similar ledges are also seen for injection from the top Si-rich SiO_2 injector for negative gate voltage bias V_g^- [17,19]. From the current position of the ledge I_l and its voltage width ΔV_{g_l}, it can be easily shown that the SiO_2 trapping parameters of the electron capture cross section σ_{c_0} and the total number of traps per unit area N_{∞_0} can be determined, assuming the Si-rich SiO_2 layers are highly conductive compared to the SiO_2 layer, from the relationships [17,33]

$$\sigma_{c_0} = \frac{qA(dV_g/dt)}{\Delta V_{g_l} I_l} \tag{1}$$

and

$$N_{\infty_0} = \frac{\varepsilon_0 \Delta V_{g_l}}{q(\ell_0 - \bar{x}_0)} \tag{2}$$

where A is the electrode area, q is the charge on an electron (-1.6×10^{-19} coul), dV_g/dt is the voltage ramp rate, ℓ_0 is the total SiO_2 layer thickness, $\bar{x}_0$ is the centroid of the trapped electron distribution measured from the appropriate injecting Si-rich SiO_2-SiO_2 interface, and ε_0 is the low frequency permittivity of SiO_2 ($3.9 \times 8.86 \times 10^{-14}$ F/cm). Furthermore, if partial ledge widths $\Delta V_g^{\pm}$ are measured for both polarities of DEIS structures [17,19] or if ΔV_g^- is measured for a SEIS with only a top Si-rich SiO_2 injector and the flat-band voltage shift ΔV_{FB} is deduced from capacitance-voltage measurements [17], it can be shown that the charge centroid $\bar{x}'_0$ measured from the top Si-rich SiO_2-SiO_2 interface and the number of trapped bulk SiO_2 charges per unit area N_0 can be determined from [17]

$$\frac{\bar{x}'_0}{\ell_0} = \left[1 - \frac{\Delta V_g^-}{\Delta V_g^+(\Delta V_{FB})}\right]^{-1} \tag{3}$$

and

$$N_0 = \frac{\varepsilon_0}{q\ell_0}\left[\Delta V_g^- - \Delta V_g^+(\Delta V_{FB})\right] \tag{4}$$

where it is assumed that the Si-rich SiO_2 is highly conductive and thin compared to the SiO_2 layer [5,6,17] with the (ΔV_{FB}) term replacing ΔV_g^+ when a SEIS is used. These relationships given by Eqs. 3 and 4 are the same as the photocurrent-voltage (photo I-V) equations [34] with essentially the same physics applying; that is, $\Delta V_g^{\pm}$ are a measure of the reduction in field at the appropriate injecting interface due to the trapped charge build-up in the bulk of the SiO_2 layer.

Purposely added "W" traps, CVD SiO_2 traps, and normal thermal SiO_2 traps have been studied using these ramp I-V techniques on DEIS or SEIS capacitors [17,19]. The results of these measurements have been shown to give agreement with the determination of the trapping parameters using the standard techniques of avalanche-injection with flat-band voltage tracking [2,35] and photo I-V [34]. The ramp I-V technique has the advantage that it is simpler and faster than the standard techniques, although probably less accurate. For instance, it would be appropriate when large numbers of structures must be monitored.

IV. CONCLUSIONS

Si rich SiO_2 layers incorporated as an intervening layer between contacting electrodes and a SiO_2 layer have been demonstrated to give high electronic current injection at moderate applied average electric fields. This electron injection phenomena is believed to be controlled by electric field distortion at the Si-rich SiO_2-SiO_2 interface associated with the two phase nature of the Si-rich SiO_2 material. Several electrical and physical measurements support this model.

Structures based on the "insulator engineering" discussed here such as the DEIS with its stacked layers of Si-rich SiO_2 and SiO_2, have been shown to have importance in the area of non-volatile memory, the area of minimizing low voltage breakdowns in MOS structures, and the area of rapidly measuring charge trapping parameters of impurities either purposely or inadvertently introduced into SiO_2 films. The possibility of even faster switching times (perhaps $\leq$ 1 μsec) for EAROM structures could possibly be demonstrated as devices using DEIS stacks are optimized further through increased electron injection efficiency of the injectors or through design considerations where most of the applied voltage is dropped across the DEIS stack rather than any of the other SiO_2 layers.

In the future, other materials, such as Si rich Si_3N_4, may also give enhanced electron injection into SiO_2 at even lower applied fields. DEIS stacks with Si_3N_4 replacing the SiO_2 layer is another interesting possibility in the realm of this new field of insulator engineering.

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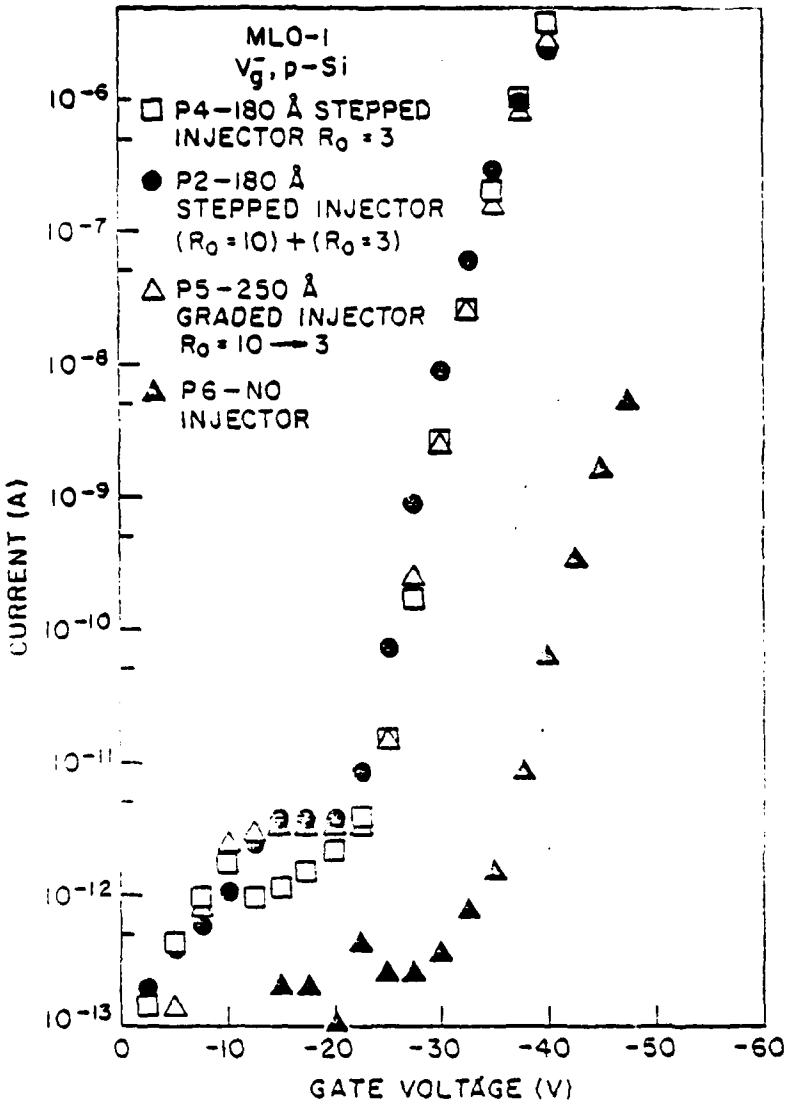

Figure 1. Point by point magnitude of the dark current as a function of negative gate voltage on various GI-MIS and SI-MIS structures. In this measurement, the gate voltage was stepped by −2.5 V starting from 0 V every 20 sec with the dark current being measured 18 sec after each voltage step increase. The Si-rich SiO_2 layer was either stepped or graded with R_o defined as $[N_2O]/[SiH_4]$ as an indicator of the Si content of this layer. R_o from 10 (40% atomic Si) to 3 (46% atomic Si) was used with Si content increasing towards the top metal gate electrode when several layers were stacked on top of the underlying 550 Å thick thermal SiO_2 layer (R_o = 10 + 3) or when a graded layer was used (R_o = 10 → 3). Taken from Reference 5.

Figure 2. High-resolution cross-section TEM of a dual electron injector structure (DEIS) stack on top of the first (floating) poly-Si layer with the lower part of the top (control gate) poly-Si layer showing in uppermost part of the micrograph. The DEIS stack is composed of sequentially deposited layers of Si-rich SiO_2, SiO_2, and Si-rich SiO_2 with 46% atomic Si in the Si-rich SiO_2 layers. The entire structure was annealed at 1000°C in N_2 for 30 min.

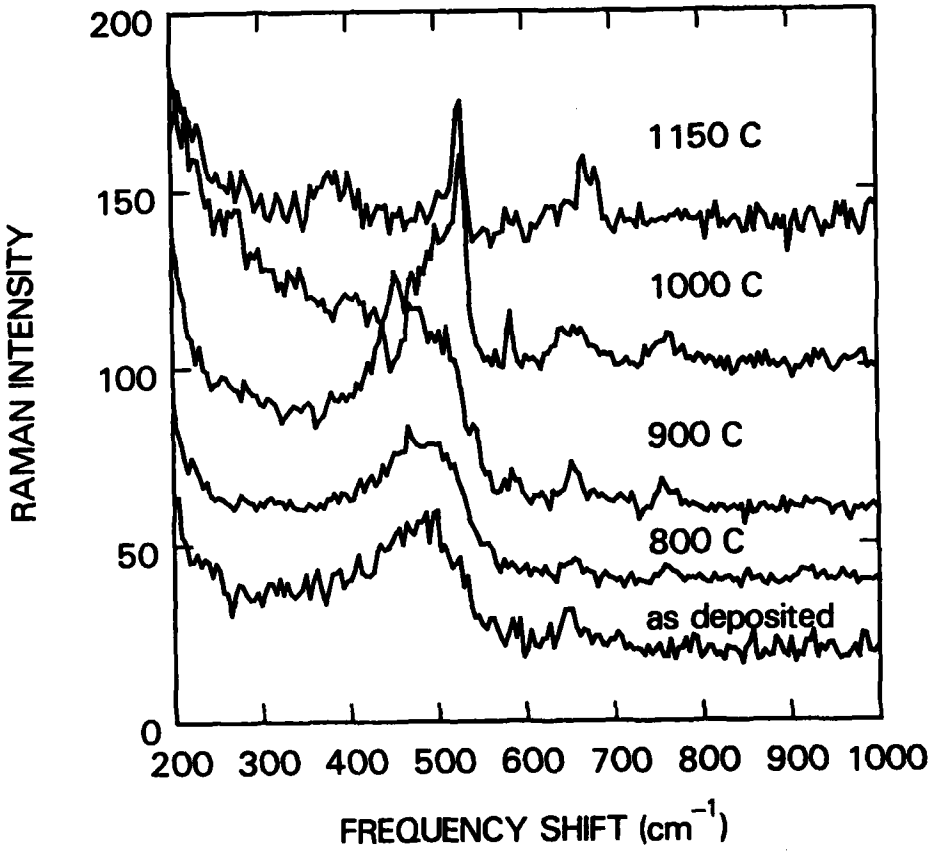

Figure 3. Raman scattering spectra for a Si-rich SiO_2 film with 46% atomic Si which was sequentially annealed in N_2 for 30 minutes at 800°C, 900°C, 1000°C and 1150°C from its as-deposited state. Taken from Reference 14.

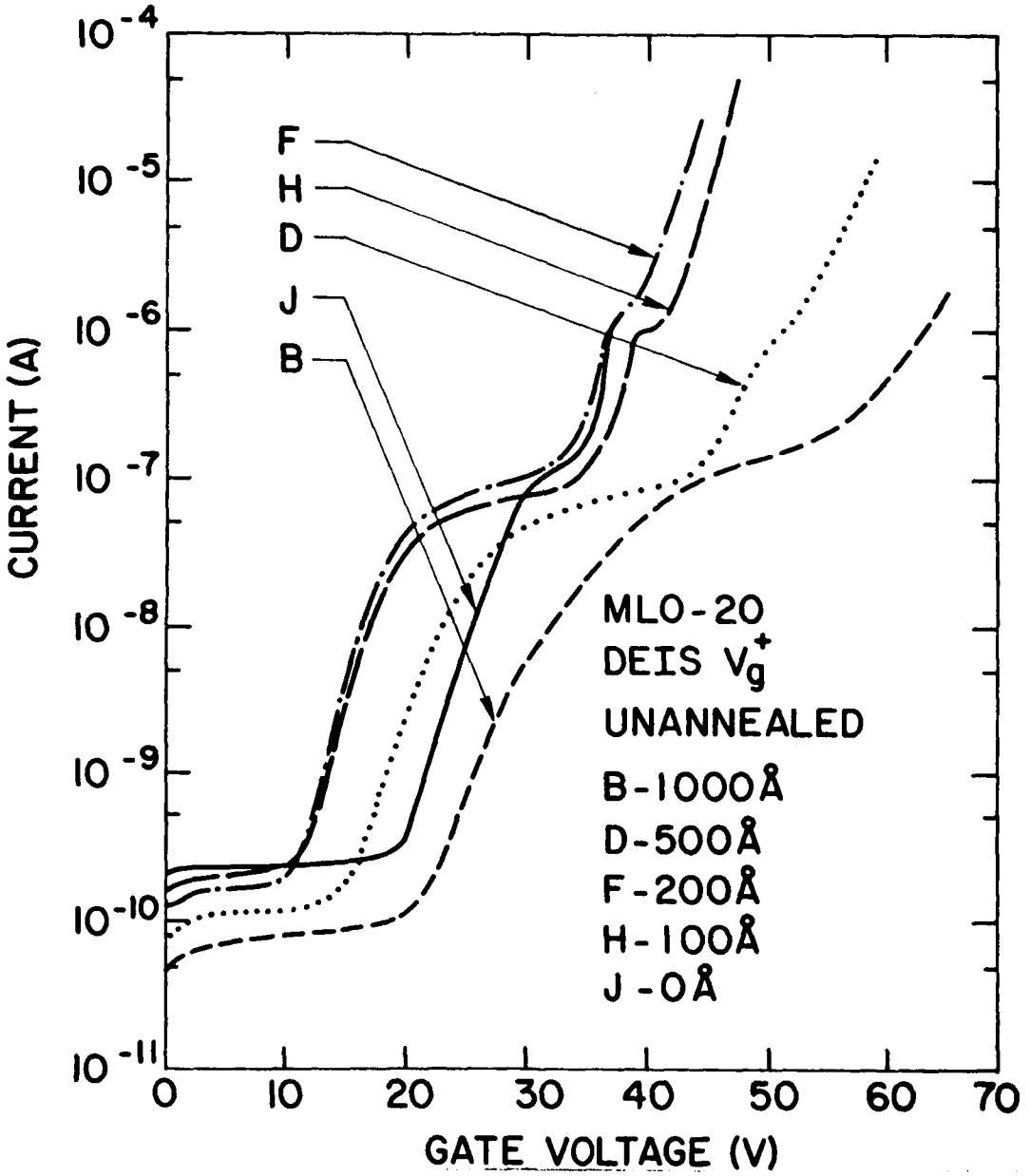

Figure 4. Magnitude of the dark current as a function of positive ramped (0.47 V/sec) gate voltage on DEIS capacitor structures with various CVD Si-rich SiO_2 (46% atomic Si) injector thicknesses (0 Å, 100 Å, 200 Å, 500 Å, and 1000 Å) and a 400 Å intervening CVD SiO_2 layer. Structures were not annealed prior to Al gate electrode deposition.

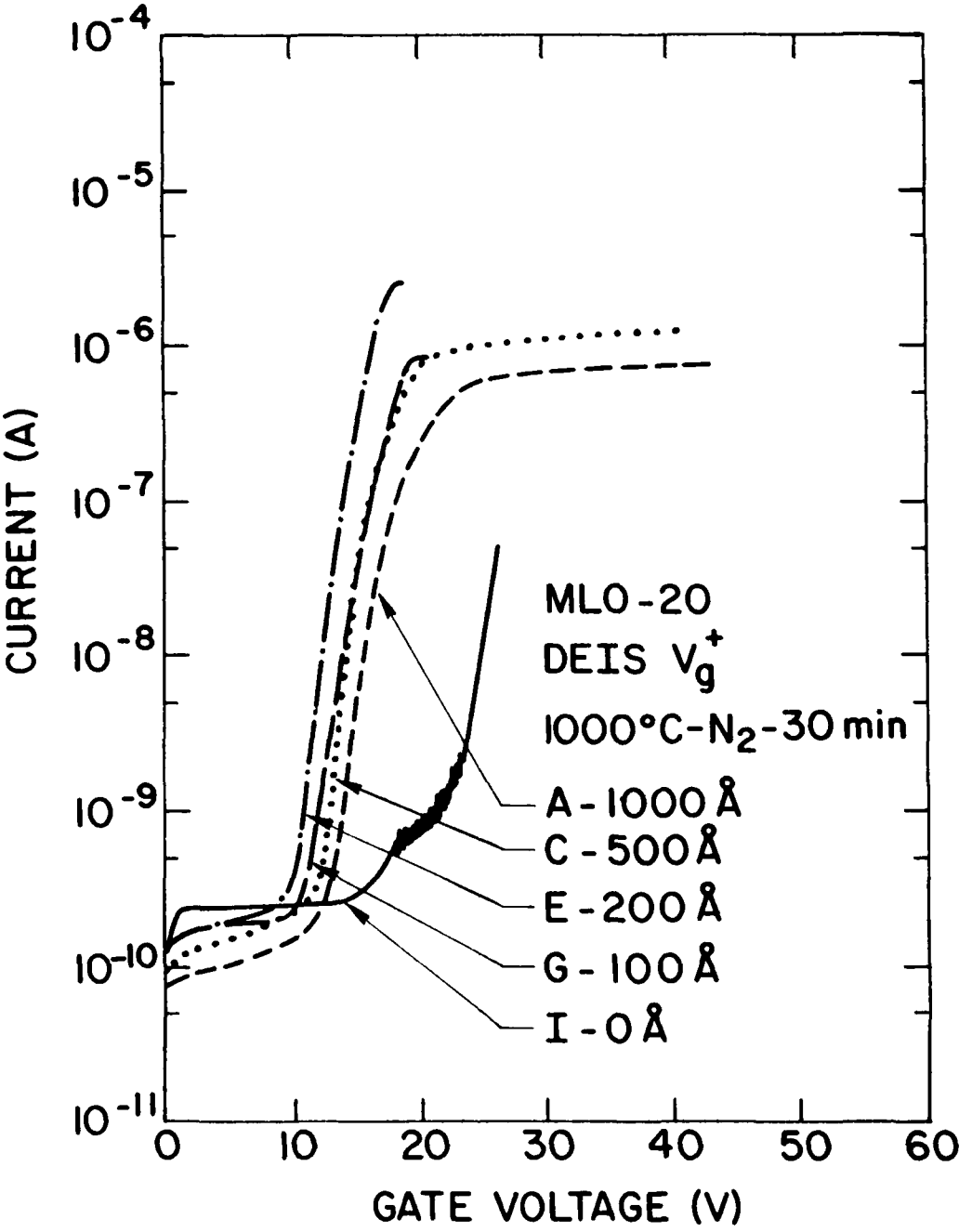

Figure 5. Magnitude of the dark current as a function of positive ramped (0.47 V/sec) gate voltage on DEIS capacitor structures which are identical to those in Fig. 4 except that they were annealed at 1000°C in N_2 for 30 min. prior to Al gate metallization.

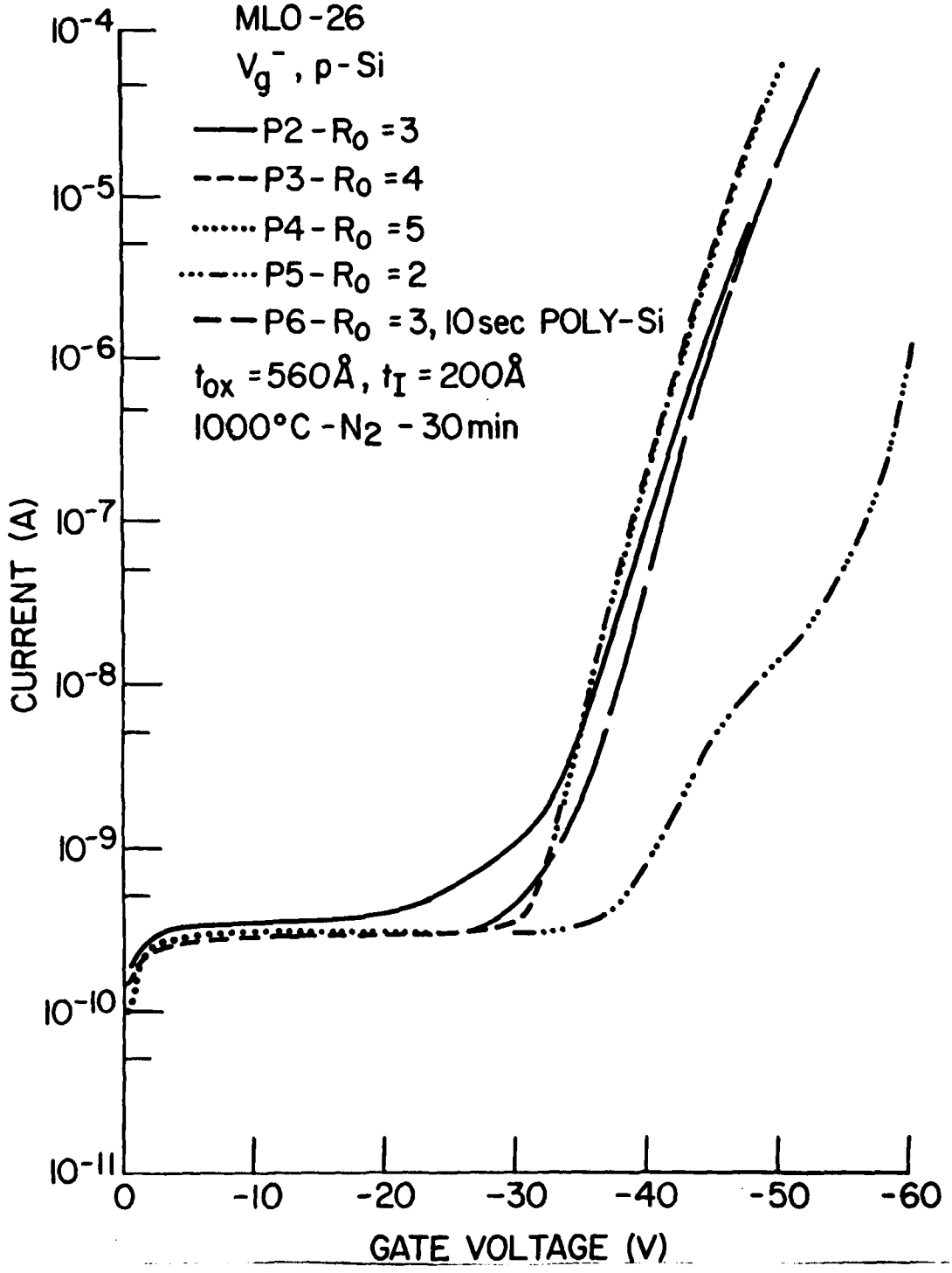

Figure 6. Magnitude of the dark current as a function of negative ramped (−0.47 V/sec) gate voltage on single Si-rich SiO_2 injector structures with various amounts of incorporated Si in the vicinity of 46%. The ratio R_o of $[N_2O]/[SiH_4]$ is used as an indicator of the Si changes. The injectors were all 200 Å thick with an underlying thermal oxide of 560 Å in thickness.

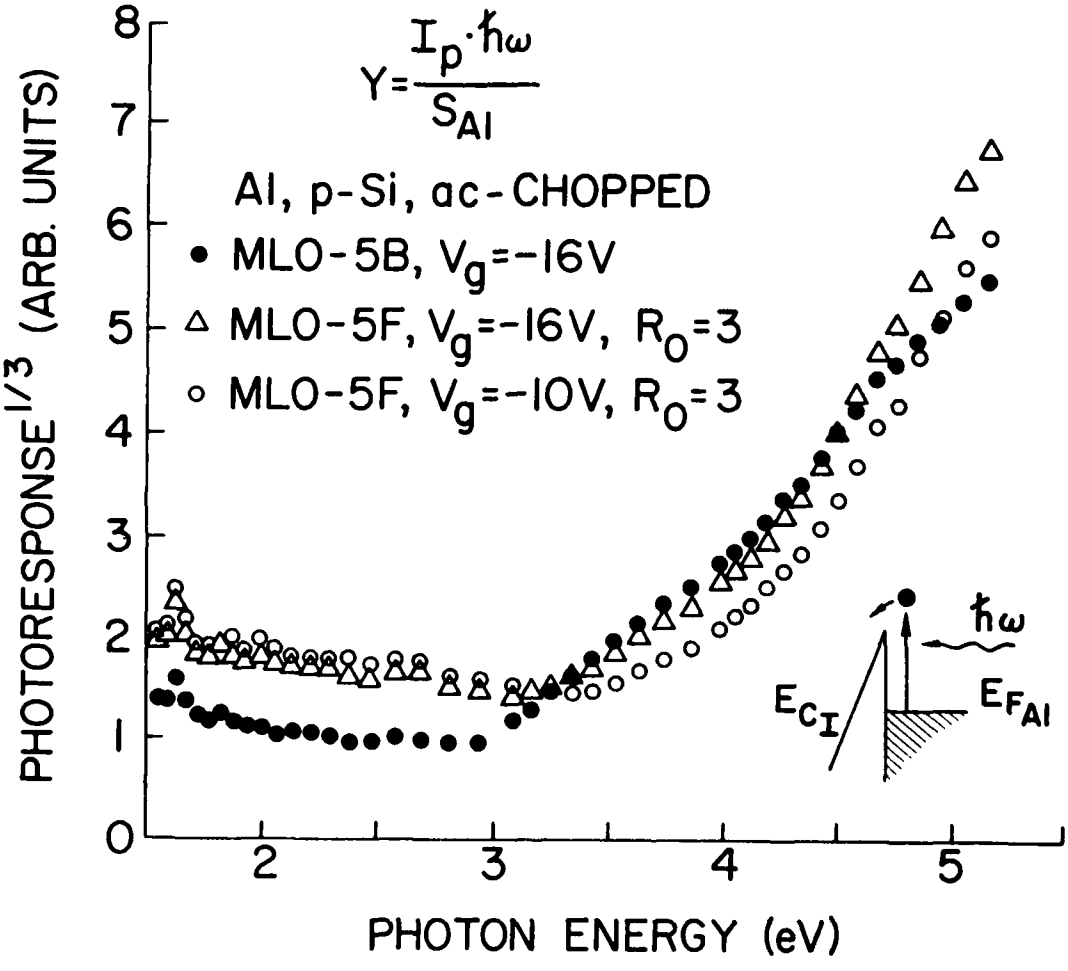

Figure 7. Cube root of the a.c. photoresponse as a function of photon energy on various SI-MIS structures under negative gate voltage bias. R_0 = 3 (46% atomic Si) Si-rich SiO_2 material with a thickness of 120 Å was used for the injector on MLO-5F, the gate electrode was Al (135 Å), and the thermal SiO_2 thickness was 290 Å. MLO-5B is the control structure with no injector. Taken from Reference 5.

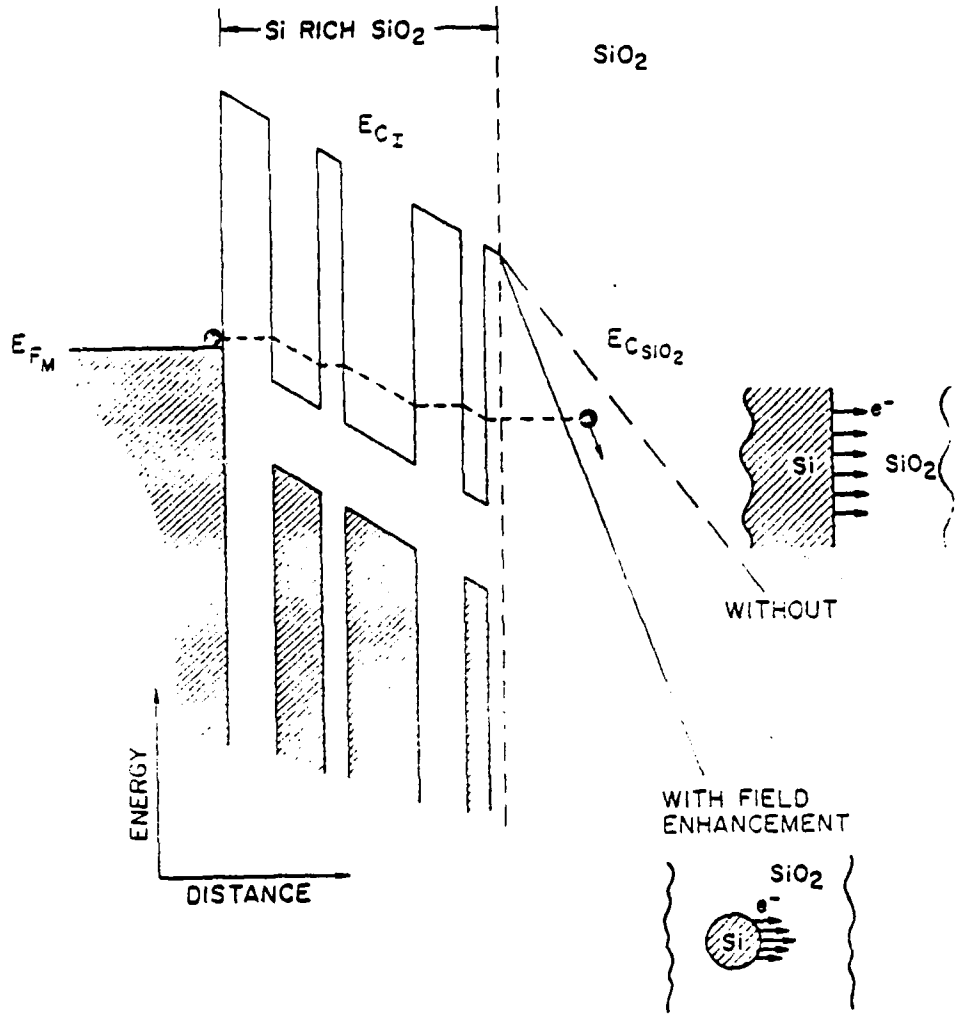

Figure 8. Schematic energy band representation of conduction in the Si-rich SiO_2 layer via direct tunneling between isolated Si regions in the SiO_2 matrix of this two phase system and subsequent high field injection into the underlying SiO_2 region due to local electric field enhancement caused by the curved surfaces of the Si regions. Electronic Fowler-Nordheim tunneling into SiO_2 from a planar Si surface is shown for comparison. Taken from Reference 5.

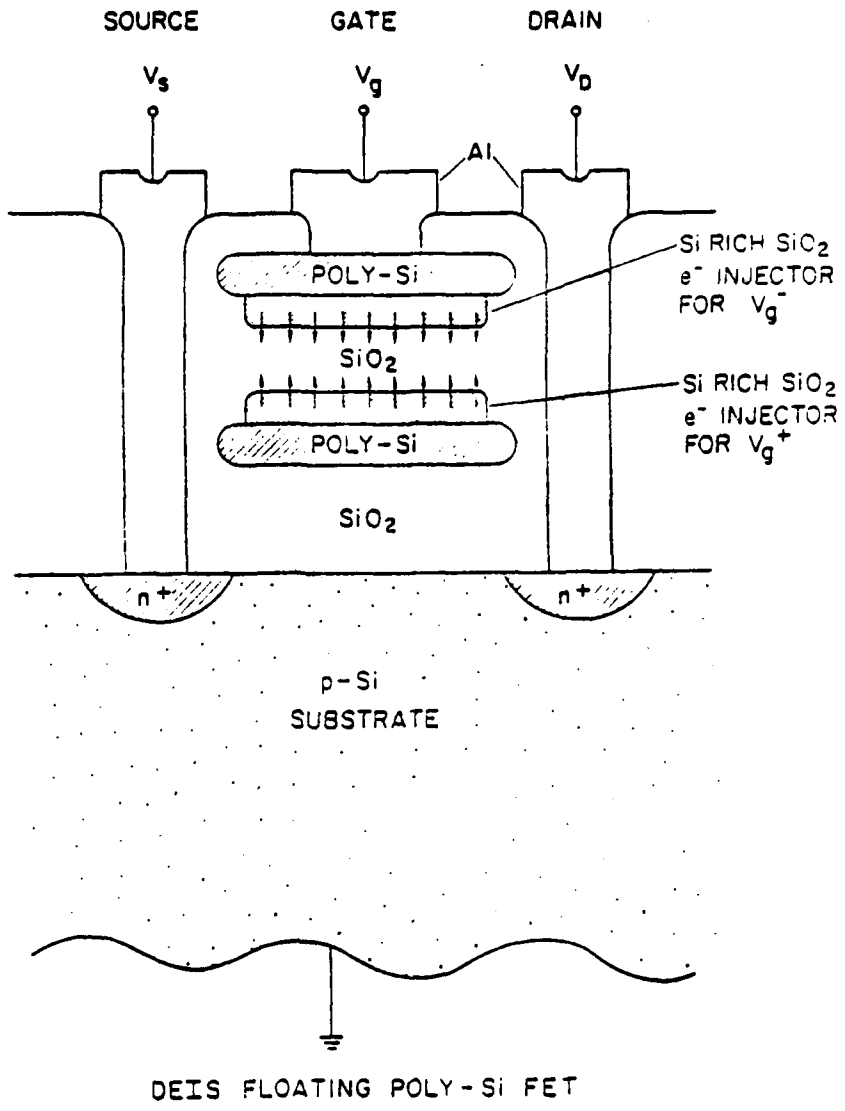

Figure 9. Schematic representation of a non-volatile n-channel field-effect-transistor (FET) memory using a DEIS stack between a control gate and a floating poly-Si layer. Writing (erasing) is performed by applying a negative (positive) voltage, V_g^- (V_g^+), to the control gate which injects electrons from the top (bottom) Si-rich SiO_2 injector to the floating poly-Si storage layer (back to the control gate). Structure is not drawn to scale. Taken from Reference 19.

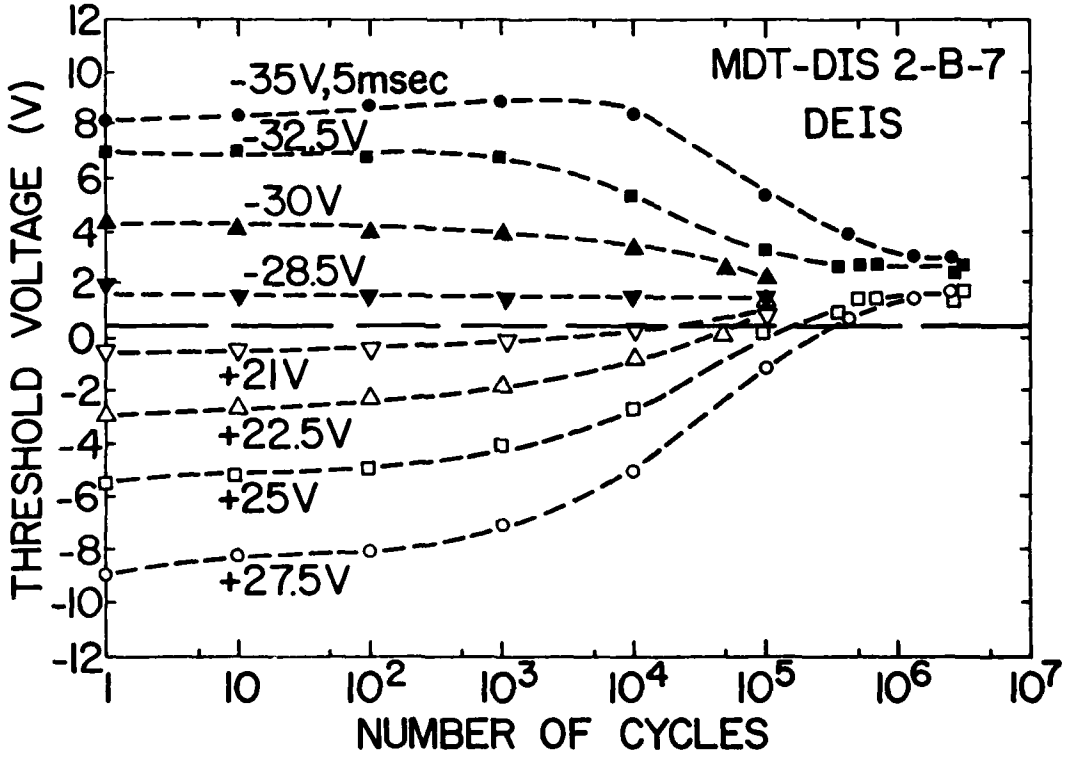

Figure 10. Threshold voltage after writing and erasing as a function of the number of write/erase cycles for various $V_{W/E}$ conditions on a DEIS FET from wafer MDT-DIS 2-B (340 Å gate oxide from the floating poly-Si layer to the Si substrate and a CVD DEIS stack of 150 Å Si-rich SiO_2 - 100 Å SiO_2 - 150 Å Si-rich SiO_2 from floating poly-Si to control gate poly-Si with the Si-rich SiO_2 having 46% atomic Si). Solid and open symbols correspond to the threshold voltage after writing and erasing for 5 msec, respectively. The horizontal dashed line indicates the initial threshold voltage of the as-fabricated FETs before cycling. Taken from Reference 21.

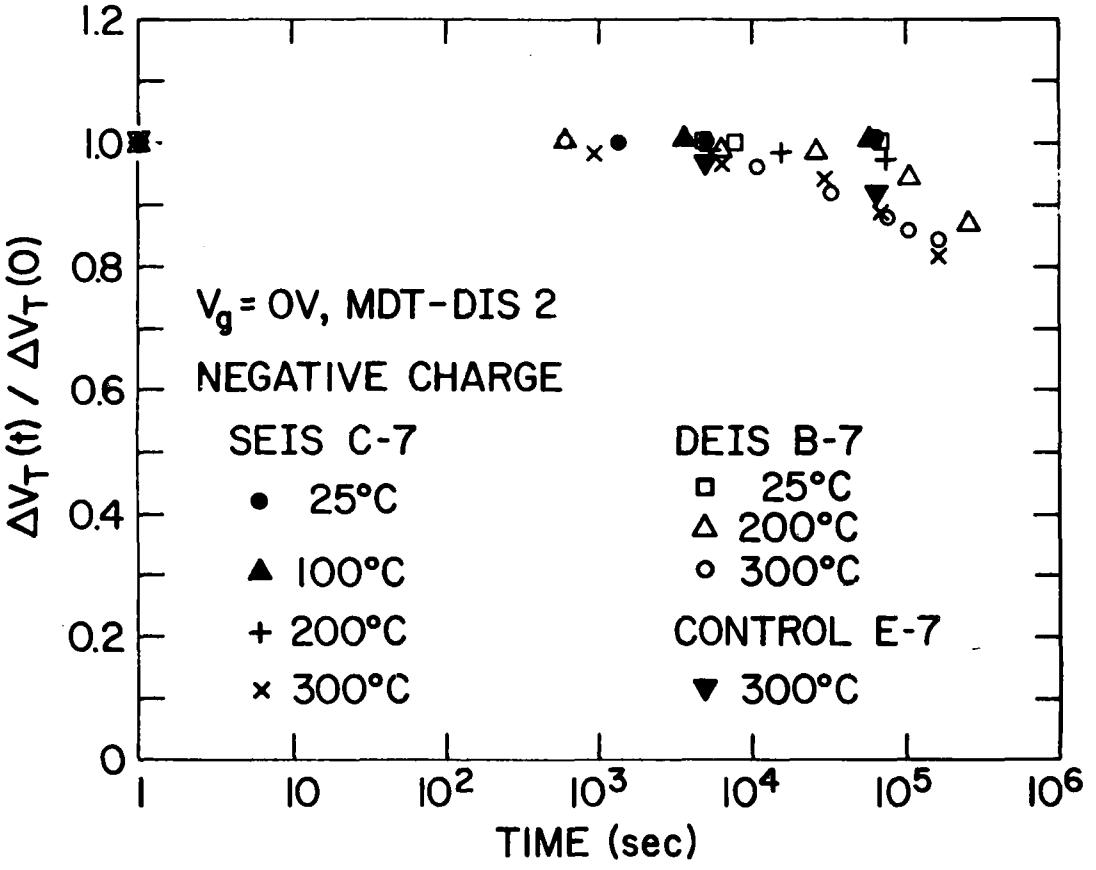

Figure 11. Stored electronic (initially $\approx 5 \times 10^{12}$ cm^{-2}) charge loss as a function of time on DEIS, SEIS, and the control FETs from the MDT-DIS 2 series for a grounded gate condition $V_g = 0$ at temperatures of 25°C, 100°C, 200°C, and 300°C. Charge loss is calculated in normalized units of $\Delta V_T(t)/\Delta V_T(0)$ as described in the text. The SEIS and control FET had stacks of 100 Å SiO_2 - 150 Å Si-rich SiO_2 and 100 Å SiO_2, respectively, between floating poly-Si and control gate poly-Si. The DEIS FETs are described in Fig. 10. Taken from Reference 21.

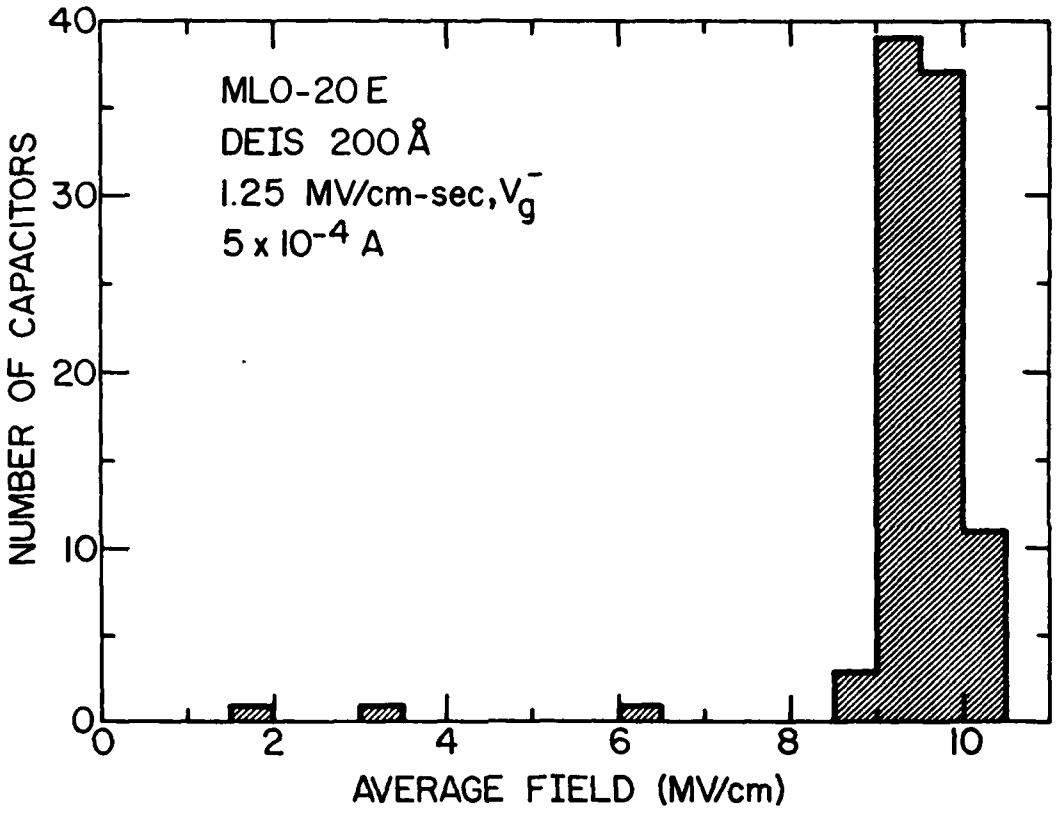

Figure 12. Histogram (in 0.5 MV/cm bins) of the number of capacitors (.006 cm^2 area) on a DEIS wafer to draw a current of 5×10^{-4} A as a function of the average oxide field, sequentially performed after first ramping to 2×10^{-6} A. The CVD Si-rich SiO_2 injectors were 200 Å thick and contained 46% atomic Si, the intervening CVD SiO_2 was 400 Å thick, and the structure was annealed at 1000°C in N_2 for 30 min prior to Al metallization. Samples were ramped with negative gate voltage bias from 0 V at a rate of 1.25 MV/cm-sec. Taken from Reference 21.

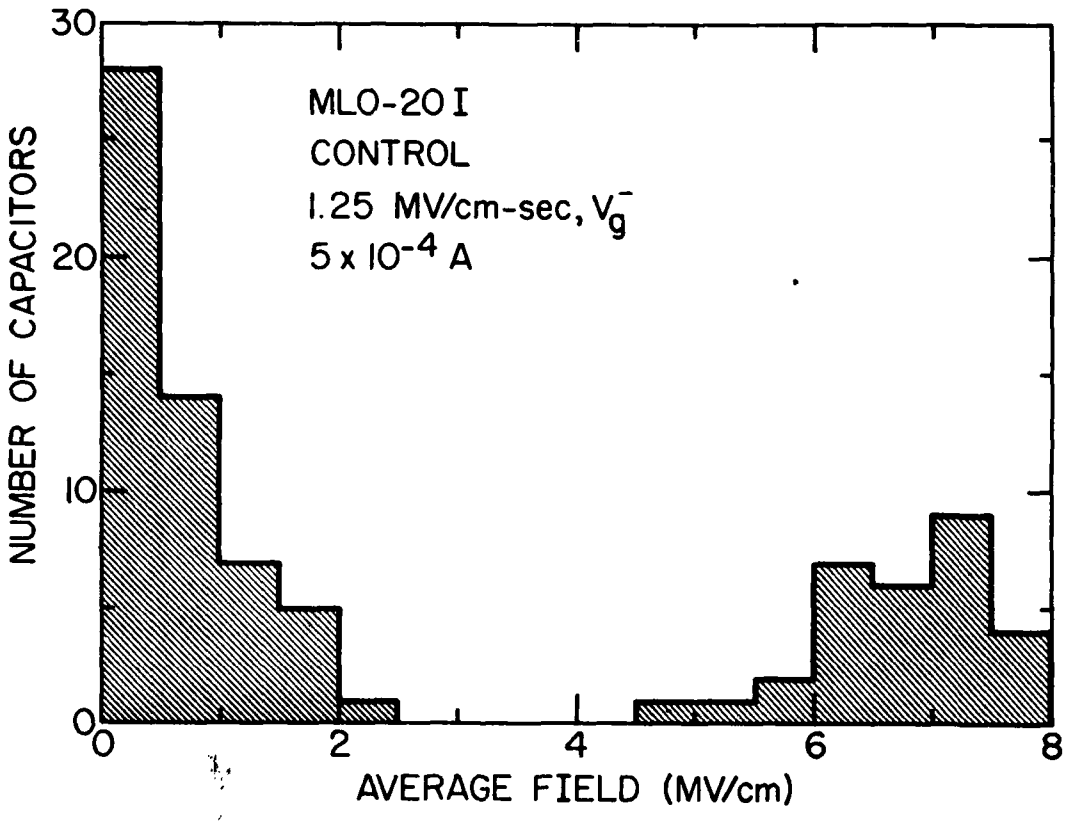

Figure 13. Histogram (in 0.5 MV/cm bins) of the number of capacitors (.006 cm^2 area) on a control wafer with just a 400 Å thick CVD SiO_2 layer to draw a current of 5×10^{-4} A as a function of the average oxide field, sequentially performed after first ramping to 2×10^{-6} A. The structure was annealed at 1000°C in N_2 for 30 min prior to Al metallization. Same experimental conditions as in Fig. 12 were used. Taken from Reference 21.

CHARGE TRAPPING STUDIES IN SiO_2 USING HIGH CURRENT INJECTION FROM Si RICH SiO_2 FILMS

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Abstract: The high electron injection phenomenon of Si rich SiO_2 films deposited on top of SiO_2 can be used for novel charge trapping studies of sites normally present or purposely introduced in the SiO_2. From the position and extent of current ledges observed in dark current as a function of ramped gate voltage (I-V), the capture cross section and total number of traps can be determined. Using these measurements with capacitance as a function of gate voltage (C-V), the trap distribution centroid and number of trapped charges can also be found. Several experimental examples are given including trapping in thermal SiO_2, in chemically vapor deposited (CVD) SiO_2, and on W less than a monolayer thick sandwiched between thermal and CVD SiO_2. These SI-MIS ramp I-V results for the trapping parameters are shown to be in good agreement with those determined using the conventional photo I-V and avalanche injection with flat-band voltage tracking techniques. A numerical simulation of the ramp I-V measurements assuming electric field-enhanced Fowler-Nordheim tunneling at the Si rich SiO_2-SiO_2 interface is described and is shown to give good agreement with the experimental data. These techniques for SI-MIS structures are faster and easier, although less accurate, than the conventional techniques.

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I. INTRODUCTION

Thin Si rich SiO_2 layers deposited on SiO_2 and incorporated into stepped or graded insulator metal-insulator-silicon (SI-MIS or GI-MIS) structures, as shown in Fig. 1, give high electron injection into the SiO_2 layer at moderate negative gate voltages [1,2]. Fig. 2 illustrates this phenomenon and compares various SI-MIS and GI-MIS structures to a control sample with no Si rich SiO_2 injector layer present, but otherwise processed in an identical fashion. This high current injection at moderate gate voltages will be shown to allow dark current as a function of gate voltage (dark I-V) characteristics to be used for easy, rapid, trap characterization on sites normally present or purposely introduced in SiO_2 layers. Fig. 3 shows charge trapping ledges caused by traps in a chemically vapor deposited (CVD) SiO_2 layer on top of thermal SiO_2 [3] and on W (less than a monolayer thick) related sites sandwiched between these two oxide layers [3-8]. The ledges only appear on samples fabricated with the thin Si rich SiO_2 injector. No ledges are seen on samples without the injector present, although in principle they should appear [9]. This absence of trapping ledges is due to the high applied electric fields necessary to get significant current injection in normal MIS structures. The high electric fields probably pull charge carriers out of the traps as soon as they are captured possibly by field ionization, and/or the high fields decrease the trapping rate of the carriers [3]. As will be shown here, the position and extent of the charge trapping ledges in dark I-V characteristics will give the trapping parameters of interest: initial trapping probability, capture cross-section, and total number of traps [3]. When these dark I-V characteristics are used together with capacitance as a function of gate voltage (C-V) measurements [10,11], the centroid and total amount of trapped charge can also be determined.

The details of the high current injection phenomena produced by the CVD Si rich SiO_2 layers has been discussed in a previous publication [2]. The high current is believed to be caused by a localized electric field distortion at the Si rich SiO_2 – SiO_2 interface due to the two phase (Si and SiO_2) nature of this material [12-14], by the size (tens of Angstroms) and large density of the Si regions [12,13], and by the low resistivity of the Si rich SiO_2 layer itself compared to SiO_2 [14]. However, the trapping parameters of sites in the SiO_2 region (not the Si rich SiO_2 injector) are independent of the details of the injection process; they depend only on the magnitude of the current injected at moderate gate voltages.

Three different trapping sites will be investigated using the SI-MIS ramp I-V technique described here. These sites include traps normally present in thermal SiO_2 layers grown on Si substrates [15,16], traps normally present in CVD SiO_2 layers deposited on thermal SiO_2 [3], and W related trapping sites produced by depositing W, less than a monolayer thick, between

thermal and CVD SiO_2 layers [3-8]. In each case, the results of trap characterization from the SI-MIS ramp I-V measurements will be compared to results obtained using conventional avalanche-injection with flat-band voltage tracking [16-18] and photocurrent as a function of gate voltage (photo I-V) techniques [5,19,20]. This comparison shows good agreement in all cases. The main advantages of SI-MIS ramp I-V measurements will be shown to be its speed and simplicity, particularly when large numbers of samples must be tested.

In section II, the sample preparation and experimental apparatus will be described. In section III, the SI-MIS ramp I-V technique will be presented together with the experimental results for the three trapping sites under consideration here. Comparison with conventional techniques to show the accuracy of the technique will also be performed. Finally in section IV, a numerical simulation will be compared to the experimental ramp I-V results.

II. EXPERIMENTAL

A. Sample Preparation

The Si rich SiO_2 layers were chemically vapor deposited (CVD) on top of thermal SiO_2 layers grown on <100> 2 Ωcm p-type single crystal Si substrates or on top of CVD SiO_2 layers. All thermal SiO_2 layers were given a 5 min. - 1000°C - N_2 anneal prior to being removed from the furnace. In some cases, CVD SiO_2 layers were stacked on top of the thermal SiO_2 layers prior to CVD Si rich SiO_2 deposition. A top gate electrode of Al with an area of .006 cm^2 and a thickness of 4,000 Å was then deposited from resistance heated W boats under a vacuum of less than 10^{-6} Torr. All Al electrode samples had a 400°C forming gas (90% N_2 - 10% H_2) anneal for 20 min performed after metallization. In some samples, a W layer less than a monolayer in thickness was deposited between the thermal and CVD SiO_2. The samples used in this study are summarized below:

MLO - 2D	Si - thermal SiO_2 (109 Å) - CVD SiO_2 (310 Å) - Si rich SiO_2 (90 Å) - Al
MLO - 2F	Si - thermal SiO_2 (109 Å) - W (1×10^{14} atoms/cm^2) - CVD SiO_2 (310 Å) - Si rich SiO_2 (90 Å) - Al
MLO - 1P4	Si - thermal SiO_2 (535 Å) - Si rich SiO_2 (180 Å) - Al

Control samples without the Si rich SiO_2 layer present, but otherwise identically processed (MLO-2K, MLO-2J and MLO-1P6, respectively) were also fabricated.

The CVD SiO_2 and Si rich SiO_2 were deposited at 700°C using a concentration ratio, R_o, of N_2O to SiH_4 in the gas phase of 100 and 3, respectively [14]. For $R_o = 3$, the Si rich SiO_2 has an excess of 13% atomic Si over stoichiometric SiO_2 [14]. The resistivity of this Si rich SiO_2 film is much less than that of SiO_2 at any electric field strength [14]. Na^+ levels were shown to be $\lesssim 3 \times 10^{11}$ cm^{-2} as measured by the use of temperature bias stressing (+10 V at 200°C for 30 min, then cooled back down to room temperature under +10 V bias). All samples were stored in a nitrogen dry box when not in use.

B. Apparatus

Dark I-V measurements, done at a constant but adjustable voltage ramp rate dV_g/dt where V_g is the voltage on the gate electrode, used a Keithley #26220 logarithmic picoammeter to measure current. Point-by-point dark current as a function of gate voltage measurements were performed using the same voltage stepping unit used in photo I-V measurements, previously described [20]. The experimental apparatus to do photocurrent as a function of gate voltage (photo I-V) [5,19,20], capacitance as a function of gate voltage (C-V) [10,11], and avalanche-injection with flat-band voltage tracking [16-18] have also been described in previous publications. Photo I-V and avalanche-injection with flat-band tracking measurements were used to determine independently the trapping parameters.

III. CHARGE TRAPPING STUDIES

In this section, the SI-MIS or GI-MIS ramp I-V technique is described in detail and applied to trapping in thermal SiO_2, CVD SiO_2, and on W-related sites. In section III-A, the physics describing the occurrence of the charge trapping ledges for any site is discussed.

A. CVD SiO_2 and W Traps

Examples of charge trapping ledges in I-V characteristics obtained at a constant voltage ramp rate are shown in Figs. 3-5 for the CVD SiO_2 traps and "W" traps. Similar characteristics are seen in these figures for voltage ramp rates from −.047 V/sec to −47 V/sec. The constant displacement currents observed at gate voltages before current injection starts are equivalent to $C_1(dV_g^-/dt)$ where C_1 is the total dielectric stack capacitance.

The ledge occurs when the electric field near the injecting interface is being held approximately constant since the increase in the internal field of the trapped electron space

charge build-up nearly cancels the increase due to the voltage ramp. The electric field near the injecting interface at any time t can be shown from simple electrostatics (using Poisson's equation) [5,19] to be given by

$$E(t) = \frac{(V_g^- - \Phi_{ms} - \Psi_s) - Q_o\frac{(L-\bar{x}_o)}{\epsilon_o} - Q_n[\frac{(\ell_n-\bar{x}_n)}{\epsilon_n} + \frac{\ell_o}{\epsilon_o}]}{\ell_n + \frac{\epsilon_n}{\epsilon_o}\ell_o} \qquad (1)$$

for the case of a dual dielectric structure where the "o" and "n" subscripts refer to the layers closest to the Si substrate and Al gate electrode, respectively. In the case considered here "o" refers to the total SiO_2 layer (thermal and CVD oxides) while "n" refers to the thinner Si rich SiO_2 layer. Fig. 1 schematically shows the dual dielectric structure and the notation used in this section with the origin of coordinates at the Al–Si rich SiO_2 interface. In Equation 1, L is the total thickness of the composite structure ($L = \ell_o + \ell_n$), ℓ_o (ℓ_n) is the thickness of the SiO_2 layers of the composite structure (Si rich SiO_2 layer), Φ_{ms} is the work function difference between the metal and semiconductor electrodes, Ψ_s is the silicon surface potential, $\bar{x}_o$ ($\bar{x}_n$) is the centroid of the trapped charge distribution in the SiO_2 layer (Si rich SiO_2 layer) as measured from the Al interface with the Si rich SiO_2 layer, Q_o (Q_n) is the "bulk" trapped charge per unit area of this distribution in oxide layer (Si rich SiO_2 layer), and ϵ_o (ϵ_n) is the low frequency permittivity of SiO_2 (Si rich SiO_2).

The thin Si rich SiO_2 layers are neglected in the calculations that follow because of their low resistivity as compared to SiO_2. This is shown in Fig. 6 where the quasi-static capacitance, $C = I_{ext}/(dV_g^-/dt)$ where I_{ext} is the current measured in the external circuit, as a function of gate voltage characteristic [21] is plotted. This characteristic is observed to switch at low voltages from a value indicative of a two layer dielectric stack with dielectric constants of 3.9 and 7.5 for the SiO_2 and Si rich SiO_2 layers, respectively, to a value close to that of the SiO_2 layer alone. This figure indicates that the conductivity of the Si rich SiO_2 is much greater than that of SiO_2 as expected [14], and little voltage is dropped across this layer at the gate voltages of interest in the ramp I-V studies which will be described. However, small signal a.c. (15 mV rms) measurements from 1 MHz to 100 Hz at any negative voltage bias where the p-Si substrate is accumulated also indicate a dual dielectric stack of SiO_2 and Si rich SiO_2 with dielectric constants of 3.9 and 7.5, respectively. The dip observed in the quasi-static measurements between 0 and −1 V is due to the capacitive response of the p-Si in series with the insulator stack [21]. Therefore, in these calculations, the injection current per unit area J^- ($J^- = I^-/A$ where A is the electrode area) is limited by the SiO_2–Si rich SiO_2

interface. I^- is the particle current which is equivalent to the current measured in the external circuit minus the displacement current due to the voltage ramp; that is, $I_{ext} - C_I (dV_g^-/dt)$. The dependence of this current density on Si rich SiO_2 composition and thickness has been previously described [2]. It will be shown in this section that for the well known case of electron trapping on "W" atoms sandwiched between thermal and CVD SiO_2 layers [3-8], the centroid of the captured carriers is in excellent agreement with the actual location when the thin Si rich SiO_2 layer is ignored. As J^- becomes large enough, a particular trapping center starts to fill and

$$\frac{dQ_o(t)}{dt} = J_I^- \sigma_{c_o} N_{\infty_o}. \tag{2}$$

Here J_I^- is the current level per unit area ($J_I^- = I_I^-/A$) near the start of the ledge (see Figs. 4 and 5), σ_{c_o} is the capture cross section, and N_{∞_o} is the total number of traps per unit area. Under the approximate condition that $\frac{dE(t)}{dt} \approx 0$ when the traps start to fill and during filling, using Equation 1 and neglecting the Si rich SiO_2 layer,

$$\frac{dV_g^-}{dt} = \frac{1}{\epsilon_o}(\ell_o - \bar{x}'_o)\frac{dQ_o(t)}{dt}. \tag{3}$$

Here $\bar{x}'_o$ is the centroid distance measured from the SiO_2-Si rich SiO_2 interface where $\bar{x}'_o = \bar{x}_o - \ell_n$. Also, this equation would hold for any double dielectric system where $\frac{dQ_n}{dt} = 0$ since $L - \bar{x}_o = \ell_o - \bar{x}'_o$. Equation 3 assumes that the silicon surface potential and charge centroid in the oxide layer do not change with time. The former assumption is true for the p-Si substrates used here, because they are strongly accumulated for the negative gate bias conditions of these measurements. The latter condition will be shown to be true from the data for the cases considered here. In general, this latter condition is satisfied if the initial trapping probability ($N_{\infty_o}\sigma_{c_o}$) is $\lesssim .3$ [3-5,19]. Substituting Equation 2 into Equation 3 and solving for $N_{\infty_o}\sigma_{c_o}$ yields

$$N_{\infty_o}\sigma_{c_o} = \frac{\epsilon_o}{(\ell_o - \bar{x}'_o)}\frac{\frac{dV_g^-}{dt}}{J_I^-}. \tag{4}$$

As seen in Figs. 4 and 5, $N_{\infty_o}\sigma_{c_o}$ is independent of the voltage ramp rate $\frac{dV_g^-}{dt}$ divided by J_I^-. Therefore, the onset of the charge trapping ledge should move to larger negative gate voltages with increasing rate ramp due to the finite slope of the dark current-voltage characteristic. This is seen experimentally in Figs. 4 and 5. Integration of Equation 3 over the extent of

the current ledge (from traps unfilled to traps filled) yields

$$N_{\infty_0} = \epsilon_0 \frac{\Delta V_{g_1}^-}{q(\ell_0 - \bar{x}_0')} \tag{5}$$

where q is the charge on an electron (-1.6×10^{-19} coul) and $\Delta V_{g_1}^-$ is the voltage width of the ledge (see Figs. 4 and 5). Substituting Equation 5 into Equation 4 yields,

$$\sigma_{c_0} = \frac{q \, dV_g^-}{\frac{dt}{\Delta V_{g_1}^- J_1^-}} \tag{6}$$

Table I lists values for σ_{c_0}, N_{∞_0}, and $N_{\infty_0} \sigma_{c_0}$ determined using the technique described here and compares them to values determined using avalanche injection with flat-band voltage tracking [18] on similar MIS structures without the Si rich SiO_2 layer. As seen from this table, the agreement is very good. The values for the charge distribution centroids $\bar{x}_0'$ which are needed to find N_{∞_0} and $N_{\infty_0} \sigma_{c_0}$ were determined using a technique which will be described next.

Figures 7–10 show sequential C-V and ramp I-V measurements on the same SI-MIS structures as in Figs. 4 and 5. Before and after each ramp I-V cycle, a C-V trace is recorded starting with the as fabricated virgin sample. From the flat-band voltage shifts ΔV_{FB} obtained from the C-V characteristics and the voltage shifts ΔV_g^- obtained from the ramp I-V measurements, the trapped charge per unit area in traps located in one of the SiO_2 (thermal or CVD) layers and the centroid of this distribution can be obtained in much the same way as with the photo I-V technique [5,19,20]. The voltage shifts ΔV_{FB} and ΔV_g^- indicate the extent of trap filling at any time as reflected by the electric field in the Si substrate near the Si–SiO_2 interface and in the SiO_2 layer near the SiO_2–Si rich SiO_2 interface, respectively. ΔV_g^- is equivalent to that portion of the charge trapping ledge traversed during a ramp I-V cycle (or between cycles) and, in this case, it is always a negative number.

The C-V flat-band voltage shift, ΔV_{FB} [10,11], and the ramp I-V voltage shift, ΔV_g^- [15,19,20], can be shown from electrostatics to be

$$\Delta V_{FB} = -Q_o \left[\frac{(\bar{x}_o - \ell_n)}{\epsilon_o} + \frac{\ell_n}{\epsilon_n} \right] - \frac{\bar{x}_n Q_n}{\epsilon_n} \tag{7}$$

and

$$\Delta V_g^- = \frac{Q_o}{\epsilon_o}(L - \bar{x}_o) + Q_n \left[\frac{(\ell_n - \bar{x}_n)}{\epsilon_n} + \frac{\ell_o}{\epsilon_o} \right] \tag{8}$$

for a dual dielectric system with trapped charges Q_o and Q_n in the SiO_2 layer and Si rich SiO_2 layer, respectively, as discussed previously. Equation 8 is derived from Equation 1. ΔV_g^- is the change in gate voltage necessary to keep the electric field near the injecting interface, E(0), approximately constant as traps fill during a dark current, ramp I-V measurement. Assuming that the trapped charge state of the Si rich SiO_2 layer is not changing significantly during the ramp I-V cycle which can be verified experimentally (see Reference 2 and compare Figures 7, 9 and 11), equations 7 and 8 reduce to

$$\Delta V_{FB} = -Q_o \left(\frac{\bar{x}_o'}{\epsilon_o} + \frac{\ell_n}{\epsilon_n} \right) \tag{9}$$

$$\Delta V_g^- = \frac{Q_o}{\epsilon_o}(\ell_o - \bar{x}_o') \tag{10}$$

where the relation $\bar{x}_o = \bar{x}_o' + \ell_n$ has been used. If the low resistivity of the Si rich SiO_2 layer during current injection into SiO_2 is taken account of as was done in an earlier portion of this section by neglecting this layer, Equation 10 would still be valid. However, the Si rich SiO_2 layer can <u>not</u> be neglected during high frequency, small signal, a.c. C-V measurements as stated earlier. As seen, Equation 9 must contain a term indicating this layer's contribution to the total a.c. capacitance. From Equations 9 and 10, the total number of trapped charges per unit area N_o and centroid $\bar{x}_o'$ as measured from the SiO_2-Si rich SiO_2 interface is given by

$$\frac{\bar{x}_o'}{\ell_o} = \left(1 - \frac{\Delta V_g^-}{\Delta V_{FB}} \right)^{-1} \times \left(1 + \frac{\Delta V_g^-}{\Delta V_{FB}} \frac{\epsilon_o \ell_n}{\epsilon_n \ell_o} \right) \tag{11}$$

and

$$N_o = \frac{\epsilon_o}{q\ell_o}(\Delta V_g^- - \Delta V_{FB}) \times \left(1 + \frac{\epsilon_o}{\epsilon_n}\frac{\ell_n}{\ell_o}\right)^{-1} . \quad (12)$$

Clearly, Equations 11 and 12 reduce to the well known single dielectric results for bulk trapped charge [5,19,20], if $\ell_n \rightarrow 0$ and $\bar{x}_o' \rightarrow \bar{x}_o$. Tables II and III summarize the values of $\bar{x}_o'/\ell_o$ and N_o deduced from Equations 11 and 12 using the experimental quantities ΔV_g^- and ΔV_{FB} obtained from the data of Figs. 7 and 8 for "W" trapping and Figs. 9 and 10 for CVD oxide trapping. Values of $\bar{x}_o'/\ell_o$ determined in this manner are in good agreement with the predicted position of $\bar{x}_o'/\ell_o$ and with the value of $\bar{x}_o/\ell_o$ determined using the photo I-V technique on similar MIS samples without the Si rich SiO_2 layer present. This agreement is also summarized in Tables II and III. As seen from the tables, the centroid is not a very strong function of the amount of trapped charge. This is expected for the two cases considered here where the initial trapping probability is $\approx .3$ for a delta-function-like "W" trapping distribution and $\approx 4 \times 10^{-3}$ for approximately uniformly distributed trapping in the CVD oxide.

Trapping in the CVD oxide which is believed to be related to H_2O incorporated into the film during deposition shows another interesting phenomena. When these traps are nearly filled with electrons, a compensating positive charge appears in the film near the Si-SiO_2 interface and causes the C-V characteristic to shift to lower gate voltages. The values for N_{o_c} and N_{o_p} in the last entry in Table III showing this phenomena were calculated from ΔV_{FB} and ΔV_g^- using relationships like Equations 9 and 10 containing terms for the positive and negative charges with the centroids of each distribution assumed to be $\bar{x}'_{o_c}/\ell_o = .25$ for the electrons and $\bar{x}'_{o_p}/\ell_o = 1$ for the positive charges. The appearance of this positive charge was not dependent on the voltage ramp rate and therefore the current level (see Fig. 4). It tended to appear at electric fields of 8-9 MV/cm in the oxide films. This type of positive charge phenomena is also seen in thermal SiO_2 layers at higher currents and will be discussed later. Native thermal SiO_2 trapping sites have capture probabilities $\leq 10^{-5}$, and these traps also are thought by some researchers to be related to H_2O [3,15,16]. High temperature annealing (1000°C in N_2 for 30 min) on the CVD SiO_2 layers, lowers the trapping probability and hence moves the current ledge to higher current levels. This annealing is believed to drive off H_2O. The appearance of the positive charge at the Si–SiO_2 interface under negative gate bias voltage conditions is believed by some to be related to the diffusion of a neutral species to the Si–SiO_2 interface where it is subsequently ionized or dissociated. Weinberg has argued that excitons may cause this phenomena [22], but agrees that atomic hydrogen could produce

a similar result [23]. Atomic hydrogen released during electron capture by some of the water related sites [15], its diffusion to the Si–SiO_2 interface, and its ionization to H^+ still remains a possible explanation.

B. Thermal SiO_2 traps

Charge trapping in thermal SiO_2 layers was also investigated using the ramp I-V technique described in preceding paragraphs. Figure 11 shows sequential ramp I-V cycling through a charge trapping ledge caused by electron traps in a thermal SiO_2 layer, and Figure 12 shows the corresponding C-V characteristics. These figures also show that the formation of the positive charge at the SiO_2 interface [3,16,23,24] occurs at lower negative bulk trapped charge densities but at about the same electric field magnitudes (8-9 MV/cm). The formation of the positive space charge did not depend on the injection current level as was similarly seen for the CVD oxide case.

From Figure 11 and Equations 4, 5, and 6, the initial trapping probability, the effective capture cross section, and total number of traps per unit area can be determined for the sites which capture electrons. For $J_I^- = -3 \times 10^{-5}$ A/cm^2 and $\Delta V_{g_L}^- = -17$ V, $N_{\infty_o} \sigma_{c_o} = 1.2 \times 10^{-5}$; $\sigma_{c_o} = 8.9 \times 10^{-19}$ cm^2; and $N_{\infty_o} = 1.4 \times 10^{13}$ cm^{-2}. These results were not very sensitive to current level as was similarly seen for the CVD oxide and W trapping results. In these calculations, $\bar{x}'_{o_c}$ was set equal to $\ell_o/2$ (charge centroid is half the SiO_2 thickness) which has been shown using the photo I-V technique on MOS structures without the Si rich SiO_2 injector [3,16,23]. The results for $N_{\infty_o} \sigma_{c_o}$, σ_{c_o}, and N_{∞_o} are consistent with results reported in the literature for electron trapping sites believed to be related to H_2O [3,15,16,23]. Initial trapping probabilities are $\lesssim 10^{-5}$ with trap densities and capture cross sections dependent on processing [3,16]. In a recent paper by Young et al. using avalanche injection-flatband voltage tracking and photo I-V techniques, capture cross-sections for sites in SiO_2 films of the same thickness without the injector were determined to be $\approx 3 \times 10^{-18}$ cm^2 and 3×10^{-19} cm^2 for two traps with about the same densities [16]. This is in good agreement with the result here which would more heavily weigh the larger cross section trap. The total number of thermal SiO_2 traps per unit area determined (1.4×10^{13} cm^{-2}) on the SI-MIS structure used here was larger than the total determined by Young et al. (2.8×10^{12} cm^{-2} [16]). However, Young's structures saw a 1000°C anneal in N_2 for 30 min prior to metallization which reduces the H_2O content of the films and therefore the number of these traps.

One conclusion concerning the electric field dependence of the appearance of positive charges in CVD and thermal oxides comes from comparing the previous results. This positive charge appears at electric field magnitudes between 8-9 MV/cm in these films. The magnitude of the average field ($|V_g - \Phi_{ms} - \Psi_s|/L$) is $\approx$ 8.5 MV/cm, while the magnitude of the field near the Si-thermal SiO_2 interface is $\geq$ 9 MV/cm (which is equal to the magnitude of the average field plus the portion of the flat-band voltage shift due to the trapped electrons divided by the total oxide thickness ℓ_o). Approximately the same magnitudes of the electric fields ($\geq$ 9 MV/cm) were observed on control samples without the Si rich SiO_2 injector when positive charge started to form. However, for these controls, very little negative charging in the bulk of the CVD oxide or thermal oxide layers was observed because of the normally low injection currents from the Al-SiO_2 interface under negative voltage bias. The extent of this positive charge formation was low (much less than observed in Figs. 10 and 12), and these structures suffered destructive voltage breakdown when the formation of the positive charge began. If similar structures with CVD SiO_2 on top of thermal SiO_2 (see Table III) but no Si rich SiO_2 injector were charged using internal photoemission or avalanche injection to similar trapped electron densities, no large positive charge formation was observed. However, some small amounts of positive charge were observed particularly under internal photoemission from the Al. Here the electric field magnitudes near the Si-SiO_2 interface were $\lesssim$ 5.8 MV/cm and the average field magnitudes were $\lesssim$ 7 MV/cm because of the electron injection techniques used with the Al internal photoemission experiments having higher field magnitudes at the Si-SiO_2 interface. The overall conclusion from comparing all results is the possibility that positive charge which forms near the Si-SiO_2 interface could also be influenced, at least in part, by the high electric fields near this interface. The dependence of this positive charge on bulk CVD SiO_2 or thermal SiO_2 electron trapping, as far as the negative gate voltage ramp I-V measurements are concerned, could be due to the added contribution to the field between the edge of the trapped negative charge distribution and the Si-SiO_2 interface from this negative space charge. However, in the "W" trapping studies reported here where positive charge formation was not observed, electric field magnitudes near the Si-SiO_2 interface were also observed to be $\geq$ 9 MV/cm when these traps were filled. In addition, under avalanche injection from the substrate Si where the *electric field* at this interface is held *constant* [16,18] for a constant injection current density, positive charges were observed to build up in both CVD SiO_2 and thermal SiO_2 MOS structures which were not annealed to drive out H_2O [16], but not in the annealed structures, after negative bulk oxide charge trapping started. Thus, it appears that this positive charge formation depends on the amount of H_2O in the oxide layers, the trapping associated with it, and the local electric field near the Si-SiO_2 interface.

Weinberg et al. also saw positive charge build-up near the Si-SiO_2 interface at high electric fields using negative corona charging of the exposed SiO_2 surface [25]. They observed an electric field magnitude threshold of $\approx$ 11 MV/cm at an electron current density of 5×10^{-7} A/cm^2 for this charge build-up. They attempted to use a model dependent on hole tunneling from the Si substrate into the SiO_2 layer, but the results were not consistent with simple Fowler-Nordheim tunneling. Weinberg subsequently saw a dependence on the crystallographic Si substrate orientation [26].

The positive oxide charges near the Si-SiO_2 interfaces behaved on all samples somewhat like "slow" donor states which could be filled or discharged by tunneling electrons from or to the Si conduction band at positive and negative voltages, respectively. This behavior was also observed by Young et al. [16] on thermal SiO_2 MOS structures in which the interfacial positive charge was formed after avalanche injecting $\lesssim$ .1 coul/cm^2 of electrons under positive voltage bias conditions independent of the current level [16] (similar to the SI-MIS structures). Somewhat less than this amount of injected negative charge ($\gtrsim$ .01 coul/cm^2) was necessary in the negative gate bias ramp I-V measurements on the SI-MIS structures to start the positive charge formation (see Figs. 11 and 12). However, the SI-MIS structures have a larger number of thermal SiO_2 traps than Young's oxides [16] as was described previously. Thus, it appears that the same phenomena are occurring in both Young's experiments [16] and the ones described here on the SI-MIS structures.

IV. NUMERICAL SIMULATION

In this section, a computer simulation of the ramp I-V measurements is described and is shown to give good agreement with the experimental data for the three cases considered in section III which scan the range of trapping probabilities from 3×10^{-1} to 1.2×10^{-5}. The ramp I-V current measured in the external circuit, I_{ext}, is composed of two terms

$$I_{ext} = C_o \frac{dV_g^-}{dt} + J^-(t) \times A \qquad (13)$$

where the first term refers to the displacement current due to the ramp rate dV_g^-/dt and the capacitance of the thermal oxide layer and/or CVD SiO_2 layer, C_o, and the second term is the injected particle current per unit area. The Si rich SiO_2 layer is neglected because of its high conductivity as described in section III-A. Also, displacement current contributions due to the charge trapping [19] are ignored in Equation 13 because of the low capture probabilities of the sites studied here.

Previous experimental evidence suggests that the injected particle current is controlled by the Si rich SiO_2 interface with the SiO_2 layer [2], and that it is Fowler-Nordheim-like in nature [27,28]. Furthermore, due to the two phase (Si and SiO_2) composition of the Si rich SiO_2 layer, densely packed Si regions embedded in an SiO_2 matrix have been proposed to give electric field distortions which locally increase the field on a microscopic scale near the Si rich SiO_2 – SiO_2 interface. However, due to the microscopic nature of the distortions and their density, the trapping sites in the SiO_2 layer away from this interface "see" an approximately uniform injection in a macroscopic sense [2] over the entire electrode area, A. In general, however, the total injecting area is less than the actual electrode area. Therefore, in the simulation, the particle current per unit area, J^-, has been modeled as Fowler-Nordheim emission from a Si conduction band from the Si regions into an SiO_2 conduction band at the Si rich SiO_2 – SiO_2 interface with a field enhancement factor χ due to the field distortions caused by the two phases. J^- is given by [27]

$$J^-(t) = \frac{q^3[\chi E(t)]^2}{16\pi^2\hbar\Phi_B} \exp\left[\frac{-4(2m_e^*)^{1/2}\Phi_B^{3/2}}{3\hbar\chi|qE(t)|}\right] \tag{14}$$

where $\hbar$ is Planck's constant divided by 2π, Φ_B is the barrier height from the Si conduction band to the SiO_2 conduction band (3.1 eV was used [3], with no corrections for image-force barrier lowering which would be small), and m_e^* is the effective mass of a tunneling electron (.5 of the free electron mass was used [27,28]). Corrections for temperature dependence which would be small [27] were also not included in Equation 14. This field enhancement near the Si rich SiO_2 – SiO_2 interface decreases rapidly in the direction away from this interface into the SiO_2 bulk where charge trapping is occurring [29]. The electric field without the field enhancement, E(t), near the Si rich SiO_2 – SiO_2 interface can be derived from Equation 1 by again neglecting the Si rich SiO_2 layer because of its high conductivity assuming $Q_n \to 0$, $\ell_n \to 0$, and $\epsilon_n \to \epsilon_0$. With these assumptions, Equation 1 reduces to

$$E(t) = \frac{(V_g^-(t)-\Phi_{ms}-\Psi_s)}{\ell_0} - \frac{Q_0(t)}{\epsilon_0}\frac{(\ell_0-\bar{x}_0)}{\ell_0} \tag{15}$$

Finally, the build-up of trapped charge on any sites either normally present or purposely introduced in an SiO_2 layer can be described from first order kinetics for trapping probabilities less than unity by [3]

$$\frac{dQ_0(t)}{dt} = \frac{J^-(t)}{q}\sigma_{c_0}[qN_{x_0}-Q_0(t)]. \tag{16}$$

This equation reduces to Equation 2 for the case where the traps are nearly empty ($N_{x_0} >> Q_0(t)/q$) near the start of the charge trapping ledge as discussed in section III-A.

Equation 16 also assumes that internal fields due to the trapped charge itself and the applied voltage are not large enough to cause significant trap emptying by field ionization (tunneling), particularly in the region of the charge distribution closest to the Si – SiO_2 interface where electric fields would be highest ($\geq$ 9 MV/cm when $\approx 10^{13}$ traps/cm^2 are filled) in the SI-MIS ramp I-V experiments described here. For the energetically deep "W" and SiO_2 sites ($\gtrsim$ 5 eV from the bottom of the SiO_2 conduction band edge [3,30]) considered here, electron tunneling out of these traps should not be very probable even at fields as high as 10 MV/cm (tunneling distances are $\geq$ 50 Å). This is consistent with detrapping rates which were deduced from experimentally measured flat-band voltage shifts. After filling of the "W" or CVD SiO_2 traps, the samples were stressed at high positive voltages where no appreciable current injection from the Si – SiO_2 interface occurs but where electric field magnitudes are > 7 MV/cm over the part of the trapped charge distribution closest to the Si rich SiO_2 – SiO_2 interface. These detrapping rates were slow compared to the trap filling rates of the SI-MIS ramp I-V experiments. In Figs. 4 and 5, the invariance of the voltage width of the trapping ledge, $\Delta V_{g_1}^-$, (which is proportional to the total number of filled traps per unit area) over three orders of magnitude in current but only slightly different gate voltages, also shows that the detrapping rate due to field ionization of trapped electrons is negligible.

Equation 16 also assumes that σ_{c_0} is spatially constant [3] which would not be rigorously true if carrier heating and/or field ionization from excited states is occurring near the edge of the trapped charge distribution closest to the Si – SiO_2 interface in the SI-MIS ramp I-V experiments. However, if these effects are very significant, the charge centroid position should decrease (move closer to the Si rich SiO_2 – SiO_2 interface) with increasing amounts of trapped charge. This was not observed experimentally, at least for the "W" and CVD SiO_2 traps (see Tables II and III).

Equations 13–16 uniquely define the current measured in the external circuit as a function of ramped gate voltage. They form a non-linear system that must be solved numerically. It was found that the well known Runge-Kutta method of integration gave excellent results if the initial condition Q_0 (0) = 0 was replaced by the analytic behavior (A.12), as described in the Appendix. In addition, a mesh size of the order of one-tenth of the voltage range during which the current first rises steeply gave accurate results. This voltage difference is directly proportional to $\tau_2 - \tau_1$ of the Appendix [cf. Eqs. (A.11), (A.13), and (A.15)].

Equations 4 and 5 for the current at the ledge and the extent of the ledge are dimensional equivalents of Eqs. (A.14) and (A.17). All these considerations are embodied in a simple interactive APL program that first calls for experimental conditions, and then automatically calculates the turning points, the mesh size and useful voltage range, and finally computes the current, field, and trapped charge as a function of gate voltage.

Figures 13 and 14 show the solutions of the equations and plots $N_o - V_g$, $|E| - V_g$, and $|I_{ext}| - V_g$ characteristics for the case of electron trapping on W related sites embedded in an oxide layer. Figures 15 and 16 show the numerical simulation of $|I_{ext}| - V_g$ for the case of electron trapping on CVD SiO_2 and thermal SiO_2 sites. The open circles in Figs. 13, 15 and 16 are the experimental data from the ramp I-V measurements on SI-MIS structures MLO-2F, MLO-2D, and MLO-1P4, respectively. The values of N_{∞_o},σ_{c_o}, $\bar{x}_o$ used in the computer simulations were taken from Tables I, II and III and section III-B. The voltage ramp rate used was $-.47$ V/sec, and $\Phi_{ms} + \Psi_s$ was set equal to -1 V. The value of χ used was determined from the ratio of the voltages at constant current after the onset of particle current injection of the sample with no injector to the sample with the Si rich SiO_2 injector using the data of Figs 2 and 3. As can be seen in the simulation (Fig. 14), the traps start to fill near the start of the current ledge and the electric field remains approximately constant over the extent of the ledge until the traps are filled. These general results were also seen for simulations of CVD SiO_2 and thermal SiO_2 trapping. This verifies the assumptions concerning the onset of trapping and $dE/dt \approx 0$ used in section III-A to obtain Equations 4-6 from which charge trapping parameters were determined. As can be seen from Figs. 13, 15, and 16, the simulation is in good agreement with the experimental data for all the cases considered here, particularly in the first current rise and ledge regions.

V. CONCLUSIONS

The techniques discussed are clearly made possible by the property of the thin Si rich SiO_2 layer: high current injection at moderate average electric fields into the SiO_2 layers. Similar techniques to study charge trapping could be used with an MOS capacitor [9]. However, to get similar magnitudes of current in these MOS structures without a Si rich SiO_2 injecting layer requires very high average electric fields (see Figs. 2 and 3) which could field-ionize trapped charges as soon as they are captured and/or reduce significantly the charge carrier capture rate [3]. Also voltage breakdown of the MOS structures due, for example, to weak spots is much more probable at the higher average fields.

These techniques using the SI-MIS structures are very advantageous in terms of speed as compared to conventional avalanche injection with flat-band voltage tracking to determine σ_{c_o} and N_{x_o} and photo I-V to determine $\bar{x}_o$ and N_o. However, the conventional techniques, although more tedious, are probably more accurate particularly in separating trapping sites with comparable capture probabilities as shown for thermal SiO_2. Ramp I-V and C-V measurements on SI-MIS structures are very practical when large amounts of data on many samples are required for trapping centers in SiO_2 either normally present, purposely introduced, or introduced inadvertently during processing.

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APPENDIX: Analytic approximations

For a constant ramp rate r, the gate voltage is $V_g^- = -rt$, and Eqs. (13-16) read

$$-I_{ext}/A = c - J^-, \tag{A.1}$$

$$-J^- = aE^2 \exp(-b/|E|), \tag{A.2}$$

$$E = -dt' + eN_o, \tag{A.3}$$

$$\frac{dN_o}{dt'} = f(-J^-)(N_{\infty_o} - N_o). \tag{A.4}$$

Here, t' stands for the shifted time variable $t - t_o$, where $t_o = -(\Phi_{ms} + \Psi_s)/r$, and N_o is the trapped charge at time t ($N_o = Q_o/q$). It is assumed that initial current injection due to the Si surface potential and work function differences between the Si and Al contacts is negligible, so that N_o, E, and therefore J^- are effectively zero for $t \leq t_o$. The constants a.....f (all positive) are obtained by comparing Eqs. (13-16) and (A.1-4). Thus

$$\left.\begin{aligned} a &= |q|^3\chi^2/16\pi^2\hbar\Phi_B, \quad b = 4(2m_c^*)^{1/2}\Phi_B^{3/2}/3\hbar|q|\chi, \\ c &= \varepsilon_o r/\ell_o, \quad d = r/\ell_o, \quad e = (|q|/\varepsilon_o)(1-\bar{x}_o/\ell_o), \\ f &= \sigma_{c_o}/|q|. \end{aligned}\right\} \tag{A.5}$$

The discussion is simpler if one transforms these equations to a dimensionless form. Introducing reduced field, charge, current, and time

$$\left.\begin{aligned} \mathscr{E} &= E/b, \quad u = -\ln[(N_{\infty_o} - N_o)/N_{\infty_o}], \\ j &= -J^-/c, \quad \tau = t'd/b, \end{aligned}\right\} \tag{A.6}$$

one gets the convenient form

$$-I_{ext}/Ac = 1 + j, \tag{A.7}$$

$$j = \alpha\mathscr{E}^2 \exp(-|\mathscr{E}|^{-1}), \tag{A.8}$$

$$\mathcal{E} = -\tau + \beta(1 - \exp(-u)), \tag{A.9}$$

$$\frac{du}{d\tau} = \gamma j, \quad u(0) = 0. \tag{A.10}$$

In these equations, $\alpha = ab^2/c$ depends only on fundamental constants and the ramp rate, $\beta = eN_{x_0}/b$, and $\gamma = b\varepsilon_0 f$. Note that the Fowler-Nordheim current has been normalized to the capacitive current c, that the product $\beta\gamma = N_{x_0}\sigma_{c_0}(1 - \bar{x}_0/\ell_0)$ gives the value of $N_{x_0}\sigma_{c_0}$, and that the time-like variable τ is proportional to V_g^-; thus,

$$V_g^- = -b\ell_0\tau + (\Phi_{ms} + \Psi_s). \tag{A.11}$$

The essential singularity of the Fowler-Nordheim current (A.8) precludes straightforward numerical integration. Therefore one must first find the initial behavior around $\tau = 0$ by Picard iteration. This will also yield useful analytic results. The initial condition suggests the first iterate $u_1 = 0$, and Eqs. (A.9) and (A.8) then give $\mathcal{E}_1 = -\tau$ and

$$j_1 = \alpha\tau^2 \exp(-\tau^{-1}). \tag{A.12}$$

Insertion of expression (A.12) into (A.10) allows the computation of the second iterate u_2 in terms of exponential integrals, and the process can then be repeated. However, the above results are sufficient. For example, the first turning point τ_1, at which the current first rises rapidly is given by $j(\tau_1) \cong j_1(\tau_1) \cong 1$. This states nothing more than the equality of the capacitive and Fowler-Nordheim currents. Using Eq. (A.12) and taking logarithms, one easily sees that

$$\tau_1 \cong (\ln \alpha - 2 \ln \ln \alpha)^{-1}, \tag{A.13}$$

for large values of α, as is the case here.

The behavior for intermediate values of time is also readily available. As the space charge builds up, it creates a field opposed to that generated by the driving gate voltage. One expects the $\mathcal{E}(\tau)$ and therefore the $j(\tau)$ curves to flatten. The time (voltage) τ_2 for this occurrence is given approximately by the condition $d\mathcal{E}/d\tau \cong 0$ (see also the discussion of section III). Differentiating Eq. (A.9), using (A.10), and remembering that $N_0 << N_{x_0}$ in that range, one gets

$$j(\tau_2) \cong (\beta\gamma)^{-1}. \tag{A.14}$$

If one approximates j by the first Fowler-Nordheim current j_1 [cf. Eq. (A.12)], then the current ledge begins when

$$\tau = \tau_2 \cong \left(\ln (\alpha\beta\gamma) - 2 \ln \ln (\alpha\beta\gamma) \right)^{-1}. \tag{A.15}$$

Note that $N_0/N_{\infty_0} \cong \tau/\beta +$ const. in the neighborhood of τ_2 as Eqs. (A.10) and (A.14) easily show.

Finally, the extent of the ledge is readily estimated, because this ledge terminates when all traps are filled. The condition $N_0 \cong N_{\infty_0}$ implies $u \to \infty$ and $\varepsilon \to -\tau + \beta$. Therefore the current (A.8) becomes

$$j \sim \alpha (-\tau + \beta)^2 \exp (-|-\tau + \beta|^{-1}). \tag{A.16}$$

This is nothing more than another Fowler-Nordheim current, parallel to j_1 and displaced by an amount β on the $\tau-$ scale. Thus the current (A.16) increases rapidly for

$$\tau > \tau_3 = \tau_2 + \beta. \tag{A.17}$$

The estimates for τ_1, τ_2, and τ_3 are essential for the successful implementation of any integration scheme. Furthermore, the above results allow immediate computation of the physical quantities σ_{c_0} and $N_{\infty_0} (1 - \bar{x}_0/\ell_0)$. This is illustrated in section IV of the text.

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Table I

"W" – Trapping Parameters

Technique	$N_{\infty_0}\ \sigma_{c_0}$	$N_{\infty_0}(cm^{-2})$	$\sigma_{c_0}(cm^2)$
SI-MIS			
Ramp I-V	3.0×10^{-1}	1.1×10^{13}	2.7×10^{-14}
MIS[a,b]	3.1×10^{-1}	1.1×10^{13}	2.7×10^{-14}

CVD Oxide – Trapping Parameters

Technique	$N_{\infty_0}\ \sigma_{c_0}$	$N_{\infty_0}(cm^{-2})$	$\sigma_{c_0}(cm^2)$
SI-MIS			
Ramp I-V	4.1×10^{-3}	1.1×10^{13}	3.6×10^{-16}
MIS[b]	3.4×10^{-3}	1.2×10^{13}	2.9×10^{-16}

a Taken from Table I of Reference 12 with correction for charge centroid position.

b MIS structures were used with avalanche injection and flatband voltage tracking techniques. Centroids were determined using the photo I-V technique.

Table II

"W" – Number of Trapped Charges
and Centroid Location

Ramp I-V Cycle	ΔV_g^-(V)	ΔV_{FB}(V)	$\bar{x}_o'/\ell_o$	N_o(cm^{-2})
3rd – 2nd	−2.5	7	.71	4.4×10^{12}
4th – 2nd	−4	11.2	.71	7.1×10^{12}
4th – 3rd	−1.5	4.3	.71	2.7×10^{12}

a) $\bar{x}_o'/\ell_o$ calculated $= \frac{310\ \text{Å}}{419\ \text{Å}} = .74$

b) $\bar{x}_o/\ell_o$ using photo I-V = calculated values knowing thickness of layers (see References 18 and 19).

Table III

CVD Oxide – Number of Trapped Charges and Centroid Location

Ramp I-V Cycle	ΔV_g^-(V)	ΔV_{FB}(V)	$\bar{x}_{o_e}'/\ell_o$	$N_{o_e}(cm^{-2})$	$N_{o_p}(cm^{-2})$
2nd – 1st	−3.5	+1.4	.21	2.3×10^{12}	0
3rd – 1st	−9.5	+4.25	.23	6.4×10^{12}	0
3rd – 2nd	−6	+2.85	.25	4.1×10^{12}	0
4th – 1st	−14	−.75	.25 (Assumed)	9.5×10^{12}	3.3×10^{12}

$\bar{x}_{o_e}'$ = centroid of trapped electron distribution; $\bar{x}_{o_e}'/\ell_{o_{CVD}}$ range

$$= \frac{(.21 \rightarrow .25) \times 419\ \text{Å}}{310\ \text{Å}} = .28 \rightarrow .34$$

N_{o_e} = number of trapped electrons per unit area

$\bar{x}_{o_p}'$ = ℓ_o = centroid of trapped positive charge distribution (assumed)

N_{o_p} = number of trapped positive charges per unit area

a) $\bar{x}_{o_e}'/\ell_o$ calculated assuming uniform distribution in CVD oxide = $\dfrac{\frac{310\text{Å}}{2}}{419\text{Å}} = .37$

b) $\bar{x}_{o_e}/\ell_{o_{CVD}}$ range using photo I-V = .16 → .31.

$\bar{x}_{o_p}$ using photo I-V = ℓ_o

$\bar{x}_{o_e}$ and $\bar{x}_{o_p}$ were determined using photo I-V sensing and internal photoemission charging from Al with 4.5 eV light and with V_g^- ranging from −7 to−35 V on a set of samples (.1 Ωcm p Si – 300 Å thermal SiO_2 – 350 Å CVD SiO_2 – 135 Å Al) equivalent to SI-MIS structures in Table III except for the injector. $\bar{x}_{o_e}/\ell_{o_{CVD}}$ shows a range of values for different amounts of trapped electrons similar to the densities in Table III. However, charging by avalanche injection from the Si substrate did move the centroid of the negative charge distribution closer to the center of the CVD oxide film. The trapped electron distribution

increases near CVD oxide interfaces with other materials. No large accumulation of positive charge was observed at the $Si\text{-}SiO_2$ interface under avalanche-injection charging out to $\Delta V_{FB} \approx 16$ V; however, some was observed particularly under internal photoemission charging at -28 to -35 V.

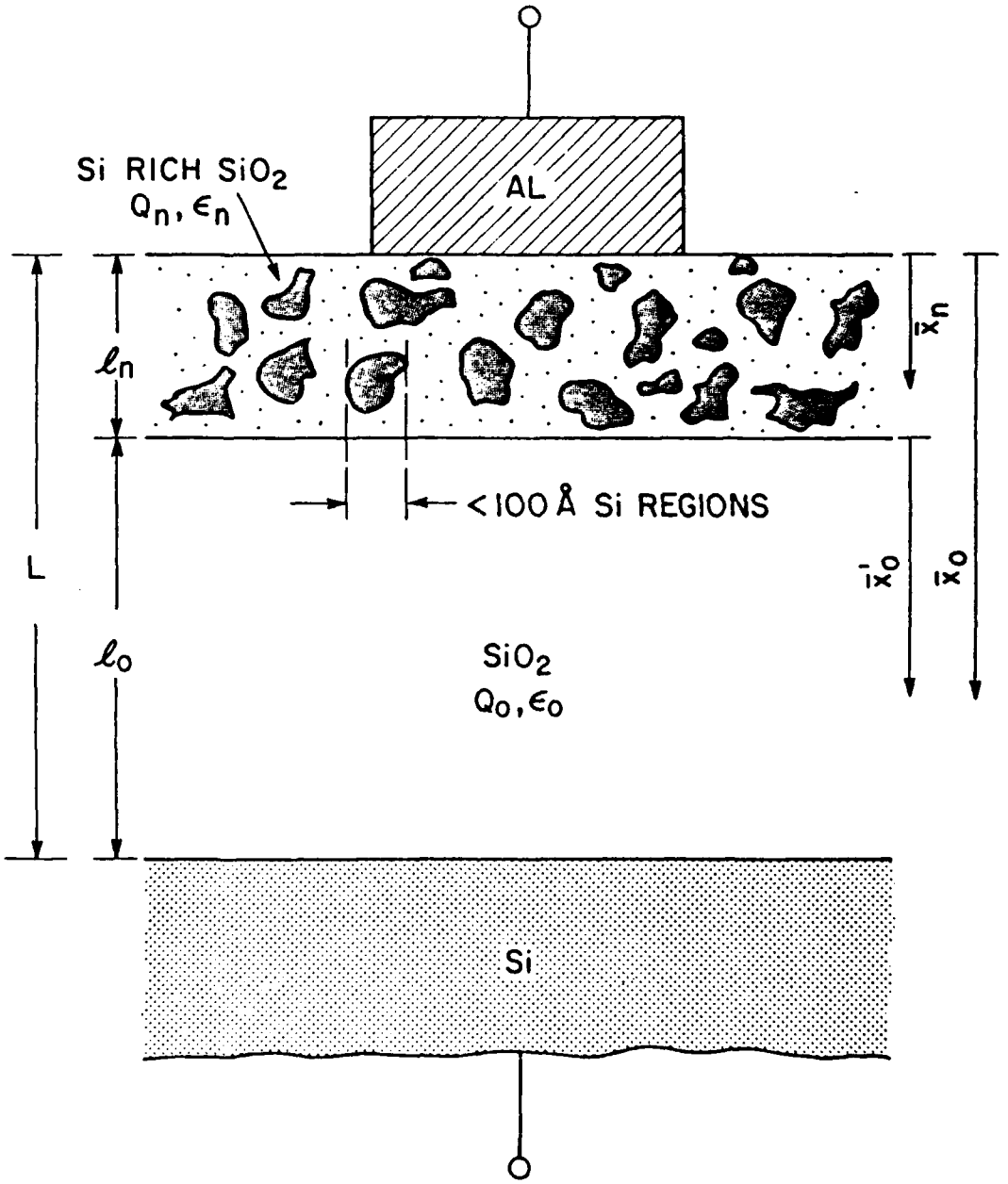

Fig. 1. Schematic illustration of proposed two phase model of the Si rich SiO_2 injector incorporated into a SI-MIS capacitor. Notation is defined in the text.

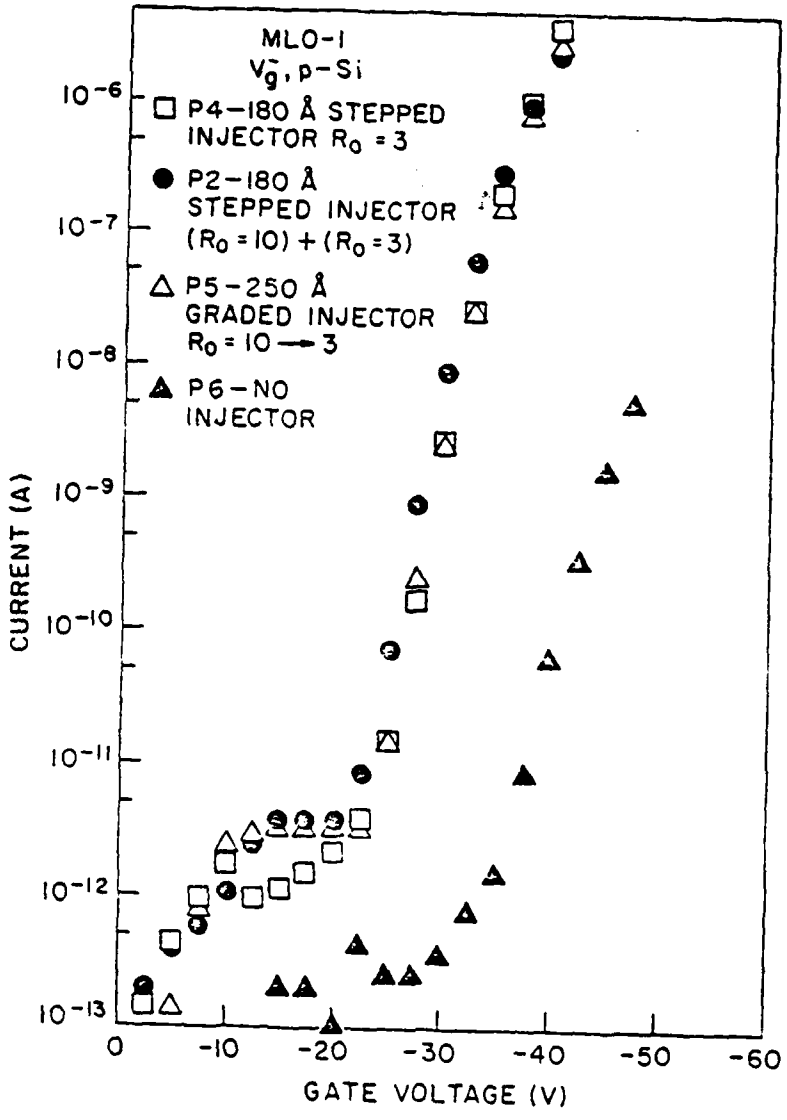

Fig. 2. Point by point magnitude of the dark current as a function of negative gate voltage on various GI-MIS and SI-MIS structures. In this measurement, the gate voltage was stepped by −2.5 V starting from 0 V every 20 sec with the dark current being measured 18 sec after each voltage step increase. The Si rich SiO_2 layer was either stepped or graded with R_o defined as $[N_2O]/[SiH_4]$ as an indicator of the Si content of this layer. R_o from 10 (40% atomic Si) to 3 (46% atomic Si) was used with Si content increasing towards the top metal gate electrode when several layers were stacked on top of the underlying 550 Å thick thermal SiO_2 layer (R_o = 10 + 3) or when a graded layer was used (R_o = 10 → 3). The current ledge observed at low voltages is due to trapped space charge build-up in the Si rich SiO_2 injector layer which tends to hold off further current injection until a certain voltage is reached [2].

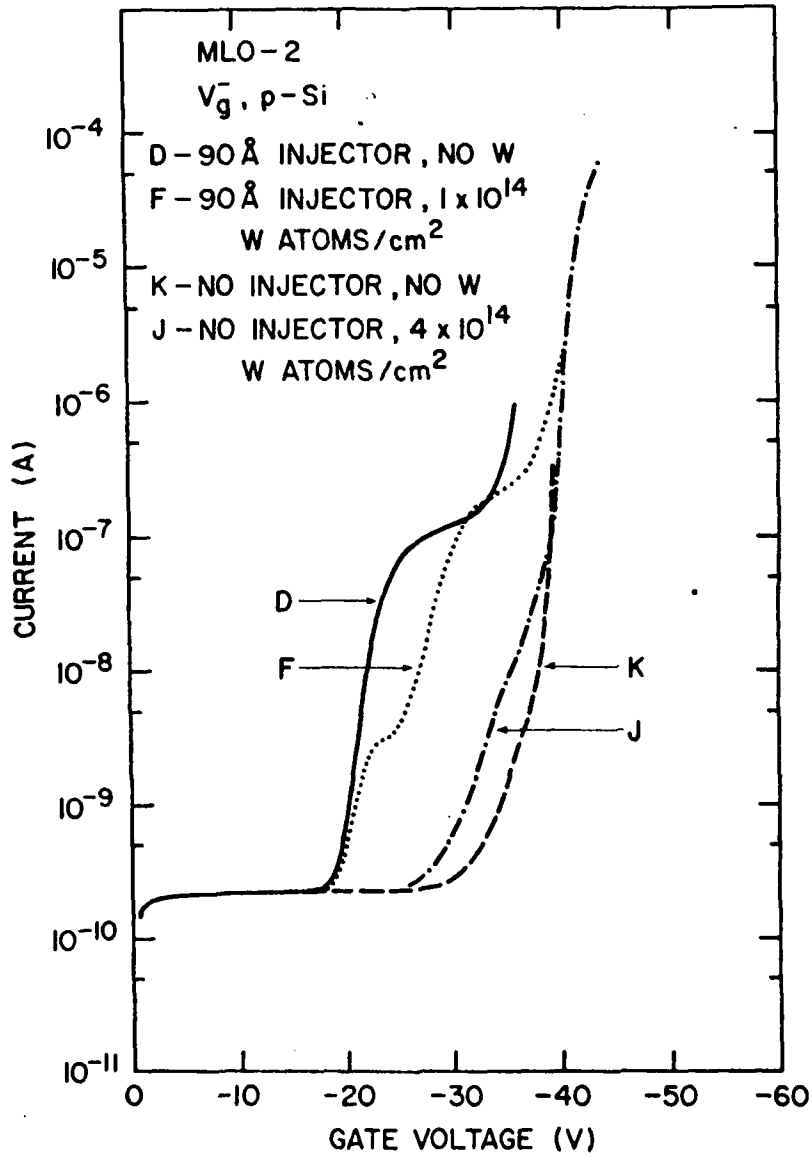

Fig. 3. Magnitude of the dark current as a function of negative ramped (−.47 V/sec) gate voltage on several SI-MIS structures and their control MIS structures which do not have the Si rich SiO_2 injecting layer present.

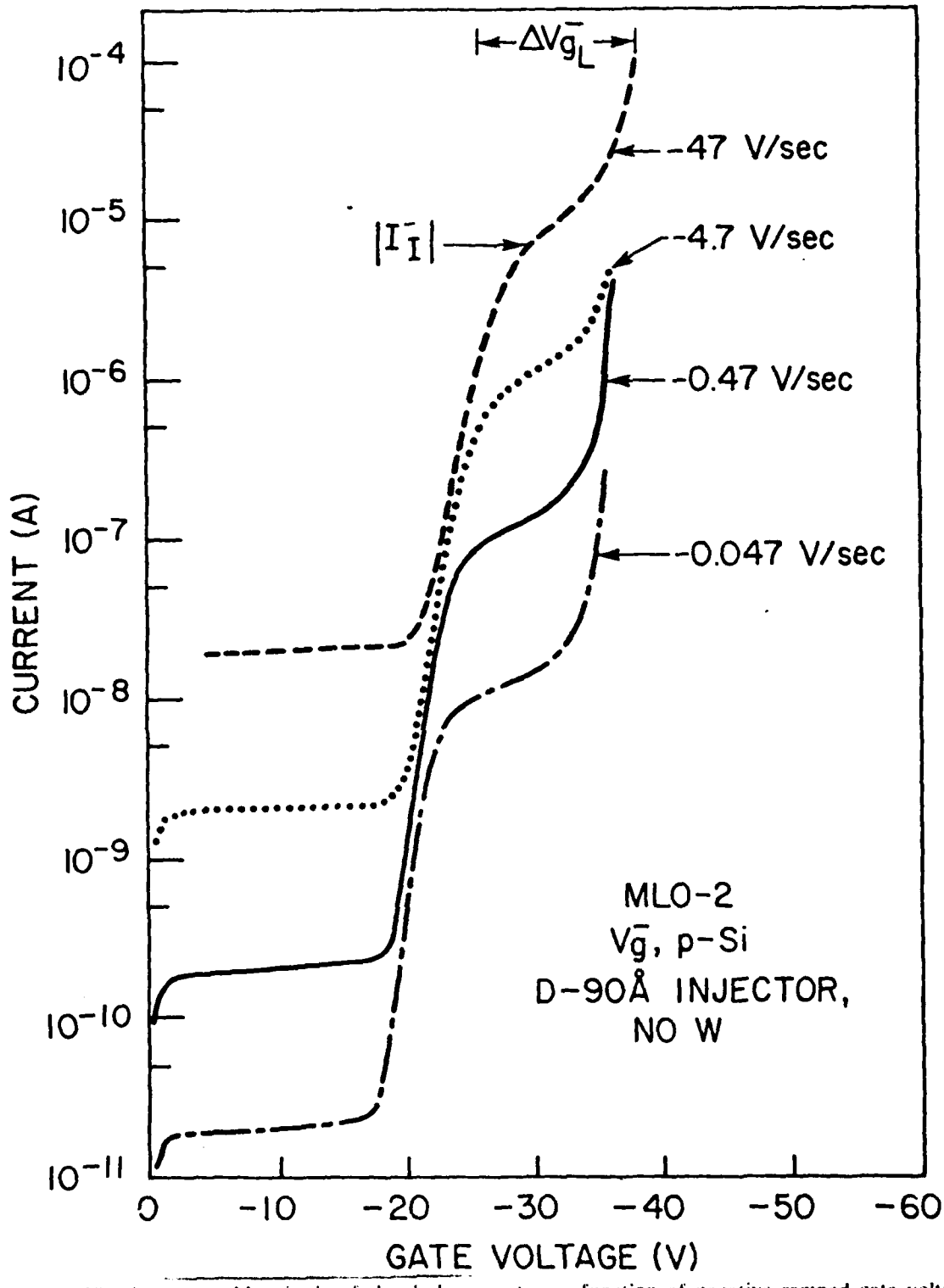

Fig. 4. Magnitude of the dark current as a function of negative ramped gate voltage on a SI-MIS structure with a CVD SiO_2 layer deposited on thermal SiO_2 (MLO-2D) for various voltage ramp rates. A virgin as-fabricated location was used for each ramp rate.

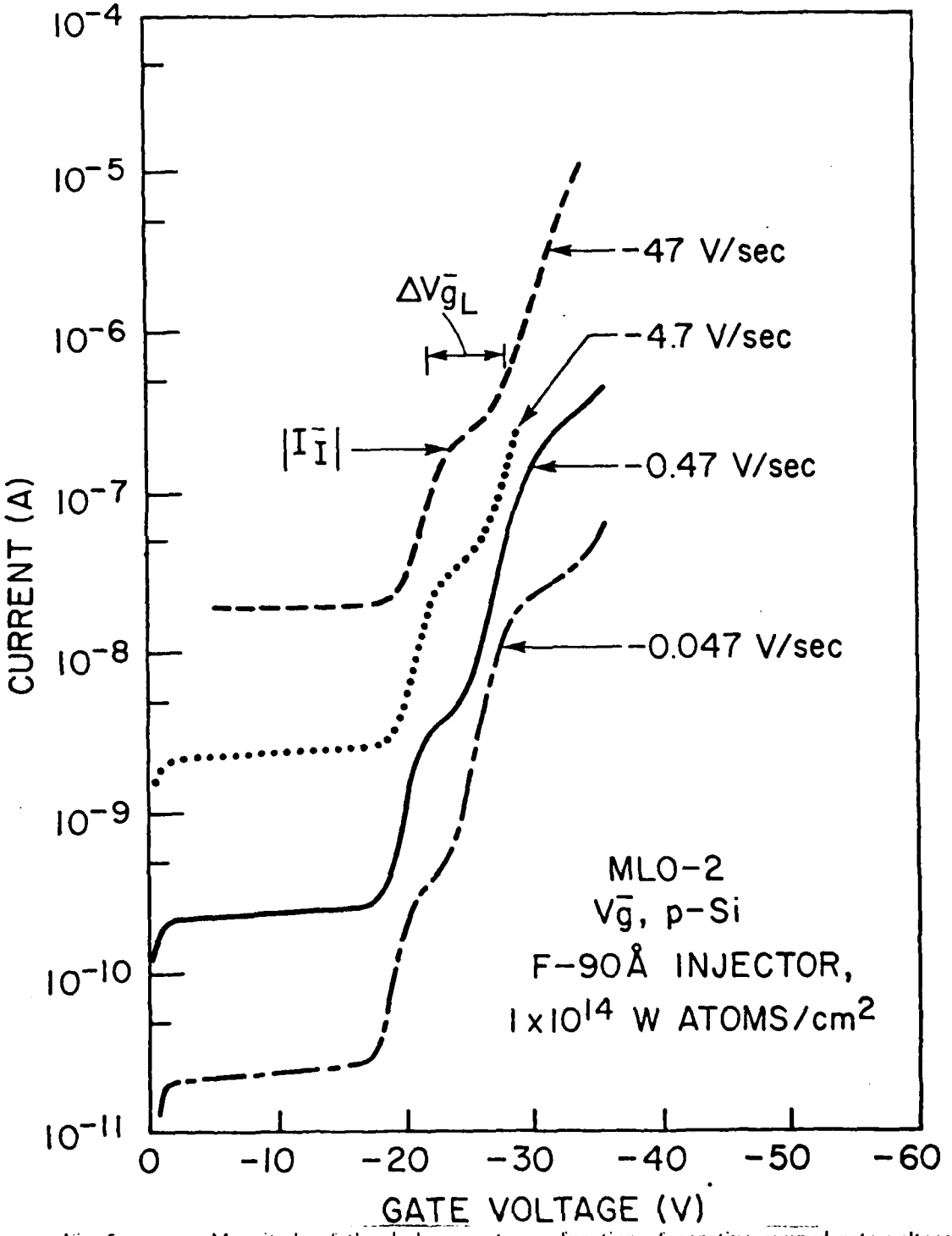

Fig. 5. Magnitude of the dark current as a function of negative ramped gate voltage on a SI-MIS structure equivalent to that in Fig. 4 except for the presence of a W trapping layer (MLO-2F) for various voltage ramp rates. A virgin as-fabricated location was used for each ramp rate.

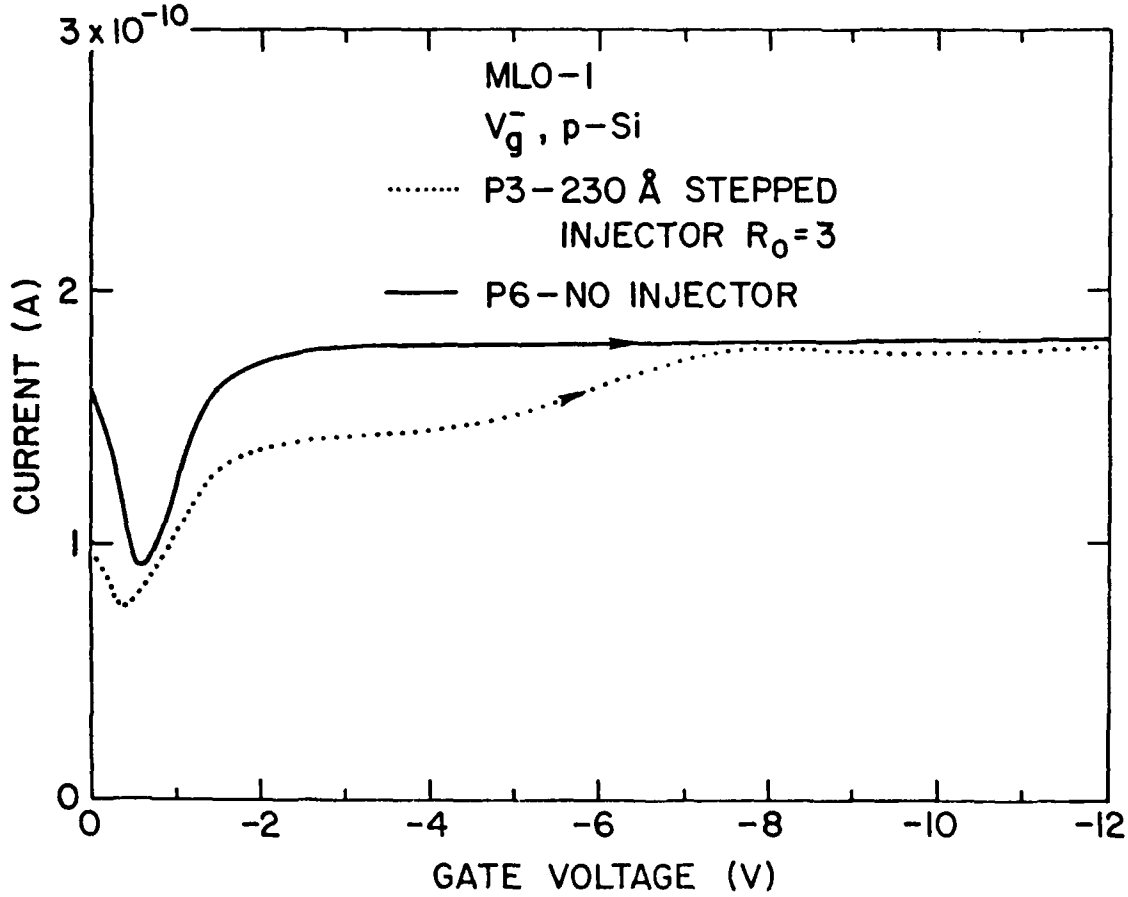

Fig. 6. Quasi-static capacitance ($C = I_{ext}/(dV_g^-/dt)$) as a function of gate voltage on a SI-MIS structure with 230 Å of Si rich SiO_2 ($R_o = 3$) deposited on 534 Å of thermal SiO_2 (MLO-1P3) compared to a control MIS sample with no Si rich SiO_2 layer present (MLO-1P6).

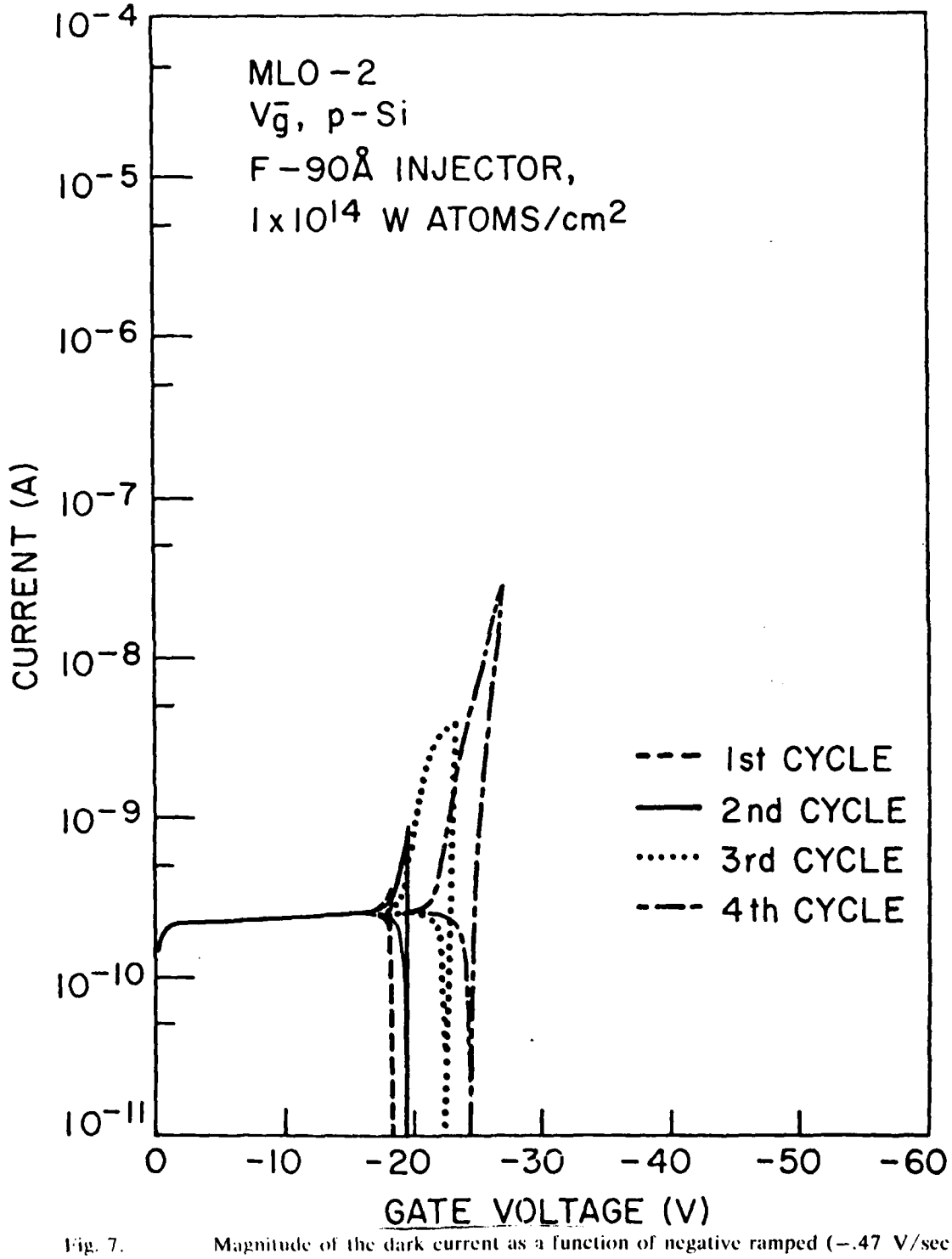

Fig. 7. Magnitude of the dark current as a function of negative ramped (−.47 V/sec) gate voltage on one SI-MIS structure equivalent to those in Fig. 5 which was cycled four times to consecutively higher voltages through the W trapping ledge. On the return portion of the trace (.47 V/sec), the displacement current $C_I dV_g^-/dt$ changes sign.

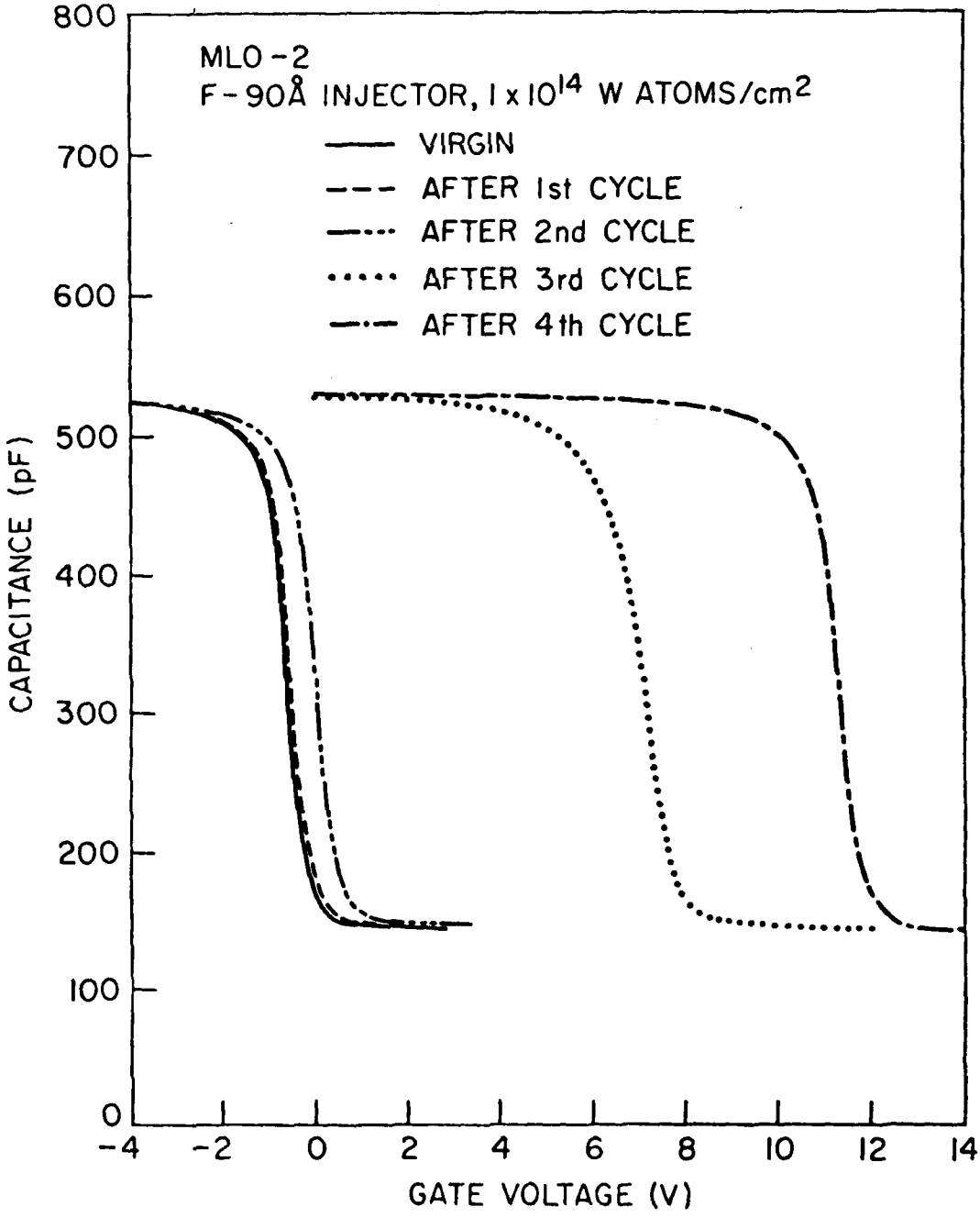

Fig. 8. High frequency (1 MHz) capacitance as a function of gate voltage on the same sample as in Fig. 7 before cycling (virgin) and after each cycle shown in Fig. 7.

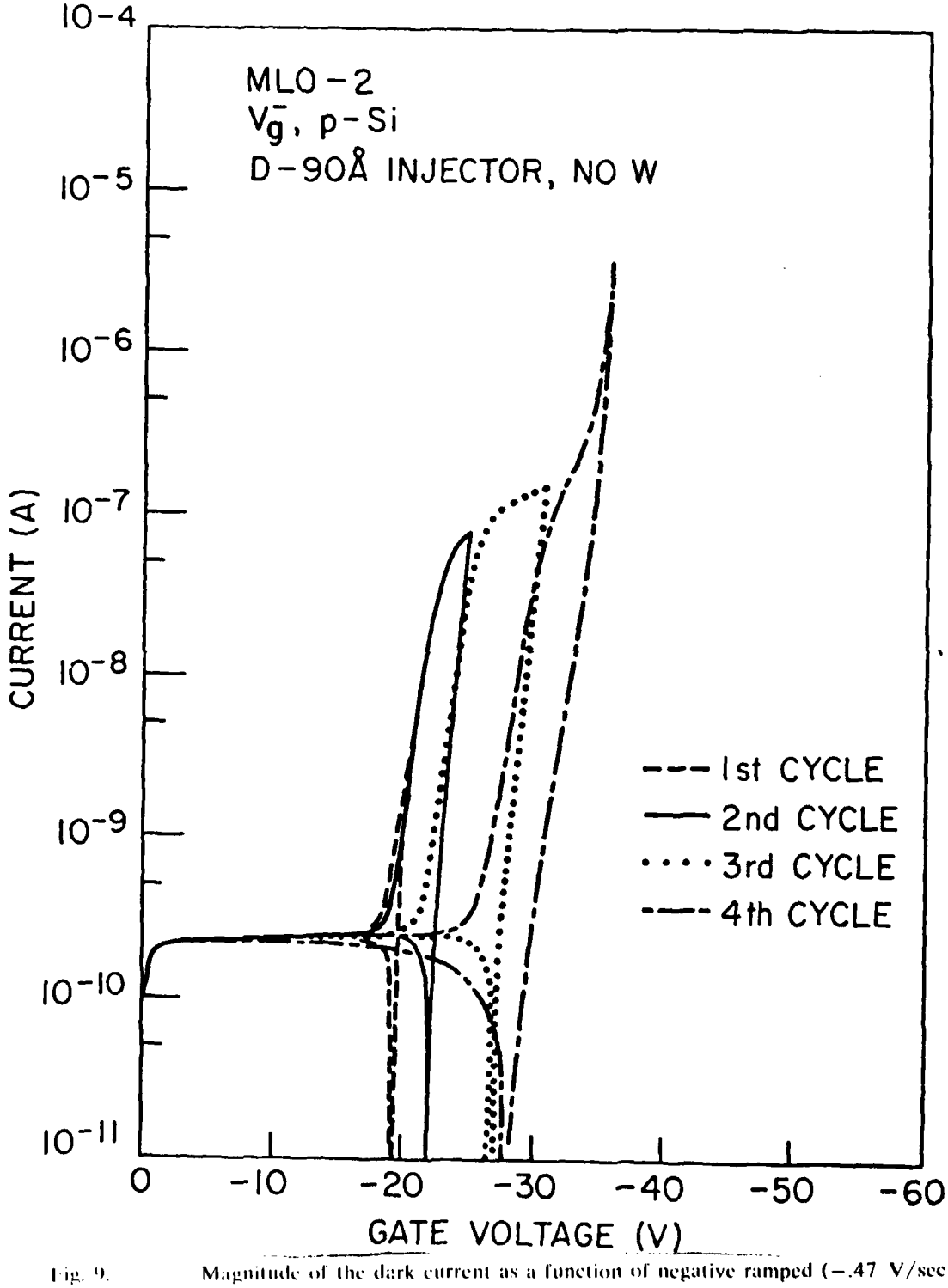

Fig. 9. Magnitude of the dark current as a function of negative ramped (−.47 V/sec) gate voltage on one SI-MIS structure equivalent to those in Fig. 4 which was cycled four times to consecutively higher voltages through the CVD oxide trapping ledge. On the return portion of the trace (.47 V/sec), the displacement current $C_i dV_g^-/dt$ changes sign.

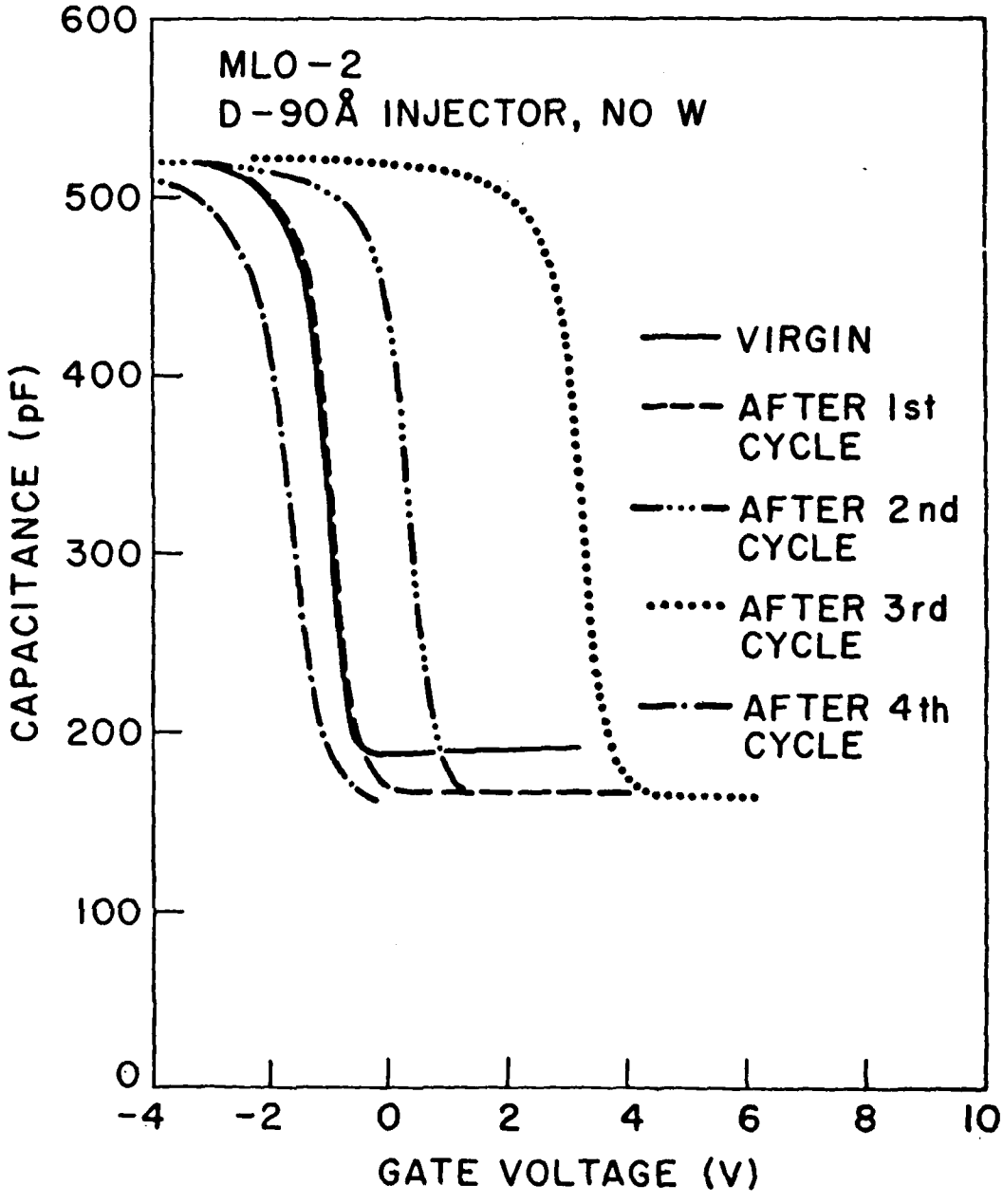

Fig. 10. High frequency (1MHz) capacitance as a function of gate voltage on the same sample as in Fig. 9 before cycling (virgin) and after each cycle shown in Fig. 9.

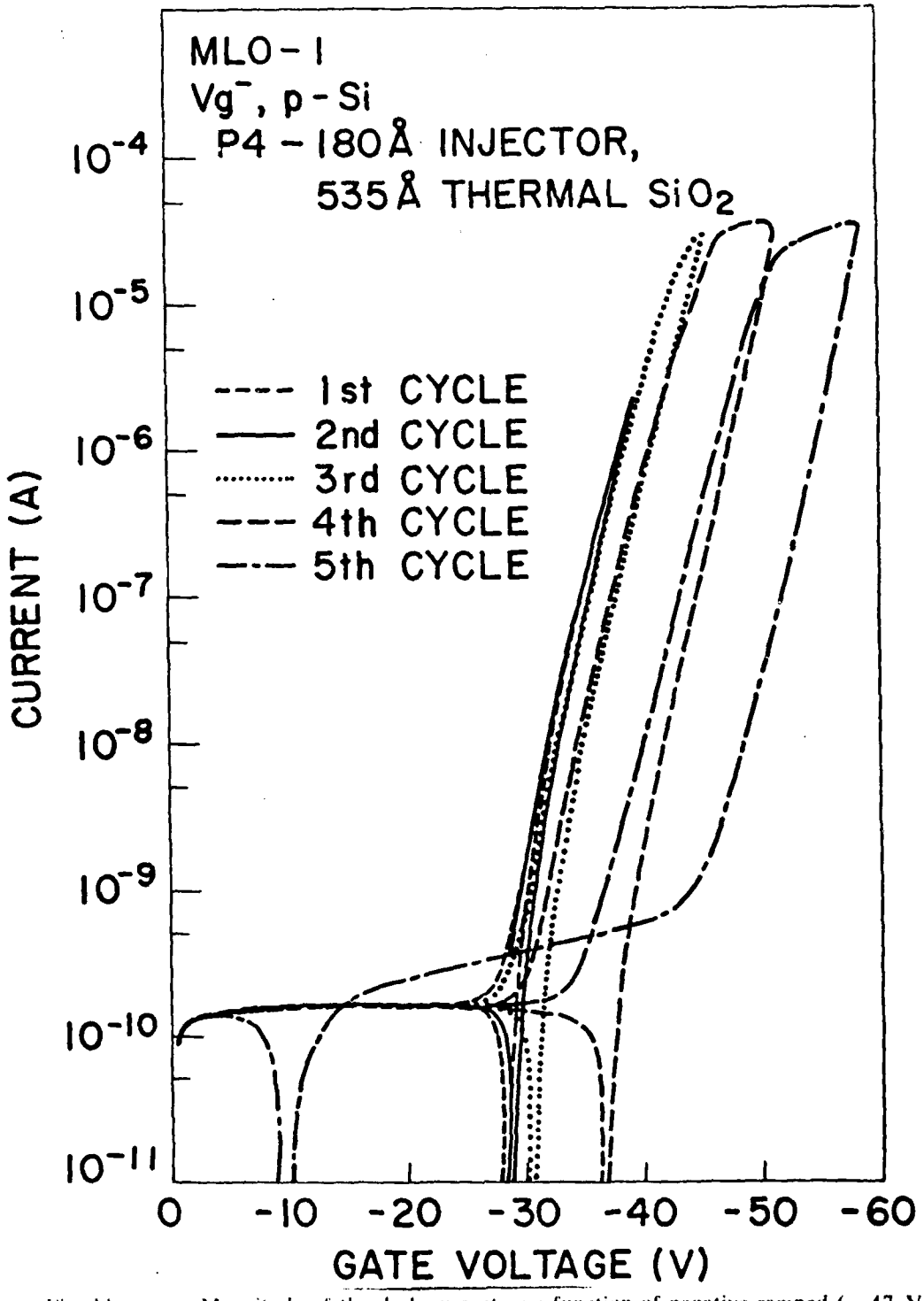

Fig. 11. Magnitude of the dark current as a function of negative ramped (−.47 V/sec) gate voltage on one SI-MIS structure with only a thermal SiO_2 layer (MLO-1P4) which was cycled five times to consecutively higher voltages through the thermal oxide trapping ledge. On the return portion of the trace (.47 V/sec), the displacement current $C_I dV_g^-/dt$ changes sign.

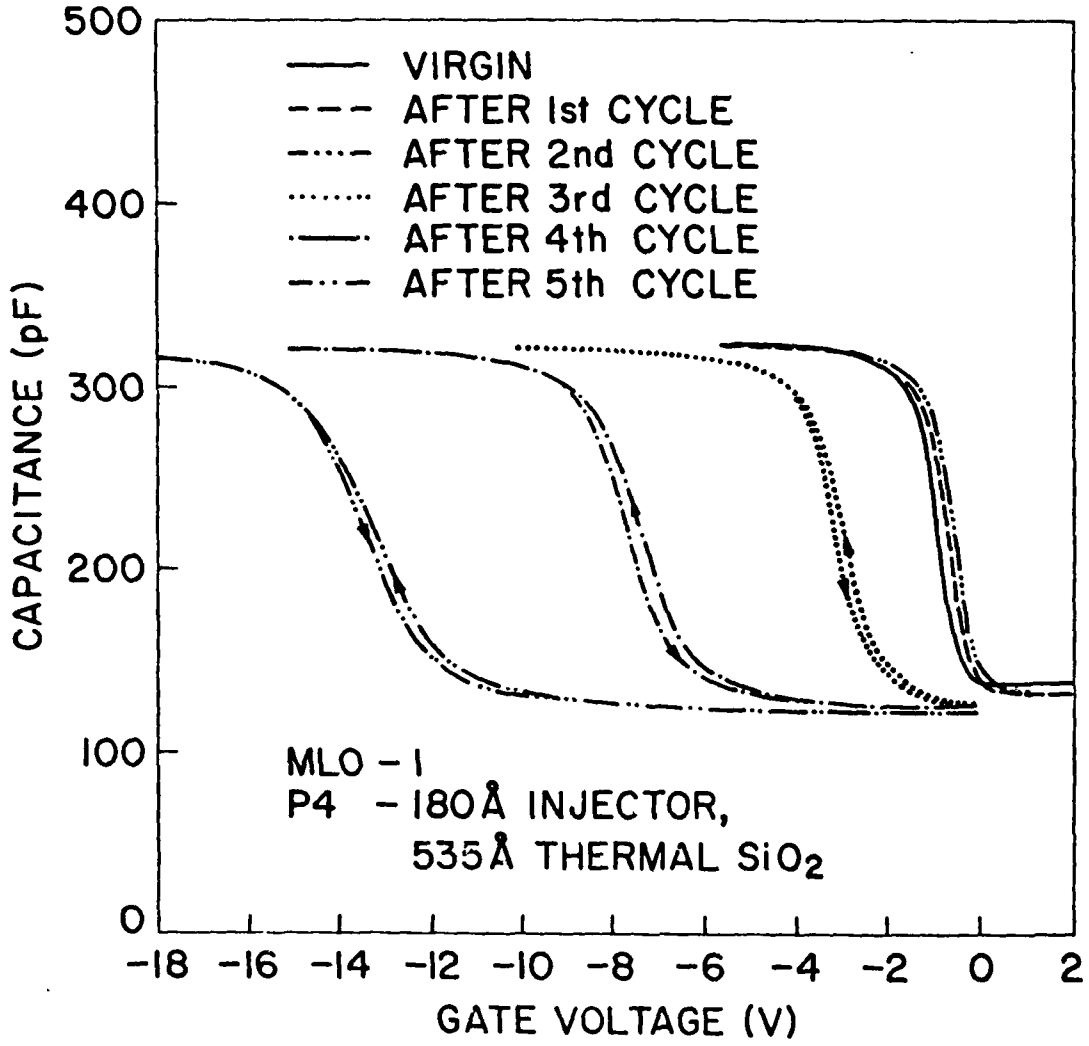

Fig. 12. High frequency (1 MHz) capacitance as a function of gate voltage on the same sample as in Fig. 11 before cycling (virgin) and after each cycle shown in Fig. 11.

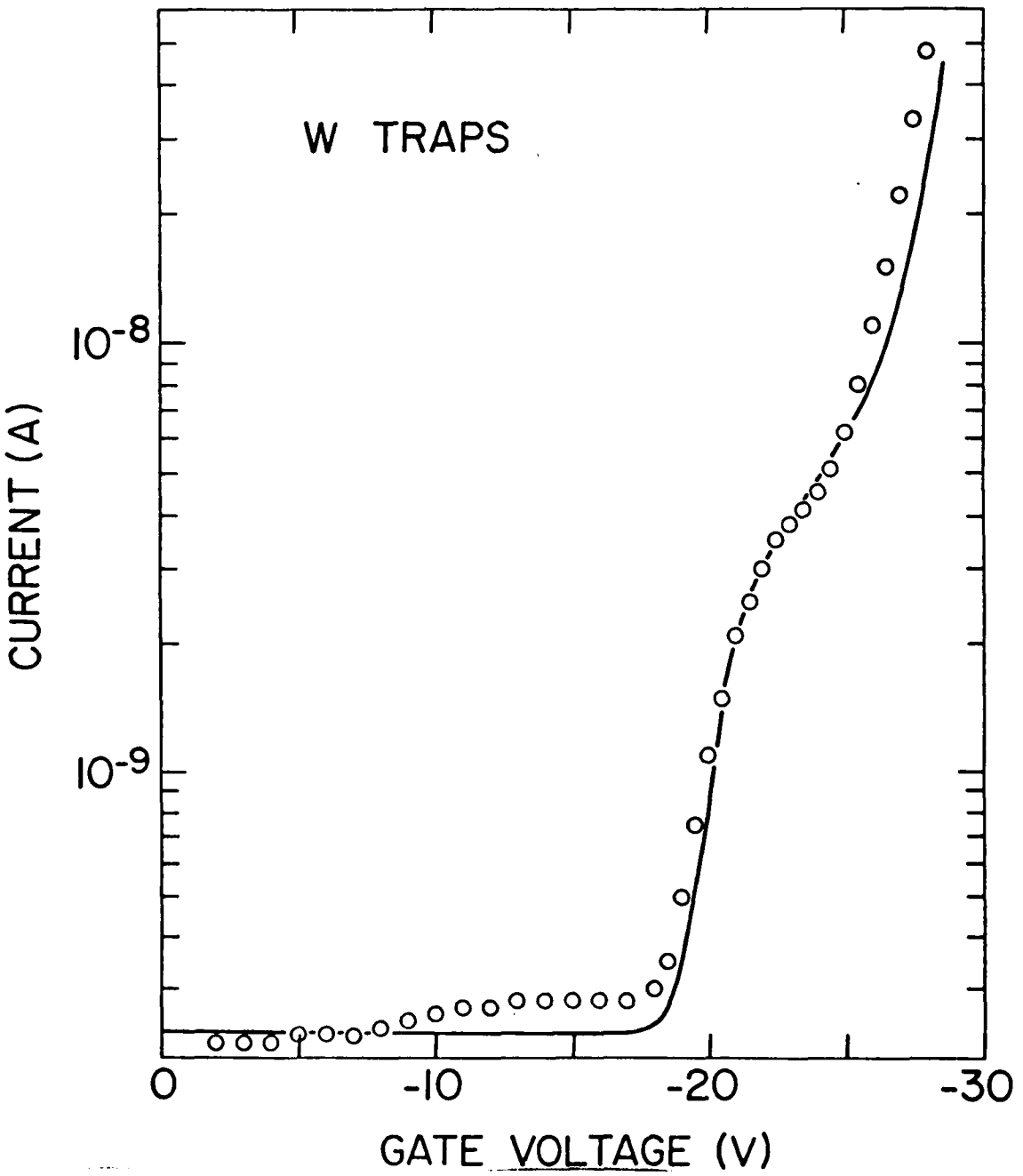

Fig. 13. Numerical simulation as described in the text for the magnitude of the current measured in the external circuit as a function of negative gate voltage for W trapping sites in the SI-MIS structures considered here. The open circles are experimental data for MLO-2F.

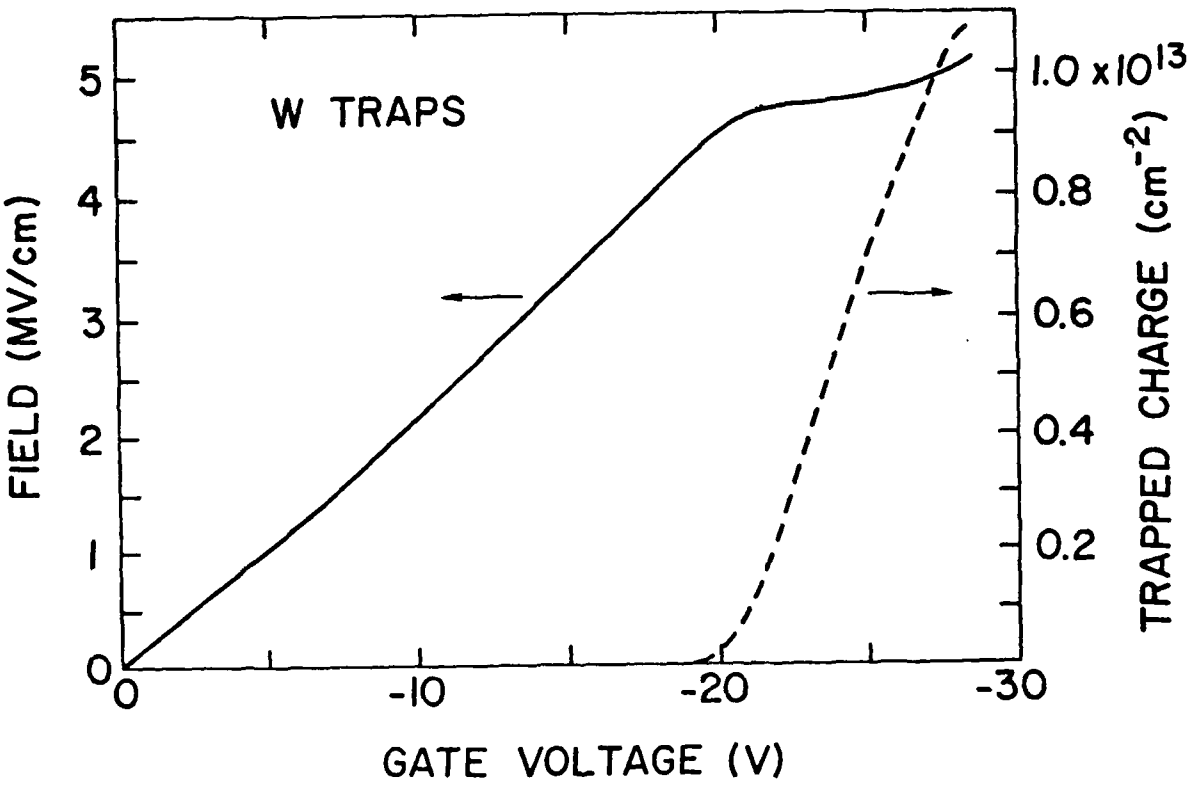

Fig. 14. Numerical simulation as described in text for trapped charge build-up, and the magnitude of the electric field at the Si rich SiO_2–SiO_2 interface as a function of negative gate voltage for W trapping sites in the SI-MIS structures considered here.

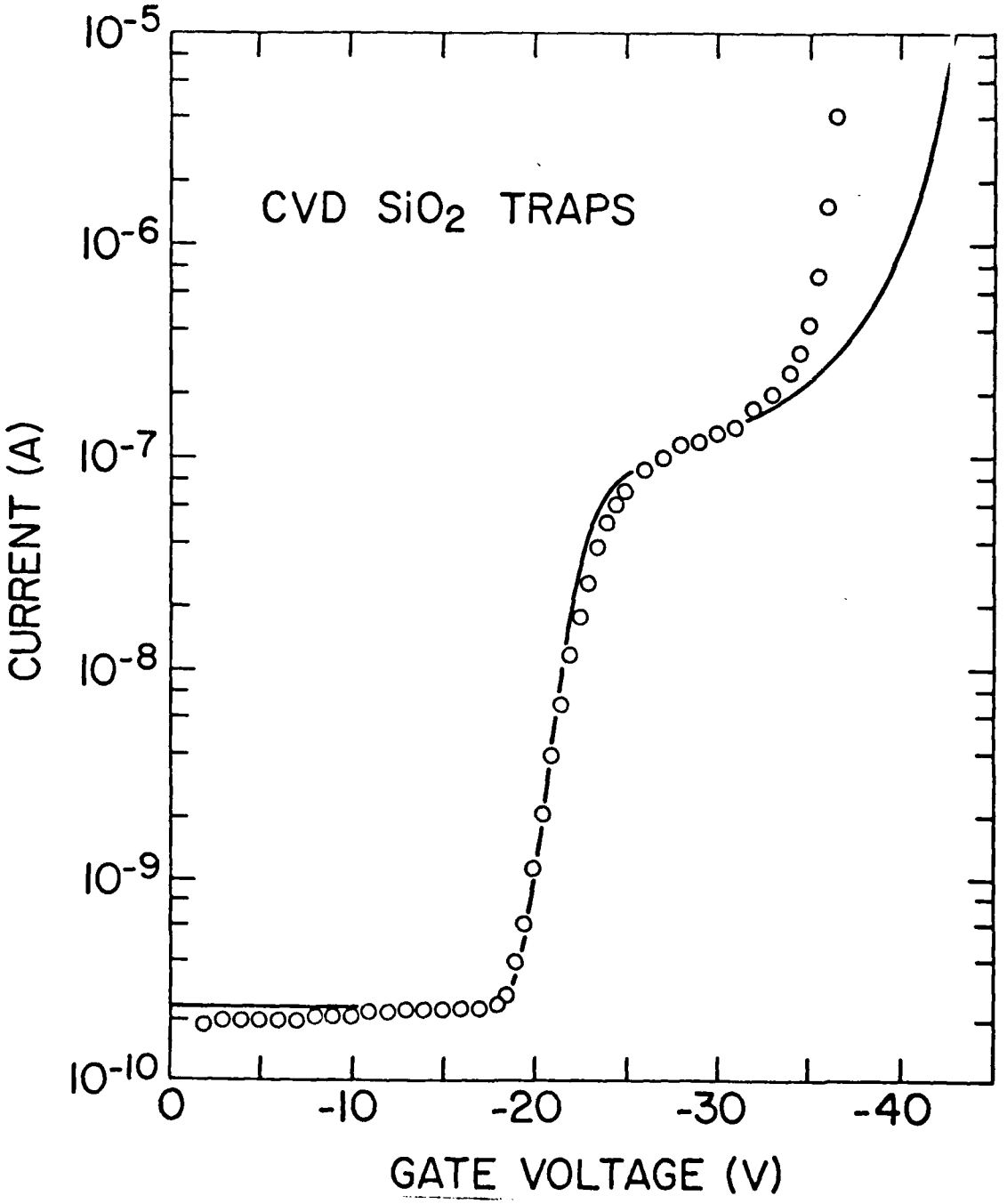

Fig. 15 Numerical simulation as described in the text for the magnitude of the current measured in the external circuit as a function of negative gate voltage for CVD SiO_2 trapping sites in the SI-MIS structures considered here. The open circles are experimental data for MLO-2D.

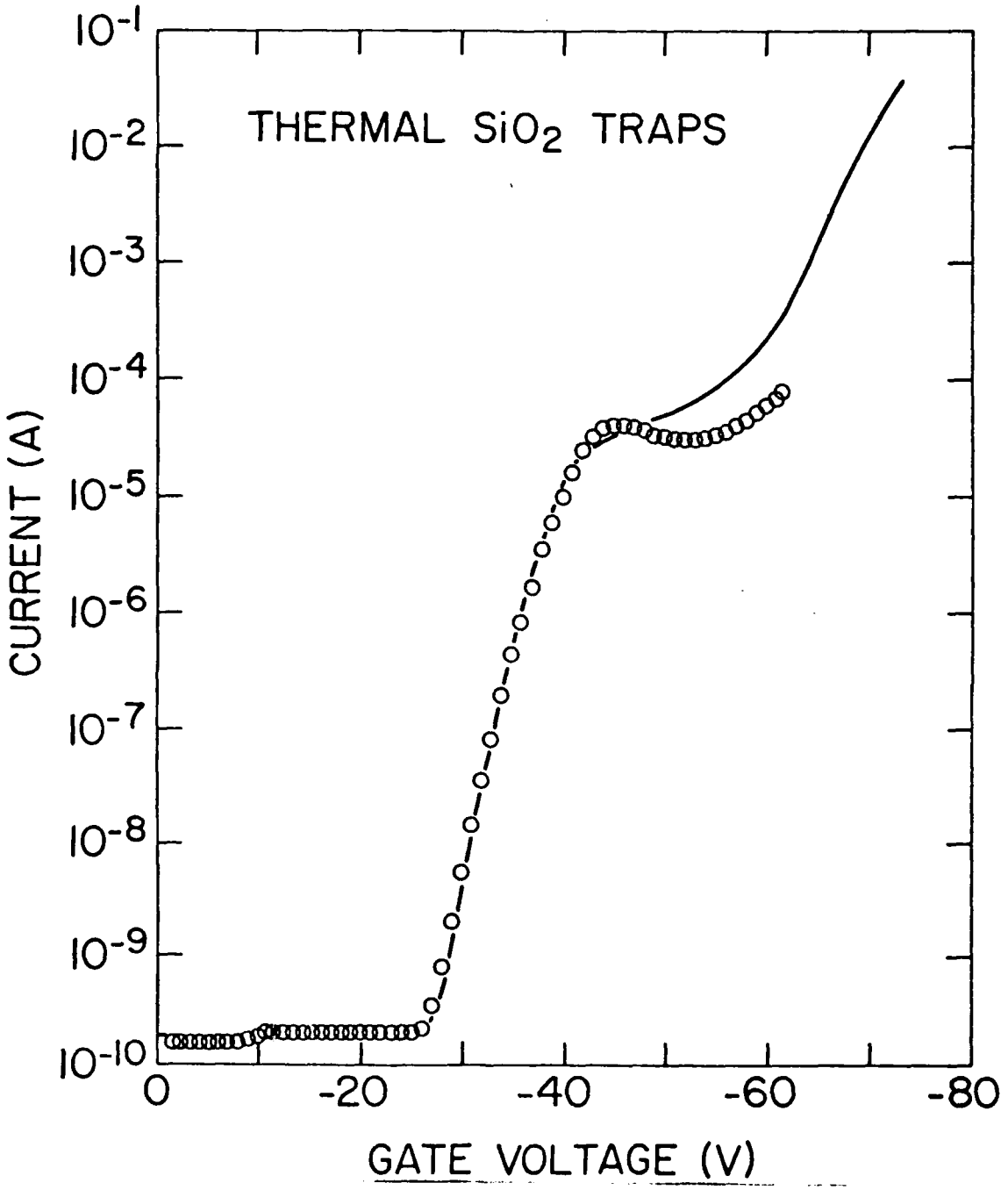

Fig. 16 Numerical simulation as described in the text for the magnitude of the current measured in the external circuit as a function of negative gate voltage for thermal SiO_2 trapping sites in the SI-MIS structures considered here. The open circles are experimental data for MLO-1P4.

OBSERVATION OF AMORPHOUS SILICON REGIONS IN SILICON RICH SILICON DIOXIDE FILMS

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ABSTRACT

Raman scattering and optical transmission measurements have been made on CVD deposited Si rich SiO_2 films (SIPOS). The measurements show seggregated regions of amorphous silicon in the as-deposited films. Annealing the films at 1150 C completely crystallizes the amorphous silicon. Annealing at lower temperatures produces films with both amorphous and crystalline regions.

Currently, there is much interest in silicon rich silicon dioxide films (commonly called semi-insulating polycrystalline silicon, SIPOS) for passivation[1,2] and non-volatile memory device[3,4] applications. Previous investigations using Auger electron spectroscopy (AES), X-ray diffraction, transmission electron microscopy (TEM), and X-ray photoelectron spectroscopy (XPS) have shown the presence of elemental silicon and various silicon oxide phases in these films[5,6]. The exact nature of the Si regions, whether they are crystalline or amorphous, is not readily determined in these films, particularly for oxygen concentrations greater than 40%, where the silicon microcrystals, if they exist at all, are less than 10 Å in size[5]. For Si rich SiO_2 films annealed at temperatures greater than 900 C, larger microcrystals have been observed ($\leq$ 100 Å), whose size increases with annealing temperature and is only weakly dependent on oxygen concentration[5].

In this study, Raman spectroscopy has been used to show directly that as-deposited Si rich SiO_2 films, with excess Si concentrations $\leq$ 13%, contain regions of amorphous silicon which crystallize with annealing treatments. Only after annealing at 1150 C are the amorphous silicon regions completely crystallized. A transition region is shown to exist for annealing temperatures intermediate between the deposition temperature and the highest annealing temperature (1150 C). Optical transmission measurements in the visible for both as-deposited and annealed Si rich SiO_2 films support the Raman scattering results.

The Si rich SiO_2 films used in this study were chemically vapor deposited (CVD) at 700 C on both sapphire substrates to a thickness of 3000 Å and quartz substrates to a thickness of 1000 Å for the Raman and the optical transmission measurements, respectively. Using techniques previously described[7], the CVD Si rich SiO_2 layers contained 46% atomic Si and were fabricated using a ratio, R_0, of the concentration of N_2O to SiH_4 in the gas phase equal to 3. Annealing was performed sequentially at higher temperatures (800 to 1150 C) in N_2 for 30 min. with the sample surface cleaned prior to each anneal. Cleaning was performed in

alkali and acid peroxide solutions using a procedure similar to that used by Irene[8] but without HF.

The Raman spectra were excited by the 5145 Å line of an Ar^+ laser and measured in the backscattering geometry. The samples were studied at room temperature and the scattered light analyzed by a conventional double monochromator. Figure 1 shows the Raman spectra obtained from the as-deposited and annealed 3000 Å Si rich SiO_2 films. The Raman lines due to the underlying sapphire substrate have been suppressed in the figure.

The Raman spectra of crystalline and amorphous silicon (α-Si) differ considerably[9,10]. The Raman spectrum of crystalline silicon shows a single strong line at $\approx$525 cm^{-1}. This is due to scattering from the three-fold degenerate, k=0 optical phonon of Si. The Raman spectrum of α-Si shows no sharp lines for frequency shifts above 200 cm^{-1} but rather a broad assymmetric continuum peaked near 480 cm^{-1}. This continuum arises from the relaxation of the normal Raman selection rules for scattering from a crystal due to the loss of translational symmetry in the amorphous state.

In figure 1 the as-grown film and the film following an annealing step at 800 C show no evidence for any sharp line in the Raman scattering near 525 cm^{-1}. The spectra is in fact identical to that observed for amorphous silicon[9,10]. For the 1000 C anneal, and possibly for the 900 C anneal as well, we observe both the continuum scattering and the sharp line at 525 cm^{-1}. For the 1150 C anneal we observe only a single sharp line at 525 cm^{-1}. This spectrum is identical to that measured on single crystal and polycrystalline silicon.

In figure 2 we show the optical density of a 1000 Å thick film both as-deposited and following an anneal at 1000 C. The film was deposited on a quartz substrate, and the transmission was measured in a double beam spectrometer with a quartz blank in the reference beam. The optical absorption of amorphous silicon is characterized by a broad featureless continuum beginning at about 1.0 eV[11]. In contrast, the absorption of crystalline or polycrys-

talline silicon shows considerable structure in the energy region between 1 and 4 eV[11]. This structure is due to density of states effects associated with critical points in the band structure of the crystal. The loss of translational symmetry in amorphous silicon smears out this structure. We find that the annealed film shows structure which is absent in the as-deposited material. These results, combined with the Raman scattering results, strongly suggest the presence of α-Si regions in these Si rich SiO_2 films.

The Raman scattering results were checked on similar films deposited on crystal silicon substrates. The as-deposited films showed the α-Si signal, but it was not possible to repeat the annealing studies since the substrate already exhibits the crystal silicon Raman signal. Films of various thicknesses were also studied to confirm that the α-Si regions are a bulk effect and not a surface effect. Additional values of the excess silicon concentration in the films were also studied with similar results.

From these experiments we conclude that the Si rich SiO_2 films contain regions of amorphous silicon within a SiO_2 matrix. These regions are distributed throughout the bulk of the film and are quite possibly the same size ($\leq$ 100 Å) as the size of the crystal silicon regions found in the annealed films. These small amorphous silicon regions crystallize at temperatures considerably above those required to crystallize amorphous silicon.

We wish to thank J. A. Bradley and R. E. Fern for invaluable technical assistance.

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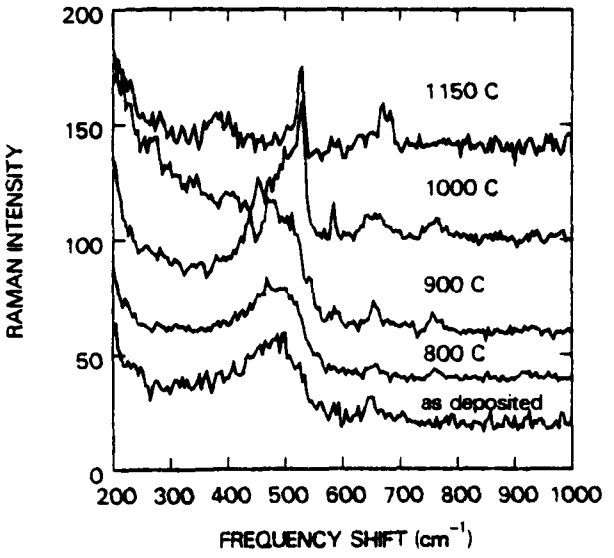

Figure 1 shows the Raman scattering spectra for Si rich SiO_2 films as-deposited and annealed at various temperatures.

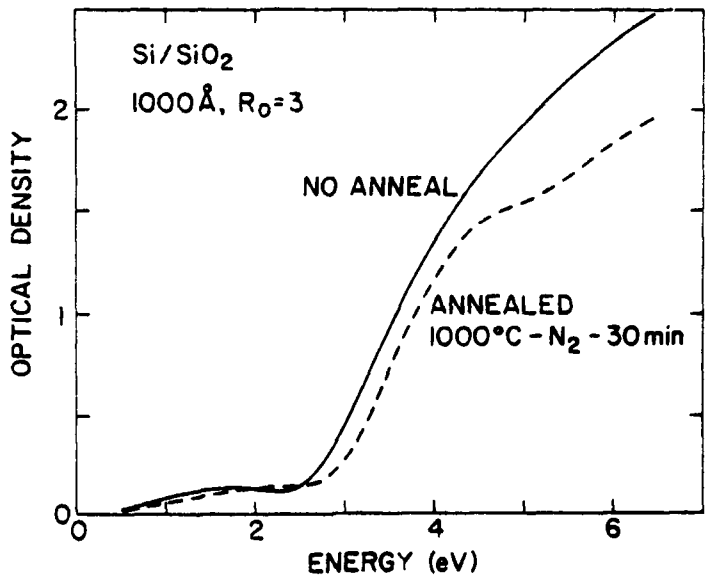

Figure 2 shows the optical density for Si rich SiO_2 films both as-deposited and following a 1000 C anneal.

ATTENUATED TOTAL REFLECTANCE STUDY OF SILICON RICH SILICON DIOXIDE FILMS

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ABSTRACT

The infrared absorption of Si rich SiO_2 films has been measured using the attenuated total reflection technique. Absorption lines attributed to SiOH, H_2O and SiH groups have been observed in the as-deposited films. The concentrations of these impurities were found to be in the mid 10^{18} cm^{-3} range. Following a 1000 C anneal no absorption lines were observed, and the concentration limit was found to be less than the mid 10^{16} cm^{-3} range.

Currently, there is much interest in silicon rich silicon dioxide films (commonly called semi-insulating polycrystalline silicon, SIPOS) for passivation[1,2] and non-volatile memory device[3,4] applications. Previous investigations using Auger electron spectroscopy (AES), X-ray diffraction, transmission electron microscopy (TEM), and X-ray photoelectron spectroscopy (XPS) have shown the presence of elemental silicon and various silicon oxide phases in these films[5,6]. In a recent study, Hartstein et. al.[7] have shown that the as-deposited Si rich SiO_2 films consist of regions of amorphous silicon within an SiO_2 matrix, and subsequent annealing above 1000 C crystallizes the amorphous regions. The size of these crystalline regions had been previously shown to be $\leq$ 100 Å, increasing with annealing temperature and only weakly dependent on oxygen concentration[5].

Pliskin[8] has investigated the infrared absorption properties of thick SiO_2 films deposited in a variety of ways. Of particular interest to us, he has quantified the infrared absorptions due to SiOH and H_2O groups in these films. Beckmann et. al.[9] and Murau et. al.[10] have used the attenuated total reflection (ATR) technique to look at the infrared absorption due to SiOH, H_2O, and SiH groups in thin ($<$ 1000 Å) SiO_2 films. In this paper we present the results of an attenuated total reflectance study of Si rich SiO_2 films. We find significant amounts of SiOH, H_2O, and SiH groups in the as-deposited films, but no detectable impurities following a 1000 C anneal.

For this study, both SiO_2 and Si rich SiO_2 films were chemically vapor deposited (CVD) at 700 C on silicon total internal reflection elements to a thickness of 1000 Å. Using techniques previously described[11], the CVD Si rich SiO_2 films were fabricated using a ratio, R_0, of the concentration of N_2O to SiH_4 in the gas phase equal to 3, and contained 46 atomic percent Si. After measurement, the samples were cleaned in alkali and acid peroxide solutions using a procedure similar to that used by Irene[12], but without HF, and subsequently annealed at 1000 C in N_2 for 30 min.

The infrared spectra were obtained using a Perkin Elmer Model 180 spectrometer. The internal angle of incidence in the silicon total internal reflection element was 32°, and the geometry was such that 80 internal reflections were obtained. The spectra obtained for the CVD SiO_2 film both as-deposited and following the 1000 C anneal are shown in Fig. 1. The corresponding spectra obtained for the CVD deposited Si rich SiO_2 film both as-deposited and following the 1000 C anneal are shown in Fig. 2. Both of the as-deposited films exhibit absorption lines at 3640 cm^{-1}, 3400 cm^{-1}, and 2260 cm^{-1}, which are absent after annealing. The lines at 3640 cm^{-1} and 3400 cm^{-1} have been attributed to SiOH and H_2O groups, respectively.[8] The line at 2260 cm^{-1} has been attributed to the SiH group.[9,10] It is clear from the spectra that more impurities are present in the Si rich film than in the pure SiO_2 film, particularly the SiH group. It is also clear that annealing at 1000 C removes these impurities from the films. In what follows we seek to determine the actual concentration of impurities represented by the absorption lines in the spectra.

Pliskin[8] has analysed the silanol (SiOH) and water content of SiO_2 films gravimetrically and related the weight percents to the strengths of the infrared absorptions. The relationships given are

$$W = (-14A_{3650} + 89A_{3330})(2.2/\rho) \quad \text{and} \tag{1}$$

$$S = (179A_{3650} - 41A_{3330})(2.2/\rho), \tag{2}$$

where W is the wt. % water (including H_2O from "easily" removed silanol), S is the wt. % OH as silanol, ρ is the density of the film in g/cm^3, and A_ν is the optical density per μm of film at frequency ν. In the analysis that follows, we take the density of the films to be 2.2 g/cm^3, and identify our 3640 cm^{-1} absorption with Pliskin's 3650 cm^{-1} absorption, and our 3400 cm^{-1} absorption with his 3330 cm^{-1} absorption. The weight percentage determination is easily changed to a concentration determination by using the atomic weights of the species involved.

In order to utilize Eqs. 1 and 2 to determine the concentration of silanol and water in the SiO_2 films, we must calibrate the absorption strength measured in our particular ATR geometry. We have chosen a direct method of accomplishing this. The absorption band in transmission of SiO_2 near 1600 cm^{-1} was accurately measured using a 6.56 μm thick sample annealed at 1000 C. The strength of this absorption was then compared to the same line measured on the annealed samples using the ATR geometry. From this comparison it is found that the effective gain from this ATR geometry was a factor of 92 over a transmission measurement. Using this factor and Eqs. 1 and 2, the concentration of SiOH and H_2O groups in the SiO_2 films can be calculated. The results of this calculation are shown in Table 1. The entry for the annealed films gives the upper limit of the concentration of these impurities that can be set from the present measurement. It does not represent the limits of the sensitivity of the ATR technique.

The correlation of the infrared absorption of the Si-H bond to concentration has been worked out in detail by Brodsky et. al.[13] They give the following relation for the concentration of any species to its absorption.

$$N = \frac{(1+2\epsilon_m)^2}{9\epsilon_m^2} \frac{N_A n}{(\Gamma/\zeta)} \int \frac{\alpha(\omega)}{\omega} d\omega \qquad (3)$$

where N is the concentration of Si-H bonds, $\epsilon_m = 2.2$ is the optical dielectric constant of SiO_2, N_A is Avogadro's number, n is the number of host bonds in units of m-mole/cm^3, Γ is the absorption strength of the Si-H bond in units of cm^2/m-mole, ζ is the number of Si-H bonds per silicon atom (taken to be 1 for our case), α is the absorption coefficient and ω is the frequency. Following Brodsky et. al.[13], we take $\Gamma = 3.5$ for Si-H bonds. Brodsky's[14] nuclear analysis of the H content of amorphous silicon films shows that Eq. 3 overestimates the Si-H concentration by a factor of 2.

In order to calibrate the determination of the concentration of Si-H bonds, we have used a technique similar to that described above. Using the transmission data of the thick SiO_2 film

and Eq. 3, we have obtained the value of $\Gamma = 0.094$ cm^2/m-mole for the particular vibrational mode of SiO_2 giving the 1600 cm^{-1} absorption. Using this value and the absorption data for the same line in the ATR spectrum, it is possible to calibrate the integrated absorption lines in a similar way to the procedure already used to calibrate the absorption intensities. With this scaling procedure, the absorption lines at 2260 cm^{-1} were analysed using Eq. 3, including the factor of 2 correction, in order to obtain the concentration of Si-H bonds in the samples. These results are also given in Table 1.

From these results it is clear that the amounts of silanol and water in both the as-deposited Si rich SiO_2 and the CVD SiO_2 films are comparable. The Si rich film shows somewhat more silanol and almost a factor of 2 more water than the normal CVD film. The Si rich film also shows more than 10 times more SiH than the normal CVD film. This fact is consistent with the presence of excess Si, but the concentration of SiH does not even come close to accounting for the majority of excess Si present in the film. The excess Si is predominantly contained in seggregated amorphous silicon regions.

It is also important to note that the frequency of the SiH absorption observed (2260 cm^{-1}) is not the same as observed for SiH bonds in amorphous Si,[13] but is rather close to the Si-H bond (2280^{-1}) found in amorphous SiO_2.[15] Therefore, although it might be tempting to suppose that the hydrogen is present in the amorphous Si regions, that appears not to be the case. It must be present in the SiO_2 itself (it is also observed in the normal CVD SiO_2) and possibly also at the interfaces between the SiO_2 and the amorphous Si regions.

There is an additional small absorption line at 2140 cm^{-1} which we have been neglecting up till now. It is close to the absorption line expected for Si-H bonds in amorphous silicon when either O of N is present in the back bonds of the Si.[15] If this identification is correct, the absorption corresponds to a uniform density of 3.8×10^{17} cm^{-3}. Equivalently, it corresponds to a hydrogen density in the amorphous silicon regions of 3.1×10^{18} cm^{-3}. It should be noted that this absorption line is only seen in the Si rich films.

It is quite difficult to assess the possible error present in the concentrations determined using this procedure. In the ATR work of Beckmann et. al.[9], they claim an accuracy of only an order of magnitude. The present experiment is much better than that since we used a direct experimental method of calibrating the ATR method rather than the theoretical calculation used by Beckmann et. al.[9] The absolute accuracy is then probably better than a factor of 2, and the relative accuracies of the concentrations considerably better than that.

In passing, it is worth noting that in the Si rich SiO_2 film, one additional absorption line can be detected which is not present in either the CVD oxide or the annealed samples. The line appears at 1770 cm^{-1}. We have not identified the mechanism responsible for this absorption as yet. It could be due either to bonding differences in the Si rich oxide or to an additional impurity.

In conclusion, we have measured the infrared absorption of Si rich SiO_2 films using the attenuated total reflection technique. The films were found to contain substantial amounts of SiOH, H_2O and SiH groups. These impurities were found to disappear following a 1000 C anneal.

We wish to thank M. H. Brodsky for many helpful discussions as well as a critical reading of this manuscript.

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TABLE 1

	Impurity Concentration (cm^{-3})		
	SiOH	H_2O	SiH
Si rich SiO_2 as-deposited	5.2×10^{18}	3.9×10^{18}	1.0×10^{18}
CVD SiO_2 as-deposited	4.0×10^{18}	2.3×10^{18}	8.5×10^{16}
Si rich and CVD SiO_2 1000 C anneal	$< 5 \times 10^{16}$	$< 3 \times 10^{16}$	$< 1 \times 10^{16}$

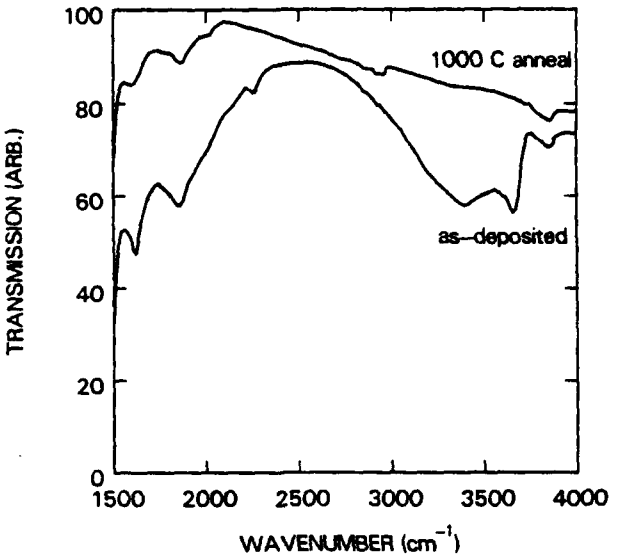

Figure 1 shows the infrared ATR spectra for CVD deposited SiO_2 films both as-deposited and following a 1000 C anneal. Because of the ATR geometry, the units of transmission should be regarded arbitrary. The curve for the 1000 C anneal has been shifted upward for clarity. Prior to this shift the transmissions at 4000 cm^{-1} were equal.

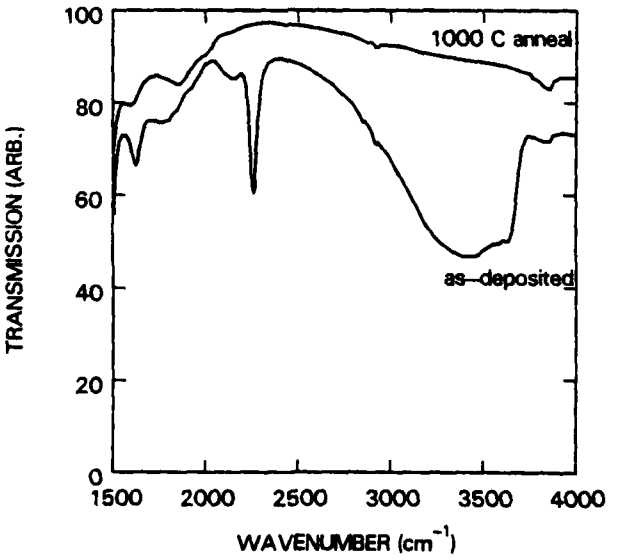

Figure 2 shows the infrared ATR spectra for CVD deposited Si rich SiO_2 films both as-deposited and following a 1000 C anneal. The transmission is in arbitrary units, and the 1000 C anneal curve has been shifted for clarity. Prior to this shift the transmissions were equal at 4000 cm^{-1}.

Residual Stress, Chemical Etch Rate, Refractive Index and Density Measurements on SiO_2 Films Prepared Using High Pressure Dry Oxygen

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ABSTRACT

Dry oxygen pressure at 500 atm is used to grow SiO_2 films 10^3 nm thick on silicon at 800°C. The residual film stress, chemical etch rate, refractive index, and density of the pressure-oxide films is measured and compared with measurements of thermal oxide films prepared at 1 atm dry oxygen pressure. The high-pressure/low-temperature films exhibited higher refractive indices, slower chemical etch rates, and higher measured densities compared to 1 atm thermal oxides prepared at 1000°C. These results are attributed to the lower oxidation temperature rather than the higher oxidation pressure of the pressure-oxide films. It is concluded that the formation of higher density SiO_2 films is a specific result of low temperature processing. The use of high pressure oxidation provides a convenient technique to prepare the low temperature high density SiO_2 films of sufficient thickness for further study.

*Electrochemical Society Active Member
Key Words: high pressure oxidation, silicon, silicon dioxide, density, film stress

INTRODUCTION

Recently, Zeto et al (1,2) reported enhanced oxidation rates for single crystal silicon thermally oxidized in dry oxygen at elevated oxygen pressures up to 500 atm. It was shown (1) that the silicon oxidation rate obtained by using oxygen at 140 atm (ie the pressure of oxygen in commercially available oxygen tanks) and 800°C was comparable to the rate obtained by using 1 atm oxygen at 1200°C. Therefore, the use of elevated oxygen pressures enables a reduction of the oxidation temperature and/or time for an oxidation step. This temperature/time reduction has great technological importance because of the need to maintain sharp dopant profiles and minimize the creation of thermally induced defects in modern small devices. The use of steam (3) and high pressure steam (4) for the thermal oxidation of silicon also offers considerable kinetic enhancement, however, the quality of the SiO_2 and Si may be degraded based on reports of increased electron trapping in SiO_2 due to H_2O (5) and increased Si defects resulting from exposure of the Si to steam oxidation (6).

Whether the MOS industry will accept a new process, such as the use of increased oxidant pressures, will depend both on the need for the lower temperature processing and the demonstration that the SiO_2 quality is not degraded by the new process. It is clear from the industry trend towards smaller devices that lower processing temperatures are required and therefore this study is aimed toward demonstrating that important aspects of the SiO_2 quality resulting from high pressure dry oxidation of silicon can be equivalent to the SiO_2 grown in the conventional 1 atm processes.

As with any new process, the dry high pressure oxidation process has problems associated with reproducibility and optimization. Notwithstanding these anticipated difficulties, Zeto et al (2) reported that mobile and fixed charge levels were acceptably low (in the low $10^{10} charges/cm^2$ range) on many samples. These promising results have provided the impetus to improve the process through equipment evolution and to obtain more physical properties data on the resulting SiO_2 films.

The present study reports the results of several physical properties measurements on SiO_2 grown by the high pressure dry oxidation of silicon: residual film stress, chemical etch rates, density, refractive index and film morphology as obtained by transmission electron microscopy (TEM). Collectively, these measurements show that the films have increased density as compared with 1 atm films prepared at conventional oxidation temperatures of 1000°C. The higher refractive indices, slower etch rates and higher measured densities of the high-pressure low-temperature films are attributable to the lower processing temperatures rather than the higher oxygen pressures. Thus a specific advantage of high pressure oxidation methods is that these higher density low temperature SiO_2 films can be prepared in practical oxidation times.

EXPERIMENTAL PROCEDURES

Sample Preparation

Four high pressure dry oxygen oxidation runs were performed as described below to grow oxides about $10^3 nm$ thick on six Si substrates. The Si slices were nominally 2 Ω -cm P type, 2.54 cm diameter and 0.02 cm thick. Three each of <111> and <100> orientations were used and designated 111, 112 and 113 for the <111> samples and 012, 013 and 014 for the <100> samples. Control oxides were grown at 1 atm, 1000°C or 800°C in pure dry O_2 on <100> silicon to similar thicknesses and were used in the film stress, etch measurements and refractive index measurements to obtain meaningful comparisons with the high pressure grown samples. Prior to any oxidation all Si slices were thoroughly cleaned by a previously described procedure (7). The six samples for high pressure oxidation were initially oxidized at 1000°C in 1 atm ultra dry O_2 to obtain 100 nm SiO_2. This was done to obtain a reproducible initial curvature in the Si substrates for the stress measurements.

Pressure Oxidation

The apparatus used for the high pressure dry oxidation was described previously (1) with the exception that a larger pressure vessel was used to accommodate the 2.54 cm. diameter Si slices noted above. For each of the experimental oxidations, the Si slices were heated to about 800°C while a vacuum was drawn on the vessel. Then, 500 atm dry oxygen pressure was applied within several minutes. After the desired oxidation time the pressurized vessel was withdrawn from the furnace and cooled by radiation. All samples were oxidized at 800°C to yield about $10^3 nm$ SiO_2. The oxidation rates for the <100> samples were about 87 nm/hr and 132 nm/hr for the <111> Si. The H_2O content of the pressurized gas was measured as less than 1 ppm.

Film Stress

The residual room temperature stress was calculated from a measurement of the curvature of a Si wafer before and after the SiO_2 film growth by dry pressure-oxidation. The change in Si curvature was measured by an optical interference technique. The apparatus, appropriate equations, elastic constants used for the calculations as well as the procedures were previously described (8) for a study of Si_3N_4 film stress. Only a small difference (less than 10%) is anticipated in the residual stress for <100> and <111> orientations due to the difference of elastic constants for the different Si orientations and we ignored this difference in the present study. The pressure-oxide samples had about 5% thickness non-uniformity across the sample as compared with about 1% for the 1 atm SiO_2 oxides. The direct implication of this on the measured film stress has not been determined but it may contribute to the overall scatter of the pressure-oxide stress data.

Chemical Etch Rates

Chemical etch rates have been shown to be a very sensitive measure of SiO_2 film density (12). The temperature, composition and extent of agitation of the etchant solution can all alter chemical etch rates. In order to preclude obscuring comparisons between high pressure oxides, controls and low temperature oxides due to experimental diffculties, samples and controls for a given comparison were etched simultaneously in the same solution. For the comparison of high pressures oxides with 1 atm 1000°C standards, two samples of each were etched together in a commercially available 9/1: NH_4F/HF mixture at ~22°C. For this comparison (Figure 1) more scatter was seen for the pressure oxides. The scatter was due to the larger non-uniformity of the SiO_2 thickness for these samples and the problem of returning to the same spot on the sample for ellipsometric thickness measurement after each exposure to etchant. However, the results to be reported are outside this scatter. Similarly, the comparison of etch rates for the 1 atm 800°C and 1000°C grown SiO_2 was made on samples etched in a 9/1: NF_4/HF simultaneously and together at ~22°C. The differences in the 1000°C 1

atm controls are presumably due to the above mentioned temperature, agitation and etchant batch differences.

Density

The SiO_2 film density, ρ_1 was calculated from measured values for the mass change of the samples before and after removal of the film by etching and the volume of the film as obtained from the area of the Si wafer and the film thickness. Only the film on the polished side of the Si was used and a correction was made for the area lost as the Si wafer flat. The weighing accuracy was better than $3 \times 10^{-6} g$ while the oxide mass was about $10^{-3} g$. The average film thickness accuracy was estimated to be better than about 3% based on multiple ellipsometric measurements taken across the wafers and the surface area was known to better than 3%. Based on these values, the error in ρ, $\Delta \rho$, is calculated to be about 10^{-2}. Therefore, the higher density measured for the high pressure grown and 800°C, 1 atm oxides as compared with 1000°C, 1 atm is a real difference but the absolute values are somewhat uncertain to better than several percent.

Film Thickness and Refractive Indexes

The SiO_2 thickness and refractive indexes were measured by ellipsometry. A description of the instrument with the various constants used was previously published (9). The reported measurements of refractive index were made near one-half of an ellipsometric period i.e. at odd multiples of ~140 nm for the 632.8 nm light and ~120 nm for 546.1 nm light. Near these thicknesses the ellipsometric measurement is most sensitive to different refractive indexes. The index measurements were made during the course of the etching experiments and the index values corresponding to half-period thicknesses were tabulated.

TEM

Samples were prepared for microscopy by removal of the Si with an $HF - HNO_3$ etchant. Since the SiO_2 was too thick ($\sim$ 1 μm) for penetration by the 100 KeV electrons, the etchant was also used to etch away most of the SiO_2 leaving about 100 nm for examination by TEM.

EXPERIMENTAL RESULTS

Residual Stress Measurements

A comparison of the SiO_2 film stress for the high pressure oxides, controls (1 atm O_2, 1000°C) and literature values are shown in Table 1. The high pressure oxides show more scatter in the stress values than the controls and this may be due to the greater thickness non-uniformity found for these films (about 5% across the wafers). Considering the scatter in the stress values, the film stress for the high pressure oxides is the same as for the controls. Optical microscopic examination revealed no evidence for Si slip due to stress on any of the substrates.

Chemical Etch Rates

Figure 1 shows the combined etching results from two pressure-oxide and two control samples 1 atm 0_2, 1000°C. Individually the etch rates were 50.0 nm/min and 48.2 nm/min for the pressure samples and 58.6 nm/min and 58.7 nm/min for the controls. The spread in the pressure-oxide samples was due to thickness non-uniformity which required returning to the exact same spot on the SiO_2 film for the repeated thickness measurements. However, the difference in etch rate between pressure-oxides and controls was well outside the scatter and is therefore considered significant. Pliskin and Lehman (12) reported that a more dense SiO_2 can give rise to a slower etch rate in an HF based etchant.

Index of Refraction

Table 2 shows that the high pressure grown samples have a significantly higher refractive index than the controls. This may be caused by pressure oxides having a higher density since it was reported that a higher SiO_2 film density will yield a measurably higher refractive index (12). The measurements associated with sample 013 are particularly interesting, since this sample has an initial oxide thickness near one-half an ellipsometric period. The initial oxide

thickness is about 1000 nm, of which 100 nm is a 1 atm 1000°C SiO_2 and the remaining SiO_2 has been grown at 800°C with 500 atm oxygen. Since oxidation takes place at the Si - SiO_2 interface, the 1 atm SiO_2 is always on top of the high pressure SiO_2 hence it would be removed after the first etching. However, before etching the composite index is larger than for 1 atm 1000°C SiO_2 but smaller than the high pressure SiO_2 while after the removal of this outer SiO_2 that has a lower index, the index returns to the pressure oxide value. This is a predictable result based on the fact that 1 atm, 1000°C SiO_2 has a lower index than the 500 atm 800°C films and this result demonstrates the sensitivity of the ellipsometric measurement.

Film Density

Since both the etch rate and index of refraction measurements showed the possibility that pressure-oxide SiO_2 samples have higher density, the direct measurement of density was performed. Table 3 shows that indeed the pressure-oxide films have a higher density than the 1 atm oxides.

TEM

Figure 3 shows an area of a pressure-oxide film which had an unusually large amount of particulate. Diffraction showed the particulate to be amorphous and the electron contrast appeared to be about the same as for the 1 atm SiO_2. The pressure vessel used to prepare these samples contained a fused silica test tube liner to hold the silicon slices. We believe that the particulate is SiO_2 dust from the fused silica insert since procedures required that it be thermally cycled, physically handled, and mechanically vibrated in every experiment. Undoubtedly this particulate would contribute to various dielectric failure modes, therefore a second generation high pressure oxidation system has been designed to eliminate this problem.

Up to this point the properties measurements on the high pressure oxides taken collectively indicate that these films have a higher density that the 1 atm 1000°C controls. However, in view of a recent study by Taft (13) which shows that a higher refractive index results from

lower oxide growth temperatures, the higher density found for the high pressure oxides in this study may be due to the 800°C oxidation temperature and therefore independent of the higher oxidation pressure. To check this possibility measurements of the refractive index, etch rates and density using the same techniques described above were done on 800°C, 1 atm oxygen grown SiO_2 films. The results shown in Table 4, while not extensive, clearly show that the lower temperatures produce a more dense oxide film. When an 800°C 1 atm SiO_2 film was heated in flowing N_2 at 1000°C for 2 hrs, the refractive index returned to the 1000°C value. This suggests that higher defect concentrations produced at higher temperatures are responsible for the lower densities. Further work to clarify this situation is in progress.

SUMMARY AND CONCLUSIONS

It was previously demonstrated that a significant oxidation rate enhancement is obtained by using high dry O_2 pressures and that acceptable oxide charge and interface state levels could also be obtained. The present study extends the property measurements to include film stress, chemical etch rate, refractive index, density and TEM morphology. These measurements show that: (1) there is no significant difference in the residual Si/SiO_2 film stress for high pressure and 1 atm thermal oxides, (2) high-pressure/low-temperature thermal oxide SiO_2 films have a significantly higher density than films prepared at conventional oxidation temperatures such as 1000°C, and (3) 1 atm thermal oxides prepared at 800°C have a higher density than films prepared at 1000°C.

The formation of high density SiO_2 films on silicon is therefore a specific merit of reduced oxide growth temperatures. The preparation of these higher density SiO_2 films is an advantage afforded by high pressure oxidation methods since higher pressures allow the oxides required in IC devices to be prepared at reduced temperatures in practical oxidation times. It remains to be determined whether or not the higher density material has other interesting properties, such as improved dielectric strength.

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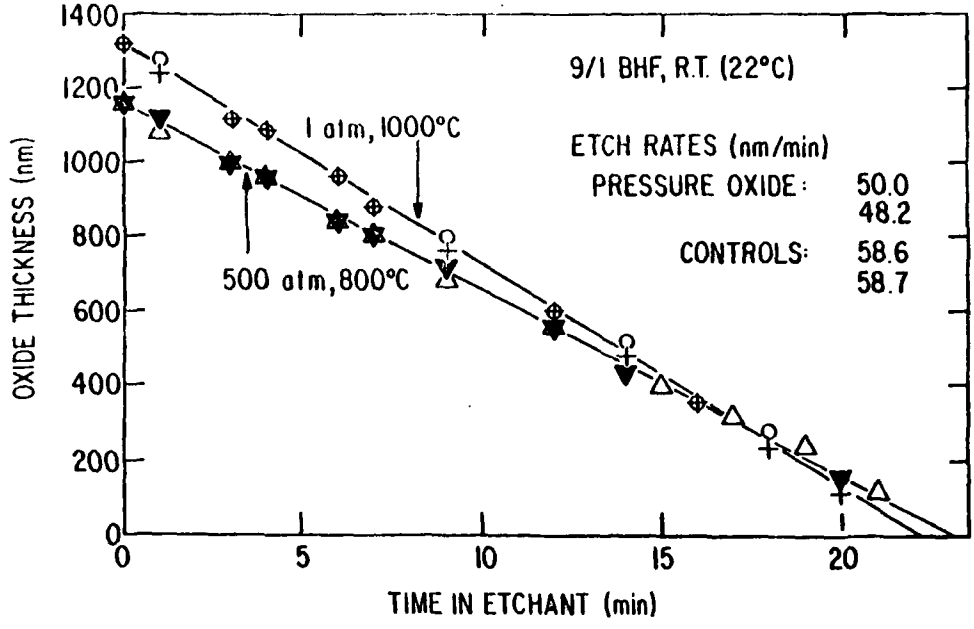

Figure 1. Plot of SiO_2 thickness versus time in etchant for two pressure-oxide and two control samples.

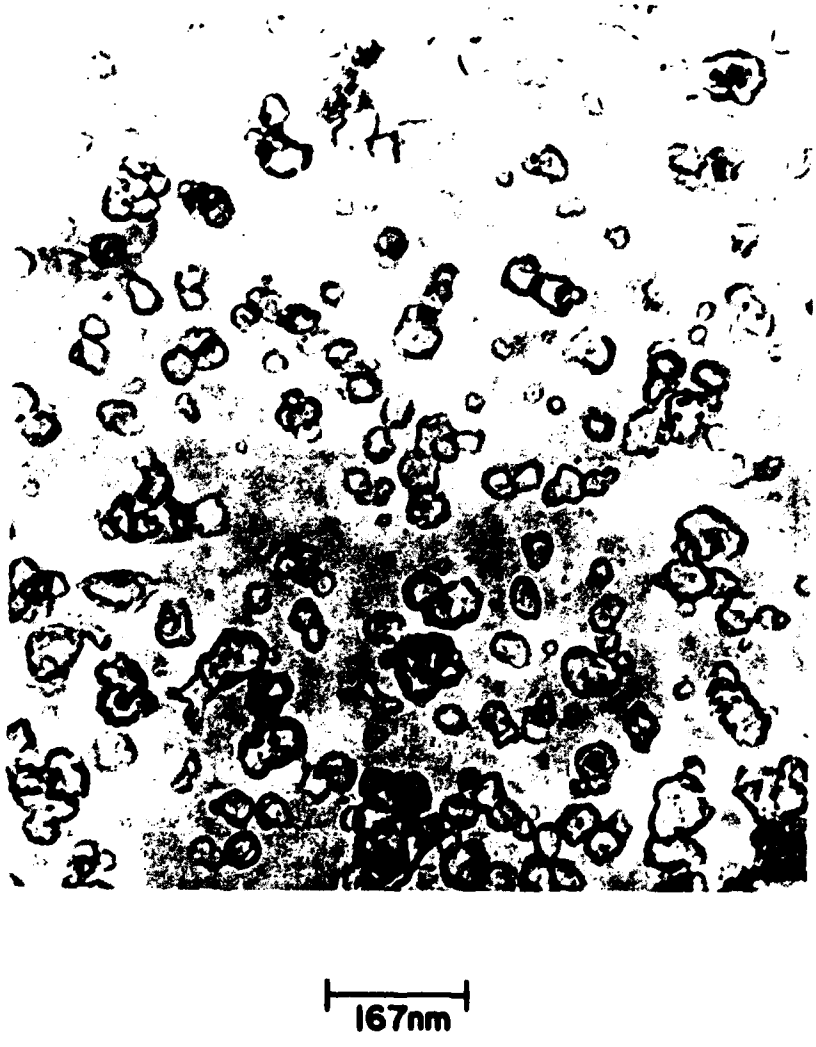

Figure 2. TEM micrograph of pressure-oxide area which has a large number of amphorous SiO_2 inclusions.

Table 1

SAMPLE ID	STRESS ($dynes/cm^2/\cdot 10^{-9}$)
PRESSURE OXIDES (500 atm, 800°C)	
012	1.5
013	4.0
014	4.0
111	2.3
112	4.0
113	2.8
Average:	3.1
CONTROLS (1 atm, 1000°C)	
005	4.1
006	4.2
LITERATURE	
Jaccodine and Schlegal (10)	2.0 for 875°C SiO_2 2.7 for 1000°C SiO_2
Whelan et al (11)	3.7 for 1200°C SiO_2

Table 1. Residual film Stress Results for Pressure-Oxide SiO_2, Normal 1 atm SiO_2 and Literature Values.

Table 2

SAMPLE ID	SiO_2 THICKNESS (nm)	REFRACTIVE INDEX (at λ = 632.8 nm)
PRESSURE OXIDES (500 atm, 800°C)		
112	947.6	1.476
	153.3	1.475
014	983.0	1.473
	941.4	1.473
	685.7	1.475
	129.8	1.478
113	960.0	1.475
013	967.2 (No etch)	1.467
	684.6	1.477
	Average Pressure-Oxide = 1.475	
CONTROLS (1 atm, 1000°C)		
001	959.0	1.461
002	951.4	1.461
	1293.0	1.462
	Average Control = 1.461	

Table 2. Refractive Index Results for Pressure-Oxide SiO_2 and Control Samples fn 632.8 Light.

Table 3

SAMPLE ID	DENSITY (g/cm^3)
PRESSURE-OXIDES (500 atm, 800°C)	
113	2.41
013	2.35
CONTROL (1 atm, 1000°C)	
005	2.26

Table 3. Density Results for Pressure-Oxide and Control Samples.

Table 4

Refractive Index:	1.468 @ 632.8 nm light 1.476 @ 546.41 nm light
Etch Rate:	800°C - 1 atm - 72 nm/min 1000°C - 1 atm - 81 nm/min Control
Film Density:	two samples 2.47 g/cm^3 2.42 g/cm^3

Table 4. Refractive Index, Etch Rate and Film Density Results for 1 atm 800°C SiO_2

Automatic Tester Used in Electron Trapping and Hole Trapping in SiO_2*

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ABSTRACT

Electron trapping in SiO_2 is a limiting factor in the design of n-channel MOSFET structures. This paper describes an automatic tester of the RF avalanche technique using MOS capacitor structures (Nicollian et al. 1969).

1. Introduction

The automatic avalanche injection tester uses a 50 KHz saw-tooth waveform. This allows the tester to be used for both electron and hole injection. The amplitude of the saw-tooth is automatically adjusted to maintain a constant average current through the oxide as monitored by the electrometer. The output of the electrometer closes the servo loop that controls the saw-tooth amplitude. Since the charge due to trapped electrons in the oxide grown on a p-type substrate can be monitored by the change in flat-band voltage, the tester is designed to automatically interrupt the avalanche injection and measure the flat-band voltage. The data are stored on tape using a 5100 computer. For the sake of continuity, redundancy is added to the circuit descriptions when going from one circuit card to another.

Some of the features of this tester are as follows:

1. The average avalanche current can be dialed in directly with a 3-digit accuracy over the range of 10^{-11} to 10^{-6} amps.

2. The capacitance ratio, used for flat-band voltage measurements, can be dialed in directly with a 3-digit accuracy.

3. Flat-band voltages of up to 20 volts can be measured.

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4. The maximum saw-tooth voltage, used for avalanche injection, is approximately 100 volts. This voltage is switched off before the sample is switched from avalanche to the flat-band measurement mode to protect the relays used for switching.

5. The time is automatically corrected by stopping the timer during the flat-band measurement mode to give the actual integrated avalanche time.

6. The tester outputs lend themselves nicely to any automatic data acquisition system. The data can be analyzed by the computer programs available to result in a characterization of the traps involved.

2. Circuits Used in the Avalanche Tester

A.	Timing diagram	(Fig. 1)
B.	Crystal controlled clock and timer circuit	(Fig. 2 and 2A)
C.	Shift register card timing	(Fig. 2)
D.	Sample and hold card	(Fig. 3)
E.	Shift register card comparator and reset	(Fig. 4)
F.	Avalanche card	(Fig. 5)
G.	Tester panel circuitry	(Fig. 6)
H.	Probe circuitry	(Fig. 7)
I.	Composite drawing	(Fig. 8)

3. Circuit Description

A. Crystal Controlled Clock and Timer Circuit (see Figs. 2 and 2A)

The crystal controlled clock uses a MOS counter time-base integrated circuit developed by Mostek Corp. (MK5009P). The circuit uses a 1 MHz crystal and then divides it down to 1 Hz. This 1 Hz clock goes to the timer circuit via the avalanche card. If the avalanche card is not in its socket correctly, the timer will not work (interlock).

The timer circuit consists of five numeric displays with logic (TIL 306). The binary outputs are connected to the device coupler connector. The time is gated off, on the avalanche card, when the tester switches from avalanche to measure flat-band voltage. There is a program disconnect push button on the input to the timer which allows the termination of a run at any time.

B. Shift Register Card Timing (see Figs. 1 and 2)

The 1 Hz clock goes to the shift register (74164), and the time interval counters (74196). The time interval counters are used to determine the time between flat-band measurements. The output of the counters go to a two wafer switch. The output of the switch goes to the input of a monostable multivibrator (74121). The output of the 74121 is a narrow pulse which goes to the shift register. This pulse is shifted through the shift register at a 1 Hz rate. (See timing diagram Fig. 1). The first shift register output used is pin 4 which is inverted and goes to a latch (7474). The latch output goes to the avalanche card where it disconnects the 50 KHz saw-tooth and the bias from the electrometer's comparator. It also gates off the clock and the timer stops for six seconds. The second shift register output used is pin 5 which is one second after the pin 4 output. This output goes to inverters and then goes to two latches and a 74121 which triggers the meters. The first latch (7474) drives a 2N4401 transistor which energizes the relays in the probe circuitry, and changes the mode of the tester from avalanche to flat-band measurement for four seconds. At this time from shift resister pin 12 the device coupler will be sent a pulse to take data. The second latch is a 7404 hex inverter wired as a latch. This latch is on the sample and hold card and it keeps the sample and hold in the hold state until either the inverted second output is applied or a flat-band measurement on a sample is made. (This will be explained later when the sample and hold card is explained). The third output pin 6, which is two seconds after the pin 4 output, goes to a 7404 hex inverter wired as a latch. The output of this latch is two seconds long and goes to the input of a MOS analog switch (AH0014D) which is located on the sample and hold card.

C. Sample and Hold Card (see Fig. 3)

The input to the MOS analog switch (AH0014D) mentioned above switches a negative voltage to the gates and source of an n-channel dual gate MOSFET. This MOSFET charges a capacitor with a constant current to produce a linear ramp. This ramp goes to the input of an

FET op-amp (LH0052D) with a gain of two. The amplitude of the ramp is changed by switching the negative supply voltage (SW-1) which is located on the tester panel.

The output of the op-amp is filtered and goes to the input of the sample and hold. This output ramp also goes to the low bias input on the back of the Boonton capacitance meter (Model 72BD). In the flat-band measurement mode this negative ramp is applied to the substrate of a p-type sample or to the aluminum contact on the oxide of an n-type sample via the capacitance meter.

The comparator that controls the latch, which sets the sample and hold circuit in the hold state, works in the following manner:

Assume that a sample is on the probe station. The (test - cap. set.) switch located on the panel is set in the cap-set position, which connects the (avalanche-cap. set) panel meter between the analog output of the capacitance meter via panel switches, and the top of the capacitance ratio incremental voltage divider. Adjust the cap. set potentiometers to obtain zero on the panel meter. Switch back to the test position and allow the tester to run by switching the (run-reset) switch to run. The arm or the capacitance ratio divider goes to one of the comparator inputs. The analog output of the capacitance meter goes to the other comparator input.

When the test ramp is applied to the sample and the sample and hold, the analog output of the capacitance meter follows the capacitance of the sample. When the analog output reached the pre-determined ratio, the comparator's output triggers the latch which sets the sample and hold circuit in the hold state. This latch output goes to a monostable which triggers the panel meters to take data. The output of the sample and hold goes to two voltage dividers connected to the inputs of the panel meters. The flat-band panel meter is referenced to a bias which also goes to the high bias input on the rear of the capacitance meter.

D. Shift Register Card Comparator and Reset (see Fig. 4)

The avalanche current is set by the range of the electrometer (Keithley 616) and the units chosen on the current incremental divider. The voltage across the divider is designed to be 1.00 volts. The output of the electrometer is one volt at full scale.

The arm of the current divider goes to the inverting input of the comparator (LM 311). The electrometer output goes to the non-inverting input of the comparator. When the electrometer reaches the pre-set current of the divider, the comparator output goes positive.

This output feeds two op-amps (TP1319). One op-amp with a gain of about 8, drives a line driver (74128) wired as a latch. This latch starts the tester by changing the reset potential from about zero to about +5 volts. It also turns off the LED to indicate that the tester is running. The other op-amp is on the avalanche card and its output eventually controls the amplitude of the avalanche voltage.

E. Avalanche Card (see Fig. 5)

The comparator output from the shift register card goes into the inverting input of the low drift op-amp (TP1319). Turn on the avalanche switch. The (TP1319) output goes in a negative direction when the avalanche current is reached and in a less negative direction when more avalanche current is required to balance the comparator's inputs.

To set the amplitude of the avalanche voltage, lift the probe off the sample and switch Cx out of the circuit with the avalanche switch on. While observing the avalanche voltage on an oscilloscope, adjust Rx and the function generator output to get maximum amplitude without distortion. Switch Cx back into the circuit and turn off the avalanche switch. When the avalanche voltage reaches zero, put the probe back on sample and turn the avalanche switch on.

The DC level from (TP1319) passes through one of the relays operated by shift register output pin 4, and then charges capacitor Cx through a very large time constant. The voltage on the capacitor, in conjunction with the 50 KHz saw-tooth, is applied to the non-inverting input of an FET op-amp (LH0062D). The output of this op-amp feeds into a special high voltage, high speed FET op-amp (model 1801 manufactured by Dynamic Measurements Corporation). The power supplies used to generate the + and − 63 volts used by the 1801 are two ± 24 volt and one ± 15 volt supplies, connected in series. The output of the 1801 is DC restored to −5.6 volts to drive the sample into accumulation on every cycle and thus stop the minority carrier build-up. This output goes to the relay at the probe and through a diode and divider to the avalanche panel meter via the panel switch (S2-B-2).

The other relay on this card operated by shift register output pin 4, disconnects the 50 KHz saw-tooth when a flat-band measurement is being taken. The same shift register output which operates the relays also gates the timer off by use of the NAND circuit (7400).

F. Tester Panel Circuitry (see Fig. 6)

This circuitry consists mostly of switches to change modes of operation and bias condition for the sample.

Switch S2 is called (aval test - cap. set). In cap. set, this switch places a -10.2 volt bias on the sample gate for p-type and drives it into accumulation. It also energizes the relays at the probe which connects the capacitance meter to the sample. Procedure for cap. set was described in the sample and hold card description. In the aval test position, a -5.1 volt bias is applied to the gate of a p-type sample. This enables the flat-band test ramp to start at -5.1 volts instead of zero.

Switch S1 is called (ramp voltage) and it adjusts the test ramp amplitude to -5 volts, -10 volts and -18 volts in three steps. S1 also changes the -5.1 bias mentioned above to about -2.5 for the -5 volt ramp (thin oxide mode).

Switch S4 is the bias switch to extend the usefulness of the test ramp. In the normal position (N) there is -5.1 or -2.5 volts of bias. The other bias voltages are 0, $+5$, -10.2. An automatic bias tracking circuit has been developed and can easily be added to the tester. This eliminates the need of switching in different bias voltages.

Switch S3 is called (x-y recorder-tester). In the x-y recorder position a 1 with the tester reset, an initial capacitance vs. voltage (C-V) plot can be taken. In this position, the analog output of the capacitance meter is switched to the 'y' input of the x-y recorder. The high bias of the capacitance meter is switched to the 'x' input of the x-y recorder. After the C-V plot is taken, this switch is returned to the tester position.

G. Probe Circuitry (see Fig. 7)

The relays at the probe are normally de-energized and in the avalanche position. With a sample on the probe station, the avalanche saw-tooth passes through one relay to a teflon reversing switch. The switch position is chosen by the wafer type (n or p). In the case of the 'p-type' substrate, the saw-tooth is applied to the aluminum gate contact over the SiO_2. The substrate is connected through the teflon switch to the arm of the second relay. The normally closed contact has a filter with a special time constant connected between it and the input to the electrometer. The time constant is chosen to slow down the electrometer so that the servo feedback which controls the avalanche amplitude does not oscillate.

Timer Pin Connections

DIGIT	TIMER OUTPUT PINS	CONNECTOR PINS	DEVICE COUPLER PINS	NOTES
(10,000)	3	1	1	
	2	2	2	
	1	3	3	
	4	4	4	
1000	3	5	5	
	2	6	6	
	1	7	7	
	4	8	8	
100	3	9	9	
	2	10	10	
	1	11	11	
	4	12	12	
10	3	13	13	
	2	14	14	
	1	15	15	
	4	16	16	
1	3	17	17	
	2	18	18	
	1	19	19	
	4	20	20	
		58	58	Control pulse from shift reg. to device coupler

Flat-Band Panel Meter Pin Connections

Digit Name	Datel Meter Output Pins	Connector Pins	Device Coupler Pins	Notes
Polarity	A16	4	4	Pins 1,2,3, Grounded
Bit 10,000 out	A15	8	8	Pins 5,6,7 Grounded
Bit 8,000	A17	9	9	
Bit 4,000	B17	10	10	
Bit 2,000	B16	11	11	
Bit 1,000	B15	12	12	
Bit 800	B14	13	13	
Bit 400	B13	14	14	
Bit 200	B12	15	15	
Bit 100	B11	16	16	
Bit 80	B10	17	17	
Bit 40	B9	18	18	
Bit 20	B8	19	19	
Bit 10	B7	20	20	
Bit 8	B6	21	21	
Bit 4	B5	22	22	
Bit 2	B4	23	23	
Bit 1	B3	24	24	
		53	53	Ground

Instruments Needed for the Tester

1 Boonton Digital Capacitance Meter Model 72BD-03 with the 100 mV option (≈ cost $1,600.00).

1 Keithley Digital Electrometer Model 616 (≈ cost $1,500.00) and 1 triaxial to coaxial UHF adapter Model 6013 (or 6012) $60.00.

1 H.P. Function Generator Model 3310A

3 Datel Panel Meters (4 1/2 digits) Model DM-4000 B6. These meters employ a differential, optically isolated floating input (necessary for the flat-band meter. ≈ cost $320.00 each).

Some Special Parts Needed

1. Some type of probe set-up is required. We use a DR-100 test station made by Dumas Instrument Company [≈ cost $265.00]. The supplier is Semimetals Inc., Mountain View, California 94040.

4 Mercury wetted contact relays Model 7210-ic-05K made by 5th Dimension, Inc. Princeton, NJ 08540 ($41.00).

2 Teflon switches, ordered from Kay Electronics, Pine Brook, NJ 07058 ($10.00).

2 Incremental voltage dividers made by EECO. The distributor is Marshall Industries located at 230 Sherwood Industrial Park, Farmingdale, NY (≈ $55.00).

1 1801 High voltage, high speed FET op-amp by Dynamic Measurements Corp., 6 Lowell Avenue, Winchester, Massachusetts 01890.

Avalanche Tester Operating Instructions

1. Turn on power.

2. Put Run-Reset switch in the Reset position and push reset button.

3. Put Run-Reset switch in Run position.

4. Set the tester for a 10-second time interval and let it run. This will automatically set all the latches for proper operation.

5. Make sure the switches on the front panel are in the following positions:
   S1 - Ramp voltage switch set for 10 V, very thin oxides switch to 5 V.
   S2 - Aval. test - Cap. Set switch set to Aval. Test
   S3 - X-Y recorder - Test switch set to Test
   S4 - Bias to extend ramp switch set to N position. Capitor Cx switched in and the avalanche switch must be off.

6. Put the Run-Reset switch to reset. This should reset tester.

7. Check to see that the aval capacitor (Cx) is discharged by observing the reading on the (cap. set - aval) meter with the fast time constant switch set for fast time constant. If the capacitor is not discharged, you will see the voltage increase to a peak value ($\approx$ 100 volts) and then return to a minimum ($\approx$ .7 to 1 volt).

8. If a capacitance vs. voltage plot is required, reset tester and put (x-y Recorder - Test) switch in (x-y Recorder) position.

9. Place sample on probe assembly and put switch on probe assembly in proper position depending on sample type ('p' or 'n').

10. Set up x-y Recorder and make a capacitance vs. voltage plot. Turn off x-y recorder.

11. Return (x-y Recorder) switch to test position.

12. Put the (Aval. Test - Cap. Set) switch in the Cap. Set position.

13. Adjust the Cap. Set potentiometer to obtain zero on the (Cap. Set - Aval) meter. (Record the Cap. on the Cap. Meter).

14. Return the (Aval. Test - Cap. Set) switch to the Aval. Test position.

15. Set the capacitance ratio on the thumbpot. Determine ratio from oxide thickness and resistivity.

16. Set the current you wish to avalanche at, on the thumbpot and and the electrometer range switch.

17. Set the time interval switch to 10 seconds.

18. Place the Run-Reset switch in the Run position.

19. Set up 5100 for testing or sign on terminal. (See attached sheets).

20. After the initial flat-band voltage is printed out, place the Run-Reset switch to Reset and push the Reset button.

21. Set the time interval switch to 20 seconds.

22. Type in TMAX in seconds (no comma).

23. Turn on avalanche voltage (50 KHz ramp).

24. Record avalanche voltage when current is reached.

Testing With the 5100 Computer

1. Turn on the 5100 Computer.

2. Place sample on probe and adjust the avalanche tester to perform the desired test.

3. Insert the data tape into the 5100 Computer.

4. Rewind the data tape by pressing the command button and the rewind button at the same time. Then hit execute.

5. Check what is stored on the data tape by typing)LIB and then hit execute. (Hit execute after each of the commands following).

6. If what is stored on the tape is no longer needed, type)DROP 2 as an example of clearing Library No. 2.

7. Take off the data tape and load the serial I/O tape.

8. Check to see that the serial I/O tape is on safe.

9. Type)MODE COM (when the display calls for options, press number 6). When tape has transferred all information, take it off the 5100.

10. Load the 3 dec tape on the 5100 Computer by typing)COPY 3 DEC. This tape contains programs needed for testing with the device coupler.
    When completed, take the tape off and re-insert the data tape.

11. To start to test, type RUN.

12. Supply information as requested on the display (e.g. ID, LIB No., etc).

13. After supplying all the parameters, hit execute and the program will take six initial flat-band measurements and print out the average value.

14. Reset the tester and type in the TMAX (e.g. 3000) = 3000 seconds. Hit execute.

15. Turn on avalanche switch. When current reaches pre-set value, tester will begin taking data. (Run will end at TMAX or by holding in disconnect button).

To Transfer Data from Tape to the Host
168T Computer Using the 5100

1. After storing data on tape, take out the data tape and press restart on the 5100 Computer.

2. Load the communication tape and type)MODE COM.

3. After the tape stops, enter number 1.

4. When the display says 'HOME', take out the communication tape and reload the data tape.

5. Type in &RATE 300 (& is gotten by pressing command and No. 1 simultaneously).

6. Sign on the 168T computer high speed line Type I CMS, then APLCMS. When the display says 'put on APL ball', you type in the following:

7. &SYSTEM APL; Hit execute.

8. Hit execute again.

9.)LOAD AVAL2; Hit execute.

10. EXPDATA ← 1 0

11. &OPEN IN LIB. NO.; Hit execute.

12. RFILE

13. &TAPEIN

14. When data is transferred, display will say 'DONE'. At this point ***YOU MUST HIT EXECUTE***.

15. &CLOSE; Hit execute.

16. RUNTSAVE; Hit execute – Display will ask for Identification Name.

17. ULTRADRY MAR 2001; Hit execute. (Type name of run - e.g. ULTRADRY MAR 2001).

18. Check for storage in 168T by typing FETCH.

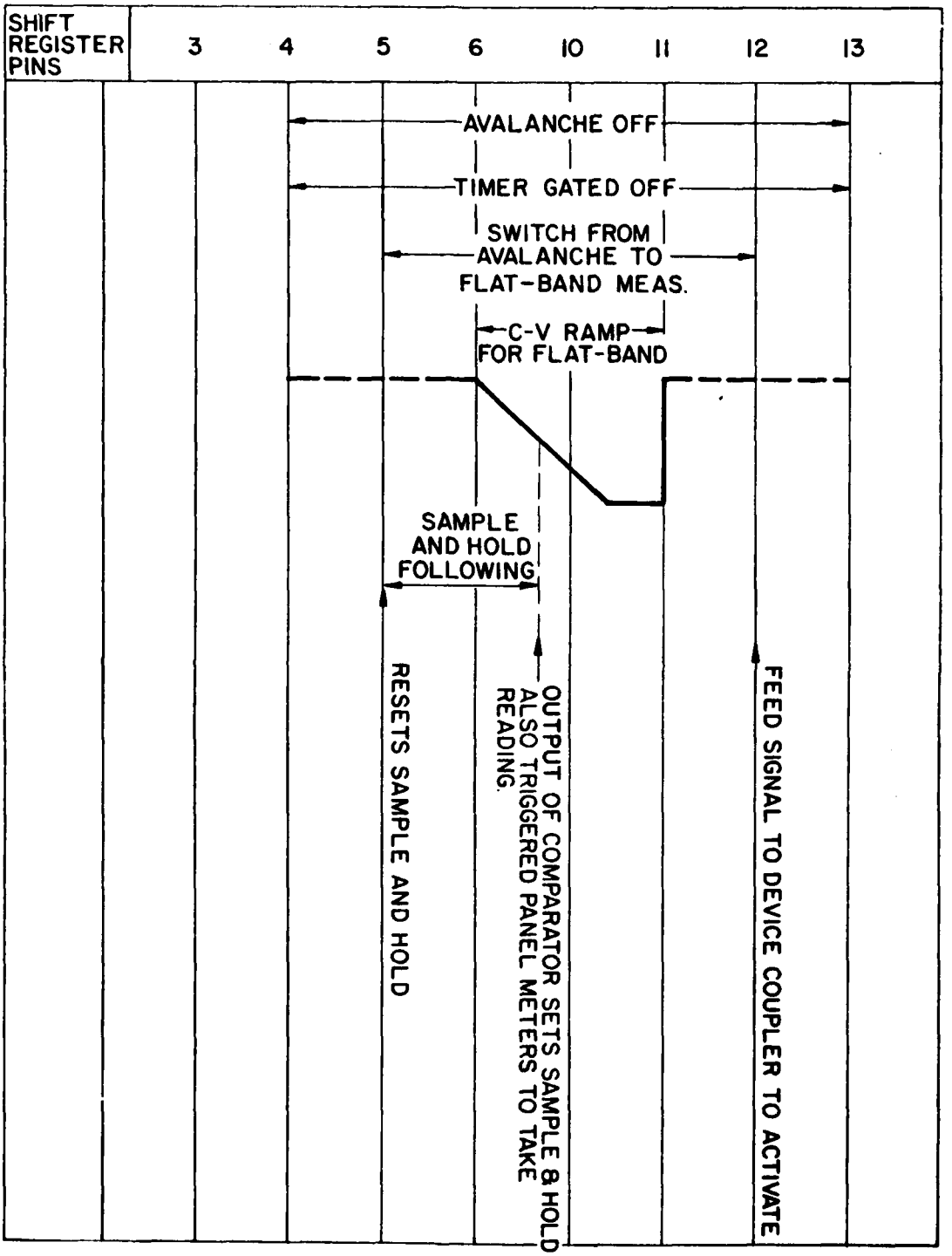

SHIFT REGISTER PINS
3
4
5
6
10
11
12
13
AVALANCHE OFF
TIMER GATED OFF
SWITCH FROM AVALANCHE TO FLAT-BAND MEAS.
C-V RAMP FOR FLAT-BAND
SAMPLE AND HOLD FOLLOWING
RESETS SAMPLE AND HOLD
OUTPUT OF COMPARATOR SETS SAMPLE & HOLD ALSO TRIGGERED PANEL METERS TO TAKE READING.
FEED SIGNAL TO DEVICE COUPLER TO ACTIVATE

FIGURE 1.

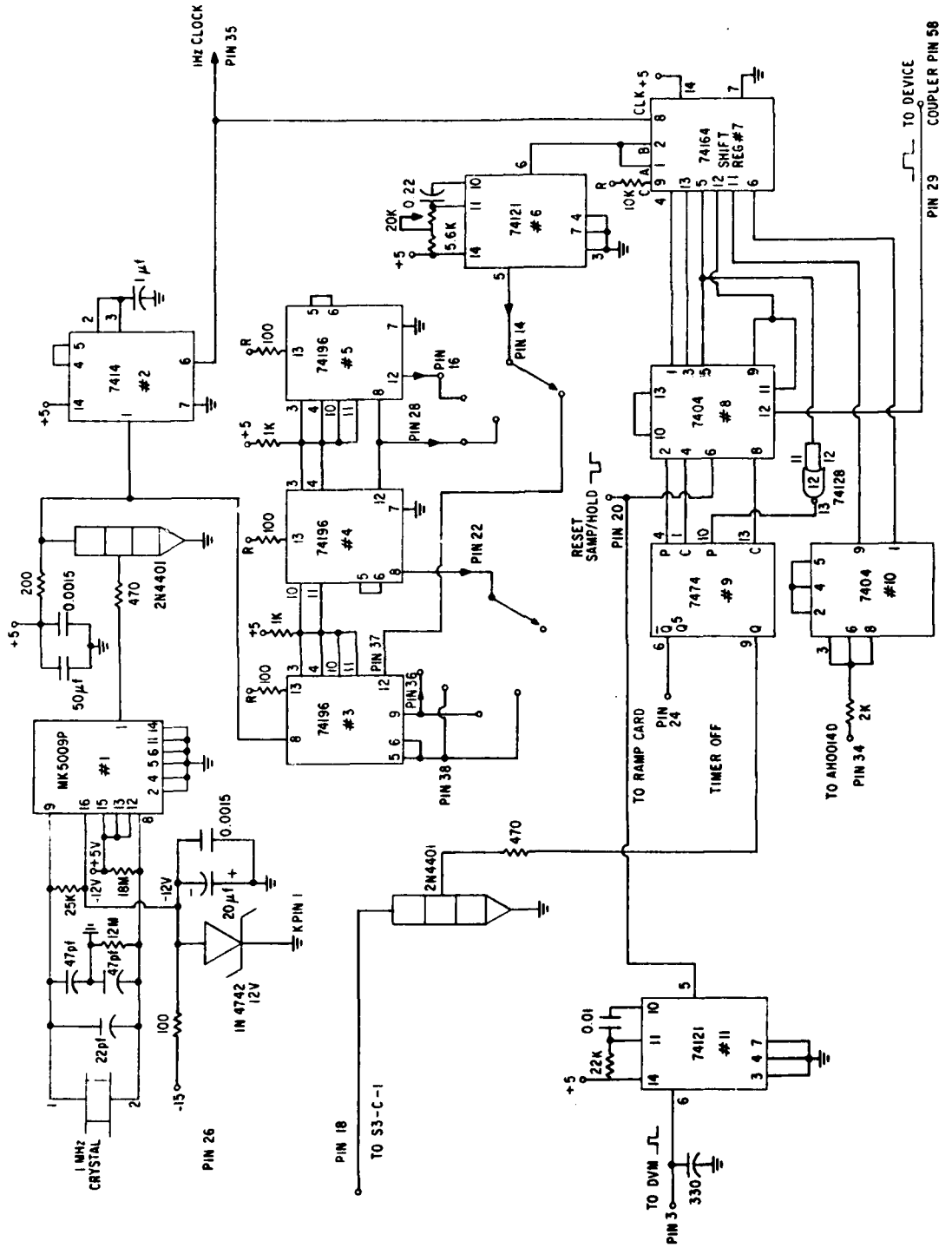

1Hz CLOCK
PIN 35
TO DEVICE
COUPLER PIN 58
PIN 29
CLK+5
74164
SHIFT
REG#7
74121
#6
20K
5.6K
0.22
10K
R
+5
PIN 14
7414
#2
1 µf
74196
#5
100
1K
PIN 16
PIN 28
74196
#4
PIN 22
74196
#3
PIN 37
PIN 36
PIN 38
7404
#8
74128
RESET
SAMP/HOLD
PIN 20
7474
#9
TO RAMP CARD
PIN 24
TIMER OFF
7404
#10
TO AH0014D
PIN 34
2K
MK5009P
#1
200
0.0015
470
2N4401
50µf
25K
18M
-12V
+5V
47pf
12M
22pf
1 MHz
CRYSTAL
PIN 26
100
-15
-12V
20µf
0.0015
IN 4742
12V
KPIN 1
2N4401
470
PIN 18
TO S3-C-1
74121
#11
22K
0.01
TO DVM
PIN 3
330

FIGURE 2.

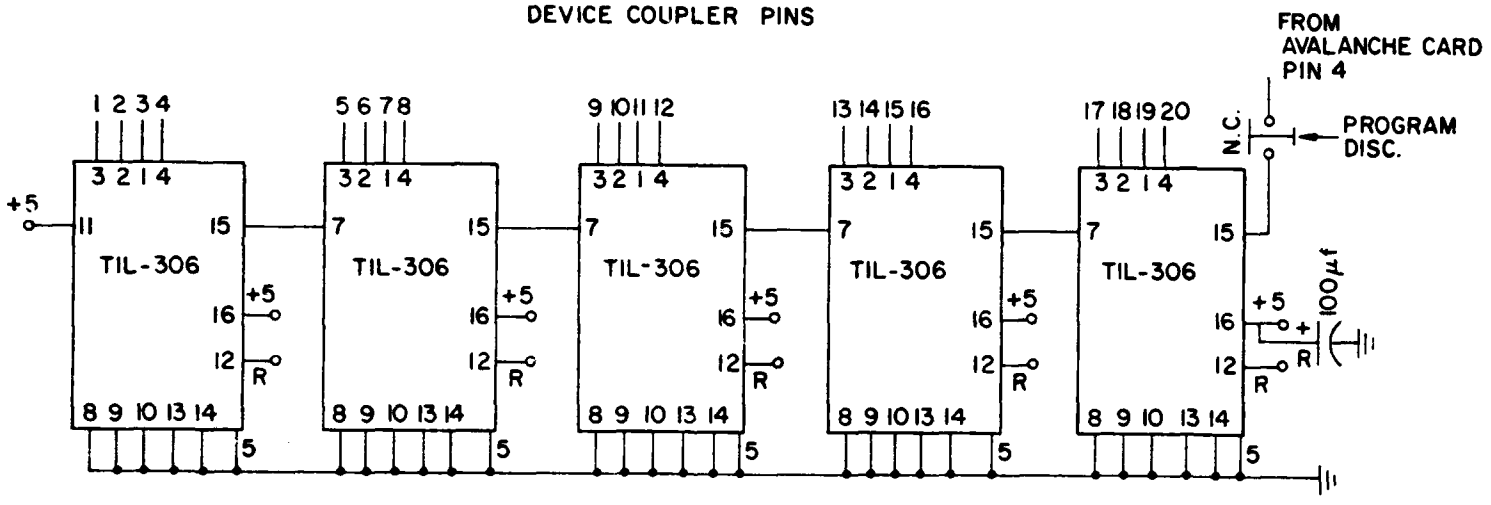

DEVICE COUPLER PINS
FROM AVALANCHE CARD PIN 4
PROGRAM DISC.
N.C.
1 2 3 4
5 6 7 8
9 10 11 12
13 14 15 16
17 18 19 20
3 2 1 4
+5
11
15
7
16
12
R
TIL-306
8 9 10 13 14
5
100μf

FIGURE 2A.

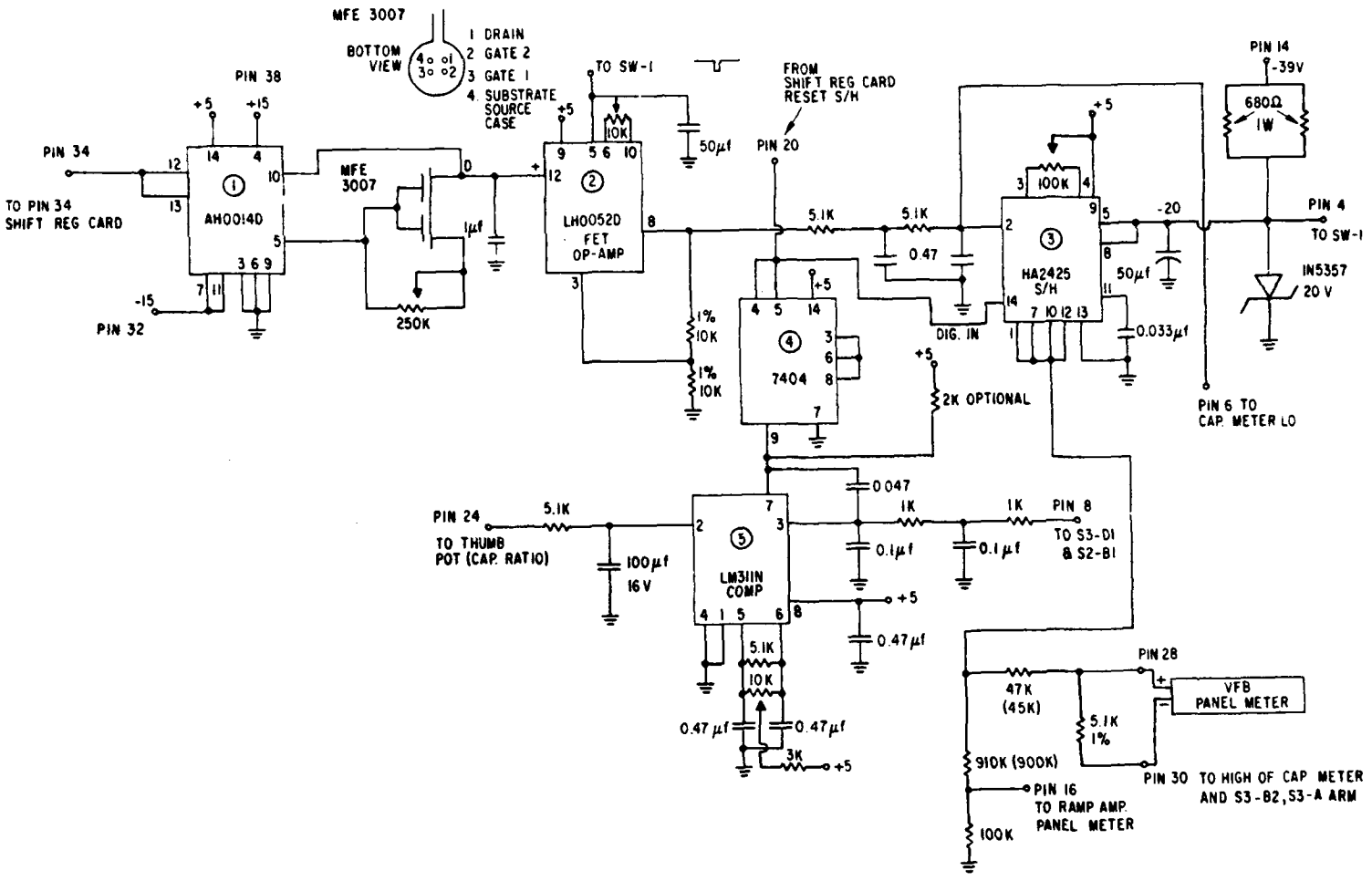

MFE 3007
BOTTOM VIEW
1 DRAIN
2 GATE 2
3 GATE 1
4 SUBSTRATE SOURCE CASE
TO SW-1
FROM SHIFT REG CARD RESET S/H
PIN 14
-39V
PIN 38
+5
+15
PIN 34
TO PIN 34 SHIFT REG CARD
AH0014D
MFE 3007
1µf
250K
-15
PIN 32
LH0052D FET OP-AMP
10K
50µf
PIN 20
5.1K
0.47
HA2425 S/H
100K
680Ω 1W
-20
50µf
PIN 4
TO SW-1
IN5357 20 V
DIG. IN
0.033µf
PIN 6 TO CAP. METER LO
1% 10K
1% 10K
7404
2K OPTIONAL
PIN 24
TO THUMB POT (CAP. RATIO)
5.1K
100µf 16V
LM311N COMP
0.047
1K
0.1µf
PIN 8
TO S3-D1 & S2-B1
0.47µf
PIN 28
47K (45K)
VFB PANEL METER
5.1K 1%
910K (900K)
PIN 16 TO RAMP AMP. PANEL METER
PIN 30 TO HIGH OF CAP METER AND S3-B2, S3-A ARM
100K
3K

FIGURE 3.

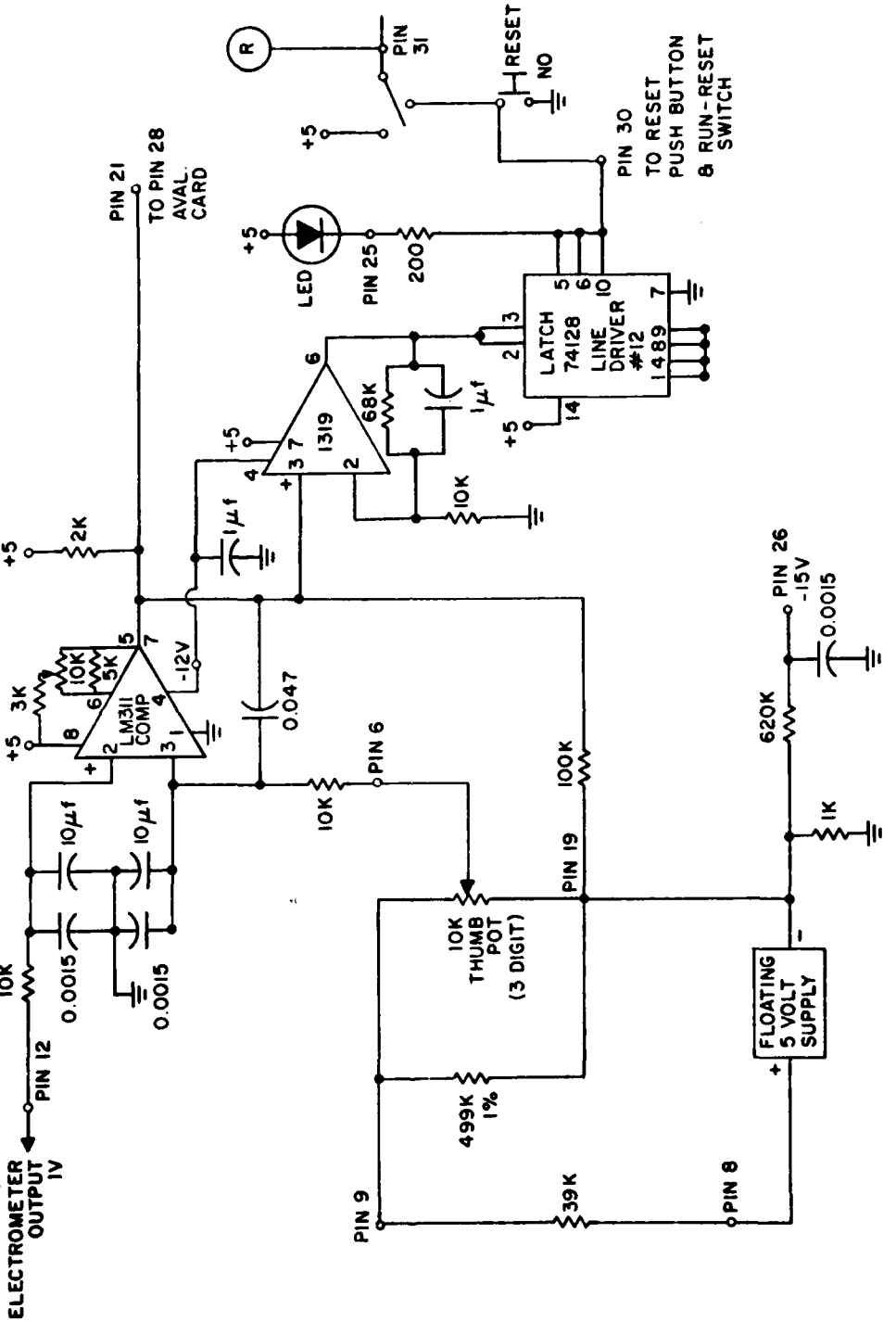

R
PIN 31
RESET
NO
+5
PIN 30
TO RESET
PUSH BUTTON
& RUN-RESET
SWITCH
PIN 21
TO PIN 28
AVAL.
CARD
LED
PIN 25
200
LATCH
7412B
LINE
DRIVER
#12
1489
1319
68K
1µf
10K
+5
2K
1µf
0.047
LM311
COMP
10K
5K
3K
-12V
PIN 6
10K
100K
PIN 19
10µf
10µf
0.0015
0.0015
10K
10K
THUMB
POT
(3 DIGIT)
499K
1%
39K
PIN 9
PIN 8
PIN 26
-15V
0.0015
620K
1K
FLOATING
5 VOLT
SUPPLY
PIN 12
616
ELECTROMETER
OUTPUT
1V

FIGURE 4.

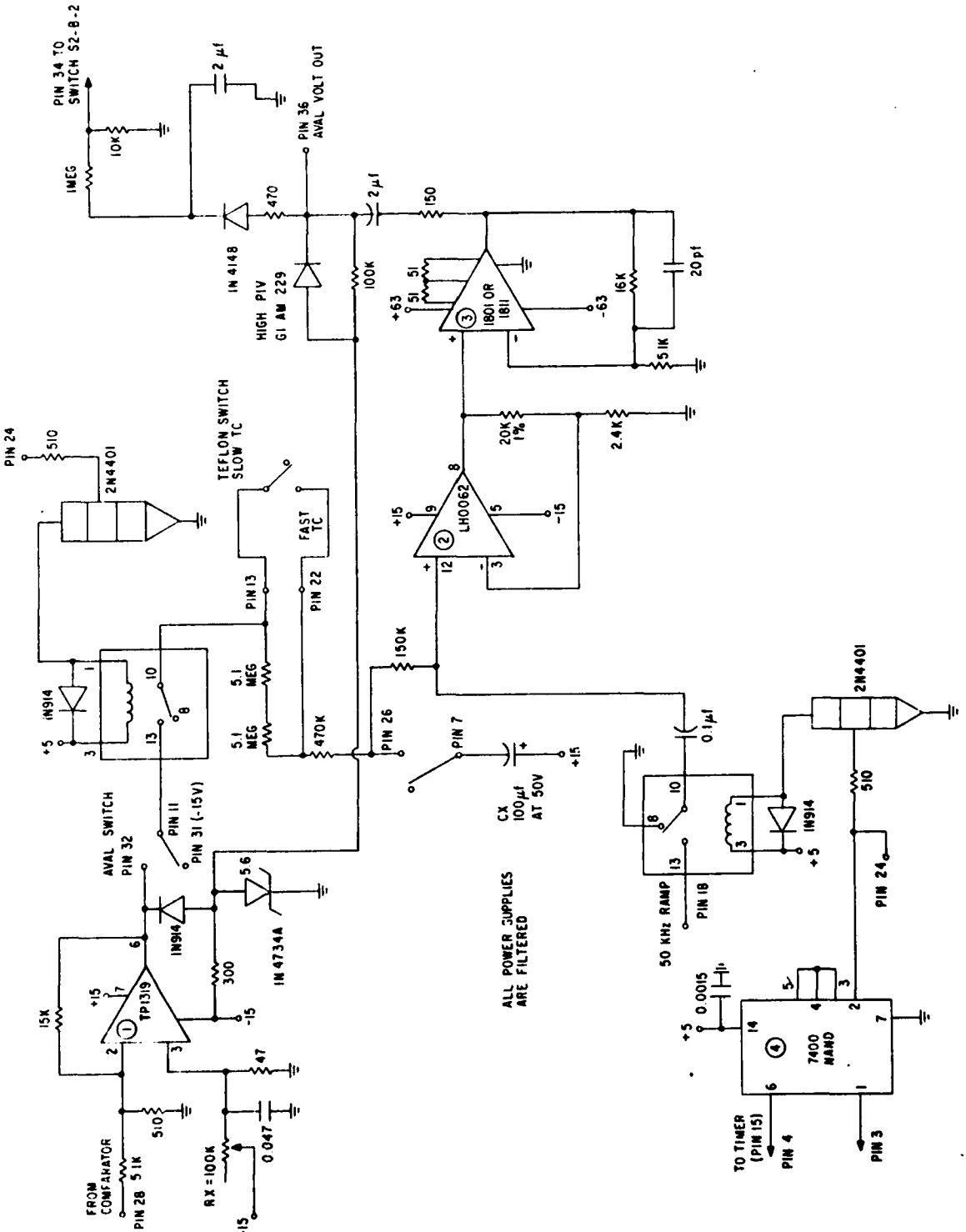
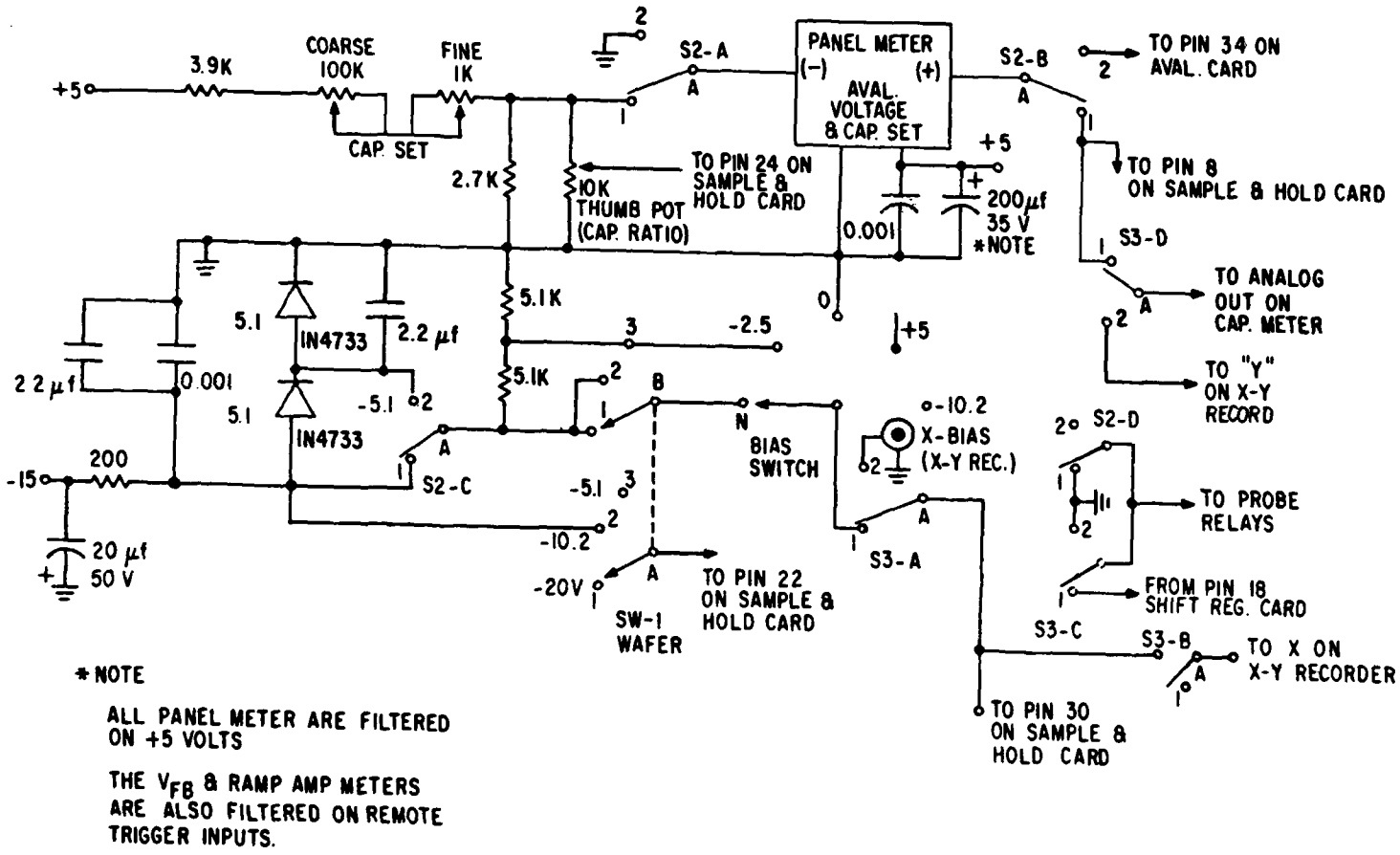

PIN 34 TO SWITCH S2-B-2
10K
1MEG
2 µf
PIN 36 AVAL VOLT OUT
470
IN 4148
HIGH PIV G1 AM 229
2 µf
150
100K
+63
51
51
1801 OR 1811
-63
16K
20 pf
5 1K
20K 1%
2.4K
PIN 24
510
2N4401
TEFLON SWITCH SLOW TC
FAST TC
LH0062
+15
-15
PIN 13
PIN 22
IN914
+5
5.1 MEG
5.1 MEG
470K
150K
PIN 26
PIN 7
CX 100µf AT 50V
+15
0.1µf
AVAL SWITCH PIN 32
PIN 11
PIN 31 (-15V)
5.6
IN914
IN 4734A
300
15K
TP1319
+15
-15
47
510
0.047
FROM COMPARATOR PIN 28 5 1K
RX = 100K
+15
ALL POWER SUPPLIES ARE FILTERED
50 KHz RAMP
PIN 18
IN914
+5
2N4401
510
PIN 24
0.0015
+5
7400 NAND
TO TIMER (PIN 15)
PIN 4
PIN 3

FIGURE 5.



*NOTE

ALL PANEL METER ARE FILTERED ON +5 VOLTS

THE V_{FB} & RAMP AMP METERS ARE ALSO FILTERED ON REMOTE TRIGGER INPUTS.

FIGURE 6.

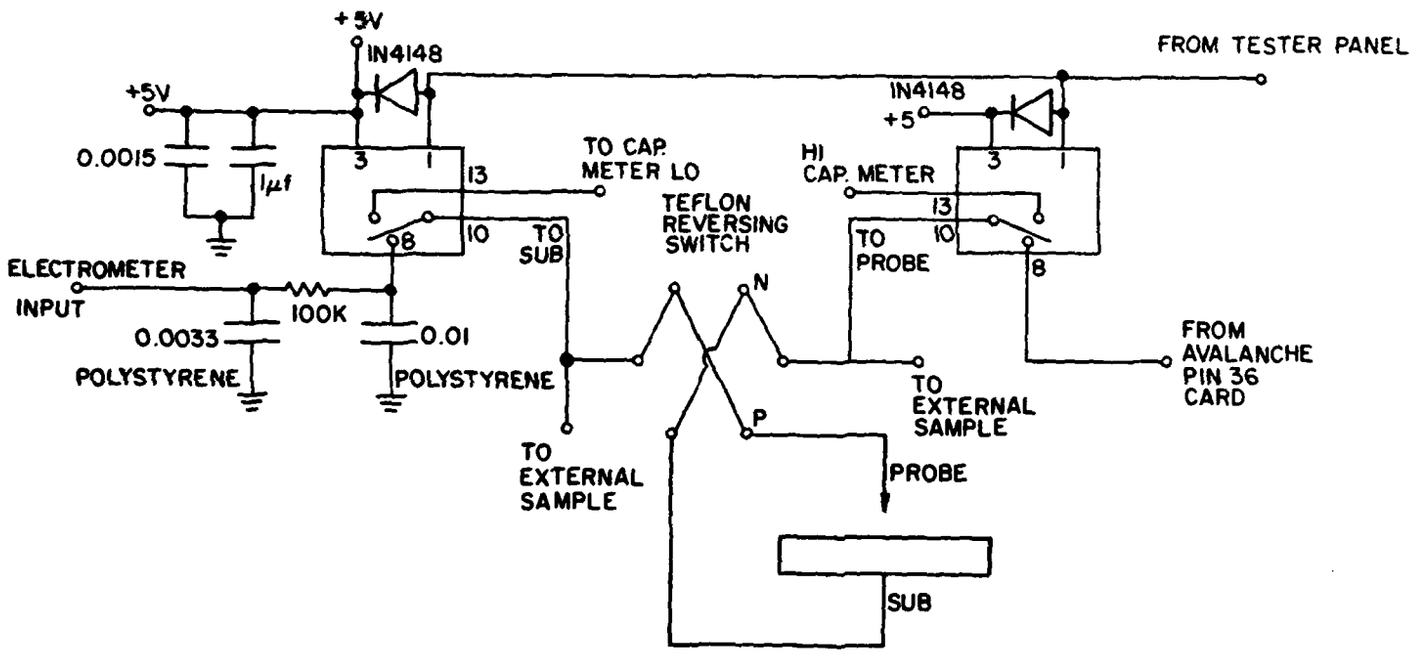

+5V
IN4148
FROM TESTER PANEL
+5V
0.0015
1μf
3
1
13
TO CAP.
METER LO
IN4148
+5
HI
CAP. METER
3
1
13
TEFLON
REVERSING
SWITCH
8
10
TO
SUB
TO
PROBE
10
8
ELECTROMETER
INPUT
100K
N
0.0033
POLYSTYRENE
0.01
POLYSTYRENE
FROM
AVALANCHE
PIN 36
CARD
TO
EXTERNAL
SAMPLE
P
TO
EXTERNAL
SAMPLE
PROBE
SUB

FIGURE 7.

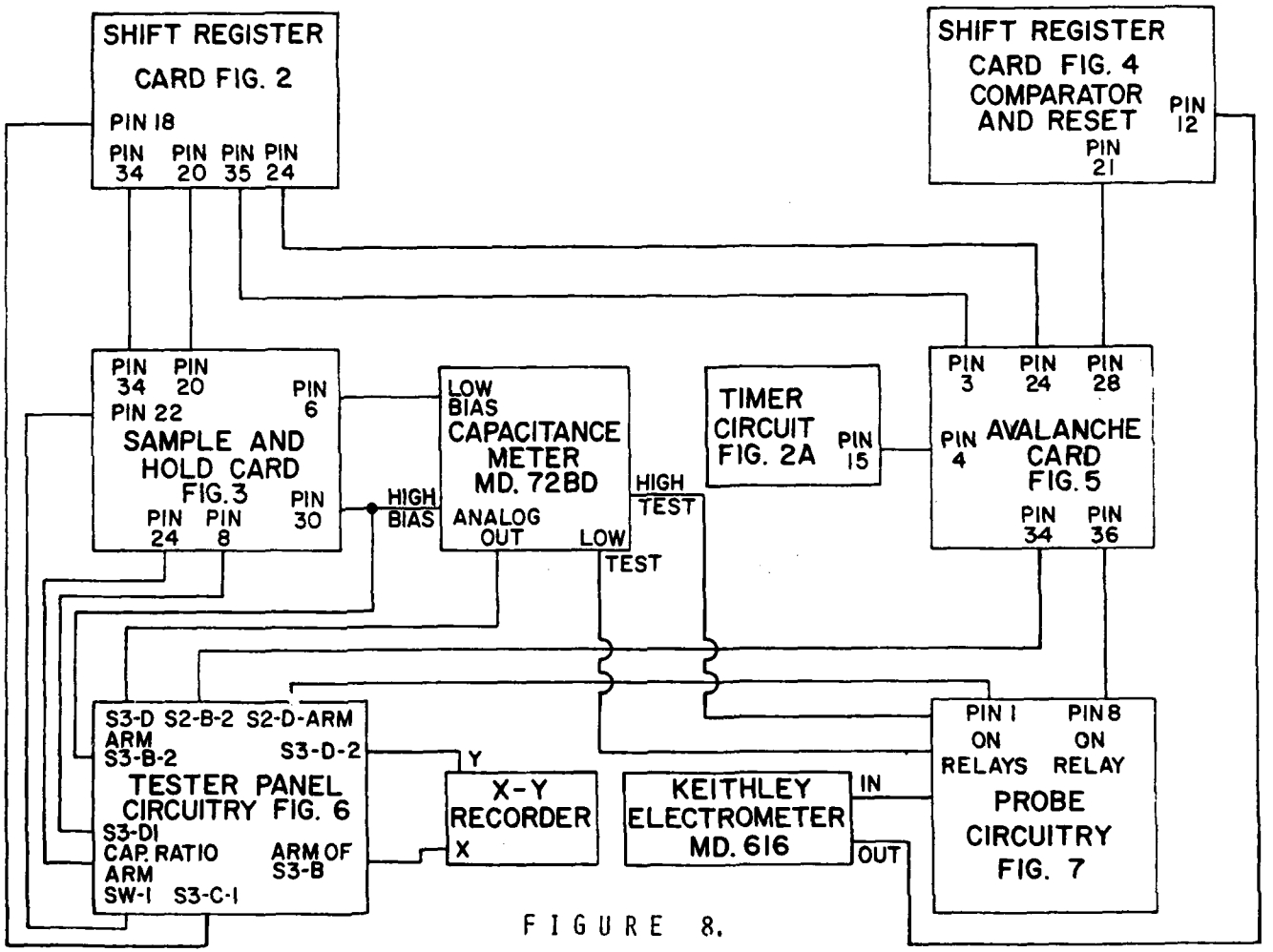

SHIFT REGISTER
CARD FIG. 2
PIN 18
PIN 34
PIN 20
PIN 35
PIN 24
SHIFT REGISTER
CARD FIG. 4
COMPARATOR
AND RESET
PIN 12
PIN 21
PIN 34
PIN 20
PIN 22
PIN 6
SAMPLE AND
HOLD CARD
FIG. 3
PIN 24
PIN 8
PIN 30
HIGH
BIAS
LOW
BIAS
CAPACITANCE
METER
MD. 72BD
ANALOG
OUT
LOW
HIGH
TEST
TEST
TIMER
CIRCUIT
FIG. 2A
PIN 15
PIN 3
PIN 24
PIN 28
PIN 4
AVALANCHE
CARD
FIG. 5
PIN 34
PIN 36
S3-D
S2-B-2
S2-D-ARM
ARM
S3-B-2
S3-D-2
TESTER PANEL
CIRCUITRY FIG. 6
S3-DI
CAP. RATIO
ARM
SW-1
S3-C-1
ARM OF
S3-B
Y
X
X-Y
RECORDER
KEITHLEY
ELECTROMETER
MD. 616
IN
OUT
PIN 1
ON
RELAYS
PIN 8
ON
RELAY
PROBE
CIRCUITRY
FIG. 7

FIGURE 8.

MISSION
of
Rome Air Development Center

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