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CCD ANALOG PROGRAMMABLE MICROPROCESSOR (APUP) STUDY

Westinghouse Electric Corporation

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) A cross-correlation of radar signal processing needs and CCD-compatible analog signal processing devices yielded a functional partitioning into several distinct candidates primarily on the basis of data storage time and data format. The azimuth processing function clearly preferred for implementation has two alternate architectures: the discrete correlation transform versus the two part combination of a "corner-turn memory" plus a transversal filter. The greater flexibility of the correlation (Cont'd)			

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Transform scheme translates immediately into greater user acceptance, larger markets, and lower costs. The details of the transform/filter APUP candidate are given, including an ingenious new application of the traditional push/pull scheme to cancel even-harmonic distortion as well as offset fixed pattern noise arising from nonuniformities in thermal leakage or FET threshold. Also incorporated is a new additive refresh technique aimed at maintaining sample-to-sample isolation during multiple recirculations. Mixed technology circuitry combining the best features of MOS and bipolar transistors is recommended in order to obtain, with minimum active area, both wide-band low-noise analog buffers and fast, low-power, driver-translators. The resultant fast-settling MDAC is even further facilitated via the very light loading of CCD input gates. The projected performance falls in the 55dB to 60dB range for all the following parameters: peak signal to temporal noise, peak signal to RMS harmonic distortion, sample to sample isolation and sidelobe rejection, all at a rate of ten million filter outputs per second using less than 0.65 watts in a chip less than one quarter inch square having an analog memory of 18,432 stages.

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PREFACE

This Final Report was prepared by the Advanced Technology Laboratories of the Westinghouse Electric Corporation, Baltimore, Maryland under Contract No. F30602-78-R-0315. It describes work performed from 21 September 1978 to 15 October 1979 in the Solid State Technology Section, Dr. W.S. Corak, Manager. The Program Manager and Technical Director was Dr. Donald R. Lampe. Other members of the technical staff who contributed to the program were S.J. Mederer, A.R. Gedance, J. Mattern, I.A. Mack, E.H. Naviasky, R.J. Wiegand and J.D. Fogarty. The Air Force Technical Monitor was W. Simkins of RADC.

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EVALUATION

Charged Coupled Device (CCD) technology has promised the possibility of low cost, low power signal processing modules for several years. With recent breakthroughs in architecture and the progressive maturation of fabrication techniques, the technology may, at last, have overcome two obstructions to field implementation: temperature sensitivity and inflexible architecture. Devices currently being developed offer 40 to 60 dB of dynamic range, 1 to 20 MHz of bandwidth, and can be programmed or reconfigured by a microprocessor. This effort reviewed the functions performed by radar processors and tried to identify the minimum number of programmable CCD architectures required to perform those functions. This set of Analog Programmable Microprocessors (APuP) candidates were then reviewed for usefulness and current development. This effort chose, as most useful, a device with a reconfigurable architecture which can operate as a second order recursive filter, a multiply and sum transform processor, or a high speed buffer memory.

This device is currently being developed in a subsequent procurement and will have applications in on-board processing for airborne, ground based tactical, and other portable radar systems. This work is in support of TPO R4B.

William Simkins
WILLIAM SIMKINS
Project Engineer

1.0 INTRODUCTION

1.1 The Objective

An attractive concept for obtaining low cost and high performance in radar systems is the use of programmable signal processing modules. Using large quantities of the same module (or the same modules for many functions) allows high production and, thereby, lower cost per module. Programmability allows not only flexibility in operations but graceful degradation since the working modules can be programmed to compensate for a failing module. Furthermore, the analog nature of charge-coupled devices (CCD's) gives the prospect of a small-area, low-power, cost-effective alternative to the various digital technologies. But CCD technology has not yet matured to the point where it has achieved widespread acceptance into the hostile environments of military systems. Therefore, the objective of the study is to determine the feasibility and limitations of a CCD ANALOG microprocessor for use as a programmable radar signal processor.

1.2 The Problem

In view of the above objective, an analog programmable microprocessor (APUP) must now be defined. The traditional digital microprocessor consists predominately of some form of programmable digital logic array capable of executing a variety of operations on digital data in accord with an instruction word which sets configuration control switches so as to carry out such aforesaid operations as add, multiply, shift right/left, store, etc. Such simple instructions can then be combined into a sequential list, sometimes called "code", fully describing the sequential "reconfigurations" experienced by the digital microprocessor in response to the instruction words as it performs the computations needed for radar signal processing. With

this as a reference "benchmark", the analog microprocessor is more easily described.

The analog programmable microprocessor (APUP) consists of an array of analog signal processing elements such as memory, multipliers, summers, etc. which can be variously interconnected in response to an instruction or configuration command word. For example, the appropriate instruction word could configure the APUP as a full Doppler transformer or as a general canonic second-order filter, over a wide range of memory lengths. Thus in the APUP, a single instruction code word replaces all the digital code list needed for the specified radar signal processing function. Like the digital microprocessor, an APUP should be capable of accepting auxiliary digital data (like Doppler transform or filter coefficients) during the computational operation.

With the preceding as an illustrative example, the problem becomes an investigation of possible universally programmable radar signal processing architectures based on CCD-compatible technology. Tradeoffs between performance, functional programmability, device topology, and fabrication problems are considered in projecting the feasibility, limitations, and compromises of implementing such an APUP device or family of devices.

1.3 The Approach

The first step of the APUP study effort was a cross-correlation of radar signal processing techniques and need against CCD and related device characteristics and capabilities. This leads to partitioning the overall signal processing problem on the basis of key device parameters such as data retention time and data format (like serially-adjacent versus periodic, non-serially-adjacent). With several well-defined "partitions" capable of executing nearly all radar signal processing requirements, the next step is to ascertain their relative usage frequency within a typical population of many different kinds of radar systems, thereby yielding a relative ranking of the

several functional partitions.

Focusing on that functional partition most likely to achieve the greatest reduction in equipment, further tradeoffs were required comparing alternate implementations. At this point fine-grain circuit and fabrication details become important, and repeated iterations are needed to define the tradeoffs still left unspecified. Peculiarities of the organization/facility selected for any subsequent APUP development certainly bring unique strengths and weakness to bear on the problem and can thus influence the fine details of the most attractive APUP candidate. Consequently, a facility with a very broad spectrum of capabilities, and technology mixes, was assumed for the relevant parts of the study effort, as well as projecting the likely risks versus payoffs for competing alternatives.

1.4 The Report Outline

The next chapter presents a summary of results of the study effort, followed by two chapters describing the surveys of radar signal processing techniques and charge transfer device (CTD) related analog signal processing techniques done at the outset of the study and leading to the cross-correlation of radar requirements against analog CTD-related elements. This cross-correlation and the derived partitioning are given in chapter five, with the problems of the preferred APUP candidate detailed in chapter six. Chapter seven presents the initial implementation details of the preferred approach.

2. SUMMARY

During this study program, both radar signal processing techniques and charge transfer device (CTD) related analog signal processing elements were surveyed and cross-correlated with the objective of determining the feasibility and limitations of a CTD analog microprocessor for use as a programmable radar signal processor.

Radar signal processing involves data storage, convolutions, correlations, transformations, combination and other arithmetic and logic operations. With regard to CTD analog signal processing, the characteristic data storage time is one of the most sensitive parameters for dividing the overall range of signal processing techniques into reasonably well defined categories:

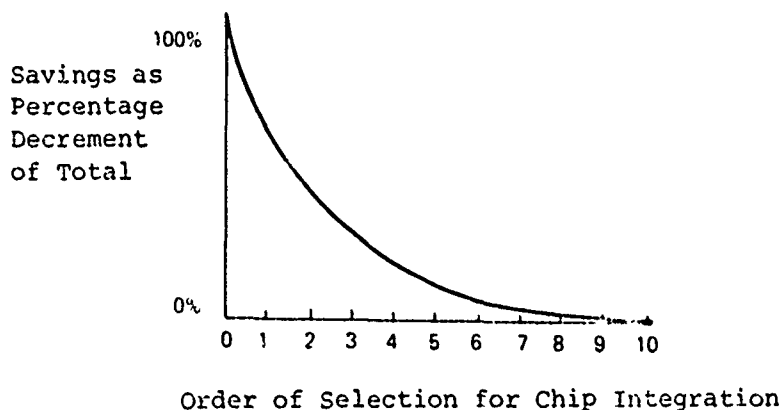
Table 2-1: Primary Analog CCD Radar Signal Processing Categories

<u>Category</u>	<u>Example</u>	<u>Approximate Data Storage Time</u>
1. Range	Pulse Compression	1 microsecond to 1 millisecond
2. Azimuth	MTI, Doppler	1 millisecond to 1 second
3. Scan to Scan	Target Tracking, Clutter Maps	Over 1 second

For the range processing category, the data to be processed occur naturally in serial form and with storage times short enough that this category is a close match for CCD-based processors. For azimuth processing, the data samples involved in the arithmetic transformation do not occur naturally serially but are separated by a full interpulse period (IPP). Thus such a processor's architecture must accommodate both the different data format and the much longer storage time at potentially

elevated (MILSPEC) temperatures. These distinct categories are clearly indicated in Figure 2-1, which has superimposed markings to show those operating regions for which CCD-based signal processors are already available. With the exception of three corner-turn arrays, most such devices transform serially adjacent data samples (like category 1).

The radar surveys, on the other hand, clearly show the dominant computational volume or equipment allocation to be the azimuth processing category as shown in Table 2-2. The relative ranking of the major APUP candidates described therein is intended to correspond to the order of selection for chip integration as indicated in Figure 2-2.



Reduction vs Order of Selection

Figure 2-2

Thus the obviously preferred APUP from the viewpoint of the system user is one to perform azimuth processing. Various architectures and many analog signal processing elements were considered in order to determine if any analog CTD-based chip might prove feasible, cost-effective, and attractive to a large number of users in terms of cost, programmability, and universal applicability.

The joint problems (for azimuth processing) of data format and long data storage times are both addressed by selecting an architecture which provides for more uniform analog memory

TABLE 2-2: THE MAJOR APUP CANDIDATES

<u>DATA FUNCTION/FORMAT</u>	<u>ITEM</u>	<u>RANKING BY SIGNAL PROCESSING QUANTITY</u>
1. LINEAR TRANSFORMATION OF PERIODIC (IPP), NOT SERIAL, SAMPLES	AZIMUTH CORRELATION: MTI, DOPPLER FILTERS (a) general purpose transform/filter architecture (b) corner-turn memory PLUS linear trans- formation of serial data	1
2. LINEAR TRANSFORMATION OF SERIAL DATA SAMPLES	RANGE CORRELATION (PULSE COMPRESSION), CFAR, CENTROIDING, INTERPOLATION	2
3. ANALOG BUFFER MEMORIES	(a) UP TO 1GHZ "FAST WRITE/SLOW READ" BANDWIDTH COMPRESSION, DOUBLE-BUFFERING (b) LONG STORAGE TIME CORNER-TURN ARRAYS.	3
4. ADAPTIVE LINEAR TRANSVERSAL TRANSFORMATION	ADAPTIVE CLUTTER REJECTION FILTERS, ECM- JAMMING REJECTION NOTCH FILTERS, ANTENNA SIDELOBE REJECTION	4
5. SPECIAL PURPOSE FUNCTIONS:	(a) ACOUSTO-OPTIC IMAGE PREPROCESSOR AS FOR SPECTRAL ANALYSIS (b) FLIR deinterlacer/synchronizer	5

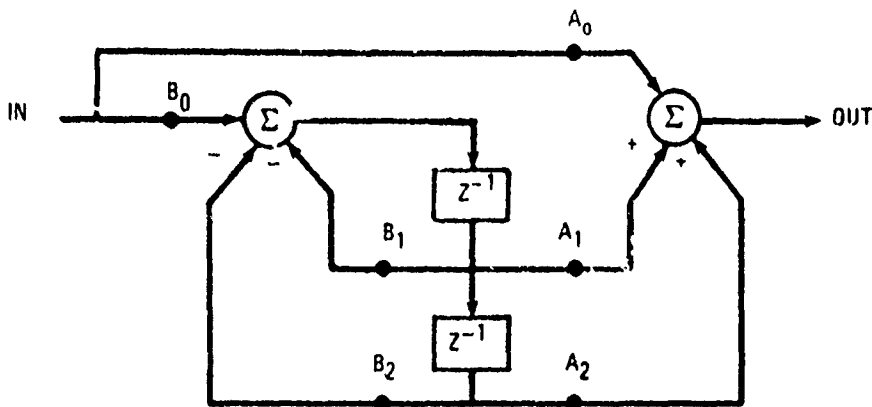
operation than is allowed with the traditional corner-turn approach, as illustrated in figures 2-3 and 2-4, and called the transform/filter APUP. The problems unique to the analog memory and its associated analog circuitry, such as fixed pattern noise, linearity, circuit temporal noise, and cross-talk between analog samples, are then addressed and ingeniously solved by a novel combination of previously documented performance improvement schemes, as in Table 2-3.

Table 2-3: Analog Performance Enhancement

<u>Problem</u>	<u>Solution</u>
<ul style="list-style-type: none"> • Harmonic Distortion • Fixed Pattern Noise from leakage and other offset nonuniformities 	<ul style="list-style-type: none"> • Sequential Push-Pull
<ul style="list-style-type: none"> • Sample-to-Sample Crosstalk 	<ul style="list-style-type: none"> • Additive Refresh
<ul style="list-style-type: none"> • Limited Area, Power • Circuit Temporal Noise 	<ul style="list-style-type: none"> • Selective use of Bipolar/MOS circuitry

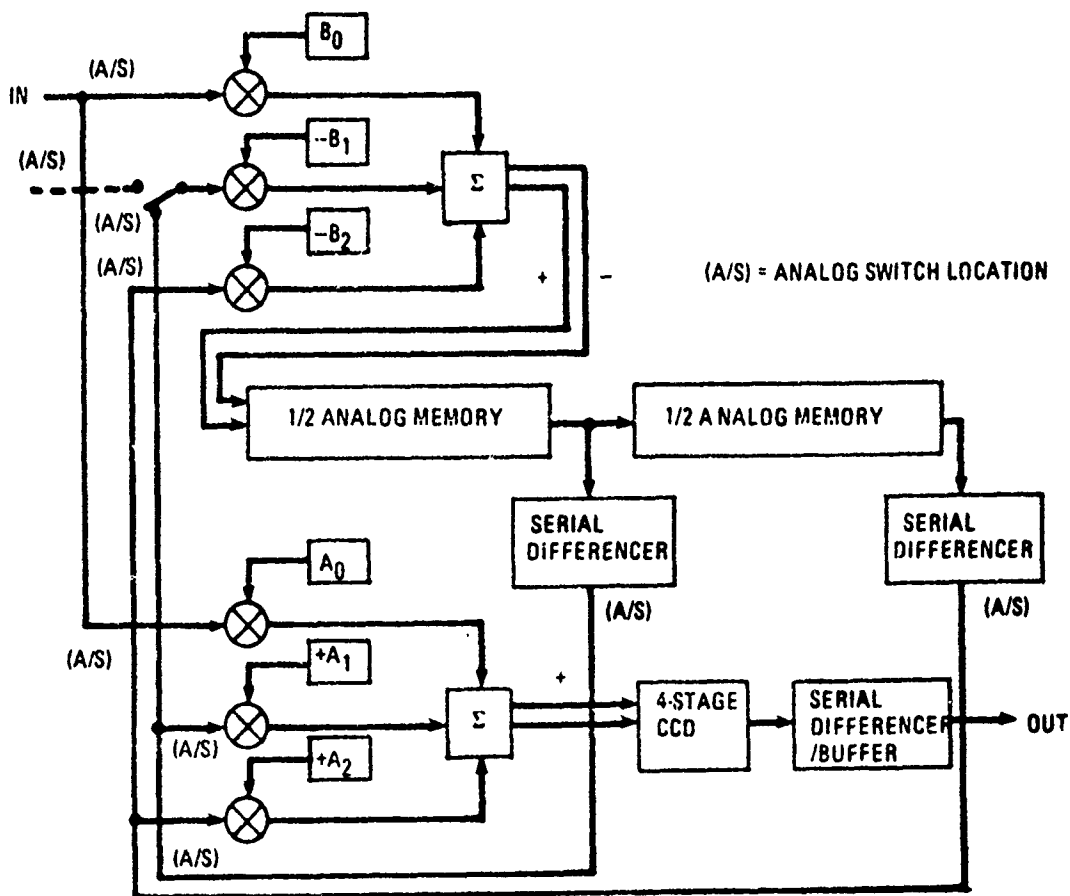
The solutions, in fact, are so effective as to enable the preferred transform/filter APUP to execute complete transform/filter computations at the rate of 10^7 per second or function as a double buffer in the "max. data mode" at a sample rate of 2×10^7 per second with a memory of 16, 320 stages. Moreover, at this signal processing speed, the digital data rate to transport all six multiplier coefficients to their respective MDAC's without greatly increasing the pin-out, becomes high enough to give strong preference to the high-speed, low-power, bipolar, "ISL" digital logic circuitry.

The combined MOS/Bipolar technology is now being used for an integrated bandwidth compression memory chip capable of sampling rates exceeding 200 MHz. Consequently use of similar fabrication techniques should not represent an extraordinary risk, albeit somewhat more complicated than needed for a pure CMOS/CCD type chip. The slightly higher risk of the MOS/



a) 2ND ORDER RECURSIVE FILTER

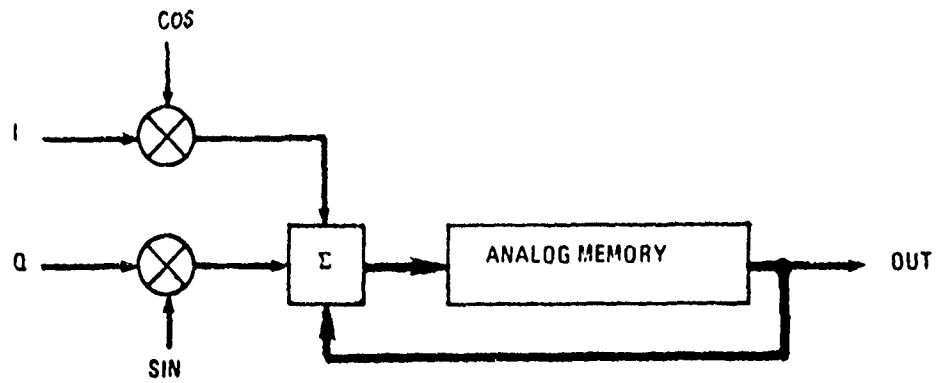
$$H(z) = A_0 \frac{1 + (B_1 + B_0 \frac{A_1}{A_0}) z^{-1} + (B_2 + B_0 \frac{A_2}{A_0}) z^{-2}}{1 + B_1 z^{-1} + B_2 z^{-2}}$$



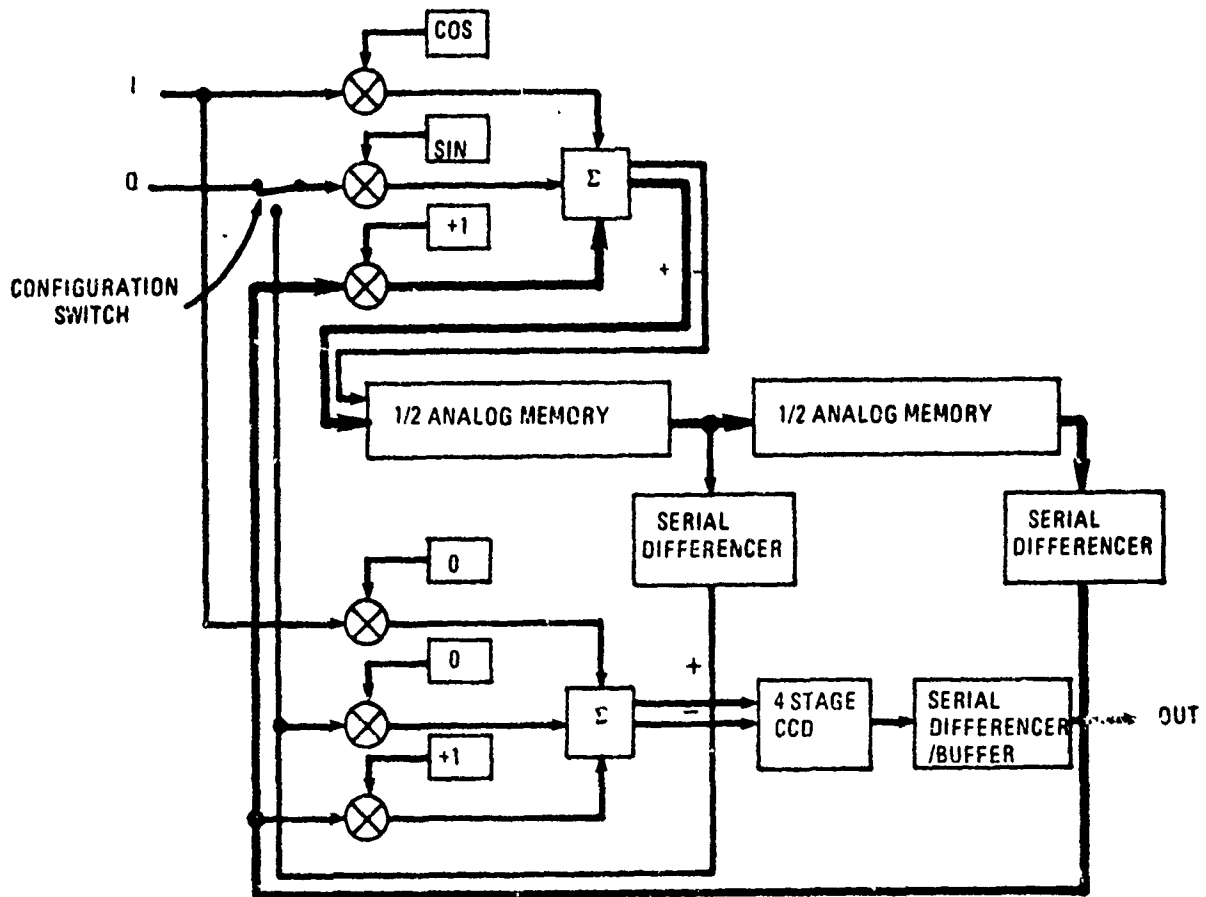
b) RECURSIVE FILTER CONFIGURATION

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Figure 2-3 Demonstration APUP Modes



A) TRANSFORM CONFIGURATION



B) TRANSFORM RECONFIGURED FROM RECURSIVE FILTER

80 0024-V-20

Figure 2-4 Demonstration APUP Modes

Bipolar technology should be offset by the greatly increased universality and user acceptance obtained by the higher speed. Indeed, the performance projected in sections 6 and 7 are the following:

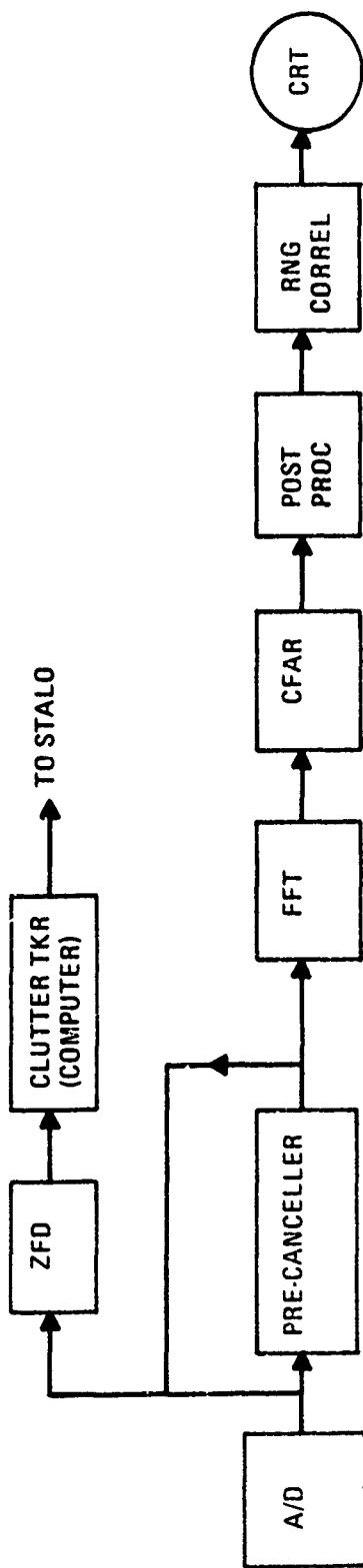
Table 2-4: Projected APUP Performance

Mode:	High Accuracy (Isolated Samples)	Max Data Handling (ECDS Only)
Analog Samples stored	2304	9216
Max. sampling rate	10 MHz	20 MHz
No. of multipliers	6	6
No. of memory taps	4	4
Max. digital data transfer rate	30 MHz	30 MHz
Reconfiguration time	<1μsec	<1μsec
Sample-to-Sample Crosstalk	-83dB	-56dB
Dynamic Range	55-60dB	
Harmonic Distortion	-55 to -60dB	
Configurations:	<ul style="list-style-type: none"> a) Fast-in/slow-out b) 2-pole recursive (IIR) filter c) Generalized transform 	

3. SURVEY OF RADAR SIGNAL PROCESSING REQUIREMENTS

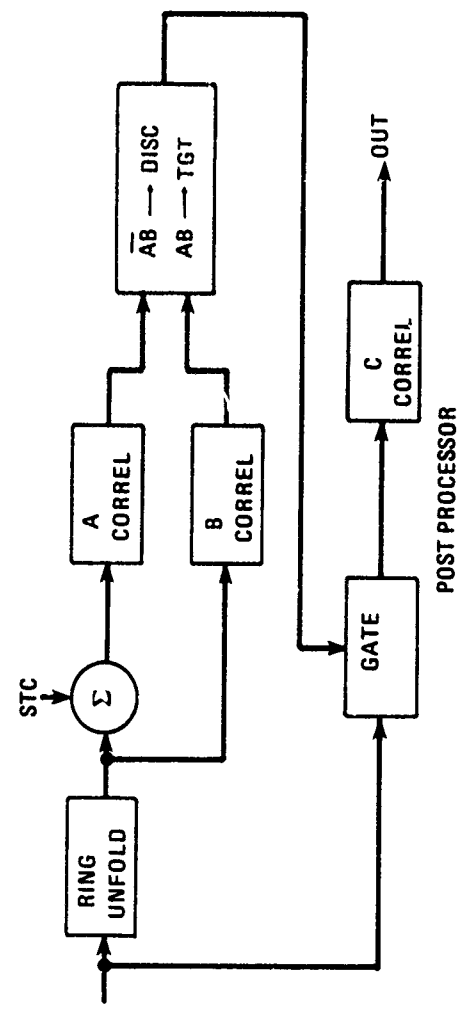
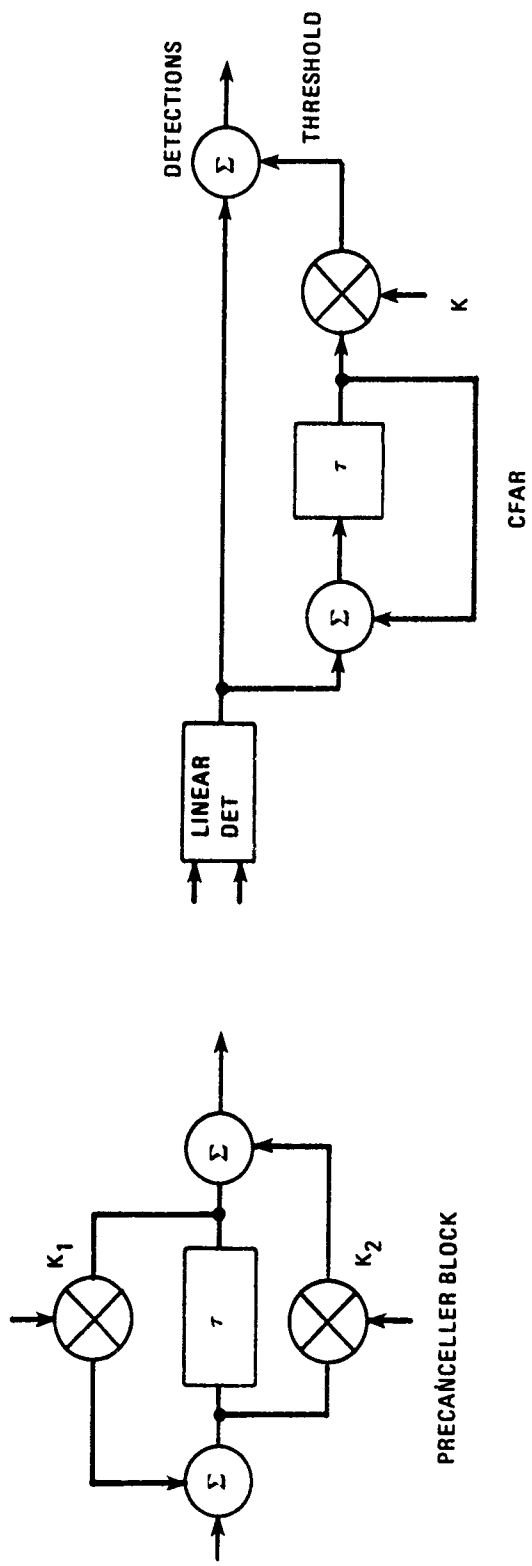
3.1 AIRBORNE RADARS

Many airborne radar signal processors give more emphasis to coherent predetection processing than to subsequent processing such as scan-to-scan correlation for absolute velocity discrimination. That is, with the exception of the AWACS/E3A where scan-to-scan target tracking is an important objective, most airborne radars use such arithmetic functions as FFTs, correlations, corner turns, buffer storage, pulse compression, integrator, etc., similar to - but not as extensive as - some of the arithmetic operations in the SEASAT SAR. Illustrative block diagrams are given in Figures 3.1-1, 3, 5, 7, & 8 for processing associated with air-to-air (A/A), air-to-ground mapping (A/G/M), terrain follow/terrain avoidance (TF/TA), Doppler beam sharpening mapping (DBSM), and EAR TF/TA, respectively, with more details shown for constituent arithmetic functions in Figures 3.1-2, 4 & 6, respectively. In order to implement some of the selected radars with CCDs, key parameters related to CCD performance will be determined. The range resolution is related to the signal sampling rate during the radar return pulse and thus the CCD input rate, either directly or sub-harmonically, depending on parallelism. Similarly, the number of instrumented range cells and the extent of coherent pulse-to-pulse (or azimuth) processing combine to specify a two-dimensional array of devices such as corner turns, analog shift-register memories, or transversal azimuth-filter CCDs. Radar system parameters, such as the number of pulses coherently processed for azimuth correlation or multiple PRF schedules, strongly impact such two-dimensional coherent processing arrays via requirements to store data for extended integration periods, during which times



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FIGURE 3.1-1: Typical Air-to-Air Processor



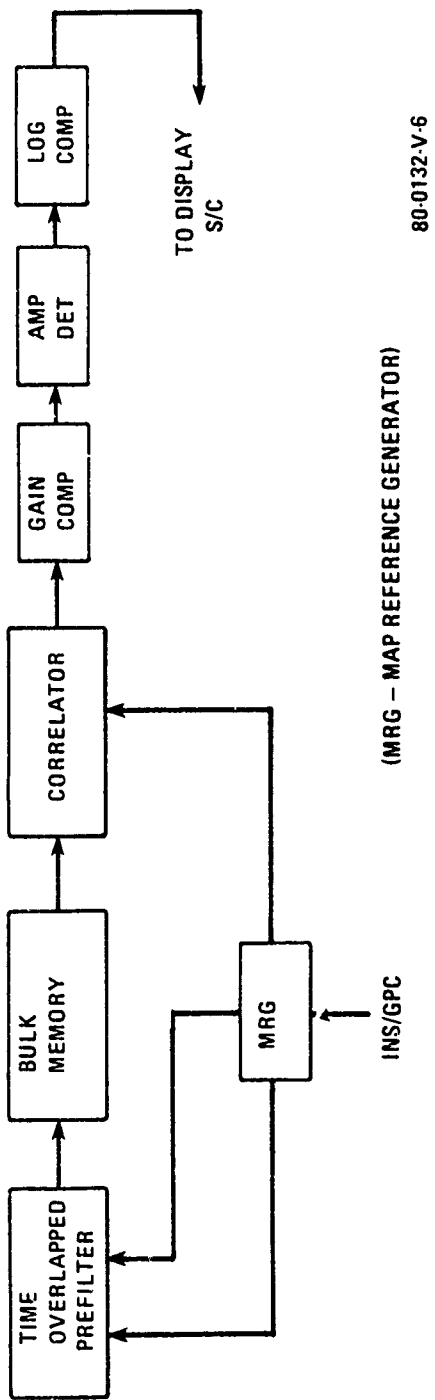
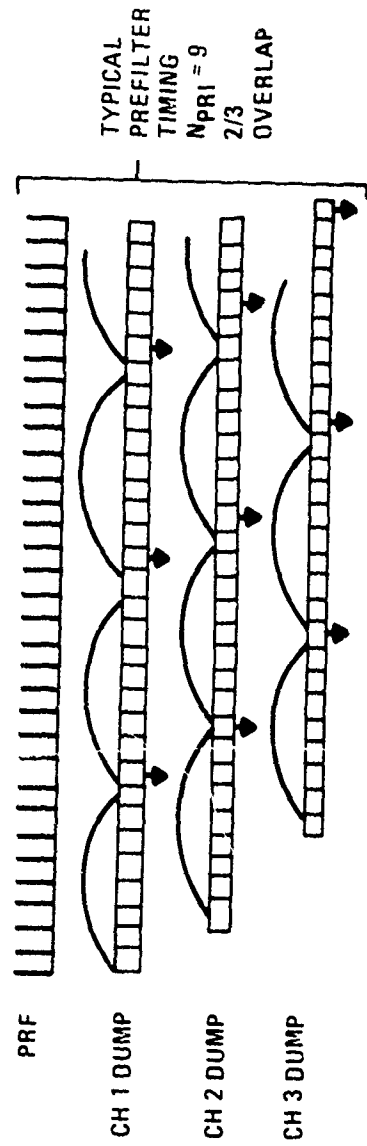
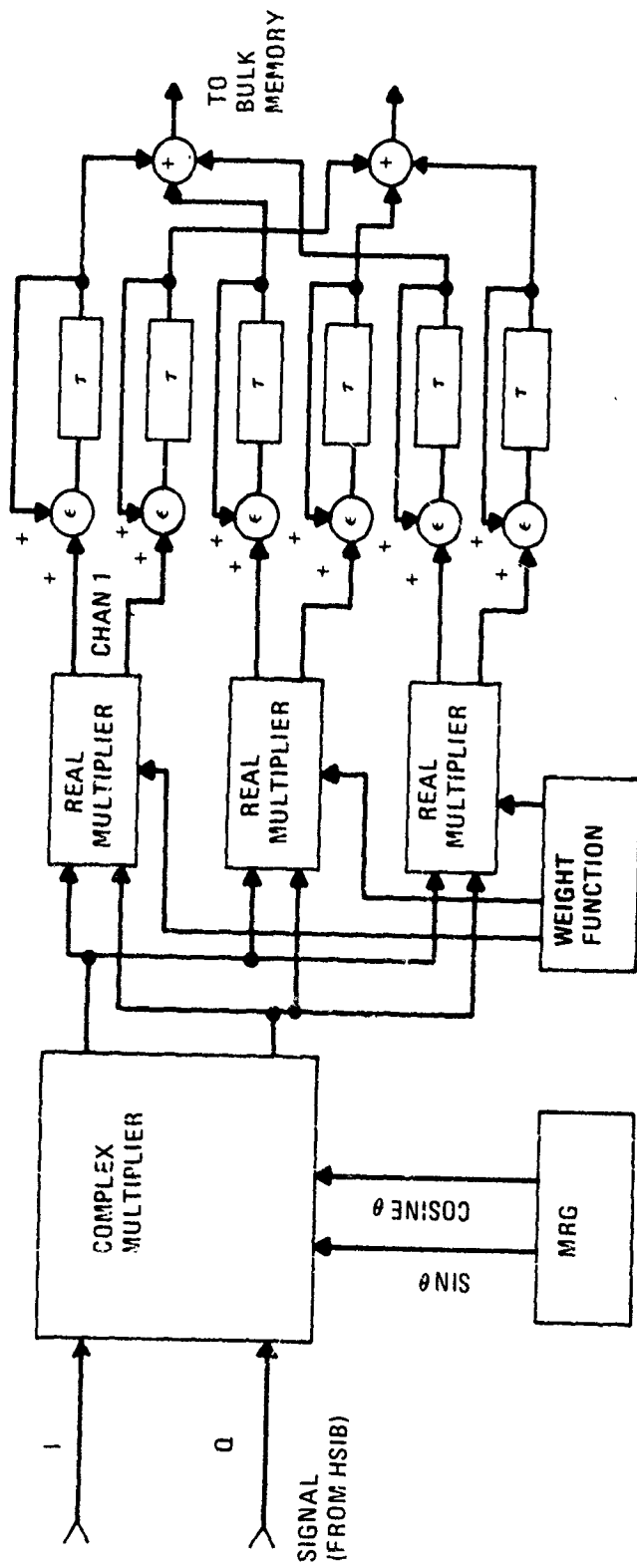
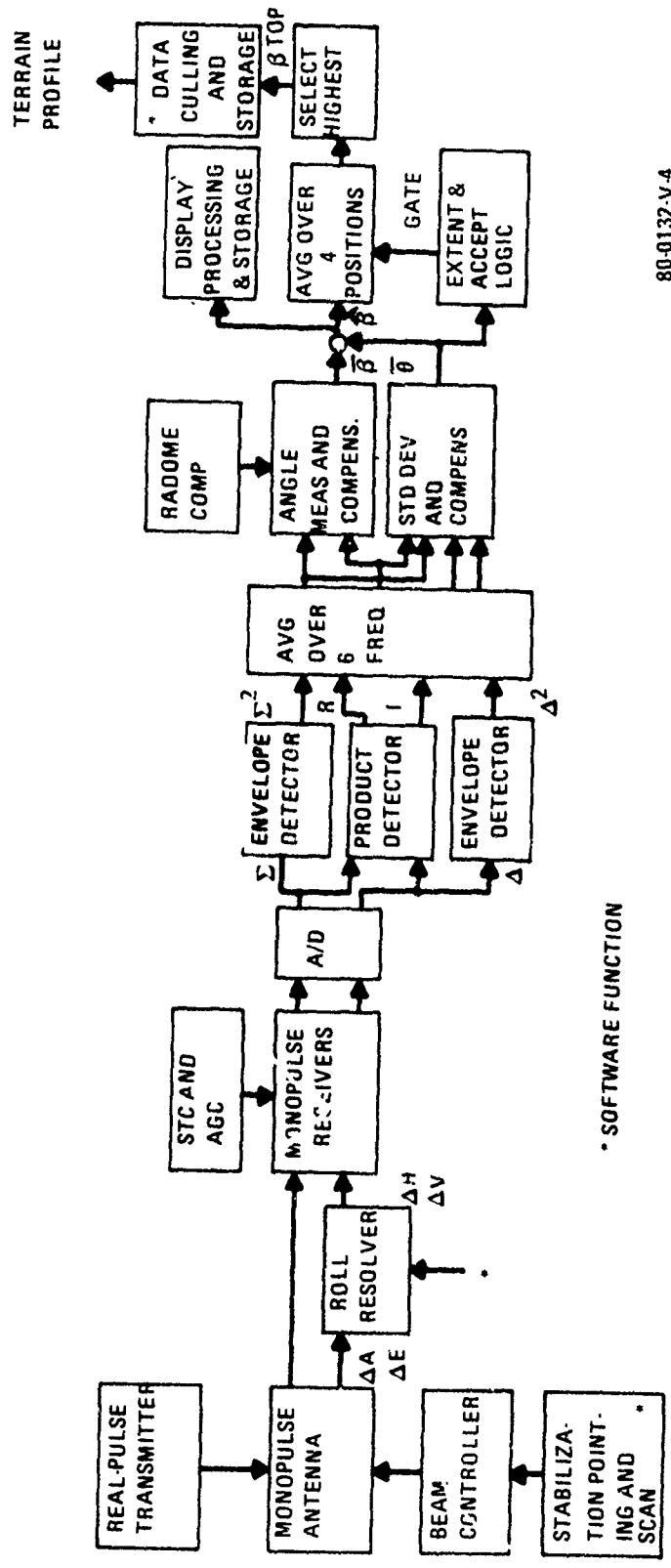


FIGURE 3.1-3: Typical Air-to-Ground Mapping Processor



80-0132-V-3

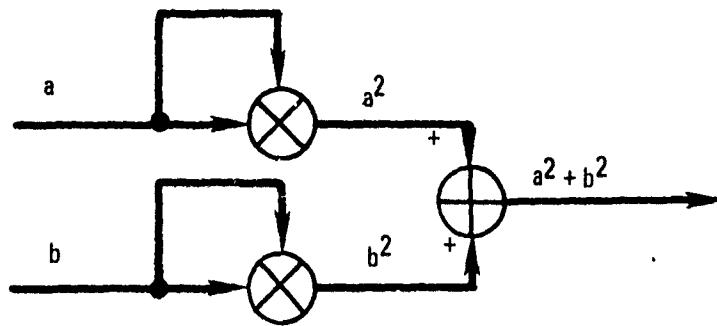
FIGURE 3.1-4: Typical Air-to-Ground Prefilter Mechanization



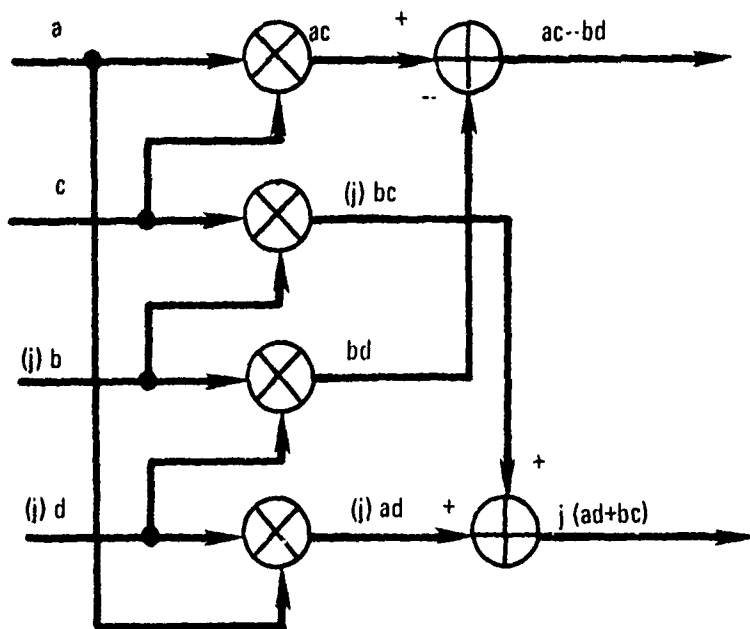
* SOFTWARE FUNCTION

80-0132-V-4

FIGURE 3.1-5: Typical Terrain-Follow/Terrain-Avoidance Processing



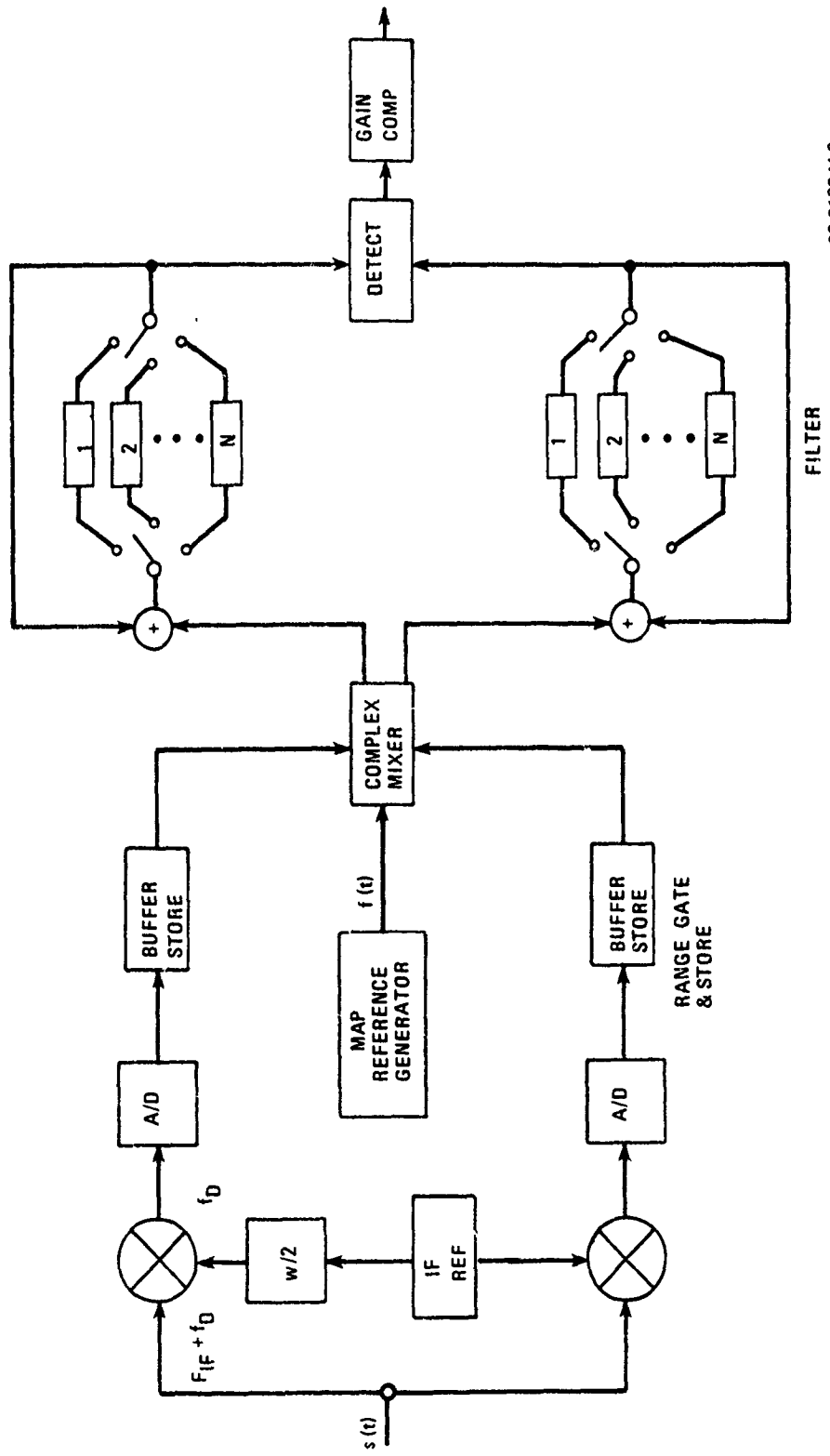
SQUARELAW DETECTOR



COMPLEX MULTIPLIER

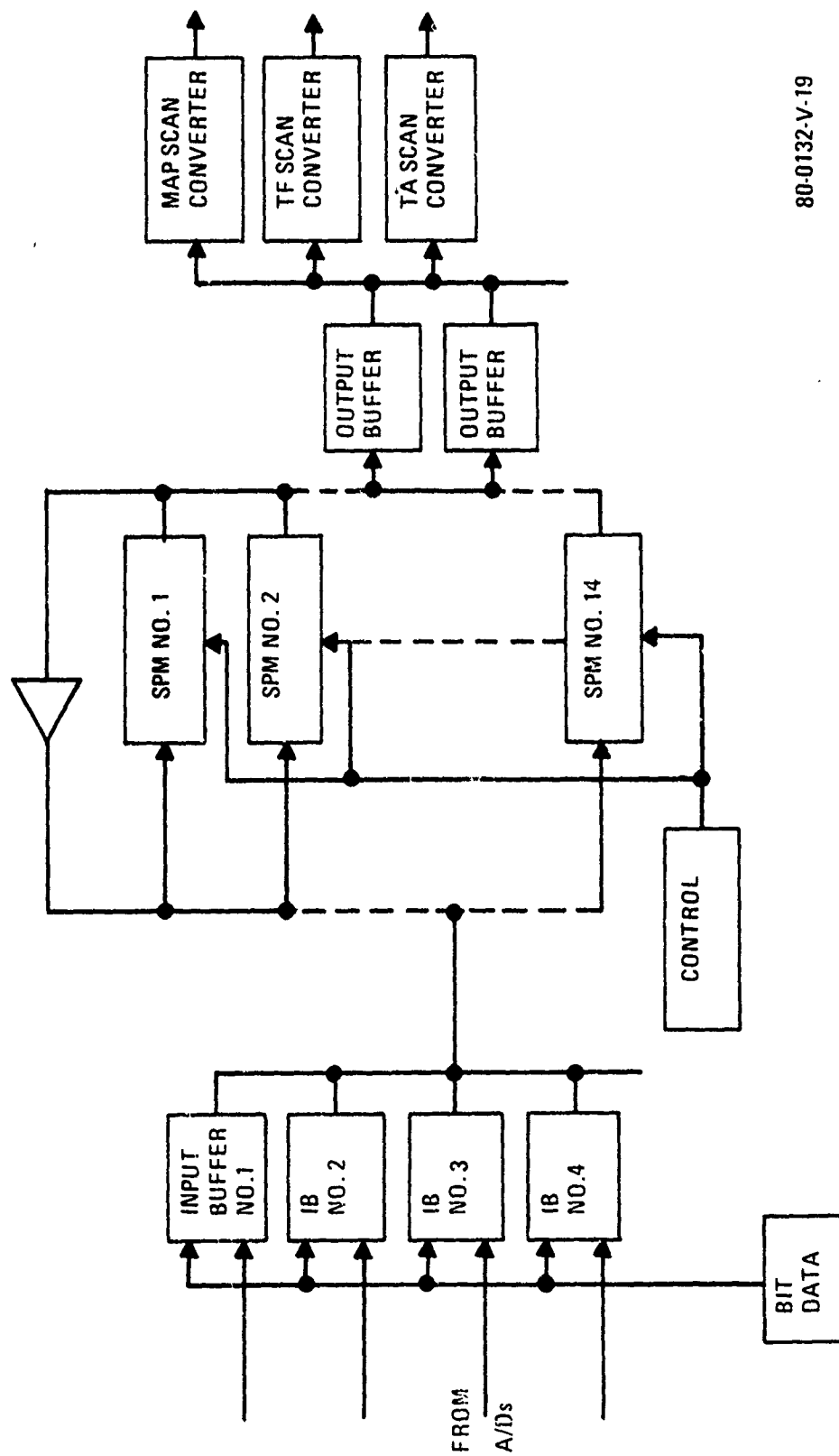
80-0132-V-15

FIGURE 3.1-6: Typical Terrain-Follow/Terrain-Avoidance Processing Blocks



80-0132-V-8

FIGURE 3.1-7: Simplified Diagram for Low Resolution Mapping via Doppler Beam Sharpening (DBS)



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FIGURE 3.1-8: The Programmable Array Architecture for the Electronically Agile Radar (EAR)

the data may move irregularly within the array. These needs are then expressed in terms of such device parameters as array uniformity with respect to leakage current, threshold voltages, etc. Correlating the typical values for space and airborne radar parameters given in Table 3.1-1 with the above observations immediately alerts us that the 2-dimensional arrays (homomorphic to existing preferred radar processing architectures) often must be much larger than most currently published signal processing CCD arrays.

3.1.1 COHERENT MTI RADARS

3.1.1.1 General

The typical airborne coherent MTI radar uses pulse Doppler techniques to detect and resolve targets in the dimensions of both range and velocity. A basic simplified block diagram of a digital signal processor for such a radar is given in Figure 3.1.1-1. The internal details of the blocks vary substantially from radar to radar according to the exact application of the radar as well as to basic design decisions. Indeed, one or more of the blocks may be omitted entirely.

Before discussing the block diagram, it should be mentioned that to date the processing takes place at "zero intermediate frequency". That is, the radio frequency is heterodyned to zero Hertz, and folding of the spectrum about zero is prevented by carrying an in-phase and a quadrature channel. The correct local oscillator frequency to beat the signal to zero is usually determined approximately by computation on the basis of the aircraft velocity vector and the antenna pointing angle, the calculations being made by the systems control computer. In many systems this open-loop calculation is fine-tuned through the use of a zero-frequency discriminator.

The clutter tracker locates the main-beam clutter return in range-frequency space and measures the displacement of the peak clutter return from zero frequency. The output of this block is fed back to the local oscillator to keep the main-beam clutter spectrum centered at zero Hertz. This ensures

TABLE 3.1-1: TYPICAL VALUES FOR KEY PARAMETERS OF AIRBORNE/SPACEBORNE RADARS

PROCESSOR TYPE (ILLUSTRATIVE APPLICATION)	RANGE RESOLUTION (NANOSEC)	NO. OF INSTRUMENTED RANGE CELLS	PRF (Hz)	COHERENT AZIMUTH		OTHER ITEMS
				PROCESSOR TYPE	NO. OF PTS.	
SAR (SEASAT)	50	4000	1645	matched filter correlator	3000	Range Pulse Compression: Linear FM Time- Bandwidth Product = 634 By SAW devices
SAR (EAR)	40	300	2000 to 4000	line-by-line correlator	200	30 pulse co- herent pre- filter; 0.1 sec integration time in AZ cor- relator.
MAPPING (F16)	250	256	1000	FFT	64	
MTI (SOTAS)	200	2600	1500 to 2000	DBS FFT	20 64	

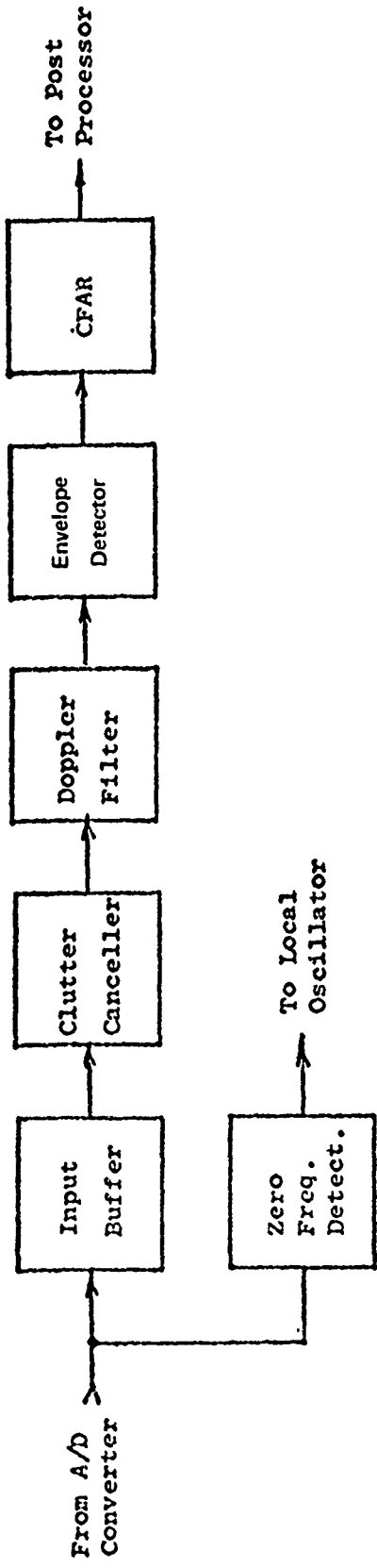


FIGURE 3.1.1-1: Basic Block Diagram of Airborne MTI Radar Signal Processor

maximum clutter rejection by the clutter canceller. The clutter tracker is sometimes considered part of the radar receiver and precedes the input buffer of the signal processor, or it may be included as part of the processor and placed either before or after the input buffer.

In modern fighter aircraft the trend is toward the use of multimode radars. The signal processors in such radars are designed to accommodate the mode which places the highest demands on memory and on arithmetic capacity. This means that the actual block diagram of such a radar frequently performs the less demanding modes with unnecessary complexity of implementation simply because it is easier and more straightforward to include the extra parts or features than it is to switch them out.

The first block in the processor proper is an input buffer. This block is of greatest importance in low-PRF modes, where it is possible to slow the data rate by taking advantage of the fact that only a fraction of the interpulse period is used for data collection. Double buffering permits the data collected in $1/N$ th of the period to be passed on over the entire period. This reduces the data rate to subsequent blocks by the factor N . High-PRF medium modes use the entire interpulse period for data collection, so that for these an input buffer cannot be used to slow the data rate. Nonetheless, input buffers find application in some high - and medium-PRF radars for two other purposes. First, the buffer can act as an interface device between the A/D converter and the multiple parallel processors which follow. Second, the input buffer can help to solve the timing problems which occur when a shift in PRF takes place. Then used for this purpose the buffer must be large enough to hold the range bins of at least one interpulse period.

The clutter canceller is a band-stop filter, centered at zero frequency to reject the main-beam clutter return. It is used in situations in which the clutter spectrum is broad and the clutter amplitude is very high with respect to the thermal

noise. It is used for downlook air-to-air modes of radars in fixed-wing aircraft. Uplook modes don't need the clutter canceller because in these modes the main beam never intercepts the ground.

The benefit of the clutter canceller is that by removing the very strong clutter signal ahead of the Doppler filtering operation, the dynamic range and the sidelobe weighting required in the Doppler filters are very greatly reduced.

The Doppler filtering block may be implemented with any one of several techniques. Correlation processing could be used, but the survey indicated that it is not generally applied to MTI, possibly because more filters are needed than are practically achievable with this technique. Instead, one of two FFT techniques are used. The two techniques differ in the organization of the memory and the arithmetic units. The more common technique collects the input data in a corner-turn memory, then processes the data in an arithmetic unit. The corner-turn memory accumulates the data ordered in strings of consecutive range elements for a given interpulse period (IPP). The data is passed on to the arithmetic unit reordered in strings of sequential samples for a given range gate. The output of the arithmetic unit is ordered as strings of frequency responses for a given range cell.

The other filtering technique makes use of relatively small blocks of serial memory interspersed between arithmetic stages in a pipeline configuration. This is an older, less versatile technique, and is not likely to be much used in future digital processors. Nonetheless, its pipeline nature might make it more suitable for a CCD type of implementation.

The envelope detection block is usually implemented in one of two ways according to whether squarelaw or linear detection is desired. Squarelaw detection is accomplished using two multiplies and one add to form the expression $I^2 + Q^2$. Linear detection is performed by approximating $\sqrt{I^2 + Q^2}$ by $I + Q/2$ if I is greater than Q , and by $I/2 + Q$ if Q is greater than I .

This approximation takes hardly any more hardware or time than squarelaw detection and is much simpler than an exact square-root operation.

Envelope detection should not be confused with target detection. It is just the first step in the target detection process. Following the envelope detector is usually found a CFAR (constant false alarm rate) processor. The CFAR performs the next step (which is sometimes the last step) in detection by comparing the signal strength of the range-frequency cell under examination with the average strength of surrounding cells. A detection decision is made whenever the strength of the cell under test exceeds the average background strength by a predetermined factor. This process keeps the false alarm rate constant independent of the noise level in the vicinity of the target.

The CFAR circuit is often considered the last step in the signal processor proper, although further processing steps are often taken. The further steps most often are performed by a general purpose processor rather than by dedicated hardware within the signal processor. Important examples of such further processing are dual threshold (M out of N) processing, resolution of frequency ambiguities, and resolution of range ambiguities.

It should be mentioned that CFAR processing is used only in modes requiring automatic target detection. These include almost all air-to-air modes. Modes in which the detection is made by a human operator viewing a PPI, sector scan, or similar cathode-ray display do not require a CFAR circuit. This includes most air-to-ground modes.

3.1.1.2 Effect of Application on Parameters

The application of a particular airborne MTI radar affects the selection of the parameters of the radar. The radar applications fall into two basic categories; air-to-air and air-to-ground applications. The radar and processor parameter most directly affected by this dichotomy is the pulse repetition

frequency. Targets moving on the ground have relatively low velocities, so that the width of the doppler spectrum is low. The minimum PRF which permits unambiguous detection of the doppler spectrum is equal to the width of the spectrum. The width of the spectrum is given by the equation

$$\begin{aligned} BW &= \frac{2\Delta v f}{c} \\ &= 2.99\Delta v_{\text{mph}} \times f\text{GHz} \end{aligned}$$

where f is the radio frequency of the radar transmitter, c is the velocity of light, and Δv is the spread of velocities which can be encountered within the radar beam. Assuming that the maximum velocity of a ground target is 50 mph, then the difference between an opening and closing target is 100 mph, leading to a doppler spread of 3000 Hz for a 10 GHz radar. Thus, a relatively low PRF permits unambiguous velocity measurement for the air-to-ground case. In contrast, the velocity spread for the air-to-air case can be easily 20 times as great, resulting in a requirement for a PRF 20 times higher than the air-to-ground case if unambiguous velocity measurement is demanded.

In practice, other considerations prevent the use of a PRF high enough to give completely unambiguous velocity measurement. In the air-to-ground case it may be desired to have unambiguous range measurement over a larger distance than would be permitted by a PRF high enough to yield completely unambiguous velocity measurement. The relationship of PRF to maximum unambiguous range is

$$\begin{aligned} \text{PRF} &= \frac{c}{2 \times R_{\text{max}}} \\ &= 80992/R_{\text{max}} \quad (\text{in nautical miles}) \end{aligned}$$

If a PRF of 3000 Hz is substituted in this equation the result is only 27 nautical miles, which may be inadequate for many situations. In such a case then a lower PRF may be used, and the ambiguities in the measurement of Doppler shift may be

resolved by the use of multiple PRF's together with the Chinese Remainder Theorem.¹

Another consideration in the selection of the PRF is the elimination of the main beam ground clutter. The spectrum of the ground clutter return from the area illuminated by the main lobe of the radar is a function of the aircraft velocity v , the angle α between the velocity vector and the main beam, and the angular width of the beam. If the PRF is not sufficiently higher than the width of the clutter spectrum, then aliasing of the signal spectrum will fold the clutter and the target returns together so that frequency filtering cannot separate them. To be practical, the clutter bandwidth should be no more than perhaps 30 percent of the PRF, to allow adequate probability that the target returns will not fall within the clutter region.

The clutter bandwidth can be calculated from the simple approximation

$$BW_c = \frac{2v}{dc} \cos \alpha$$

where d is the diameter of the antenna. This formula takes into account the variation of beamwidth with radio frequency. A formula which breaks out the effect of beamwidth and radio frequency is:

$$BW_c = f_0 \frac{2v}{c} \cos \alpha \Delta\beta$$

where f_0 is the radio frequency and $\Delta\beta$ is the antenna beamwidth.

Before leaving the subject of PRF, the connection between PRF and number of range gates should be discussed. High-PRF systems naturally tend to have a small number of range gates because the duty ratio is usually high. For example, a radar having a 1-microsecond pulse and a 30-KHz PRF can have its 33.3-microsecond interpulse period divided into only 33 non-overlapping range gates. A 50% overlap would up this number only to 66 gates. On the other hand, a low-PRF radar, with its much lower duty ratio, can have its period divided into many more range gates. The practical limit in the low-PRF

situation is set by the active portion of the interpulse period. For example, a radar might be designed for an air-to-ground mode using a PRF of 1600, which gives a maximum unambiguous range of about 50 n.mi. If this radar were to cover a range segment extending from, say, 35 n.mi. to 50 n.mi., then only 30% of its interpulse period would be actively used for data collection. Assuming that the radar were to use a 1-microsecond pulse, then the number of non-overlapping range gates needed would be $.30 / (1600 \times 1 \times 10^{-6}) = 187$.

The radar designer must make a fundamental tradeoff between the total range segment covered and the size of the signal processor. The processor grows in direct proportion to the number of range gates to be processed. In multimode radars the range interval covered in a low-PRF air-to-ground mode might be determined by the amount of processing power designed in to handle a primary air-to-air mode.

By way of summary and clarification, pulse doppler radars are usually thought of as having low, medium, or high PRF's, according to the following definitions:

1. Low PRF - A PRF low enough to give unambiguous ranging
2. High PRF - A PRF high enough to give unambiguous velocity measurements (usually against airborne targets)
3. Medium PRF - A PRF for which both range and velocity measurements are ambiguous.

Air-to-ground MTI modes usually use a low PRF. Long-range air-to-air surveillance modes tend to use a high PRF because it enables a high average transmitted power without resorting to high peak power or pulse compression. Finally, air-to-air fighter modes usually use a medium PRF.

Another radar parameter which has a major impact on the signal processor is the number of doppler filters used to cover the signal spectrum. This parameter is influenced less by the radar application (i.e., air-to-air or air-to-ground uses) than it is by more detailed considerations. Other factors

being fixed, the narrower the Doppler filters, the higher the sensitivity of the radar, because the Doppler filters are pre-detection integrators. Two principal factors prevent the designer from making the filters arbitrarily narrow. The bandwidth cannot be narrower than the reciprocal of the dwell time or the signal power will be spread over more than one filter. This would both lower the detection sensitivity and force the use of frequency centroiding to determine the correct target velocity. Thus no gain would be achieved by the needlessly narrow bandwidth. Secondly, the effect of filter bandwidth on processor size may impose a practical limit. If the Doppler filters are implemented by an FFT approach, then the processor memory requirement goes up linearly with the number of filters while the processor speed requirement increases somewhat faster than linearly by the relation

$$\text{Speed} \propto N \log_2 N$$

where N is the number of points in the transform.

If a convolution approach is used, then the speed requirement increases much faster according to the relation

$$\text{Speed} \propto N^2.$$

For the radars surveyed, the number of Doppler filters varies from 16 to 128.

3.1.1.3 Survey Data

The survey data for the major blocks of the signal processor are given in tables 3.1-2 through 3.1-4. For each processor block the data is broken down according to radar application. The fixed-wing, long-range surveillance and the rotary-wing applications each stand alone from the other applications in the survey data. All of the others are related modes of modern multimode fighter aircraft radars. It will be apparent from the data, particularly in the input buffers and the clutter cancellers, that the implementation of the various modes was influenced by the requirements of whichever mode was the most demanding.

3.1.1.4 Input Buffers

Table 3.1-2 gives the data on input buffers. Only the high PRF long range surveillance radar application does not use an input buffer. The various modes of the multimode radars all use an input buffer, but only the air-to-ground modes make use of the buffer for the purpose of data rate reduction. The air-to-air modes use the buffer only as an I/O device between the analog/digital converters and the rest of the signal processor, as described in an earlier paragraph. Note that the helicopter radar, which was designed primarily for an air-to-ground application, uses the input buffer for data rate reduction.

3.1.1.5 Clutter Cancellers

Data on clutter cancellers is given by Table 3.1-3. The most noticeable aspect of the data is that the long range air-to-air surveillance radar places the greatest demands upon the clutter canceller, the air-to-air downlook modes and air-to-ground modes are much less demanding, and the air-to-air uplook mode and the helicopter radar have no need for the clutter canceller. The 120-dB (20-bit) requirement of the surveillance radar is clearly beyond the present state of the art of CCD techniques. The 66-dB (11-bit) requirement of the three modes of the multimode radar lies just beyond the present 60-dB CCD capability. If a radar designer were constrained to use a CCD implementation for this purpose he might be able to do so by making system trades and compromises. Lower dynamic range in the clutter canceller can be compensated for by greater dynamic range in the Doppler filtering process.

As mentioned earlier in the general discussion, the air-to-air uplook mode does not need the clutter canceller because the main beam does not intersect the ground, consequently there is no main-beam clutter to cancel. The helicopter radar does without a clutter canceller for another reason. Because of the relatively low velocity of the helicopter radar platform the main-beam clutter has a very narrow Doppler spread. Further-

TABLE 3.1-2: INPUT BUFFER

	PRF (KHz)	DATA RATE (MHz)	NO. OF RANGE CELLS	WORD LENGTH
Air-to-Air Long-range Surveillance	N	O N E		
Air-to-Air Search, Uplook	1 KHz	0.125 in, 0.25 out *	128	11 I + 11 Q
Air-to-Air Dogfight Downlook	7.8 - 14.3	1.0 in, 2.0 out *	128	11 I + 11 Q
Air-to-Ground MTI	1.35-1.65	0.125 to 1.75 in, 0.25 to 3.5 out *	128 or 64	11 I + 11 Q
Air-to-Ground MTT	2.7 - 3.3	0.5 to 1.75 in, 1 to 3.5 out *	128 or 64	11 I + 11 Q
Helicopter Air-to-Ground	1.75 max	5	2600	8 I + 8 Q

Multi
Mode
Radar

* I and Q data input in parallel, output in series

TABLE 3.1-3: CLUTTER CANCELLER

	DATA RATE	REGISTERS		ADDS		MULTIPLIES RANGE		
		NO. USED	BITS	NO. USED	BITS	NO. USED	BITS	GATES
A/A Long-Range Surveillance	2.5MHz	4	20	8	20	7	12X20	50
A/A SEARCH UPLOOK	N	O	N	E				
A/A DOGFIGHT DOWNLOOK		2	11	2	13	1	by 2	128
A/G MTI		2	11	2	13	"		128 or 64
A/G MTT		2	11	2	13	"		128 or 64
HELICOPTER A/G	N	O	N	E				

Multi Mode Radar

more, the targets of the radar are slow-moving ground vehicles. To be useful, the clutter filter would have to be very narrow in bandwidth. This type of filter has a poor transient response which would be a problem to the radar designer. Consequently, for this type of system a good design decision is to omit the clutter canceller and solve the clutter problem with greater dynamic range and low sidelobes in the Doppler filtering FFT.

3.1.1.6 Doppler Processing

The survey data on the Doppler processing is given by table 3.1-4. All but one of the radar applications make use of a corner-turn memory followed by an arithmetic unit which computes an FFT. The exception is the long range surveillance radar, which uses a pipeline-organized FFT with its memory distributed between its arithmetic stages. The number of filters generated by the FFT varies rather widely across the radar applications, from 16 filters for the air-to-ground modes of the fighter-type radar to a high of 256 filters in the helicopter radar. Similarly, the number of range cells processed also varies widely, from a low of about 50 cells in the long-range air-to-air surveillance radar to a high of 2600 cells in one mode of the helicopter radar. The computational loading of the various applications is given as the approximate number of megops per second. (An "op" is defined as one complex multiply plus one complex addition plus one complex subtraction.) This number is computed as follows:

$$S = \frac{M R}{T}$$

where S = speed in ops/second, M = number of ops per FFT, and R = number of range cells. The factors T and M may be calculated thus:

$$T = N/f_r, \text{ and}$$

$$M = \frac{N}{2} \log_2 N$$

where N = the number of filters in the FFT and f_r = the pulse

TABLE 3.1-4: DOPPLER FILTERING

PRF (KHz)	DATA (MHz)	NO. OF RANGE CELLS	NO. OF FILTERS	CELLS X FILTERS	WORD SIZE	REL SPEED (Meg Ops)	SIDELobe LEVEL (dB)	COMMENTS
25-31	2.5	50	128	6400	6 to 9 bits	5.42	40	Pipeline organized 7-stage FFT Word size increases through the stages.
1KHz	0.25*	128	64	8192	8I+8Q	0.384	60	Corner-turn memory followed by arithmetic unit
8-14	2.0*	128	64	8192	8I+8Q	5.38	60	"
0.45-1.6	0.25 to* 3.5	128	16	8192	8I+8Q	0.334	60	"
2.7-3.3	0.25 to* 3.5	128	16	2048	8I+8Q	0.845	60	"
1.45 - 1.75	5.0	(310-2500)	256 48	79K 125K	8I+8Q 8I+8Q	2.17 25.4		"

Air-To-Air
Long-Range
Surveillance

Air-To-Air
Search
Uplook

Multi
Mode
Radar

Air-To-Air
Dogfight
Downlook

Air-To-Ground
MTI

Air-To-Ground
MTT

Helicopter
Air-To-Ground

*I and Q data in series

repetition frequency. Substitution of the expressions for T and M into the equation for S yields

$$\begin{aligned} S &= \frac{N}{2} \log_2 N \cdot R / (N/fr) \\ &= \frac{fr}{2} R \log_2 N. \end{aligned}$$

For the reader's convenience, figure 3.1.1-2 presents a graphical means of solving this equation. Directions for its use are given above the figure.

3.1.1.7 CFAR

CFAR processing schemes vary greatly from radar to radar. The background area which is averaged to produce the threshold level may extend in the two dimensions of range and frequency, forming a rectangular annulus around the target area. Alternatively, it is frequently just one-dimensional, taking the form of a several-cell window on both sides of the target, either in the dimension of range or of frequency. In digital data processor implementations, the CFAR processing imposes a considerable processing load. For each target position to be examined, $N-1$ additions are required to form the sum of N background cells, one multiplication is required to scale this sum down to an average, and one subtraction is required to test the target cell amplitude against the average. Weighting of the contributions of the various background cells is not generally used because this would increase the computation load by N multiplications.

The CFAR process, as described above, would readily be implemented by CCD techniques. The sliding windows, complete with weighting if desired, can take the form of transversal filters. If CFAR processing in two dimensions is required, then provided that the outputs in the second dimension are available in parallel, the second dimension can be obtained through the use of paralleled transversal filters. Weighting in the second dimension is obtained just as easily as in the first, by adjustment of the summing resistors into the summing

Enter curves with PRF and number of filters in FFT. Read ops/second per range cell on scale on left. Project this reading diagonally toward upper right to intersection with vertical line corresponding to number of range cells. Project this point to the scale on right to read total speed requirement. For example: PRF of 1350 Hz and N of 16 leads to 2750 ops/second per range cell. 20 range cells leads to total requirement of 55,000 ops/second.

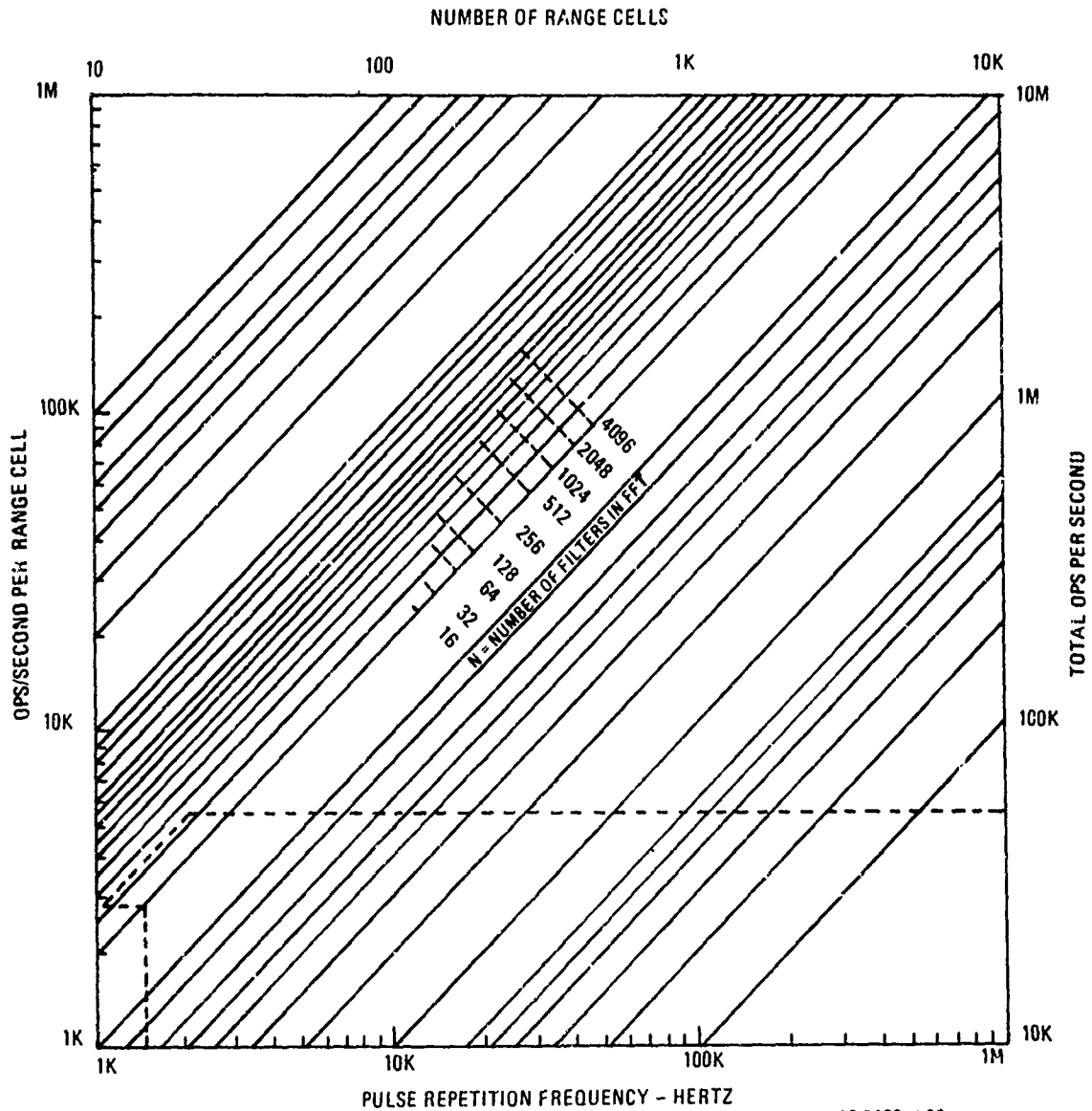


FIGURE 3.1.1-2: Operations per Second as a Function of Filter Number and PRF

node of an amplifier.

The dynamic range of the signal into the CFAR process seems to run in the range of 8 to 12 bits. When implemented in a straightforward fashion with digital techniques the dynamic range of the CFAR arithmetic must be greater than that of the input by $\log_2 N$ (where N is the number of background cells averaged) in order to be certain of not saturating. With an analog implementation the presence of the weighting factors built into the transversal filters prevents the buildup of dynamic range through the CFAR summation.

3.1.2 AIR TO AIR PULSE-DOPPLER RADAR

3.1.2.1 General

The contemporary air-to-air pulse doppler radar (with a downlook capability) uses a filter bank which in most cases is established with an FFT algorithm. The essential parameter here other than speed is the filter bank sidelobe level. Typical minimum values for A/C to A/C work in AWI radars is -60 dB and for missile detection by an A/C radar a value of -80 dB is normal. With the FFT, these levels are obtained by Dolph Chebyshev weighting. It is important to note that weighting as high as -120 dB is not uncommon. The reason for these large values is the radar hardware investment and processor data rates vs the S/C performance required, compared to the relatively low difficulty in getting the -60 to -80 dB.

The following section outlines the processing requirement for an A/C radar which performs the function of detecting anti-aircraft aerodynamic missiles having a built-in active target seeker. The need here is to construct a -80 dB SL bank of 64 Doppler filters spaced continuously across the selected spectrum and duplicated over 10 gates in range. The number of range-gates and filters in the bank is minimized to conserve radar and signal processing hardware while maintaining specified performance against the anti-aircraft missile. To lessen the SL requirement, the clutter patch (range-gate/velocity-bin) dimension must be reduced in size.

Assuming that an analog filter bank could be built with a -40 dB SL level the changes indicated in Table 3.1.5 would be needed. As can be seen, they impact the radar and the signal processor. Depending on the missile dynamics the Doppler filter quantity may not be able to be increased to 256 or instead tracking may be required.

3.1.2.2 Air-Air Missile Detection

3.1.2.2.1 Corner Turn Memory

The input to the corner turn memory (Figure 3.1.2-1) is for 10 range-gates at an 0.8 MHz rate with a dynamic range of $S + 11$ bits (66dB). The CT is a 32 k bit static MOS RAM configured to handle the 10 range gates and the 64 FFT samples (radar IPP's).

3.1.2.2.2 Doppler Filter

The 64-point FFT, which operates on one RG at a time, has an input dynamic range of 66 dB and an output dynamic range of 90 dB with -80 dB sidelobes formed by Dolph Chebyshev weighting. The filter spacing is governed by the PRF's used. If two PRF's are incorporated to resolve range ambiguities, then there will be two filter widths for the same number of FFT coefficients. The comparable velocity resolution of these 2 filter widths is accomplished by scaling (to be described later). The PRF's selected for satisfying the missile dynamics and the ambiguity resolution results in filter bandwidths in the vicinity of 300 to 400 Hz for this example.

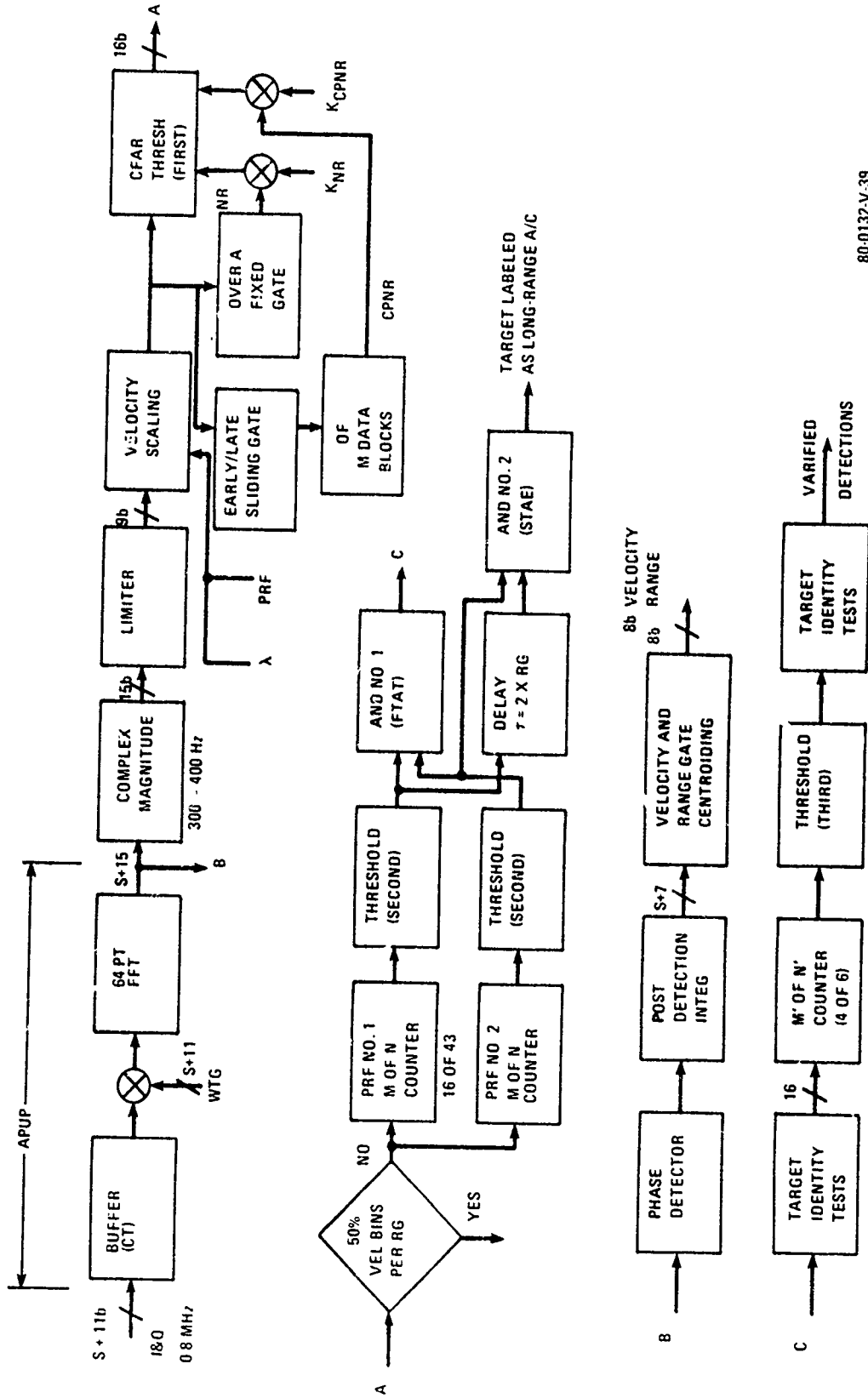
3.1.2.2.3 Complex Magnituder

The complex data out of the FFT is passed through a conventional magnituder which can be implemented by either of the following algorithms, the selection depending on mechanization and/or accuracy requirements although for most cases either is satisfactory from a performance viewpoint.

$$\text{Magnitude} = |I^2 + Q^2|^{1/2}$$
$$\text{or Magnitude} = \max [(I + 1/2Q), (Q + 1/2I)]$$

TABLE 3.1-5: RADAR/PROCESSOR COMPLEXITY COMPARISON

ITEM OR FUNCTION	-80 dB FILTER SL	-40 dB FILTER SL
RADAR PULSE COMPRESSION	NONE	YES
TARGET RANGE TRACKING	NONE	YES
NUMBER OF RANGE GATES	10	256
NUMBER OF DOPPLER FILTERS	64	256
PROCESSOR INPUT RATE	0.8×10^6 WPS	20.5×10^6 WPS
CORNER-TURN MEMORY	32 kB	1600 kB
A/D DYNAMIC RANGE	66 dB	30 dB



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FIGURE 3.1.2-1: Air-to-Air Radar (Missile Detector)

3.1.2.2.4 Velocity Scaling

In most systems of this type, there are multiple transmitter frequencies used in order to establish sample independence, lower the interference from other radars, and provide some ECCM. In addition, two PRF's are incorporated for resolving first time around echos (FTAE) from echoes at integer multiples of the IPP (MTAE). Transmitter frequency diversity causes a variation of Doppler to relative-target-velocity calibration (inversely with wavelength), while two PRF's results in two different FFT output filter widths. To obtain accurate velocity definition, a variable scaling operation must be performed on the output FFT data-blocks. To accomplish rejection of the ground clutter return sensed by the radar, the first 18 to 25 (depending on PRF and problem geometry) Doppler filters are discarded, thus the velocity scaling by the microprocessor need only be done on the remaining 46 or fewer filters. For the example selected, the Doppler filters used are mapped into 46 velocity bins. The transformation utilizes wavelength, PRF, and A/C ground speed as inputs.

3.1.2.2.5 CFAR

The CFAR (constant-false-alarm-rate) is set by automatically adjusting the level of a target detection threshold. For this particular application, there are two CFAR regions (thresholds) considered; i.e., one is for clutter-plus-noise region (CPNR) and the other for noise-only region (NR). Two ratioing values (CFAR constants) are computed in the microprocessor; one constant is for the CPNR in the data-block and the other, NR. The receiver channel data is utilized to form the two separate CFAR thresholds.

The CFAR operation for the CPNR is implemented by sliding a dual window made up of velocity bins $(n + 1)$ and $(n + 5)$ from any sequence of 5 continuous bins. This quantity is summed over 2 to 4 FFT data block outputs (a value of 3 is assumed here) and then is multiplied by the CFAR constant prior

to use on the first threshold.

The NR magnitude is obtained by summing the last 12 velocity bins over one data-block for a range gate. It is then multiplied by the CFAR constant for NR prior to use on the first threshold. The boundary (in a sequence of 46 bins) between the CPNR and the NR is determined by a calculation using A/C ground speed and vertical data.

3.1.2.2.6 Detection Function

The detection function selected here is a 2-stage M of N. The steps or levels of discrimination in the detection process are described in the following:

- Level 1 Requires a target in a range/velocity-bin to have an amplitude greater than the CFAR threshold. Data words are supplied to this threshold at a rate of 46 velocity bins per range-gate i.e., (PRF)/64 or 300 to 400 Hz.*
- Level 2 Requires there be fewer than 50% of the velocity bins in an FFT data-block (per range gate) that have targets exceeding the CFAR threshold in order for that data-block to be considered valid.
- Level 3 Requires that at least 16 level-1 detections exist in 43 valid data-blocks for a specific range/velocity-bin location to be tagged as possible target. The numbers 16 and 43 are determined in part by the allowable false alarm rate and the relative velocity and acceleration characteristics of missile targets. For the example selected, the 43 data-blocks require about 1/4 of a second of elapsed time to occur. Alternately interleaved with the above 43 data-blocks are 43 more data-blocks from the FFT's calculated with PRF #2. It is at this point where FTAT are

*As noted under the discussion for velocity scaling, there are 46 velocity bins established for each range gate, thus n varies between 0 and 41.

verified and STAE are rejected by delaying the low PRF second threshold outputs and testing for coincidence in a particular range/velocity-bin with the higher PRF (#1) in an "AND" gate. If the coincidence in AND #1 is verified, a level-3 detection is satisfied at this point as a missile or an A/C.

Level 4 This is the final threshold which tests for four level-3 detections in any sequence of six. Since a level-3 detection takes approximately 1/4 second, then the total integration period or detection cycle would be effectively 1.5 seconds.

There are several other processing functions which can aid in the automatic classification of a target as a potential missile threat, namely: measurements of radar cross-section, target velocity, and target geometric distribution in range-gate/velocity-bin space.

3.1.2.2.7 Target Location Determination

To define the target location to a higher accuracy in range-gate/velocity-bin space, it is possible to add both range and velocity centroiding (shown in diagram). The improvement by centroiding is required for a higher accuracy in the calculation of target velocity, time for the target to impact the A/C containing the radar, and in maximizing the time for counter measures by this A/C.

The velocity centroid examines the range/velocity detections for an FFT data-block in a range-gate by gate basis. The circuitry takes the start velocity-bin number and the last velocity-bin number for a continuous group of detections, sums them, and then divides by 2. If, for adjacent range gates, the velocity centroids are within 1 filter then the detection is assumed to be from the same target and only one detection entry is saved. Thus, the velocity centroiding action is used to narrow down the number of indicated detections for processing.

For range-gate centroiding the FFT output for each velocity-bin used is accumulated over the entire integration

period of 1/4 second. Then the most intense return for a velocity-bin on a range-gate basis is further subdivided by using the adjacent range-gate PDI values to form a weighted centroid. The centroiding function is performed by a micro-processor which, in addition, corrects for any detection non-linearity and STC if used.

3.1.3 TERRAIN AVOIDANCE/TERRAIN FOLLOW (TA/TF) MONOPULSE

3.1.3.1 Introduction

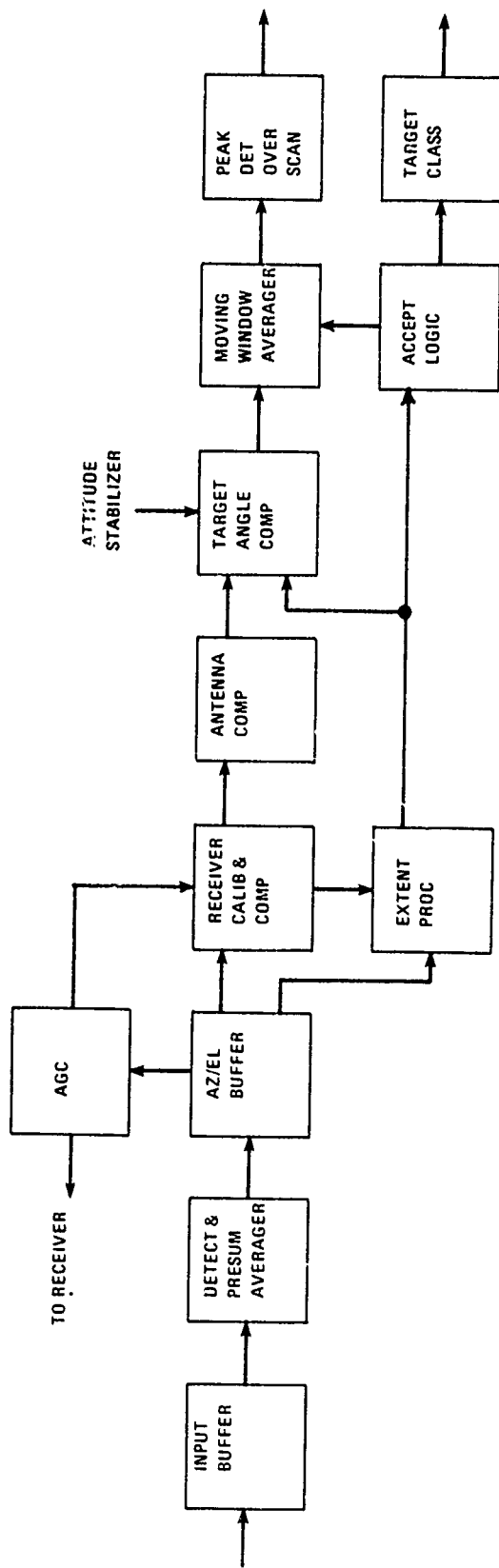
An overall block diagram of a signal processor for a monopulse terrain follow and terrain avoidance radar is shown in figure 3.1.3-1. The radar used with this processor is a non-coherent, phase-monopulse, pulsed radar system which alternately operates in the azimuth and elevation dimensions. Of the many blocks composing the signal processor, four are of most interest to the APUP study in terms of suitability for implementation using CCD techniques. These four are the input buffer, the detector and presum averager, the azimuth-elevation buffer, and the receiver calibration and compensation block. These four blocks comprise the bulk of the memory and processing load. Also, the processing rates in these blocks are best suited for CCD implementation. For these reasons the discussion which follows concentrates on these blocks.

3.1.3.2 Input Buffer

The radar receiver outputs to the input buffer comprise four video signals, as follows:

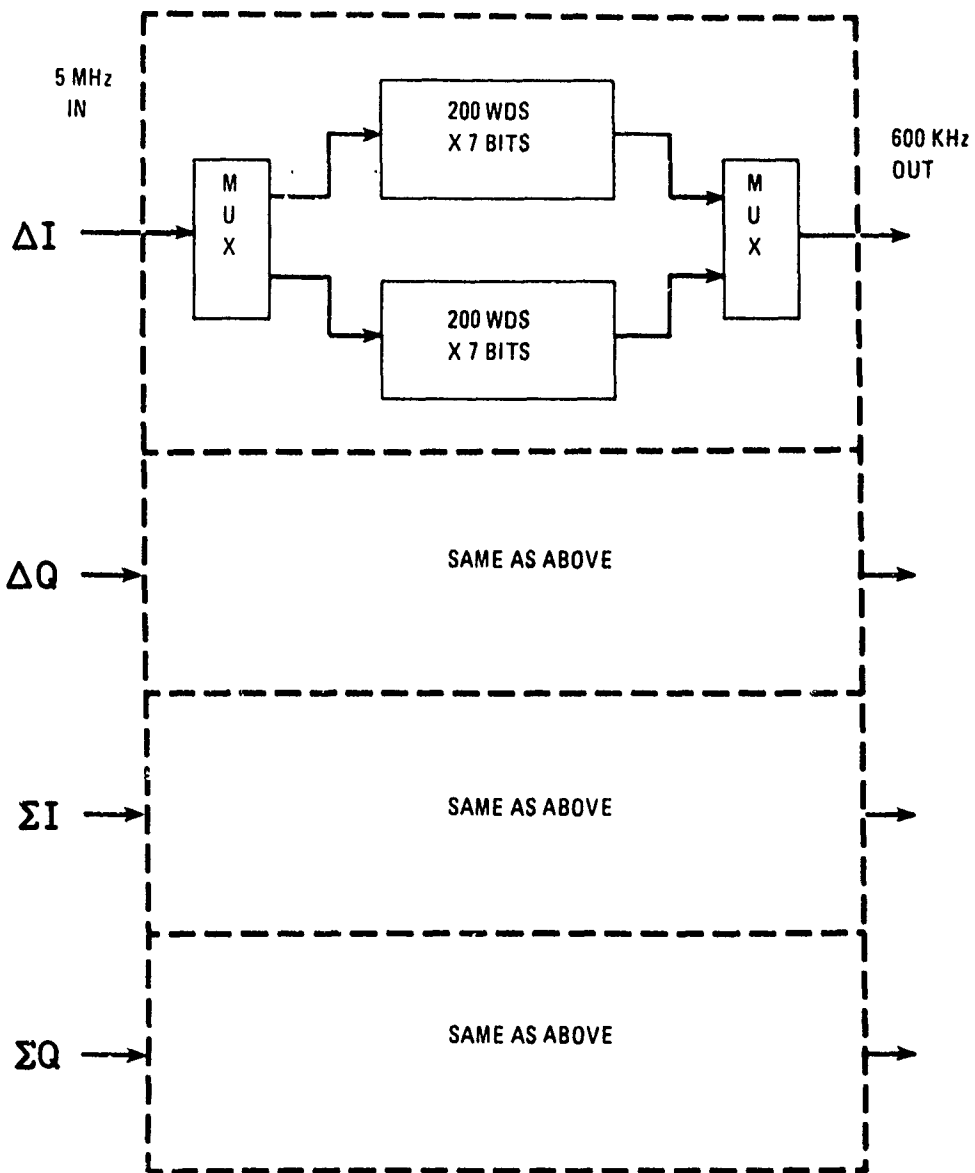
1. In-phase sum (ΣI)
2. Quadrature sum (ΣQ)
3. In-phase difference (ΔI)
4. Quadrature difference (ΔQ)

These signals are the result of heterodyning the radar signals to a "zero-frequency IF". Consequently, they are bipolar video signals. The radar produces these signals during only a small fraction of the interpulse period. The function of the input buffer (block diagram in figure 3.1.3-2 is to take advantage of this fact by spreading the data flow uniformly over the entire



80-0132-V-18

FIGURE 3.1.3-1: Block Diagram of a Signal Processor for Terrain-Follow/Terrain-Avoidance Radar



80-0132-V-17

FIGURE 3.1.3-2: Block Diagram of Input Buffer

interpulse period. This is done by double-buffering. One buffer register is rapidly loaded during the active portion of the interpulse period, while the other buffer outputs its data at a uniform, much lower rate.

A substantial reduction of the data rate is achieved this way. For example, the following may be taken as typical numbers. Let the pulse width of the radar be .2 microseconds, the PRF be 3000 pps, and let the radar collect data over a 40-microsecond range window. Then the peak data rate at the input to the buffer is 5 MHz, but the buffer slows this to a rate of only 200 samples X 3000 sets of samples = 600 KHz. This is a reduction ratio of over 8 to 1. The reduced data rate is much easier for the subsequent processing circuits to handle.

3.1.3.3 Detection and Presum

The block diagram of the detection and presum operations is given in figure 3.1.3-3. It must be remembered that even though the signals leaving the input buffer are at video frequencies, they are analogous to IF signals in that they have not yet been detected. The magnitudes of the sum and the difference signals are found by squarelaw detection. Each squarelaw detector contains two multipliers and one adder, as shown in figure 3.1.3-4. It forms the expression $a^2 + b^2$ where a and b are the inputs to the detector.

The angular information is contained in the relative phases of the signals. It is extracted by complex multiplication of the sum and difference signals. The complex multiplier, illustrated in detail in figure 3.1.3-5 forms the product of two complex signals:

$$(a + jb) \cdot (c + jd) = (ac - bd) + j(ad + bc)$$

It can be seen that the complex multiply operation includes four multiplies and two adds and is equal in complexity to two squarelaw detections.

The speed required of the squarelaw detectors and of the complex multiplier is approximately 500 to 600 KHz. The dynamic range, as presently implemented in digital processors,

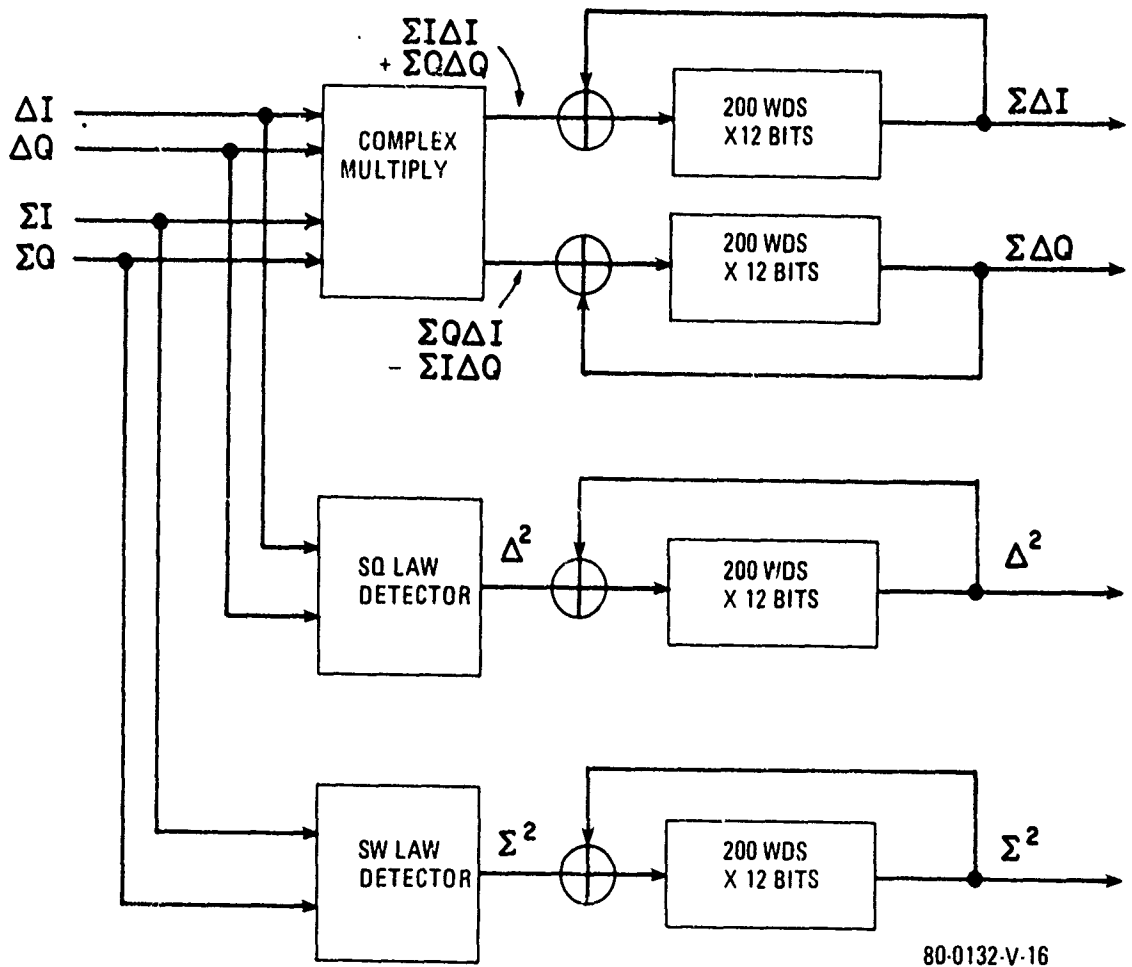


FIGURE 3.1.3-3: Detection and Presum Averager

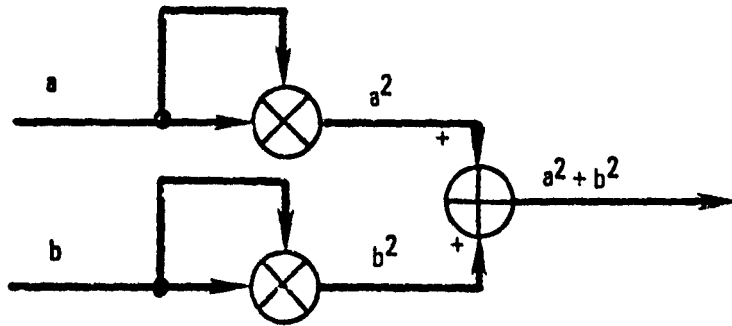


FIGURE 3.1.3-4: Square-law-Detector

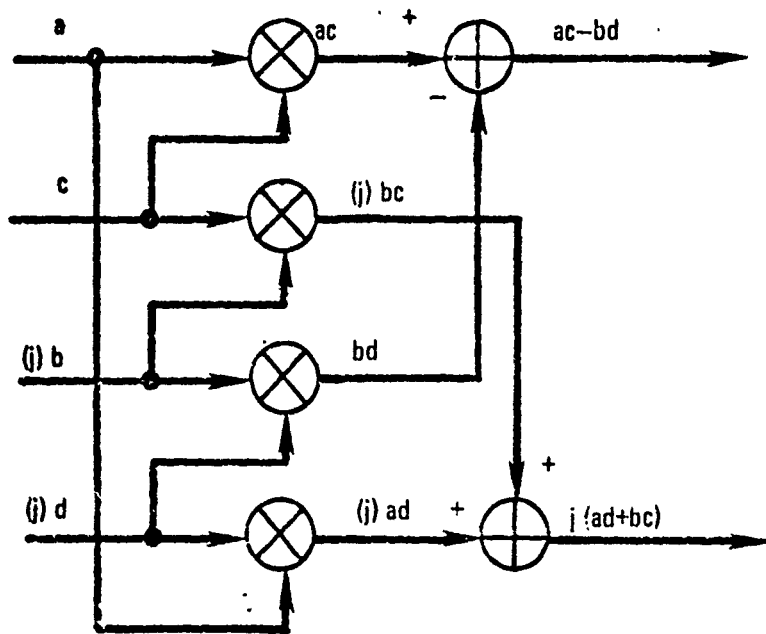


FIGURE 3.1.3-5: Complex Multiplier

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is 2^7 at the input and 2^{11} at the output.

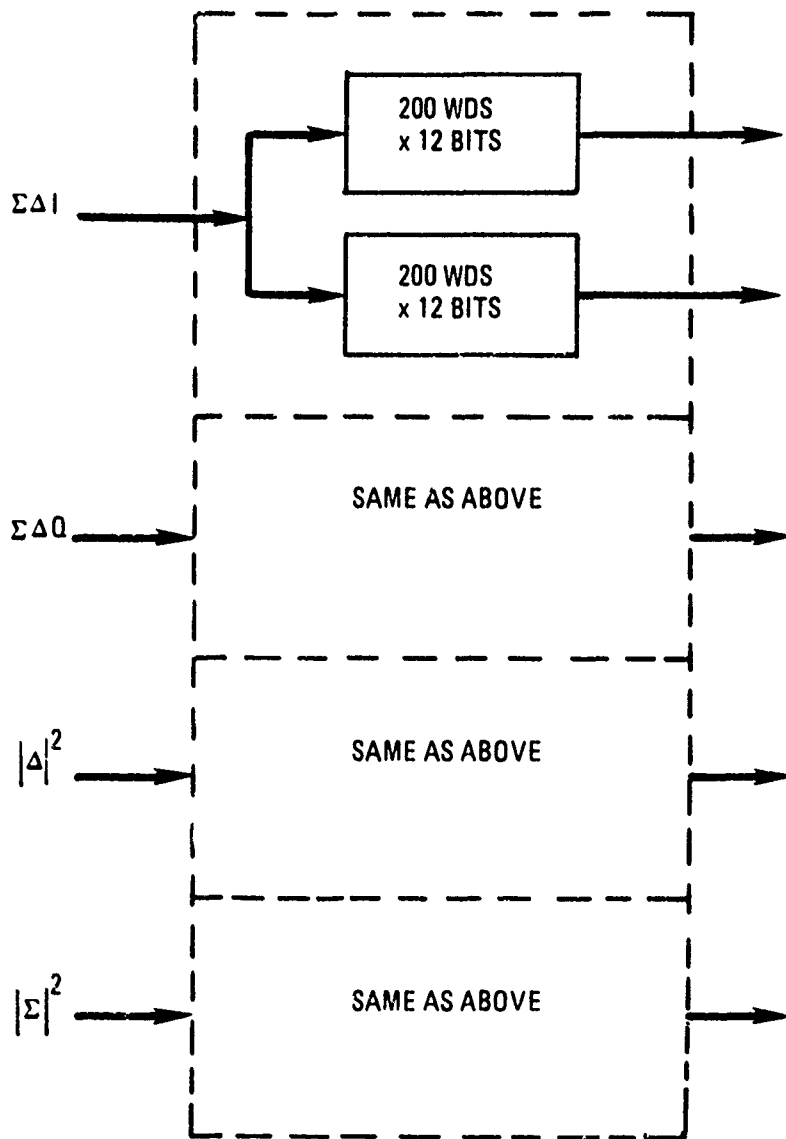
The signals leaving the detection operations are measurements made on a single-pulse basis. The next step in the processing procedure is pulse-to-pulse integration. This step is required if pulse-to-pulse frequency diversity is used by the radar. Typically, the radar might transmit groups of five to ten sequential pulses, each pulse within the group being of a different frequency. The monopulse direction may be shifted between azimuth and elevation after each group of pulses. The recirculating registers shown in the block diagram and the signal returns for each pulse within the group form an average over the range of frequencies. At the end of each group the register is cleared and the integration process is restarted on the next group.

The length of the register must accommodate the total number of range gates, 200 being a typical number. In present implementation, occasional saturation of this register is allowed so that a dynamic range of only 2^{12} need be provided for. Modifications of the processing scheme might lower this range further. The access rate of the register is roughly 600 KHz, and the storage time is 330 microseconds.

Note that the presum registers accomplish a reduction in the average data rate, the reduction factor being equal to the number of pulses integrated. Assuming that six pulses are integrated, the average rate at the integrator output is down to approximately 100 kilohertz. The peak rate remains at the 600 KHz rate, however.

3.1.3.4 Azimuth-Elevation Buffer

The block diagram of the azimuth-elevation buffer is shown in Fig.3.1.3-6. It is at this point in the signal processor that demultiplexing of the azimuth and elevation information occurs. The information collected during the six or so pulse repetition intervals comprising an elevation data collection period is gated into one set of buffers, and the azimuth data is similarly gated into the other set. The average data rate after the



80-0132-V-14

FIGURE 3.1.3-6: Azimuth-Elevation Buffer

demultiplexing operation is therefore only 50 kilohertz, although the peak rate is still 600 kilohertz. If the azimuth and elevation buffers are read out as slowly as possible between the bursts of incoming data, then the peak data rate out of the buffers would be only 60 kilohertz. Double buffering would probably not be worthwhile, since it would result in a further reduction of only 0.167 to 50 kilohertz.

3.1.3.5 Receiver Calibration and Compensation

The buffered azimuth and elevation signals must be corrected for phase and amplitude imbalance in order to yield accurate measurements. As shown in Fig. 3.13-7 this is done by complex multiplication of the signals with inphase and quadrature corrections supplied by a calibration memory. The corrections are derived during an in-flight calibration mode that injects test signals into the Σ and Δ receiver channels. The corrections are applied only to the phase angle signals. The magnitude signals do not need a correction. The corrections must be derived and stored to cover the frequency range of the radar.

The final operation in this processing block is the normalization of the signals by the $|\Sigma|^2$ signal. This operation is indicated in the block diagram as division, but in a digital implementation of this processor was actually performed by multiplication by the reciprocal of the $|\Sigma|^2$ signals. The reciprocal was obtained by a look-up table with a dynamic range of 10 bits.

3.1.4 AIRBORNE NOSE-MOUNTED MAPPING RADARS

3.1.4.1 General

The modes of operation that these radars are used for primarily deal with navigation, navigation avionics update, and target cueing for FLIR, LLTV, or Laser. A principal signal processing function utilized by these radars is that of doppler beam sharpening for azimuth resolution improvement. The following sections describe the general processing requirements, configuration, and example parameters for this type of processing.

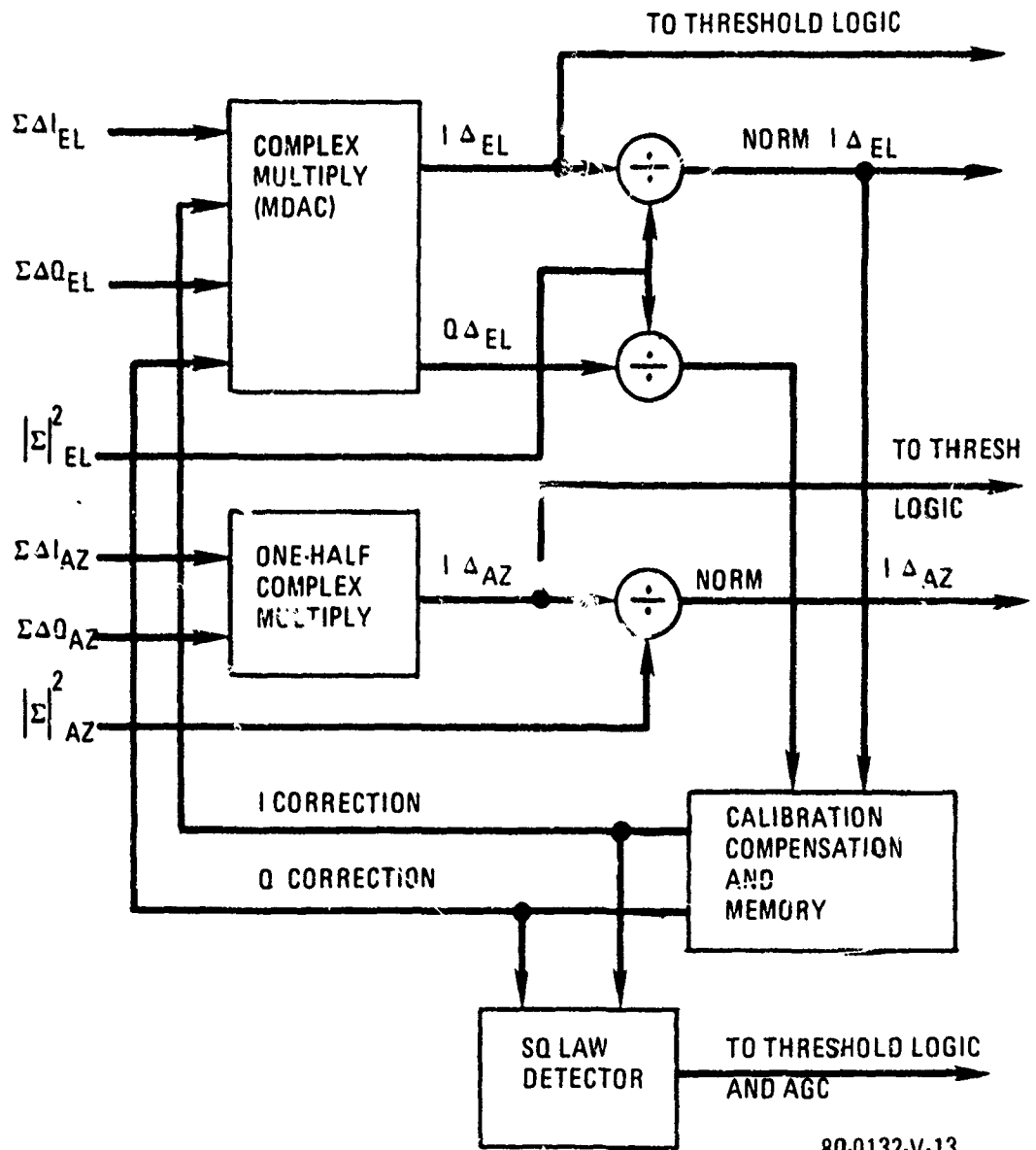


FIGURE 3.1.3-7: Receiver Calibration and Compensation

3.1.4.2 Unfocused Doppler Beam Sharpening

Unfocused Doppler beam sharpening (DBS) effectively divides the antenna far-field real bandwidth into M sub-beams, where M is the selected beam sharpening ratio. Thus, the azimuth angular resolution (θ_{DBS}) obtained after sharpening is:

$$\theta_{DBS} = \frac{1}{M} \times \frac{K}{D_H}$$

The resultant linear resolution (r_{az}) realized for mapping is:

$$r_{az} (DBS) = \frac{R_S}{M} \times \frac{K\lambda}{D_H} = R_S \times \frac{P_R}{M}$$

The integration time (T_I) for DBS is less than that for an unfocused SAR equipment where the length of the synthetic antenna is selected so that mapping is essentially done at the boundary line between the antenna near- and far-fields. In contrast to DBS, the resolution (at any squint angle) for an unfocused SAR equipment is:

$$r_{az} (\text{unfocused}) = \frac{K_S \sqrt{R}}{2}$$

The integration times for the two types of radars are:

$$T_I (DBS) = \frac{K_S}{K} \times \frac{D_H}{2V \times \sin\alpha} \times M = \frac{K_S \times \lambda \times M}{2V \times \beta_R \times \sin\alpha}$$

$$T_I (\text{Unfocused}) = \frac{\sqrt{\lambda R}}{V \times \sin\alpha}$$

The DBS system is generally used to look left and right of the A/C velocity vector and develop all or segments of a PPI type of map. In this mode of operation there is no DBS improvement realized within the region of 3 real beamwidths from the A/C nose to directly along the ground track where $T_I \rightarrow \infty$, for which the azimuth resolution is that of real beam only. The unfocused SAR is normally used for generating strip maps at broadside or squinted scan angles. The two techniques

(DBS and SAR) can overlap in application if a map sector or spot is required at some squinted scan angle. The scan time for the two equipments when operated in the spot or map sector mode is:

$$T_S \text{ (DBS)} \approx \frac{M}{N_{CC}} \times T_I \times N_{LA} = \frac{K_S \times \lambda \times M^2 \times N_{LA}}{2V \times \beta_R \times N_{CC} \times \sin \alpha} *$$

$$T_S \text{ (unfocused SAR)} \approx \frac{A_z C}{N_{FIL}} \times T_I \times N_{LA}$$

(Note that in the above two equations the T_I values are not the same and the quantity used is that associated with DBS or unfocused SAR).

3.1.4.3 DBS Radar

The DBS radar is implemented by placing a bank of Doppler filters of quantity M , each with a bandwidth corresponding to the Doppler spread across a desired resolution element centered at the peak of the real beam. For M equal to 10, each spatial filter will possess an azimuth resolution capability of $\sim 1/10$ of the real beamwidth.

The requirement for DBS processing results in the target Doppler return remaining principally in one filter channel during T_I . This type of operation removes the need to Doppler de-chirp the input signal prior to azimuth processing or as part of the complex mixer reference. Here, the Doppler frequency change of any target return during T_I is small enough to be considered a constant. With this constraint, a constant reference frequency is generated for each synthetic beam as a function of V_a/c (ground speed) and the azimuth squint angle of that beam.

* N_{CC} in the denominator comes about by the fact that the antenna can scan only N_{CC} filters in a T_I to stay in real time processing.

3.1.4.4 Azimuth Correlator Configuration

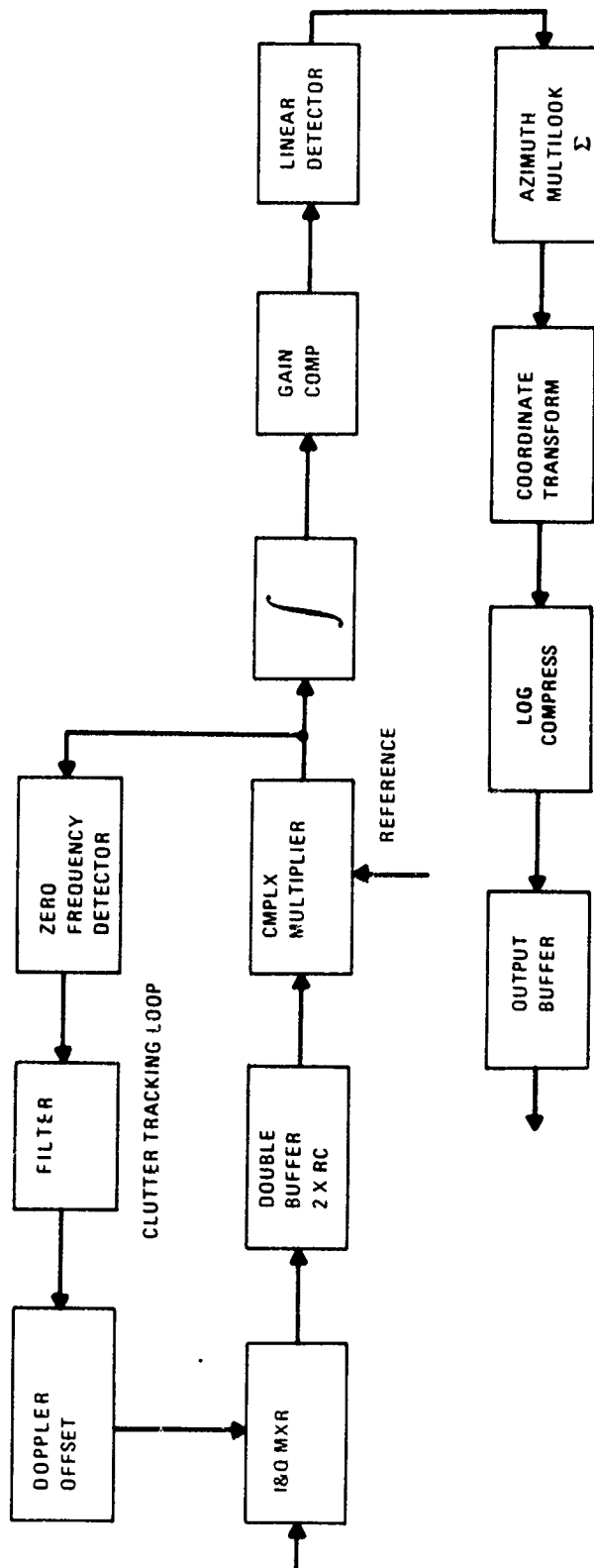
The configuration of a typical DBS azimuth correlator is shown in Figure 3.1.4-1. In this diagram, the IF reference for the I and Q mixer is corrected by the clutter tracker loop which tracks the long term Doppler shift of the spectrum. This correction can also be accomplished as part of the complex multiplier reference. The Doppler clutter tracking loop will be described as a separate equipment processing requirement; it is shown here for continuity. In addition to the tracking correction, a range gate drift correction circuit is implemented in the synchronizer to correct for range changes due to A/C motion. The purpose of both of these functions is to maintain the map at a fixed geographic location during the mapping interval.

The reference signal into the complex multiplier translates the Doppler spectrum of the specific synthetic beam being formed down to DC. The signal is then coherently summed for a period of T_I seconds in an accumulator (linear dumped integrator) constituting a narrow band Doppler filter. Depending on the processing rate capability of the narrow band Doppler filter, the quantity of parallel correlator channels N_{CC} (always $\leq M$) is defined. Parallel channelizing can include the complex multiply and add or be limited to the accumulators only. Fig. 3.1.4-2 shows only the accumulators as part of the parallel channels. The number of IPP's summed in the accumulator N_{COR} which is RC/N_{CC} storage positions in length and dumped every T_I seconds is determined by the Doppler filter bandwidth (Δf_c) required.

$$\Delta f_c = 1/T_I \quad (\text{Where } T_I \text{ is increased by weighting Factor } K_S)$$

$$N_{COR} = T_I \times \text{PRF}$$

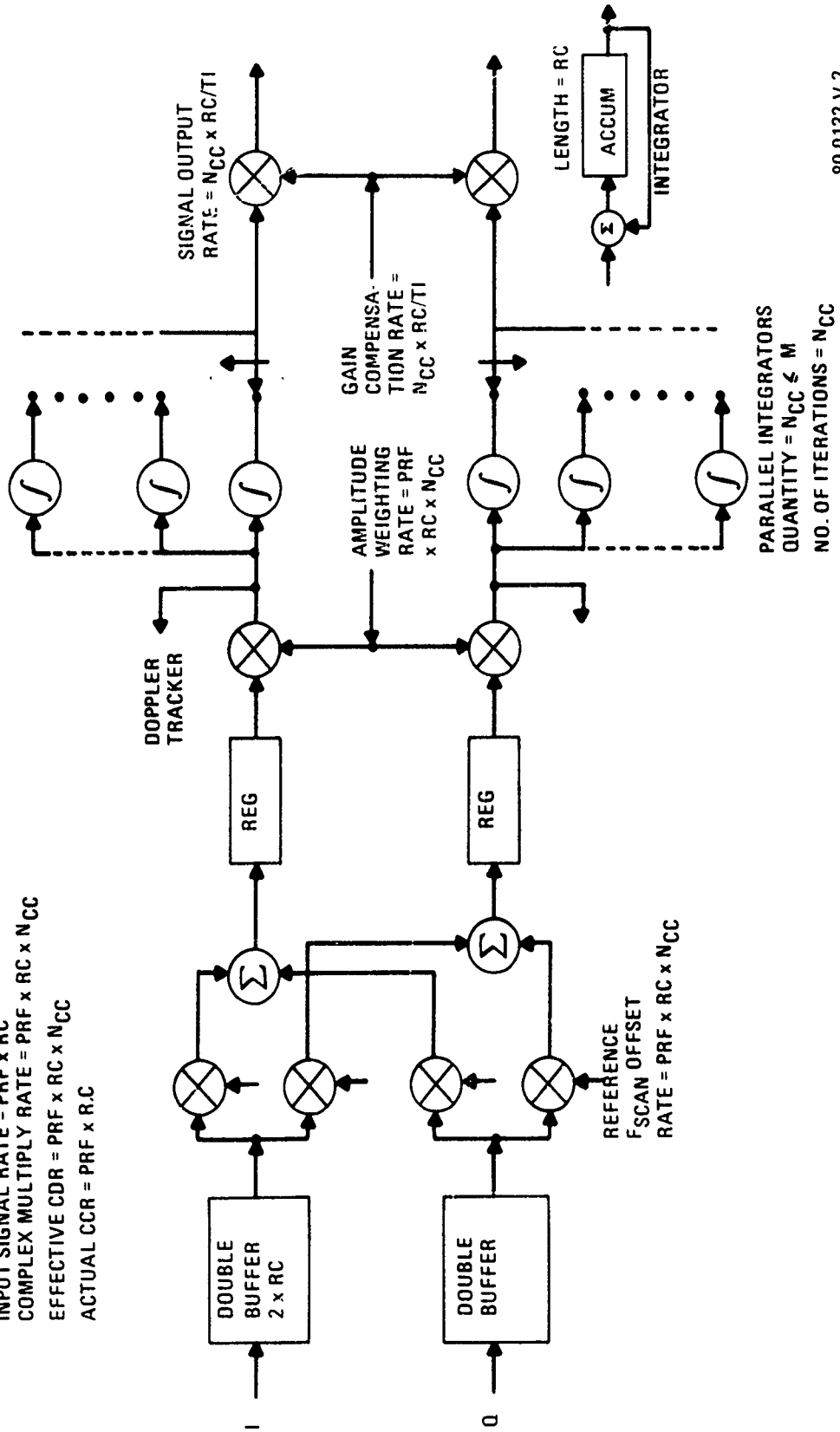
The outputs of the azimuth correlator are then multilook summed and processed through a coordinate transformation routine (polar to rectangular). The transformation utilizes



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FIGURE 3.1.4-1: DBS Signal Processor

INPUT SIGNAL RATE = $PRF \times RC$
 COMPLEX MULTIPLY RATE = $PRF \times RC \times N_{CC}$
 EFFECTIVE CDR = $PRF \times RC \times N_{CC}$
 ACTUAL CCR = $PRF \times RC$



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FIGURE 3.1.4-2: DBS Correlator

a "cardinal-data-hold" interpolation algorithm prior to being passed through log compression to limit the word size.

3.1.4.5 Numerical Examples

The azimuth correlator integration gain is:

$$\text{Integration Gain} = T_I \times \text{PRF}$$

This value assumes that the scene mapped has specular targets. If the scene is primarily made up of clutter-type targets, the gain is equal to the square root of this quantity.

The azimuth CDR is given by the following (assuming that the complete interpulse period is available for processing):

$$\text{CDR} = \text{PRF} \times \text{RC} \times M$$

If parallel filter channels are used, the correlator channel rate (CCR) is inversely related to N_{CC} . Normally with VLSI the N_{CC} quantity available equals largest M.

$$\text{CCR} = \frac{M}{N_{CC}} \times \text{PRF} \times \text{RC}$$

Table 3.1-6 lists the typical parameter limits which an airborne radar with this mode might expect to encounter.

Table 3.1-7 utilizes the unfocused DBS equations for r_{az} , T_I , T_S and CDR and the input parameters from table 3.1-6 to illustrate example equipment operating values for $M = 10, 15, \text{ and } 20$ and for R_S varying between 2 and 50 nmi. The quantities N_{CC} and N_{LA} were set equal to one for purposes of normalization.

3.1.4.6 Memory Considerations and Configuration Options

The purpose of the input buffer is to stretch out the range returns over a complete IPP. The complex multiply is done for N_{CC} filters, RC range cells at the PRF rate. This means only N_{CC} filters are processed and that the scan rate (frame time) must be adjusted (slowed down) in order to retain the real-time processing function, optimum is with N_{CC} equal to the largest M value. (The register after the complex multiply is not required unless time isolation is necessary.)

TABLE 3.1-6: TYPICAL RADAR PARAMETER LIMITS

R_s	2 to 50 nmi
$V_{a/c}$	150 ft/s to 1500 ft/s
ψ (antenna scan angle)	-65° -- 0° -- $+65^\circ$
γ (radar wave length)	.1' to .25'
$h_{a/c}$ (aircraft altitude)	200' to 75K'
r_{rg} (range resolution)	50' to 200'
r_{az} (azimuth resolution)	0.1° to 0.5°
M (beam sharpening ratio)	7 to 20
N_{LA} (azimuth multilooks)	1 to 4
N_{CC} (number of parallel correlator channels)	1 to M
β_R (antenna real beam width)	1 1/2 to 6°
PRF	500 to 4000

TABLE 3.1-7: DBS OPERATING EXAMPLE VALUES*

M	V	R_s	r_{az}	T_I	T_s	A	B	N_{COR}
	(ft/s)	(nmi)	(ft)	(sec)	(sec)	(MHz)	(MHz)	
10	150	2	42.4	.239	.239	.2	2	478
10	↓	8	169.7	"	"	↓	"	"
10	↓	14	296.9	"	"	↓	"	"
15	↓	20	282.8	.358	.358	↓	3	716
15	↓	26	367.6	"	"	↓	"	"
15	↓	32	452.5	"	"	↓	"	"
20	↓	38	403	.477	.477	↓	4	954
20	↓	44	466.6	"	"	↓	"	"
20	↓	50	530	"	"	↓	"	"

$N_{LA} = 1$, PRF = 2000, RC = 100, $\alpha = 30^\circ$, $\beta_R = 2^\circ$, $v = .1'$, $N_{CC} = M$,
 $K_s = 1.25$

$A = PRF \times RC$, $B = PRF \times RC \times N_{CC}$

*Values in table are for fixed operating constants; see Table 3.1-6 for range of constants.

Figure 3.1.4-3 has essentially the same operation as Figure 3.1.4-2 except more of the circuit is duplicated in order to reduce the data rate in the complex multiply. The MUX of the Doppler filters can either be done at point A or B on the diagram, and the gain compensation and linear detection blocks can be interchanged, depending on ease of mechanization.

An alternate to multiplying the frame time by N_{LA} is to multiply N_{CC} by N_{LA} which assumes room enough on chip to accommodate extra filters.

3.1.5 SPOT MODE

In "spot" mode operations, the antenna is steered so as to "spotlight" a single point on the ground while the A/C continues on its path. This single area within the beam is illuminated for a longer time than a fixed antenna aim would provide on a normal fly-by so that the "crossrange" (azimuth) resolution can be improved by the greater integration time. It is not SAR, but on a sidelook it produces more resolution than DBS. The signal processing components are characterized in the following sections.

3.1.5.1 Correlator Input Buffer

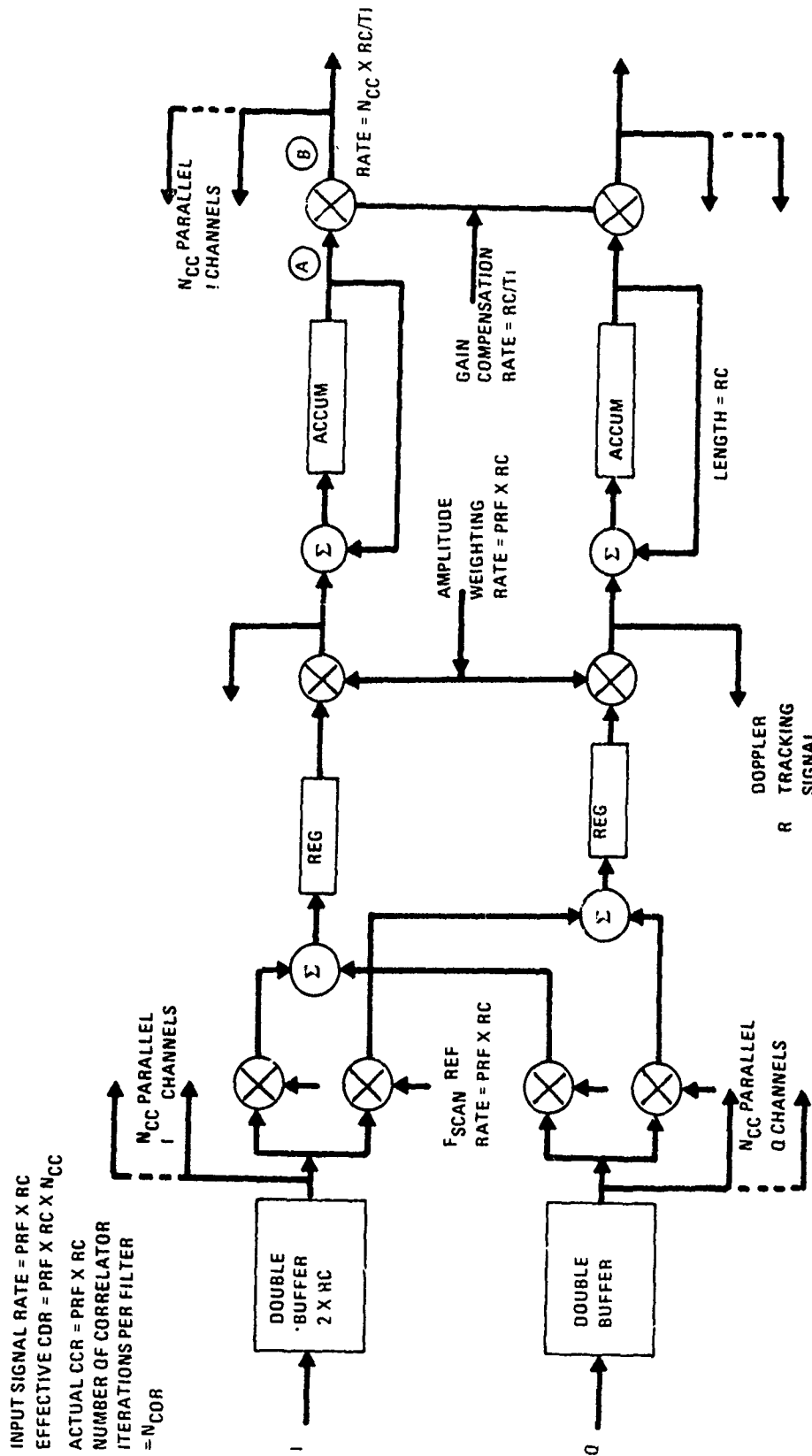
1. Reduces the data rate in range by spreading the range gates equally over entire IPP.
2. If multilook in range is used, it allows summing of adjacent gates to give desired range resolution.
3. Size of buffer is twice the length of one range swath since item (1) above introduces a read-out slow down.

$$\text{Min. Buffer Size} = 2 \times RC$$

$$RC = \text{Number of range gates or cells.}$$

3.1.5.2 Azimuth Prefilter

1. Reduces the azimuth processing bandwidth with a narrow band filter to that required to match the Doppler band to be correlated, Fig. 3.1.5-1.
2. In squint mode operation, the prefilter removes the Doppler offset by using a scanning reference.



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FIGURE 3.1.4-3: DBS Correlator (Alternate)

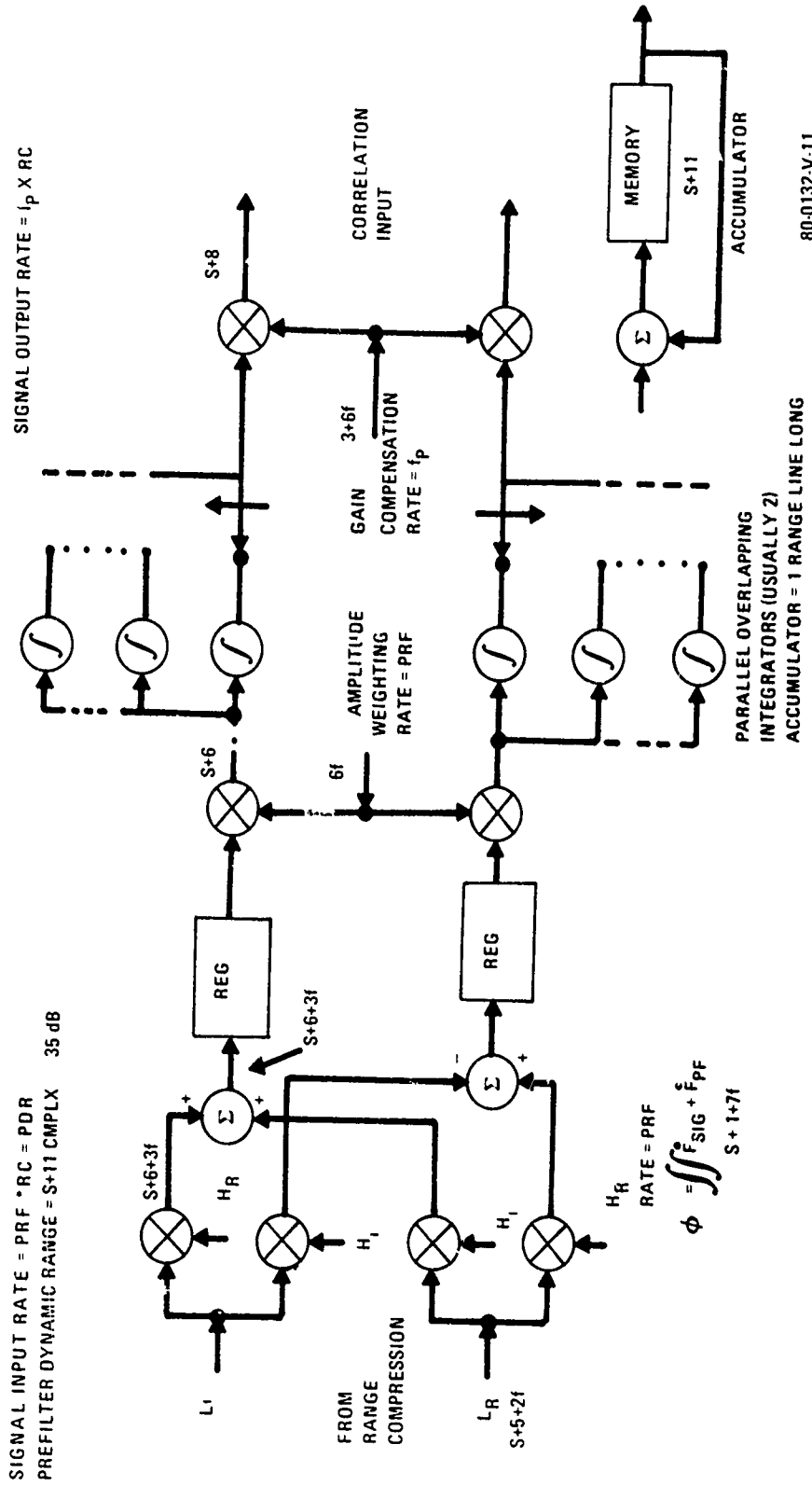


FIGURE 3.1.5-1: Prefilter

$$\Delta f_{\text{DOP}} = K_s \left(\frac{V \sin \alpha}{r_{\text{az}}} \right)$$

$$\Delta f_{\text{PRE}} = K_{\text{OS}} (f_{\text{DOP}}) = \text{prefilter bandwidth}$$

$$N_{\text{PRE}} = \frac{\text{PRF}}{f_{\text{DOP}}} = \text{number of pulses summed in one prefilter channel}$$

$$f_{\text{P}} = N_{\text{OL}} \frac{(\text{PRF})}{N_{\text{PRE}}} = \text{prefilter output sample rate (when a prefilter is used)}$$

$$N_{\text{FIL}} = f_{\text{DOP}} \times T_{\text{I}} = \text{number of correlator filters}$$

$$N_{\text{COR}} = f_{\text{P}} \times T_{\text{I}} = \text{number of pulses correlated (with prefilter); PRF} \times T_{\text{I}} \text{ otherwise}$$

$$T_{\text{PRE}} = \frac{N_{\text{PRE}}}{\text{PRF}} = \text{prefilter integration period}$$

$$T_{\text{I}} = \frac{K_s R_s}{2 V r_{\text{az}} (\sin \alpha)} = \text{coherent integration time}$$

3.1.5.3 Corner-Turn Memory (Prefilter to Correlator)

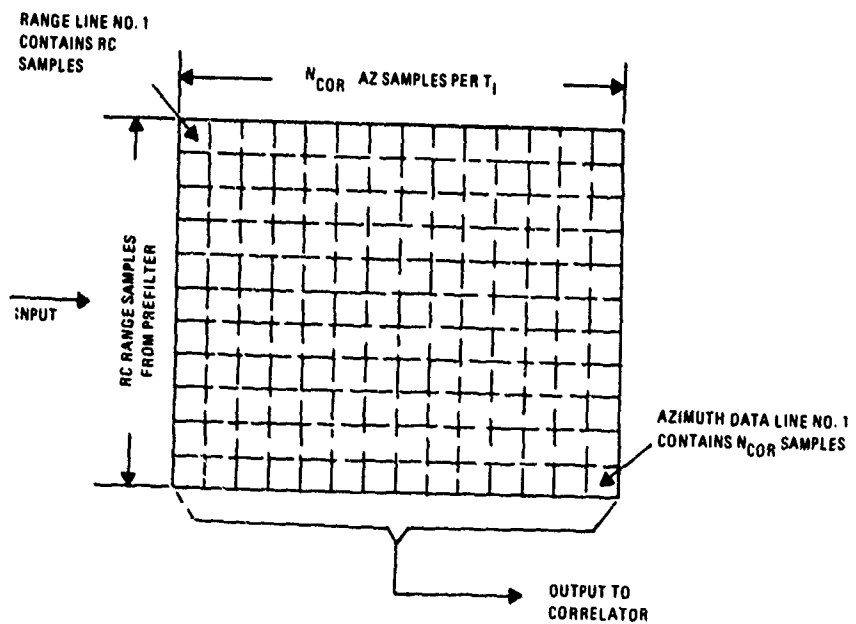
The memory stores consecutive prefilter outputs (range lines). Azimuth lines of samples, N_{COR} in length, are then made available to the correlator at a rate of one azimuth line per correlator integration time (T_{I}), Fig. 3.1.5-2.

$$\text{Memory size} = 2 \times N_{\text{COR}} \times \text{RC} \times 2$$

(The first "2" is for I and Q, and the second for double buffering).

3.1.5.4 Azimuth Correlator

1. Processes one azimuth-line at a time from bulk memory. With each line consisting of N_{COR} range-line samples of one range cell (RC) duration. Each sample is multiplied by a complex reference frequency, and then accumulated over a period equal to T_{I} to form one narrowband Doppler filter, Fig. 3.1.5-3.
2. The complex reference function cancels the FM due to scanning the prefilter and provides amplitude weighting for azimuth sidelobe control.
3. Next, the signal is hardlimited and the magnitude de-



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FIGURE 3.1.5-2: Corner-Turn Memory

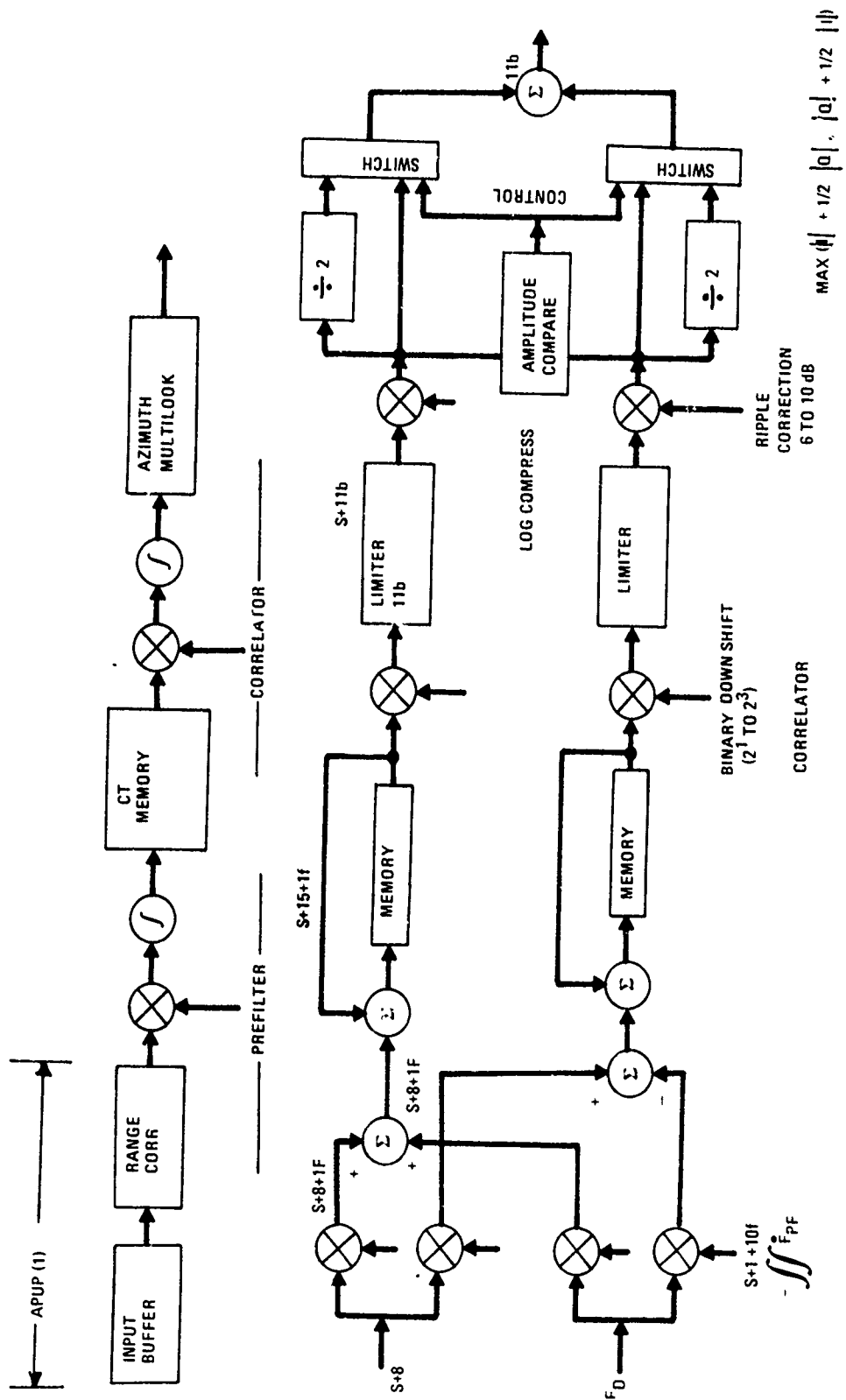


FIGURE 3.1.5-3: Azimuth Correlator

terminated from a $\max(|I| + 1/2|Q|, |Q| + 1/2|I|)$ test.

4. Finally, multilook in azimuth is performed by either of the following:

- a. Collect two sequential sets of N_{COR} samples over a period of $2 \times T_I$, correlate each coherently, and sum the two results non-coherently.
- b. Operate two correlators in parallel and then non-coherently sum the outputs.

3.3.5.5 Options to Accommodate N_{LA}

1. Calculate N_{FIL} , T_I , and CDR on the single azimuth look resolution basis and slow down the scan T_S by the factor N_{LA} .
2. Calculate N_{FIL} , T_I , T_S on the single azimuth look resolution basis and speed up the correlator data rate by N_{LA} .
3. Calculate CDR on a single look basis. Set the quantity of parallel correlators equal to N_{LA} .

TABLE 3.1-8

R_s	5 to 50 nmi
$V_{a/c}$	150 ft/s to 1500 ft/s
α	-45° -- 0° -- $+45^\circ$
γ	..'
altitude	200' to 75K'
r_{rg} and r_{az}	10' to 50'
spot size (azimuth or range cells)	1000^2 to 10000^2 cells
azimuth multilooks	1 to 4
N_{OL} (prefilter, sample rate improvement)	2 to 3
Range (time X bandwidth)	10 to 1000
Max. Range Pulsewidth (Transmit)	50
Quantity of Radar Range Compression Ratios	1 to 6

$$\text{Min. allowed PRF} = K (K_s \times V_{a/c} \times N_{LA} \times \sin\alpha) / r_{az}$$

$$f_{PRE} = (K_{os} \times V_{a/c} \times \sin\alpha) / r_{az}$$

$$PDR = PRF \times RC$$

TABLE 3.1-9

f_{PRE}	PRF min. (PPS)	PDR	N_{LA}	r_{az} (ft.)	α (deg.)	V ('/s)
6	9	2700	1	50	90	150
22	32	9600	1	10	45	150
60	90	27000	1	50	90	1500
212	318	95400	1	10	45	1500
6	36	10800	4	50	90	150
22	85	25500	4	10	45	150
60	360	108000	4	50	90	1500
212	849	254700	4	10	45	1500

$$T_s = \frac{K_s \lambda \times AZC \times (R_s^2 - h_{a/c}^2)^{1/2} \times N_{LA}}{2 N_{FIL} r_{az} \frac{V_{a/c}}{\sin(\alpha)}} = \frac{T_I \times AZC \times (R_s^2 - h_{a/c}^2)^{1/2} \times N_{LA}}{R \times N_{FIL}}$$

$$T_s \approx \frac{MW \times \sin \alpha \times (R_s^2 - h_{a/c}^2)^{1/2} \times N_{LA}}{K_s R_s V_{a/c}}$$

$$CDR = N_{COR} \times \frac{N_{FIL}}{T_I} \times RC \approx \frac{K_s^3 \times \lambda \times R_s \times V_{a/c} \times RC \times N_{OL} \times \sin \alpha}{2 r_{az}^3}$$

TABLE 3.1-10

N_{FIL}	R_s (nmi)	$V_{A/C}$ (ft/sec)	RC	N_{OL}	r_{az} (ft)	α (deg)	CDR (hz)	T_s min (1 look)
11	50	150	300	2	50	90°	27573	71.8
11	↓	↓	↓	↓	50	45°	19497	101.5
16	↓	↓	↓	↓	40	90°	46670	61.7
16	↓	↓	↓	↓	40	45°	33000	87.2
20	↓	↓	↓	↓	30	90°	114989	45.4
29	↓	↓	↓	↓	30	45°	81210	64.2
65	↓	↓	↓	↓	20	90°	385121	30.4
65	↓	↓	↓	↓	20	45°	272322	42.9
257	↓	↓	↓	↓	10	90°	3010285	15.4
257	↓	↓	↓	↓	10	45°	2128539	21.8

3.2 SPACEBORNE RADARS

An illustrative example of spaceborne radars is the SEASAT SAR for ocean surveillance and mapping. The objective of the SEASAT SAR is to image ocean waves with a 25-meter resolution in a 100km wide swath from a circular near-polar orbit of approximately 800km with a slant look angle of $20^{\circ} \pm 3^{\circ}$ off vertical. Such fine resolution across track is obtained by effectively time-gating the returns into 4000 range resolution cells via a range clock of nearly 19MHz. Practical satellite implementation dictated the use of pulse compression in order to minimize the peak transmitted power required to get adequate signal-to-noise ratio. Consequently the SEASAT SAR uses a linearly-swept FM pulse with a 634 to 1 pulse compression ratio, 19MHz bandwidth, and 34 μ sec duration, generated by pulsing a surface acoustic wave (SAW) device. To realize the needed resolution along track, which is much finer than the antenna beam pattern incident on the ground, approximately 3000 return echoes are processed coherently at a maximum PRF of 1645Hz.

The typical processing sequence of the video from the L-Band return pulses is the following:

- 1) Pulse compression to collapse the signal from a point target into a single range resolution cell.
- 2) Coherent accumulation of data in a two-dimensional array of (4000 range cells) by (3000 return echo lines).
- 3) The centroids of the Doppler spectrum for selected lines of the 3000 are used to more accurately specify the ground map elements than allowed by the antenna boresight knowledge (range migration correction).
- 4) Precise knowledge of the ground position (including latitude) specifies the azimuth matched filter or cross-correlation operation performed on each column or range bin of the 2-D array; and like the range

compression process, this collapses a point target to a single azimuth resolution element.

- 5) Noncoherent integration of a maximum of four independent looks reduces the standard deviation of the return signal strength measurement, effectively smoothing the texture of the radar image & reducing its monochromatic speckly nature, but demands processing the data 4 times, generating 4 separate images and registering the 4 images prior to integration.

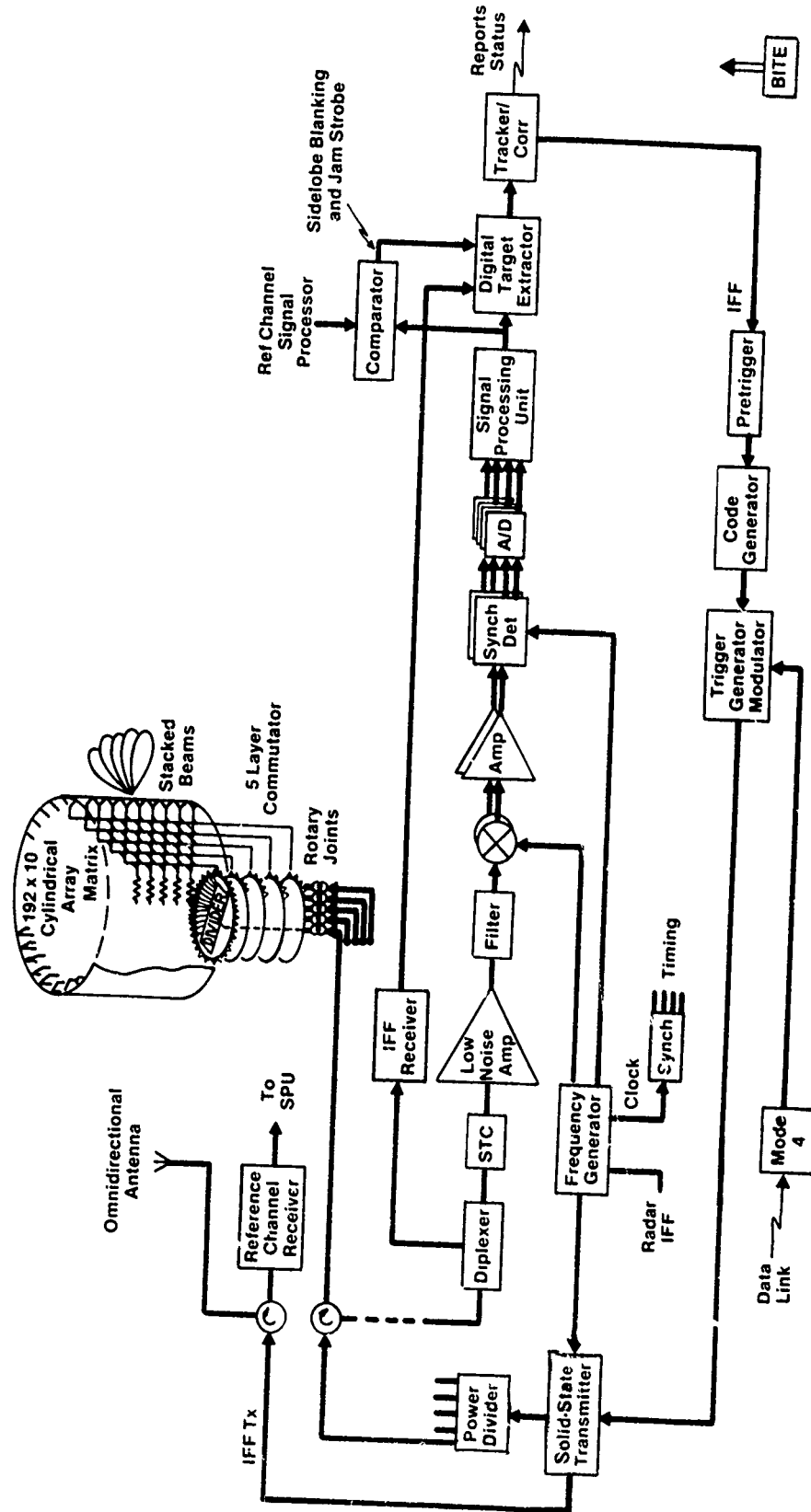
Presently, all this data processing is performed on the ground, not in real time, by either a digital computer or by optical techniques using film, coherent light and lenses. Suggested block diagrams for CCD implementation of the above data processing have been developed under NASA Contract # NAS-7-100 at Caltech JPL and published at the American Institute of Aeronautics and Astronautics by Wayne Arens.

3.3 GROUND OR SHIP BASED RADARS

Most of these radars employ pulse techniques resulting in unambiguous range but ambiguous Doppler information. Consequently, optimally weighted filter techniques are generally preferred to Fourier transform schemes except for systems with ranges less than 80 nautical miles which can use Doppler bank filters similar to the moving target detection (MTD) approach of the MIT Lincoln Laboratory. Because of moderate sample rates ranging from 0.25MHz to 2MHz, hardwired pipelined implementation is generally used, although array technology and microprogrammed processors are making inroads. While both serial and parallel arithmetic are employed, performance of existing systems is typically limited by the analog-to-digital converters (ADC) and/or memory.

The system block diagram for an illustrative example of an unattended radar is given in Figure 3.3-1 with more details on its signal processing unit and its "Track-While-Scan" (TWS) post-processor shown in Figures 3.3-2 and -3. Because CCDs can also be used for feature extraction, cross-correlation, or associative processing, as well as the bulk memory needed for target track-files, both the coherent and the TWS post-processor are described.

The principal function of the Signal Processor is to provide target detection inputs to the Digital Target Extractor (DTE). The DTE then uses these detections to generate target reports which are fed to the Tracker circuits. Most importantly the signal processor must accomplish its target detection function in an interference environment (noise, clutter, ECM, birds, etc.) without generating an excessive number of false detections. In fact, the number of false detections must be held below the levels that would cause saturation of the DTE or Tracker circuits. Saturation of these circuits would prevent them from accomplishing their primary tasks of generating track reports for all true targets actually present. Adaptive track initiation and maintenance help avoid system overloads resulting from multiple



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FIGURE 3.3-1: Illustrative Example of an Unattended Radar

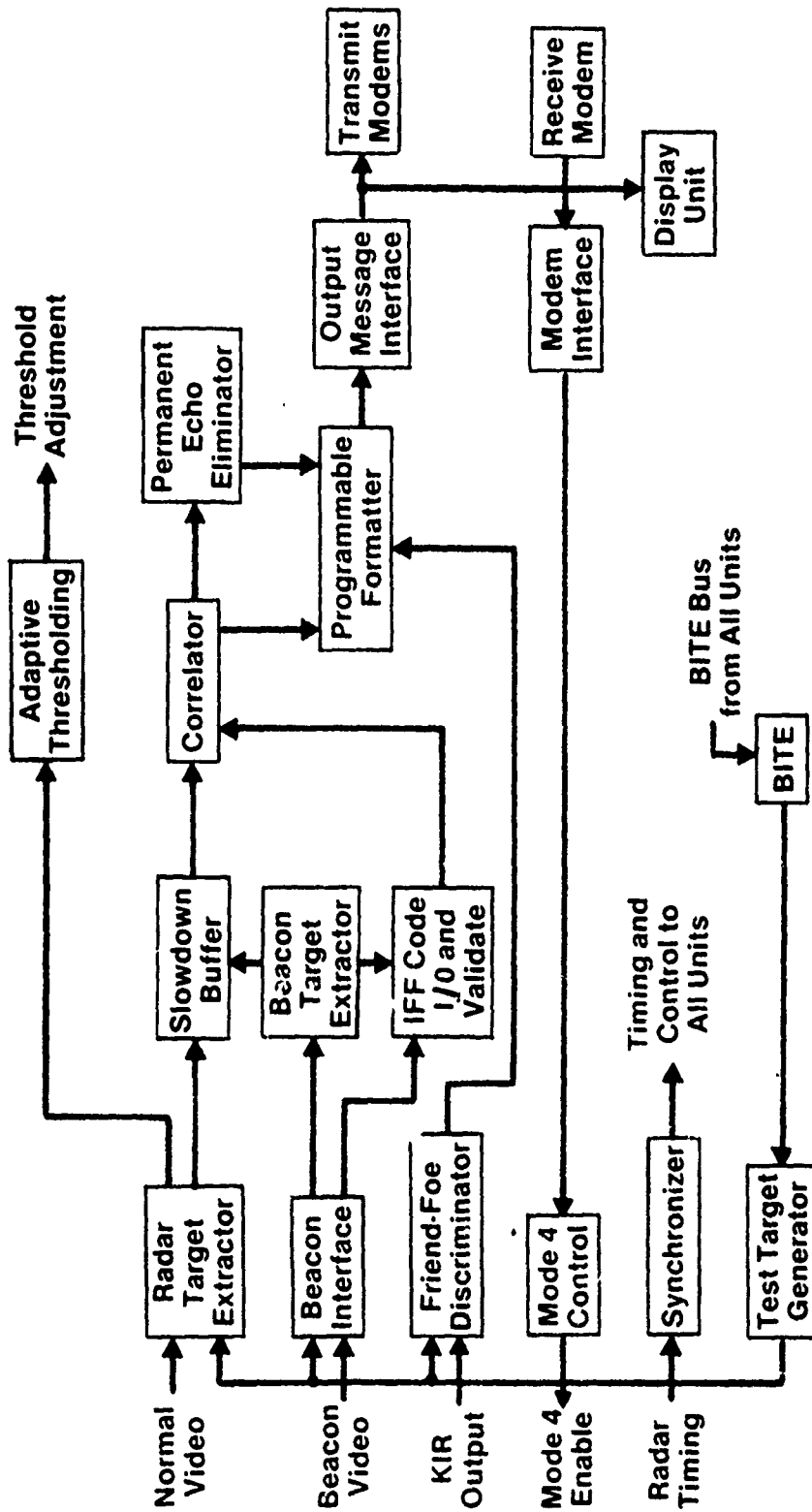


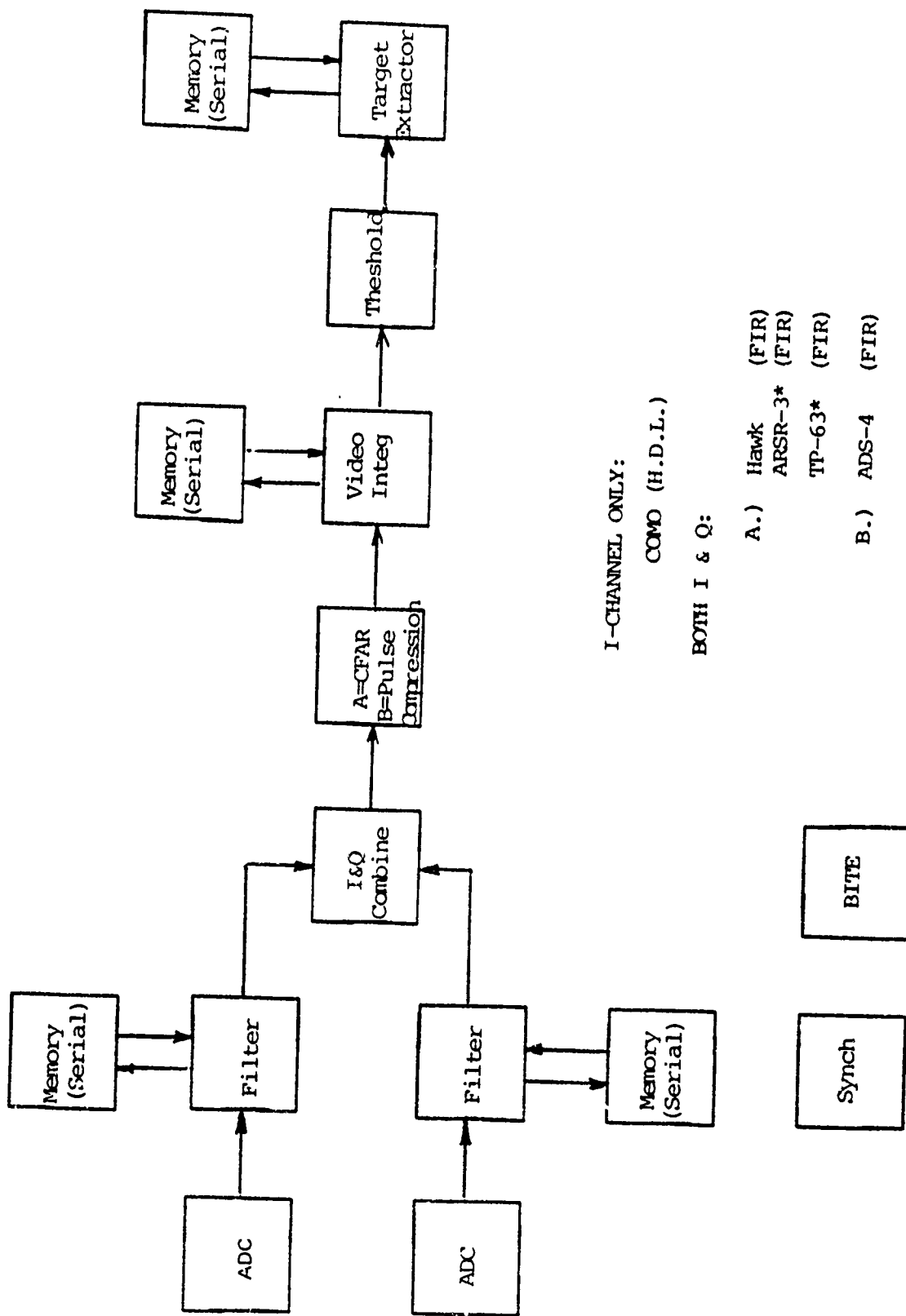
FIGURE 3.3-3: Illustrative Example of a Track-While-Scan (TWS) Post-Processor

S77-0018-VA-9

bird tracks. Another useful feature is automatic velocity discrimination for track reporting, making use of multiple track files: one for slowly moving tracks, one for higher velocity (> 80 knots) tracks, and one for tentative tracks.

A further objective for the signal processor is to maximize the detectability of true targets in the interference environment by taking advantage of spectral or spatial differences between the target echoes and the interference. The signal processor must also have the additional ability of generating jam strobes under ECM conditions. The accomplishment of these signal processor functions implies a number of processor features. Clutter rejection channels are necessary to discriminate between target echoes and ground, sea or precipitation clutter (and possible birds) on the basis of differences in their doppler spectra. Zero velocity channels, in conjunction with clutter mapping, are able to take advantage of the typical spatial inhomogeneity of ground clutter and hence provide inter-clutter and super-clutter visibility in shadowed or low clutter areas of the radar coverage. ECCM requirements include the provision of CFAR capability against noise jamming and the generation of noise jam strobes. Sidelobe blanking is required to restrict the generation of a jamming strobe message to main beam interference.

The typical architecture for a more basic surveillance radar processor is shown in Figure 3.3-4; while Figure 3.3-5 describes a unique variation used for the shipboard radar SPS-65 (which also served as the basis for the high-reliability Micronet implementation study). A concise survey of typical values for ground and shipboard radars for important parameters strongly affecting potential CCD implementation of the processors is given in Table 3.3-1. Furthermore, on the assumption of a CCD-compatible analog signal processor architecturally homomorphic to the digital signal processing, functional partitioning of the processing steps gives the typical analog memory requirements shown in Table 3.3-2. Since the analog memory is an important design factor in the structure of the



I-CHANNEL ONLY:
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BOTH I & Q:

- A.) Hawk (FIR)
- ARSR-3* (FIR)
- TP-63* (FIR)
- B.) ADS-4 (FIR)

*: x2 Channels
 FIGURE 3.3-4: Basic Surveillance Radar Processor

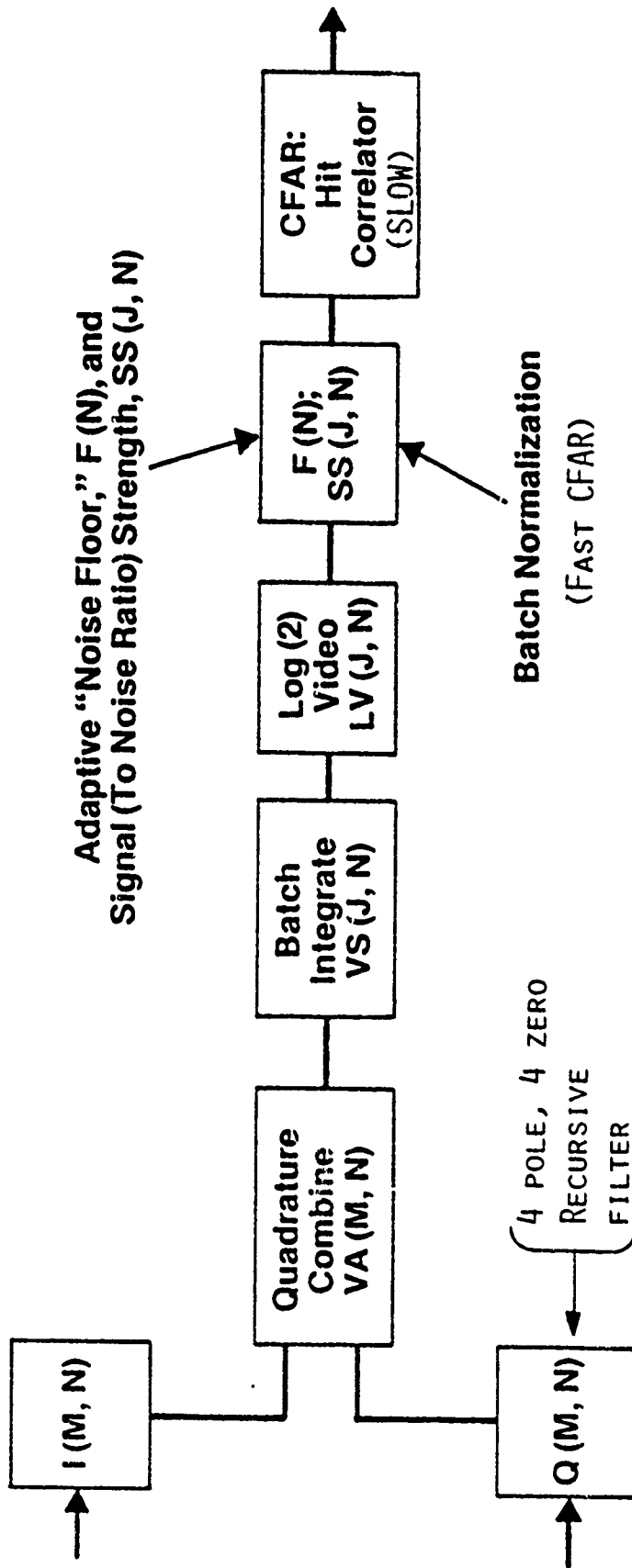


FIGURE 3.3-5: SPS-65 Shipboard Radar

TABLE 3.3-1A: TYPICAL PARAMETERS OF GROUND AND SHIPBASED RADARS

SYSTEM	SEEK IGL00	TRACS	ARSR - 3	AOS-4	SPS-58	TPS-43E	TPS-63	TPS-65
<u>MULTI PARAMETERS</u>								
CANCELLER CONFIGURATION								
NO OF BEAMS	4 pulse var coef. 6	4 pulse var coef. 1	3 pulse 1	4 pulse var coef. 1	4 pole Elliptic 1	3 pulse 6	4 pulse var coef. 2	4 pulse var coef. 2
PULSE REPETITION FREQUENCY	300 ± 25% 160 nmi	640 ± 25% 60	330 ± 10% 200 nmi	279 ± 27% 200 nmi	3472/2004 307 2 μs/ (25 nmi)	250 ± 10% 240 nmi	774 ± 27% 80 nmi	773 ± 20% 80 nmi
PROCESSED RANGE								
DATA RATE	2x10 ⁶ I&Q 0.556 MS (45 nmi)	1.3x10 ⁶ I&Q 41.2 (0.508 ms)	1.3 MHz I&Q 23 nmi (0.28 ms)	2.25 MHz I&Q 28 nmi (0.346 ms)	200 KHz I&Q 0	2 MHz I Only 54.5 μs	1 MHz I&Q 2.8 nmi (0.346 ms)	1 MHz I&Q 7.3 nmi (0.090 ms)
MINIMUM DEAD TIME	2.34 ms (190 nmi)	98.2 (1.212 ms)	70 nmi (0.864 ms)	169 nmi (2.087 ms)	192 μs	116 3 μs	52.9 nmi (0.653 ms)	45.7 nmi (0.564 ms)
MAXIMUM DEAD TIME	3951	963	3210	5555	64	5888	988	988
NO. OF RANGE CELLS/BEAH	128 x 11,853Wx2 108x11,853Wx10	108x963x6	98x3210Wx4	108x555Wx6	128x64Wx8	108x5888Wx12	118x988Wx12	118x988Wx12
MEMORY SIZE	60 dB 14	60 dB (10B) 13	54 dB (9B) 13	60 dB (10 Bns) 13	60 dB (10 Bits) >160	60 dB (10 Bns) 8	66 dB (11B) 30	66 dB (11B) 30
DYNAMIC RANGE								
HITS PER BEAMWIDTH								
RAIN CANCELLER								
<u>PULSE COMPRESSION</u>								
CODING METHOD	Taylor	None	None	Barker	None	13 Bit Barker		Taylor 13/26
COMPRESSION RATIO	13:1			13:1		13:1		13-1/26:1
INPUT PULSE LENGTH	6.5 μs			6 μs		6.5 μs		13 μs/26 μs
OUTPUT PULSE LENGTH	0.5 μs			0.4675 s		0.5 μs		1 μs

TABLE 3.3-1B: TYPICAL PARAMETERS OF GROUND AND SHIPBASED RADARS

SYSTEM	SEEK IGL00	TRACS	ARSR-3	ADS-4	SPS-58	TPS-4CE	TPS 63	TPS-65
TARGET EXTRACTION-AZIMUTH								
HITS PER BEAMWIDTH	14	13	13	13	110	8	30	30
NO. OF RANGE CELLS	3951	963	3210	555	64	5888	988	988
NO. OF BEAMS	6	1	1	1	1	6	2	1
EXTRACTION TIME	0.0267x2	0.0125x2	0.0242x2	0.0287x2	0.104x2 Sec	0.032x2	0.0207x2	0.0207x2
Δ AZ RESOLUTION	5 Bits	5 Bits	5 Bits	5 Bits	5 Bits	5 Bits	5 Bits	5 Bits
MEMORY SIZE	14x11,853x5	13x963x5	13x3210x5	13x555x5	110x64x5	8x5888x5	30x988x5	30x988x5
VECTOR ADDITION	-	Log power comb	Log power comb	-	7/8 I + 1/2 Q or 7/8 Q + 1/2 I	1 + 1/2 Q or 1/2 I + Q (TPS-4CEM)	-	(I ² + Q ²) ^{1/2} From Look-up Table
POST DETECTION INTEGRATION								
RESOLUTION	6 Bits	6 Bits	6 Bits	6	11 Bits	6 Bits	7 Bits	6 Bits
FEEDBACK FACTOR	7/8	7/8	7/8	7/8	32 pulse batch	7/8	15/16	15/16
MEMORY SIZE PER INTEGRATOR	68x11,853	68x963W	68x 3210W	68x555W	118x64W	68x5888W	78x988W	68x988W
NUMBER OF INTEGRATIONS	6	1	1	1	1	12	2	2
EFFECTIVE INTEGRATION TIME	0.0267 sec	0.0125 sec	0.0242 sec	0.0287 sec	0.104 sec	0.032 sec	0.0207 sec	0.0207 sec

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programmable two-dimensional processing arrays, such programmable arrays needed for groundbased surveillance radars (versus those for space or airborne radars) are generally smaller, more feasible and likely to be developed more rapidly.

TABLE 3.3-2: TYPICAL ANALOG MEMOP' REQUIREMENTS BASED ON FUNCTIONAL PARTITIONING (HOMOMORPHIC TO THE DIGITAL SIGNAL PROCESSORS).

FUNCTION	RADAR APPLICATION	CCD ARCHITECTURE			INPUT SAMPLE RATE (MHZ)	DYNAMIC RANGE (dB)	LINEARITY (%)	STABILITY (%)
		TYPE	MULTIPLICITY					
			SERIAL	PARALLEL				
MTI	IGLOO	SI/SO	600	2	0.813	60	0.5	-
	TRACS-ASR	SI/SO	494	3	1.29	60	0.5	-
	SPS-65	SI/SO	64	4	0.208	72	0.1	0.1
DOPPLER BANK	IGLOO	SI/SO	600	7X2	0.813	50	0.5	-
	FROST	SI/SO	190	7X2	0.253	50	0.5	-
PULSE	IGLOO	SI/SC	32	32 TAPS; 1	0.813	40	1	-
COMPRESSION	FROST	SI/SO	32	per delayed sample	0.253	40	1	-
INTEGRATION	IGLOO TRACS-ASR SPS-65	Accumulator	600	1	0.813	40+12	1	-
		(e.g. SI/SO)	494	1	0.29	40+12	1	-
		SI/SO	64	1	0.208	40+12	1	-
CFAR, RANGE AVERAGING	IGLOO	SI/SO	32	32 TAPS; 1 per delayed sample	0.813	40	1	-

3.4 RELATED APPLICATIONS

3.4.1 Scan Converter-Interpolator

The data from the azimuth correlator represents lines of data in a skewed coordinate system as determined by the squint angle of the radar beam. In modern aircraft systems it is desirable to display data in a TV format. This function is in the scan converter, which is shown in Figure 3.4-1.

The radar range data appears in Figure 3.4-2 in regular time samples whose data points march out on the "map" in regular rows at the squint angle. In order to display this map accurately on a rectangular TV raster, the new data points must be generated with a timing along each TV horizontal sweep such that they occur at the intersection of that sweep line with the projected radar range line being displayed and they must each have a single amplitude value which is "interpolated" between the values of the range cells before and after the range line intersection with that sweep.

Interpolation may be done with a transversal filter structured APUP. It is apparent from Figure 3.4-2 that changing the squint angle, ψ , will change the time relationship between the original set of data points and the interpolated points. To perform the interpolation for any given point, however, it is only necessary to know the offset between the desired (interpolated) point and the points in the skewed coordinate system. The accuracy of the interpolation depends upon how well the offset between the data and the desired points is known and how many different offset functions are provided. Around 10 should be adequate for scan converters.

Another accuracy consideration is the interpolation function itself and the number of points used in the interpolation. The optimum function depends upon the shape of the bandpass preceding the interpolation.

Figure 3.4-3 shows, however, that the optimum function is not greatly different (for a 10-point interpolation), whether the spectrum has a sharp transition (uniform) or a gradual

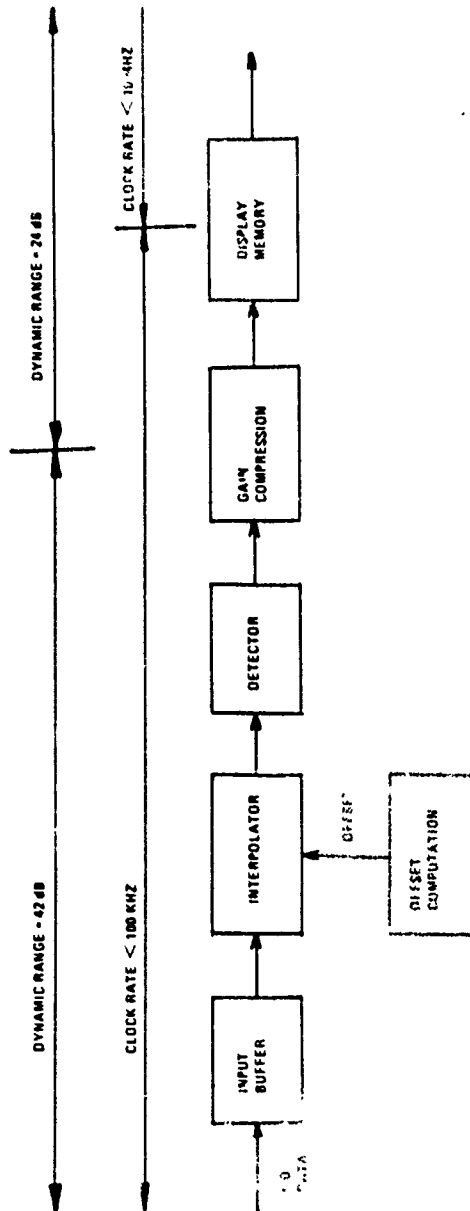


FIGURE 3.4-1: Squint SAR Scan Converter

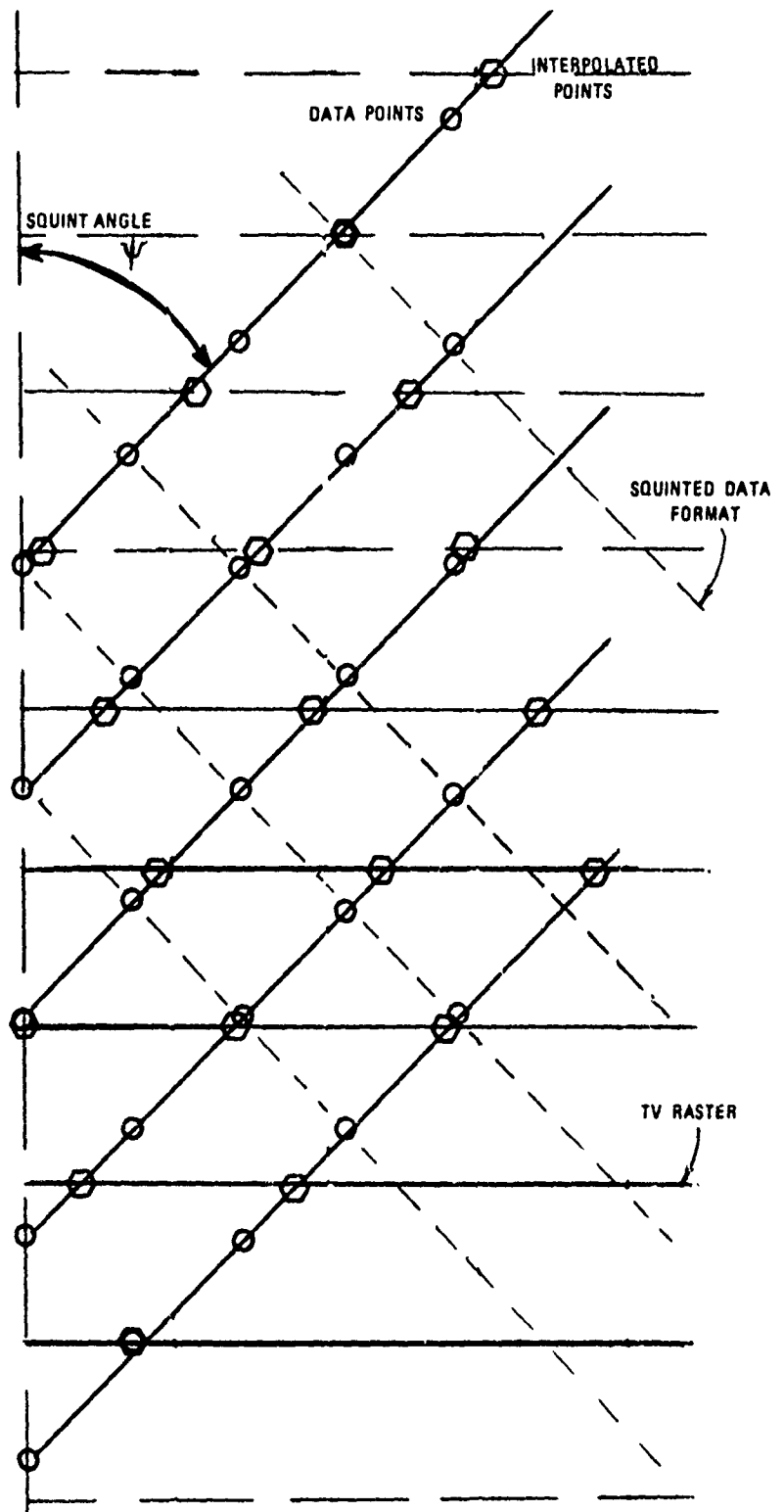


FIGURE 3.4-2: Squint SAR Interpolation Problem

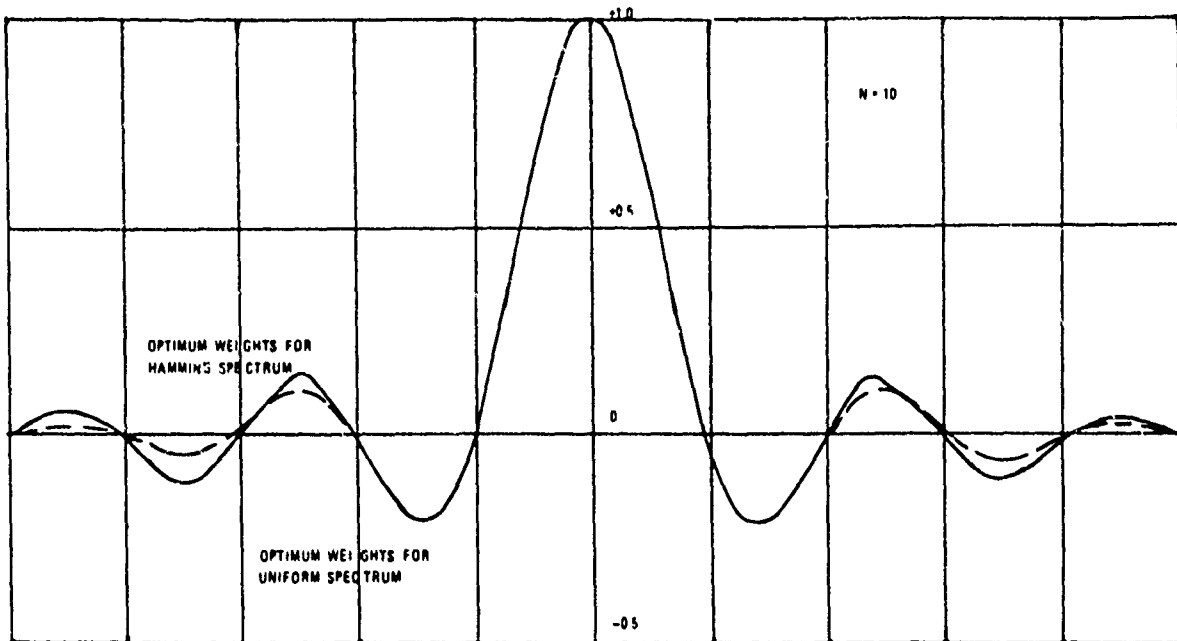


FIGURE 3.4-3: Optimum Weights for a 10-point Interpolation

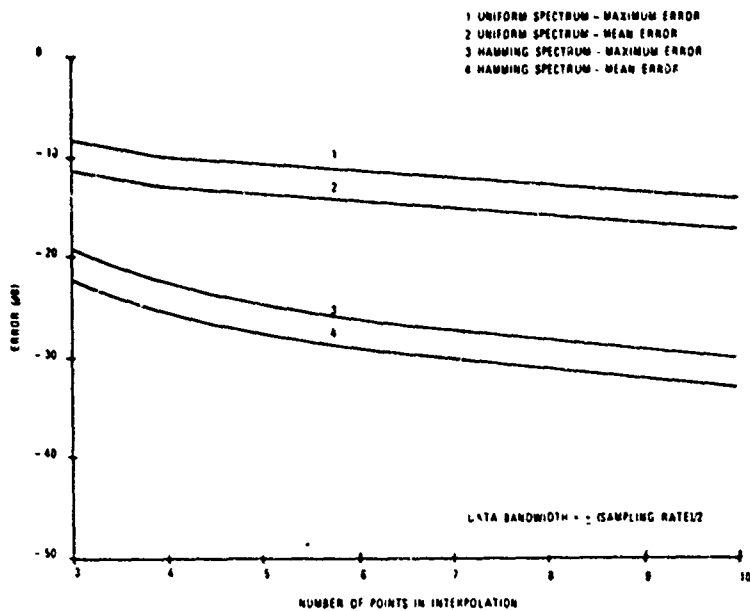


FIGURE 3.4-4: Interpolation Error for Nyquist Sampling

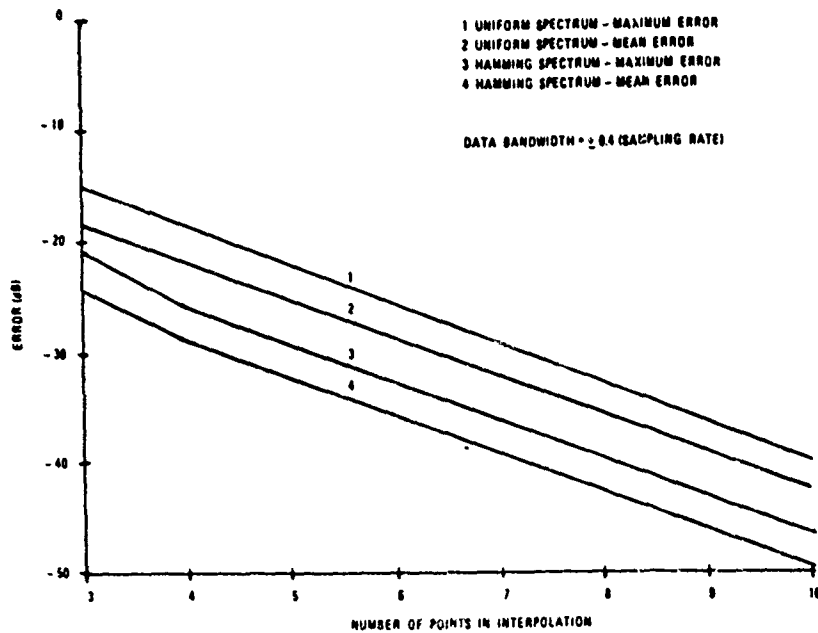


FIGURE 3.4-5: Interpolation Error for 25% Oversampling

one (Hamming). Error is reduced by using more points in the interpolation as shown in Figures 3.4-4 and 3.4-5, but the accuracy is greatly enhanced by a small amount of oversampling as shown in Figure 3.4-5.

3.4.2 APUP Applied To ECM

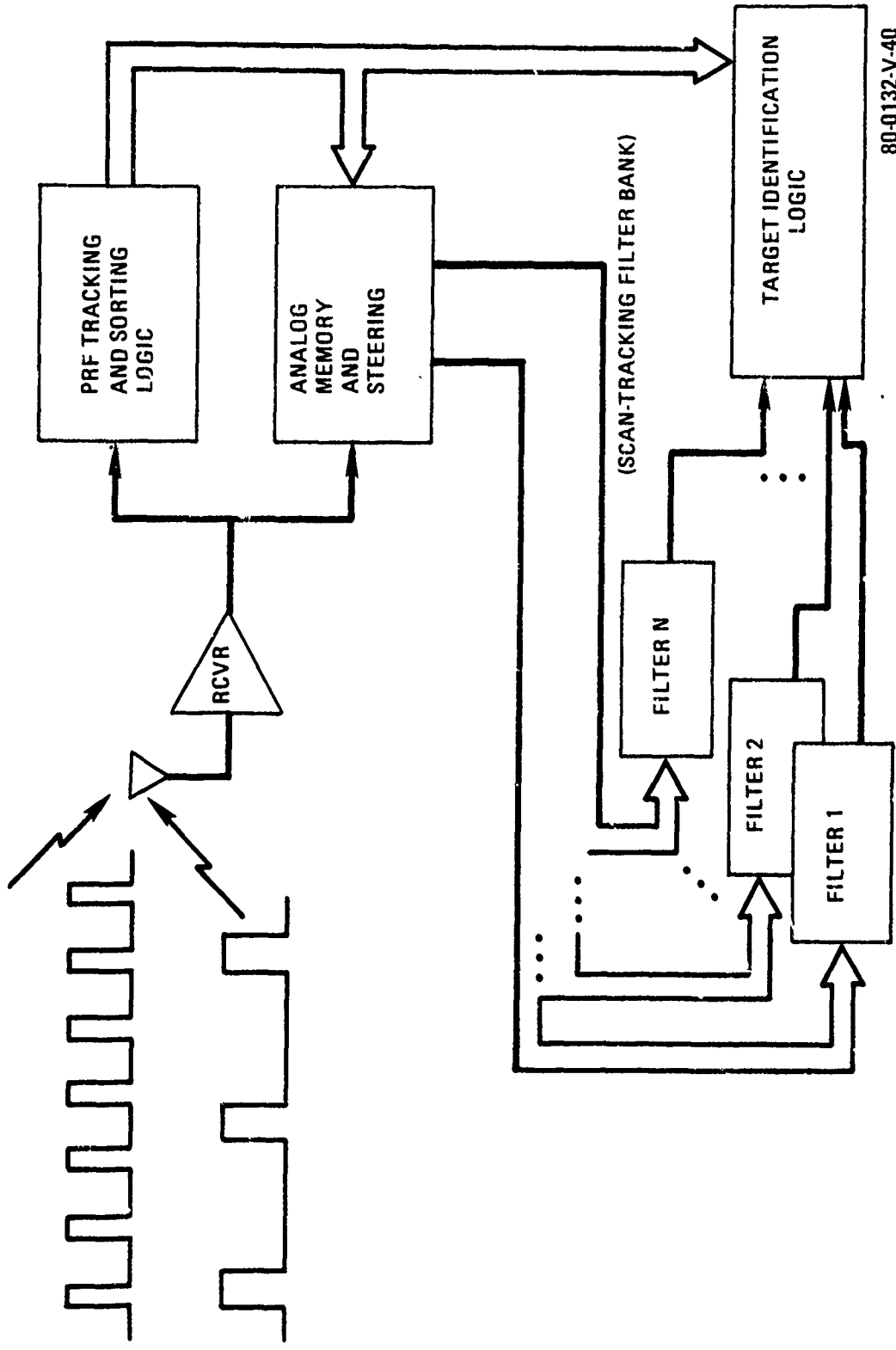
3.4.2.1 Introduction

This is intended to be a brief analysis of the application of APUP devices to electronic warfare (EW) systems. The application of APUP devices to the extraction of narrow band signals in the presence of wideband noise is well documented in the literature, but a related application is not. That is the extraction of multiple narrowband signals, interleaved on a sampling basis, in the presence of wideband interference, which itself may consist of a multitude of sampled signals.

APUP devices could have a significant role to play in EW systems. This includes 1) signal extraction based on antenna-scan-induced amplitude modulation, 2) application of such modulations in a real-time inverse gain modulation program, 3) application as an important aid to but not necessarily a central role in PRF tracking with or without an active antenna scan, and 4) tapped delay line applications.

3.4.2.2 Description of the Application

The trend in active electronic counter measures (ECM) systems has been for "intelligent" power managed systems capable of operating in a dense multi-signal interleaved pulse train environment. For this report, the PRF of each radar threat will be considered to be equivalent to its sampling rate. Most of the tracking threats have pulse duty cycles on the order of 0.1% with pulse widths of a fraction of a microsecond. The other large class of threats is SEARCH, with similar duty cycles but with pulse widths on the order of several microseconds, generally. Most of these radar transmitters have outputs that cannot be deliberately amplitude modulated (as opposed to just gating the pulse), an important point for this CCD APUP study. The signal received by the ECM system will,



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FIGURE 3.4.2-1: ECM Signal Analyzer

however, experience amplitude modulation from the active antenna scan as well as from ground bounce, atmospheric transmission effects, range variations, and the heading (pitch, roll and yaw) of the aircraft.

Because of the dense signal environment and the resulting need for power management, an important function of ECM front-ends is to separate the signals on a carrier frequency and time multiplexed basis. Another function is to apply inverse gain modulation to the threat radar. In such a role the APUP can "pass through" the detected active antenna scan from reception to active transmission modulation, provided the modulations can be individually extracted and intelligently steered by the ECM central processor. This usually means that the amplitude word is presented to the proper microwave carrier frequency channel under a time-of-arrival (TOA) gate or a general "range gate", if false ranges are to be transmitted. This real-time steering manipulation can and is being handled with existing technology. However, that usually amounts to "calling up" a particular class of waveform (sine wave, triangle wave, sawtooth, etc.), often with various levels of AM and FM superimposed on one another, from a central waveform generator subsystem. These modulation rates are relatively slow with respect to the time scales of these "windows". However, the inverse gain modulation, with all of its odd shapes (the simplest ideal antenna pattern has a $\sin x/x$ shape) and various amplitude perturbations, presents at minimum an order of magnitude increase in the amount of data involved compared to selecting a set of parameters from the waveform generator. A CCD APUP could be ideal for such a role.

Almost all of the tracking threats have dispensed with an active antenna scan, probably in response to ECM since they have to pay a price in performance to do that. Therefore, this role will find its main application in response to SEARCH and older type tracking threats.

The role as an aid to PRF tracking, however, is an important

function needed against the latest tracking threats. Although there will be no nominal antenna scan, there will be a nominal range dependent, and hence time dependent, amplitude. Further, this will have variations on it due to the radar characteristics (power supply ripple, etc) as well as the aircraft motion moving the antenna and ground bounce effects. Some of these phenomena are repetitious or semi-repetitious. This information can be quite useful. The simplest case is when the amplitude variation range of each pulse train does not overlap that of others. Even in this case, the data handling requirements are significant. If they overlap, it appears that CCD filtering capabilities would be ideal to extract the nominals and the correlation factor for each pulse.

In summarizing the application, remember the basic philosophy advocated here: it is the intent to apply APUP-type hardware in ECM roles where the function is based on restraints from either 1) the laws of physics or 2) reasonable technology imposed on the radar designer. For example, using APUP firmware rather than software for the latest application of PRI modulation tracking leaves us vulnerable to arbitrary choices of the radar designer. That is, the amount of effort to build the specialized APUP structure is unwarranted because of the volatility of both the threat parameters and their nature. Threat characteristics that are not arbitrary as received by the jammer can be very effectively funneled through APUP processes. This will make the development of these APUP structures quite cost effective, filling the important requirements described above.

This application philosophy does not mean that the APUP structure should not interface with software. It seems quite advantageous for some of the variants to the above applications to have their parameters (e.g., feedback gain) loaded in real time based on either 1) the environment characteristics or 2) the output of the APUP itself.

The above application descriptions assume an on-board

active power-managed system. The impact on RPV's (remotely piloted vehicles) could be much larger as a percentage of the overall system. At present there is considerable opinion in the EW community that RPV's will be the new growth area for ECM, since it offers a solution to some fundamental ECCM (electronic counter countermeasures) expected and presently employed by radar designers. The RPV ECM electronics will largely have the assignment of making delayed transmissions, albeit with appropriately modulated or selected delays and amplitudes. There are two basic system philosophy approaches: 1) the pulses can be held in microwave delay lines or 2) the pulse data can be digitized and passed through shift registers. In the first case it is considered difficult to reliably preserve the amplitude accurately so APUP-type hardware can be employed nicely as a transmission medium for the pulse amplitude for either approach. Passing the carrier frequency data through a CCD delay line, however, could place an unrealistic accuracy spec on these lines, so other technologies may be more appropriate.

Several key points of similarity and difference with radar applications should be indicated. The dynamic range is approximately 30 to 40 db, probably less than most radar applications. All waveforms processed by APUP structures for radar applications are characterized by the availability of basic sync. However, this "hard and fast rule" is completely reversed for ECM applications which may lead to unique ECM APUP structures. The ECM input is characterized as a multi-signal environment, multiplexed on several levels, i.e., the carrier signals are varied and the pulse trains are interleaved.

In summary, the ECM applications of APUP-type structures are 1) inverse gain pass-through and phase-shifted modulation, 2) real-time identification (ID) based on scan data, 3) real-time ID based on second-order Lobe-on-Receive-Only (LORO) modulations and levels, 4) an aid to PRF tracking, and 5) a tapped delay line for RPV transmissions. Table 3.4-3 outlines

TABLE 3.4-1

ECM REQUIREMENTS

(These are guides only, since classified values were not used)

- 1.) Tapped Delay Line:
 - Dynamic Range 40db
 - Delay 1 to 5 msec
 - Time Resolution 0.1 usec
 - # of taps 25 to 50
- 2.) Inverse Gain Element I
 - Dynamic Range 40db
 - Cycle Range 10 to 200 Hz
 - Time Resolution 1%
- 3.) Inverse Gain Element II
 - Dynamic Range 40db
 - Cycle Range 1 to 0.1 Hz
 - Time Resolution 0.1%
- 4.) Scan ID
 - Dynamic Range 25db
 - # of interleaved sample trains 5
 - Sampling Rate 1 to 5 KHz and 100 to 500 Hz
 - Modulation Rate 10 to 200 Hz and 1 to 0.1 Hz
- 5.) LORO ID
 - Dynamic Range 25db
 - # of interleaved sample trains 20
 - Short term modulation range 1 to 3 db
 - Moderate term amp variation 15 db
 - Sampling Rate 1 to 5 KHz
 - Modulation Rate 400 to 0.1 Hz
 - Variation Rate 5 minutes

the characteristics required of an APUP for these applications.

3.4.3 Acousto-Optical (A-O) Signal Processing

3.4.3.1 System Concept

Acousto-optics (A-O) is a high speed processing technology that can perform linear environment analysis instantaneously and retain temporarily-related signal characteristics for subsequent processing. A system concept, based upon A-O technology, is shown in Figure 3.4.3-1 and was evolved to exploit the high speed linear characteristics of A-O technology.

The A-O signal processing system concept consists of a multi-channel wideband optical processor located near the system front end which accepts signals from the environment, analyzes and digitizes them, providing a pulse-to-pulse intercept report to the system's digital processor.

Signals from the environment are intercepted by the antenna, demultiplexed, and converted to the A-O processor intermediate frequency (IF). A-O signal analysis results from optical energy diffracted onto a focal plane sensor which transforms the light energy into electronic signals. Intercepted data is quickly transferred to temporary storage, maintaining time-of-arrival (TOA) intercept resolution while the sensor array is released to further analyze the intercepted environment and thus maintain a high probability of intercept. Data on the temporary storage array is detected, centroided, digitized, and transferred to the digital processor for subsequent analysis. This APUP-type monolithic element providing both the detection and preprocessing functions is being addressed here. TOA and scan data analysis is performed elsewhere in the system digital processor along with library correlation.

The initial processing objective is a single-dimensional optical processor providing a spectral analysis of the input signal. For this, a linear imager-preprocessor is required compatible with integrated optics differential amplitude direction-of-arrival (DOA) measurement implementation techniques. These

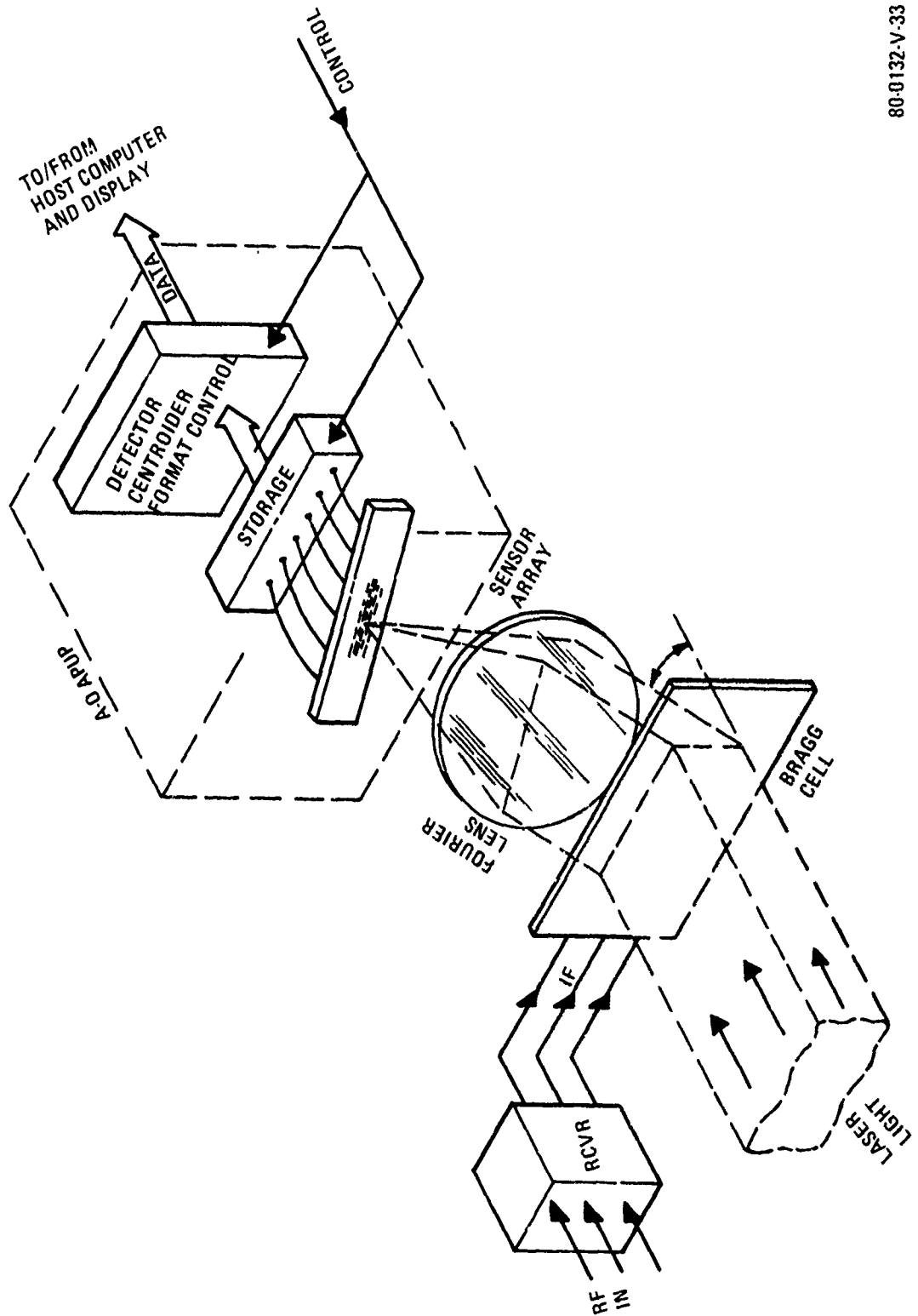


FIGURE 3.4.3-1: Acousto-Optical Signal Processing System Concept

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emitters may be further categorized into narrow pulse and high duty-cycle emitters. The narrow pulsed emitters exhibit nominal 0.1 usec to 1.0 usec pulse width and 10 msec to 10 usec pulse repetition intervals. Frequency variations up to 10% of operating frequency can also be expected for chirped and hopped signals although other emitter types normally exhibit frequency stability within $\pm 0.1\%$ of center frequency.

The signal environment presented to the optical processor is indeed a varied one. Signals range from CW-type illuminations encountered in noise jamming, spread spectrum, CW illumination, and pulse doppler to variations of the more conventional narrow pulse radar. The optical processor and its imager preprocessor must be capable of detecting and measuring the relevant signal parameters to the resolution required for subsequent classification.

3.4.3.2 Functional Requirements

The environmental aspects of the electronic warfare problems indicated above outline parameters of interest for emitter classification. A list of relevant processor emitter parameters is given in Table 3.4.3-1. Optical processors employing Bragg cell diffraction provide frequency measurement as the position of an illuminated element in the linear optical detector array. Intercepted signal bandwidth is correspondingly determined by the number of detector elements illuminated. Since the diffracted optical energy is proportional to signal level and the detector charge is proportional to incident optical energy, relative signal amplitude is determined by a measure of the charge stored in an energized photo-optical detector. Signal time-of-arrival measurements result from near real-time imager access, providing subsequent system processing elements with pulse by pulse data for signal temporal characteristic analysis. Together signal frequency, pulse time-of-arrival data, and signal amplitude can be used to classify environment signals by establishing the intercepted signal operating frequency, pulse train modulation characteristics, and scan

TABLE 3.4.3-1

Emitter Parameters	Usable Performance		Design Goals	
	Range	Resolution	Range	Resolution
Frequency	.5 GHz to 18 GHz	10 MHz	.5 GHz to 40 GHz	1 MHz
Bandwidth	CW to .5 GHz		CW to 1 GHz	
Pulse Rep. Int.	10 usec to >100 msec	5 usec	10 usec to >100 Msec	25 usec
Signal Amplitude	-40 dBm to +10 dBm	1 dB	-60 dBm to +10 dBm	25 dB

characteristics.

The environment characteristics in conjunction with the functional processing requirements indicate the scope of the processing problem to be effected by the optical processor and interfaced by the imager circuit. Certain boundary conditions can be established which form the basis for imager processor development. Considering the environment density and the mix of emitters contained therein, capability for intercepting and reporting ten intercepts in any aperture period (through-put time uncertainty - 0.5 microsecond or 0.25 microsecond design goal) is adequate. Further advantages result as sufficient processing flexibility is incorporated into the detector pre-processor to accommodate the differing environment analyses required by both high duty-cycle and narrow pulse signals. For example, algorithms required to eliminate spectral sidelobe responses from a pulsed signal environment are not appropriate for a corresponding CW environment.

3.4.3.3 Linear Imager Requirements

The linear imager requirements based upon the tactical electromagnetic environment expected, the signal parameters required for accurate electronic warfare threat assessment, and the capabilities of the optical processors to which these linear imagers will be applied are presented in Table 3.4.3-2. Here functionally related sensor, intercept processing, control, and implemented data transfer imager requirements are outlined for both usable performance and design goals. Each of these areas is discussed below in some detail.

Sensor Functions

The sensor functional requirements reflect the circuit requirements of the optical transducer array at the photo detector element. The number of elements establish the processor spectral resolution while the small pitch eases optical component requirements. Dynamic range is of primary interest and is defined as the signal range above threshold over which an input signal amplitude can be accurately

Table 3.4.3-2

LINEAR IMAGER REQUIREMENTS

FUNCTION	PARAMETER	USEABLE PERFORMANCE	DESIGN GOAL
Sensor	No. of Elements	100	1000
	Element Spacing, Center to Center	10 um	5 um
	Detector Equivalent Noise	200 Electrons	50 Electrons
	Anti-Blooming Im. Adjacent Element Crosstalk	20 dB*	30 dB*
	Dynamic Range	-50 dB**	-70 dB**
	Optical Wave-Length	50 dB	70 dB
	Quantum Efficiency	0.65 to 0.91 um	0.65 to 0.91 um
	Response Uniformity	50% min.	50% min.
	Storage Time	+ 12% ABS	+2.5% ABS
	Threshold FAR	10 msec	10 msec
		10 ⁻¹²	10 ⁻¹²
Intercept	Spectral Sidelobe Rejection Multiplexing	1 Rpt/Intercept 100:1	1 Rpt/Intercept 1000:1
Processing	A/D Conversion Resolvable Steps Processing Rate Throughput Time Uncertainty	64 10 Emitters/usec 0.50 usec	256 10 Emitters/usec 0.25 usec
Control	Serial Input Control Frequency Address On/Off Control Sidelobe Rejection Algorithm Control data Rate Imager Clock Input	7 bits 1 bit 1 bit >1 Mbit/sec Variable 1% to 100%	10 bits 1 bit 1 bit >1 Mbit/sec Variable 1% to 100%
Data Transfer	Data Format Frequency Data Amplitude Data	Parallel Digital 7 bits 6 bits	Parallel Digital 10 bits 8 bits

* For 1% Clock Rate

** For elements beyond closest neighbor to illuminated element

quantized. The threshold is established by the maximum circuit false alarm rate (FAR) indicated in Table 3.4.3-2 and is related to the imager circuit noise statistics. If noise variations are gaussian and white over the frequency range of interest, a threshold of 14 dB above the RMS noise level is required to provide the circuit FAR indicated. Since signals have already been optically channelized before they reach the detector, the optical-to-electronic transduction need not be linear. A logarithmic relationship would compress the signal amplitude range for convenient subsequent intercept processing.

Intercept Processing

Intercept processing is required as on-chip monolithic signal analysis to reduce the high speed raw data interface rate and make centroided intercept data available to the system digital processor. Photo-detector analog storage is provided, freeing the sensor elements to image additional optical processor readout while previously intercepted signals are being interfaced out of the circuit. The first data reduction processing step is thresholding to eliminate non-illuminated channels from further processing consideration. The circuit is required to threshold detected signals as near to the noise floor as is compatible with the indicated circuit FAR. To further cull extraneous data the circuit will compare levels of adjacent elements and inhibit those contiguous cells of lesser amplitude from being processed further. Multiplexing is performed to rapidly index through the imager element outputs accessing the thresholded, ambiguity-resolved data into a digitized output. The amplitude of each multiplexed valid intercept is then analog-to-digital converted and provided as part of the digital report along with the digital frequency representation. Monolithic processing capability is required to extract the parameters of ten simultaneous emissions on the focal plane in a submicrosecond period and preserve their essential temporal characteristics.

Linear Imager Data Transfer

The measured intercepted signal parameters are provided off circuit to the system digital processor for temporal analysis and classification. Output data is transferred in parallel digital format compatible with the high report rates expected in dense environments and with the digital processor with which it interfaces. Frequency and signal level data are provided at transfer rates of 10^7 reports per second.

Linear Imager Control

The electronic warfare electromagnetic environment is complex and requires a high degree of flexibility adapting processor performance to signals of interest. The control functions provide this flexibility. Since the control message rate is expected to be low, system interactive commands are supplied to the imager preprocessor through a serial data line. The control word consists of a frequency address, a related on/off control bit, and a total circuit-related spectral sidelobe rejection control bit. The frequency word accesses a storage element where the associated control bit is stored, either enabling or disabling responses from that cell. This characteristic is advantageous when a large population of friendly high duty-cycle emitters exist in the environment overloading the imager preprocessor, digital processor or both. Frequency element on/off control can be used to remove these emitters from further processing on a system interactive basis.

While pulsed signals require spectral sidelobe rejection, this processing can be counter-productive in an environment containing closely-spaced high duty-cycle stable RF frequency emitters. For this reason a control bit is required to enable or disable the spectral sidelobe rejection processing logic. Optical processor performance can consequently be adapted on a system interactive basis to either high resolution spectral signal analysis in a dense CW emitter environment or enhanced on-chip data reduction for dense narrow pulse environments such as those encountered from conventional radars.

3.4.3.4 Functional Implementation Discussions - Overview

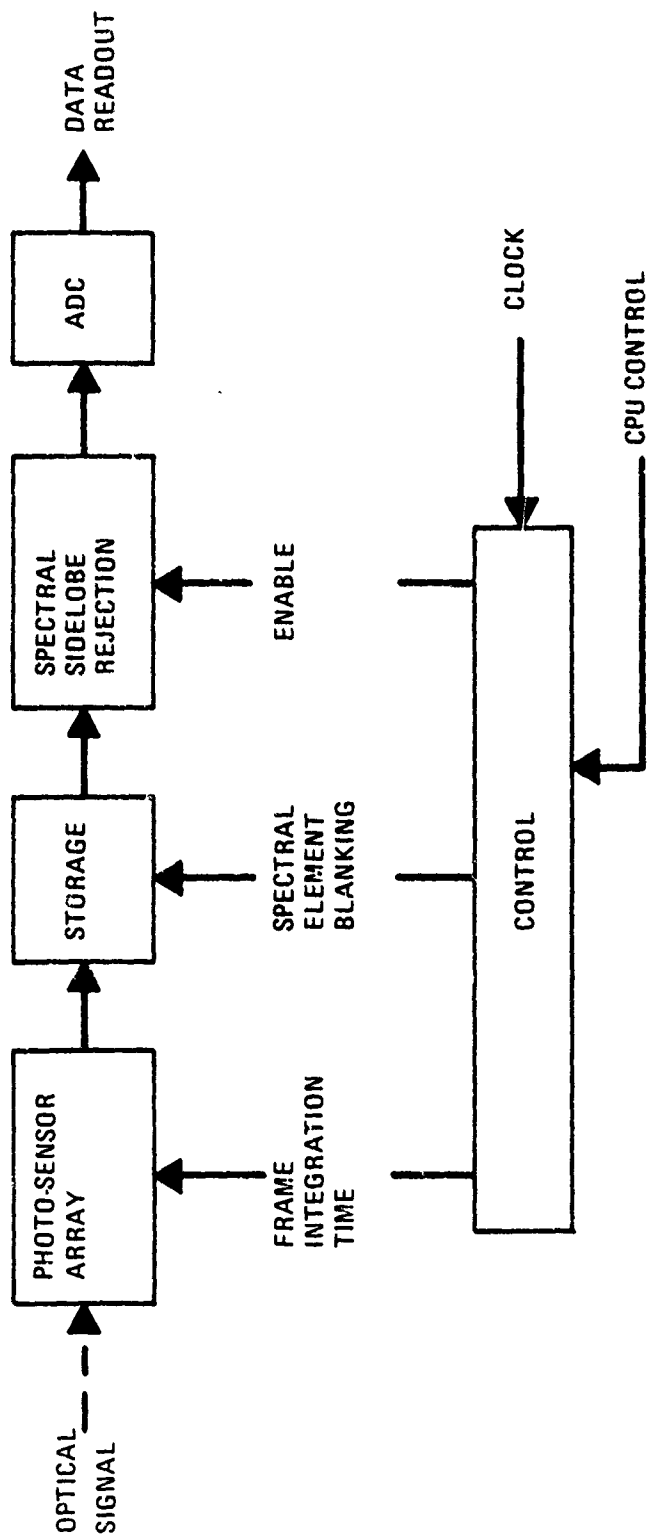
A simplified functional diagram of the imager preprocessor circuit is indicated in Figure 3.4.3-2. It consists of a sensor array performing the optical to electrical transduction and associated storage establishing a near 100% optical sensor activation time and enhancing the optical processor probability of intercept. Stored intercepts are accessed by the processing electronics and ambiguous data discarded. Valid data logarithmically compressed is supplied to the A/D converter, digitized, formatted, and delivered external to the system digital computer. System interactive control is provided through on-chip circuitry that interfaces directly with the system central processing unit (CPU).

Photosensor and Storage

A single photosensor and storage element functional block diagram is shown in Figure 3.4.3-3. The incident optical signal is applied to the photo detector where its energy is transduced into electronic charge. To relieve subsequent processing elements from handling a widely varying amplitude signal range, the detector output is compressed logarithmically to a much smaller amplitude range. The resulting charge is integrated for the duration of the intercept period and transferred to temporary storage by the array storage strobe. The stored charge (voltage level) is provided to the intercept processor for further on-chip processing.

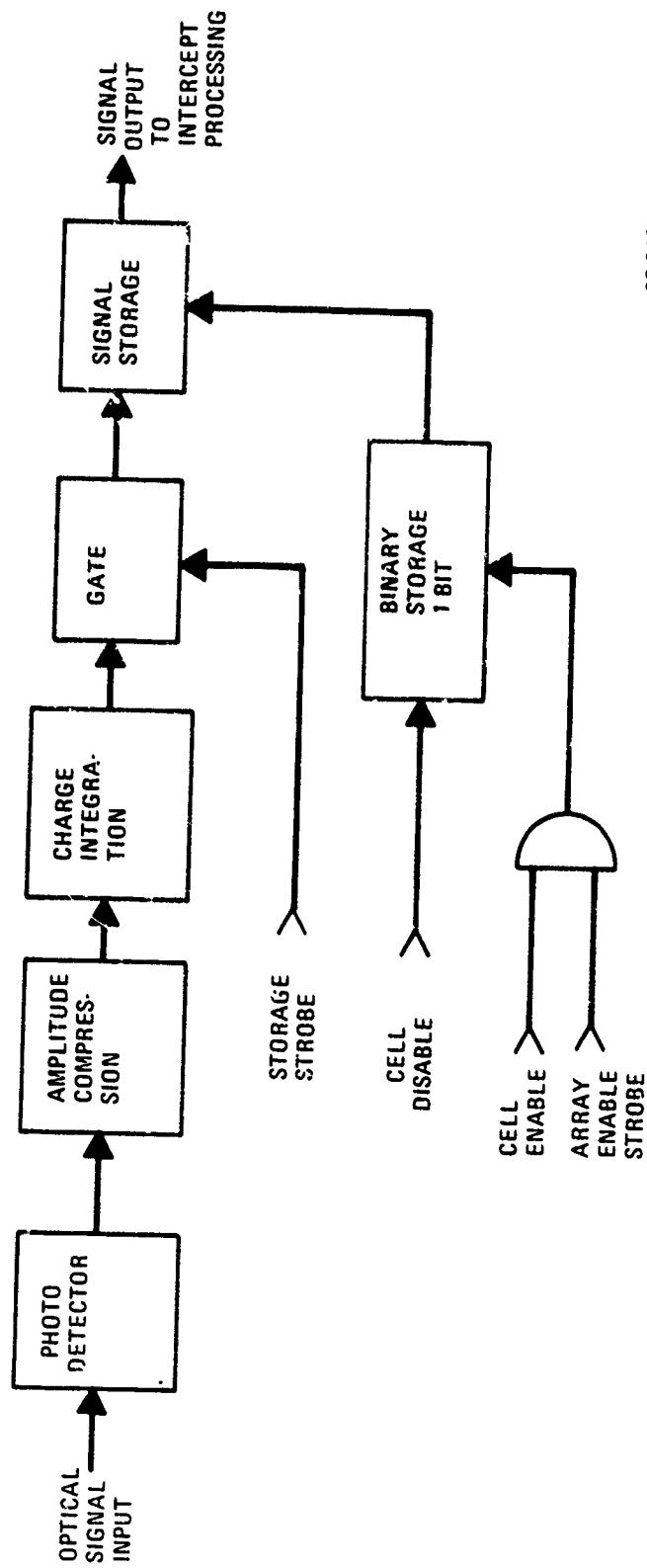
Sensor Element Processing

After the signal is detected and stored, it is processed further to delete extraneous focal plane illuminations and condition the signal for subsequent data readout. At each sensor element the processing functions that operate on the stored signal of the associated sensor element are indicated in Figure 3.4.3-4. The stored signal input drives a level comparator where its amplitude is compared to that of adjacent cells. Further intercept data processing is enabled if the element being evaluated exhibits the largest amplitude of those



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FIGURE 3.4.3-2: Acousto-Optical APUP Array



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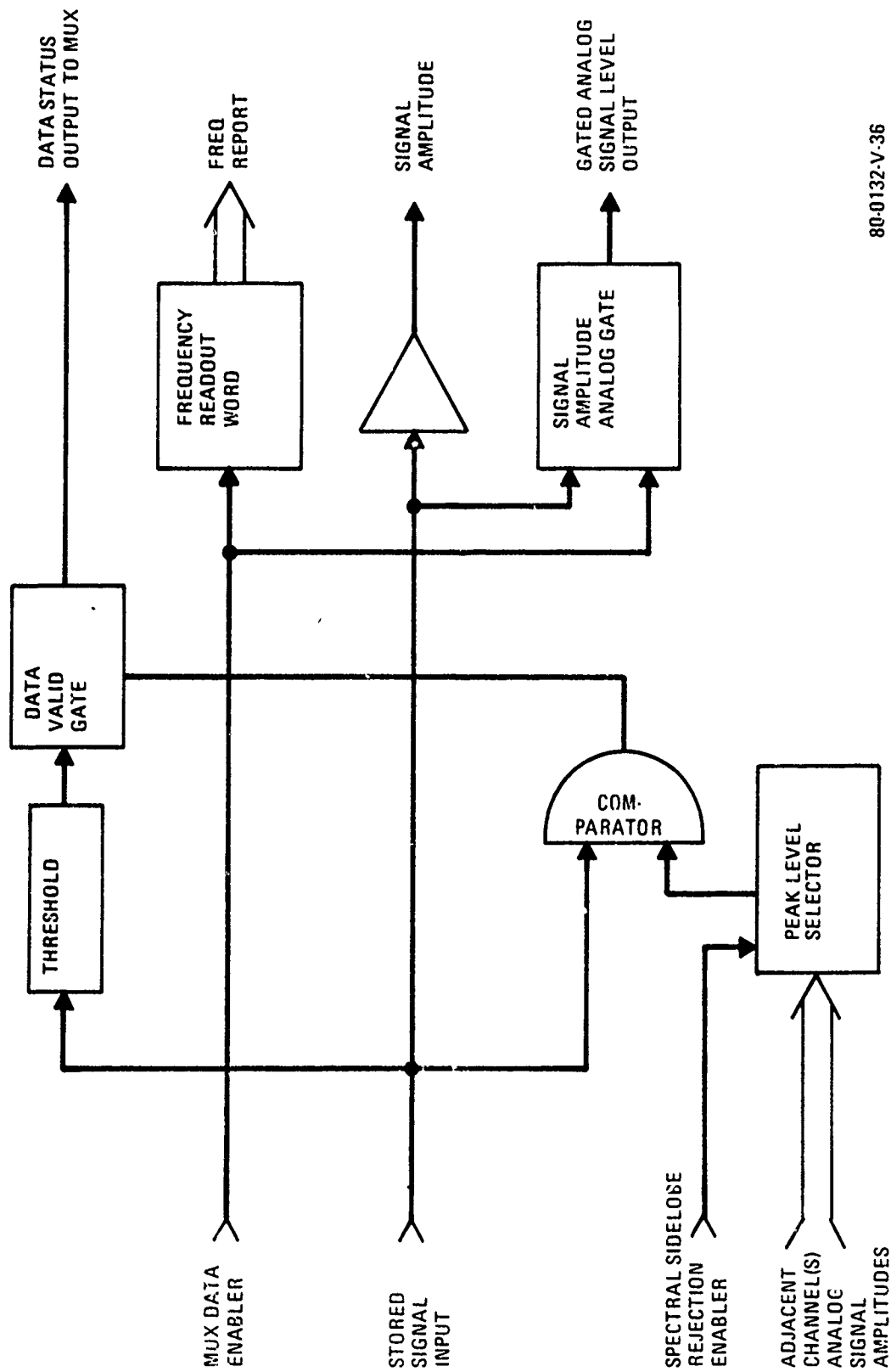
FIGURE 3.4.3-3: Photo-Sensor and Storage

compared. The comparator is driven in the opposite sense by the peak level selector which applies to it the largest amplitude signal in the adjacent channels. This processing inhibits spectral sidelobes from being processed as valid data and reduces the data output volume. The number of adjacent channels providing inputs to the peak level detector depends upon the spectral coverage provided by each element and the narrowest expected pulse widths. For example, a 100-element imager array providing a 500-MHz spectral coverage in an environment where pulse widths as small as 0.1 usec are to be processed requires four adjacent channel inputs to assure reporting only signal center frequency, two from both above and below. Correspondingly, a 1000-element imager array providing a 1-GHz spectral coverage in the same environment would require twenty adjacent channel inputs, 10 above and 10 below. An enabling control function input to the peak level selector is provided to defeat the spectral sidelobe rejection feature when a high-resolution environment analysis is dictated by the presence of high duty-cycle emitter.

The stored signal input is also applied to a thresholding circuit that functions when sufficient signal energy has been received to overcome noise. This circuit also reduced subsequent data processing by requiring sufficient input signal-to-noise ratio to preclude subsequent processing on random noise peaks. The threshold circuit output is gated by the spectral sidelobe rejection comparator. The resulting data status output is provided to the circuit multiplexer indicating the existence of valid data at this element location and enabling access.

3.4.3.5 Conclusions

An APUP-type imager-preprocessor integrated circuit is a key optical processing component. Currently available imaging technology established first order optical processor limitations for speed and dynamic range so important to electronic warfare support measures applications. A comprehensive imager development program is currently being formulated to provide sensitive,



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FIGURE 3.4.3-4: Sensor Element Processing

high speed, high dynamic range imager technology. The approaches to circuit implementation presented here are intended to be illustrative of the functional processing required to achieve the desired performance. These approaches should be considered functional illustrations only. The circuit requirements are derived from electronic warfare system objectives and are established as the development goals.

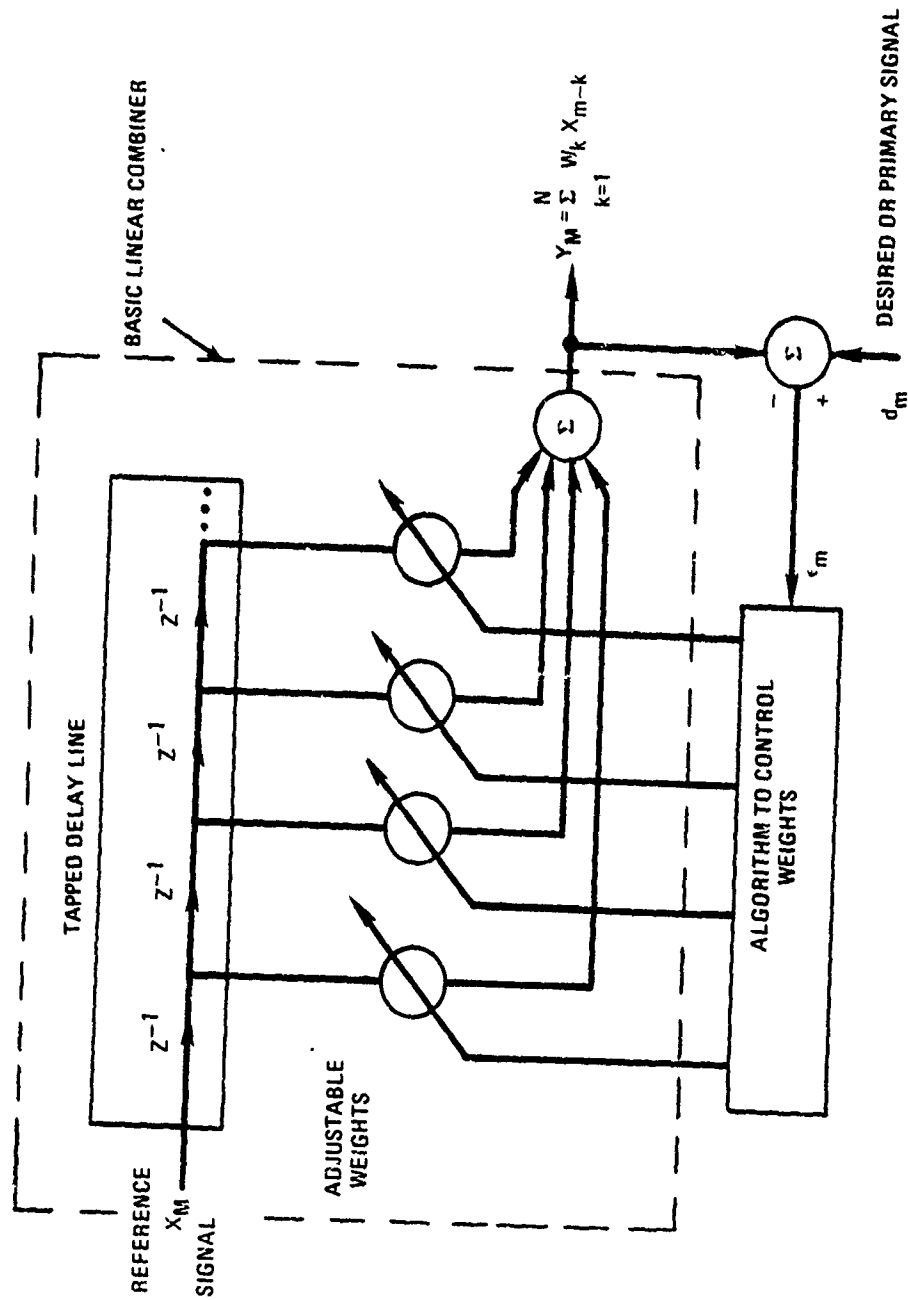
3.4.4 ADAPTIVE SIGNAL PROCESSING

Adaptive filters are a class of "learning machines" in which the filter design (weight or parameter adjustment) is self-teaching and based upon the estimated (measured) statistical characteristics of the input and output signals. The most general implementation of an Adaptive filter is limited by practical considerations since the inversion and storage of large matrices of data require a sizeable volume of computer space, making real-time signal processing difficult to achieve. An iterative least-mean-square algorithm (LMS) requires very little computer storage or time, and this algorithm is suitable for real-time processing of large amounts of data. The statistics of the signal are not measured explicitly to design the filter, but instead, through a recursive algorithm, the weight adjustments are made automatically with the arrival of each new data sample.

A block diagram of the basic adaptive filter used to implement an LMS algorithm is shown in Figure 3.4.4-1 (1) while the chip layout map and a photomicrograph of an actual die on a wafer are shown in Figure 3.4-2.

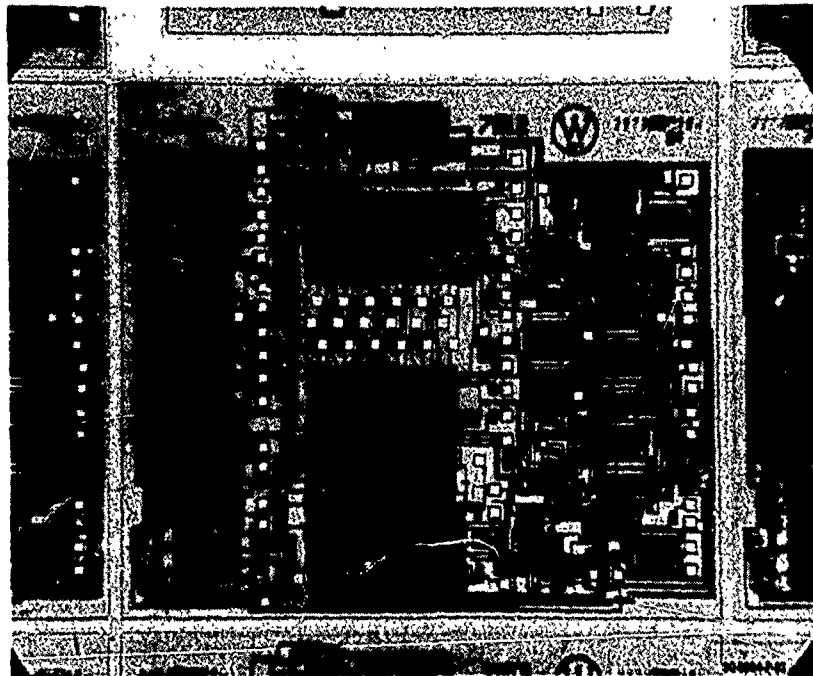
The LMS error algorithm is a practical technique for determining in real-time the optimal weights of the linear combiner which minimize the mean square error. The important features of the algorithm are: 1) no explicit measurement of correlation functions, 2) no large memory storage or matrix inversion, and 3) the accuracy is determined by the statistical sample size. These advantages over the direct computation algorithms permit an adaptive analog signal processor to be realized as a monolithic integrated circuit.

The process of weight optimization can be pictured as the point in time when the error sequence is orthogonal to the data sequence. The result is an implementation of the orthogonality principle in N-dimensions. This optimization may be likened to a correlation cancellation loop (CCL) (2) that removes or cancels from the output signal any component



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FIGURE 3.4.4-1: Block Diagram of a Basic Adaptive Filter



Chip Organization of Monolithic 16-Tap Adaptive Analog CCD Filter

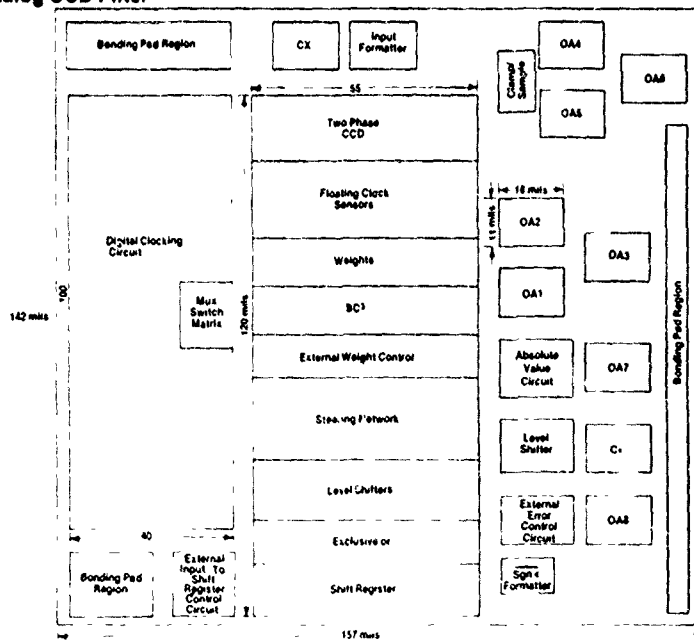


Fig 3.4.4-2: The CCD Adaptive Filter Chip Using Combined CCD/CMOS/Bipolar Technology for Mixed Digital and Analog Signal Processing

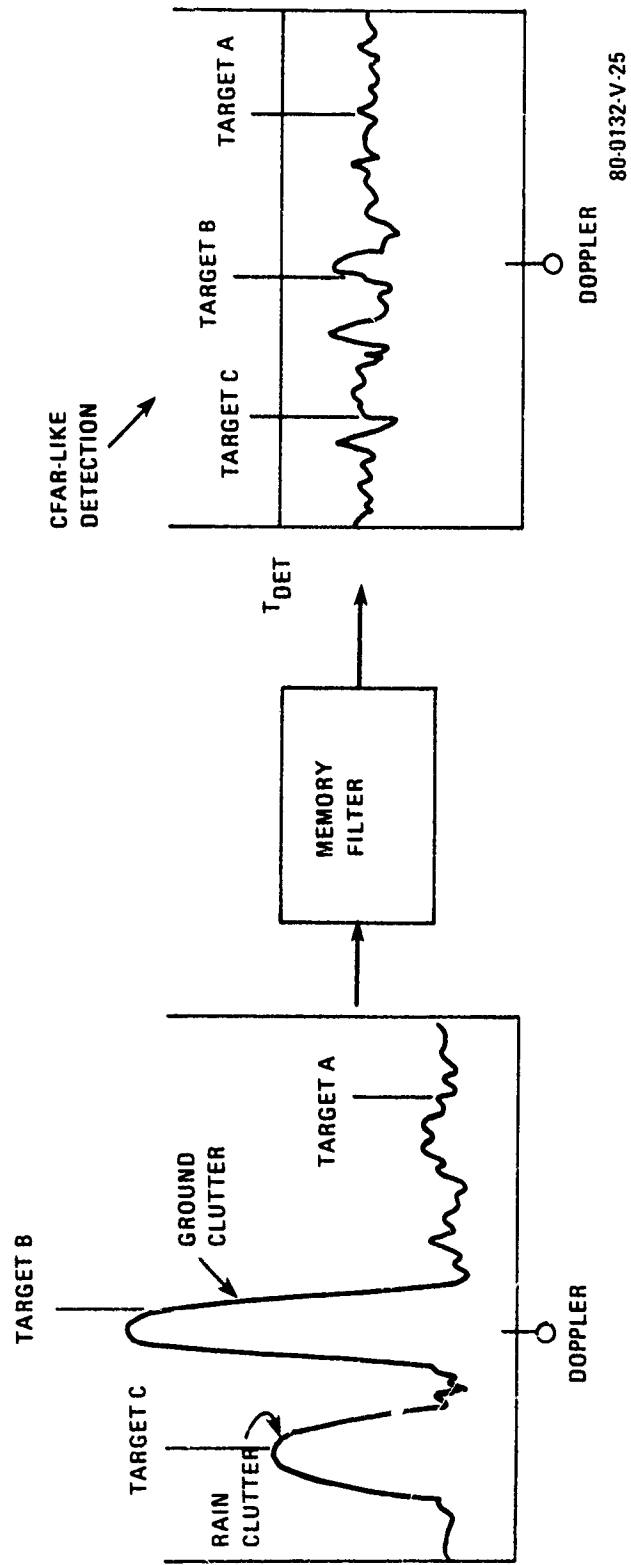
of the primary signal that is correlated with the tapped data signal (reference). The subtraction process continues until no correlation is detected between the output error and the reference input, at which time the mean input to the integrator is zero.

The adaptive filter development of the 1960s was an important commercial outgrowth of research and development at the Bell Telephone Laboratories ⁽³⁾ ⁽⁴⁾ on algorithms for adaptive equalization. There are numerous applications for CCD adaptive signal processors. They include estimation/prediction, filtering, spectral analysis, data compression, interpolation, echo cancellation, speech analysis, noise cancellation, and system modeling.

An important application for this work is for a noise canceller. Noise cancellation finds application in clutter cancellation (e.g., antenna, hydrophone, seismic/acoustic transducer and electro-optical systems) and coherent signal processing when periodic or narrow-band signals must be separated from broadband interference (e.g., spread spectrum systems). The adaptive clutter canceller has been modeled. The results of this simulation are shown in Figure 3.4.4-3.

Clutter rejection filters are commonly used in radar systems to suppress the clutter returns for the purpose of improving the detection and tracking of targets. The conventional clutter cancellers are deterministic filters which are designed for specific clutter environments. To account for the wind-driven rain and foliage clutters, the filter is required to have a wide rejection band to cover all possible clutter speed (for example, 0 to ± 20 knots). This wideband rejection characteristic of the conventional clutter canceller compromises the system capability in detecting moving targets whose doppler frequencies fall within the rejection band.

In addition to the land, sea and rain clutters, the clutter environment may contain other interferences such as



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FIGURE 3.4.4-3: Simulation of Adaptive Clutter Cancellation

chaff and jamming, and the clutter environment may be highly nonstationary with respect to time, range and azimuth angle. For the radar to be effective under such conditions, it is therefore required that the clutter rejection filter be a signal-based, self-adapting one which is capable of sensing the varying clutter situation and structures the filter characteristics to match it. The radar capability in detecting and tracking targets will be severely limited without such an adaptive clutter rejection filter.

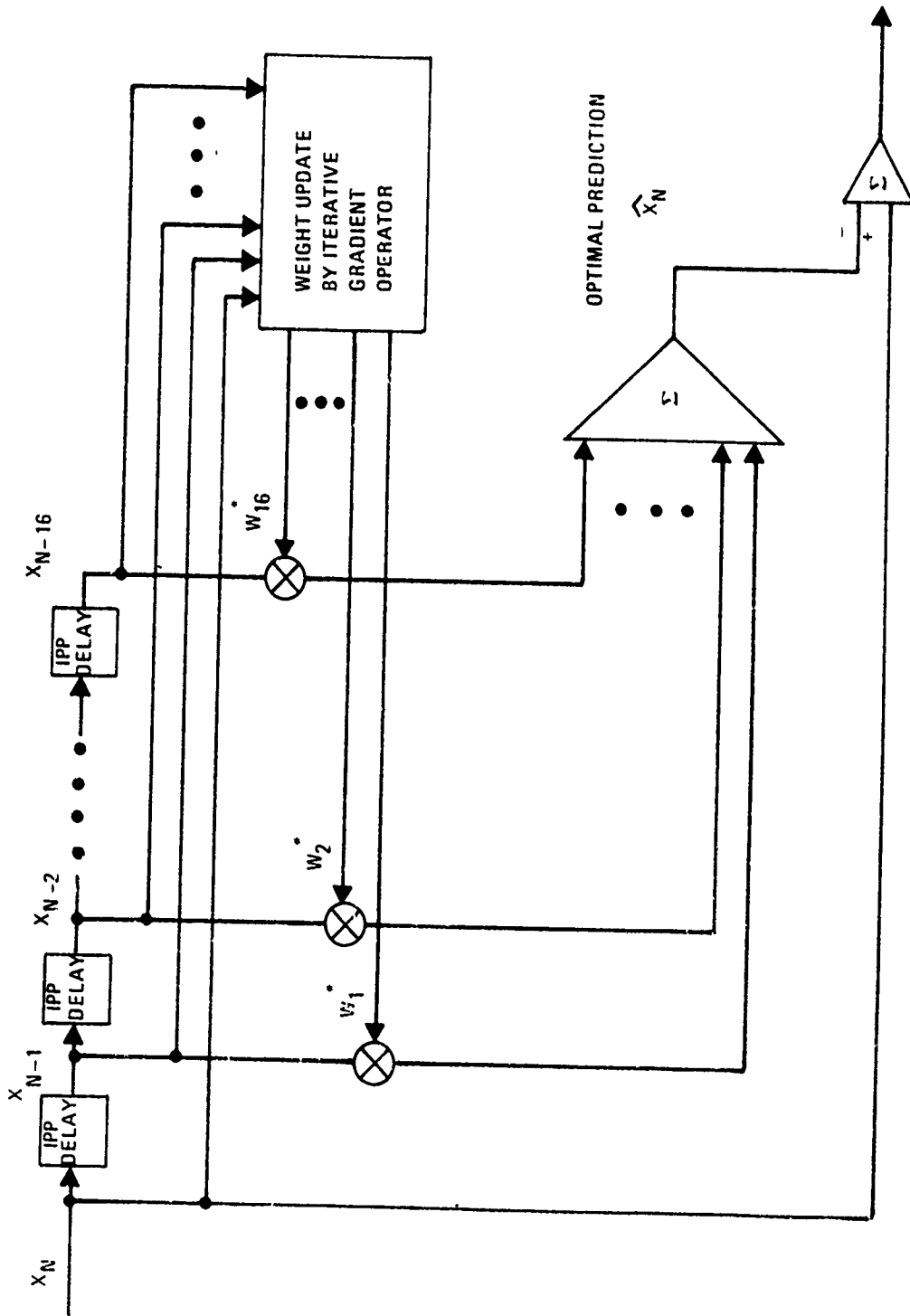
3.4.4.1 Optimum Linear Prediction Procedure

The shortcomings of the conventional clutter rejection filters are overcome with an adaptive clutter canceller which in effect senses the Doppler frequencies of the different clutter sources and automatically places the filter nulls at those frequencies in an optimal manner. The adaptive clutter rejection filter is based on an optimum linear forward prediction procedure. It can be shown that the resulting adaptive filter is identical to that obtained through the maximum entropy method (MEM) of Burg.⁽⁵⁾

Figure 3.4.4-4 shows the block diagram of a 16-weight adaptive clutter rejection filter. The filter inputs $x_n - i$; $i = 0, 1, \dots, 16$ are complex radar measurements of 17 consecutive IPPs at each range cell. The filter output is the difference between radar measurement x_n and the weighted sum of the 16 previous measurements $x_n - i$; $i = 1, 2, \dots, 16$. The weights w_i ; $i = 1, 2, \dots, 16$ will be adaptively generated from the input data based on an optimum forward linear prediction procedure. The procedure involves generating a prediction of x_n , \hat{x}_n , as

$$\hat{x}_n = \sum_{i=1}^{16} w_i^* x_{n-i}$$

such that the expected value of the magnitude squared of the difference between the prediction and the actual measurement is minimized. This mean square error criterion to be minimized



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FIGURE 3.4.4-4: Block Diagram of a 16-Weight Adaptive Clutter Rejection Filter

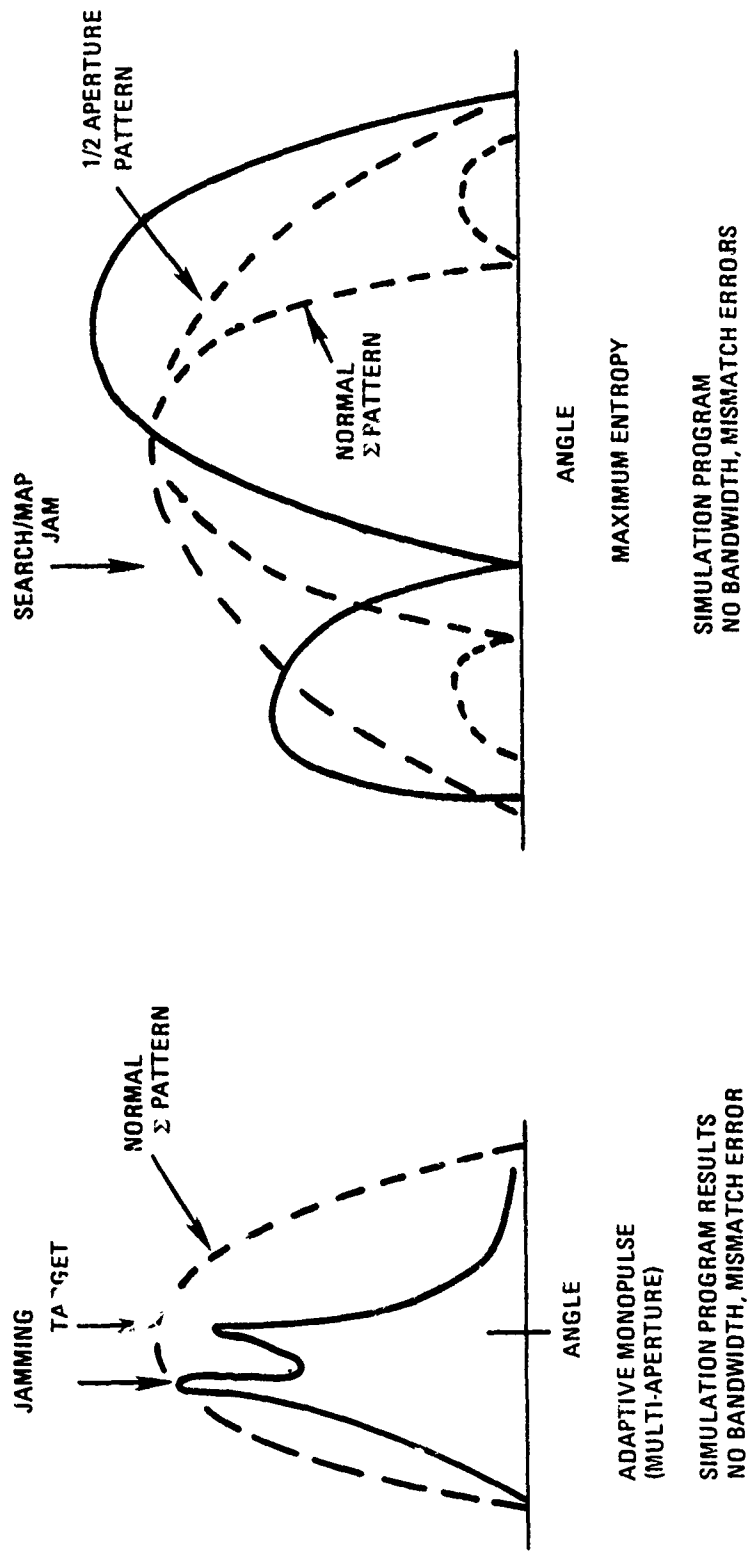
can be expressed as

$$E = |x_n - \hat{x}_n|^2$$

When optimum weights are applied for the prediction of x_n , the difference between the actual measurement and its prediction is essentially a best fit to white noise. The adaptive filter thus obtained is a spectrum weighting filter which will suppress all clutter sources. The performance of a single threshold detector following the adaptive filter will exhibit CFAR characteristics in the Doppler domain.

An adaptive antenna sidelobe canceller (ASLC) has also been modeled. A simulation of its use in adaptive ECM cancellation by mainbeam shaping is shown in Figure 3.4.4-5.

An analog CCD adaptive operator can be incorporated into the above three radar adaption processes, as follows, for the case of adapting the radar signal processor to more accurately reject jamming and unwanted clutter, while enhancing any weak targets which may occur in the vicinity of large clutter or jamming. Either the maximum entropy technique or the technique using two inputs (one is the noise corrupted signal while the other may be the noise corruption alone) can be used to iteratively update the filter weights. The underlying assumption, however, is that the statistical environment must remain stationary during the interative convergence period. Studies are presently underway to characterize the statical nature of radar clutter, i.e., it's "stationarity" as a function of time.



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FIGURE 3.4.4-5: Simulation of Adaptive Antenna Sidelobe Cancellation

Table 3.4.4-1: ADAPTIVE APUP CANDIDATE COMPARISON

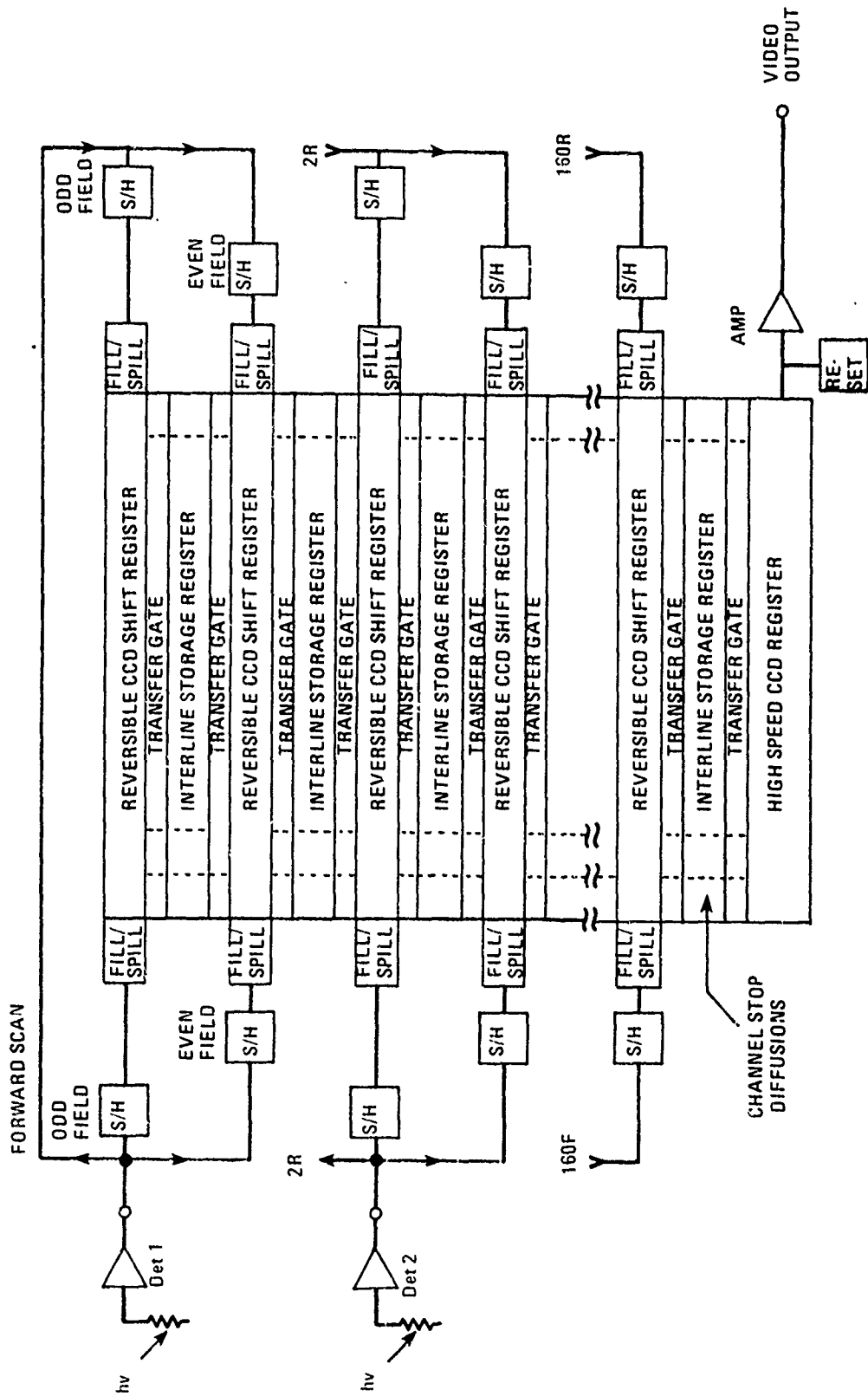
	<u>ALL ANALOG</u>	<u>ANALOG/DIGITAL</u>
Basic Multiplier:	Analog-Analog	MDAC, Analog-binary
Multiplication Product:	Current	Charge
Summation Scheme:	Low Impedance Current Summing Amplifier	Interconnected Capacitor Electrodes
Multiplier Coefficients		
Storage Scheme:	Dynamic MOS Capacitor	Binary Static Registers
Retention Time:	<10 ms (room temp)	Unlimited
Read out:	Indirect, via impulse response	Direct via digital shift register.
Write in:	Complex Housekeeping needs feedback, dynamic adjustment & comparison against desired coefficients via impulse scanning	Direct via digital shift register.
Resolution:	Continuous variability reduces accuracy requirement but temporal drift effects unknown	Word length needs bits for both accuracy and coefficient range.
Adaptive Update:	Both approaches feature parallel update of all coefficients at the same rate as the analog input sampling, to give faster convergence.	

3.4.5. FLIR VIDEO SIGNAL PROCESSING

A modern forward looking infrared (FLIR) system typically uses a line array of detectors with parallel outputs as indicated to the left of figure 3.4.5-1. After buffering, these IR detectors drive a visible light emitting diode (LED) array, which scans (by means of the backside of the very same mirror used to scan the IR detectors over the scene) onto a visible sensing element like a vidicon or the human eye. These last few elements in the signal path must be replaced in order to perform automatic/electronic video signal processing. The wobbly scan mirror has a variety of problems including non-linear mapping of the scene (in the time domain), mechanical instability, the need to interlace viewing fields (like commercial TV) in order to effectively double the number of detectors in the line array, and finally the inability to tightly synchronize the output video with a very stable video data processing computer. All these handicaps are overcome by the FLIR deinterlacer/synchronizer of figure 3.4.5-1.

Basically, the FLIR deinterlacer/synchronizer is a unique analog corner-turn array. Hence, it is operated in tandem or ping-pong fashion, as are all corner-turn arrays. While one of the pair is filling with new data, the previous data are being read from the other one. The array can be filled in several ways, but the following illustrates the techniques for overcoming the aforementioned difficulties. The sequence for detector 1 only is given.

On the forward scan of the first field, data are injected from left to right into the top S/R. As the mirror turns around, they are shifted in parallel to the first interline storage register. The reverse scan then goes into the topmost S/R in the reverse direction and are added to the forward scan pixels simply by the parallel transfer to the interline storage register. This addition effectively averages out some of the mechanical instability of the mirror. The summed first field of video data are held in the odd-field storage registers



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FIGURE 3.4.5-i: FLIR Deinterlacer/Synchronizer

while the whole process is repeated for the even field, which is interlaced by slightly tilting the mirror between fields. At the end of the second field, all the storage registers contain a sum of the forward and reverse scans while the reversible input registers are empty. It is this interlaced storage of the odd fields during the input of the even fields, which provides the "de-interlacing" action during read-out which occurs through the bottom high-speed register. Furthermore, by means of suitable reflective markers on the mirror axle, the signal input sampling can be clocked linearly across the scene. Then during readout the stored data is clocked out synchronous with the video signal processing data base. Thus the device easily linearizes the scan of the scene, de-interlaces the video from a dual-interlaced-field picture frame to a single-noninterlaced-field picture frame, and synchronizes with the data bus so as to greatly facilitate computer video signal processing.

3.5 SYSTEM-RELATED PROCESSOR PARAMETERS

3.5.1 Memory Configuration: Size and Tap Points

A survey has been made of existing radar signal processors to determine what requirements are for register lengths in the various processing applications. The object is to develop a register design which is a best compromise between simplicity and flexibility in meeting the requirements of most radar applications. The two extremes of register design are:

1. registers of fixed length and no taps, which must be either selected in length to fit a particular application, or may be cascaded to form a longer register, or
2. registers sufficiently long to exceed most requirements, but with taps at every few stages to permit use in almost any application.

The first extreme results in no flexibility and no programmability. The second extreme is clearly totally impractical. This section explores the compromises which can be made in both the register design and the processor design which will result in a good combination of register simplicity, flexibility, and efficiency of utilization.

Tap Arrangements

The registers used in the general filter/transform chip will most probably be configured as serial-parallel-serial registers in order to minimize the number of shifts that a datum undergoes in progressing through the register. In order to "bring out taps", the register is actually subdivided into a series of smaller registers, with each "tap" located at the node between two small registers. An arrangement of this sort is illustrated in figure 3.5.1-1. Each small register is a complete serial-parallel-serial register, because a tap anywhere internal to the complete register could bring out only a fraction of the data.

Figure 3.5.1-1 illustrates a register whose taps are uniformly distributed over its length. In contrast, the register

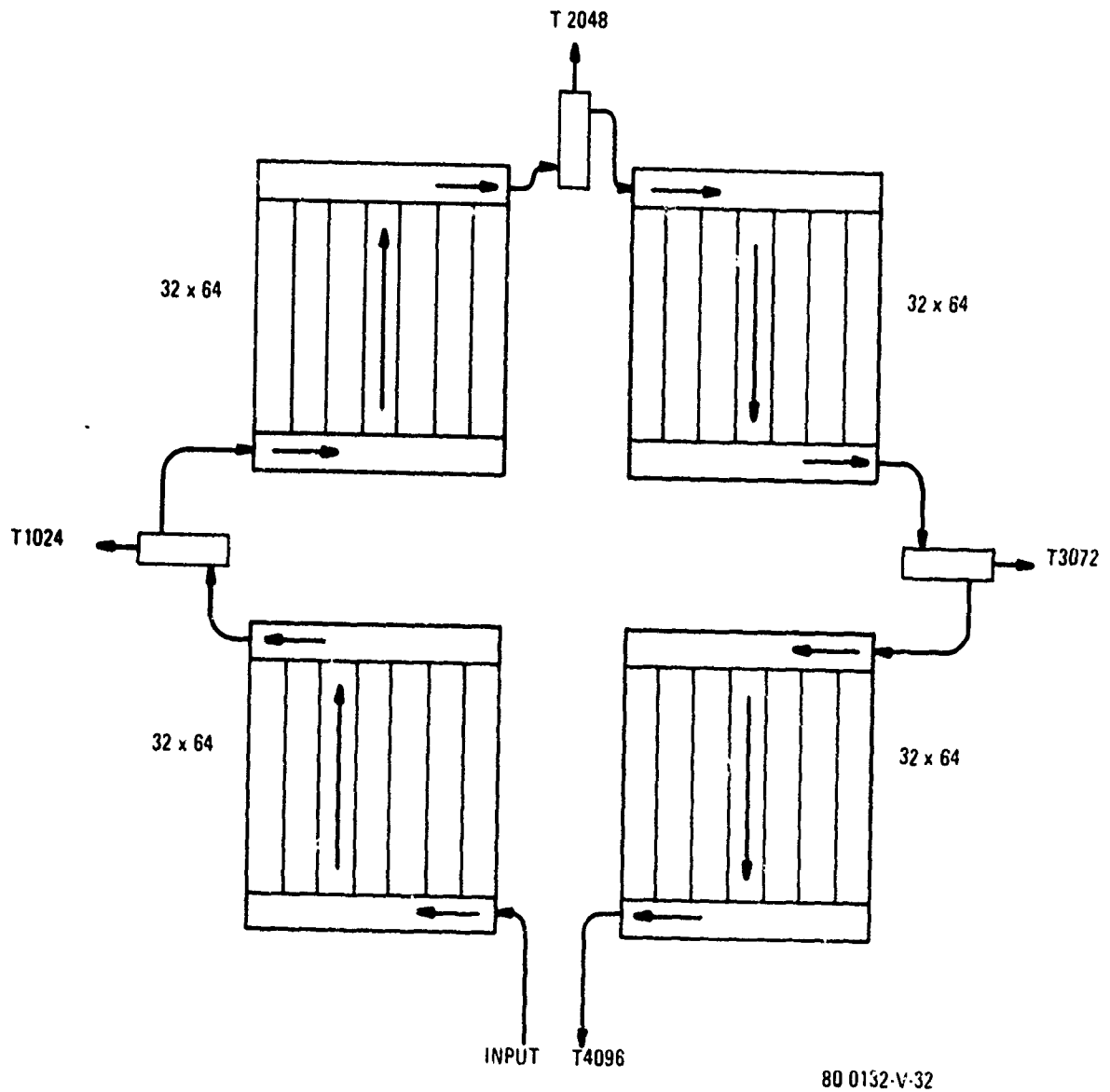
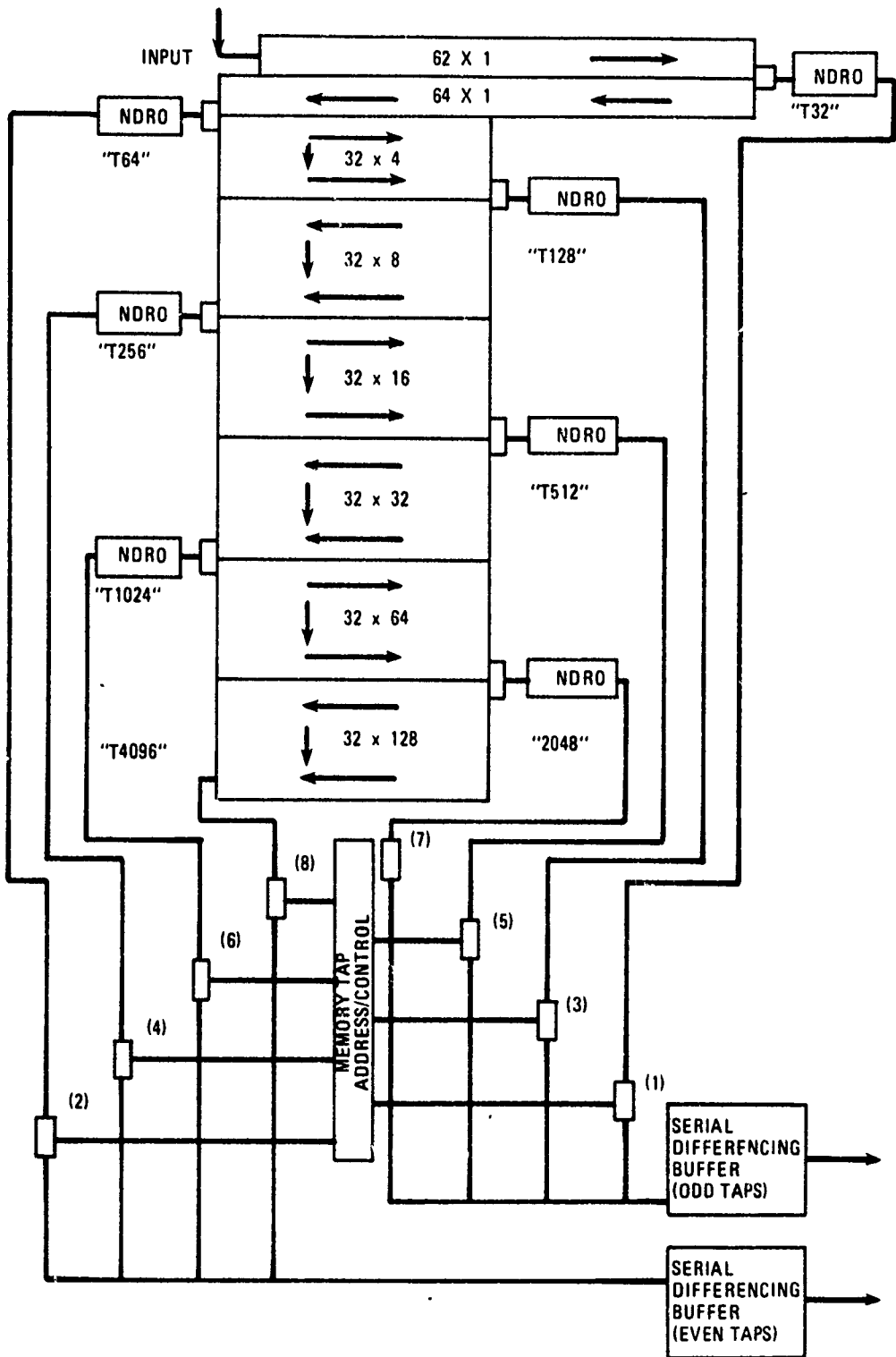


FIGURE 3.5.1-1: Analog Memory with SPS Registers, Tapped Uniformly Along its Length

of figure 3.5.1-2 has its taps arranged in a geometrically increasing fashion with the closest spacing at the beginning of the register. This arrangement makes the space between taps a constant percentage of the distance from the start of the register. It has the advantage over the uniform tap distribution that it gives the closest tap spacing at the beginning of the register where it is most likely to be needed.

The practicalities of chip design make it desirable to limit the number of taps to a reasonably small number. The envisioned uses of the general filter/transform chip do not require connection to more than two taps per register. The tap switching may be done on the chip if sufficient address lines are carried on to the chip to address the correct tap. Register design considerations suggest limiting the number of taps to not more than eight. If eight taps are used then they may be addressed with three address lines. If, further, the register has its taps arranged geometrically according to the ratio r (that is, the distance from the beginning of the register to the n^{th} tap is r times the distance to the $(n-1)^{\text{th}}$ tap), then the overall length of the register is $(r^n - 1)$ times the length of the register to the first tap. If the ratio is equal to 2 and n is taken as 8 (which are both convenient numbers for register design) then the distance to the last tap is 128 times the distance to the first tap. Thus, a register measuring 64 stages to the first tap would have an overall length of 8192 stages.

If a particular application requires a specific number of stages that do not conform to the taps available, then with a geometrically arranged register based on a ratio of 2, in an unlucky situation the closest tap could be wrong by as much as 33 percent. This situation could be improved by placing two or more registers, similarly tapped, on the same chip. For example, with a register as described above (that is, a ratio of 2, eight taps, first tap at the 64^{th} stage) a bad situation would be a requirement for a tap at stage #6144. This would



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Fig 3.5.1-2: Geometrically Ratioed ($r=2$) Tap Distribution

lead to the closest available tap being either at stage 4096 or 8192, an error of 1/3 of the required length. If a second similarly tapped register were cascaded on the chip, then the error would be brought to zero by cascading the second register and taking the output of the first register at tap 4096 and of the second register at tap 2048. To put it in symbolic terms, the use of one register allows the selection of taps at stages numbered $ar^{(n-1)}$, where a is the stage number of the first tap, r is the geometric ratio of the tap arrangement, and n is the number of the tap. The use of the second register in cascade permits achieving a total number of stages of the form $(ar^{(n-1)} + r^{(m-1)})$. If $r = 2$ as in our example, then this expression becomes $a(2^b + 2^c)$, where b and c are integers. The availability of the second register therefore cuts the maximum possible difference between the desired stage and the closest available stage in half. It is apparent that additional cascaded registers would cut this difference further, with each such register reducing the error by a factor of 1/2.

Power Arrangements

The tapped registers described above permit the user to select a register length close to a desired length, but unless some modification is made to the register, the entire register consumes power beyond the tap in use, even though only a fraction of the register may be in actual use. A modification which would remove the disadvantage would be to clock each section of the register through an independent driver. In this arrangement the address lines are not only decoded to select the output tap but to control the clock drivers as well. This architecture permits the unused latter portion of the register to be disconnected from the clock, preventing needless power consumption.

Register Requirements

The survey made of signal processor register requirements in existing radars revealed a very wide range of register lengths, from a low of 49 stages to a high of 11,853. In most

cases the register lengths are neither integer powers of 2 or other "nice even numbers" and consequently do not fall close to any regular series of register taps. This fact causes two questions to arise. First, is a limited selection of register lengths a severe limitation to the design of a new radar system? Second, can existing systems be adapted to make use of the available registers?

For most new radar designs the designer has a wide latitude of selection of radar parameters with which to meet his design objectives. The constraint of a geometrically tapped register with a ratio of 2 would in most cases not be a problem, the closest tap being an acceptable choice. If for some reason a specific number of stages not available at a tap were required, then methods of accommodating to this requirement can be employed. For example, consider an MTI radar with a requirement for 1500 range cells in its clutter canceller to be implemented with processor chips with taps at the 1024th and 2048th stages. In this case the tap at the 2048th stage can be used, and the excess 548 stages can be clocked through during the inactive portion of the interpulse period. This technique is applicable to all cases in which sufficient dead time exists. The penalty for the use of this technique is the increase in power that it requires above power required by a register of just the correct length. In the example, the excess average power would be $548/1500 = 37$ percent.

An alternative and advantageous way of handling the situation of the too-long register is to increase the oversampling ratio of the radar. This reduces the sampling loss which is inherent whenever a continuous signal is converted to discrete samples for further processing. For example, consider a radar whose pulsewidth and receiver bandwidth lead to a range resolution of 1 microsecond as measured at the 3-dB points of the radar's impulse response. A sampling rate of 1 sample per microsecond is sufficient to assure that no point target will miss being sampled, but there is a chance that it may be sampled at the

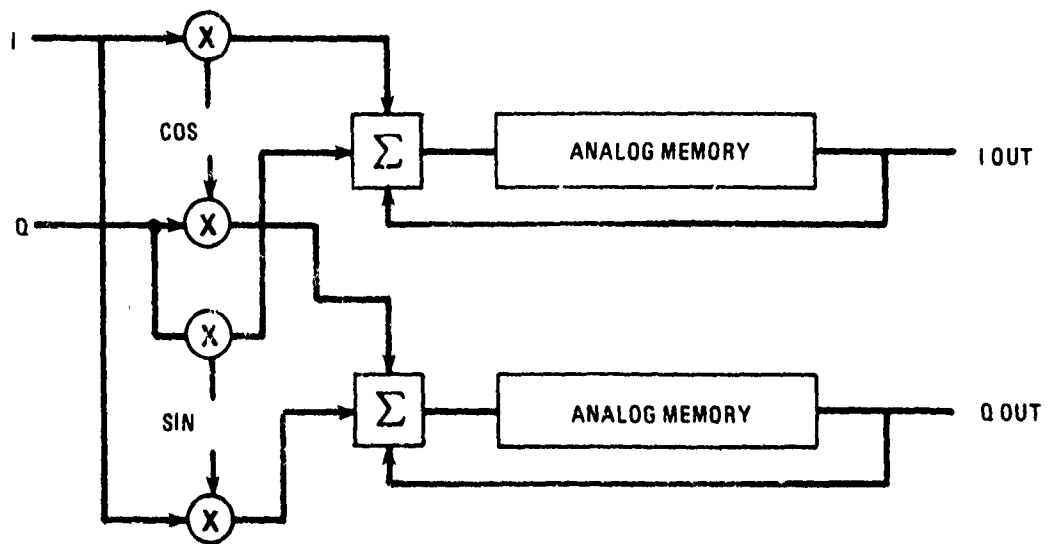
3-dB point of the radar response. This fact causes a loss of detection probability. If the output of the receiver is sampled twice as frequently (an oversampling ratio of 2) then in the worst case the radar response to a point target can be down by no more than a fraction of a decibel. In most cases it is found that the increase in processor input power necessitated by oversampling is more than repaid by a resulting decrease in transmitter power requirements.

It should be noted that an increase in the oversampling ratio is possible even in systems in which there is no dead time during the interpulse period, a situation in which the technique of clocking through excess stages cannot be used.

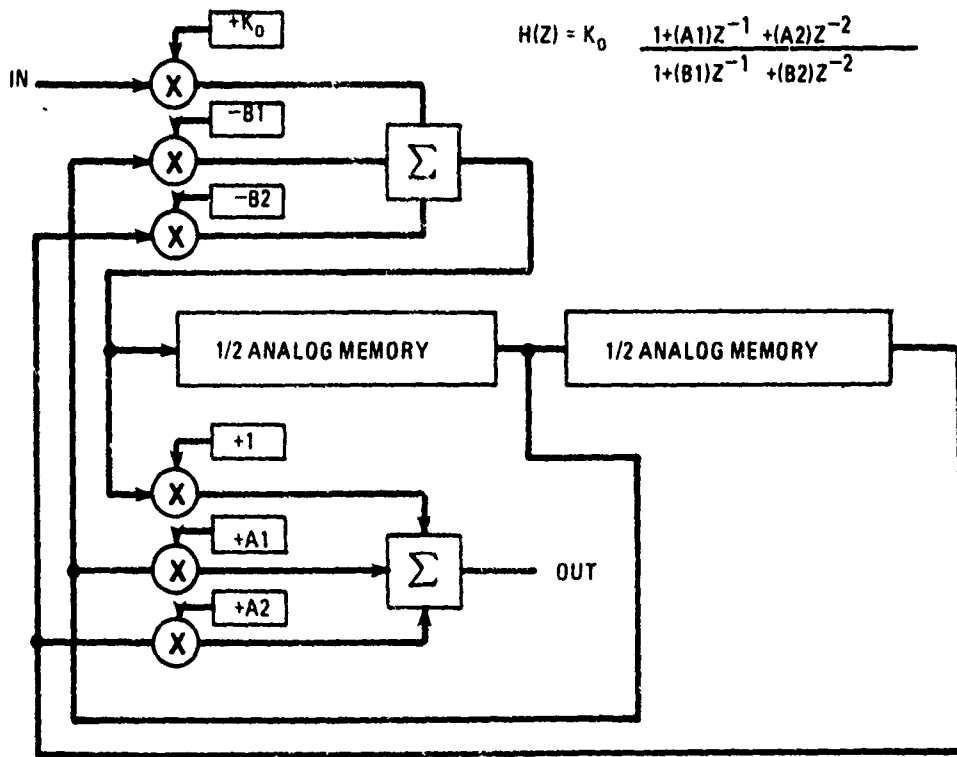
Time multiplexing of the processor chip is still another technique which can be used to increase the utilization of the memory register. One such application is scan-to-scan post detection integration. In a non-coherent scanning radar, post-detection integration is frequently used to improve detection probability by summing all the pulse returns for each range cell for a period which corresponds to the dwell of the antenna pattern on a target. This is usually accomplished by either a continuous technique making use of a two-pole recursive filter or by an "integrate and dump" technique which restarts the integration process every T seconds, where T is the antenna dwell time. A block diagram of a two-pole recursive filter is given in figure 3.5.1-3. This filter can be implemented with general transform/filter chips as shown in figure 3.5.1-4.

Multiplexing several recursive filters into the same analog memory is illustrated in figure 3.5.1-5.

The integrate-and-dump processor is much more amenable to the use of multiplexing. Usually, when an integrate-and-dump processor is used, provision is made for an azimuth oversampling ratio of 3. That is, three integrators are provided for each range cell, with a 67 percent overlap in the integration periods. The simplest conceptual way to implement this scheme using the



a. TRANSFORM CONFIGURATION

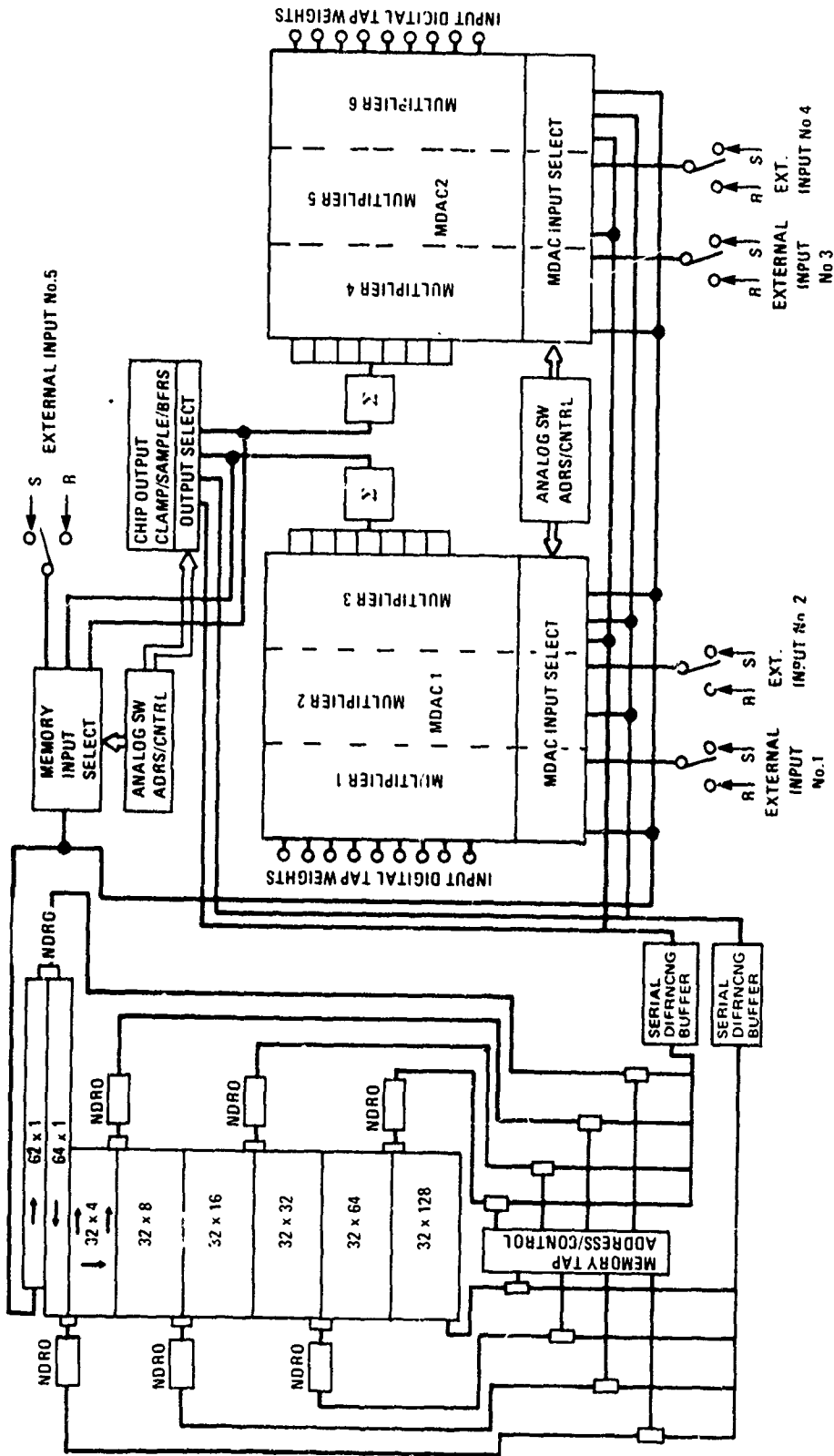


$$H(Z) = K_0 \frac{1+(A1)Z^{-1} + (A2)Z^{-2}}{1+(B1)Z^{-1} + (B2)Z^{-2}}$$

b. RECURSIVE FILTER CONFIGURATION

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Fig 3.5.1-3: Primary APUP Modes



80-0024 VA-10

Fig 3.5.1-4: The APUP General Transform/Filter Chip

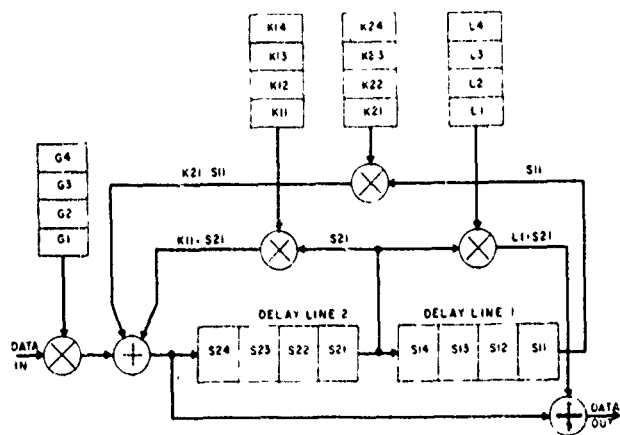


FIGURE 3.5.1-5: Conceptual Diagram of Multiplexed Filter

general filter/transform chip is illustrated in figure 3.5.1-6. The three overlapping channels are interlaced into the single analog memory in the same manner as shown in figure 3.5.1-5. This method uses only one filter/processor chip. It clocks the register at 3 times the range sampling rate, and by so doing uses adjacent stages of the one shift register to store the 3 overlapping integrands for each range cell. Resetting of the integrators is done by inserting a zero feedback coefficient at the high clock rate, thus opening the feedback loop for the selected integrator.

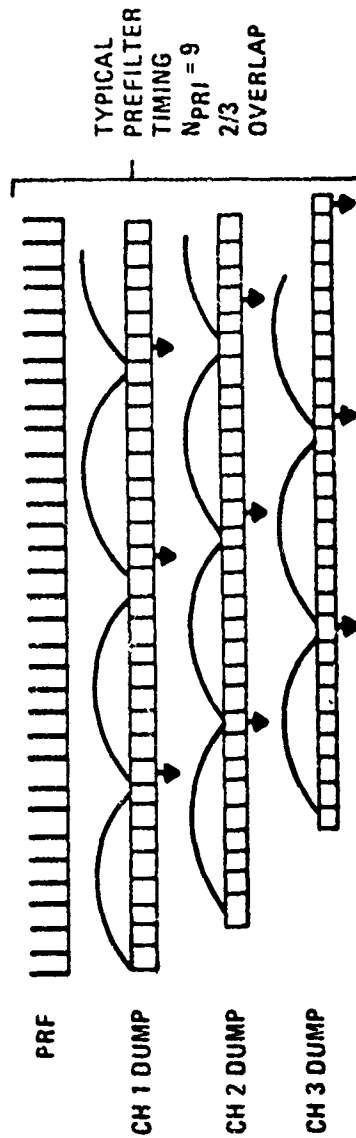
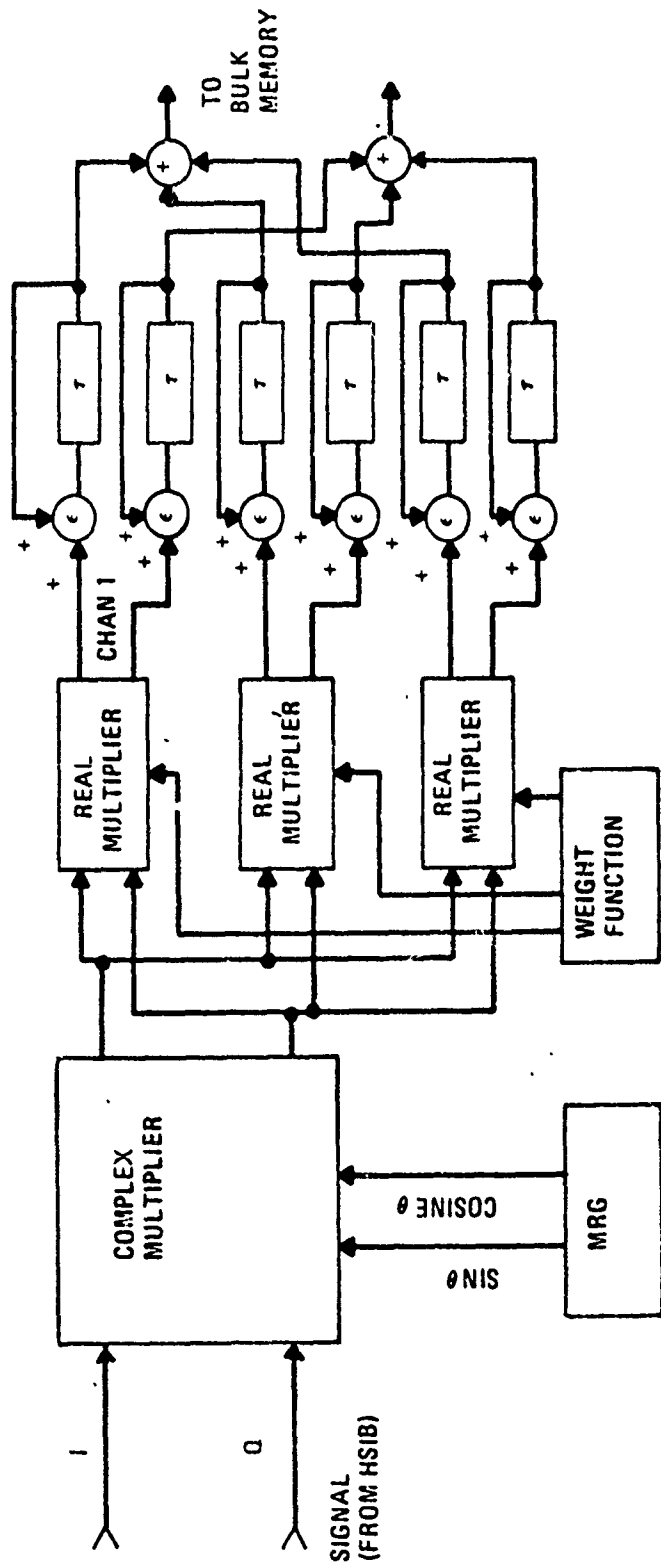
Another application of the general filter/transform chip in which multiplexing can be used in order to improve processor utilization is in Doppler filtering. Airborne pulse Doppler radars usually have air-to-air modes which use a small number of range gates, on the order of 64 or thereabouts. If each frequency channel is implemented with its own filter/transform processor then most of the register capacity of the chips will be wasted. This waste can be avoided or at least minimized by multiplexing the processing of a number of different frequency channels into the same processor chip. This is done by successively multiplying the input for each range cell by the different reference frequencies. There are two limits on the number of channels which can be handled by a processor. First, the product of the number of frequency channels and the number of range cells cannot exceed the length of the shift register. Second, the product of the range sampling frequency and the number of frequency channels cannot exceed the maximum operating frequency of the processor chip, including that of the MDAC's. In many cases this frequency limitation will be far more stringent than the limitation on register length. For example, consider the following parameters of a typical airborne PD radar:

Range sampling rate - 1 MHz

Number of range cells - 128

Number of doppler frequencies - 64

Number of range-frequency cells = $128 \times 64 = 8192$



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FIGURE 3.5.1-6: Overlapping Azimuth Processing

Consider implementing the radar processor with a filter/transform processor chip whose shift register is 8192 elements long with the taps arranged geometrically by powers of 2, the first tap being at the 64th stage. While 64 of these chips could be used to form the frequency filter banks with the registers connected at the third tap (stage #256) to accommodate the in-phase and quadrature components, it can be seen that the total storage requirement of 16,384 cells is just matched to the capacity of the shift registers on two chips. If this were done, however, the processing rate would climb to 64 MHz which is many times the anticipated MDAC speed. A more practical arrangement would be to multiplex 4 complex Doppler channels per processor chip, thus limiting the processing rate to 8 MHz. Connection would be made to the fifth tap (stage #1024) of the shift registers. This arrangement would meet the processing rate limitation and would result in good register utilization. Only 16 processor chips would be required.

3.5.2 MDAC Bit Requirements

An important limit on the performance of the transform/filter chip is the accuracy of the MDAC's. The number of bits comprising each MDAC determines the quantization noise which the MDAC imposes on the signal entering through its digital port. Several conflicting considerations make the choice of number of bits a compromise. On the one hand, the smaller the number of bits, the faster the MDAC can operate and the smaller and cheaper the device will be. On the other hand, the greater the number of bits, the lower the quantization noise and the greater is the dynamic range. In order to determine an appropriate number of bits to suit most applications, an analysis was made of the operation of the transform/filter chip in a typical Fourier transform application. The analysis and simulations will be discussed in the sections which follow.

Analysis

For a signal which is immersed in white noise whose bandwidth is limited only by the sampling rate, the discrete Fourier transform process improves the signal-to-noise ratio by an amount which depends on the time-aperture weighting function. For a uniform weighting function the S/N power ratio improves as the number of points, n , summed in the discrete transform. If a weighting function such as a Hamming or Dolph-Tchebychev is used to reduce the sidelobe level of the transform, then the gain in S/N power ratio is somewhat reduced. The effect of the non-uniform weighting function is to broaden the main lobe of the transform at the expense of approximately 6 to 7 dB of integration gain. However, at the same time the weighting function reduces the buildup of noise power by approximately 4 to 5 dB, making the loss in signal-to-noise improvement only about 2 dB.

The APUP transform/filter processor chip is different from most signal processors in that it is a mixture of analog and digital circuits. The more usual situation is a homogeneous set of all digital or all analog circuitry. In the all-digital processors the quantization noise problem almost always occurs in the quantization of the incoming signal. In the APUP chip, in contrast, it is the reference function rather than the signal that is quantized. The effect of quantization of the signal is easily handled because the combination of signal and receiver noise is relatively broadbanded and noiselike in character. This causes the quantization process to add an uncertainty to the combined signal that is rather well decorrelated from sample to sample. This uncertainty can be represented accurately as an additive noise whose rms value is $q/\sqrt{12}$, where q is the size of the quantum step. In this situation it is easy to set the requirement on the number of bits of accuracy at the input of the processor. To illustrate, let the processor be making an n -point Fourier transform and require that the processing noise at the output be a factor K below the peak response.

Since the transform improves the S/N voltage ratio by approximately \sqrt{n} , the size of the quantum step at the input should be no greater than $\sqrt{12n}/K$ times the peak input signal. For a numerical example, consider a typical radar requirement of a 64-point transform with a sidelobe level of -60 dB or better. The -60 dB requirement corresponds to a K of 1000. If the peak input signal is taken as unity, then the size of the quantum must be less than $\frac{\sqrt{64 \times 12}}{1000} = 0.0277$. This leads to a bit requirement of $\log_2 (0.0277) = 5.17$ bits (plus sign). This number makes no allowance for any processing gain lost due to the weighting function. If 2 dB of loss is allowed, then the processing gain drops from $1.0n$ to $0.794n$. This correction leads to a bit requirement of 5.34 bits. We see that 6 bits plus sign will be required.

The relationships and numbers developed in the preceding paragraph are somewhat optimistic for the APUP processor but can be taken as a lower bound on the bit requirement. In the APUP transform/filter chip it is the weighted reference function which is quantized, and this is a narrow-band, highly un-noise-like waveform. The noise added by quantization cannot in this case be assumed to be uncorrelated from sample to sample but will most likely exhibit some degree of periodicity. The degree of periodicity is not easy to calculate exactly for most circumstances, but an upper bound on the problem can be easily set. Imagine that the reference functions were sawtooth rather than sinusoidal waves. Then the worst case error waveform generated by quantization would also be a sawtooth whose amplitude would be $q/2$. The rms value of this wave is $q/\sqrt{12}$, with most of the energy concentrated at the fundamental frequency. The rms amplitude of the fundamental is $q/(\sqrt{2}\pi) = 0.2250q$, just slightly less than $q/\sqrt{12}$. This concentration of energy would show up as a discrete sideband in the transform and would pass through the process with the same gain as a coherent signal. Consequently, to keep the quantization noise at the output of

the transform no larger than $1/K$ times the peak response for a coherent signal, the quantum size at the input must be set no greater than $q = 1/(0.225K)$. Note that the number of points, n , in the transform does not enter into this calculation. Assuming the same 60-dB S/N requirement as before, $q \leq 1/225$, leading to a requirement for almost 8 bits plus sign.

The size of the MDAC is now bracketed as requiring at least $\log_2 \left(\frac{K}{\sqrt{12n}} \right)$ bits but no more than $\log_2 (0.225K)$ bits plus sign. Fractional results must, of course, be rounded to the next higher integer. For our 64-point 60-dB sidelobe example, this is a range of 6 bits to 8 bits. This is too wide a range to be satisfactory for design purposes since it corresponds to a four-to-one range in MDAC speed and in production accuracy. Since a more exact analysis is not practical, a series of computer simulations were made.

Computer Simulation

As a baseline for the simulation studies it was decided to investigate the use of the transform/filter chip for the typical MTI filtering job used as an example earlier. That is, all simulations were made of a 64-point Fourier transform using a 60-dB weighting function. A first quick simulation was made by taking advantage of an existing fast Fourier transform (FFT) software package. Although the transform/filter chip operates by taking a discrete Fourier transform by convolution rather than by an FFT, this first simulation had the advantage of using proven software such that its results could be used as a check against which further more exact simulations could be matched.

This first simulation was made as illustrated by the flow chart of figure 3.5.2-1. A sinusoidal signal with a frequency of 15 cycles per 64 samples was generated. Then a 60-dB Dolph-Tchebychev weighting function was generated. The weighting function was then quantized to the desired degree of fineness and used to multiply the stored signal. The weighted signal was then processed by the FFT subroutine. The output of a

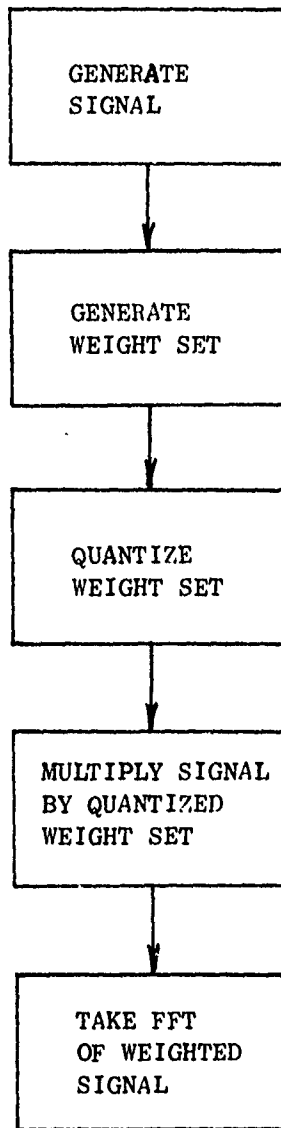


FIGURE 3.5.2-1: Flow Diagram of First Simulation

typical computer run is given in table 3.5.2-1. This table gives the complete simulation output showing important intermediate results which, for the sake of compactness, are omitted from later summary tables. The first set of data shows the 64 consecutive samples of the signal. The data read from left to right and top to bottom, as do all subsequent arrays. The second array is a tabulation of the quantized weight set. An examination of the data will reveal that although the data is represented to 7 decimal places, the numbers are all multiples of $1/64$, or .015625. This corresponds to the fineness achieved using 6 bits plus sign. The next array is the product of the signal array and the quantized weight set. The next array is the output of the FFT. These data are complex, and are to be read as pairs of numbers, a real followed by an imaginary. The first pair of numbers are an exception in that the first number is the DC component and the second would be identically equal to zero except for computer round-off errors. The second pair of numbers are the in-phase and quadrature components of the filter at the fundamental frequency (that is, one cycle per 64 points). Succeeding pairs are the second, third, etc. harmonics. The data are not normalized, and show the full gain of the Fourier transform. The next data array, labelled "Results for Quantizing, etc." presents the transform data as normalized by the transform gain and then converted to decibels. The next data array differs in that the normalization has been made to the peak response of the transform. The final array of data is the power spectrum expressed in dB relative to the peak response. Table 3.5.2-2 summarizes the results of runs of this program made for five degrees of quantization running from 6 to 10 bits. Only the normalized power spectrum data is presented in this summary.

Table 3.5.2-2 shows that six bits (plus sign) of quantization is inadequate to preserve the 60-dB sidelobe level which should be yielded by the weighting function. The six-bit run gave one sidelobe of only 47.9 dB down and many others in the -50-dB

Table 3.5.2-1: Fast Fourier Transform (FFT) Simulation:
60dB Dolph-Tchebychev weights only quantized to 6 bits.

APUP.LP 8/15/79 19:20:53 CREATED 8/15/1979 19:20:00

64-POINT SIGNAL WITH FREQUENCY= 15.000									
1.000	.098	-.981	-.290	.924	.471	-.831	-.634	.707	.773
-.356	-.882	.383	-.957	-.195	-.995	-.000	-.995	.195	-.957
-.383	.882	.556	-.773	-.707	.634	.831	-.471	-.924	.290
.981	-.098	-1.000	-.098	.981	.290	-.924	-.471	.831	.634
-.707	-.773	.556	-.882	-.383	-.957	-.195	-.995	.000	-.995
-.195	.957	.383	-.882	-.556	.773	.707	-.634	-.832	.471
-.924	-.290	-.981	.098						
WEIGHT SET QUANTIZED TO 6 BITS									
.0312500	.0156250	.0312500	.0468750	.0625000					
.0781250	.0937500	.1093750	.1406250	.1718750					
.2031250	.2343750	.2612500	.3125000	.3593750					
.4062500	.4531250	.5000000	.5625000	.6093750					
.6562500	.7031250	.7500000	.7968750	.8437500					
.8750000	.9062500	.9375000	.9687500	.9843750					
1.0000000	1.0000000	1.0000000	1.0000000	1.0000000					
.9687500	.9375000	.9062500	.8750000	.8437500					
.7968750	.7500000	.7031250	.6562500	.6093750					
.5625000	.5000000	.4531250	.4062500	.3593750					
.3125000	.2612500	.2343750	.2031250	.1718750					
.1406250	.1093750	.0937500	.0781250	.0625000					
.0468750	.0312500	.0156250	.0312500						

WEIGHTED SIGNAL				
.31250E-01	.15315E-02	-.30650E-01	-.13607E-01	.57742E-01
.36828E-01	-.77950E-01	-.69387E-01	.99436E-01	.13286
-.11285	-.20670	.10763	.29905	-.70102E-01
-.40429	-.77439E-05	.49759	.10975	-.58313
-.25116	.62009	-.41669	-.61597	-.59664
.55307	.75354	-.44190	-.89507	.28571
.98079	-.97979E-01	-1.00000	-.98063E-01	.76545
.28125	-.86612	-.42724	.72752	.53530
-.56345	-.57978	.39060	.57873	-.23317
-.53029	.97516E-01	.45095	.20700E-04	-.35764
-.60984E-01	.26913	.89706E-01	-.17913	-.95497E-01
.10870	.77345E-01	-.59470E-01	-.64968E-01	.29458E-01
.43308E-01	-.90690E-02	-.15325E-01	.30603E-02	

TRANSFORMED WEIGHTED SIGNAL				
.18111E-01	.30246E-08	.28896E-01	.47323E-02	.46192E-01
-.24376E-01	-.24554E-02	.58467E-02	.23839E-01	-.11226E-01
.24935E-01	.18633E-01	.93593E-02	.38633E-01	-.20018E-01
.56724E-02	-.40686E-02	.87455E-02	.65460E-02	.67984E-02
-.21006E-01	.20350E-01	-.88262E-02	.50522E-02	-.24270E-03
.12108E-01	.65809	-.71496E-01	-.78133	.38718
15.125	.28085E-02	-.78127	-.35640	.65936
.64916E-01	-.18349E-02	-.27635E-01	.94030E-02	-.53536E-02
-.26281E-01	-.96544E-02	.20387E-02	.75193E-02	-.41131E-02
-.14154E-01	-.17914E-01	-.10918E-01	-.58554E-02	-.18737E-01
.12426E-01	-.29188E-02	.25208E-01	.71195E-02	-.58340E-02
-.97141E-03	.60977E-01	-.32693E-02	.28967E-01	-.12662E-01
.10660E-01	.60863E-02	.17842E-01	.12910E-01	.10727E-01

RESULTS FOR QUANTIZING WITH 64 POINT WEIGHTING FUNCTION TO 6 BITS.									
-64.944	-200.490	-60.896	-76.601	-56.812	-62.364	-82.301	-74.765	-62.561	-69.099
-62.167	-64.697	-70.678	-58.364	-64.075	-75.023	-77.914	-71.267	-73.784	-73.455
-63.332	-63.932	-71.188	-76.033	-102.402	-68.442	-33.737	-53.017	-12.246	-38.345
-6.509	-81.134	-12.247	-39.064	-33.721	-53.854	-84.831	-61.274	-70.638	-75.530
-61.710	-70.409	-83.916	-72.580	-77.820	-67.034	-65.039	-69.340	-74.752	-64.649
-68.216	-80.799	-62.072	-73.054	-74.784	-90.355	-54.400	-79.814	-60.865	-68.053
-69.548	-74.416	-65.074	-67.879						

RESULTS FOR QUANTIZING WITH 64 POINT WEIGHTING FUNCTION TO 6 BITS.									
-58.435	-193.981	-54.377	-70.093	-50.303	-55.855	-75.792	-68.256	-56.052	-62.590
-55.658	-58.188	-64.169	-51.855	-57.566	-60.519	-71.405	-64.758	-67.275	-66.946
-56.823	-57.423	-64.679	-69.524	-95.893	-61.933	-27.228	-46.508	-5.737	-31.836
.000	-74.625	-5.738	-32.555	-27.212	-47.347	-78.322	-54.765	-64.129	-69.021
-55.201	-63.900	-77.407	-66.071	-71.311	-60.577	-58.530	-62.831	-68.243	-58.140
-61.707	-74.290	-55.563	-66.545	-68.275	-83.846	-47.891	-73.305	-54.356	-61.544
-63.039	-67.907	-58.565	-61.370						

PEAK RESPONSE= -6.5089				
-58.435	-54.262	-49.236	-67.550	-55.181
-53.731	-51.608	-57.230	-63.907	-64.097
-54.102	-63.448	-61.931	-27.177	-5.7262
.00000	-5.7291	-27.170	-54.746	-62.909
-54.651	-65.763	-60.225	-57.159	-57.735

-61.474	-55.230	-68.156	-47.878	-53.596
-61.813	-56.735			

Table 3.5.2-2: Summary of FFT results for quantizing only the weighting function.

APUP60DB1.LP 8/15/79 20:18:20 CREATED 8/15/1979 20:14:00

This file is a series of runs of APUP for a 60-dB weighting function. An FFT is used to perform the Fourier transform. The weighting function is quantized to the number of bits shown for each run.

NBITS=64, HARMONIC=15.00
NBITS=6

PEAK RESPONSE= -6.509

-58.435	-54.262	-49.236	-67.550	-55.181
-53.731	-51.608	-57.230	-63.907	-64.097
-54.102	-63.448	-61.931	-27.177	-5.7262
.00000	-5.7291	-27.170	-54.746	-62.909
-54.651	-65.763	-60.225	-57.159	-57.735
-61.474	-55.230	-68.156	-47.878	-53.596
-61.813	-56.735			

NBITS=64, HARMONIC=15.00
NBITS=7

PEAK RESPONSE= -6.504

-91.669	-62.369	-61.753	-61.507	-64.546
-64.303	-63.071	-60.068	-61.743	-65.527
-66.139	-58.769	-55.411	-28.000	-5.7374
.00000	-5.7368	-28.003	-55.564	-65.408
-70.049	-65.528	-65.255	-59.517	-61.812
-65.551	-62.031	-61.000	-67.627	-62.067
-64.483	-61.098			
-78.561	-74.263	-65.609	-69.041	

NBITS=64, HARMONIC=15.00
NBITS=8

PEAK RESPONSE= -6.498

-91.046	-62.909	-70.225	-63.478	-71.562
-62.942	-74.987	-65.387	-73.614	-62.100
-63.126	-59.494	-76.581	-27.746	-5.7388
.00000	-5.7382	-27.730	-67.095	-59.628
-63.060	-61.925	-76.354	-67.477	-71.933
-67.919	-72.317	-65.773	-70.693	-61.579
-72.891	-63.984			

NBITS=64, HARMONIC=15.00
NBITS=9

PEAK RESPONSE= -6.494

-64.428	-69.556	-69.206	-69.657	-62.992
-70.689	-69.851	-75.509	-71.291	-66.870
-61.860	-59.336	-63.831	-27.849	-5.7416
.00000	-5.7422	-27.854	-63.610	-59.292
-62.023	-73.565	-72.030	-77.314	-71.982
-66.760	-65.164	-75.118	-69.045	-70.702
-65.284	-68.447			

NBITS=64, HARMONIC=15.00
NBITS=10

PEAK RESPONSE= -6.496

-67.999	-65.987	-65.379	-67.671	-66.265
-67.210	-68.883	-67.381	-68.366	-72.556
-63.960	-60.664	-65.242	-27.806	-5.7403
.00000	-5.7402	-27.808	-65.075	-60.683
-63.160	-73.242	-75.902	-75.939	-72.428
-70.473	-66.973	-66.515	-66.341	-66.999
-67.227	-67.521			

range. The seven-bit run did much better with only 1 sidelobe slightly higher than -60 dB. No final conclusion can be drawn from these data, however, because the FFT simulation was not an exact simulation of how the transform/filter chip works. In this simulation, only the weighting function was quantized whereas in actuality the transform/filter chip requires quantization of the product of the weighting function with the individual sinusoidal reference functions. For that reason further simulations were made.

The second simulation is summarized by table 3.5.2-3. This simulation used a convolution transform rather than an FFT and so was somewhat more accurately representative of the action of the transform/filter chip. However, once more the quantization was confined to the weighting function rather than to the product of the weighting function and the reference. This was done to provide output to check directly against the first simulation. Before attempting a comparison of tables 3.5.2-2 and 3.5.2-3, one must take note that the format is somewhat different. The data in each output array of table 3.5.2-3 starts with the fundamental, rather than with the DC component which isn't given. This fact displaces all of the data in table 3.5.2-3 one position to the left of the corresponding data in table 3.5.2-2. With this fact in mind, an examination of the data shows very good agreement between the two simulations. This experiment verifies the software used in the second simulation.

The next simulation, summarized by the data of table 3.5.2-4, quantized the weighted reference functions and so was a full simulation of the APUP mechanization. These data, like the data for the previous simulation (table 3.5.2-3), starts with the fundamental component and does not give the DC term. This fact is also true for all tables which follow. A comparison of table 3.5.2-4 with tables 3.5.2-2 or 3.5.2-3 shows that quantizing the weighted reference functions has somewhat degraded the performance. Seven-bit quantization is no longer

Table 3.5.2-3: Summary of results for a convolution transform with quantization of weights only.

APUP260.LP 8/15/79 21: 9:44 CREATED 8/15/1979 21: 9:00

This file is a series of runs of APUP2 for a 60-dB weighting function. A convolution is used to perform the transform. To check against the results of the FFT experiment, the weighting function is quantized before multiplying the reference functions.

NBITS: 64, HARMONIC=15
NBITS: 6

PEAK RESPONSE= -6.509

-54.262	-49.236	-67.554	-55.182	-53.733
-51.606	-57.238	-63.903	-64.079	-54.104
-63.448	-61.928	-27.178	-5.7264	00000
-5.7290	-27.169	-54.750	-62.906	-54.657
-65.783	-60.232	-57.159	-57.734	-61.475
-55.228	-68.147	-47.879	-53.597	-61.815
-56.734	-62.985			

NBITS: 64, HARMONIC=15
NBITS: 7

PEAK RESPONSE= -6.504

-62.371	-61.753	-61.506	-64.546	-64.305
-63.062	-60.055	-61.768	-65.529	-66.144
-58.770	-55.409	-28.000	-5.7376	00000
-5.7367	-28.002	-55.564	-65.412	-70.036
-63.488	-65.237	-59.548	-61.813	-65.553
-62.029	-61.000	-67.616	-62.063	-64.493
-61.111	-59.256			

NBITS: 64, HARMONIC=15
NBITS: 8

PEAK RESPONSE= -6.497

-62.908	-70.227	-63.480	-71.567	-62.947
-75.031	-65.409	-73.590	-62.105	-63.134
-59.494	-76.560	-27.727	-5.7389	00000
-5.7381	-27.730	-67.076	-59.626	-63.075
-61.899	-76.310	-67.475	-71.928	-67.922
-72.312	-65.783	-70.688	-61.580	-72.869
-63.967	-78.834			

NBITS: 64, HARMONIC=15
NBITS: 9

PEAK RESPONSE= -6.494

-69.554	-69.207	-69.658	-62.994	-70.704
-69.848	-75.435	-71.285	-66.860	-61.866
-59.335	-63.829	-27.850	-5.7418	00000
-5.7421	-27.853	-63.620	-59.290	-62.037
-73.535	-72.096	-77.317	-71.975	-66.760
-65.158	-75.127	-69.054	-70.701	-65.291
-68.427	-68.442			

NBITS: 64, HARMONIC=15
NBITS: 10

PEAK RESPONSE= -6.49

-65.986	-65.380	-67.620	-66.267	-67.218
-68.892	-67.357	-68.356	-72.555	-63.968
-60.564	-65.240	-27.806	-5.7404	00000
-5.7401	-27.807	-65.078	-60.681	-63.176
-73.149	-75.978	-75.938	-72.423	-70.476
-66.970	-66.514	-66.344	-67.000	-67.237
-67.505	-67.482			

Table 3.5.2-4: Summary of results for APUP Convolution transform with weighted reference products quantized.

APUP560DB1.LP 8/15/79 20:31: 5 CREATED 8/ 3/1979 15:50:00

This file is a series of runs of APUP5 for a 60-dB weighting function. The signal frequency is held constant at the 15th harmonic, but the number of bits of quantization is varied.

NPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 6

PEAK RESPONSE= - -6.5097
 -58.169 -55.797 -60.957 -57.826 -60.257
 -54.614 -60.634 -65.400 -58.776 -49.730
 -55.761 -67.103 -27.657 -5.7266 .00000
 -5.7254 -27.525 -58.512 -51.909 -59.507
 -62.675 -58.869 -54.895 -59.439 -64.856
 -56.183 -60.465 -54.072 -56.695 -57.997
 -55.132 -65.552

NPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 7

PEAK RESPONSE= - -6.4970
 -49.313 -64.163 -55.151 -70.454 -59.606
 -61.435 -68.440 -66.736 -63.155 -61.468
 -60.907 -64.368 -28.011 -5.7468 .00000
 -5.7446 -27.703 -59.459 -57.845 -60.249
 -66.139 -70.162 -77.244 -61.720 -62.093
 -59.635 -66.151 -71.752 -74.020 -67.256
 -64.392 -61.830

NPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 8

PEAK RESPONSE= - -6.4995
 -74.605 -63.395 -63.217 -73.077 -61.213
 -69.397 -64.981 -70.586 -71.530 -63.421
 -63.596 -61.586 -27.817 -5.7347 .00000
 -5.7373 -27.797 -60.732 -59.879 -62.654
 -63.910 -69.986 -66.432 -80.263 -63.887
 -71.116 -71.451 -64.635 -79.926 -63.574
 -66.687 -81.430

NPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 9

PEAK RESPONSE= - -6.4952
 -70.401 -67.329 -69.428 -70.268 -78.683
 -77.304 -78.991 -73.151 -70.100 -65.820
 -59.835 -65.152 -27.820 -5.7379 .00000
 -5.7414 -27.870 -66.616 -60.513 -65.333
 -69.977 -74.982 -82.769 -77.059 -67.394
 -64.436 -67.655 -103.47 -69.015 -69.001
 -68.668 -71.015

NPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 10

PEAK RESPONSE= - -6.4958
 -70.752 -70.815 -75.054 -70.608 -69.350
 -70.401 -79.392 -76.523 -73.673 -66.952
 -60.706 -64.467 -27.812 -5.7413 .00000
 -5.7407 -27.808 -63.760 -60.614 -64.990
 -72.174 -78.450 -88.026 -75.879 -73.972
 -70.697 -68.735 -69.222 -68.758 -75.973
 -74.920 -70.055

sufficient to ensure no sidelobes materially higher than -60 dB. Eight bits are now required.

The next two tables present the results of a study intended to examine the effect of moving the signal frequency from the center to the edge of the filter bin. In both tables the signal frequency is stepped from the 15th to the 15.5th harmonic by steps of 0.1. Table 3.5.2-5 holds the quantization level constant at 7 bits and table 3.5.2-6 holds it at 8 bits. Both of these tables show some degradation of performance as the signal frequency moves off center. Part of this degradation is apparent, rather than real, because of the fact that each set of data is normalized to the strongest filter response, rather than to a fixed value. This makes all of the numbers for the 15.5th harmonic look 1.4 dB worse than they would have had they been normalized to the same reference as the centered (15th harmonic) case. Another part of the reason for the somewhat worse performance as the signal moves off from the filter center is that the Dolph-Tchebychev weighting function does not have its sidelobe peaks fall exactly at the centers of the various filters.

Of course, if an overall sidelobe level of better than -60 dB is desired, it should not be too surprising that it cannot be achieved if the selection of weighting function alone causes sidelobes of that level. For that reason, another series of computer runs was made, repeating the conditions which gave rise to the last three tables but with a change to a 63-dB Dolph-Tchebychev weighting function. By and large, the results are improved. Table 3.5.2-7 shows that 7 bits of quantization is now almost sufficient to give -60 dB performance for a signal located in the center of a filter. Tables 3.5.2-8 and-9 step the signal frequency from filter center to filter edge for 7 and 8 bits of quantization respectively. The data of table 3.5.2-9 shows that 8 bits of quantization performs nicely even for the case of the signal lying at the filter edge (15.5th harmonic). If an adjustment of -1.3 dB is made

Table 3.5.2-5: Summary of APUP Transform Results as Signal Moves through Doppler Channel (7 bits quantization).

APUP560DB2.LP 8/15/79 20:31: 9 CREATED 8/ 3/1979 15:49:00

This file is a series of runs of APUP5 for a 60-dB weighting function. The number of bits of quantization is held constant at 7, but the signal frequency is varied from the 15th to the 15.5th harmonic.

NPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 7

PEAK RESPONSE= - -6.4970

-69.313	-64.163	-55.151	-70.454	-59.606
-61.435	-68.440	-66.736	-63.135	-61.468
-40.907	-64.368	-28.011	-5.7440	.00000
-5.7446	-27.703	-59.459	-57.845	-60.249
-66.139	-70.162	-77.244	-61.720	-62.093
-59.635	-66.151	-71.752	-74.030	-67.256
-64.392	-61.830			

NPTS= 64, HARMONIC= 15.10, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 7

PEAK RESPONSE= - -6.5521

-63.985	-65.204	-54.644	-69.349	-60.126
-58.513	-63.522	-69.649	-64.068	-66.732
-62.106	-60.561	-32.156	-6.9738	.00000
-4.5576	-24.151	-63.524	-57.860	-57.624
-64.815	-63.140	-67.190	-64.239	-59.700
-60.874	-73.984	-64.368	-68.900	-72.685
-63.242	-67.154			

NPTS= 64, HARMONIC= 15.20, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 7

PEAK RESPONSE= - -6.7173

-60.579	-62.003	-54.192	-64.508	-59.946
-56.670	-59.878	-66.072	-62.922	-69.310
-65.007	-58.925	-37.073	-8.2456	.00000
-3.3973	-20.913	-68.550	-58.844	-56.030
-63.128	-59.564	-62.784	-64.088	-57.535
-61.036	-79.001	-60.429	-63.106	-72.472
-61.377	-82.918			

NPTS= 64, HARMONIC= 15.30, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 7

PEAK RESPONSE= - -6.9934

-58.365	-59.161	-53.924	-61.505	-59.481
-55.550	-57.516	-62.683	-60.710	-63.528
-71.709	-58.653	-43.358	-9.5727	.00000
-2.2563	-17.909	-65.110	-61.327	-55.157
-61.811	-57.450	-60.276	-61.709	-55.920
-59.925	-67.777	-57.959	-59.613	-67.713
-59.795	-71.164			

NPTS= 64, HARMONIC= 15.40, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 7

PEAK RESPONSE= - -7.3820

-56.943	-57.297	-53.942	-59.817	-59.165
-55.019	-56.030	-60.650	-58.747	-59.645
-80.226	-59.225	-52.808	-10.968	.00000
-1.1279	-15.082	-65.552	-67.108	-54.915
-60.982	-56.250	-58.891	-59.444	-54.847
-58.404	-63.360	-56.355	-57.333	-64.780
-58.765	-64.586			

NPTS= 64, HARMONIC= 15.50, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 7

PEAK RESPONSE= - -7.8849

-56.140	-56.208	-54.347	-59.110	-59.279
-55.074	-55.213	-59.705	-57.376	-57.381
-66.434	-60.061	-61.332	-12.449	.00000

-54.779E-02	-12.390	-62.671	-81.082	-55.293
-60.553	-55.812	-58.338	-57.926	-54.278
-57.139	-60.909	-55.395	-55.852	-63.363
-58.296	-61.474			

Table 3.5.2-6: Summary of APUP Transform Results as Signal Moves through Doppler Channel (8 bits quantization).

APUP560DB3.LP 8/15/79 20:31:14 CREATED 8/ 3/1979 15:52:00

This file is a series of runs of APUP5 for a 60-dB weighting function. The quantization level is held constant at 8 bits, but the signal frequency is varied from the 15th to the 15.5th harmonic.

NPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 8

PEAK RESPONSE= - -6.4995

-74.605	-63.395	-63.217	-73.077	-61.213
-69.397	-64.981	-70.586	-71.530	-63.421
-63.596	-61.586	-27.817	-5.7347	.00000
-5.7373	-27.797	-60.732	-59.879	-62.654
-63.910	-69.986	-66.432	-80.263	-63.887
-71.116	-71.451	-64.635	-79.926	-63.574
-66.687	-81.430			

NPTS= 64, HARMONIC= 15.10, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 8

PEAK RESPONSE= - -6.5548

-67.034	-61.234	-61.180	-74.514	-58.892
-71.395	-65.499	-64.830	-69.198	-69.981
-68.004	-58.644	-31.863	-6.9530	.00000
-4.5509	-24.223	-66.041	-59.296	-60.840
-60.590	-67.964	-65.406	-68.540	-70.155
-63.872	-75.100	-69.162	-67.189	-68.876
-73.126	-73.752			

NPTS= 64, HARMONIC= 15.20, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 8

PEAK RESPONSE= - -6.7201

-63.303	-59.774	-60.044	-65.829	-57.172
-67.352	-63.558	-61.065	-62.490	-78.363
-81.747	-57.826	-36.603	-8.2152	.00000
-3.3906	-20.968	-64.760	-59.842	-60.077
-58.738	-65.078	-62.432	-63.040	-77.773
-60.034	-65.667	-73.057	-61.092	-84.586
-79.303	-66.073			

NPTS= 64, HARMONIC= 15.30, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 8

PEAK RESPONSE= - -6.9964

-61.229	-58.845	-59.690	-61.907	-56.039
-64.373	-61.501	-58.647	-58.713	-65.607
-66.606	-58.591	-42.524	-9.5318	.00000
-2.2492	-17.950	-59.873	-61.833	-60.238
-57.874	-63.173	-60.048	-60.030	-67.484
-57.550	-61.285	-69.570	-57.503	-70.330
-69.135	-62.257			

NPTS= 64, HARMONIC= 15.40, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 8

PEAK RESPONSE= - -7.3852

-60.155	-58.366	-60.156	-59.713	-55.449
-62.884	-60.107	-57.090	-56.346	-60.611
-60.301	-61.053	-51.038	-10.916	.00000
-1.1202	-15.112	-59.290	-66.036	-61.523
-57.887	-62.295	-58.522	-58.211	-62.720
-55.876	-58.734	-66.002	-55.069	-64.106
-64.505	-59.925			

NPTS= 64, HARMONIC= 15.50, PHASE= 30.00, SLDB= 60.00, 3-DB BW= 1.463
NBITS= 8

PEAK RESPONSE= - -7.8854

-59.862	-58.280	-61.694	-58.514	-55.415
-62.681	-59.457	-56.241	-54.847	-57.736
-56.710	-65.775	-77.584	-12.388	-.29364E-02

.00000	-12.414	-63.026	-68.994	-64.574
-58.916	-62.515	-57.731	-57.253	-60.046
-54.801	-57.227	-64.052	-53.338	-60.784
-61.806	-58.560			

Table 3.5.2-7: APUP transform results with 63dB Dolph-Tchebychev weighting and various quantizations.

APUP563DB1.LP 8/15/79 20:32:19 CREATED 8/3/1979 11:3:00

This file is a series of runs of APUP5 for a 63-db weighting function. The signal frequency is held constant at the 15th harmonic, and the number of bits of quantization is varied.

NPPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 6

PEAK RESPONSE= - -6.7099

-60.141	-62.545	-52.463	-63.744	-59.463
-60.018	-47.735	-55.138	-55.836	-58.916
-52.723	-65.280	-25.685	-5.4770	.00000
-5.4602	-25.746	-59.452	-49.987	-62.308
-55.052	-50.712	-61.881	-54.515	-61.321
-56.948	-56.956	-62.373	-57.177	-52.424
-61.748	-62.445			

NPPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 7

PEAK RESPONSE= - -6.7096

-63.912	-64.373	-71.510	-62.753	-61.825
-61.286	-58.139	-59.474	-69.069	-58.790
-57.743	-57.392	-25.860	-5.4746	.00000
-5.4600	-26.013	-57.125	-60.482	-62.999
-63.213	-67.447	-58.000	-58.531	-62.116
-59.304	-70.565	-61.573	-57.024	-57.521
-71.838	-61.617			

NPPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 8

PEAK RESPONSE= - -6.7097

-67.442	-66.218	-62.746	-73.641	-65.114
-69.102	-73.350	-67.569	-65.935	-64.268
-60.453	-67.395	-25.883	-5.4643	.00000
-5.4650	-25.959	-66.457	-59.257	-58.793
-65.967	-72.377	-62.757	-70.209	-76.970
-76.111	-79.987	-70.511	-72.043	-64.994
-62.048	-84.385			

NPPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 9

PEAK RESPONSE= - -6.7080

-69.690	-70.962	-76.942	-68.820	-74.178
-75.892	-86.817	-68.383	-66.159	-65.846
-70.002	-85.548	-25.925	-5.4672	.00000
-5.4718	-25.858	-72.027	-62.442	-69.620
-74.792	-65.816	-75.880	-73.405	-70.071
-74.142	-71.596	-71.189	-73.066	-68.298
-71.764	-77.450			

NPPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 10

PEAK RESPONSE= - -6.7085

-75.038	-73.720	-77.602	-73.709	-69.841
-75.140	-93.742	-73.039	-70.397	-68.142
-62.190	-91.782	-25.847	-5.4711	.00000
-5.4720	-25.870	-80.521	-64.256	-65.089
-72.184	-73.781	-85.161	-90.568	-76.316
-74.402	-81.839	-70.304	-71.160	-72.536
-72.179	-74.966			

Table 3.5.2-8: APUP transform results with 63dB Dolph-Tchebychev weighting, 7 bit quantization, and signal stepped through Doppler Channel.

APUP563DB2.LP 8/15/79 20:32:25 CREATED 8/ 3/1979 11:24:00

This file is a series of runs of APUP5 for a 63-dB weighting function. The number of bits of quantization is held constant at 7 bits (plus sign), but the frequency of the signal is varied from the 15th to the 15.5th harmonic.

NPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 7

PEAK RESPONSE= - -6.7096

-63.912	-64.373	-71.510	-62.753	-61.825
-61.286	-58.139	-59.474	-69.069	-58.790
-57.763	-57.392	-25.860	-5.4744	.00000
-5.4600	-26.013	-57.125	-60.437	-62.999
-63.213	-67.447	-58.000	-58.531	-62.116
-59.304	-70.567	-61.573	-57.024	-57.521
-71.838	-61.617			

NPTS= 64, HARMONIC= 15.10, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 7

PEAK RESPONSE= - -6.7621

-63.317	-69.089	-65.063	-60.801	-64.920
-59.597	-59.975	-56.973	-70.442	-59.714
-58.338	-58.095	-29.372	-6.6310	.00000
-4.3359	-22.754	-50.240	-60.817	-62.965
-59.761	-67.486	-58.189	-58.376	-60.195
-61.336	-68.975	-62.156	-57.323	-57.392
-66.742	-63.350			

NPTS= 64, HARMONIC= 15.20, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 7

PEAK RESPONSE= - -6.9198

-62.096	-80.488	-61.095	-59.425	-64.455
-58.156	-32.009	-55.247	-70.905	-60.389
-59.841	-58.510	-33.311	-7.8252	.00000
-3.2344	-19.752	-58.152	-61.908	-62.280
-57.753	-67.816	-58.148	-57.843	-58.712
-62.766	-66.543	-62.589	-58.003	-57.378
-62.588	-65.847			

NPTS= 64, HARMONIC= 15.30, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 7

PEAK RESPONSE= - -7.1836

-60.930	-76.094	-58.518	-58.399	-61.524
-57.112	-63.598	-54.073	-69.602	-60.205
-62.472	-59.233	-37.862	-9.0260	.00000
-2.1492	-16.945	-58.440	-63.596	-61.604
-56.620	-68.247	-58.001	-57.226	-57.664
-61.499	-64.861	-62.674	-59.147	-57.546
-60.069	-69.599			

NPTS= 64, HARMONIC= 15.40, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 7

PEAK RESPONSE= - -7.5546

-60.129	-68.321	-56.729	-57.784	-59.048
-56.495	-63.776	-53.334	-67.690	-59.014
-66.850	-60.775	-43.370	-10.364	.00000
-1.0744	-14.289	-60.140	-63.433	-61.219
-56.150	-67.924	-57.922	-56.752	-57.035
-60.083	-64.104	-62.424	-60.961	-57.966
-58.569	-76.231			

NPTS= 64, HARMONIC= 15.50, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 7

PEAK RESPONSE= - -8.0348

-59.785	-64.811	-55.465	-57.567	-57.361
-56.361	-62.852	-53.028	-66.171	-57.359

-72.393	-63.695	-50.577	-11.733	.00000
-45338E-02	-11.750	-52.093	-60.557	-61.048
-56.789	-65.971	-58.007	-56.656	-56.809
-58.931	-64.374	-62.049	-63.948	-58.757
-57.748	-124.02			

Table 3.5.2-9: APUP transform results with 63dB Dolph-Tchebychev weighting
8-bit quantization, and signal stepped through Doppler Channel.

APUP563DB3.LP 8/15/79 20:32:30 CREATED 8/ 3/1979 11:44:00

This file is a series of runs of APUP5 for a 63-dB weighting function. The number of bits of quantization is held constant at 8 bits, but the signal frequency is varied from the 15th to the 15.5th harmonic.

NPTS= 64, HARMONIC= 15.00, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 8

PEAK RESPONSE= - -6.7097
-67.442 -66.218 -62.746 -73.641 -65.114
-69.102 -73.350 -67.569 -65.933 -64.268
-60.453 -67.395 -25.883 -5.4643 00000
-5.4650 -25.959 -66.457 -59.237 -58.793
-65.967 -72.377 -62.757 -70.209 -76.970
-76.111 -79.987 -70.511 -72.043 -64.994
-62.048 -84.385

NPTS= 64, HARMONIC= 15.10, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 8

PEAK RESPONSE= - -6.7620
-64.836 -65.757 -61.257 -67.874 -62.995
-73.501 -84.957 -64.755 -69.530 -65.071
-69.794 -64.668 -29.470 -6.6204 00000
-4.3789 -22.710 -65.501 -59.772 -58.129
-63.946 -80.922 -63.091 -64.843 -74.693
-79.278 -73.102 -76.908 -66.383 -67.647
-64.202 -77.774

NPTS= 64, HARMONIC= 15.20, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 8

PEAK RESPONSE= - -6.9194
-63.055 -65.535 -60.108 -64.280 -61.425
-68.026 -73.678 -62.643 -69.739 -66.217
-62.133 -62.826 -33.557 -7.8143 00000
-3.2359 -19.718 -62.312 -61.070 -58.104
-62.703 -78.480 -62.867 -61.754 -69.290
-69.455 -68.009 -72.333 -62.450 -67.111
-67.156 -69.735

NPTS= 64, HARMONIC= 15.30, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 8

PEAK RESPONSE= - -7.1827
-61.073 -65.672 -59.361 -62.079 -60.315
-64.540 -68.476 -61.166 -65.682 -67.043
-64.550 -62.836 -38.420 -9.0546 00000
-2.1496 -16.919 -62.311 -63.176 -58.778
-62.128 -73.195 -62.521 -69.741 -65.798
-65.418 -64.858 -67.325 -59.930 -63.810
-71.082 -65.688

NPTS= 64, HARMONIC= 15.40, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 8

PEAK RESPONSE= - -7.5531
-61.181 -66.181 -59.056 -60.808 -59.604
-61.882 -65.844 -60.268 -62.293 -66.687
-67.955 -64.777 -44.680 -10.352 00000
-1.0743 -14.270 -64.650 -64.817 -60.420
-62.172 -71.057 -62.437 -58.447 -63.530
-63.252 -62.770 -64.439 -58.247 -60.782
-74.992 -63.112

NPTS= 64, HARMONIC= 15.50, PHASE= 30.00, SLDB= 63.00, 3-DB BW= 1.496
NBITS= 8

PEAK RESPONSE= - -6.0325
-60.924 -66.719 -59.274 -60.274 -59.253
-60.282 -64.410 -59.962 -59.954 -65.382
-68.916 -68.927 -54.450 -11.750 00000

- 41838E-02 -11.737 -51.844 -63.807 -63.715
-63.807 -70.961 -62.911 -57.737 -62.069
-63.160 -61.398 -62.792 -57.239 -58.516
-74.560 -61.469

to these data to compensate for the normalization to the smaller response at the band edge, then it will be seen that only two filters have a response as high as -58 dB, and only a total of three filters lie at all over the -60 dB goal.

The last of the series of computer simulations is summarized in table 3.5.2-10. These data were obtained by adding one bit of pseudorandom, uniformly distributed white noise to the weighted reference functions before quantizing. The purpose of this experiment was to find whether the addition of the noise would reduce any periodicity generated in the quantization process, thus eliminating peaks in the sidelobe structure. Of course, it was expected that the price paid for this reduction in periodicity would be a small increase in the general sidelobe level.

The data of table 3.5.2-10 should be compared with the data of table 3.5.2-4 which was made for the same experimental setup without the addition of noise. A visual comparison of the data shows no startling improvements with the addition of the noise. While the far sidelobes are different with some filling in of the nulls and some reduction of peaks, in general the overall rise in noise level and the occasional appearance of new sidelobe peaks indicate that the noise addition is not a useful technique in this particular situation.

Table 3.5.2-10: APUP transform with one LSB pseudorandom, uniformly distributed white noise added to weighted reference function before quantizing.

APUP360.LP 8/20/79 11:36:50 CREATED 8/20/1979 11:36:00

APUP3, CORRELATION TRANSFORM WITH NOISE ADDED TO WTD REF FN.
 This file is a series of runs of APUP3, a convolution transform with one bit of uniformly distributed random noise added to the weighted reference functions before quantizing.

NBITS: 64, HARMONIC=15
 NBITS: 6

PEAK RESPONSE= -6.496
 -60.510 -60.439 -48.797 -65.309 -53.174
 -57.835 -51.813 -65.112 -54.173 -60.629
 -50.315 -56.365 -27.668 -5.7090 .00000
 -5.7450 -28.100 -61.783 -58.839 -47.452
 -50.763 -53.895 -50.653 -51.277 -52.279
 -50.140 -48.347 -55.001 -47.611 -59.401
 -56.300 -54.179

NBITS: 64, HARMONIC=15
 NBITS: 7

PEAK RESPONSE= -6.499
 -57.075 -63.994 -59.660 -59.601 -59.399
 -62.919 -37.766 -62.619 -59.024 -58.781
 -51.769 -53.552 -27.858 -5.7443 .00000
 -5.7098 -27.942 -74.418 -50.963 -56.627
 -58.781 -65.190 -67.067 -67.158 -64.405
 -60.372 -63.623 -55.845 -53.624 -67.424
 -67.083 -64.054

NBITS: 64, HARMONIC=15
 NBITS: 8

PEAK RESPONSE= -6.493
 -67.830 -59.773 -59.690 -73.428 -67.439
 -64.426 -74.923 -62.939 -62.020 -60.214
 -62.073 -65.529 -27.713 -5.7436 .00000
 -5.7422 -27.689 -61.567 -59.980 -66.544
 -61.222 -62.805 -71.576 -62.111 -68.322
 -77.555 -70.639 -67.406 -57.669 -63.421
 -71.756 -67.510

NBITS: 64, HARMONIC=15
 NBITS: 9

PEAK RESPONSE= -6.499
 -64.361 -65.748 -70.428 -71.336 -67.607
 -68.761 -78.897 -66.389 -68.952 -60.143
 -58.533 -69.037 -27.884 -5.7363 .00000
 -5.7386 -27.827 -57.964 -58.270 -62.182
 -63.895 -66.714 -69.591 -71.141 -69.381
 -74.783 -68.821 -69.757 -78.145 -66.835
 -74.728 -65.775

NBITS: 64, HARMONIC=15
 NBITS: 10

PEAK RESPONSE= -6.496
 -66.553 -66.937 -65.405 -67.957 -69.537
 -69.307 -68.873 -68.618 -71.410 -64.243
 -60.039 -65.987 -27.829 -5.7402 .00000
 -5.7408 -27.820 -67.703 -61.201 -63.474
 -60.215 -75.649 -74.820 -72.924 -65.916
 -65.448 -65.909 -67.719 -65.986 -65.991
 -67.301 -70.794

3.5.3 Traditional "Corner Turning" Accomplished Directly in APUP Serial Memory

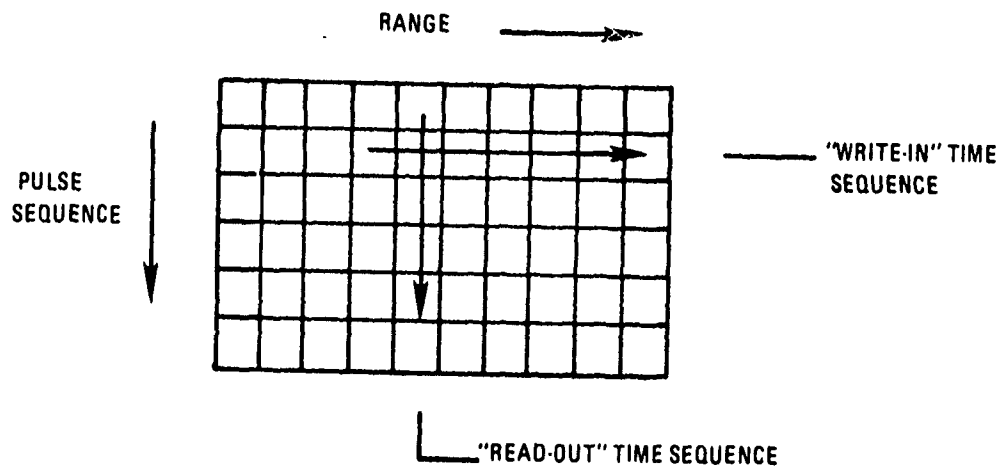
The classical range/Doppler Analyzer stores range gate samples linearly along one axis of a large memory, accumulating sets of samples for each PRI in a batch (or "dwell"). These are ordered as sketched in Figure 3.5.3-1. During analysis, the "read-out" is done crossways with all the samples of one range cell read out in pulse sequence, then all the samples of the next range cell, etc.

The APUP can store these samples linearly and read them out the same way, only at a different clock rate. For, say, an 8 Doppler bin analysis, one range sample is stored, then the clock races ahead 8 shifts before the next range sample is stored, etc. This gapped storage continues for the designed range bin count, then the clock is "slipped" (stopped for one advance time). When the return samples for the next transmitted pulse are stored, they will land one cell ahead of the others all along the CCD storage chain. After 8 such "offset" storings of range data, the APUP memory is loaded and ready to be read out for Doppler analysis. The ordered memory contents are sketched in Figure 3.5.3-2.

The clock rate may be slowed during read out. The samples for all pulses of each range gate emerge in sequence for that range gate, immediately available for multiplication by the Doppler reference function(s) and integration. Analysis is thus accomplished after the last RF pulse without any data re-orientation.

If I & Q samples are taken, these also can be handled by APUP using the same immediately-sequential technique. Figure 3.5.3-3 illustrates this I & Q method applied to the cornerless pulse Doppler analysis problem for approach/recede differentiation. The I and Q channels are sampled simultaneously but stored sequentially in adjacent cells.

While the foregoing discussion presented the APUP operation in a fast-store slow-readout mode with Doppler analysis performed



80-0132-V-29

FIGURE 3.5.3-1: Classic Pulse Doppler Memory Organization

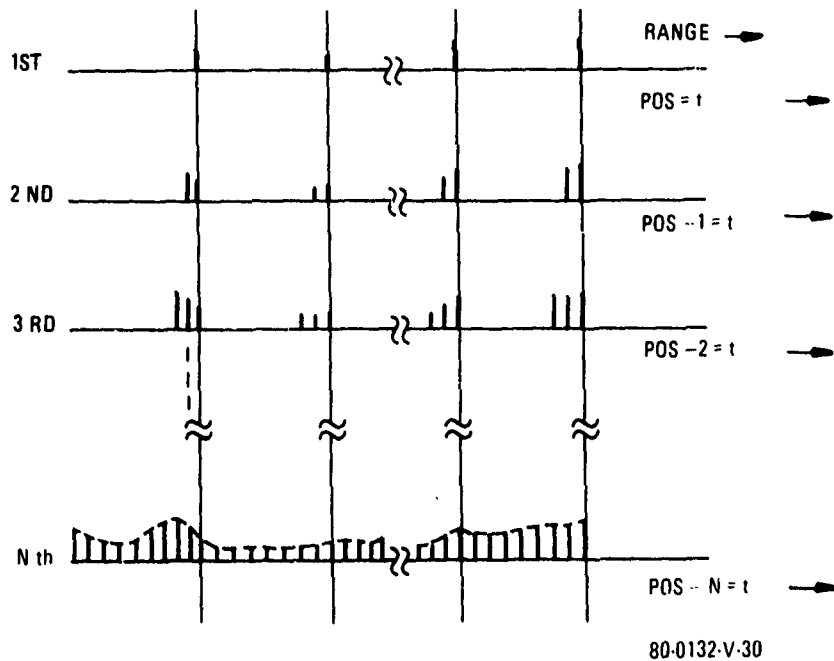


FIGURE 3.5.3-2: "Corner-Turn" Timing Waveforms

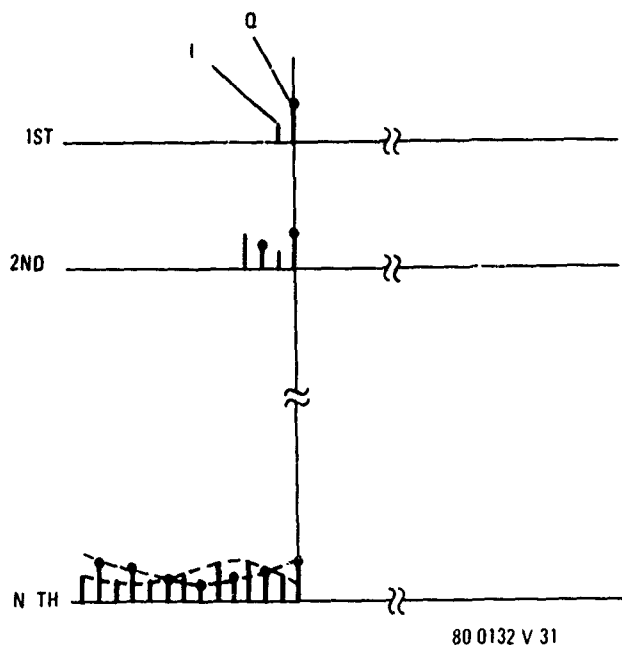


FIGURE 3.5.3-3: I and Q Waveforms

after the batch is completed, the analysis may indeed proceed as part of the storage process. The choice depends upon the MDAC speed relative to the range sampling rate and the number of Dopplers required. If there were no MDAC speed problem, the Doppler reference pre-multiplies could be done during data taking, i.e., instead of racing the CCD clock to space out the range samples in one sweep, then "slipping" it to offset the sweeps in the batch, each range sample could be pre-multiplied by all Doppler reference functions in turn, the appropriate partial result being read out from the memory and summed with each new product, then the new sum stored again until the next sweep. In this way the APUP memory acts as a multicell integrator in the transform configuration rather than as a raw data storage device, and the answers are complete at the end of the batch.

Since it appears unlikely that one APUP could compute rapidly enough to accomplish the above, some split between speed and hardware is needed. The worst case for this Doppler transform mode would be using one APUP per Doppler. On the other hand if N range cells and k Doppler bins are required and one APUP can handle m Dopplers per range cell interval, the hardware implementation would require k/m APUPs, each with mN storage locations, in order to complete the analysis within the batch time.

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4. SURVEY OF CTD-RELATED ANALOG SIGNAL PROCESSING TECHNIQUES

A comprehensive treatment of this subject could easily fill a book as it has at least twice in the past ^(1,2). These textbooks are periodically updated with invited survey papers ⁽³⁾ and the proceedings of related technical conferences such as the International Conferences on the Applications of CCD's. Publications of attractive device developments also occur regularly in other journals and proceedings. Since all these publications are available in the public domain, the device survey will be presented as follows. Device technical details are included (where needed) in the comparison description and specification of the selected APUP device in sections 6 and 7. In Table 4-1, are given only the salient features of any particular development, keyed to a cross-reference number which is the counting index number for the list of device references in Table 4-2. The device references, in turn, are listed in chronological order from the newest to the oldest, with the textbooks and an illustrative survey paper first.

Table 4-1: Highlights of Important Device Developments Related to any CTD-Based APUP.

<u>Item</u>	<u>Table 4-2 Reference Numbers</u>
I. Processor Basic Building Blocks	
A. Line Arrays	
1. Mask-programmable transversal operators:	
a.) Single-split-electrode 63dB peak Fourier output above output noise; 46dB sidelobe rejection at 800KHz (reduced performance at 1.5MHz); 10-bit MDAC; 475 mW at 1 MHz (500 taps)	68
55 dB above thermal noise but only 26 dB above clock fixed pattern feedthrough; 8- bit MDAC (32 taps)	88
b.) Double-split-electrodes 86 dB signal to noise ratio; 40 dB stopband rejection; -50 dB harmonic distortion at 32 KHz sample rate (71 taps)	71
c.) Displacement charge subtraction 78-dB signal-to-noise ratio, -44 dB harmonic distortion at 20 KHz (62 taps)	111
d.) Analog/analog serial batch premultiply	120
2. Electrically programmable "split-electrode" transversal filters 35-dB Signal-to-noise ratio, -42 dB harmonic dis- tortion at 100 KHz; weighting via resistive poly gates; (8 taps)	36
3. Parallel-input analog multiplexers OR premultiply-delay- and-add transversal operators.	
a.) 68-dB dynamic range with -34 dB harmonic dis- tortion and 13-MHz 3-dB signal bandwidth	

	clocked at 50 MHz. (12 taps)	51
b.)	100-dB dynamic range and distortion re- jection at 143 KHz. (16 taps, 212 ⁰ F) 64 taps also available.	102
B. Area Arrays		
1.	Analog/analog (2-D) matrix transforms	
a.)	A 16 X 16 matrix multiplier has been per- sonalized to perform a 16-point Walsh- Hadamard, 8-point discrete cosine, and 8-point complex discrete Fourier transforms	19
b.)	A 3 X 3 matrix multiplier has been per- sonalized to perform Sobel edge detection, local averaging, unsharp masking, and binarization at up to 4 MHz.	95
2.	Analog Corner-Turn Arrays	
a.)	A 32 X 32 with 43-dB peak signal to rms fixed pattern at room temperature and 1-MHz sample rate	13, 99, 100
b.)	A 33 X 66 yielded better than 40 dB dynamic range clocked at 12.5 MHz	100
c.)	A 16 X 128 with 3-level clock to hold column data gave about 40-dB dynamic range at 1-MHz clock	101
II. High-order CCD Analog Signal Processors		
A.	Serial-in/Parallel-out (SI/PO) Analog-binary operators.	
1.	NMOS, 127 taps, 2 MHz, -40 dB harmonic distortion, 34-dB dynamic range	33
2.	512 taps, 10-MHz CCD clock, 34-dB dynamic range, -40 dB harmonic distortion, power= 2.1 watts	34, 67

3.	C ² L/CMOS/NCCD, 128 stages, 50 MHz, power exceeds 0.75 watt	40
4.	NMOS; dynamic range is 56 dB at 8 MHz, 60 dB at 4 MHz, -34 dB harmonic dis- tortion	97
B.	Rotating-tap CCMDAC Arrays	119, 37
C.	SI/PO Analog-analog operators	
1.	Electrically programmable split- electrodes	36
2.	64 taps, 34 dB dynamic range impulse response, -34 dB average stop band rejection, multiplier accuracy about 2%	98, 35
D.	Parallel-in/Serial-out (PI/SO) Programmable Operators	
1.	16 taps, 9-bit CCMDAC, BBD with auxiliary stage capacitors for longer data retention	29
2.	(32 tap/1 bit) and (16 tap/4 bit) up to 10 MHz, 50 dB dynamic range, -40 dB harmonic distortion	31
3.	32 tap, analog "pentode difference of squares" multiplier (demonstrated up to 100 MHz), readout up to 20 MHz, 60 dB dynamic range, -35 dB harmonic distortion	32
E.	Adaptive analog transversal operators	
1.	SI/PO CCD plus parallel update	73
2.	Rotating tap, serial update	37, 74
3.	SI/PO CCD, serial update	50

III. Related Signal Processing Elements

A.	Charge-coupled Multiplying Digital-to-Analog Converters (CCMDAC)	
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1. Basic Concepts	4, 86, 121, 122, 162, 163
2. CCMDAC arrays	68, 88, 119
B. Buffer Amplifiers	14, 15, 16, 17, 80, 81 82, 84
C. Switched Capacitor Operators	10, 11, 12, 38, 47, 86
D. Misc. Support Circuitry	89
 IV. Device Characteristics and Techniques	
A. Linearity, Harmonic Distortion	21, 153, 161, 165
B. Sample-to-Sample Crosstalk	66, 147, 148
C. Device Temporal Noise	146, 167.

Table 4-2: Device Survey References

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5. CROSS-CORRELATION OF RADAR AND DEVICE TECHNOLOGY SURVEYS LEADS TO APUP CANDIDATE ARCHITECTURE.

5.1 Partitioning Guidelines

The cross-correlation of the survey results leads to several APUP candidates. This cross-correlation is, ideally, an objective effort requiring a broad knowledge of all disciplines from device technology to signal processing system design. The optimal distribution of signal processing functions among the individual members of an APUP family of candidates depends not only on the details of the appropriate device technologies but also on the overall mix of signal processing system applications. Often the objectives of improved system reliability and lower system power cost lead to the design goal of a reduced part count. But lower hardware costs must not be overemphasized to the point where associated software or programming costs become extraordinarily high.

A closer look at most analog signal processing devices quickly reveals that many of the complicated software instruction sets needed for such processes as Doppler filtering, MTI/clutter cancellation, CFAR, etc. are greatly reduced because the analog constituents are predominately dedicated processing elements capable of only executing such unique operations as multiply, add, subtract, memory, etc. The software instruction set is therefore transformed into a single "configuration command" word which specifies how the available analog constituents are interconnected to accomplish the desired function. Indeed, because of this very characteristic, the relationship between the APUP candidates and the system controller or host computer is essentially the same as the relationship between a subservient peripheral (like a USART) and the host computer, except reconfiguration may not occur

as frequently for an APUP as for a USART or other peripherals. Because an APUP is continually executing a complex signal processing function in its entirety; there is no need (as with a conventional digital microprocessor) to reconfigure between each different constituent operation (e.g., as from "multiply", to "add", to "store", etc.) wherein the same digital logic elements are used differently for each different constituent operation. The elementary or "fine-grained" interconnectability used in a digital microprocessor is easier than for the APUP because the typical digital "saturating" logic circuits provide more generous "zero" versus "one" level discrimination margins for interconnect nodes than are associated with 60-dB analog performance circuits.

Next, by examining the design of standard chip families, it is possible to consider that some systems could be constructed from only a few basic building blocks (such as R, L, C, and gain) used many times as was done in the bygone days of all analog circuitry before the early days of digital technology. Conversely, it may be possible someday to build some systems with only one very big integrated circuit chip. A feasibility study at Westinghouse using 6000-gate array VLSI circuits indicated that the total circuit integration of the digital system for an airborne radar including computer, signal processor, bulk memory, and bus interfaces could be accomplished with 17 chip types in addition to the memory. Another study at Westinghouse examined the marginal savings realized by the extent of the VLSI effort. The first circuits selected for integration in the system will have the most significant impact upon the reduction of parts. The second integration selected will realize less saving and finally the last circuits selected for integration will have the least impact of total savings. Figure 5.1-1 summarizes the conclusion of this study, showing the diminishing rate of savings with order of chip selection.

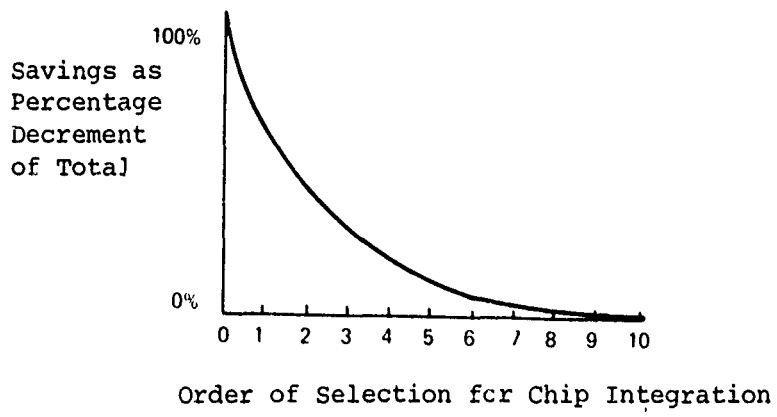
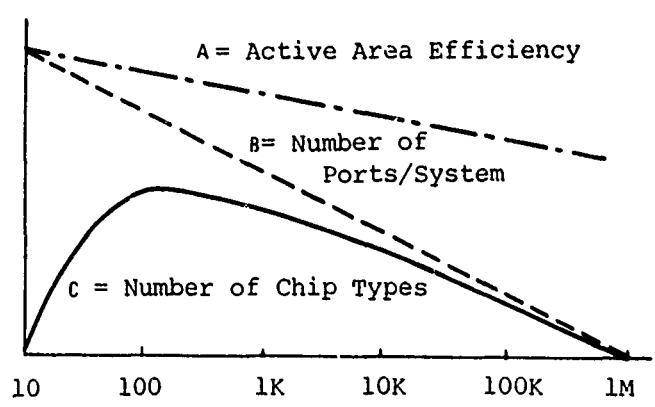


Figure 5.1-1: Reduction vs Order of Selection



"Equivalent Gates"/Chip as a Measure of Functional Capability

Figure 5.1-2: Chip Size Factors

A second model being evaluated but not proven is shown in Figure 5.1-2. This model shows the expected relationship between the number of equivalent gates (or a measure of functional capability) per chip, and the number of chip types, the number of packages, and the efficiency. The graph is not presented for costing estimates; rather it is shown to describe the relationships required for understanding partitioning effects.

Curve A shows that as the number of functions on a chip increases, chip area will be used less efficiently. Efficiency is a measure of the signal processing active area divided by total available chip area in the system. Presently it is expected that this will not be a major constraint as the cost of incremental inactive area may be negligible compared to design costs. More important is the probability that the larger the APUP chip, the more special and unique are its functions, therefore decreasing the possibility of use on other systems.

Curve B shows the reduction in total parts. Life cost and acquisition cost models show that these costs are directly related to parts counts. Reliability models also project that with the larger chips the reliability per gate will be significantly increased. Overall, it can be concluded that increasing the total capability per chip is a partitioning goal for meeting life-cycle cost objectives.

Curve C shows the relationship between the size of the

APUP chips and the numbers of chip types which will be required to totally implement a typical system.

5.2 Application of Partitioning Guidelines

The general guidelines given above are now used to partition the many radar signal processing functions into natural groupings. Most of the important signal processes in radars such as pulse compression, filtering, and CFAR involve algebraic multiplication and summing and so do not provide a natural partitioning of functions. Examination of the associated data storage and the clustering of data samples for the various processes does indeed reveal a very well defined partitioning of the processes into three distinct regions, as indicated across the top of Figure 5.2-1. The boundaries between the regions are specified in terms of both the data storage time needed and whether the individual samples within a set of analog data to be transformed occur naturally serially (each one after the other) or are separated in time by an interval like an interpulse period (IPP) or a full antenna scan time.

Most radar signal processors must be concerned with processing data in range and azimuth. A typical pulse repetition period is often on the order of one millisecond while the dwell time for a radar beam upon a target may be in the tens of milliseconds. Storing data for periods shorter than 1 msec is generally associated with processing in range, such as pulse compression and "fast time constant" (FTC) threshold adjustment to achieve a constant false alarm rate (CFAR). Furthermore, all these functions transform adjacent serial data. Many cases occur where existing charge transfer devices are able to perform such functions but are unable to operate fast enough to match the radar resolution specified by the master range clock.

Often, time intervals of tens of milliseconds are needed to collect data for such azimuth processing as MTI or Doppler filters, but for CTD analog signal processors at MIL SPEC

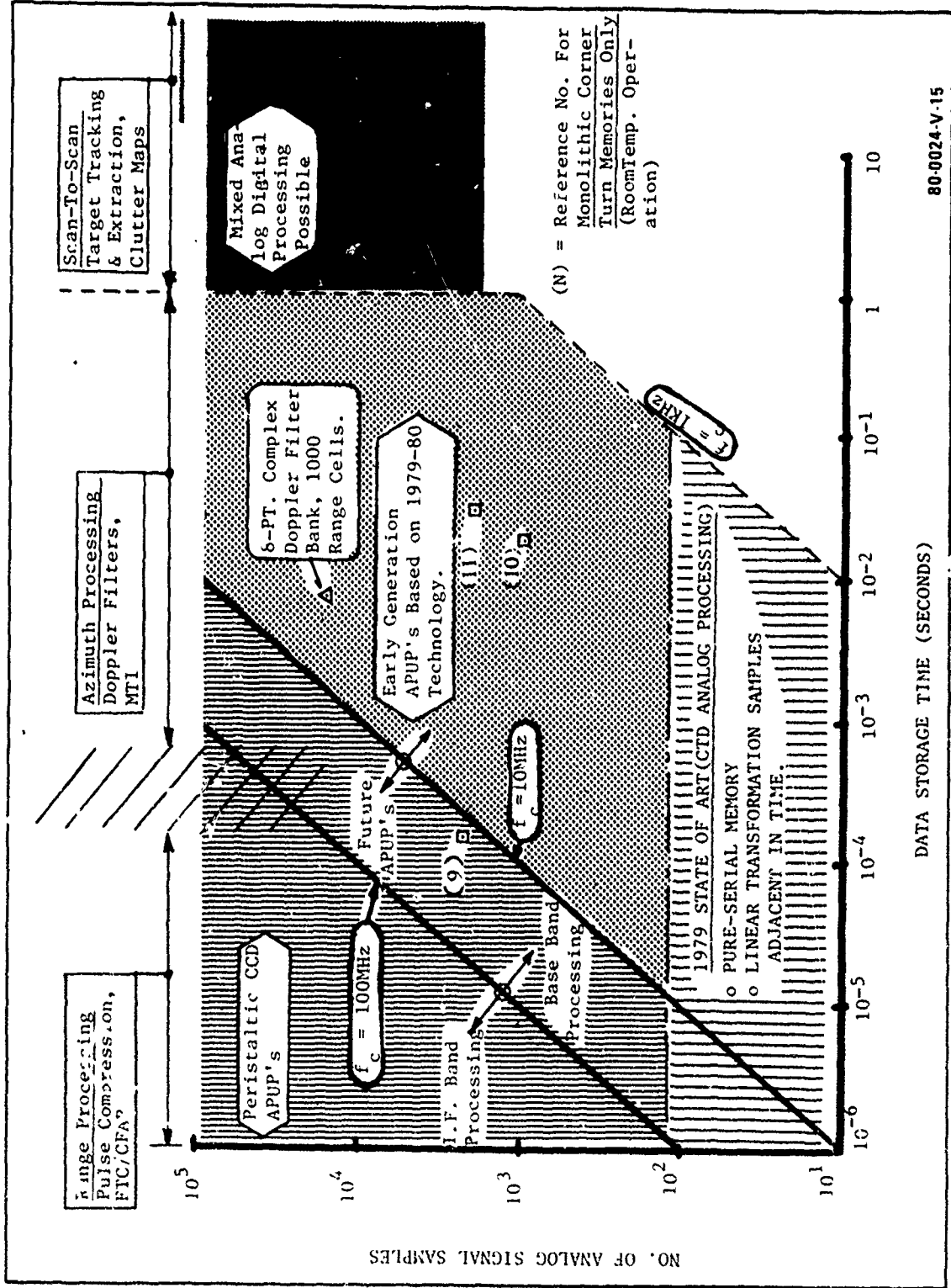


Figure 5.2-1 Military Radar CCD-Based Analog Signal Processing

ambient temperature, data retention times of tens of milliseconds can be extremely difficult to achieve. In azimuth processing of this sort, the data samples used in the transformation are no longer adjacent in time, but separated by an IPP. Thus, the many existing line-array, CTD, transform operators can not be used for this purpose with the data in its natural format. Reordering the data into an orthogonal format by means of a corner-turn array, however, puts all the data needed for an azimuth transformation into the needed adjacent serial relationship. But guaranteeing the desired minimal corruption of the data during the orthogonal reordering places very severe demands on the corner-turn array, particularly its blemishes and other nonuniformities, since all data samples for any processing batch do not travel identical/differential paths through the memory in any corner-turn array published to date. Additional azimuth processing for which transversal linear transformations are suitable include moving-window averaging for the purpose of detection and post-detection non-coherent "M out of N" correlation to remove Doppler blind spots by using multiple PRF's

Another new potential application area is adaptive radar signal processing, described briefly in section 3.4.4, where the functional chips are likely to be operating at data rates and retention times similar to those of azimuth/Doppler processing. The resultant optimized notch filters, however, may be stored by means of their weighting coefficients in memory associated with the scan-to-scan processor so as to facilitate recalling and updating such notch rejection filters which may be applied against jammers in certain quadrants.

CTD based analog signal processing devices typical of the state of the art in 1979/'80 are covered by the region delineated in the lower left of the figure 5.2-1. Operation at MIL-SPEC temperatures would normally limit data storage times to about a millisecond before excessive corruption of the data occurs. Only by means of uniform clocking through identical paths, in

the conventional architecture of 1979, can the longer data storage times as shown for that region be achieved. The second region to the far right of the figure involves the processing of scan-to-scan target tracking, processing best done by digital devices having no degradation with long storage times.

The remainder of the chart, for the most part, is not covered by any existing or proposed large-scale integrated analog programmable processor. The exceptions are a few monolithic corner turn memories as indicated in (9, 10, 11). A large, hybrid azimuth processor yielding an eight-point complex Doppler filter bank for one thousand range cells is currently being built (12) to investigate a slightly different architecture for APUP.

In that broad region of CCD-based military radar analog signal processing not yet addressed by commercial devices, early generation APUP devices are shown covering data rates below 10^7 transformation points per second with the limitation being the MDAC multiplier. Peristaltic CCD's for 400 MHz operations are currently in development (13) for fast-write/slow-read buffer operation with complete high-speed operation under parallel investigation (14). Thus any preferred APUP architecture using today's CCD/MOS/Bipolar technology, appears valid not only for most of the "baseband" processing region but also for "IF-band" processing via future generation APUP's based on PCCD/Bipolar technology currently being developed.

All the above observations may now be combined to form a list of candidate architectures which are ordered or ranked as follows: In accordance with the concept of figure 5.1-1, the highest ranking is given the signal processing task associated with the greatest volume of computations in a radar signal processor and most often, too, with the greatest quantity of parts or devices currently required for that general task. The next criterion used to partition the many types of signal processing functions performed is the sampled data format. Are the analog samples naturally serial or adjacent in time or

can they be rearranged to be so? Final consideration must then be given to special functions which are now considered not practical by system designers who are constrained to parts currently available off the shelf but which are indeed undergoing early investigation and development.

Table 5.2-1 lists the major APUP candidates ranked according to the amount of signal processing which they normally perform. From the (radar) signal processing survey, clearly the largest amount of computations and/or computational equipments are dedicated to such azimuth processing as MTI or Doppler filtering where the data samples used in the needed transformation are not naturally serial or adjacent in time but separated in time by the interpulse period. Involving a substantially lower burden of the computations are linear transformations involving serial analog samples such as pulse compression, CFAR, centroiding, acoustic beam forming, and transversal filtering and correlation. Next in overall computational population come the buffer memories which simply reformat the data samples, dominated by the "fast write/slow read" (or bandwidth compression) "double-buffer" type with the more complex "corner-turn memory" as a distant runner-up. Finally, in radar signal processing, an iterative adaptive linear transversal transformation would easily fall into the category of a special-purpose peripheral support function were it not for such a strong dependence on such a function for so many communications applications. Naturally the last category is the special-purpose peripheral support function. Included in the special-purpose category are: acousto-optic image pre-processors (as for spectral analysis) and the FLIR deinterlacer/synchronizers.

TABLE 5.2-1: THE MAJOR APUP CANDIDATES

<u>DATA FUNCTION/FORMAT</u>	<u>ITEM</u>	<u>RANKING BY SIGNAL PROCESSING QUANTITY.</u>
1. LINEAR TRANSFORMATION OF PERIODIC (IPP), NOT SERIAL, SAMPLES	AZIMUTH CORRELATION: MTI, DOPPLER FILTERS (a) general purpose transform/filter architecture (b) corner-turn memory PLUS linear trans- formation of serial data	1
2. LINEAR TRANSFORMATION OF SERIAL DATA SAMPLES	RANGE CORRELATION (PULSE COMPRESSION), CFAR, CENTROIDING, INTERPOLATION	2
3. ANALOG BUFFER MEMORIES	(a) UP TO 1GHZ "FAST WRITE/SLOW READ" BANDWIDTH COMPRESSION, DOUBLE-BUFFERING (b) LONG STORAGE TIME CORNER-TURN ARRAYS.	3
4. ADAPTIVE LINEAR TRANSVERSAL TRANSFORMATION	ADAPTIVE CLUTTER REJECTION FILTERS, ECM- JAMMING REJECTION NOTCH FILTERS, ANTENNA SIDELOBE REJECTION	4
5. SPECIAL PURPOSE FUNCTIONS:	(a) ACOUSTO-OPTIC IMAGE PREPROCESSOR AS FOR SPECTRAL ANALYSIS (b) FLIR deinterlacer/synchronizer	5

5.3 DESCRIPTION OF THE MAJOR APUP CANDIDATES

As was the partitioning and ranking of the major APUP candidates quite clear from the signal processing survey and from some familiarity with the related architectures, so also are the important details of most APUP candidates from the relevant CTD survey. Indeed, with the exception of THE MOST ATTRACTIVE APUP candidate (1-a) and the second special purpose function (5-b), all others are either commercially available or are experiencing substantial funding for development, as indicated in table 5.3-1. Since the choice of the one APUP most attractive for further development is a requirement of the study contract, the data referred to in table 5.3-1 obviously dictate a unique selection. A decision for the highest ranking candidate which features azimuth correlation over extended times for large numbers of samples leads naturally to the secondary question of detailed architecture: How does the monolithic transform/filter candidate, as illustrated in figures 7.6-1 and 7.6-2 compare with the multichip hybrid approach using corner-turn arrays to feed line-array transversal operators. The programmable line-array transversal transformations (item 2 of table 5.3-1) have already been aggressively developed to include large numbers of taps, high speed and integrated support circuitry. Meanwhile, even though the analog corner-turn arrays have been developed as indicated in the size range of 1K to 2K storage sites, ROOM TEMPERATURE characterization gave dynamic range results of only 36 dB to 40 dB associated primarily with non-uniformity fixed patterns which become exponentially worse at the higher MIL-SPEC temperatures. The simpler embodiments of the corner-turn array using three-level clocks addressed to selected columns virtually eliminates such standard techniques as correlated double sampling (CDS) (or push-pull operation) for cancelling offset nonuniformities. Even in the more complex embodiments, the very nature of the corner-turn array (data reformatting via orthogonal data flow) makes incorporation of

TABLE 5.3-1: CURRENT STATUS OF THE MAJOR APUP CANDIDATES

ITEM	STATUS: ILLUSTRATIVE PUBLICATION/CONTRACT
1-a.	<p>Transform/Filter</p> <p>Partial multichip hybrid demonstration only: Mattern, Lampe, "A Reprogrammable Filter Bank Using CCD DASP" J.S.C.-11, Feb. 76; and RADC/SPL Contract #F30602-79-C-0001, "CCD Signal Processor."</p>
2.	<p>Programmable Linear Transformation of Serial Data</p> <p>16- and 32-point chips commercially available from Reticon and Micro Tech. A 512 tap analog/binary CCD correlator by ESD Hanscom AFB on Contract #F19628-77-C-0263.</p> <p>Haque, Copeland, "Design/Characterization of a Realtime Correlator JSC-12, Dec. 77 (a 32-point rotating tap CCMDAC array) (plus numerous other publications). Denyer, Mavor, Arthur, Cowan, "A Programmable CCD Transversal Filter: Design and Application." CCD Applications Conference Oct. 1978 (64- and 256-point analog/analog device).</p>
3-a.	<p>High Speed Analog Bandwidth Compression Double Buffers</p> <p>NRL Contract #N00173-78-C-0212, "High Speed CCD for Bandwidth Compression";</p> <p>Chan, French, Green, "Extremely High Speed CCD Analog Delay Line," CCD Applications Conference, Oct. 75.</p>
3-b	<p>Analog Corner-Turn Memory</p> <p>Pocha, Balch, McConaghy, "CCD Architectures for High Speed Recording," ISSCC, Feb. 1979.</p> <p>Eversole, Mayer, Kansy, "A CCD 2-D Transform"; Bailey, Kansy, Kempf, Bennett, Owens, "A Complementary CCD/SAW Radar Signal Processor"; McCaughen, Turner, Keen, Eames, Roberts, "Developments in Radar Doppler Processing," all at CCD Applications Conference, Oct 78 (Arrays of 32 X 32, 33 X 66, and 16 X 128, respectively)</p>
4.	<p>Adaptive Processing</p> <p>White, Mack, Borsuk, Lampe, Kub "CCD Adaptive DASP" J.S.C.-14, Feb. 79 (16 taps plus bias tap, parallel update). Sinter, Chowaniec, Little, "Adaptive Filtering in CCD & MOS Technologies." CCD Applications Conference, Sept. 79 (Rotating-Taps, CCMDAC arrays, serial update).</p>
5-a.	<p>A-O Image Preprocessor</p> <p>N.R.L. Contract #N00173-78-C-0166, "Integrated Optical Photosensor"</p>
5-b.	<p>FLIR Scan Converter/Linearizer/Synchronizer</p> <p>(Night Vision Labs may find useful for upgrading common module FLIR)</p>

the CDS or push-pull technique both very difficult and of reduced effectiveness compared to the same techniques applied to a S-P-S analog memory. Thus the analog corner-turn chips are truly the intolerably weak link in the alternate APUP architecture for azimuth correlation.

This secondary azimuth correlator APUP has other lesser drawbacks, too. Even for limited instrumentation in terms of range cells and Doppler channels, at least two chips are needed, one for corner turning and a second for correlator. Conversely, such a limited instrumentation could be done in a single monolithic transform/filter chip. More instrumentation can be added by direct simple paralleling of the preferred monolithic transform/filter APUPs. However, cascading added corner-turn arrays requires either more sampling delay or special phasing, thereby adding even more parts back into the system or imposing additional delay-line degradation on the close-in range gates if the smaller corner-turn arrays are most simply cascaded.

In conclusion, only one possibility remains for the most attractive, cost-effective APUP device preferred for further development: the monolithic transform/filter APUP which is completely specified in the following two chapters.

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6. THE PROBLEMS

6.1 CCD ANALOG MEMORIES

Examination of the primary modes of the Transform/Filter APUP, as illustrated in figure shows that the second-order canonic recursive filter gives the more difficult requirements on the actual tap positions. The data must be propagated through the two memory sections so that all the data for a particular "Doppler channel/range cell" is available and processed (multiplied, summed, and stored in memory) at the same time. Thus the taps must always be arranged to allow selecting a second delayed tap where the longer delay equals twice that of the shorter delay, i.e., a geometric-ratio tap distribution with the ratio equal to two.

Another primary objective is to fill the "analog device processing coverage gap" where high-speed signal processing is combined with large analog memories designed and operated to provide high quality data retention in the face of high temperatures and long storage times. This objective is greatly facilitated by the combination of several independent techniques: First is "extended correlated double sampling" (1) where each data point is processed using two samples (signal-plus-reference) and (reference only) treated identically except for sequential differencing which removes nearly all offset nonuniformities. Second is the basic data flow (with uniform arithmetic and recirculation) which, by itself, helps greatly to reduce offset nonuniformities because each datum dwells the same time at any locations where a leakage blemish occurs. Third is the combination of CCD and bipolar technology featuring long signal-charge lifetimes (F.J. Kub, D. Boyle, M. Evey, E. Naviasky, "Monolithic Peristaltic CCD/ECL Technology," Proceedings of the Custom Integrated Circuits Conference,

May 23-25, 1979, Rochester, N.Y., P. 60) along with very high speed operation requiring less power and chip area than corresponding pure MOSFET devices.

A fourth technique to achieve longer storage times at higher temperatures is to apply the sequential differencing of extended correlated double sampling for each recirculation pass through the analog memory. Thus, the leakage charge accumulation is removed after each trip the data take through the memory since the new data to be stored reenter the memory at the prescribed bias charge level each time with no extra charge added from leakage accumulation during earlier recirculations. Because the traditional analog "fill/spill" CCD input is truly differential, the desired sequential differencing can be naturally incorporated within the CCD analog memory input with substantial savings in power and chip area.

6.1.1 Sample-to-Sample Crosstalk

a. Serial Structure

Consider the problem of crosstalk between analog signals transported by charge packets moving behind each other through the analog memory. Figure 6-1 describes the predicted charge transfer inefficiency, ϵ , as a function of clock frequency, gate length, channel thickness, and effective longitudinal aiding voltage for N-type deep buried channel or peristaltic PCCD. For PCCD's with four micron gate lengths operated with clocks slower than 60 MHz, typical field-aided transfer based on only four-volt clock swings easily yield $\epsilon < 10^{-5}$. Charge trapping within the shift register channel frequently starts to dominate at these performance levels giving a "lower floor" below which it is difficult to obtain better charge transfer efficiency repeatably over large populations. This typical lower limit ranges from 2×10^{-5} to 5×10^{-5} for each four-micron gate entity in the channel.

The isolation (I) between analog signals carried in sequential charge packets, may be obtained from the binomial expansion theorem:

$$I(t, N) = q_0(N)/q_t(N) = \frac{t! (N-t)!}{N!} (1/\epsilon^* - 1)^t,$$

where: $q_t(N)$ is the relative amplitude of the signal (after propagation through N stages) which has lagged into the t^{th} charge packet behind the proper one ($t = 0$),

$\epsilon^* = (p) (\epsilon)$ = effective charge-transfer inefficiency per stage ("p" gates), assumed here around 10^{-4} .

For example, consider a 100-stage memory where each stage has four physical/geometric gates which may be connected and operated in either four or two or 1-1/2 phase modes. The resultant signal attenuation, A, is given by:

$$A(N) = 1 - (1 - \epsilon^*)^N \text{ or}$$

$$A(N) = 1 - (0.9999)^{100} = 9.95 \times 10^{-3}.$$

Most of the missing charge lagged into the next following charge packet, giving crosstalk predicted by the above formula for isolation:

$$I(1, 100) = ((1/10^{-4}) - 1) / 100 = 99.59 \text{ or } 40 \text{ dB}$$

This checks closely from above:

$$\frac{q_0(100)}{q_1(100)} = \frac{0.99005}{9.95 \times 10^{-3}} = 99.496 \text{ or } 39.9 \text{ dB.}$$

Obviously such isolation between data samples in a memory which might be used to multiplex MTI or Doppler channels would be intolerable and produce many false targets.

Suppose now an extra "isolation stage" were used between each piece of analog data, requiring 200 stages in contrast to the 100 previously mentioned. The resultant isolation between data becomes:

$$I(2,200) = \frac{2}{(200)(199)} \times ((1/10^{-4}) - 1)^2 = 5024.12 \text{ or } 74 \text{ dB.}$$

Thus, 60-dB isolation between data samples should be easily achieved for 100 samples using two stages per sample. If the analog memory had incorporated an additive refresh stage of the type discussed by Kosonocky and Sauer (2), then periodically the signal charge lagging behind into the isolation position could be added back to the signal charge packet by holding the signal charge packets stationary, then clocking the isolation packets containing the lagged signal charge forward so as to combine the two charge packets. If the above example is extended by incorporating the additive refresh stage as the last stage pair at the end of the 200 stages, cascading five such sections will provide 1000 stages to store 500 analog samples. Although the crosstalk for each section does not exceed (-74 dB), because the lagging signal charge in the isolation position is removed and must accumulate anew within each section, the "crosstalk signal" which lagged into the second delay position simply adds directly the same contribution from each such cascaded section. Thus when five 200-stage sections are cascaded with their additive refresh stages, the overall isolation becomes:

$$I^*(2,200/5) = 5024.12/5 = 1004.8 \text{ or } 60 \text{ dB.}$$

Therefore, the additive refresh technique used every 200 stages or 100 data samples has enabled the storage of 500 data samples while maintaining 60 dB isolation between data samples. The preceding

discussion and results for the additive refresh technique can readily be expressed in a more general formula for the case where (L) segments of (K) stages (including the additive refresh stages) are cascaded in series:

$$I^* (K, L) = \frac{2}{(K)(K-1)(L)} \times ((1/\epsilon^*) - 1)^2$$

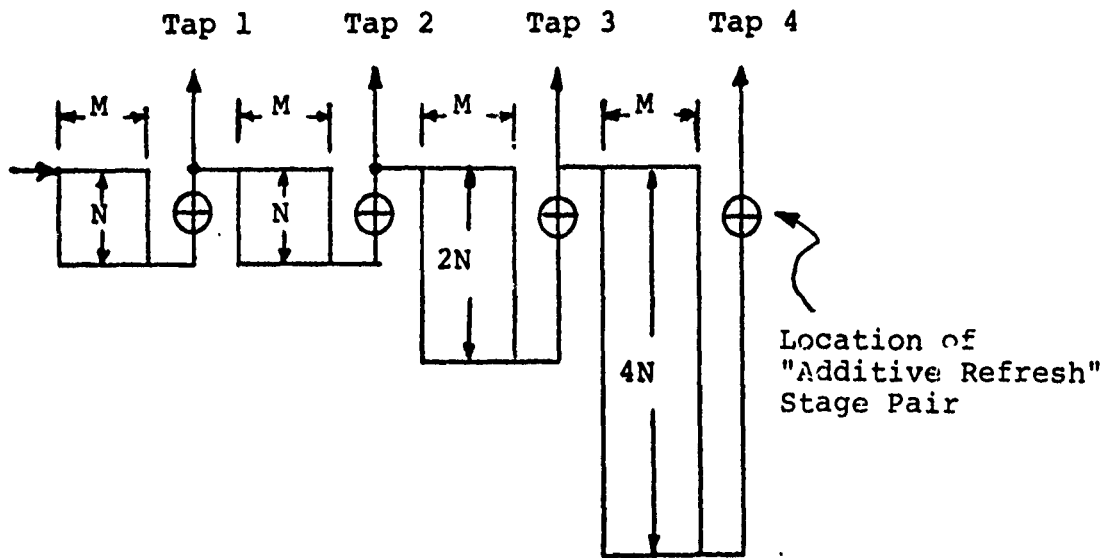
This formula applies equally well for recirculation. For example, the above 1000-stage memory might be recirculated eight times during the process of forming an 8-point Doppler Transform. Hence K = 200, but L = 5 x 8 = 40 to give:

$$I^* (200, 40) = \frac{2}{(200)(199)(40)} (10^4 - 1)^2 = 125.6 \text{ or } 42 \text{ dB.}$$

Consequently, the final crosstalk associated with the signal processing must include the effects of recirculation during the computation, which are typically an extra 20-dB crosstalk when the data pass through the memory ten times. Since many Doppler channels may involve 32, 64, or more pulse returns, extremely demanding charge transfer performance must be achieved by the analog memory.

b. Serial-Parallel-Serial Structure

The need for a reduced number of charge transfers (i.e., a short path length) is clear. The classic approach to solve this problem is the serial-parallel-serial (S-P-S) memory with M parallel columns, each having N stages stacked vertically in series. Thus the total number of storage sites is (MXN), but a datum need transfer only through (M + N) stages. The greatest saving in number of transfers occurs for square arrays (M = N) but other factors such as clock drive considerations must enter into the tradeoff. Figure 6-2 shows an analog memory with taps distributed by a geometric progression of ratio of two and with the blocks between taps configured in S-P-S subarrays. Requiring all the S-P-S subarrays to have the same number of columns yields clocking

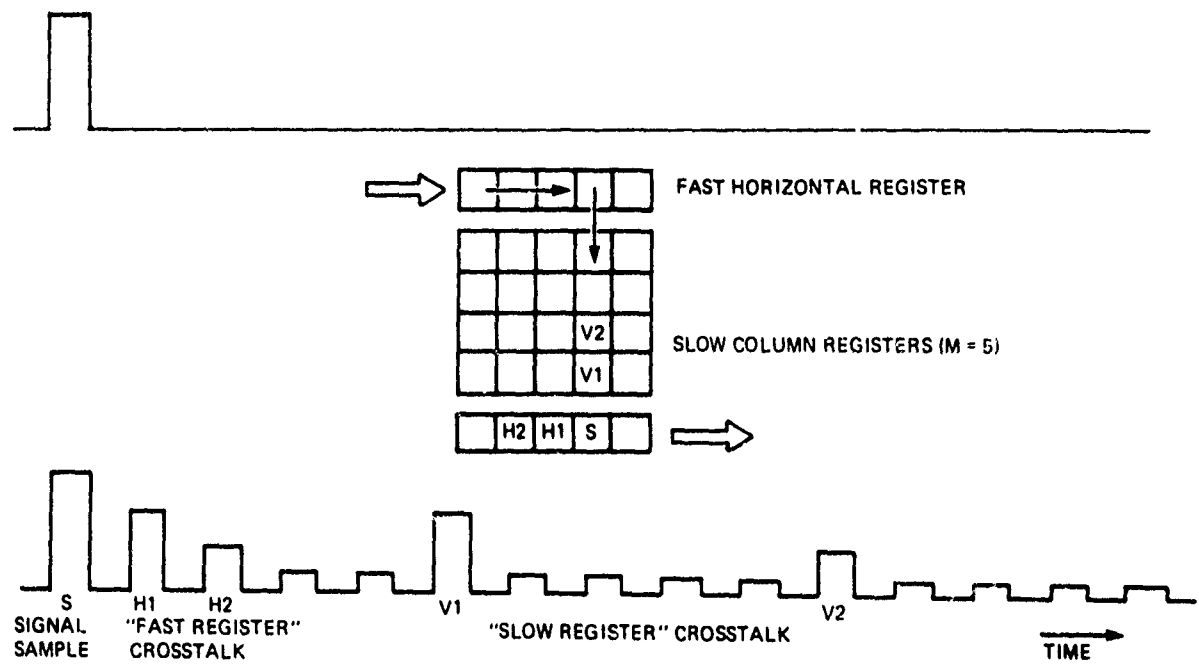


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Figure 6-2. An Analog Memory with Geometric Ratio of Two Tap Distribution

waveforms common to all parts of the memory for the fast horizontal clocks, the serial/parallel transfer pulses, and the slow vertical clocks, and is pictured in figure 6-2.

The S-P-S memory offers another benefit related to sample-to-sample isolation. The data directly behind the signal sample is one other particular signal sample in the fast horizontal register but is a completely different signal sample during transit through the slow column registers as shown in figure 6-3. Thus, in contrast to a purely serial memory, crosstalk in an S-P-S memory is split between two different sets of signal samples ((H1, H2), (V1, V2)) each with less crosstalk than for the similarly sized purely serial memory. As the number of cells in each direction of an S-P-S memory is varied, the crosstalk with each set of associated signal samples varies in response to the number of charge transfers in each direction and the effective charge transfer inefficiency for each such transfer.



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Figure 6-3. Map of SPS Memory Showing a Signal Position and the Position of Crosstalk Affected Elements

When the charge transfer inefficiency is the same for both the fast horizontal and the slow vertical shifting and the additive refresh technique has not been used to enhance charge transfer efficiency, the minimum crosstalk condition reduces to merely setting the total number of horizontal transfers equal to the total number of vertical transfers. From figure 6-2 the following conditions immediately result when using the memory out to the K^{th} tap:

Number of horizontal stage transfers = $2KM$

Number of vertical stage transfers = $N(2)^{(K-1)}$

Total available memory = $T = MN(2)^{(K-1)} = 2KM^2$

Optimum number of columns $M_{OPT, \epsilon} = (T/2K)^{1/2}$
(per SPS subarray)

Optimum sum of all horizontal stage transfers = $\Sigma_{OPT, \epsilon} = (2TK)^{1/2}$

$$\text{Optimized Isolation} = I_o = \frac{2}{(\Sigma)(\Sigma-1)} \times [(\epsilon^*)^{-1} - 1]^2 \text{ or}$$

$$I_o = \frac{2}{(2TK - (2TK)^{1/2})} \times [(\epsilon^*)^{-1} - 1]^2$$

As an example, consider an 8192-stage memory having four taps and an inefficiency per stage of $\epsilon^* = 10^{-4}$. The predicted isolation becomes $I_o = 2(9999)^2 ((8192)(8) - ((8192)(8))^{1/2})^{-1} = 3063$ or 69.7 dB. It is immediately obvious that a transform or filter computation requiring only four passes through the memory reduces the above isolation 70 dB to $(70 - 12) = 58$ dB. Since many radar Doppler channels involve from 8 to 64 points or more, the above sample memory, using two stages per analog datum so as to permit subtractive reduction of array offset nonuniformities, is very nearly unusable for all but the simplest radar signal processing. Consequently, the additive refresh technique must be employed to achieve acceptable levels of sample to sample isolation.

c. Periodic Refresh

Let us examine the additive refresh concept. A trailing "dummy charge packet" follows the signal packet along the same propagation path and accumulates the signal charge which lags behind its original packet. Periodically, the 2-step refresh operation first adds the two charge packets together, then subtracts (in the manner of a bucket brigade device) a fixed charge quantity to serve as a new trailing "dummy charge packet." Since the local additive refresh cell has no a priori information about the data it is processing, the only partition of the summed or combined charge packet, which the refresh cell can execute, is the removal of a constant amount of charge, not varying with time, but with local nonuniformities from one cell to another. Although the trailing "dummy charge packets" contain no directly usable radar signal information and exist solely to improve the apparent charge transfer efficiency, they must be handled with care throughout the memory to prevent their local nonuniformities from contaminating the true bias levels of the radar signals.

The impact of this warning follows immediately. Placement of the additive refresh cells in the serial data path such that EVERY data sample, must pass through each refresh cell guarantees that nonuniformities between refresh cells will exactly cancel when the two samples for each datum point are subtracted. Obviously this dictates the use of four CCD stages for each analog datum: two to provide for the subtractive cancellation of offset nonuniformities (and thus longer storage times and higher ambient temperatures) interlaced with another two dummy charge packets to provide the needed isolation via additive refresh. Because the total memory consists of S-P-S subarrays joined by short shift register segments incorporating the NDRO or tap stage, these short connecting segments are the logical location for the additive refresh cells as shown in figure 6-2. But will such a distribution of refresh cells adjacent to the NDRO taps, which are arranged in a binary ratioed configuration, provide adequate isolation?

The worst crosstalk contribution for a memory with additive refresh cells immediately prior to the NDRO taps comes from the vertical column path in the last and largest SPS subarray. The horizontal and vertical crosstalk contributions may be extrapolated from the earlier discussion.

$$I_H = 2 ((\epsilon^*)^{-1} - 1)^2 (KM)^{-1} (M-1)^{-1} \text{ and}$$

$$I_V = 2 ((\epsilon^*)^{-1} - 1)^2 \left((N) (N-1) + \sum_{j=0}^{K-2} (N2^j) (N2^j - 1) \right)^{-1}$$

For purposes of illustration, the memory with refreshing only near each of four taps and sized for 8000 stages is essentially optimized for maximum isolation when the smallest S-P-S subarray has 25 columns each 40 stages long and thus fast horizontal registers each 100 stages long. The predicted isolation becomes:

$$I_H = \frac{2(9999)^2}{(100)(99)4} = 5049.5 \text{ or } 74.1 \text{ dB and}$$

$$I_V = \frac{2(9999)^2}{(1.328)(160)(159)} = 5918.2 \text{ or } 75.4 \text{ dB.}$$

If such a memory were used to compute an 8-point Doppler channel, the resultant eight passes through the memory degrade the isolation by (6 dB) (\log_2 (8 passes)) = 18 dB to yield an overall 56-dB isolation. Thus, the desired performance is not quite achieved for a minimally demanding application. Consequently, to obtain acceptable performance in the more demanding typical applications, a denser distribution of refresh cells than one at each tap is definitely needed. Therefore, the additive refresh cells must be located in the columns of each S-P-S subarray as shown in figure 6-4.

Because of the double sampling or pairing nature of the S-P-S compensation technique, such an array has twice as many horizontal shift register stages as vertical register columns (see figure 6-4). Use of the additive refresh cells for improved isolation requires two more dummy stages per data sample so the number of columns equals one-quarter the number of horizontal shift register stages. Consequently half the columns in the compensated S-P-S array are selectively deactivated by breaking the serial/parallel transfer gates into two interlaced pieces, thereby yielding an attractive redundancy which enhances both MTBF/reliability and versatility as follows. The addition of some extra ISL and CMOS control circuits allows the host computer to select which set of interlaced columns are to be used in conjunction with the incorporated additive refresh cells for the high isolation mode OR to disable the internal-subarray additive refresh cells while enabling both sets of columns to give a four-fold memory increase for the low-isolation mode. The ability to select which set of interlaced columns are used in the high isolation mode effectively provides double redundancy for that key constituent of the chip. Such a redundancy may prove impractical to use in field hardware because of system restrictions on the level of fault detection, isolation, and reconfiguration. In that case, the redundancy can be used to

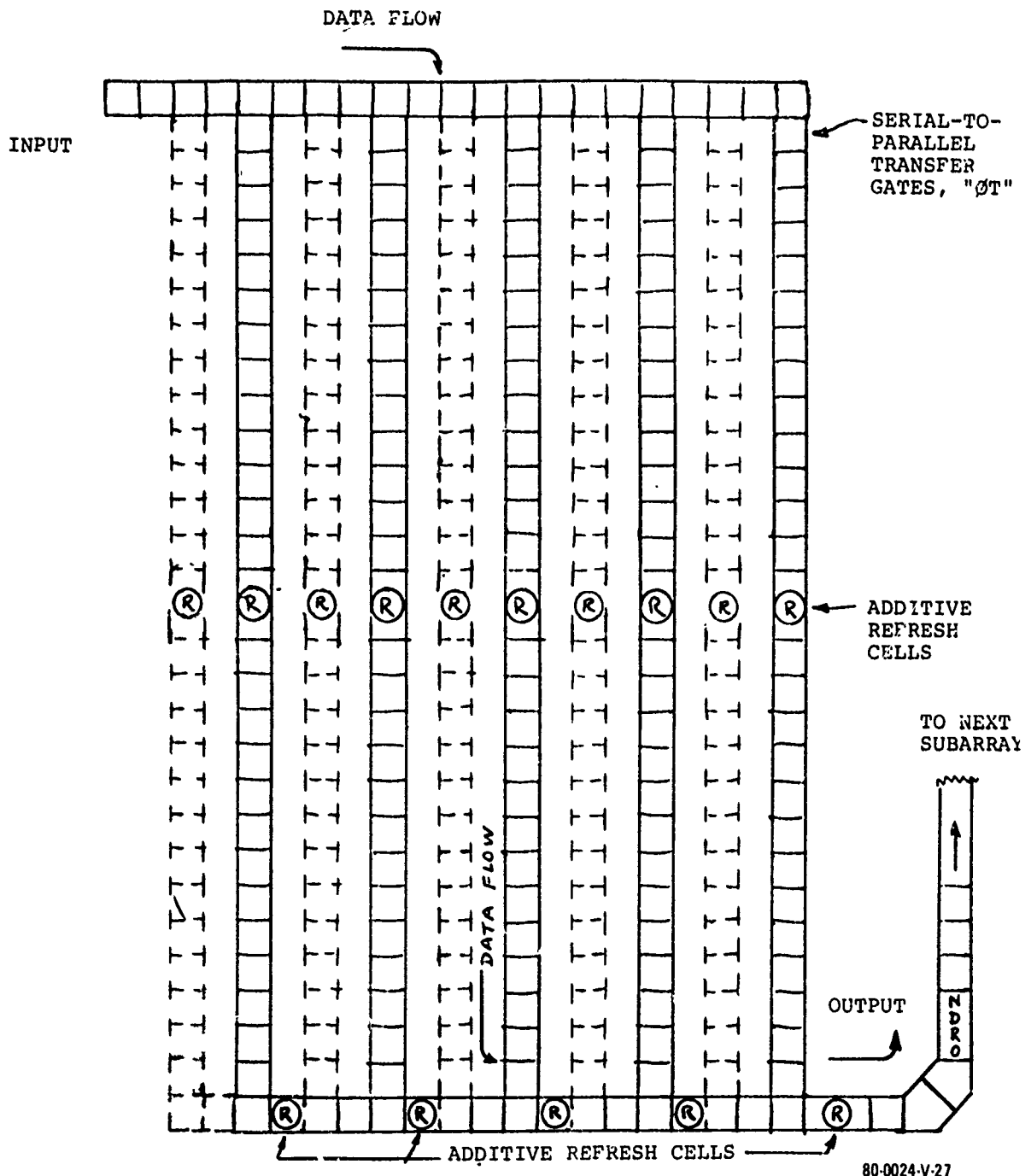
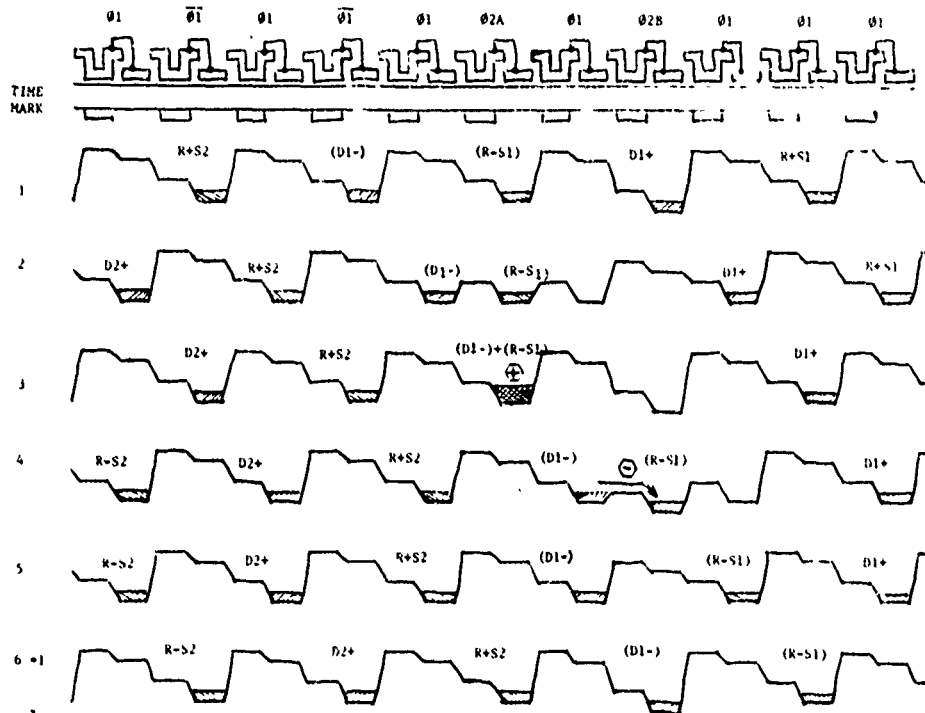


Figure 6-4. An Illustrative (5 x 28) S-P-S Subarray Configured for Sequential-Differencing Offset-Nonuniformity Cancellation with Additive Refresh Cells Distributed Internally To Minimize Crosstalk Between Signals and "Trailing Bias Charge" Nonuniformities.

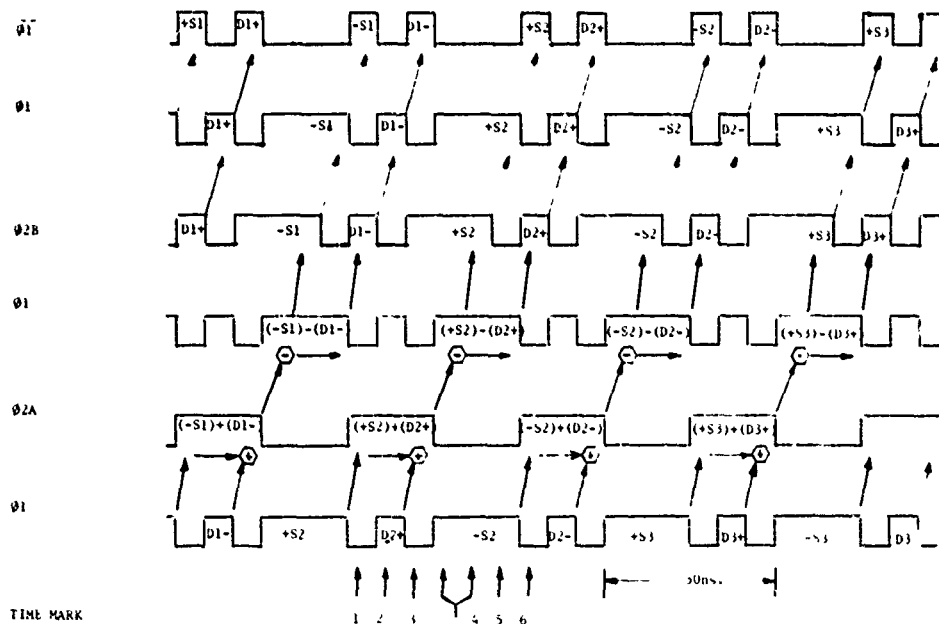
enhance production yields by disabling that set of columns which gives unacceptable offset nonuniformity rejection at the time of packaging and burn-in.

The very high density of additive refresh cells throughout the memory demands more careful attention to their design and operation than the case of only a few such refresh cells in the memory. The operation of a two phase additive refresh cell, illustrated in figure 6-5, involves the use of a complementary clock pair, ϕ_1 and $\overline{\phi_1}$, for the conventional shift register stages; while each additive refresh cell requires two stages (A and B) in which the $\overline{\phi_1}$ waveform has been replaced by the ϕ_{2A} and ϕ_{2B} waveforms respectively. The ADDITION of the two charge packets occurs in the "A" stage while the partition of the summed charge packet occurs in the B stage, thereby restoring the "dummy isolation charge packet" to be free of any signal charge contributions.

Consider the first "snapshot" of figure 6-5, which shows the charge packets arranged in pairs: $(R \pm SJ)$ are reference plus/minus J^{th} signal sample and $(DJ \pm)$ are the associated "dummy trailing bias charge packets." From time (1) to time (2), all phases reverse except ϕ_{2A} , thereby advancing all charge packets except the data sample held on position (2A) and halving the separation distance between that data sample and its respective "dummy isolation packet." With another such reversal of the phases, the two associated charge packets are added at time (3), under gate (2A). The transition from time (3) to time (4) sees all clocks reversing except ϕ_{2B} , which was an empty site attractive to the signal charge. Thus, as soon as the combined charge packets fall into the storage well under the ϕ_1 gate directly upstream from ϕ_{2B} , a previously established attractive potential pulls some of the combined charge packet forward toward the ϕ_{2B} storage well, beginning the "partitioning" part of the refresh operation. Because of the "bucket brigade", "fill/spill", or "source-follower" nature of this partitioning, the setting of the charge left behind at the ϕ_1 location is a slow process and



a. Sequential "Snapshots" of potential wells and charge packets during operation.



b. Cloning Waveforms With Data Flow Superimposed

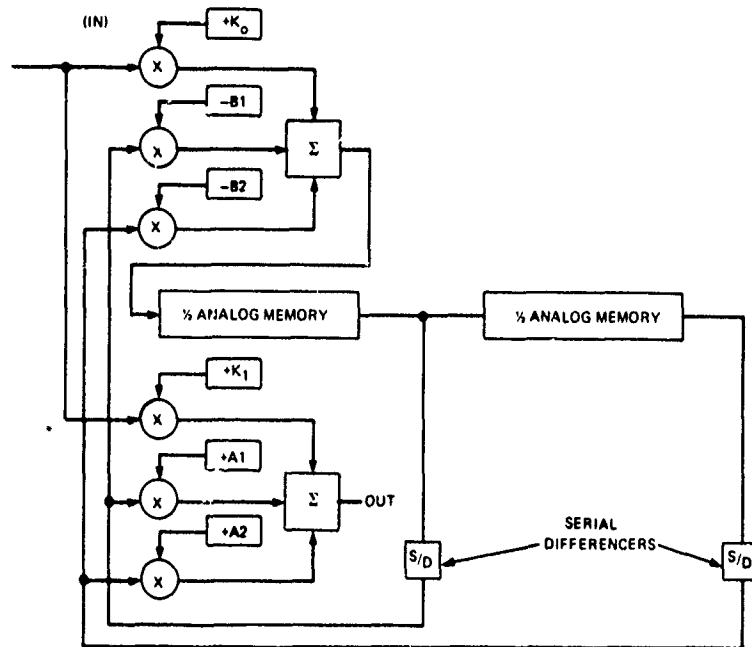
80 0024 V 28

Figure 6-5. Operation of a Two-Phase Additive Refresh Cell

therefore has been schematically allotted a double portion of clock time as marked with the number (4). Only $\emptyset 2B$ changes at the transition to time (5), moving the refreshed data charge packet back into its proper position for shifting through the remainder of the register. The waveforms of figure 6-5 are based on equal "times" for each forward shift or ADD (which are fast) and two "times" for the SUBTRACT, which is slower, so as to emphasize analog performance at the expense of waveform complexity.

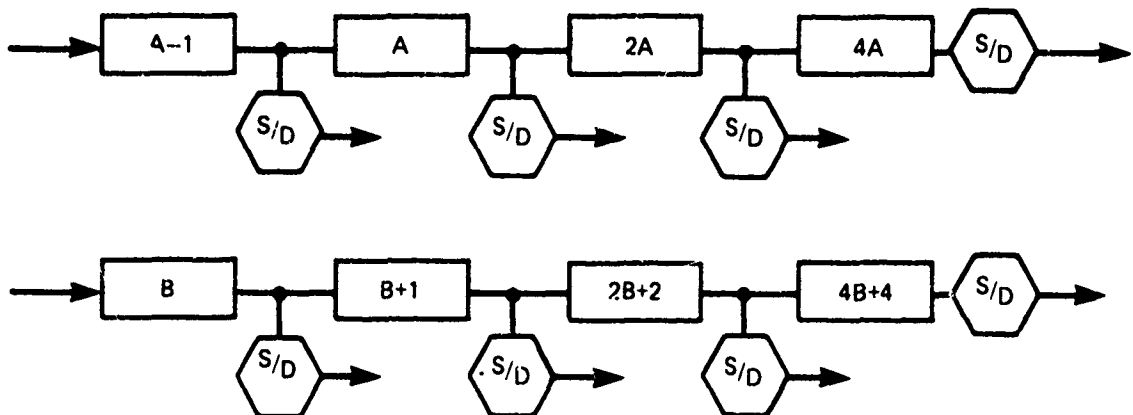
A final additional item strongly impacts the memory arrangement for optimal isolation, namely the extra delay of nearly one data sample time needed by the serial differencers to allow the subtraction of two charge packets for the cancellation of offset and leakage nonuniformities as well as the true elimination of the accumulated dark current. The location of the serial differencers in the data flow path is shown in figure 6-6. The data appearing at the output of the serial differencers must be synchronized with that arriving at the input port. Assigning a full unit data sample delay to the serial differencer, and accommodating the extra delay of the serial differencers (figure 6-7), one sees that the total loop delay around the shortest loop is $(A-1) + (1) = A$ sample times while the total delay around the second shortest loop is $(A-1) + (A) + (1) = 2A$ sample times back to the input of the summing MDAC. Thus synchronization is maintained if the first memory subarray holds one less full data sample than the second. Equivalently, by substituting $A = B + 1$, the same synchronization is achieved by making the following memory subarrays proportionately longer. Depending on the optimum subarray dimensions, this may give a smaller number of high-speed stage charge transfers.

To illustrate this, consider the optimum memory last derived above and shown schematically in figure 6-8. To shorten the first subarray by one full data sample requires stripping off the top row of the S-P-S block, then adding that row back, in pure serial fashion, but shorter by four stages. Thus, 36 high-speed stage transfers would be added. The alternate approach involves adding



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Figure 6-6. Basic Recursive Filter Configuration



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Figure 6-7. Accommodating the Extra Delay of the Serial Differencers

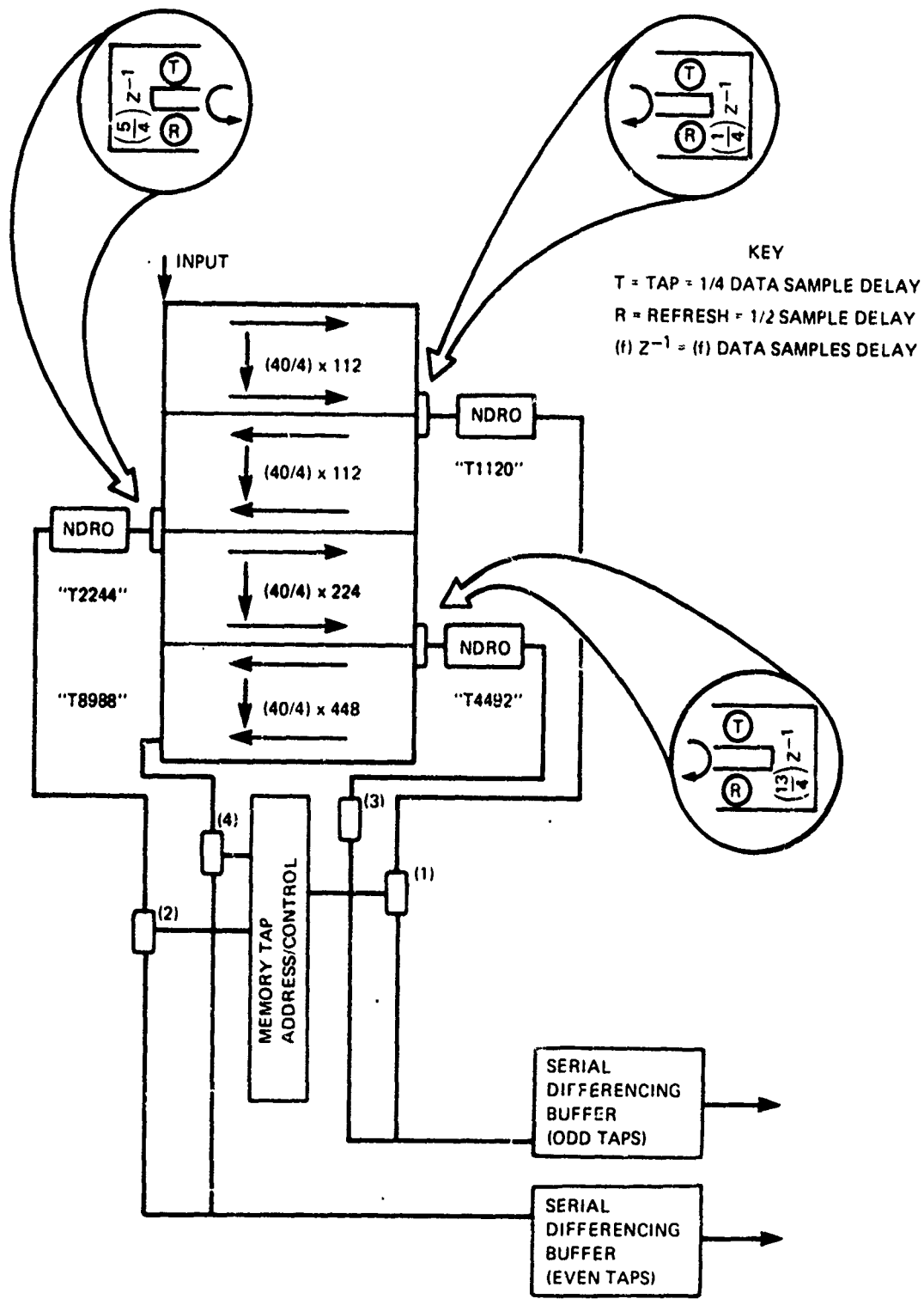


Figure 6-8. A Four Tap Memory Optimized for 90-dB Isolation Including Allowance for the Serial Differencer Delays

80-0024 VA-11

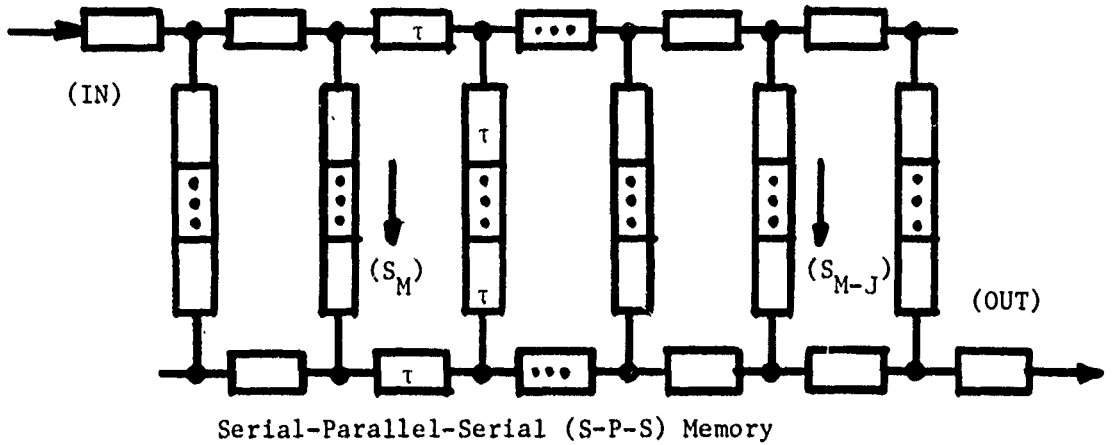
$(1+2+4) \times (4) = 28$ stages serially in the high-speed clock area. Of the 28 stages, three are the nondestructive readout (NDRO) stages and six are needed for three "additive refresh" cells as shown in the three insets of figure 6-8. The remaining 19 stages include three for turning the corners or reversing directions as indicated. Because of the location of refresh cells directly at the input to each succeeding S-P-S subarray, the extra high-speed or "horizontal" crosstalk from these stages is virtually negligible. Indeed, the crosstalk/isolation formulas as applied do not reflect some small contribution to horizontal isolation from the row of refresh cells in the very bottom read-out register of each S-P-S subarray. Thus the earlier 90-dB prediction is quite likely to still obtain.

6.1.2 Blemish Cancellation

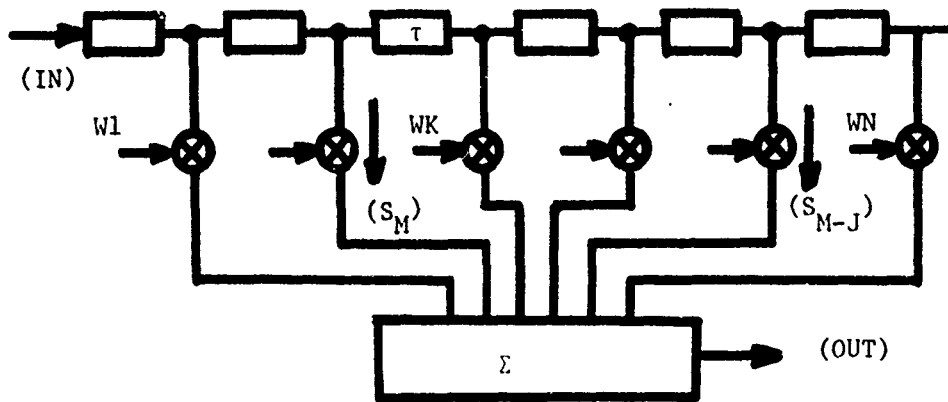
a. Non-uniformities in gain, offset, leakage

Analog devices dark current nonuniformities affect signal processing capabilities in several ways. If the signal charge samples follow the same signal processing path through the device and uniform clocking is used, the effects of most non-uniformities can be removed by extended correlated double sampling (1). This technique uses two analog samples to record a single data point. One sample is the "signal PLUS a reference" while the other is "reference only". The output is formed by the difference between the two samples. The introduction of parallel signal processing paths results in different signal samples following different paths during processing. This effect is illustrated in figure 6-9 for two different devices geometries. The serial-parallel-serial (SPS) analog memory architecture uses one input and one output but provides many distinct parallel paths for slow speed multiplexed data flow. In the most favorable circumstance of continuous uniform clocking (with no clock rate shifts or dead times) the analog data will take on an offset-fixed-pattern due to signal charge packets accumulating non-uniform leakage currents during their transit time through different paths. Assuming a buried

(a) Different Delay Paths Only, Common Gain.



(b) Different Gain and Delay Paths.



$$\text{Non-uniform gain error: } \frac{\Delta W(M)}{W(M)} \neq \frac{\Delta W(M-J)}{W(M-J)}$$

80-0024-V-4

Figure 6-9. Illustrative Non-Uniformities in Parallel Processing

channel CCD leakage current of 10 nanoamps/cm² and a CCD signal capacity of about 16 nanofarads/cm², a collapsing of the potential well due to leakage of about 0.6 volts per second results. Such a degradation of the potential well is significant when referenced to the potential barrier opposing reverse charge flow for an implanted barrier "phase and a half" or two-phase CCD, which is typically about one volt. Any parallel path containing a large leakage blemish could exceed the barrier opposing reverse flow, thereby upsetting all the analog data samples associated with the blemished path through the memory.

The limitation placed upon device performance by dark current nonuniformities in analog CCD memories can be illustrated for the case of the analog SPS memory just cited. Since the potential barrier preventing reverse signal flow for a two (or 1-1/2) phase CCD is about one volt, this value sets the maximum signal handling capacity which the shift register can propagate. For the described typical structure operating at room-temperature, a total transit time-delay of about 1.6 seconds is sufficient (on the average) to completely "erase" the analog data with full packets of leakage charge. For example, suppose a minimum usable output signal-to-noise (S/N) ratio of 10 dB is required along with a 50-dB dynamic range for the signal. This dictates an upper limit of one millivolt for the leakage-induced fixed pattern noise, giving a maximum transit time of about 1.6 milliseconds through the SPS analog memory at room temperature (assuming leakage blemishes or non-uniformities to be comparable to the average leakage). If the requirement of "MIL-SPEC" operation is added, the extra 100°C temperature increment is likely to increase the leakage currents by about one hundred fold. Thus, a 125°C operating ambient would limit such an S-P-S analog CCD to a data retention time of about 16 microseconds. This result represents a very severe restriction on the use of a two (or 1-1/2) phase S-P-S bulk analog memory. Some alternatives can overcome the leakage fixed pattern problem.

The possible solutions fall into three general categories. The most direct approach is to eliminate the cause of the problem (namely, the thermal generation of leakage charges) by operating such CCD analog memory chips in a cooled environment. The cooled temperature needed to give acceptable levels of leakage fixed patterns will depend on both the leakage characteristics of the ensemble of devices to be used and the timing details of the anticipated operation (such as fast/slow or start/stop, etc).

A second approach involves improving the fabrication process by emphasizing those techniques which give greatly reduced leakage nonuniformities both within each memory and within the expected ensemble of memories. Demanding very low levels of nonuniformity most likely will result in correspondingly low yields and higher costs.

The alternate approach involving fabrication is the development of better controls, processes, equipment, and materials so as to give more uniform device characteristics. While such fabrication improvement programs do generally exist throughout the industry, special emphasis is now being placed on those efforts by means of the Defense Department's VHSIC program. The reliable fabrication of devices having features with dimensions on the order of one micron definitely requires better materials and processing techniques than those used today. It is possible that some of these improvements can be used to give greater dark current uniformity for large scale integrated CCD circuits.

The third category of alternatives for surmounting the problems of limited analog data retention time for SPS CCD memories involves the basic design and operation of the charge-coupled analog memories. Consider first the Extended Correlated Double Sampling (ECDS) technique (1) for the more general nonuniformities illustrated in figure 6-9. The need to have both samples of the signal pair propagate identically through the signal processing array means generally that there are twice as many analog shift register stages and the analog shift register clocks must

propagate samples twice as fast. These extra charge transfers at faster rates, however, usually do not deteriorate sample-to-sample isolation because of the presence of the "reference only" samples interlaced between the "signal plus reference" samples.

Another design/operational alternative is the use of four-phase rather than two-phase analog shift registers. Since a larger potential barrier to reverse signal flow is thus provided, larger signals can be handled resulting in a greater "signal over non-uniform offset fixed pattern" dynamic range. This alternative technique can reduce the relative amplitude of both leakage and threshold nonuniformity offset fixed patterns. A third partial correction is to limit analog memories to uniformly-clocked, serpentine shift registers. This approach only eliminates leakage (not threshold) nonuniformities within a S/R and is limited to the number of stages which will not cause unacceptable sample-to-sample cross-talk.

A fifth partial alternative is very useful when long analog data retention times are needed. Instead of using storage sites which consist of comparable areas of majority carrier dielectric capacitance plus minority carrier semiconductor capacitance as in a CCD, the storage capacitance is overwhelmingly a majority carrier dielectric capacitor with only a minimal-sized access transistor which provides a very small added minority carrier semiconductor capacitance. In this way, the "semiconductor capacitance (junction or depletion region)" leakage currents give minimal voltage drift on the analog storage nodes. This approach may be used in both bucket-brigade S/R's or an analog-capacitor-RAM (3). The costs offsetting the benefits of this approach are the larger cell area (meaning only smaller numbers can be put on a chip) and a possible slower access time since the current handling capability of a minimal size transistor limits the rate at which the capacitor can be charged or discharged.

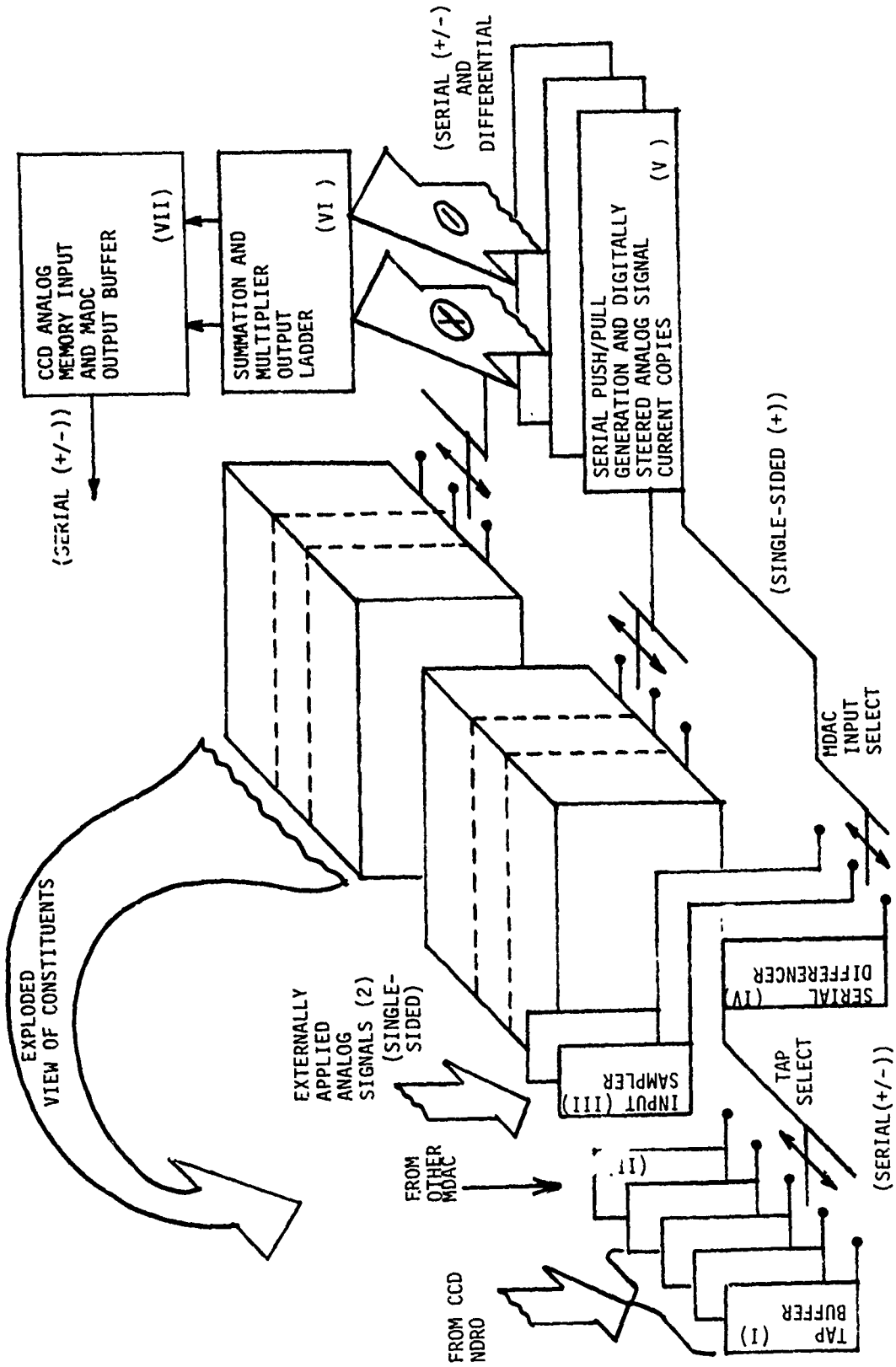
The final possibility is to merely accept the short analog data retention times needed to keep the leakage fixed patterns suitably small compared to the signal.

6.1.2.1 Serial Differencing

Accurate subtractive cancellation of errors is the driving rationale for the design of the APUP processor. For the CCD analog memory we have seen that subtractive cancellation provides significant reductions in fixed patterns from offset nonuniformities. But this basic design concept can also greatly enhance the performance of the remainder of the analog circuitry.

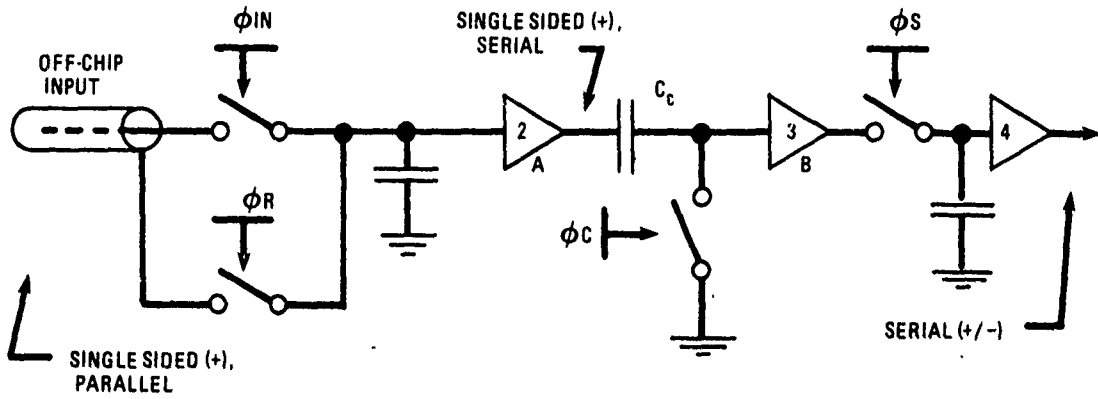
Consider the accumulation of thermally generated leakage as the analog data recirculate through the CCD memory. Even though the signal is given by the difference between two charge packets which traverse identical paths and dwell times through the memory, leakage charge can easily accumulate during a full batch processing time to cause either saturation of one or both charge packets of the pair or at best to give data which is the small difference between two large quantities and thus very susceptible to error and noise. But these difficulties can easily be absolutely prevented from ever happening by the use of a serial differencer (patented under the name extended correlated double sampling (ECDS)) as highlighted in figure 6-10. That serial differencer subtracts the charge packet pair as they are nondestructively read from the memory, automatically cancelling any accumulated leakage and giving a single quantity to represent the analog data.

Thus a single quantity representing the previously processed and stored data is presented at the input to the MDAC synchronous with the newly incoming signal needed to update that particular function. This situation is more accurately illustrated in figure 6-11, where the treatment given an input from off chip is shown in (a) and that for an on-chip input such as a CCD tap or an MDAC output is shown in (b), with the relevant waveforms in (c). Already noted above is the preferred action of the serial differencer in figure 6-11b in removing the accumulated thermal leakage after each pass through the CCD analog memory and resulting in a format change from serial pushpull (+/-) to a "single-sided serial" format having samples of the local reference level alternating

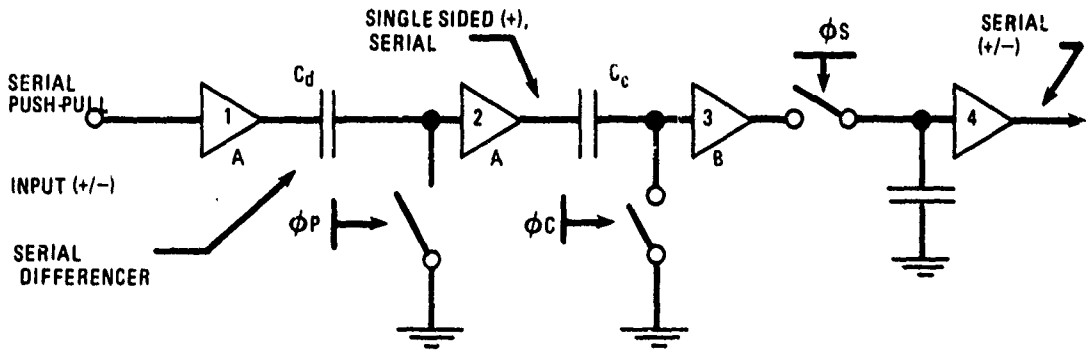


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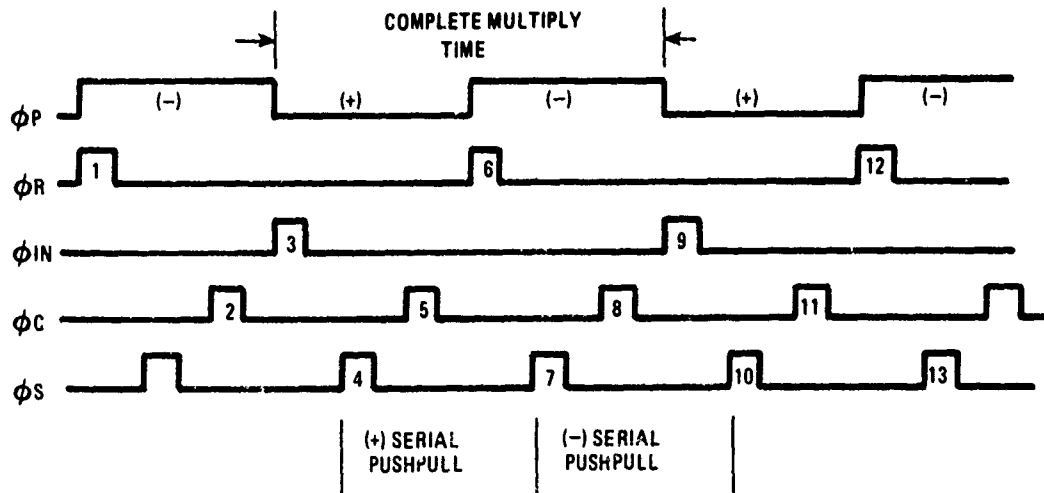
Figure 6-10. Schematic of Programmable Data Flow Through the 3 Input MDAC of the Transform/Filter APUP



a. INPUT SAMPLER AND SERIAL PUSH/PULL GENERATION FOR AN OFF-CHIP INPUT



b. THERMAL LEAKAGE CANCELLATION AT EACH RECIRCULATION.



c. SERIAL PUSH/PULL WAVEFORMS

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Figure 6-11. Implementation of the Serial Push/Pull Concept

with single samples of the data. The input sampler of figure 6-11a transforms the incoming data from continuous in time to sampled data and simultaneously translates the reference level from the incoming one (typically the shield of the coax - cable) to a new level used locally within the APUP chip. Consequently all the data ready for MDAC multiplying and summing have the same single-sided serial format.

The next step in the MDAC signal processing is the generation of the two signals (which are treated identically during the multiply and storage in the CCD memory) so that subsequent subtraction eliminates leakage and other offset nonuniformities. As more details of the circuits are given later, the choice (made here) of a push/pull signal pair to be subtracted becomes obvious. The classic push/pull technique involves using two copies of the signal with the same amplitude but 180° out of phase with each other. If the circuit transfer function can be expressed as a power series of the input:

$$y = (A_0) + (A_1) (x) + (A_2) (x)^2 + (A_3) (x)^3 + \dots$$

with push/pull inputs given by $x (+/-) = \pm (f_1 + f_2)$; then the differential output is given by:

$$z = (Y+) - (Y-) = 2 (A_1) (f_1 + f_2) + 2 (A_3) (f_1 + f_2)^3 \dots,$$

where all the even order powers of the series are cancelled by the subtraction. This cancellation of even powers demands the complementary push/pull inputs be truly the same amplitude and 180° out of phase. The serial push/pull scheme shown in figure 6-11 can meet this requirement much easier than any parallel approach where gain and phase may not be well balanced.

The steps needed to generate the push/pull analog signals in serial fashion are indicated by numbers in parentheses in figure 6-11c. The same basic sequence is valid for either the off-chip input or from another on-chip node such as a CCD tap or the output of the other on-chip MDAC.

The flow of data through the serial differencer cascaded with the serial push/pull generator as shown in figure 6-11b is illustrated in the table 6-1. The data flow for the circuit of figure 6-11a is basically the same with identical nodes bearing the same designation and with the input sampler replacing the serial differencer.

At time (1), the negative push/pull data arrive and are stored on capacitor C_d . Switch $\emptyset C$ stores the local reference (LR) on capacitor C_c at the time (2). The positive push/pull data ($Y+$) arrives at time (3) and has subtracted from it the previously stored negative data ($Y-$) to give the enhanced result $Z=(Y+)-(Y-)$, wherein "even-powers" distortion is cancelled and which is then subtractively combined with the local reference previously stored on the clamp capacitor C_c to give the newly processed output at time (4) which may be reinjected into the analog memory or used elsewhere as the leading signal sample of the push/pull pair. At time (5), the value (Z), which is still being applied to clamp capacitor C_c , is stored there by the reactivation of the clamp switch $\emptyset C$. While a new data push/pull pair starts arriving with the first sample stored on the capacitor C_d at time (6), the closure of switch $\emptyset P$ places the local reference at buffer. (2). Hence subtraction of the quantity (Z) stored on C_c at time (5) now gives $((LR) - (Z))$ to be sampled at the output. In this manner, the complementary push/pull signals are generated serially using the same serial circuit elements to obtain truly matched 180° inversion between the two samples so as to improve the rejection of even power distortion as well as the cancellation of array offset nonuniformities.

6.1.2.2 Optimum Memory Array Operation

The S-P-S subarray of figure 6-4 is a modification of S-P-S arrays typically used in infrared (IR) imaging devices, where two or more stages are used for each analog data sample. The obvious modification is the incorporation of the additive refresh cells internal to the array. Another change, not explicitly emphasized

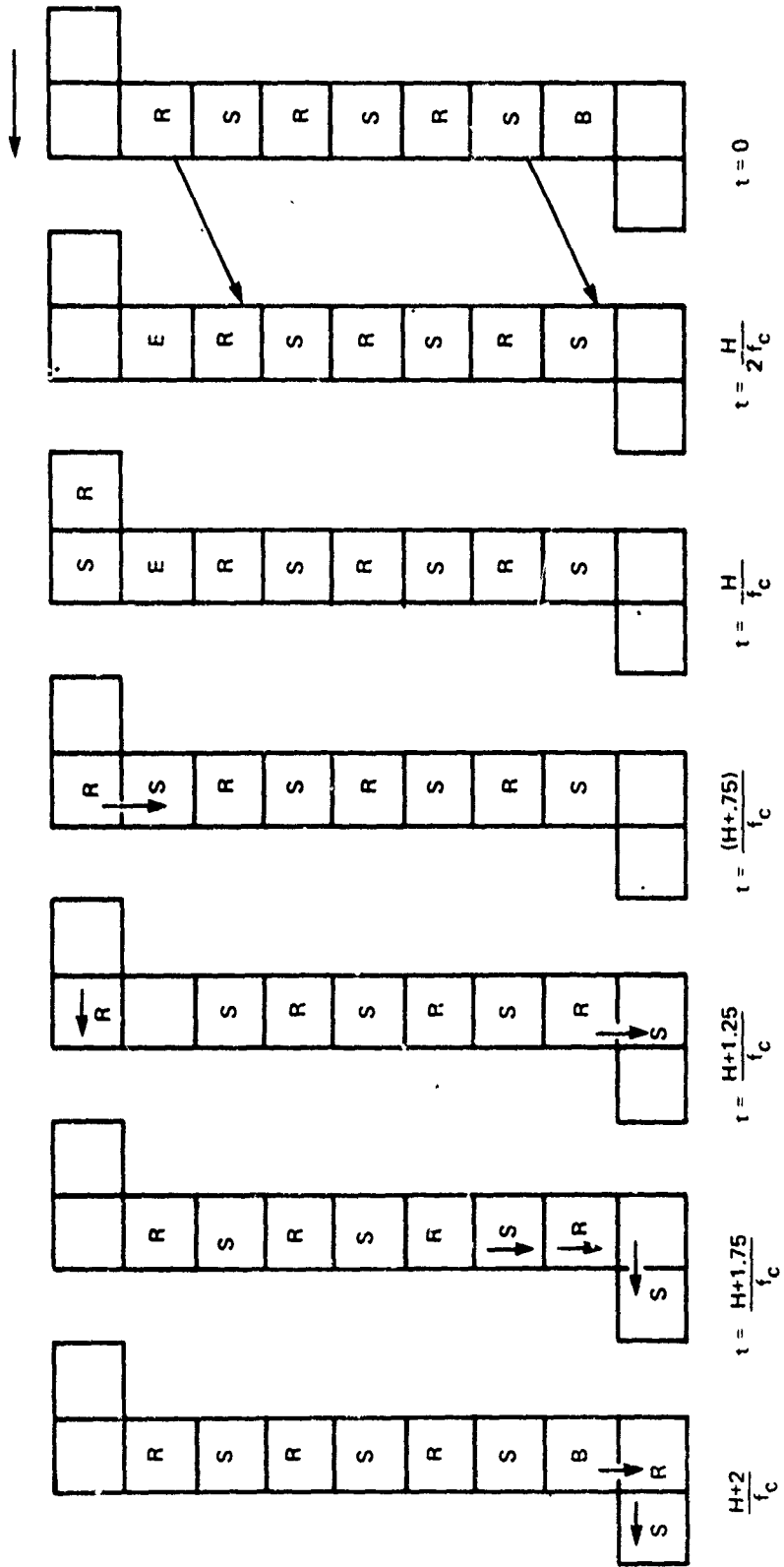
TABLE 6-1
DATA FLOW THROUGH THE SERIAL DIFFERENCER AND SERIAL
PUSH/PULL GENERATOR

TIME	NODE					
	1	CD	2	CC	3	4
1	Y1-	Y1-	LR	-	-	--
2	Y1-	Y1-	LR	LR	LR	-
3	Y1+	Y1-	Z1	LR	(Z1) - (LR)	-
4	Y1+	Y1-	Z1	LR	(Z1) - (LR)	(Z1) -- (LR)
5	Y1+	Y1-	Z1	Z1	LR	(Z1) -- (LR)
6	Y2-	Y2-	LR	Z1	(LR) -- (Z1)	(Z1) - (LR)
7	Y2-	Y2-	LR	Z1	(LR) - (Z1)	(LR) -- (Z1)
8	Y2--	Y2-	LR	LR	LR	(LR) - (Z1)
9	Y2+	Y2-	Z2	LR	(Z2) -- (LR)	(LR) -- (Z1)
10	Y2+	Y2-	Z2	LR	(Z2) -- (LR)	(Z2) - (LR)
11	Y2+	Y2-	Z2	Z2	LR	(Z2) - (LR)
12	Y3-	Y3-	LR	Z2	(LR) - (Z2)	(Z2) - (LR)
13	Y3-	Y3-	LR	Z2	(LR) - (Z2)	(LR) -- (Z2)

(Yk+, Yk-) designate push/pull data
(Zk) = (Yk+) - (Yk-) = single-sided data
(LR) = local reference

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on the schematic, is that the layout and operation of the array permit propagation of charge packets only in associated pairs. This second modification is illustrated in figure 6-12. During the first half of a "line fill time" (which is needed to fill the horizontal input register) the associated sample pairs dwell in the column registers with the bottom-most stage in a "blocking" state to minimize the depletion region in which leakage charge accumulates. During the second half of the "line fill time" the data pairs are shifted down one stage, leaving an empty stage at the top of the column, which indeed accumulates leakage charge. This leakage charge (accumulated for a half-line time) is then added to the next incoming "reference plus signal" (+S) charge packet, as shown in the center view of the data flow sequence of figure 6-12. At the same rate as the fast horizontal clock, the column is shifted down one stage, pushing an earlier (+S) charge packet into the fast horizontal readout register, while simultaneously the associated "reference only" (R) charge packet is



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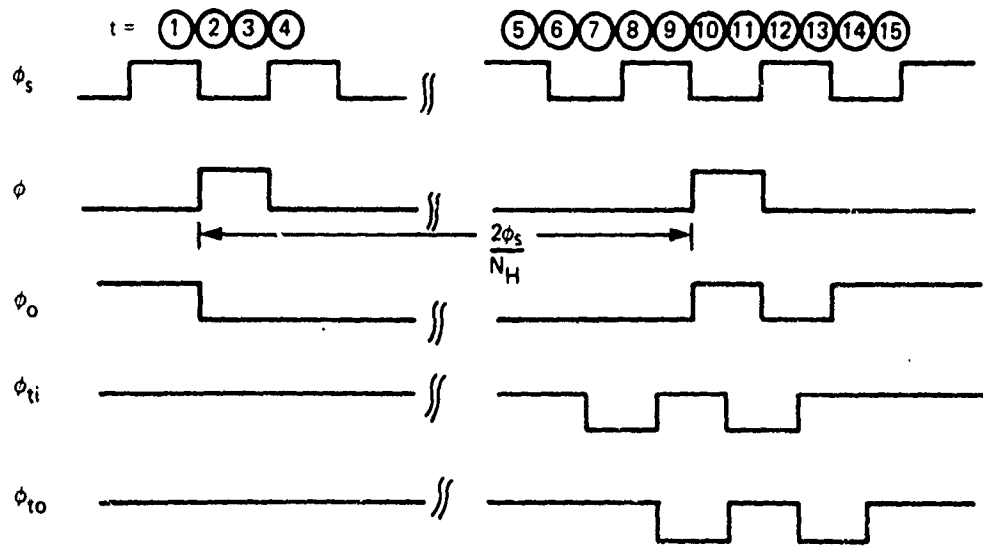
Figure 6-12. "Compensated" Operation of the "Extended Correlated Double Sampling" SPS CCD Analog Memory

entered into the top of the column where the empty stage accumulated leakage during the second half of the "line fill time." There, the associated (R) charge packet dwells for the first half of the "line fill time" accumulating very nearly the same leakage which was previously added to the (+S) charge packet, with the difference in leakage added to both charge packets of the pair arising essentially from whatever depletion region difference exists between the two half line fill times. Then for all subsequent shifts as the data sample pairs move down the column, both charge packets of the pair accumulate the same leakage charge because their respective dwell times at any position are the same. Thus when the two samples are differenced at the output, all the preceding leakage contributions are nearly cancelled.

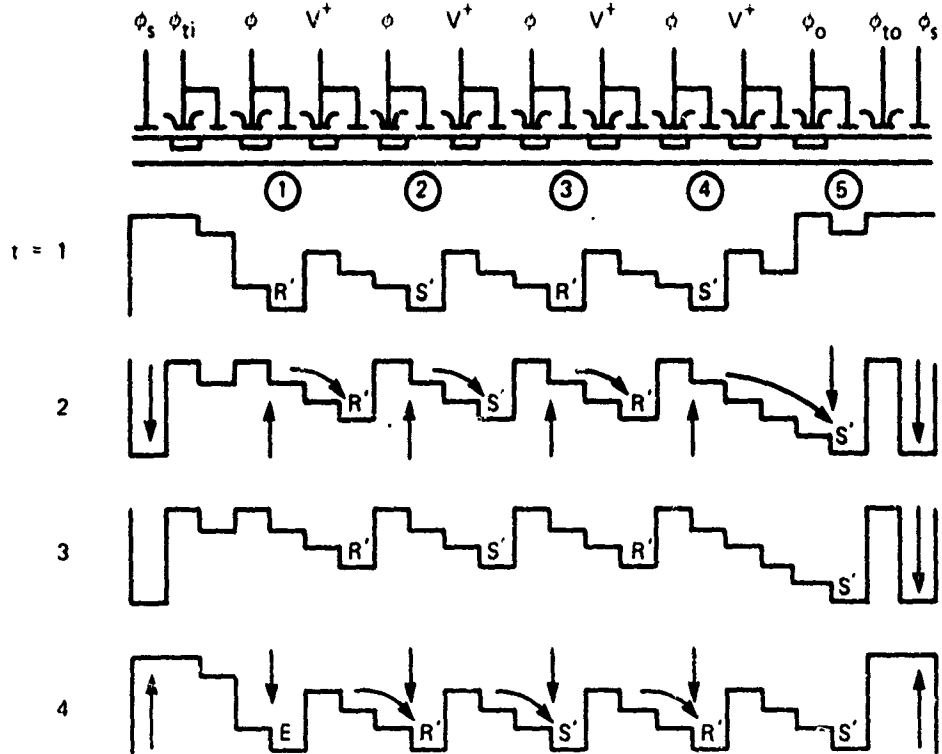
The design layout and operational details for the preceding memory compensation technique are more clearly explained using figure 6-13, which illustrates the memory cross-section potential-well diagram, and associated timing requiring for a 1-1/2 phase CCD clocking format. The timing and memory architecture is designed to maximize leakage correlation between adjacent signal/reference pairs at the memory output. High leakage correlation is achieved by structuring the memory and timing such that the signal and associated reference charge packet remain at each memory site for an equal period of time. Referring to figure -13, operation of the memory is as follows:

$$t = t_1$$

a. With ϕ low, the reference charge packet R' is stored under electrode 1. R' is the reference for the signal charge packet S' being stored under electrode 2. The prime denotes that leakage charge collected for 1/2 the "line fill time" under electrode 1 has been added to the charge packets gated from the vertical register; i.e.,

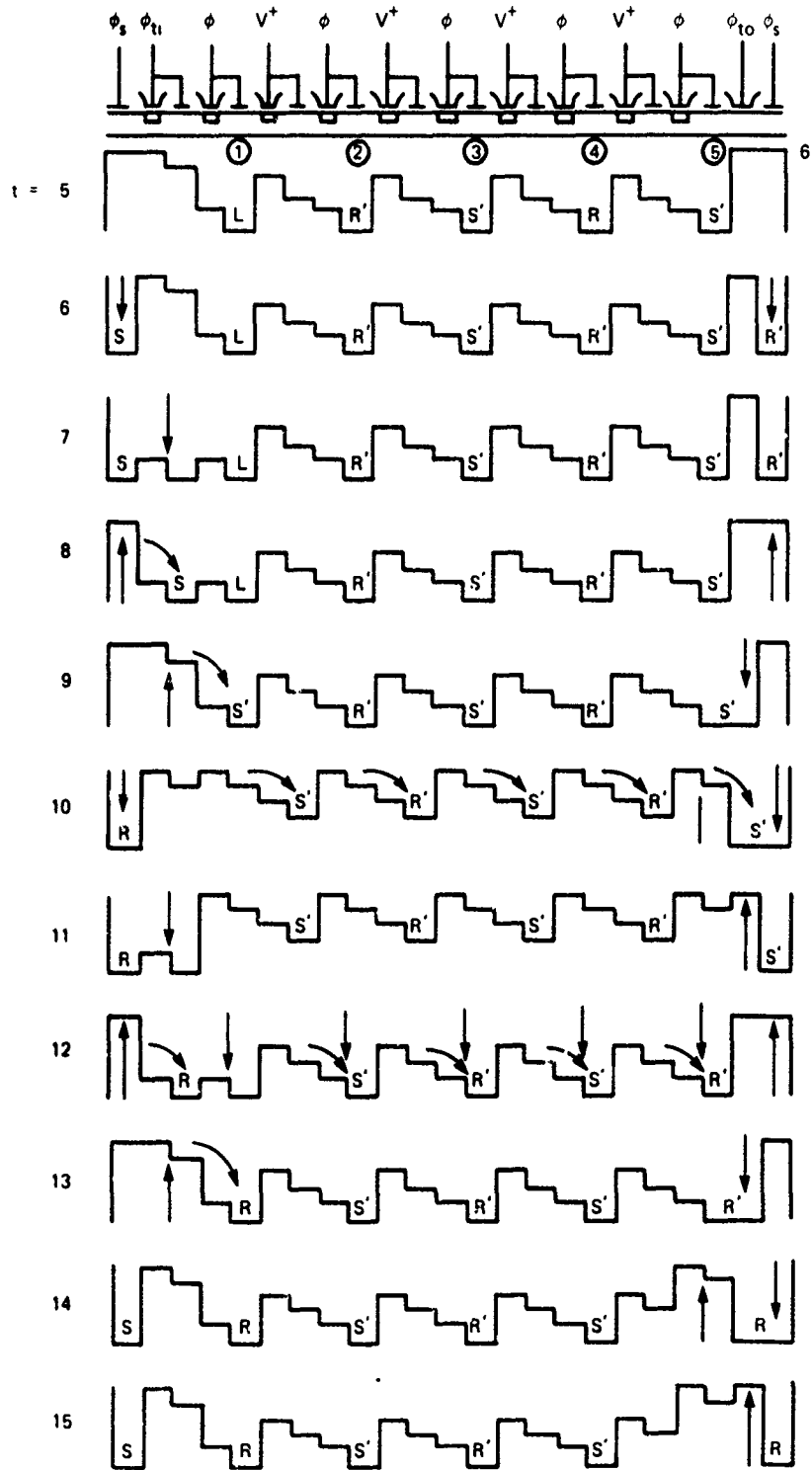


1/2 ϕ SPS MEMORY OPERATION



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Figure 6-13. Details of the Subtractive Compensation Technique for CCD Analog Memories (Sheet 1 of 2)



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Figure 6-13. Details of the Subtractive Compensation Technique for CCD Analog Memories (Sheet 2 of 2)

$$R' = R+L$$

$$L = G_1 \cdot 2/f_V$$

G_1 = leakage (blemish) change geometric rate

f_V = vertical register clock frequency

$$= f_H/M$$

f_H = horizontal register clock frequency

M = number of column registers in the S-P-S array

R = reference charge packet transferred from horizontal register

$$S' = S+L+R$$

$S+R$ = signal charge packet transferred from horizontal register

b. Under electrodes 3 and 4 (and additional pairs not shown) "reference plus signal" and "reference only" pairs are stored.

c. The potential well under electrode 5 is "repulsive" or blocking, thereby minimizing the accumulation of leakage charge from the region of electrode 5.

$$t = t_2 - t_4$$

a. ϕ goes repulsive for 2 counts and then goes attractive again. This action causes all charge packets to be shifted one electrode to the right where the charge packets will be stored for 1/2 a "line fill time."

The potential well under electrode 1 will accumulate leakage charge (L) during this time.

$$t = t_5, t_6$$

The input horizontal register is full while the output horizontal register is almost empty.

$$t = t_7 - t_9$$

a. Input transfer gate (ϕ_{Ti}) turns on (t_7). Signal charge from the horizontal register is transferred under transfer

gate (t_8), and transferred to under electrode 1 ($t = t_9$), where the signal charge is combined with accumulated leakage charge from the last half "line fill time."

b. At $t = t_9$, the output transfer gate 6 ($\emptyset T_0$) is activated. The charge S' under electrode 5 is shared between wells under 5 and 6.

$$t = t_{10} - t_{12}$$

a. \emptyset transfers each charge packet one bit on the right.

b. The Signal Charge packet (S') is transferred in a push - clock manner into the output shift register.

c. The reference charge (R) is transferred under this input transfer gate.

$$t = t_{13} - t_{15}$$

a. The reference charge for (the signal under electrode 2) is transferred to under electrode 1 where it will accumulate leakage current for $1/2$ ("line fill time").

b. The reference charge packet (R') is transferred in a push-clock fashion to the output shift register.

$$t_{15} - t_1$$

All charge packets in vertical register are stored until the input registers are half full at which time the sequence at $t = t_1$ is initiated.

In this implementation of memory, all blemish leakage is compensated except for any blemish created at this storage electrode (5) just before the output transfer gate. At this location, this signal charge is stored for $1/2$ "line fill time" ($2/M f_H$) seconds. Further, notice that while this technique gives best results when the data rate is kept constant, fast step-like changes in the master clock frequency degrade the cancellation operation only slightly. Quick changes in the clock from a high frequency, ν_H , to a low frequency, ν_L , occur in such applications as double buffering or multiple PRF's to eliminate Doppler blind spots.

Typically such a clock change occurs immediately when a memory is filled or updated. Thus the worst uncompensated dwell time difference. $\Delta t = M((v_L)^{-1} - (v_H)^{-1})$, but only the nonuniformity in leakage current (ΔI_L) between associated data storage sites during the uncompensated dwell time contributes to charge fixed patterns, ΔQ (F.P.):

$$\Delta Q(\text{F.P.}) = (\Delta I_L) (M) ((v_L)^{-1} - (v_H)^{-1}).$$

Assuming the following typical values quickly accentuates the value of the technique: $\Delta J_L = 10$ nanoamps $(\text{cm})^{-2}$, 26 vertical columns, cell area = 16 microns x 32 microns, fast write at $V_H = 10$ MHz, slow read at $V_L = 1$ MHz. Hence ΔQ (F.P.) = $(10^{-8}) (16 \times 32 \times 10^{-8}) (2 \times 26) (10^{-6} - 0.1 \times 10^{-6})$ or ΔQ (F.P.) = 2.396×10^{-18} coulombs = 15 electrons.

Since a typical peak-to-peak signal excursion may be 10^5 electrons or more, such a charge fixed pattern is 86.5 dB below the signal and even smaller than the least resolvable signal increment. Thus, for a typical double buffering application with a bandwidth compression ratio of 10, the subtractive memory compensation technique appears to promise more than adequate cancellation of offset fixed patterns. Furthermore, the above prediction is representative of the lack of compensation in dwell time for the double sample pair in the bottom-most stage of the columns; actually this prediction is too large by a factor of two for the half line fill time.

6.1.3 Refresh Cell Distribution vs Tap Count

The distribution of the additive refresh cells and the optimum array configuration may be computed. Again "K" taps are assumed distributed in a binary-ratioed manner with all subarrays having "M" horizontal shift stages and M/4 vertical columns. The shortest subarray has N stages in each column, giving a total vertical length for the whole memory of $(N) (2)^{(K-1)}$. There are now "L" additive refresh cells distributed uniformly along the length

(N) $(2)^{(K-1)}$ with one in the bottom of each subarray as shown in figure 6-4. The previous isolation formulas may be applied directly to this situation.

$$I_H = 2((\epsilon^*)^{-1} - 1)^2 (M)^{-1} (M-1)^{-1} (K)^{-1} \text{ and}$$

$$I_V = 2((\epsilon^*)^{-1} - 1)^2 \left(\frac{(N) (2)^{(K-1)}}{L} \right)^{-1} \left(\frac{(N) (2)^{(K-1)} - 1}{L} \right)^{-1} (L)^{-1}$$

Equating and simplifying: $LK M^2 \cong (N)^2 (2)^{2(K-1)}$

But the total memory size is $T = (M/4) (N) (2)^{(K-1)}$ or

$$T \cong (KL)^{1/2} (M^2)/4.$$

Substituting and combining yields

$$I (\text{optimum}) \cong ((\epsilon^*)^{-1} - 1)^2 (2T)^{-1} (L/K)^{1/2}$$

This formula suggests the number of refresh cells, L, should be a strong enough function of the number of taps, K, to overcome the isolation degradation caused by partitioning into subarrays for the taps, with the possibility of having the formula for the optimum isolation pass through a maximum at the number of taps desired for the APUP candidate. NOTE: because every pair of charge packets is always treated as an entity by all the additive refresh cells through which the pair propagates, any charge uncertainty or noise arising solely from the partition operation is cancelled by the subsequent algebraic addition. Therefore, such partition noise does not accumulate as the number of refresh operations applied to a datum sample increases.

A "refresh cell" distribution function may now be assumed. If the preferred number of memory tap points is " K_0 " and the data are refreshed uniformly " L^* " times while propagating to the K_0 th tap, then a simple, illustrative function is

$$L(K) = L' K^2 \quad \text{for } K < K_0 \text{ and}$$

$$L(K) = (L^*) \quad \text{for } K \geq K_0 \text{ where } L' = (L^*)/K_0, \text{ so that}$$

$$L(K)/K = L' K \text{ for } K < K_0 \text{ and}$$

$$L(K)/K = L' \text{ at } K=K_0 \text{ and } L(K)/K = (L^*)/K \text{ for } K > K_0.$$

Substituting this in "I(optimum)" indeed yields an optimal isolation, which is maximized for the desired number of taps, K_0 , and which may be rearranged to give:

$$L' = ((2) \cdot (T) (I(\text{optimum})) (1/\epsilon^* - 1)^{-2})^2.$$

With an objective of 90 dB single pass isolation, this predicts $L' \cong 26.85$ or $L^* = 107.4$ for $K_0 = 4$ taps and $T = 8192$ stages. Substituting further to give the subarray sizes yields

$$M(\text{optimum}) \cong 2(T)^{1/2} (LK)^{-1/4} \text{ or } 39.8 \text{ stages}$$

$$(M/N) (\text{optimum}) \cong 2^{(K-1)} (LK)^{-1/2} \text{ or } 0.386 \text{ so that}$$

$$N (\text{optimum}) \cong 103 \text{ stages.}$$

Rounding-off, modulo 4 or $2^{(K-1)}$ as needed, the following predictions are obtained:

$$N = L^* = 112, M = 40, K_0 = 4.$$

$$I_H = \frac{2(9999)^2}{(40)(39)(4)} = 32,044.9 \text{ or } 90.1 \text{ dB,}$$

$$I_V = \frac{2(9999)^2}{(8)(7)(112)} = 31,881.4 \text{ or } 90.1 \text{ dB, where}$$

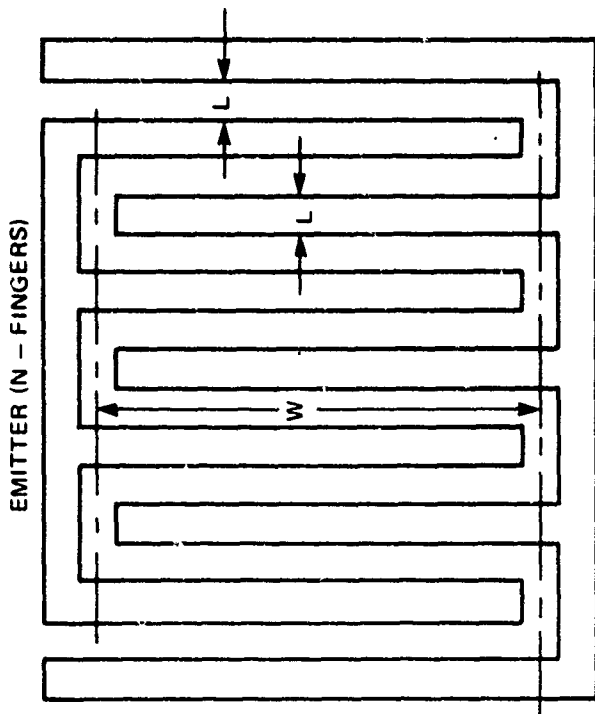
$T = (40/4) (2^3) (112) = 8960$ stages with refresh cells distributed every " λ " cells: $\lambda = N(2)^{(K-1)} (L^*)^{-1} = 8$ stages.

6.2 CCD-COMPATIBLE TECHNOLOGY ALTERNATIVES

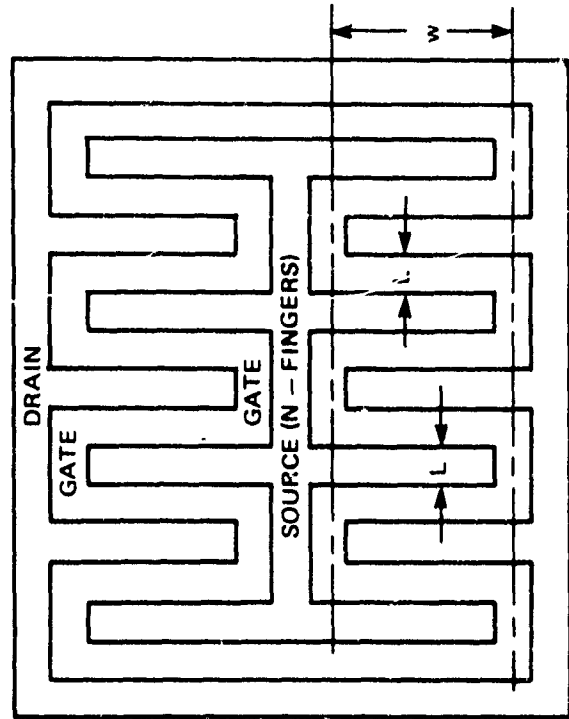
6.2.1 MOS vs Bipolar for Wideband Buffers and Drivers

A comparison of the possible device types to use in the circuits is needed, especially a contrast of an all MOS circuit types versus a mixed MOS and bipolar circuit making best use of the lower impedance bipolar transistors to more efficiently drive key signal nodes with much faster settling times. Some of the key nodes might be the capacitor plates of a charge-coupled MDAC (CCMDAC), the APUP output stage for interfacing with the next signal processing level, or even the capacitive clock gates of the CCD shift register. These illustrative situations all involve an output load on the circuit which is most strongly determined by factors independent of the circuit. The output stage may typically be required to drive an external load of about 10 pF. A single 10-bit CCMDAC (9) uses a binary weighted capacitance totalling 20 pFd. Scaling to give 9-bits resolution (one of sign and 8 of amplitude) immediately yields 10 pF capacitance which must be reset and read twice during every complete multiplication. The settling resolution and time requirements dictate a signal bandwidth of about 88 MHz, but a noise level in the APUP signal loop of nearly one millivolt leads to a maximum signal of about one volt to obtain 60 dB dynamic range. With the constraints of an 88-MHz signal bandwidth, a 1-volt maximum signal, and a 10 pF load, which type buffer amplifier - MOS or bipolar - consumes less on-chip power and less area?

The MOS and bipolar transistors to be compared for signal driver applications closely resemble each other in plan view as shown in figure 6.2-1. Both are interdigitated structures with source or emitter innermost. Moving radially outward, next comes the MOSFET channel or the emitter-base junction respectively followed by the drain contact or the base contact. Not shown, but outermost comes the FET body contact or the bipolar collector contact. The various applicable formulas for comparing the power and the area for the two device types are listed in table 2.2-1.



ACTIVE EMITTER PERIPHERY = $W \cong 2Nw$
 EMITTER BASE SPACING = L
 INTERNAL ACTIVE AREA = $A \cong 2WL = 4NLw$
 BASE RESISTANCE = $r'_b = (R_{BB}L)/W$,
 WHERE R_{BB} = BASE SHEET RESISTANCE.



ACTIVE CHANNEL WIDTH = $W \cong 2Nw$
 ACTIVE CHANNEL LENGTH = L
 INTERNAL ACTIVE AREA = $A \cong 2WL = 4NLw$

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Figure 6.2-1. The MOS and Bipolar Transistors Compared

TABLE 6.2-1

COMPARISON OF MOS VS BIPOLAR SIGNAL DRIVERS

Common "Boundary Conditions": Active interior cell area = $A = 2W \cdot L$; Transistor Quiescent bias voltage = $V_B = \gamma \cdot V_{\text{signal}}$ where $\gamma > 1$; Signal Bandwidth = $f = g_m / (2\pi C)$ where $C_{\text{LOAD}} = 10 \text{ pF}$

Item	MOS Formula/Result	Bipolar Formula/Result
Transconductance, gm	$\beta(V_{gs} - V_T) = (2\beta I_D)^{1/2}$ where $I_D = (\beta/2)(V_B)^2$	$(eI_e/kT) = (eJ_e W/kT)$ $= (eJ_e/kT)(A/2L)$
Bandwidth f	$(\beta I_D/2)^{1/2} / (2\pi C)$ $= (\beta V_B) / (2\pi C)$ or $(I_D = 2(\pi f C)^2 / \beta)$	$(eI_e/2\pi kTC)$ $= (eJ_e/4\pi kTC)(A/L)$ $(f = \lambda/L, \text{ empirically; } \lambda = 4E6)$
Quiescent Power = $P = I_D V_B$	$2 V_B (\pi f C)^2 / \beta = \pi f C (V_B)^2$	$(2\pi f C)(kT/e)(V_B)$
Device Geometry Relationship	$\beta = \mu C_{ox}(W/L)$ where C_{ox} = gate capacitance per (cm) ²	$C = C_{\text{LOAD}} + C_{\text{EMIT}}$, where $C_{\text{EMIT}} = (A)(C_e^1)$ with C_e^1 = emitter base capacitance per (cm) ²
Transistor Active Area, A	$2L^2 \left(\frac{W}{L}\right) = 2\beta L^2 / (\mu C_{ox})$ $A = (C_{\text{LOAD}}) / (\mu C_{ox} V_B) / (4\pi f L^2) - C_e^1$ where $(\mu C_{ox}/4\pi) = 1.19E-6$, $C_s^1 = 3E-3 \frac{Fd}{\text{cm}^2}$	Adjusting empirical constant, λ to give $\psi = f = (JeA)/(\psi CL)$ or $A = (C_{\text{LOAD}})/((Je)/(\psi fL) - C_e^1)$ where $\psi = 6, C_e^1 = 1.3E-7 Fd(\text{cm})^2$
Predictions for 88 MHz bandwidth, 4 micron spacing, two volt bias, $J_e = 0.6 \text{ amp/cm}$.	$P = 12.16 \text{ milliwatts}$ $A = 7.19E-5 \text{ cm}^2$ (about 85 microns square)	$P = 0.3 \text{ milliwatts}$ $A = 3.689E-6 \text{ cm}^2$ (about 19 microns square)

*A.B. Phillips, "Transistor Engineering -- An Introduction to Integrated Semiconductor Circuits" M:Graw-Hill Series in Solid State Engineering, 1962, New York, pp. 324--25.

The most important restrictions both transistors must satisfy are the ability to drive the same equally-heavy load (10 pFd.) for the same signal bandwidth. (88 MHz). Assumed in the table is emitter-follower/source-follower circuit configuration so as to permit use of pentode or saturation region formulas for the MOSFET as well as capacitive loading of the emitter which dominates the bandwidth limitation. Further simplifying assumptions are a MOS threshold near zero and a transistor quiescent bias, V_B , near two volts.

The conditions given above may be substituted into the MOS formulas to give an N-channel MOST which needs $I_D = 6.08$ milliamps to yield a g_m shunting the 10 pF. load capacitance. The area formula specifically includes that extra parallel capacitance and yields a prediction of $7.19E-5$ cm² which is equivalent to a square 85 microns on each side.

For the bipolar transistor the linear dependence of transconductance on current (rather than the square-root power) gives $g_m = 580$ millimhos at 150 microamps (much lower than the 6.08 milliamps needed by the NMOST). An empirical formula relating maximum transistor frequency to bipolar dimensions is given in "Transistor Engineering" by A.B. Phillips. Correlating that data with detailed manufacturers' specification sheets (such as National Semiconductor "Discrete Databook", '978, process 27, NPN double diffused silicon epitaxial transistor) facilitates predicting bipolar device area based on a range of values for the emitter current density per cm. length of emitter-base periphery. The current gain (β) of a bipolar transistor falls off at very low current densities because of surface states and again at high current densities reducing emitter efficiencies due to effective base area crowding and modulation of base resistivity. One guideline for the high current density is 3 milliamp per 0.001 in. or 1.2 amps per cm with low density values ranging toward 30 milliamps per cm. The area of the bipolar transistor can then be set by selecting a high current density conveniently near the upper limit (such as

0.6 amps per cm) to correspond to the peak current to be supplied to the load. Consequently, based on four micron base-emitter spacing, the active interior area of the bipolar transistor of table 6.2-1 becomes 3.689 E-6 (cm)^2 giving a stripe width of 46 microns, checking well with the assumed maximum emitter current density of 0.6 amps/cm. The 150 microamp quiescent current needed to provide the bandwidth then results in an emitter current density of 31 milliamp/cm. which is still within the broad range of useable current densities. In all fairness to the NMOS driver, for the much smaller bipolar transistor to provide the same higher drive voltage at the higher frequency limit to the load capacitor in the linear "class A" mode as can the NMOST stage, the bipolar quiescent current must be increased (but still within the allowable density range). However, even the 150 microamp quiescent bipolar bias current is able to drive in "class A" mode a full one volt signal into the load capacitor for all signal frequencies below two megahertz, using the same small area and low power requirement. Furthermore, relaxing the linear operation requirement to allow switching immediately leads to the significant benefits of using bipolar drivers for CCD clocking gates.

To summarize the preceding comparison of MOS versus bipolar drivers for analog and digital signal nodes, subject to the constraints of the same externally specified load and bandwidth, the most outstanding difference is the greatly reduced area requirements of the bipolar transistors. Secondly, for linear small analog signal situations, the bipolar power consumption is also much lower than for MOS circuitry. For drivers for linear large analog signals or for large digital clock loads (e.g., CCD clocks) the power advantage is reduced but the significantly more compact areas still obtain. Consequently, the need to combine both very fast, low power operation with a high density of functions on the APUP chips dictates the mixture of MOS and bipolar transistors. Such combinations are not only commercially available but are also made on the same chips with CCD's.

6.2.2 CMOS Proposed for Switches and Quasi-Static Registers

CMOS circuitry is proposed for the analog switches used in configuration control and also for the quasi-static registers storing the configuration status information. It also will be used on the slower clocking control for the CCD's.

Westinghouse (12) has combined CMOS, bipolar, and CCD technology in a single monolithic integrated circuit chip. Commercial products (13) are on the market which combine CMOS and bipolar technology on the same chip. The APUP development program will integrate the appropriate technologies to achieve the optimum combination of speed, packing density, and low power usage in each functional area of the APUP chip.

6.2.3 ISL Proposed for High-Speed Low-Power Digital Data

Integrated Schottky logic (ISL) is proposed for the high-speed coefficient data entry into the MDAC's. ISL has the advantage that it can be combined on-chip with analog circuitry for use in analog processing. A comparison of ISL with integrated injection logic (I^2L) and low-power Schottky TTL is presented in table 6.2-2 (14). All three were made in a process similar to that proposed for APUP, namely with an epitaxial layer approximately $3\text{-}\mu\text{m}$ thick and with minimum dimensions on the order of $5\ \mu\text{m}$.

Both ISL and I^2L exhibit packing densities an order of magnitude better than TTL. The packing density shown for the middle of the IC is twice the overall average because of the TTL buffering needed for the I/O with I^2L and ISL in the example given. In speed (minimum propagation delay) the ISL has a clear advantage. The ISL has lower power than Schottky TTL but the speed-power product can approach that of Schottky TTL. It is clearly better than I^2L and will be used for the digital data handling in the APUP.

TABLE 6.2-2⁽¹⁴⁾
 LOGIC FAMILY COMPARISON

	ISL	I ² L	"LS" TTL
Packing Density (gates/mm ²)			
Specific logic area:	120 - 180	200 - 280	15 - 20
Total active area:	60 - 100	120 - 180	10 - 20
Speed-Power Product (pJ)	0.5 - 15	0.5 - 2	19
Supply voltage (V)	1 - 3	0.7 - 1	5.0
Propagation delay (nsec)	2 - 5	10 - 20	5 - 10

6.3 MONOLITHIC CIRCUIT ALTERNATIVES

6.3.1 MDAC Implementation

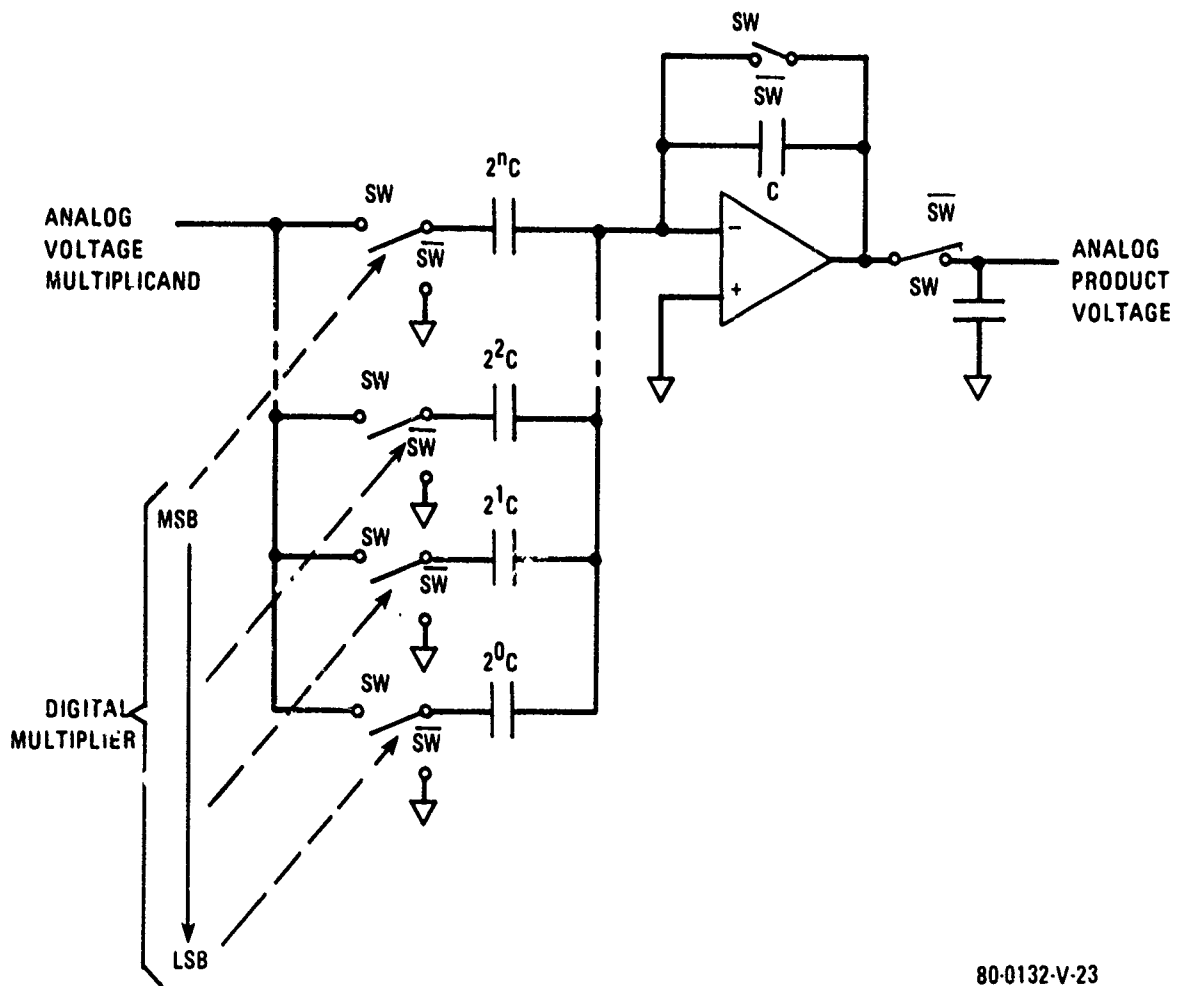
The purpose of the MDAC is to form the analog product from an analog multiplicand and digital multiplier. On the APUP chip, as shown in figures 6.3-1 and 6.3-2, MDAC's (denoted by \otimes 's) are required for both the Transform and Recursive Filter Configurations. There are two candidates for the MDAC which use state-of-the-art technology, namely a charge-coupled MDAC (CCMDAC) (4), (5) and a hybrid current source R-2R ladder network (6). To determine the optimum MDAC candidate for the monolithic APUP chip, the implementations of each candidate will first be briefly described, optimum architectures discussed, and finally a comparison with respect to power, area, and matching tolerances will be presented to meet the required 10-MHz multiply rate.

6.3.1.1 Charge-Coupled Multiplying Digital-to-Analog Converter (CCMDAC)

Arrays of CCMDAC's have already been made and investigated by Copeland (4), (5), et. al., with an objective of real-time correlation.

The concept of the CCMDAC is sketched in Figure 6.3-2.1. It resembles an inverting op-amp circuit with binarily-variable gain except that charge is being balanced by the op amp instead of current. Between measurements, all switches move to the \overline{SW} position in order to initialize the charge on the capacitors. To perform the multiplication, those switches controlled by a "1" in their multiplier bits move to the SW position while those controlled by a "0" simply remain unchanged. The output capacitor switch closes in order to sample the settled product voltage.

The CCMDAC as shown is a "two quadrant" form, i.e., the analog multiplicand may be bipolar but the digital multiplier is positive only. The same circuit may operate in "four quadrant" mode by using a 2's complement digital code (sign bit = 1 for minus) and reversing the action of the MSB switch (signum) so



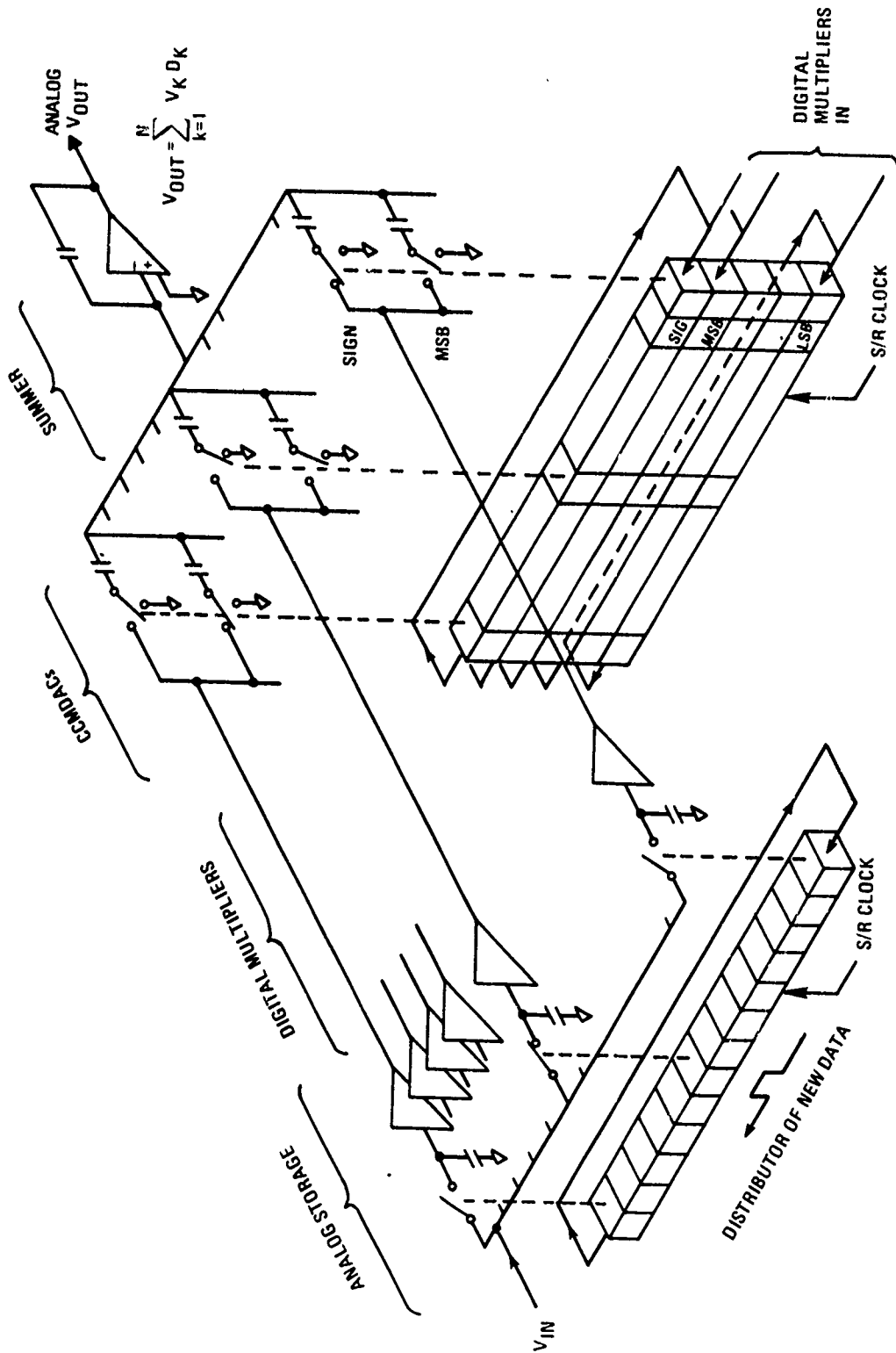
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FIGURE 6.3-2.1: CCMDAC Concept

that at \overline{SW} time it initializes on the analog multiplicand voltage and with a "1" (minus) it connects to ground. However, if all of the capacitor-initializing switch actions are reversed in this way by the digital sign bit, then the largest capacitor stage can be eliminated with a considerable saving in chip area. The digital multiplier must be in sign/magnitude code now for this to work.

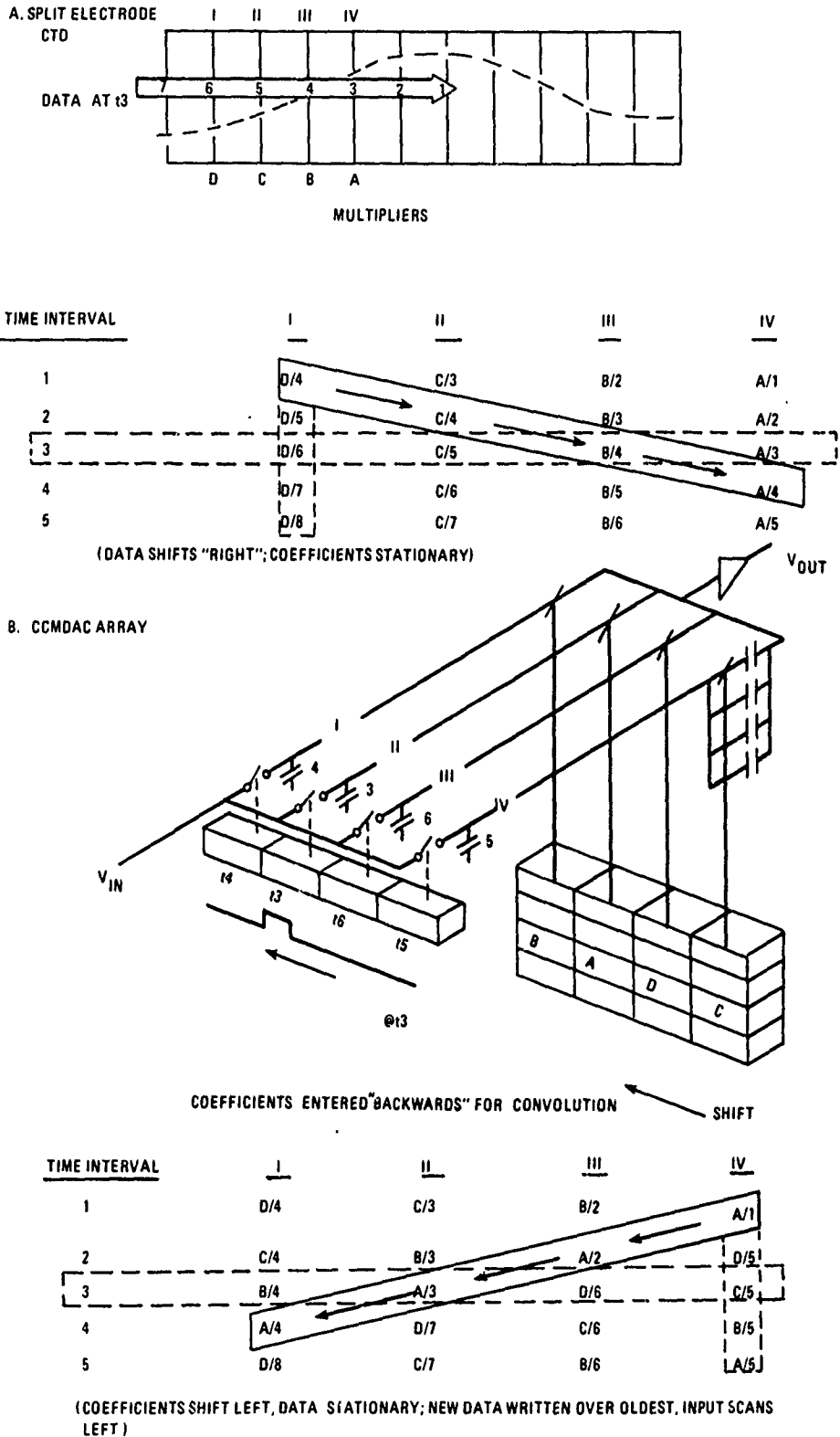
The basic concept can be expanded with multiple CCMDAC capacitor banks feeding one charge integrator. If the analog multiplicands are stored on a commutating capacitor bank as a series of samples of an input waveform while the digital multipliers are circulated in an n-level shift register stack, the data sets are able to shift relative to one another. Such a longitudinal configuration as shown in Figure 6.3-2.2 can be very attractive where simple correlations or convolutions are involved or where the number of multipliers is smaller than the word length of the coefficient needed in the correlator and a fast repetitive multiplication rate is also needed.

Figure 6.3-2.3 illustrates two contrasting techniques for performing such transversal operations as convolution or correlation. Part (a) shows the "longitudinal" configuration traditionally associated with many analog CTD's such as split-electrode filters. The multiplier coefficients are in fixed geometric or architectural positions while the analog data samples are sequentially shifted through the register, giving a new "sum of products" output with each data-packet advance by one sample-delay interval. The second scheme illustrated in figure 6.3-2.3 is the technique used by Copeland et. al., ^{(4), (5)} in their CCMDAC array correlator. The analog data remain stationary while the multiplier coefficients circulate in the opposite direction around the array. The longitudinal architecture of figure 6.3-2.2 was used by Copeland et. al., for the correlator application but suffered a serious handicap in the adaptive application. Fast adaption suggests simultaneous parallel update of all multiplier coefficients. The longitudinal serial



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FIGURE 6.3-2.2: Sliding Sum-of-Products Charge-Coupled Convolver



80 0132 V 22

FIGURE 6.3-2.3: Convolution Data Flow in a Split Electrode CTD and in a Longitudinal CCMDAC

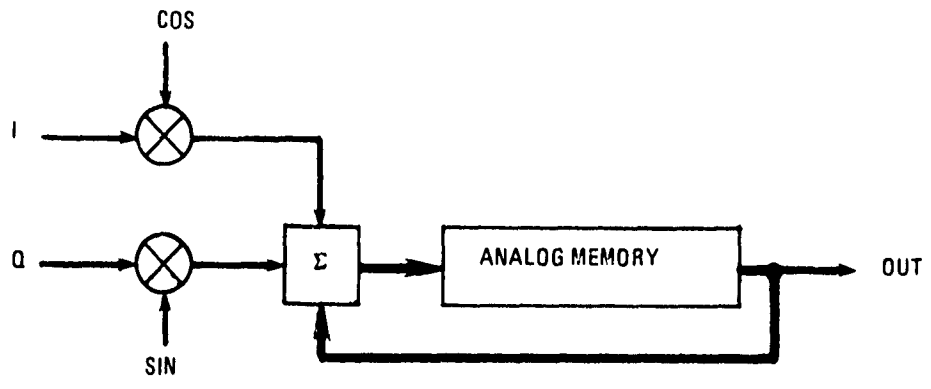
shift registers for the multiplier coefficients seriously impair simultaneous parallel access to manipulate coefficients, but can be used effectively in such added applications as the CCMDAC's needed in the Transform/Filter candidate of Figure 6.3-1. For this latter application, the longitudinal circulation of multiplication coefficients is not needed as in the convolution/correlation case of figure 6.1-2.

In one implementation, as shown in figure 6.3-3, a four quadrant multiplication of the analog input multiplicand and digital multiplier of n resolution bits to form a weighted charge product given by

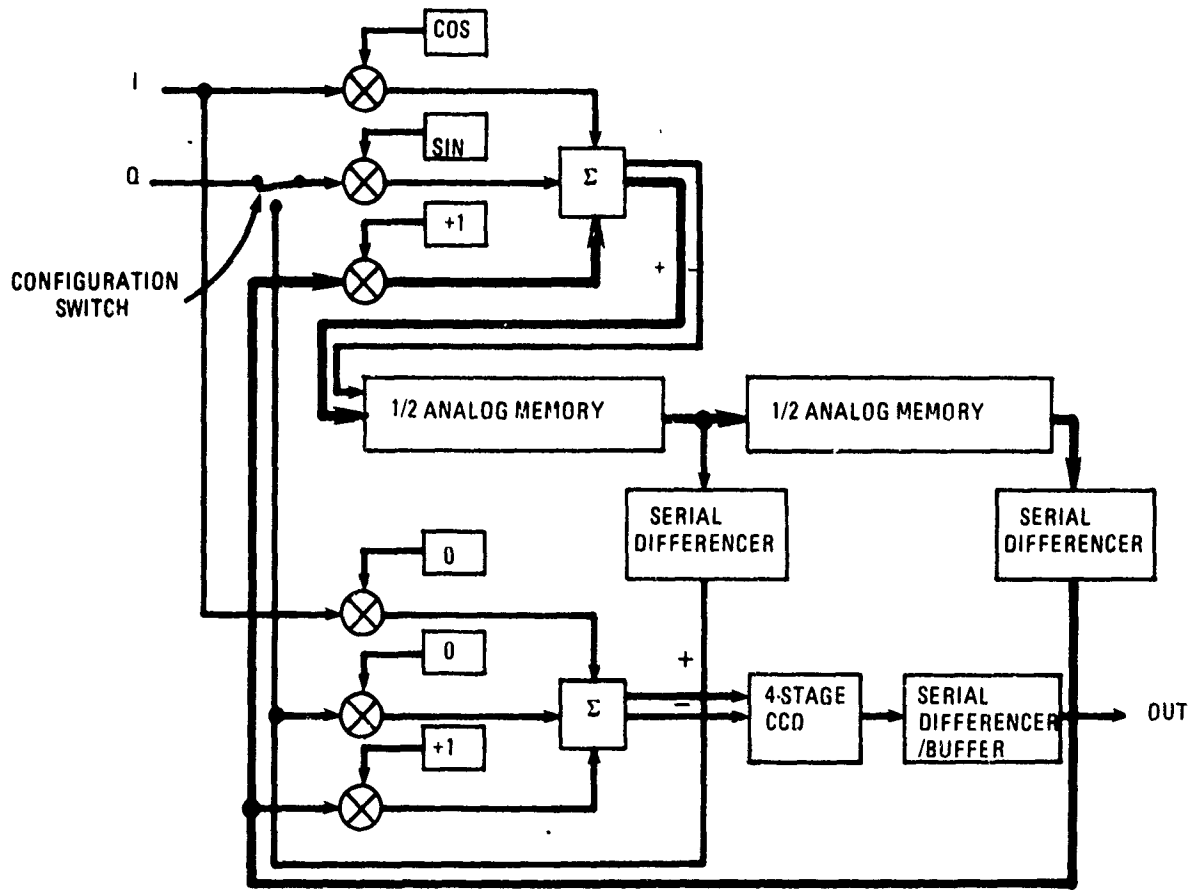
$$Q_{out} = \sum_{i=0}^{n-1} (C_i) (V_{signal}) (2^{-i})$$

requires introduction of an offset charge. This is done by adding a constant voltage to the largest capacitor, which requires n + 1 binary-weighted capacitors for n amplitude resolution bits in this implementation.

A second approach is illustrated in figure 6.3-4 in which the sign bit (sign-magnitude representation) of the multiplier determines the sequence in which the input analog signal is applied.



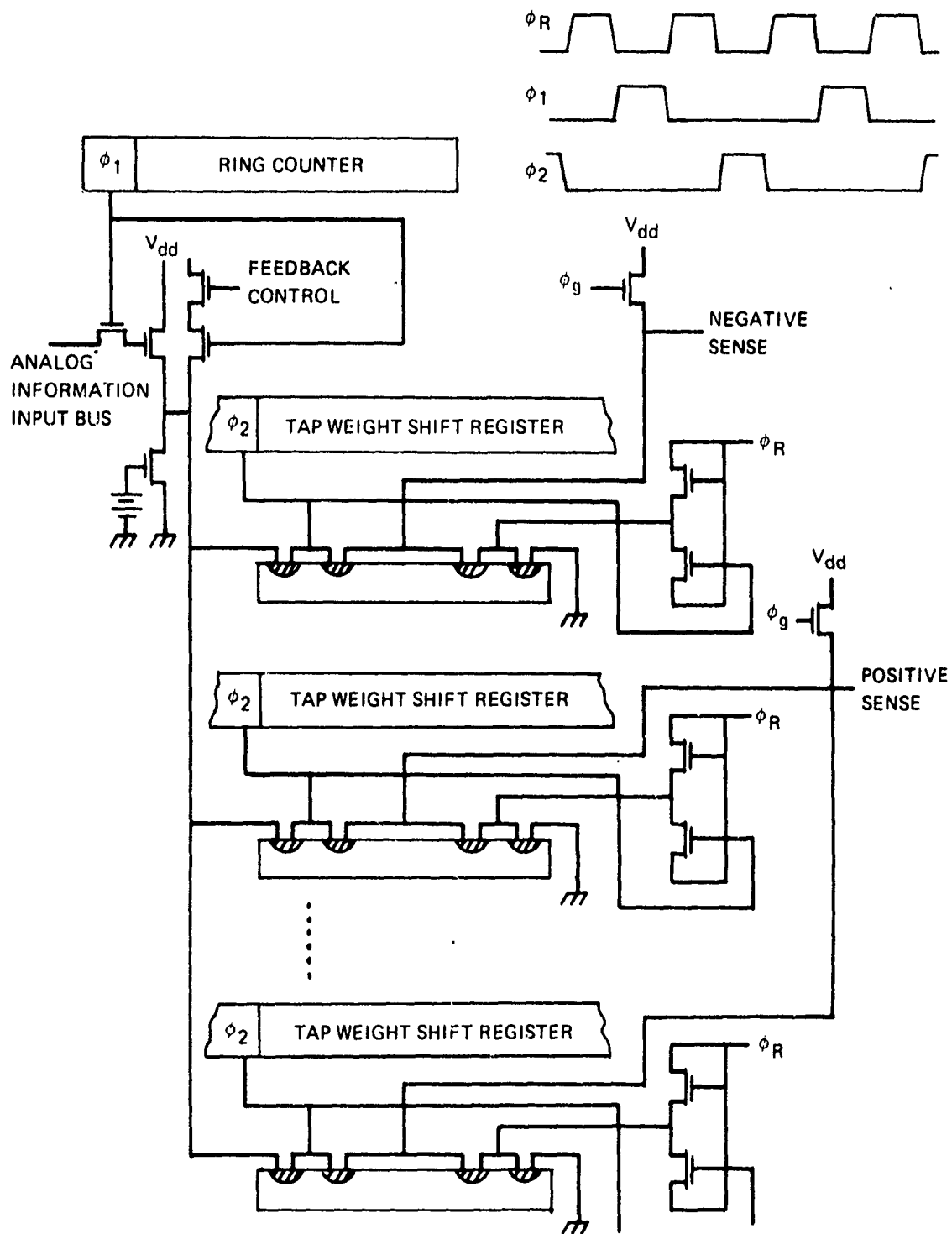
A) TRANSFORM CONFIGURATION



B) TRANSFORM RECONFIGURED FROM RECURSIVE FILTER

80-0024-V-20

Figure 6.3-2. Demonstration APUP Modes



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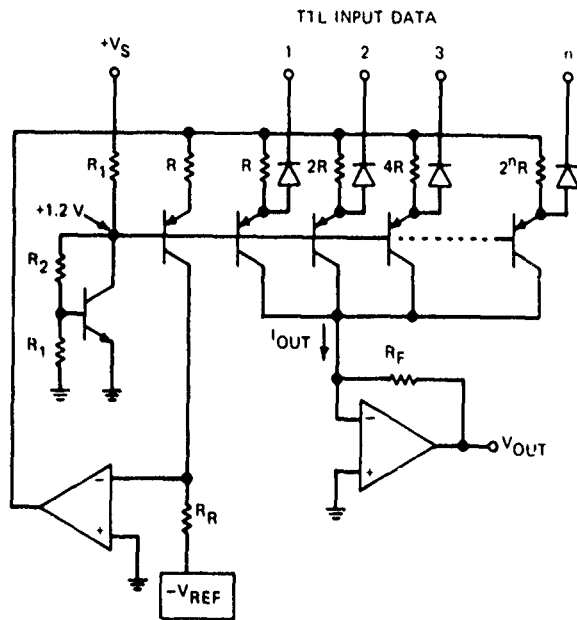
Figure 6.3-3. One Tap Portion of CCMDAC (After Copeland⁴)

to the capacitor array. In this realization, n binary-weighted capacitors are required which decreases the array capacitance by a factor of 2 over the first approach.

6.3.1.2 "R-2R" Ladder MDAC

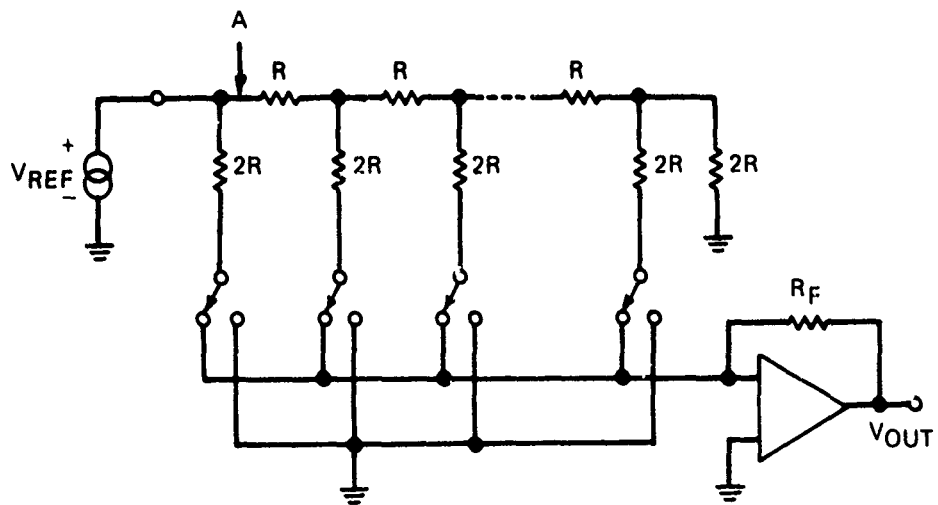
The more standard technique of implementing D/A converters can be divided into the weighted current source, shown in figure 6.3-5, and R-2R ladder shown in figure 6.3-6, and combined weighted current source/R-2R ladder (b) shown in figure 6.3-7. The weighted current source has the advantage of simplicity but the disadvantage of speed reduction and temperature stability for high resolution D/A converters due to the wide range of emitter resistors required. The R-2R ladder implementation has the advantage that only two values of resistors are required but has the disadvantage of requiring area consuming MOS transistor switches for high speed operation.

To achieve the high speed capability of lower resolution converters and the low resistor range required by the R-2R ladder, the two techniques have been combined into the circuit illustrated in figure 6.3-7 preferred for use on the APUP chip. The circuit to be described in more detail in paragraph 7.4 and illustrated in figure 6.3-8 consists of an input buffer and current mirror stage for converting voltage to current, a current source formed by a MOSFET at each line location, a current "tree" consisting of 2 series nonsaturating differential stages using ISL transistors, and a common base stage to provide a simultaneous summing point for the 3 parallel MDAC outputs. The resistors in the R-2R ladder, which are ion implanted to maintain resistor uniformity and matching accuracy, provide an actual voltage which is a weighted function of the analog input. In the current "tree", the sign bit of the digital multiplier coefficient steers all the remaining currents into the proper (+) or (-) resistor ladder.



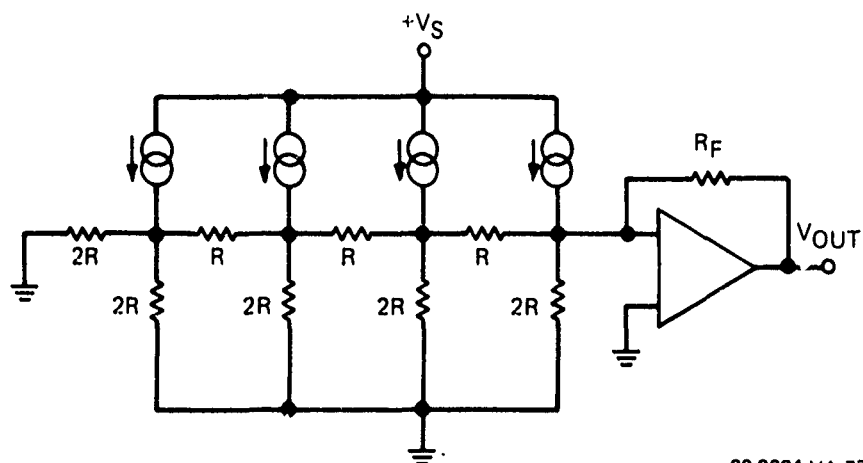
80-0024 VA 75

Figure 6.3-5. Weighted Current Source D/A Converter



80-0024-VA-76

Figure 6.3-6. R-2R Ladder D/A Converter



80-0024-VA-77

Figure 6.3-7. D/A Converter Employing R-2R Ladder with Equal Value Switched Current Sources

The amplitude bits had previously steered the current to the sign bit switches for a "1" or out a common collector bus for a "0". The APUP chip requires 4 resistor ladders and 6 sets of "trees", with each set containing 8 current sources and 8 differential stage/common-base stage structures. Two ladders are used per "trees", one ladder for outputting products with a positive multiplier and the second ladder for negative multiplier products. The analog outputs from each ladder pair are algebraically summed in a 4-stage CCD to form a single analog sum of products.

6.3.2 Comparison of CCMDAC and R-2R Ladder Implementation

6.3.2.1 Weight Matching and Absolute Weight Accuracy

The binary-weighted capacitors used in the CCMDAC implementation involve selecting the smallest reproducible capacitive element as the least significant bit (LSB). Generally, the higher bits consist of large clusters of LSB capacitors so that fabrication uncertainties, such as undercut, affect all capacitors uniformly and area ratios remain constant. The uncertainty in

capacitive matching accuracy therefore becomes proportional to the gradient in dielectric thickness. This effect can be minimized by using a common centroid geometry (7) in which the capacitor elements are symmetrically spaced about a common center point.

The value of each resistor in the ladder of the R-2R MDAC has an uncertainty due to undercut. However, as in the CCMDAC approach mismatches in resistor ratios are compensated out by making the 2R resistor a multiple replica of the R valued resistor. Mismatching them becomes a function of the ion-implanted sheet resistivity uniformity.

Characteristics of the capacitors of the CCMDAC and the resistors of the R-2R ladder implementation are compared in table 6.3-1. If the typical natural matching precision is made analogous to amplitude resolution accuracy, the ion implanted resistors correspond to 58.4 dB resolution while the MOS capacitors give 64.4 dB resolution, which corresponds to nine to ten bits, in excess of the required 8 bits. Furthermore, since circuit element ratios, rather than absolute values, control the MDAC operation, the temperature and voltage coefficients should nominally cancel or compensate.

Absolute weight accuracy is affected if all elements of a binary weighted sequence are not formed from clusters of the entity comprising the LSB. A case in point is where, in order to conserve area, the MSB array does not consist of 2^n repetitions of the element forming the LSB, which is the smallest value capacitor in a CCMDAC implementation. Referring to the MDAC array on the 512 Chirp-Z Transform chip (9), the least significant bit is a .02 pF capacitor with the next significant bit 2 repetitions of the LSB. The next 8 bits are binary multiples of a single 0.08 pF capacitor, which causes an inaccuracy in weight value because of the nonuniform effect of undercut on the first two versus the last eight bits. For a ± 1.5 micron undercut, a $\pm 1/8$ LSB weight inaccuracy is predicted for a 10 resolution bit MDAC. For an 8-bit system, the required $1/2$ LSB weight accuracy corresponds to

TABLE 6.3-1
COMPONENT MATCHING DATA

Component	Fabrication Technique	Matching	Temperature Coefficient	Voltage Coefficient
Resistors	Diffused (W=50 μ)	$\pm 0.4\%$	+2000ppm/ $^{\circ}$ C	-200ppm/V
	Ion-Implanted (W=40 μ)	$\pm 0.12\%$	+400ppm/ $^{\circ}$ C	-800ppm/V
Capacitors	MOS (t _{ox} =0.1 μ L=10 mils)	$\pm 0.06\%$	26ppm/ $^{\circ}$ C	10ppm/V

.195 percent while an inaccuracy of .093 percent would be achieved with .5 μ undercut, which is better than the specification. Weight inaccuracy problems would not be encountered with the R-2R ladder implementation since the 2R resistors will be a multiple of this fundamental unit forming the R resistor.

6.3.2.2 Sensitivity to Nonuniformities

The output of one channel of the Filter/Transform APUP using the "push/pull" sequence (see paragraph 6.1.2) is given by (after suitable buffering)

$$\begin{aligned}
 v^+ - v^- &= kV_{in} C \sum_{i=0}^{n-1} (2^{-i}) (b_i) \quad (\text{MDAC}) \\
 &= kI_O R \sum_{i=0}^{n-1} (2^{-i}) (b_i) \quad (\text{R-2R})
 \end{aligned}$$

where K = gain factor

If a nonuniformity exists in the capacitance values of the CCMDAC array or in the current source and resistor value due to threshold voltage variations or nonuniform etching, the output of each sequence (push/pull) is given by

$$\begin{aligned}
V^+ &= V_{in} \sum_{i=0}^{n-1} \frac{C + \delta C_i}{2^i} b_i \\
&= \sum_{i=0}^{n-1} (+ I_o + \delta I_i) (R + \delta R_i) \frac{1}{2^i} b_i
\end{aligned}$$

$$\begin{aligned}
V^- &= V_{in} \sum_{i=0}^{n-1} \frac{-C + \delta C_i}{2^i} b_i \\
&= \sum_{i=0}^{n-1} (- I_o + \delta I_i) (R + \delta R_i) \frac{1}{2^i} b_i
\end{aligned}$$

where

δC_i = uncertainty in capacitors value of i^{th} location

I_o = signal current

δI_i = bias current at i^{th} bit location

δR_i = uncertainty in resistance at i^{th} location

The push/pull operation performs an effective subtraction of the V^+ and V^- signals which traverse the same path through the MDAC. Therefore, first order nonuniformities should cancel via

$$\begin{aligned}
V^+ - V^- &= kV_{in} C \sum_{i=0}^{n-1} \frac{b_i}{2^i} \quad (\text{CCMDAC}) \\
&= KI_o R \sum_{i=0}^{n-1} \frac{1}{2^i} b_i \quad (\text{R-2R})
\end{aligned}$$

6.3.2.3 Area Comparison

a. CCMDAC:

MDAC:	1000 mil ² (extrapolated from Copeland)
Static Shift Register	$\frac{750 \text{ mil}^2}{1750 \text{ mil}^2}$
6 MDAC's:	10,500 mil ² (for "Capacitive Offset" approach)
	5,250 mil ² (for "Reference Steering" approach)

b. R-2R Ladder

The R/2R ladder MDAC consists of the following elements with the corresponding areas:

<u>No. Required</u>	<u>Designation</u>	<u>Area</u>
6	Multiple Currents Sources	1272
	ISL Logic	2100
9	TREE	340
1	BIAS	126
	Output Buffer	335
		<u>4173 mil²</u>

6.3.2.4 Power Requirements

a. CCMDAC

From extrapolation of data from the Chirp-Z Transform chip description (9), the following power numbers are projected for the APUP CCMDAC's:

Input and Output Buffer:

TI: 16 mw for 17 MHz bandwidth into 20 pF

APUP: Increase bandwidth by 3 to 51 MHz

Decreased Effective Load Capacitance: $1/2 \times 20 = 10$ pF

(Adjustment needed to give equivalence to ISPICE "R-2R" simulation.)

Input + Output Buffer = 2 (buffers) x 3 (bandwidth) x $1/2$ (capacitance) x 16 = 48 mw

For 6 MDAC's = 288 mw

Switching Power: C switch = $1/3$ C signal $\sim \frac{10}{3}$ pFd

F switch = 20 MHz

D switch = $CV^2F = 1.7$ mw

Total Power/CCMADC $\cong 290$ mw

b. R/2R Ladder

Power designation for the R/2R MDAC as determined from ISPICE computer simulations in 34 mw/MDAC. For 6 MDAC's this corresponds to 204 mw, which is comparable to that of the CCMDAC.

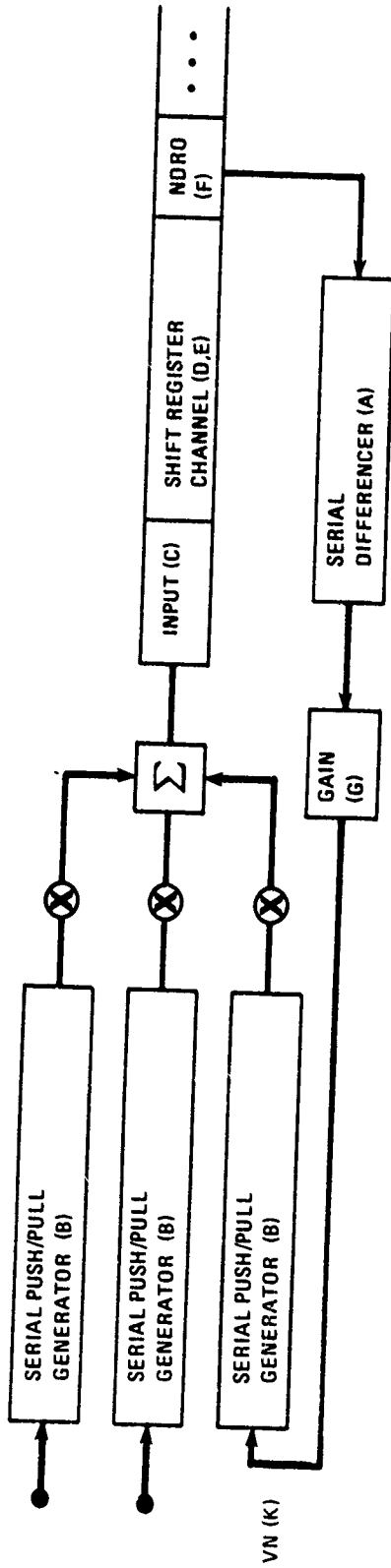
6.3.3 Wideband Buffer Circuits

To meet user requirements, the buffer circuits should be capable of handling the analog signals at the 60-dB quality level for such measures of quality as peak signal to noise, side-lobe

rejection, sample-to-sample isolation, distortion rejection, blemish or fixed pattern rejection, all at the highest frequency consistent with equally good performance in every critical parameter. For example, linear dynamic range is frequently defined as the signal-to-noise ratio (SNR) when the nonlinear distortion (including both harmonics and intermodulation components) equals the temporal or white noise. Thus a buffer circuit which gives very good distortion rejection but has a poor equivalent input noise (NES: noise equivalent signal) is not fully consistent with all the performance criteria. To achieve the desired performance, such a noisy but linear buffer demands larger signal amplitudes. Most often, such a need translates into higher bias and clock voltages, raising the on-chip power consumption and most likely the resultant chip operating temperature which strongly aggravates the blemish and offset nonuniformity on the chip's memory. In addition, the circuitry under consideration brings in the elements of noise for the minimum detectable signal and nonlinear distortion which can generate false Doppler targets via harmonic and intermodulation product frequency components. Thus these items need a more complete definition acceptable to both the system designer/device user and the device designer.

6.3.3.1 Noise and Distortion Performance Limitations

First, consider a detailed breakdown of the various temporal noise constituents the radar signals will encounter as they accumulate with each passage around the loop, schematically pictured in figure 6.3-9, where signal corruption due to device fixed pattern is examined elsewhere. Most of the fixed pattern reduction is achieved by differencing complementary signal samples which have taken identical paths through the memory. Thus, to the extent that these two complementary signal samples contain noise contributions which remain strongly correlated in both samples, such correlated noise will be reduced (along with offset fixed patterns) by the serial differencing operation. A good example of such noise reduction is the low frequency "1/f" type noise of



KEY TO NOISE SOURCE IDENTIFICATION:

- A. NDRO SERIAL DIFFERENCING TAP BUFFERS $(19.9 \text{ E-9 VOLT (Hz)}^{-1/2})$
- B. MDAC PUSH-PULL GENERATOR AND CURRENT COPIES $(54.2 \text{ E-9 VOLT(Hz)}^{-1/2})$
- C. CCD "FILL/SPILL" INPUT WITH 56.42 fFd GIVING $271 \mu\text{v}$. INPUT NOISE
- D. THERMAL LEAKAGE AT $10^{-8} \text{ AMP (cm)}^{-2}$ FOR 10^{-3} SEC IN $16 \mu\text{x}$ $32 \mu\text{G}$ GIVING 18 ELECTRONS NOISE
- E. TRAPPING NOISE, UP TO 87 ELECTRONS
- F. NDRO RESET NOISE (UNITY GAIN GIVES 56.42 fFd WITH $271 \mu\text{v}$ NOISE); NOT PRESENT WITH "INTERNAL NDRO."
- G. HYPOTHETICAL NOISE-FREE GAIN, G (ALL OTHER ELEMENTS ASSUMED UNITY GAIN).

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Figure 6.3-9. Distribution of Dominant Noise Sources in the APUP Signal Loop

the NDRO sensing FET and the associated flicker noise of that initial buffer circuit. For example, when the APUP chip is executing multiplies at the rate of 10^7 per second, the two complementary signal samples pass through this circuit within about 50 nanoseconds of each other. Consequently, slowly changing noise constituents are reduced by at least 40 dB for any frequencies below 31.8 KHz and by at least 20 dB for spectral noise out to 319 kHz. Because this noise cancellation includes virtually all the strong flicker or "1/f" noise of the analog circuits, the numerical values for circuit noise do not include contributions for flicker or "1/f" noise. While postponing the comprehensive treatment of circuit modeling, the resultant noise predictions are included here as expected values in further describing critical performance definitions.

With reference to figure 6.3-9, the corruption of the radar signal with temporal noise can most simply be described without loss of generality if each constituent circuit is adjusted to unity gain and the total noise power added to run the overall noise power grafted onto the signal with each pass around the loop. Now let the key letters of figure 6.3-9 stand for the associated noise voltage; for example, the voltage noise of resetting the CCD input capacitor according to the "fill/spill" technique is given by $(kT/C)^{1/2}$. Since the smallest capacitance likely on an overlying gate NDRO FET is around 56 fFd., the unity gain assumption gives $CIN = 56$ fFd for a CCD input fill/spill noise voltage of 271 microvolts, which is also the noise voltage arising from the reset of the overlying NDRO sensing gate and FET. The thermal leakage noise charge and the trapping noise charge may be converted directly into noise voltage based on the knowledge of the deep buried channel capacitance on which they are sensed, subject to attenuation by the parasitic loading capacitance.

The thermal leakage charge is derived on the assumption of a typical ten nanoamp per $(cm)^2$ leakage current density accumulating

in a 16 micron x 32 micron shift register stage for a typical interpulse period (IPP) of one millisecond. This yields a total of 320 leakage electrons for each such pass through the APUP loop. The resultant 18 noise electrons then develop across the 56 fFd capacitor a noise voltage of 51 microvolts. The bulk channel trapping charge noise is easily extrapolated from previously published results for N-channel CCD's (10), (11) as shown in Table 6.3-2.

TABLE 6.3-2
CCD CHARGE TRAPPING NOISE

<u>Device</u>	<u>Total (μ^2)</u>	<u>Relative</u>	<u>APPROXIMATE Trapping Noise</u>
a. Line Array: 256 stages of 200 μ x 30 μ (2)	1,536,000	3.1629	70 - 370
b. 500 x 500 Area Array: of 20 μ x 30 μ (2)	600,00	1.2355	20 - 80
c. Line Array: 150 stage of 125 μ x 30 μ (1)	562,500	1.1583	20 - 100
d. APUP: cascaded SPS: 1084 = ((4x40) + (8 x 112) + (4x7)) of 16 μ x 28 μ	485,632	1.000	18 - 87 (estimated)

The first three entries of Table 6.3-2 are very closely consistent with the hypothesis that the trapping noise is proportional to the total exposure of the signal charge to probable charge trapping sites, expressed in terms of the total area (or essentially volume) through which the signal charge passes in transit through the memory. Normalizing to the APUP exposure to charge trapping population and averaging over the three preceding devices gives estimated values of 18 to 87 electrons per signal packet. Referenced to the readout capacitance, the 87 trapping noise electrons becomes 247 microvolts.

The remaining and dominant noise contributions come from the wideband buffers used in conjunction with NDRO, serial differencing, and the serial push/pull generator, and MDAC. The first type (A), called AMP6 during circuit modelling, is aimed at the NDRO task and features a minimal size FET yielding an equivalent input spectral noise density of 19.9 nanovolts per root Hertz; while the second type (B) has a very large input FET and features the ability to make multiple analog current copies for use in the MDAC, with an equivalent input spectral noise density of 54.2 nanovolts per root Hertz. Since the basic high speed shift rate for the memory is 40 MHz, (to permit the fundamental multiply rate of 10 MHz), the maximum allowable settling time is about 10 to 12.5 nanosec. to achieve 9 - or 10 - bit amplitude resolution. Thus the needed signal bandwidth is about 88 MHz. But the actual circuits modelled only achieved a 51-MHz signal bandwidth, for which the assumed noise bandwidth may be around 100 MHz. The last projected value is then combined (by the square root) with the spectral noise density to produce the total wideband noise from those buffer circuits: 199 microvolts for (A) and 542 microvolts for (B).

The accumulation of noise during APUP radar signal processing is now more fully described. If VN (K) is the feedback noise voltage after the kth pass through the loop, then

$$(VN(1))^2 = G^2 + 3B^2 + C^2 + D^2 + E^2 + F^2 + A^2) \text{ and}$$

$$(VN(2))^2 = G^2 (1 + G^2) (A^2 + 3B^2 + C^2 + D^2 + E^2 + F^2),$$

$$(VN(3))^2 = G^2 (1 + G^2 + G^4) (A^2 + 3B^2 + C^2 + D^2 + E^2 + F^2),$$

$$(VN(4))^2 = G^2 (1 + G^2 + G^4 + G^6) (A^2 + 3B^2 + C^2 + D^2 + E^2 + F^2),$$

or in general

$$(VN(K))^2 = (A^2 + 3B^2 + C^2 + D^2 + E^2 + F^2) \left(\sum_{J=1}^K G^{2J} \right)$$

Since proper operation of the APUP correlation transform, recursive filter, or accumulator/PDI dictates unity loop gain ($G=1$) with the MDAC providing feedback coefficients less than one, the feedback accumulated noise becomes

$$(VN(K))^2 = (K) \cdot (A^2 + 3B^2 + C^2 + D^2 + E^2 + F^2)$$

On the other hand, the desired coherent signal voltage (not power) reinforces itself coherently with each pass through the loop, yielding an always improving ratio of signal power to noise power increasing in direct relation to the number of transform points or passes through the loop. More importantly all the noise power associated with the APUP signal processing loop adds directly to the circulating noise and signal build-up as follows:

$A = 199 \mu V$	$D = 51 \mu V$
$B = 542 \mu V$	$E = 247 \mu V$
$C = 271 \mu V$	$F = 271 \mu V$

to give $(A^2 + 3B^2 + C^2 + D^2 + E^2 + F^2)^{1/2} = 1063 \mu V$ or -59.5 dBV, where dBV is used to indicate the power level relative to one volt rms as zero dBV.

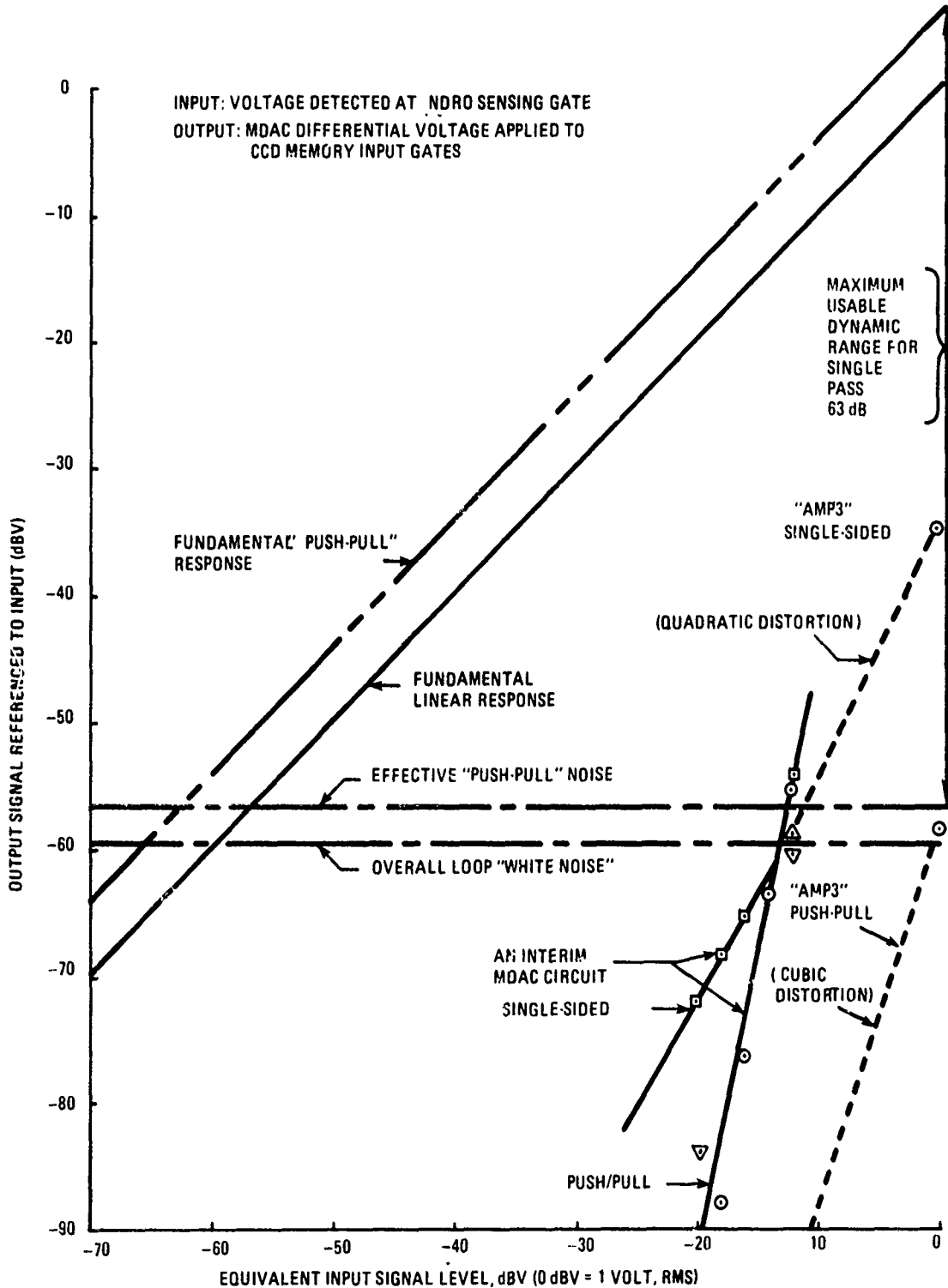
Having treated the APUP processing loop noise, the next performance measure needing definition is nonlinear distortion. An illustrative example of nonlinearity problems in radar signal processing is the simultaneous occurrence of at least two very strong Doppler frequencies, such as ground clutter and a closing attacker at a decidedly higher frequency. Therefore the best measure of performance not only is closely analogous to this situation but is also easy to instrument and yields results that are directly related to the deleterious effects in the actual radar system. Any non-linearity in the transfer characteristic of a radar signal processor has the effect of acting as a frequency mixer in the presence of multiple Doppler tones, thereby generating harmonics and intermodulation cross-products in the output spectrum. Such spurious harmonic and intermodulation spectra are immediately obvious when a radar processor output is

monitored on a spectrum analyzer as two sinusoids are fed to the input to simulate simultaneous Doppler targets. When the spurious spectra become detectable above the processor noise as the amplitude of the input signal is varied, that output signal arising solely from processor nonlinearities becomes a "false target" response. The input level corresponding to the onset of such false targets is most often used as the definition of "maximum usable dynamic range", and is clearly shown in figure 6.3-10.

Figure 6.3-10 describes the behavior of the complete circuit from the NDRO sensing gate of the CCD analog memory through serial differencing, serial push/pull generation, and MDAC current copies and steering with differential readout applied to the CCD analog memory input gates. Shown with a dotted line are the results of an interim MDAC circuit (figure 6.3-11) configured for modelling both the single-sided and push/pull techniques.

The circuit shown in figure 6.3-12, using push/pull operation, extends the maximum usable dynamic range to 63 dB because of the cancellation of "even power" distortion contributions by means of the push/pull subtraction. The circuit of figure 6.3-11 shows a maximum usable dynamic range of only 47 dB because higher power harmonics (namely the fifth power) appeared to dominate prematurely.

The technique of examining nonlinearities by means of applying two sinusoids and looking for harmonic and intermodulation terms is also easy to execute when using such computer modelling algorithms as ISPIICE or MSINC. Each modelling routine provides for the Fourier analysis of the response of the circuit to an arbitrary applied waveform. The key ingredients of the approach are highlighted in table 6.3-3, where the input is specified to be a fundamental sinusoid summed with its K^{th} harmonic, while the transfer characteristic is assumed to take the form of a power series expansion. In computer simulation of circuit non-linearity, the fundamental sinusoid and all the harmonics of interest should ideally fall within a flat frequency response



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Figure 6.3-10. Circuit Transfer Characteristics Limitation

TABLE 6.3-3

FOURIER ANALYSIS FOCUSES ON NONLINEAR DISTORTION

Input Waveform: $X = A \sin(2\pi ft) + B \sin(2\pi kft)$ where $k = \text{integer}$

Transfer Characteristic: Output = $Y = C(0) + C(1)X + C(2)X^2 + C(3)X^3 + C(4)X^4 + \dots$

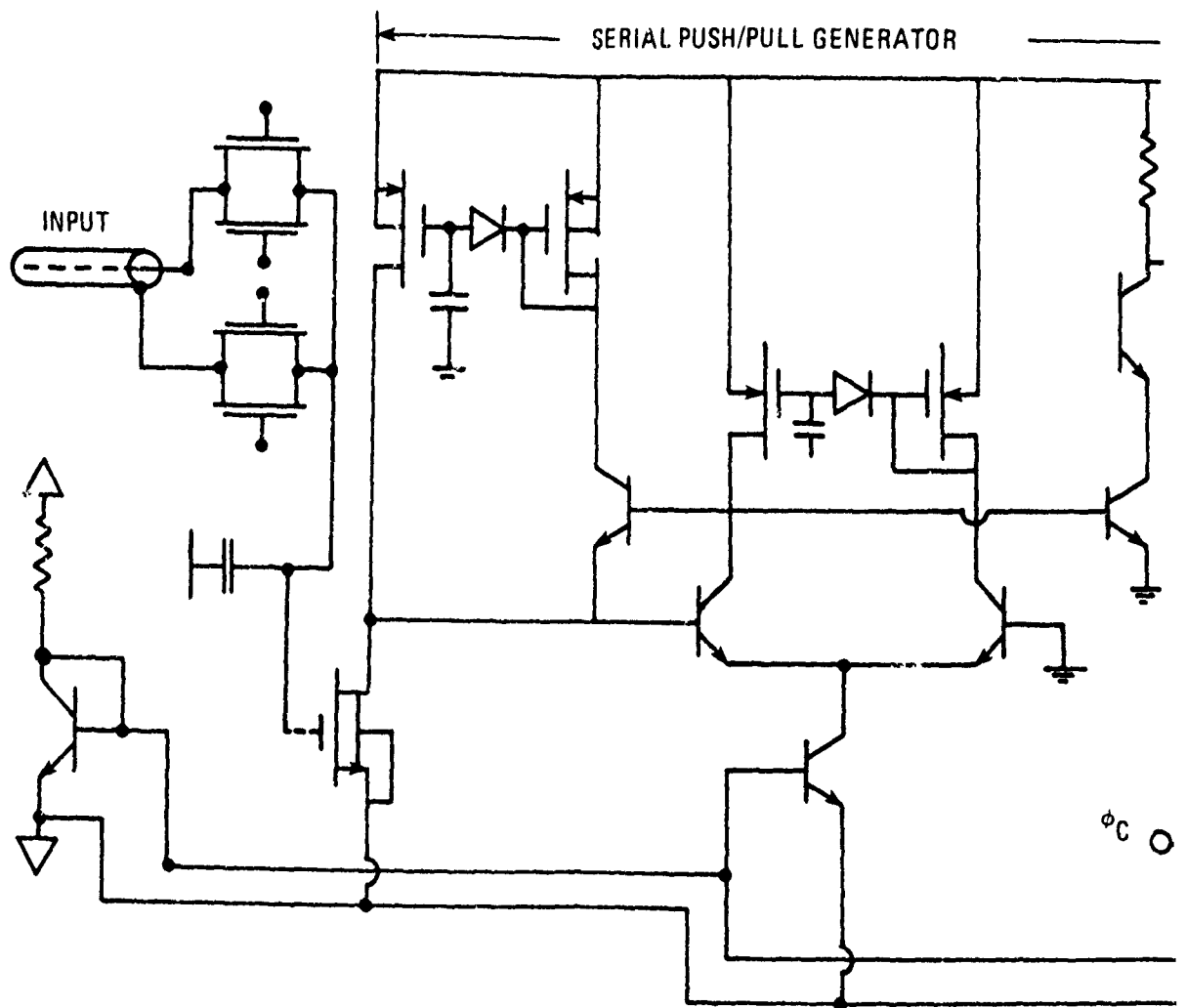
Output Spectral Constituents:

Exponent In Transfer Characteristic Power Series	Associated Spectral Lines
1 (linear)	1, k
2 (quadratic)	2, 2k, $k \pm 1$
3 (cubic)	3, 3k, $k \pm 2$, $2k \pm 1$
4 (quartic)	4, 4k, $k \pm 3$, $2(k \pm 2)$, $3k \pm 1$

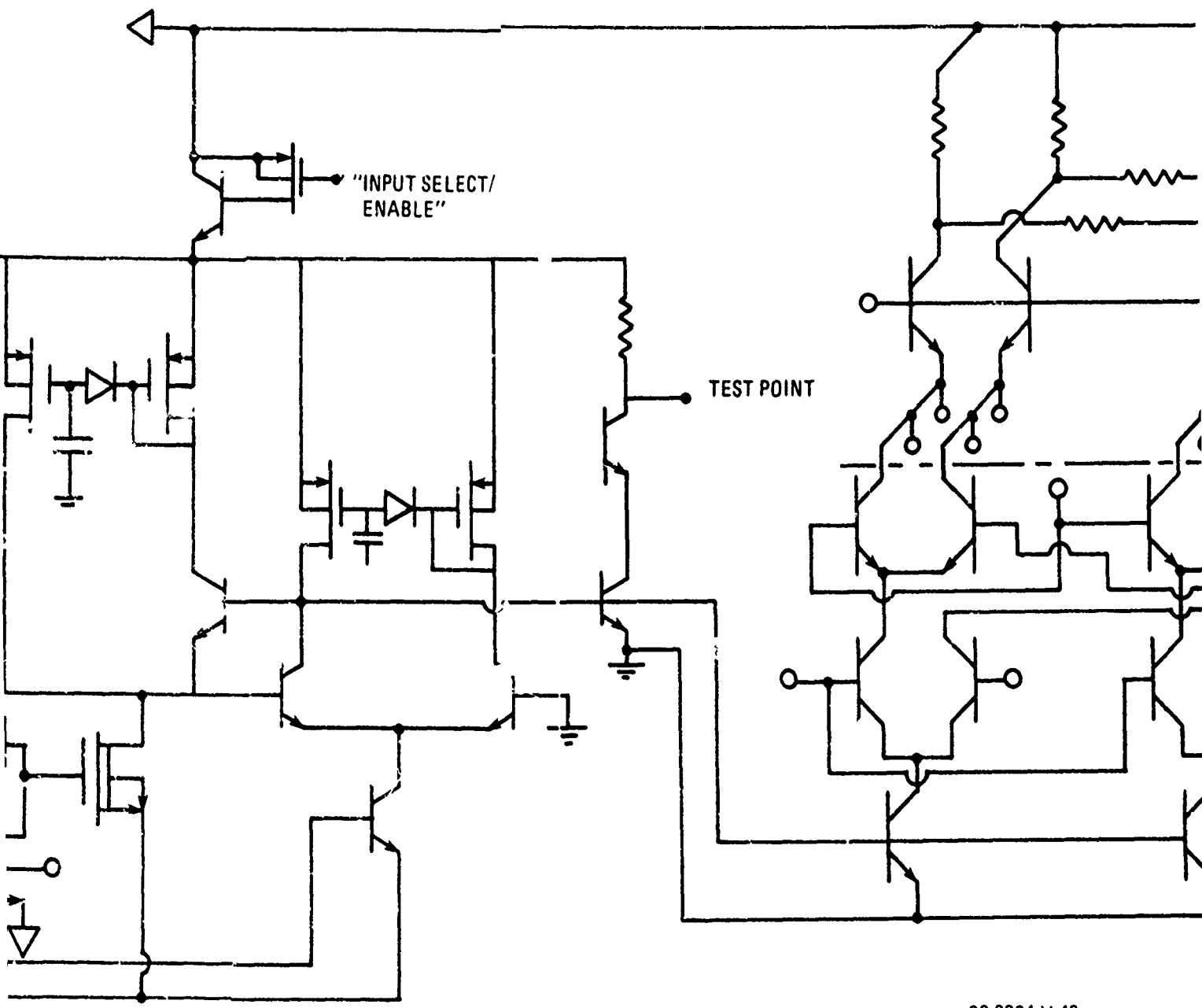
Illustrative Example ($k = 6$):

Harmonic Component Index	Input Amplitude	Output Amplitude	Lowest Exponent Contributor
1	A	y (1,A)	one
2		y (2,A)	two
3		z (3,A)	three
4		z (B-2A)	three
5		y (B-A)	two
6	B	y (1,B)	one
7		y (B+A)	two
8		z (B+2A)	three
9			four
10			four
11		z (2B--A)	three
12		y (2,B)	two
13		z (2B+A)	three
14			four
15			five
16			five
17			four
18		z (3,B)	three
19			four
20			five

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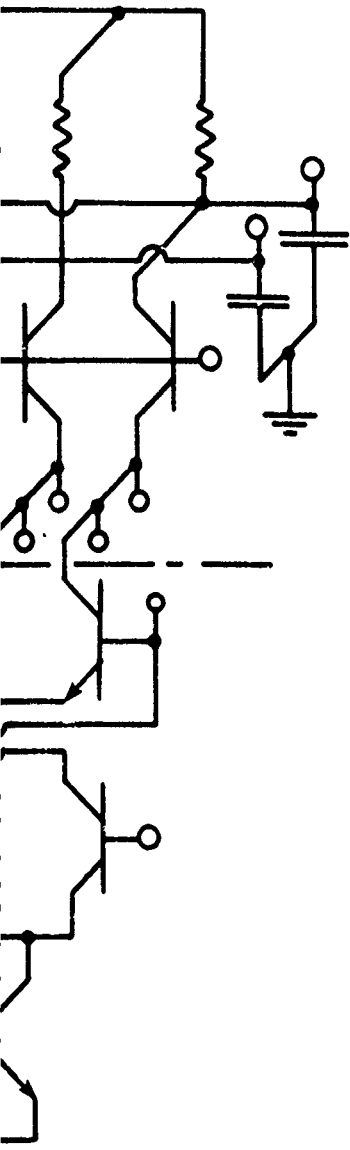
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Figure 6.3-11. An Early APUP Trial Circuit

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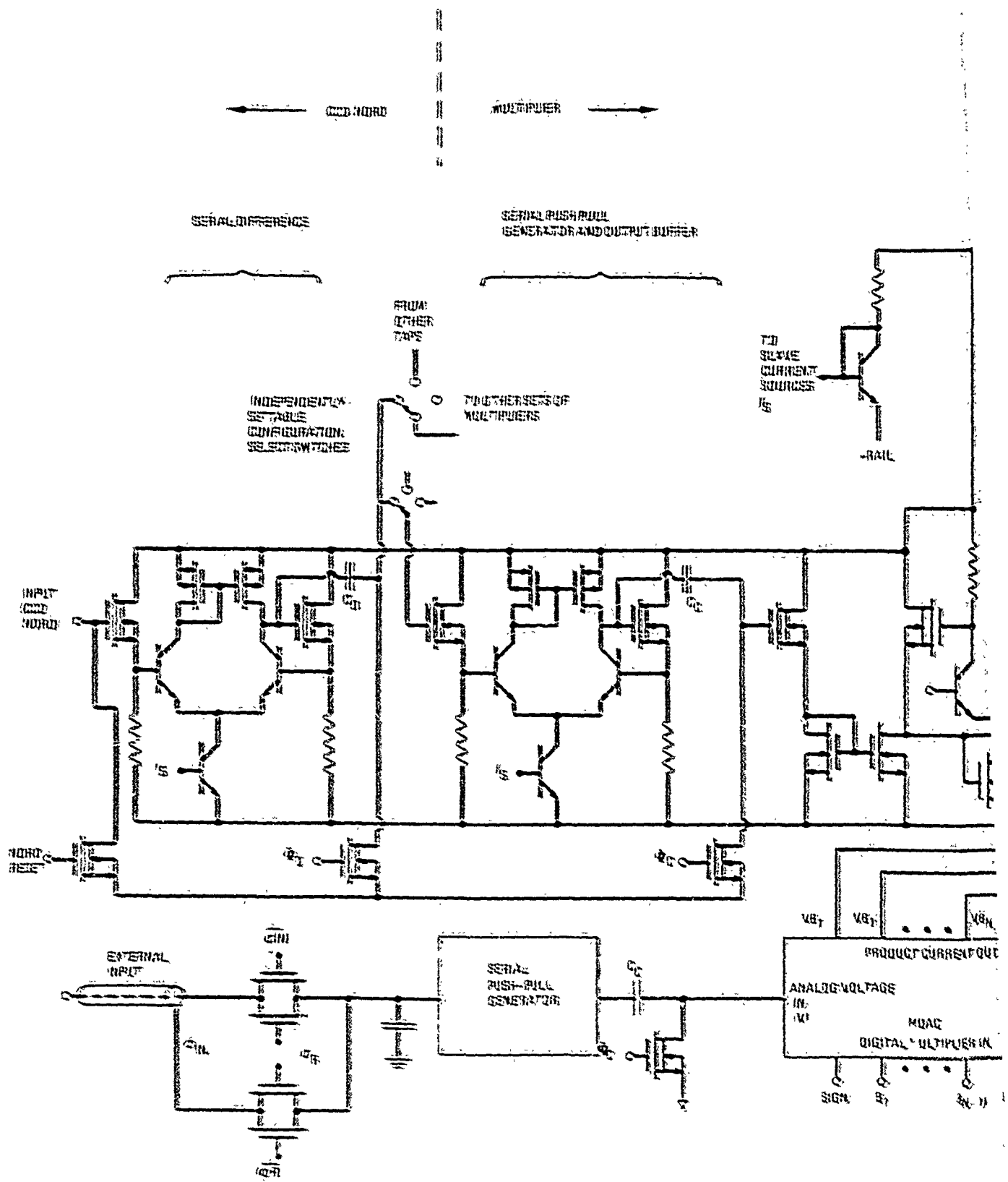


Figure 6.3-12. Analog Circ

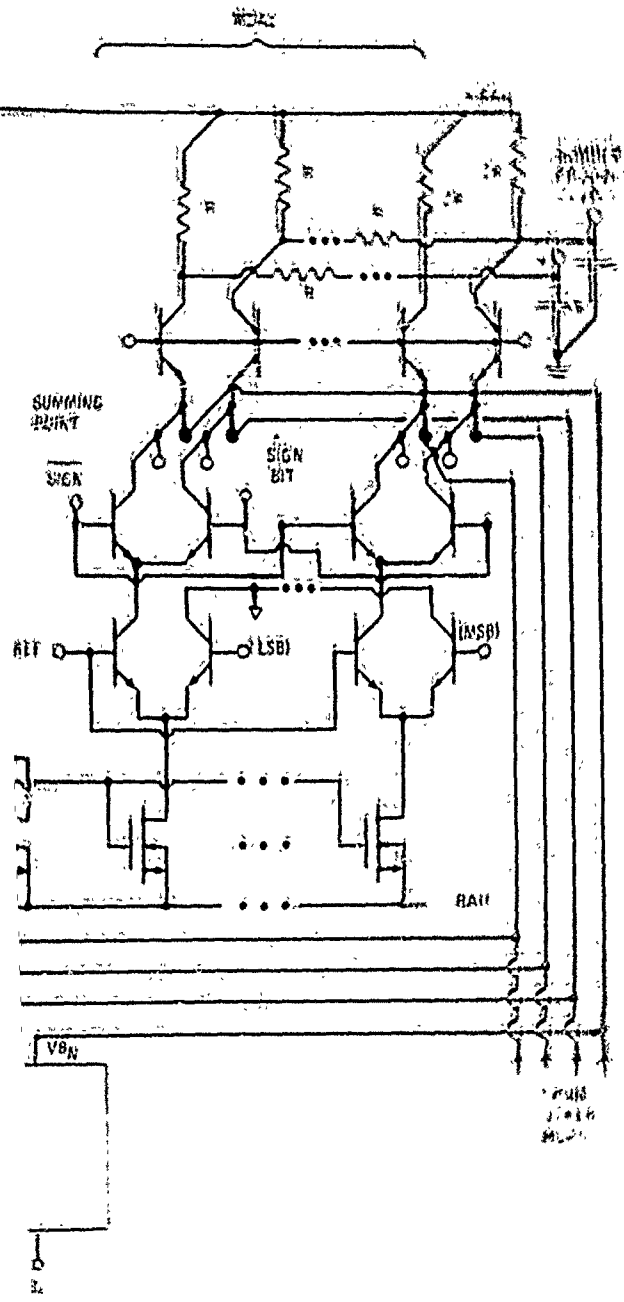


FIG. 2. Details of the transformer ADC.

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region of the circuit to guarantee that the distortion component Fourier coefficients do not unintentionally incorporate some frequency selective spurious attenuation peculiar to the computer model (such as a parasitic RC combination) which might skew the spectral distribution. The distortion curves of figure 6.3-10 are based on summing the harmonic power in the harmonics labelled with y and z and comparing that with the output power at the A and B harmonics for the cases where the complete serial-differencer circuit was modelled in both single-sided and push/pull arrangements. For the latter improved circuits, quadratic terms (y) seemed to dominate single-sided operation.

6.3.3.2 Summing Points Operation

For both the Transform and Filter configurations, the outputs of the MDAC's must be simultaneously summed. For the CCMDAC the output of each MDAC is a charge which therefore requires a high speed (20 MHz) charge-to-voltage summer. One technique is to use a capacitor in a feedback loop of an operational amplifier with a reset switch around the capacitor. ISL/MOS technology would be employed to minimize area and power which maximizing bandwidth.

The R-2R implementation of the MDAC's has employed a common base stage for the current outputs of each "tree" to perform simultaneous current summing at a 20-MHz rate. ISPICE simulations of the MDAC indicate no noticeable loss of linearity and dynamic range by the summing operation.

6.4 REFERENCES

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7. TECHNICAL APPROACH

7.1 APPLICATIONS AND THEIR DESIGN IMPACT

7.1.1 APUP Position in Data Flow Path

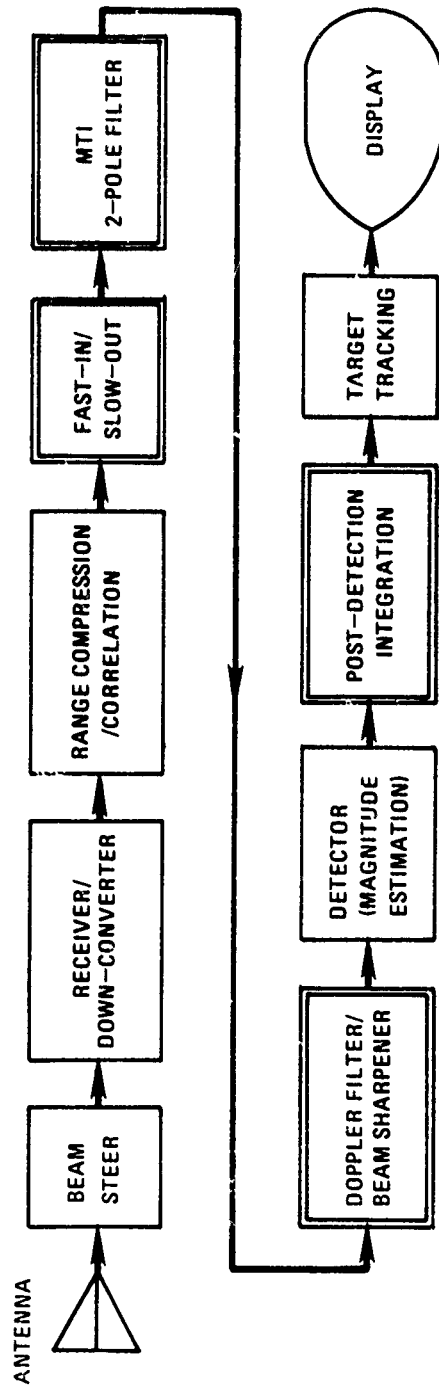
Analog signal processing in a modern radar fits in the receiver portion after the RF and before the data processing/display. Figure 7.1-1 shows the receiver major component chain with four potential APUP applications shown in the double-bordered boxes.

After the antenna and beam-steering hardware, we have the down-converter to a low IF. For a coded or chirped transmission, a range compressor or correlator is required, either as a SAW device at RF or as a dispersive chirp filter or CZT at IF.

An APUP can function next as a fast read-in/slow read-out analog storage to spread the range data in time to fill the inter-pulse period (IPP), if required for slower processing equipments. This APUP application is simplified by having no need to change multiplier coefficients; it takes the sampled data straight in with constant gain.

Next comes the clutter canceller or MTI filter, if needed. This can be of a 1- or 2-pole form. Conventionally, a feed-forward or finite impulse response (FIR) form is used for a 2- or 3-pulse MTI, requiring the "dwell" on a target to be 1 or 2 pulses longer than the useful output in order to "load" the filter. A feed-backward or infinite impulse response (IIR) form may be incorporated into the basic FIR MTI configuration for "notch" shaping. The APUP configuration will have all these forms available.

Doppler filtering often follows (or replaces) the clutter canceller. Conventionally, the range-ordered output of the sequential samples is stored in a memory for the entire "dwell".



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Figure 7.1-1. APUP Application Areas in a Radar Receiver

This memory is then read out into the doppler analyzer in a "corner-turned" order, i.e., all samples of one range cell are read out in pulse sequence, followed by all samples of the next range cell, etc. The doppler analysis may be done in various ways: optically or acoustically by diffraction pattern detection, digitally in a fast Fourier transform (FFT), or in a discrete Fourier transform. The signal should be in I and Q form or on a low IF for approach/recede differentiation.

The APUP method, however, eliminates the need for a "corner-turn" memory - it performs the analysis as it goes along in the form of a range-oriented integrate-and-dump (1-pole) filter for one Doppler frequency. Furthermore, APUP can time share the process to accumulate multiple dopplers for all range cells, limited in practice by the maximum APUP speed and the desired range resolution.

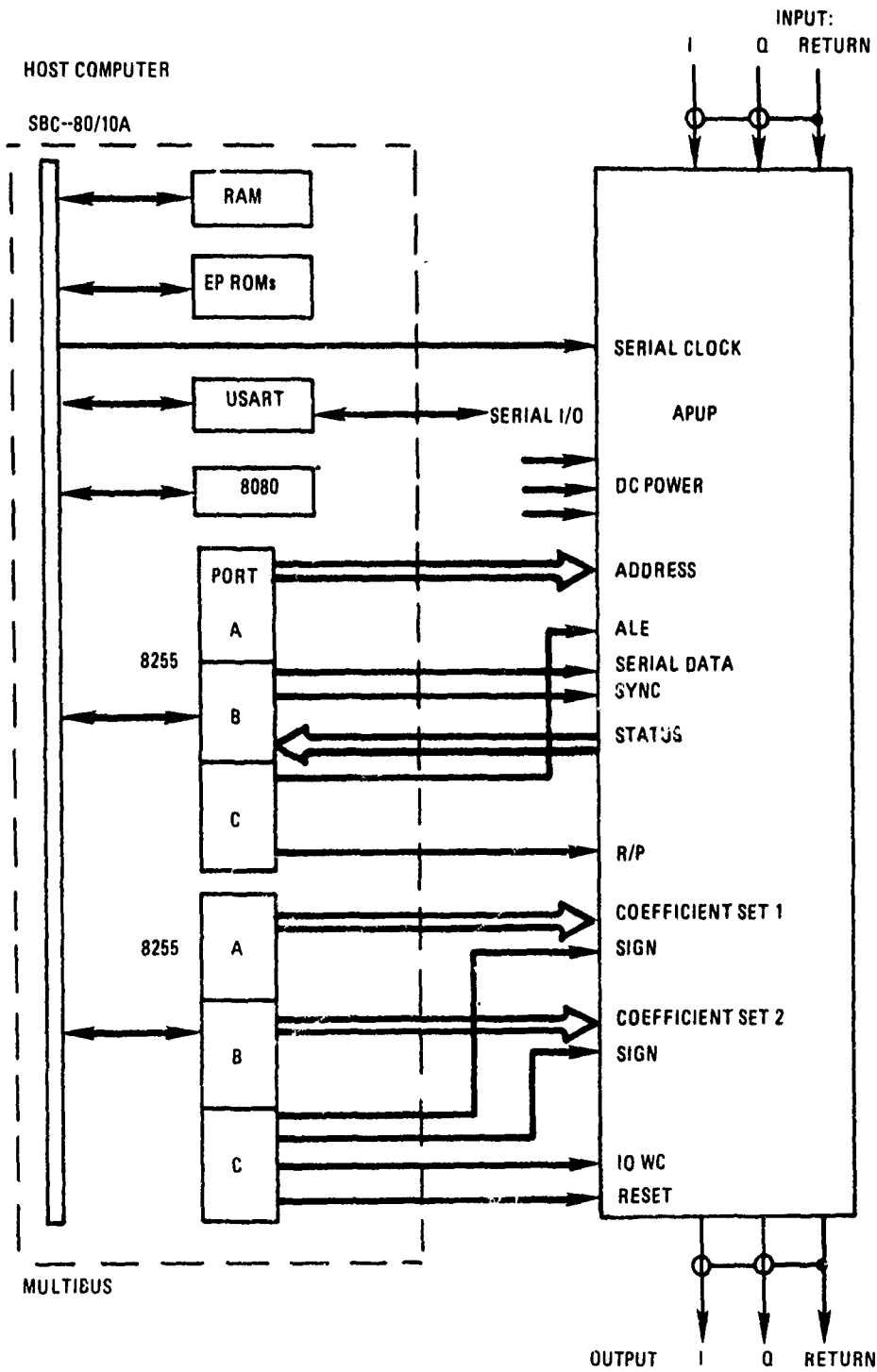
Following the doppler filters is the detector or magnitude estimator using the I and Q outputs. Usually the magnitude is computed by an approximation algorithm such as $I + 1/2 Q$ or $1/2 I + Q$ rather than by using the Pythagorean formula.

The APUP in its 1-pole recursive filter (IIR) configuration can find use as a post-detection integrator. Its retention time, however, is inadequate to serve accurately in a target tracking function.

7.1.2 APUP/System Host Interface

The APUP configuration and digital coefficient control will originate within the "host" computer which is controlling the radar system and processing the data. The APUP performs simply as another peripheral device in the system with no "intelligent" decision-making capabilities within itself.

In the demonstration system, the APUP itself will be interfaced to an Intel SBC 80/10A, a single-board microcomputer with 48 parallel output lines available. This interface is sketched in figure 7.1-2.



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Figure 7.1-2. APUP/Host Computer Interface

The control and coefficient data lines will use the parallel outputs of the two 3-port 8255 peripheral controller IC's on the SBC-80/10A. These have TTL-compatible signals with open-collector outputs which will drive MOS satisfactorily. While there is a serial port on the host computer, it is designed for teletypewriter usage and will not be connected to the APUP.

This host computer demonstration of APUP will illustrate the programmability features but not the speed of reconfiguration. The 80/10A sets up the parallel output words for each port of each 8255 sequentially, and it takes several instruction cycles for each such output. In field use, the APUP's can expect to work from a faster host computer, particularly in regard to coefficient transfer.

7.1.3 APUP Testability

The APUP does not lend itself to appreciable "built-in test" (BIT). Its functions will require standard laboratory signal generators and oscilloscopes for I/O tests plus the means to set the configuration and to enter the coefficients, initially by switches and later by the host computer once its program is debugged.

The APUP mask set will be partitioned to permit functional tests by component section during the wafer test phase.

The completed APUP can be evaluated in a series of tests. After reset (all coefficients zeroed), it must be configured, of course. The first check is to enter ones in the second coefficient set and see if the input is connected to the output. If so, then the CCD clocks can be started and the output examined for "empty" noise.

A one in the first coefficient of the first multiplier set will connect the input to the CCD analog memory. With all ones entering the APUP, the output can be checked and the taps reconfigured to check for signal passage.

Next, the recirculation path can be closed and the noise build-up or "build-down" effect observed after the memory has been either cleared or loaded with ones, respectively. This will give

an initial indication of transfer efficiency and the presence of blemishes or dark current.

If the APUP is apparently functional, the quality of its memory can be checked by the total harmonic distortion increase of a sinewave passed through the memory as a delay line. The THD measurements for all tap settings can isolate sections with poor performance. Tests with various amplitudes and dc offsets can give a measure of the dynamic range.

The transfer inefficiency and fixed charge losses in the analog memory are conventionally checked by entering a set burst of ones and observing their distortion after a fixed number of transfers or, in the case of APUP, at each output tap. Sometimes two bursts are used and the spacing (number of zeroes) between them is varied to yield more information (like trapping) about the CCD analog memory.

To test the MDAC's we first load the digital multiplier coefficients from a counter which is incremented once per coefficient. With a steady analog input, the output of the APUP should be a sawtooth as the multiplier builds up, overflows, and restarts its ramping action. Linearity better than 30 dB may be hard to quantify from a scope observation of such a sawtooth. However, if a sine/cos ROM replaces the counter as the multiplier coefficient source, the THD of the APUP sinewave output is extremely sensitive to device nonlinearities and better characterizes the multiplier linearity.

Continuing the harmonic measurement method, if the multiplier received sinusoidal coefficients of one frequency while the analog input received a sinewave input of another frequency, the spurious harmonics (other than sum and difference frequencies) from this true mixer, as seen on a spectrum analyzer, would be a good measure of the system linearity.

7.2 TOPOLOGY OF THE MONOLITHIC CHIP

The IC chip area will be partitioned according to function as much as is practical. This will aid in probe testing of the sections so that design faults can be localized more rapidly and mask corrections made. Partitioning will also expedite production testing of wafers although the form of partitioning will undoubtedly change when APUP gets to the production stage.

7.2.1 Partitioning for Fault Isolation/Development Testing

7.2.1.1 Test Cells

When the mask set is designed, it will include "test cells" representative of the ISL, CMOS, and CCD driver circuitry. These test cells will be external to the active circuit area and will constitute a subarray on each die. These test cells will allow rapid probing of each type of circuitry to ascertain its operability. Since the test cells are an integral part of each die pattern on the wafer, any misalignment in the step-and-repeat processing which causes a malfunction of a test cell is indicative of a failure on the die containing it. Successful performance of all test cells, however, cannot guarantee operation of the other die circuitry but it goes a long way toward giving confidence that other circuitry is good.

With the large chip size and the numerous I/O bonding pads already required by the APUP circuitry, there may be little active area to denote to test cells and their probing pads since theirs is a one-time usage. One solution to be explored is to position the test cells outside the scribing area of the die. Then, after the initial wafer probing, the test cells will be discarded when the wafer is diced.

The test cell area may include a separate "test clock driver" linked by polysilicon to an APUP CCD. The output of this CCD must be available as a test point. In this way, one of the major items on each die may be tested without the more-elaborate signal input required of the full APUP test. Once the CCD has passed its wafer probe test, the test clock driver lines will be scribed away along

with the rest of the test cell area. Careful attention to such "built-in test equipment" (BITE) may permit probe-test of a large portion of the APUP-proper circuitry at the wafer stage without the dangers of extensive mechanical probing.

Once this test cell stage is passed, the likelihood of die operation is high enough to justify mounting the die in a DIP package and setting it aside (open cover) for the next stage of checkout.

7.2.1.2 Probe Test

The wafer probe test is a delicate bit of work with micro-manipulated needle probes to make temporary contact with the bonding pads and test point pads on each die. The probes apply dc power plus ac clock and input waveforms to the circuitry and similarly provide outputs to an oscilloscope. This stage of testing is indeed no more than an "alive or dead" check.

The mounted chip in a package presents a much easier test situation. The majority of signals can be brought in and out via the package pins. Only a few on-board test pads need be probed to complete the "alive-or-dead" chip testing.

The chip exerciser will provide simple signals to energize all functions of the circuitry but no attempt will be made to verify the signal processing speed or performance. This will come later when the APUP is tied to the host computer. The probe test equipment must include some dedicated signal generation hardware, but the majority of it will be standard laboratory equipment tied onto the micromanipulator needles.

7.2.1.3 Order of Circuit Testing

The wafer tests will proceed from simple basic "service" portions to the more complex arithmetic functions.

The initial test will detect shorts or opens. This dc short test will be followed by a functional test with the clock driver circuitry operated at reduced speed.

The inputs may be of various sorts. For the MDAC coefficients, dc levels for binary ones and zeroes are entered. The bus addresses are also generated on a binary-switched basis. Signals can be variable dc or pulses, the pulses being of various amplitudes, durations, and repetition rates, depending on the feature being checked.

The probing will proceed through the multifarious circuit types. After the clock and waveform driver circuits are verified, the CMOS configuration paths will be tried. The PCCD operation can then be observed. The ISL digital data circuits are next, and finally the MDAC operation may be tested. Beside the PCCD, the MDAC is the most critical element type but it requires the other functions before all input types (analog and digital) can be applied to it and a significant output measured.

7.2.1.4 Partitioning or "Hybrid" Packaging

If the monolithic die pattern lends itself to partitioning, the initial APUP fabrication may best be laid out as a hybrid package of "modular dice". The concept of modular dice offers the possibility of interchanging modules (or "sub-dice") to achieve a higher yield. Figure 7.2-1 illustrates this concept.

The solid lines are the die scribe lines. Line A-A' is the test area boundary. A diamond cut along this line severs the polysilicon connections from the test driver to the PCCD included in the wafer probe test.

In addition, each die may be scribed along lines B-B' and/or C-C'. If a blotch in the process wipes out one quadrant of the die, annexing the required portion from another die during packaging may salvage a whole chip whereas two chips would be destroyed otherwise. Note that the interconnection paths are widened as they cross the quadrant boundaries. This can permit compression-bonding interconnects between the two salvaged portions providing the cut lines of each can be sufficiently aligned within the chip mounting area of the IC package.

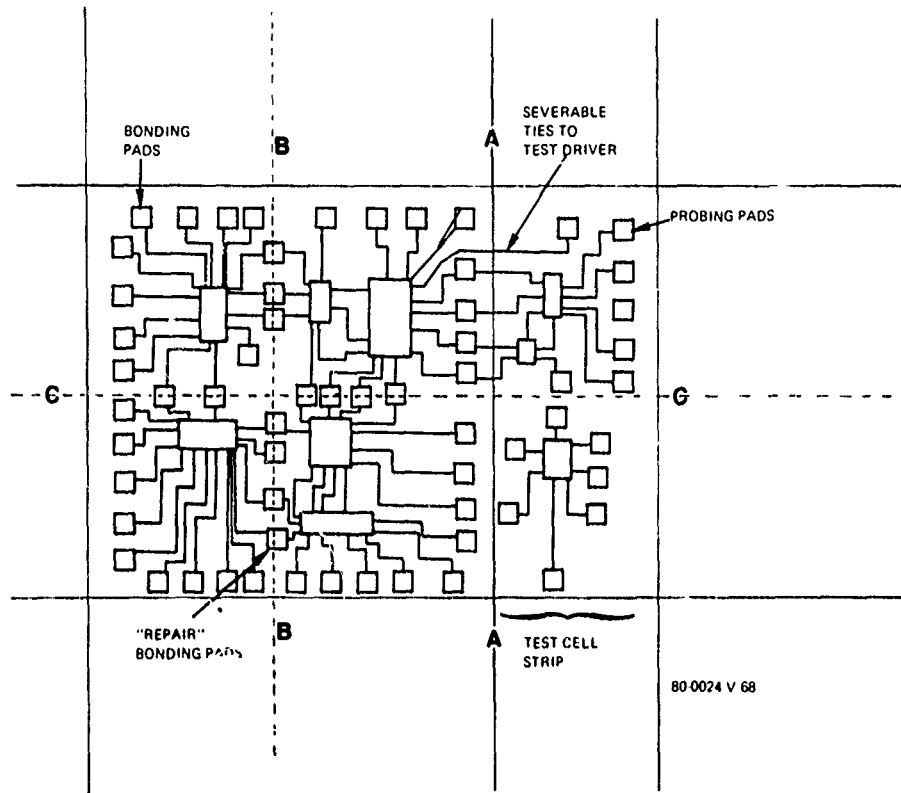


Figure 7.2-1. Die Partitioning Concept

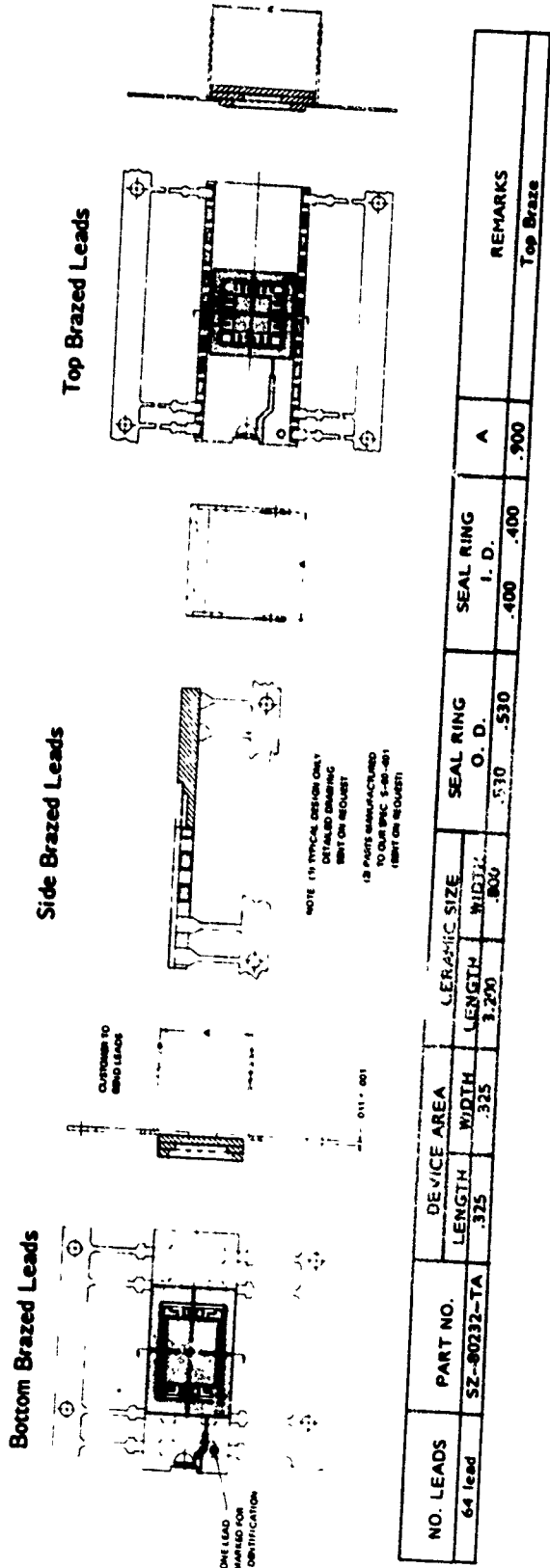
7.2.2 IC Hardware Mounting and Pin-Out

7.2.2.1 IC Packaging

The APUP monolithic integrated circuit will be mounted in a 64-lead Dual In-Line package similar to that shown in figure 7.2-2. In a production version this may be compacted into a rectangular "flatpack" but the "breadboard" demonstrator form is best handled in a standard DIP. The 64-lead size will be required in order to bring out buffered test points for operational monitoring. Also, the chip mounting area is larger and may be required in the initial models.

7.2.2.2 Pin Assignments

The signal and control line assignments cannot be made to specific pin numbers until the die pattern is finalized. However, the types of signals required can be listed now and the lead count anticipated. Table 7.2-1 gives the lead designations and quantity.



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Figure 7.2-2. Multilayer Ceramic Dual-In-Line Packages

TABLE 7.2-1
APUP I/O PIN REQUIREMENTS

<u>Pin Name</u>	<u>Signal Designation</u>	<u>Pin Count</u>
GND	Ground	1
Vcc ₁	+2.0 volts	1
Vcc ₂	+5.0 volts	1
V _{ee}	-3.2 volts	1
V _{dd}	-12.0 volts	1
SC	Serial Clock	1
PC	Parallel Clock	1
IOWC	Input/Output Write Clock	1
AO-A7	Address, Command/Coefficient	8
ALE	Address Latch Enable	1
B0-B7	Configuration Status word (bidirectional bus)	8
C0-C8	Coefficient Data	9
D0-D8	Coefficient Data	9
\bar{W}	Write/Coefficient Data	1
\bar{R}/P	Run/Program (configure)	1
I ₁	In-phase Input (analog)	1
Q ₁	Quadrature Input (analog)	1
R ₁	Signal Return-Input	1
I ₂	In phase Output (analog)	1
Q ₂	Quadrature Output (analog)	1
R ₂	Signal Return - Output	1
RESET	Initial clear	1
T0-Tx	Test Points (undesignated yet)	<u>x</u>
	Pin Count	52 + x

A single pin is labeled GND (ground). Actually, this is the dc common point for the power supplies. The R_1 and R_2 signal input and output returns function as the "grounds" for the single-ended analog data circuits. These returns are at dc ground potential but are carried as separate signal paths to minimize "common-mode" noise.

The dc voltages listed may not all be required but are shown as the likely candidates needed by the various circuit types (bipolar, CMOS, ISL, PCCD, etc) before the design is firm. Similarly, both serial and parallel clock inputs are shown. The parallel clock may be generated on-chip by dividers but also independent control of parallel transfers may look desirable as the design progresses. The I/O Write Clock is an external control command for entering or removing data.

The address data are handled in parallel. Speed may not be required when they are used to direct reconfiguration commands but serial entry will NOT keep up with coefficient routing during the "run" operations. Likewise, the coefficient data words are entered in parallel. Reconfiguration commands will be entered serially (data plus "clock") since reconfigurations of the processing components will not occur during data processing, yet we need an output port for status information during the processing. Port B is bidirectional and will be used for this status output after reconfiguration input while ports C and D fire in weighting coefficient changes during real-time adaptive processing.

The \bar{W} and \bar{R}/P lines enable coefficient writing and changing from "run" to "program" (reconfiguring) mode, respectively. In run mode, port B is always outputting the Status word regardless of the Address lines.

Provision is made for both I and Q analog signals in and out.

The PESET line performs the housekeeping function of clearing all coefficient registers. It may also revert the configuration to the most commonly called process, say, fast-in data storage.

The buffered test points are not designated at this stage, but the pin count has already exceeded 40. In a final design no test points would be called and it's unlikely that more than 5 address lines (32 points) will be actually needed, but a 64-pin package may still be required.

7.3 THE ANALOG MEMORY

Recalling from the section on analog memory problems, the two major sources of corruption of the analog data are blemishes and offset nonuniformities as well as sample-to-sample crosstalk, both of which are aggravated by repeated passes through the signal processing loop. Push/pull operation greatly reduces the first problem as well as the problem of harmonic distortion, while the additive refresh technique greatly diminishes the latter problem. In the discussion of the problem and the development of a solution, various examples were given and are summarized in table 7.3-1. Item (1) of table 3.3-1 is a cascade of smaller SPS blocks, each with 32 columns and with the following heights: 32, 32, 64, 128. Since each analog sample moves through the memory as a coupled pair of push/pull or complementary charge packets in the manner shown in figures 6-12 and 6-13, each horizontal input/output register for the SPS blocks is 64-stages long. Thus, in the absence of additive refresh, each analog sample experiences 256 stage transfers in both the vertical and horizontal direction. In memory item 2 of the table 7.3-1, additive refreshing is built in only at the taps between the SPS subarrays. Now each SPS subarray resembles that illustrated in figure 6-4, except no additive refresh cells are located within the subarray. Each subarray has 100-stage input/output registers with 25 active columns (or 50 for max data mode), and the heights of the subarrays are 40, 40, 80, 160 rows. Finally for items (3), (4), and (5) each subarray exactly resembles that of figure 6-4. For both items (3) and (4), the target isolation was set around 90 dB to permit such applications as 32-point Doppler transform with several filters multiplexed onto one APUP chip yet maintaining crosstalk to below -55 dB to -60 dB. Item (3) was optimized for 4 taps while item (4) was optimized for 8 taps. Because of the aspect ratio of these memories (i.e., few columns but many rows) the vertical clock rates are rather high, thereby causing substantial power consumption in the clock drivers for the main memory capacitance.

TABLE 7.3-1

EXAMPLES OF SAMPLE-TO-SAMPLE ISOLATION IN ANALOG MEMORIES

ITEM	MEMORY SHAPE/SIZE	NO. OF TAPS	VERTICAL		HORIZONTAL REFRESH PERIODICITY	MULTIPLICITY	VERTICAL REFRESH PERIODICITY	MULTIPLICITY	RESULTANT ISOLATION	
			CLOCK FREQUENCY	FREQUENCY					HORIZONTAL	VERTICAL
1	(64/2)(32)(8)	4	1.25 MHz	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	69.7 dB	69.7 dB
2	(10 ⁴)(40)(8)	4	1.6 MHz	40 STAGES	4	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	74.1 dB	75.4 dB
3	(40/4)(112)(8) (HIGH ACCURACY MODE)	4	4.0 MHz	40 STAGES (PLUS IN BOTTOM SPS ROW)	4	8 STAGES	112	8 STAGES	90.1 dB	90.1 dB
4	(40/2)(112)(8) (MAX. DATA MODE)	4	2.0 MHz	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	77.9 dB	47.9 dB
	(24/4)(128)(128) (HIGH ACCURACY MODE)	8	6.7 MHz	24 STAGES (PLUS IN BOTTOM SPS ROW)	8	4 STAGES	384	4 STAGES	93.1 dB	92.8 dB
	(24/2)(12)(128) (MAX. DATA MODE)	8	3.3 MHz	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	74.7 dB	38.6 dB
5	(60/4)(68)(8) (HIGH ACCURACY MODE)	4	2.7 MHz	60 STAGES (PLUS IN BOTTOM SPS ROW)	4	17 STAGES	32	17 STAGES	83.0 dB	87.2 dB
	(60/2)(68)(8) (MAX. DATA MODE)	4	1.3 MHz	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	(NO REFRESH)	70.8 dB	56.6 dB

(NOTE: The calculations in the power budget tabulation assume a memory like that of item (3) of table 7.3-1.) When the memories of items (3) and (4) are used in the maximum data handling mode, the isolation between samples degrades to 48 dB for the case of 4-taps (item 3) and to 38 dB for the case of 8 taps (item 4), both of which represent significant crosstalk problems.

Furthermore, because the additive refresh cell actually involves two stages, the 8-tap memory of item (4) is actually 50 percent dedicated to "additive refresh" cells while that of item (3) is 25 percent used for the purpose of refreshing. Therefore, even though these memories can be designed as described, considerable risk is involved since the actual charge transfer efficiency of such a refresh cell when so densely packed has not yet been published. Consequently an early agreement is required to establish analog memory performance priorities and goals as well as the configuration to be implemented.

An attractive compromise is presented as item (5). Notice the acceptable crosstalk level for the maximum data handling mode which can be used mainly for buffer applications. Because the vertical clock rate is lower, the power consumption associated with that driver is lowered and the additive refresh cells internal to the subarrays are given more time for more accurate performance. Also, the additive refresh cells now represent less than 12 percent of the active area of the main memory. On the other hand, the isolation for the high accuracy mode is reduced to only 83 dB per pass, thereby permitting approximately a 16-point Doppler transform before the crosstalk exceeds the -55 dB to -60 dB target.

In conclusion, while the optimized 8-tap memory of item (4) can be designed and fabricated, the compromise of item (5) appears to be a more attractive demonstration because of the reduced on-chip clocking power and the somewhat lower risk associated with the lower density of additive refresh cells.

7.4 WIDEBAND ANALOG CIRCUITRY

The task of the wideband analog circuitry is to process the analog signal with the addition of very low noise and harmonic distortion in a very short settling time using very little power in order to achieve serial differencing to remove the accumulated leakage charge and offset nonuniformities as well as to create, in a serial fashion, the push/pull or complementary copies of the signal for use in the MDAC and memory. The sensing transistors to readout from the CCD are typically very small to minimize the attenuation of the signal by capacitive loading. But such a small transistor limits the input g_m and makes the low-noise, wideband transformation from high impedance to lower impedance very difficult. Modeling of circuits to meet these requirements has been performed by means of ISPIICE (copyrighted by National CSS, Inc).

The ISPIICE computer modelling cannot fully simulate the APUP circuitry because of the sampled-analog-nature of the CCD. The affects of serial differencing on the noise and harmonic distortion were treated as follows. Since two analog values which followed truly identical paths (only the second one trailing behind the first by about 50 nanoseconds) are differenced, any perturbation which changes very little during the 50 nanoseconds is virtually cancelled by the subtraction. Indeed, 20-dB cancellation or reduction of perturbations obtains for noise extending out to 318 kHz. But most "flicker" or "1/f" noise falls into that region and is thereby cancelled. Thus, only the ISPIICE predictions of broadband white noise are used in calculating the overall white noise encountered by the data during one pass through the APUP signal loop.

It is also important to note that, in addition to cancelling even harmonic distortion and offset nonuniformities, the sequential subtraction associated with the recommended push/pull mode further enhances the signal-to-noise ratio as indicated in figure 7.4-1. While the signal voltage is doubled in the push/pull mode

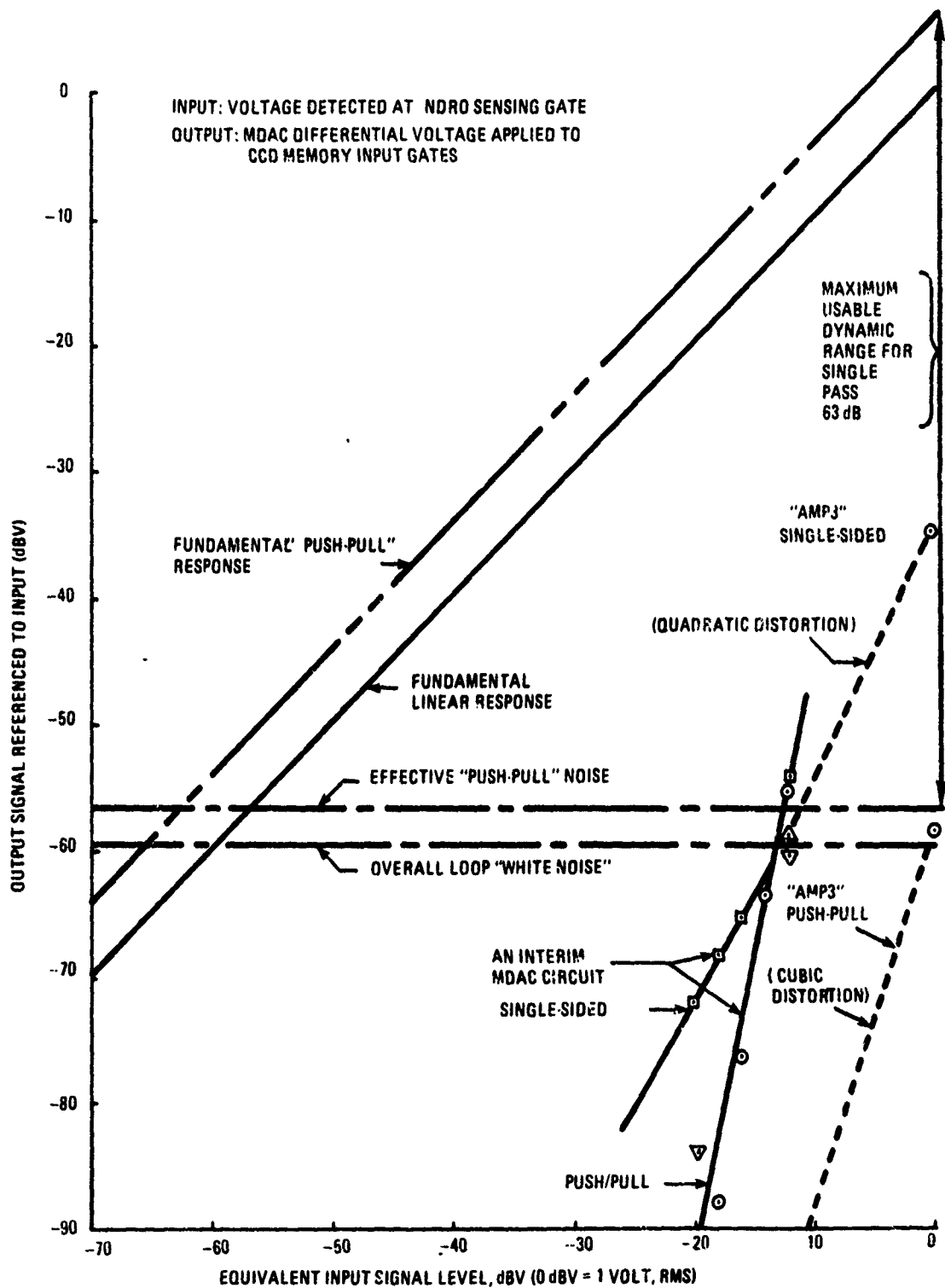


Figure 7.4-1. Circuit Transfer Characteristics Limitation

(quadrupling signal power), the noise power is only doubled, giving a net improvement of 3 dB. ISPIICE simulation of the even-harmonic distortion rejection of the sequential push/pull mode requires operating two identical copies of the circuit of interest with complementary input signals and differencing the two circuits' outputs. The ISPIICE Fourier analysis illustrated in table 7.4-1 then clearly pin-points harmonic distortion problem areas.

7.4.1 The Complete Analog Processing-Loop Circuit

The complete wideband analog circuit is shown in figure 7.4-2. The programmable data flow associated with this circuit is illustrated pictorially in figure 6-10, with the timing details presented in figure 6-11. For the purposes of the ac signal performance analysis by ISPIICE, all the shunt switches are deactivated by suitable bias and extremely low conductivity bias resistors introduced to guarantee continued proper bias without spurious signal loading. A full listing of the simulation circuit is given in figure 7.4-3 to include the MOS and bipolar transistor models expected with the fabrication "recipe" given elsewhere. The quiescent operating points of all the transistors in the circuit are given in figure 7.4-4. Note that none of the bipolar transistors are saturated, while most of the MOSFETS are in or near the pentode region except for the deactivated switches (M7.1 and M7.2). A tabulation of the various contributors to the "white noise" of the circuit is given in figure 7.4-5. Of interest to note here is that the overall transfer function represents an attenuation of 0.272 rather than gain. Thus, the output noise is dominated by the noise of the output devices (M6.3 and R3.3). To save substantially on the chip area, earlier versions of this circuit (CCMS7 subcircuit) had used bipolar transistors to make multiple identical copies of the analog signal current. But the higher noise of the bipolar compared to the FET suggested using FET's as shown in the circuit drawing of figure 7.4-2, at the expense of a somewhat larger area requirement. Indeed, even earlier trials at the needed circuits (like that illustrated in figure 7.4-6) had yielded worse noise and harmonic distortion performance

TABLE 7.4-1
FOURIER ANALYSIS FOCUSES ON NONLINEAR DISTORTION

Input Waveform: $X = A \sin(2\pi ft) + B \sin(2\pi kft)$ where $k = \text{integer}$

Transfer Characteristic: Output = $Y = C(0) + C(1)X + C(2)X^2 + C(3)X^3 + C(4)X^4 + \dots$

Output Spectral Constituents:

Exponent In Transfer Characteristic Power Series	Associated Spectral Lines
1 (linear)	1, k
2 (quadratic)	2, 2k, $k \pm 1$
3 (cubic)	3, 3k, $k \pm 2$, $2k \pm 1$
4 (quartic)	4, 4k, $k \pm 3$, $2(k \pm 2)$, $3k \pm 1$

Illustrative Example ($k = 6$):

Harmonic Component Index	Input Amplitude	Output Amplitude	Lowest Exponent Contributor
1	A	y (1,A)	one
2		y (2,A)	two
3		z (3,A)	three
4		z (B-2A)	three
5		y (B-A)	two
6		B	y (1,B)
7	y (B+A)		two
8	z (B+2A)		three
9			four
10			four
11	z (2B - A)		three
12	y (2,B)		two
13	z (2B+A)		three
14			four
15			five
16			five
17			four
18	z (3,B)		three
19			four
20		five	

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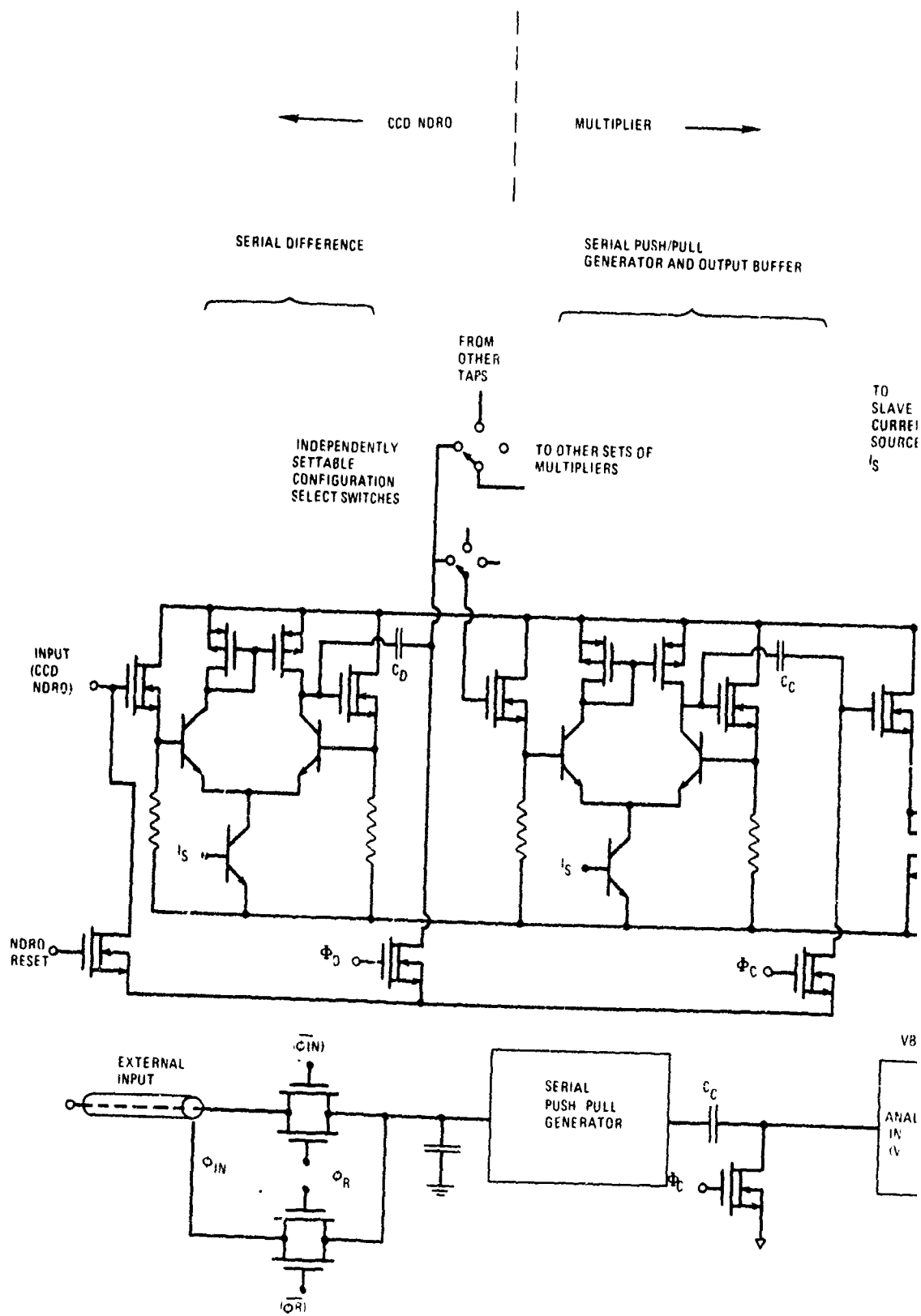
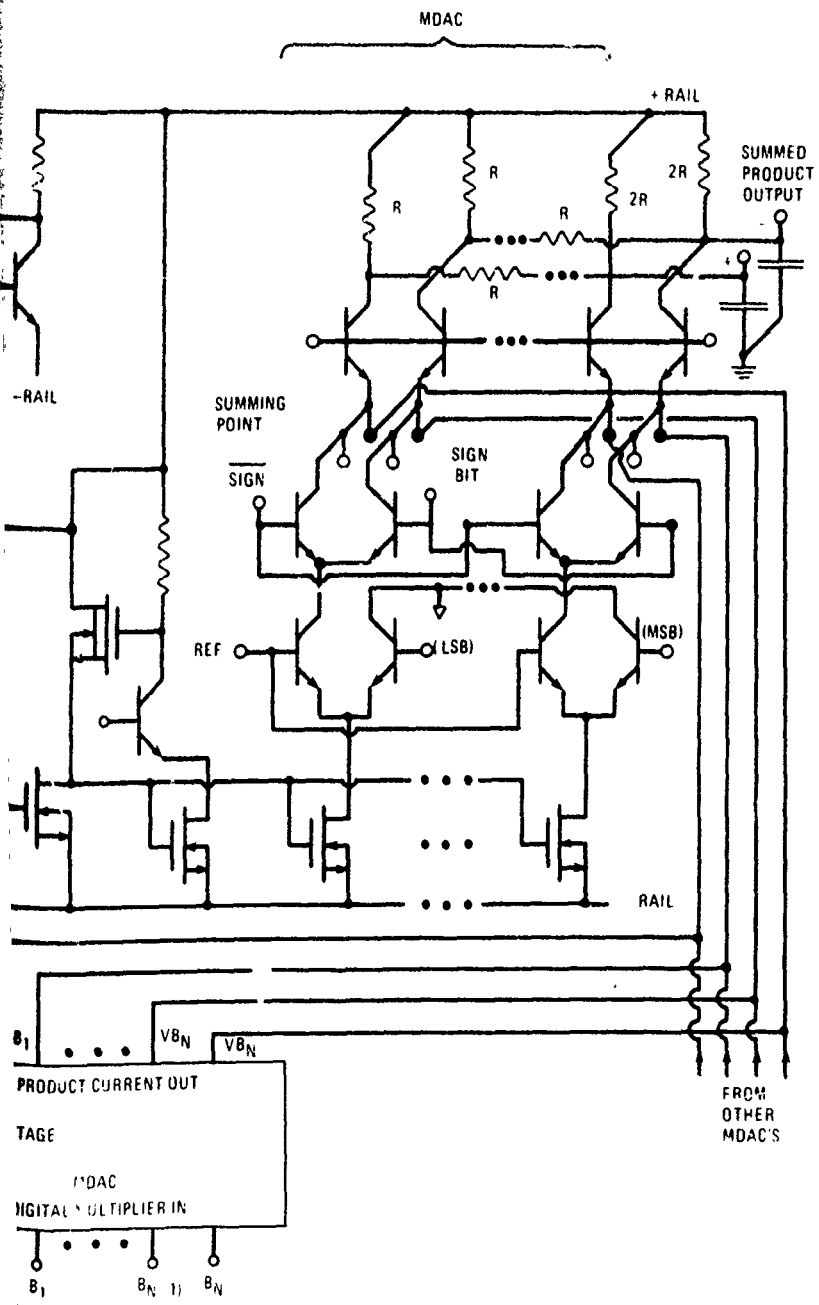


Figure 7.4-2



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Analogue Circuit Details of the nsform/Filter APUP

7-23/7-24

```

FILE: AMP3      CKT      FROM: P DISK
XN1 18 3 30 51 32 AMP6
XM2 51 3 30 31 32 AMP7
XM3 31 54 53 59 30 70 29 CCMS7
Q3 3 3 0 BP8
R3 30 3 20K
V29 29 0 0
V70 70 0 0.0
VR 32 0 4.5
VDD 30 0 8
CIN 28 18 1E-9
RB 18 32 1E10
VIN 28 19 SINE(0,.4,1E5,0,0) AC .1
V2 19 0 SINE(0,.4,6E5,0,0)

```

```

AMP7
NODES (18, 3, 30, 31, 32)
M1 30 18 2 2 NMOS3 75E-4 10E-4
M2 30 6 4 4 NMOS3 75E-4 10E-4
RM1 2 0 5K
RM2 4 0 5K
M5 21 21 30 30 PMOS2 120E-4 10E-4
M6 6 21 30 30 PMOS2 120E-4 10E-4
M7 31 0 32 0 NMOS1 12E-4 4E-4
Q1 21 2 5 BP8
Q2 6 4 5 BP8
Q4 5 3 0 BP8
CS 6 31 1E-12
RS 31 32 1E10

```

```

AMP6
NODES (18, 3, 30, 31, 32)
M1 30 18 2 2 NMOS3 12E-4 4E-4
M2 30 6 4 4 NMOS3 12E-4 4E-4
RM1 2 0 10K
RM2 4 0 10K
M5 21 21 30 30 PMOS2 120E-4 10E-4
M6 6 21 30 30 PMOS2 120E-4 10E-4
M7 31 0 32 0 NMOS1 12E-4 4E-4
Q1 21 2 5 BP8
Q2 6 4 5 BP8
Q4 5 3 0 BP8
CS 6 31 1E-12
RS 31 32 1E10

```

```

CCMS7
NODES (5, 4, 3, 9, 1, 70, 29)
M1 1 5 2 2 NMOS3 80E-4 8E-4
M2 1 4 3 3 NMOS3 80E-4 8E-4
M3 2 2 29 29 NMOS1 200E-4 5E-4
M4 3 2 29 29 NMOS1 200E-4 5E-4
M5 9 3 70 70 NMOS1 180E-4 6E-4
M6 77 3 70 70 NMOS1 180E-4 6E-4
M7 87 3 70 70 NMOS1 1440E-4 6E-4
Q1 4 76 9 BP2
Q2 10 76 77 BP2
Q3 81 76 87 BP16
R1 71 4 3.2K
R2 81 71 400
R3 71 10 3.2K
V71 71 0 6
V76 76 0 4

```

NMOS1
NSCM(VTD=1.3 PHI=.76 UD=550 NB=1.5E16 CD=3.4E-8 C1=3.4E-12 C2=3.4E-12 &
CBD=22E-12 CBS=22E-12 PB=.94 IS=1E-14 KN=.003 MN=1.58 KL=1.58 ECRIT=3.35E5)

NMOS3
NSCM(VTD=-1 PHI=.57 UD=550 NB=5E14 CD=3.4E-8 C1=3.4E-12 C2=3.4E-12 CBD=30E-12 &
CBS=30E-12 PB=.63 IS=1E-14 KN=.03 MN=1.10 KL=1.5 ECRIT=3.2E5)

PMOS2
PSCM(VTD=2.14 PHI=.66 UD=220 NB=5E15 CD=3.4E-8 C1=3.4E-12 C2=3.4E-12 &
CBD=80E-12 CBS=80E-12 PB=.72 IS=1E-14 KN=.0263 MN=1.10 KL=1.5 ECRIT=4.0E5)

BP2
NPN(BF=100 BR=1 IS=2E-14 RC=10 RB=100 RE=5 VA=40 PE=.65 PC=.65 CJC=.1P &
CJE=.16P ME=.33 MC=.33 TF=40P)

BP8
NPN(BF=100 BR=1 IS=8E-14 RC=5 PB=25 RE=1 VA=40 PE=.65 PC=.65 CJC=.40P &
CJE=.64P ME=.33 MC=.33 TF=40P)

BP16
NPN(BF=100 BR=1 IS=16E-14 RC=1 PB=12 RE=1 VA=40 PE=.65 PC=.65 CJC=.8P &
CJE=1.3P ME=.33 MC=.33 TF=40P)

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Figure 7.4-3. ISPIICE Listing of APUP Analog Circuits

```

ISPICE: >SIM AMP3
◆CORE 384K
CORE 448K
ISPICE: >DCSP
◆◆◆

```

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SINGLE POINT DC SIMULATION OF CIRCUIT: AMP3 COMPLETED
ISPICE: >PROBE OP

```

◆◆◆ BIPOLAR JUNCTION TRANSISTORS

NAME	MODEL	VBE	VBC	VCE	IC	IB
Q3	BP8	0.571	0.0	0.571	3.606D-04	3.606D-06
Q1.1	BP8	0.554	-0.514	1.068	1.878D-04	1.854D-06
Q2.1	BP8	0.553	-1.746	2.299	1.843D-04	1.763D-06
Q4.1	BP8	0.571	-1.627	2.198	3.757D-04	3.604D-06
Q1.2	BP8	0.554	-0.654	1.207	1.871D-04	1.840D-06
Q2.2	BP8	0.553	-1.837	2.389	1.838D-04	1.753D-06
Q4.2	BP8	0.571	-1.492	2.064	3.744D-04	3.604D-06
Q1.3	BP2	0.615	-0.552	1.167	4.525D-04	4.463D-06
Q2.3	BP2	0.615	-0.552	1.167	4.525D-04	4.463D-06
Q3.3	BP16	0.616	-0.552	1.168	3.620D-03	3.570D-05

◆◆◆ MOSFETS

NAME	MODEL	VGS	VDS	VBS	ID
M1.1	NMOS3	1.748	5.248	0.0	2.771D-04
M2.1	NMOS3	1.746	5.249	0.0	2.768D-04
M5.1	PMOS2	-4.734	-4.734	0.0	-1.878D-04
M6.1	PMOS2	-4.734	-3.503	0.0	-1.843D-04
M7.1	NMOS1	-4.500	-0.045	-4.500	4.465D-12
M1.2	NMOS3	1.838	5.383	0.0	5.253D-04
M2.2	NMOS3	1.837	5.384	0.0	5.250D-04
M5.2	PMOS2	-4.729	-4.729	0.0	-1.871D-04
M6.2	PMOS2	-4.729	-3.547	0.0	-1.838D-04
M7.2	NMOS1	-4.500	-0.045	-4.500	4.465D-12
M1.3	NMOS3	1.445	4.989	0.0	5.512D-04
M2.3	NMOS3	1.455	4.903	0.0	5.520D-04
M3.3	NMOS1	3.011	3.011	0.0	5.512D-04
M4.3	NMOS1	3.011	3.097	0.0	5.520D-04
M5.3	NMOS1	3.097	3.385	0.0	4.570D-04
M6.3	NMOS1	3.097	3.385	0.0	4.570D-04
M7.3	NMOS1	3.097	3.384	0.0	3.656D-03

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Figure 7.4-4. Transistor Quiescent Operating Points

AC SIMULATION OF CIRCUIT: AMP3

NOISE ANALYSIS OF: V(10,3)
 FREQUENCY = 1.000D+06

*** RESISTOR NOISE CONTRIBUTION (SQ V/Hz)

NAME	TOTAL
R3	6.035D-22
RB	3.079D-27
RM1.1	5.777D-18
RM2.1	5.778D-18
RS.1	3.094D-21
RM1.2	3.403D-18
RM2.2	2.795D-18
RS.2	3.898D-21
R1.3	1.848D-17
R2.3	5.887D-29
R3.3	5.262D-17

*** BIPOLAR JUNCTION TRANSISTOR NOISE CONTRIBUTION (SQ V/Hz)

NAME	MODEL	RE-IB	RE-IC	RE-FN	TOTAL
Q3	BP8	5.854D-20	4.815D-27	2.345D-21	1.436D-19
		3.449D-22	8.240D-20	0.0	
Q1.1	BP8	1.257D-19	1.408D-24	5.038D-21	2.775D-18
		2.109D-18	5.348D-19	0.0	
Q2.1	BP8	1.257D-19	8.855D-25	5.037D-21	2.687D-18
		2.021D-18	5.349D-19	0.0	
Q4.1	BP8	2.338D-20	2.790D-27	9.365D-22	5.887D-20
		1.279D-21	3.327D-20	0.0	
Q1.2	BP8	1.088D-19	4.176D-25	4.361D-21	1.126D-18
		6.220D-19	3.911D-19	0.0	
Q2.2	BP8	1.088D-19	2.351D-25	4.360D-21	9.928D-19
		4.944D-19	3.852D-19	0.0	
Q4.2	BP8	8.161D-21	1.121D-27	3.269D-22	2.148D-20
		1.091D-21	1.194D-20	0.0	
Q1.3	BP2	2.312D-22	1.663D-25	1.229D-23	5.095D-18
		5.042D-18	5.350D-20	0.0	
Q2.3	BP2	6.742D-22	4.741D-25	3.620D-23	1.451D-17
		1.436D-17	1.524D-19	0.0	
Q3.3	BP16	4.087D-24	1.472D-31	3.410D-25	5.658D-24
		4.996D-27	1.225D-24	0.0	

*** MOSFETS NOISE CONTRIBUTION (SQ V/Hz)

NAME	MODEL	RE-IB	RE-FN	TOTAL
M1.1	NMOS3	0.0	0.0	5.587D-18
		5.587D-18	0.0	
M2.1	NMOS3	0.0	0.0	5.588D-18
		5.588D-18	0.0	
M5.1	PMOS2	0.0	0.0	1.334D-20
		1.334D-20	0.0	
M6.1	PMOS2	0.0	0.0	1.545D-20
		1.545D-20	0.0	
M7.1	NMOS1	0.0	0.0	2.063D-31
		2.063D-31	0.0	
M1.2	NMOS3	0.0	0.0	3.758D-18
		3.758D-18	0.0	
M2.2	NMOS3	0.0	0.0	3.086D-18
		3.086D-18	0.0	
M5.2	PMOS2	0.0	0.0	9.599D-21
		9.599D-21	0.0	
M6.2	PMOS2	0.0	0.0	1.102D-20
		1.102D-20	0.0	
M7.2	NMOS1	0.0	0.0	2.599D-31
		2.599D-31	0.0	
M1.3	NMOS3	0.0	0.0	3.768D-18
		3.768D-18	0.0	
M2.3	NMOS3	0.0	0.0	9.625D-18
		9.625D-18	0.0	
M3.3	NMOS1	0.0	0.0	6.088D-18
		6.088D-18	0.0	
M4.3	NMOS1	0.0	0.0	1.563D-17
		1.563D-17	0.0	
M5.3	NMOS1	0.0	0.0	1.985D-17
		1.985D-17	0.0	
M6.3	NMOS1	0.0	0.0	5.653D-17
		5.653D-17	0.0	
M7.3	NMOS1	0.0	0.0	6.599D-26
		6.599D-26	0.0	

OUTPUT NOISE VOLTAGE 1.568D-08 VOLT/RT HZ 2.458D-16 CO VOLT/Hz

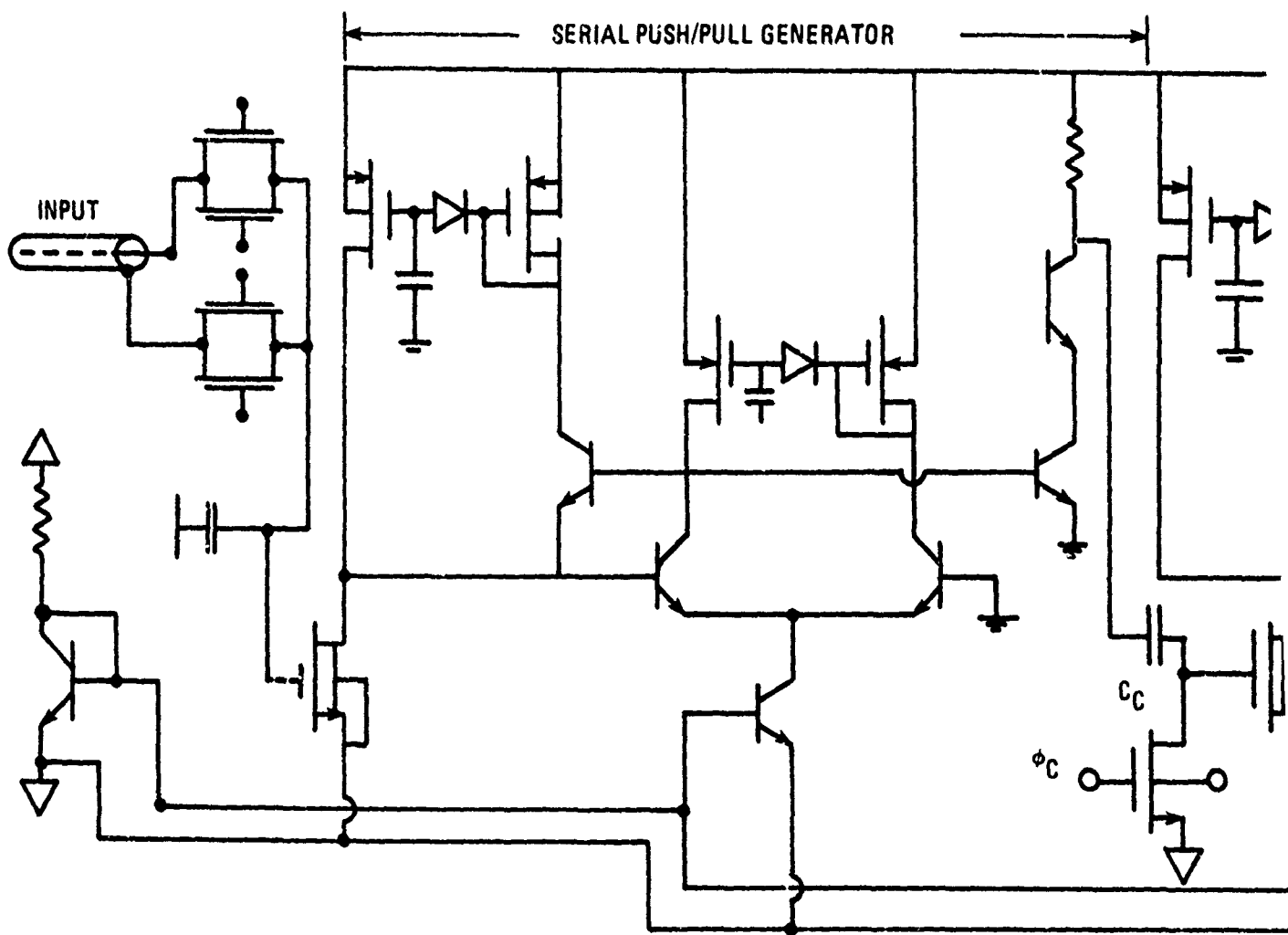
TRANSFER FUNCTION VALUE (V(10,3)/VIN) = 2.718D-01
 INPUT NOISE VOLTAGE 5.769D-08 VOLT/RT HZ 9.045D-16 CO VOLT/Hz

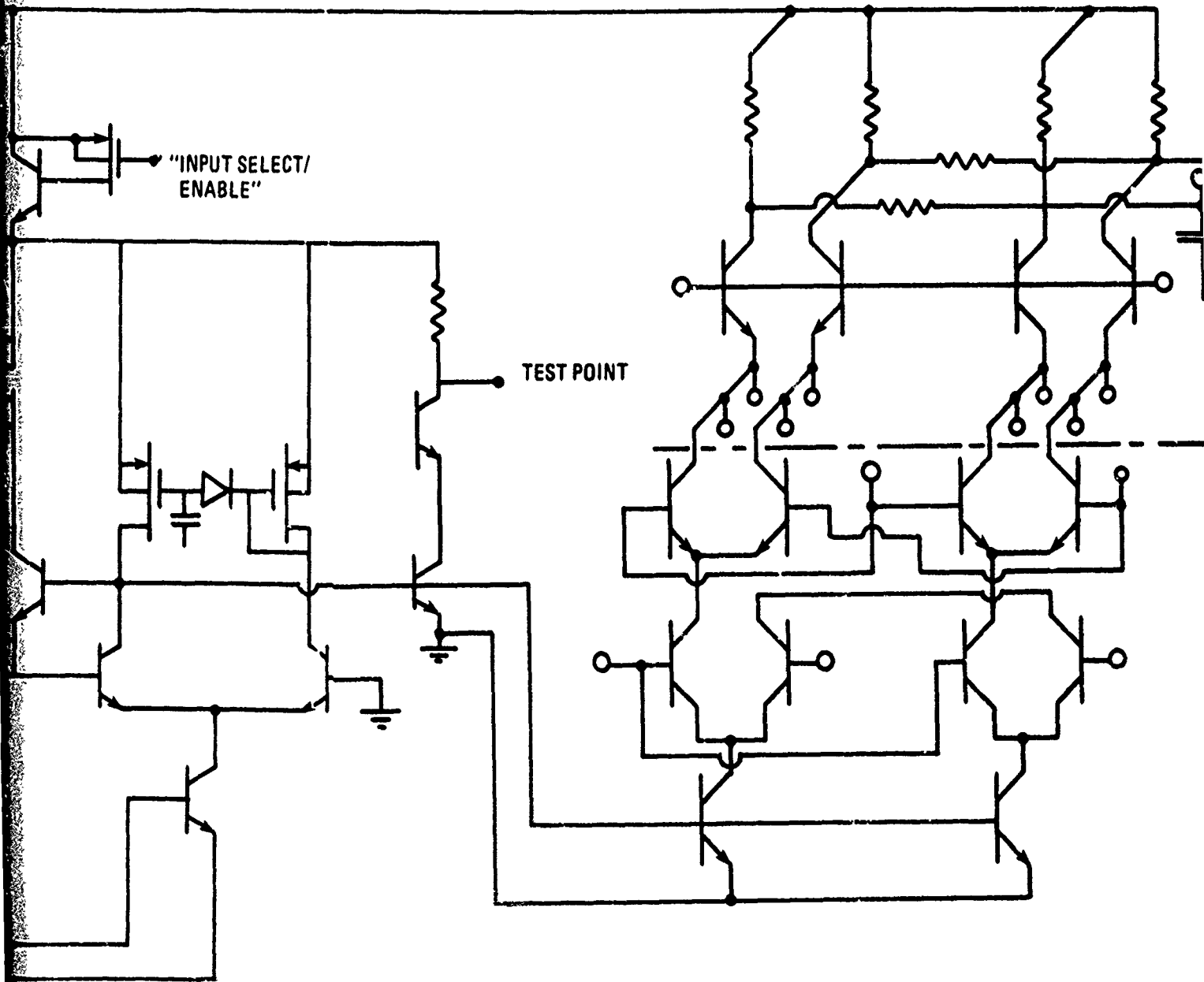
800024 V51

Figure 7.4-5. "White Noise" Analysis

albeit at the much lower power levels implied in table 7.4-2. The harmonic distortion analysis is presented in figure 7.4-7. The comparison between the single-sided and push/pull modes of operation highlights the major contribution of the quadratic distortion (over cubic and higher powers by about 30 dB). Further comparison of the circuits in figures 7.4-2 and 7.4-6 shows that the critical input or NDRO-sensing transistor in the later version is intimately coupled to a small circuit feedback loop so as to duplicate the input voltage waveform on a virtually identical MOS gate but at a lower impedance level, whereas the feedback loop in the earlier trial circuit provided a very low impedance current-summing AC-ground node which only held the source-drain bias of the NDRO sensing transistor fixed, leaving that key transistor out of the feedback loop. In addition to the harmonic distortion tabulated in figure 7.4-7, that of the earlier trial circuit of figure 7.4-6 is also reported in the curves of figure 7.4-1. The benefits of feedback linearization particularly on the push/pull mode were very obvious: The same amount of harmonic distortion did not occur until the input signal power was increased by about 12 dB.

The bandwidth and transient response of the cascaded subcircuits are presented in figures 7.4-8 and 7.4-9. The two sets of curves show nearly 50-MHz signal bandwidth and critically dampened settling of transients. Indeed, since the three subcircuits are separated by sampling capacitors and switches, the direct cascade model does not recognize that after the activation of the sampling switch a new settling operation starts within each subcircuit and that individual bandwidth and transient response curves should be more accurate. The cascaded circuits, however, give the worst case response, showing that all three subcircuits are settled in about 29 nanoseconds. But the waveforms of figure 6-11 indicate the settling time should not exceed 25 nanoseconds (or ideally be as fast as 15 to 20 nanoseconds) for the high performance operating mode with a data processing rate of 10 MHz. Thus, the circuit





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Figure 7.4-6. An Early APUP Trial Circuit

7-29/7-30

2

TABLE 7.6-2

COMPARISON OF MOS VS BIPOLAR SIGNAL DRIVERS

Common "Boundary Conditions": Active interior cell area = $A = 2W \cdot L$; Transistor Quiescent bias voltage = $V_B = \gamma \cdot V_{\text{signal}}$ where $\gamma > 1$; Signal Bandwidth = $f = g_m / (2 \pi C)$ where $C_{\text{LOAD}} = 10 \text{ pFd}$

Item	MOS Formula/Result	Bipolar Formula/Result
Transconductance, gm	$\beta(V_{gs} - V_T) = (2 \beta I_D)^{1/2}$ where $I_D = (\beta/2)(V_B)^2$	$(eI_e/kT) = (eI_e W/kT)$ $= (eI_e/kT)(A/2L)$
Bandwidth, f	$(\beta I_D/2)^{1/2} / (2 \pi C)$ $= (\beta V_B) / (2 \pi C)$ or $(I_D = 2 (\pi f C)^2 / \beta)$	$(eI_e/2 \pi kTC)$ $= (eI_e/4 \pi kTC)(A/L)$ $(f = \lambda/L, \text{ empirically; } \lambda = 4E6)$
Quiescent Power = $P = I_D V_B$	$2 V_B (\pi f C)^2 / \beta = \pi f C (V_B)^2$	$(2 \pi f C)(kT/e)(V_B)$
Device Geometry Relationship	$\beta = \mu C_{ox} (W/L)$ where C_{ox} = gate capacitance per (cm) ²	$C = C_{\text{LOAD}} + C_{\text{EMIT}}$, where $C_{\text{EMIT}} = (A)(C_e^1)$ with C_e^1 = emitter base capacitance per (cm) ²
Transistor Active Area, A	$2L^2 \left(\frac{W}{L} \right) = 2\beta L^2 / (\mu C_{ox})$ $A = (C_{\text{LOAD}}) / (\mu N C_{ox} V_B) / (4 \pi f L^2) - C_s^1$ where $(\mu N C_{ox}/4 \pi) = 1.19E^{-6}$, $C_s^1 = 3E-8 \frac{f d}{\text{cm}^2}$	Adjusting empirical constant, λ to give $\psi : f = (JeA) / (\psi CL)$ or $A = (C_{\text{LOAD}}) / ((Je) / (\psi f L) - C_e^1)$ where $\psi = 6, C_e^1 = 1.3E-7 \text{ Fd (cm)}^2$
Predictions for 88 MHz bandwidth, 4 micron spacing, two volt bias, J_e 0.6 amp/cm.	$P = 12.16 \text{ milliwatts}$ $A = 7.19E^{-5} \text{ cm}^2$ (about 85 microns square)	$P = 0.3 \text{ milliwatts}$ $A = 3.689E^{-6} \text{ cm}^2$ (about 19 microns square)

*A.B. Phillips, "Transistor Engineering - An Introduction to Integrated Semiconductor Circuits" McGraw-Hill Series in Solid State Engineering, 1962, New York, pp. 324--25.

TRAN SIMULATION OF CIRCUIT: PPAMP2 COMPLETED
 101 SWEEP POINTS COMPUTED TO TIME = 1.000D-05
 HIT RETURN FOR OUTPUT >>

SIGNAL 1: (S1); SIGNAL 2: (S2); QUADRATIC DISTORTION: (P2); CUBIC DISTORTION: (P3)

FOURIER COMPONENTS OF TRANSIENT RESPONSE: V(10.3,10.5) (PUSH/PULL)

DC COMPONENT = 6.381D-05

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000D+05	2.172D-01 (S1)	1.000000	179.722	0.0
2	2.000D+05	7.445D-06 (P2)	0.000034	-47.645	-227.367
3	3.000D+05	1.499D-05 (P3)	0.000067	-152.916	-332.638
4	4.000D+05	5.350D-05 (P3)	0.000246	-168.653	-343.375
5	5.000D+05	1.379D-05 (P2)	0.000063	-24.592	-204.314
6	6.000D+05	2.172D-01 (S2)	1.000012	179.209	-1.513
7	7.000D+05	1.857D-05 (P2)	0.000085	-17.955	-197.677
8	8.000D+05	4.531D-05 (P3)	0.000209	-159.623	-339.345
9	9.000D+05	2.370D-05	0.000109	-14.767	-194.489
10	1.000D+06	2.643D-05	0.000122	-13.275	-192.997
11	1.100D+06	9.193D-05 (P3)	0.000423	4.625	-175.097
12	1.200D+06	3.193D-05 (P2)	0.000147	-11.456	-191.173
13	1.300D+06	3.714D-05 (P3)	0.000171	-142.193	-321.915
14	1.400D+06	3.781D-05	0.000174	-10.264	-189.986
15	1.500D+06	4.093D-05	0.000189	-9.633	-189.360
16	1.600D+06	4.412D-05	0.000203	-9.241	-188.963
17	1.700D+06	4.737D-05	0.000213	-9.055	-188.777
18	1.800D+06	3.246D-05 (P3)	0.000149	-28.443	-298.165
19	1.900D+06	5.436D-05	0.000250	-8.551	-188.273
20	2.000D+06	5.815D-05	0.000268	-8.229	-187.951

TOTAL HARMONIC DISTORTION = -64.3 dB

FOURIER COMPONENTS OF TRANSIENT RESPONSE: V(10.5) (SINGLE-SIDED)

DC COMPONENT = 4.551D+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000D+05	1.036D-01 (S1)	1.000000	-0.278	0.0
2	2.000D+05	6.669D-04 (P2)	0.006141	89.473	89.751
3	3.000D+05	7.353D-06 (P3)	0.000072	31.509	31.787
4	4.000D+05	2.678D-05 (P3)	0.000247	11.725	12.002
5	5.000D+05	1.324D-03 (P2)	0.012189	-92.265	-91.987
6	6.000D+05	1.036D-01 (S2)	1.000011	-1.791	-1.513
7	7.000D+05	1.329D-03 (P2)	0.012239	87.669	87.947
8	8.000D+05	2.271D-05 (P3)	0.000209	21.205	21.482
9	9.000D+05	1.194D-05	0.000110	165.578	165.356
10	1.000D+06	1.329D-05	0.000122	167.760	168.033
11	1.100D+06	4.601D-05 (P3)	0.000424	-175.271	-175.593
12	1.200D+06	6.655D-04 (P2)	0.006128	86.740	87.017
13	1.300D+06	1.831D-05 (P3)	0.000173	39.933	39.211
14	1.400D+06	1.900D-05	0.000175	170.157	170.435
15	1.500D+06	2.057D-05	0.000189	169.060	169.338
16	1.600D+06	2.215D-05	0.000204	169.485	169.763
17	1.700D+06	2.373D-05	0.000219	168.776	169.054
18	1.800D+06	1.648D-05 (P3)	0.000152	149.857	150.135
19	1.900D+06	2.724D-05	0.000251	171.047	171.324
20	2.000D+06	2.912D-05	0.000268	170.588	170.866

TOTAL HARMONIC DISTORTION = -34.3 dB

80-0024-V-54

Figure 7.4-7. Harmonic Distortion Analysis

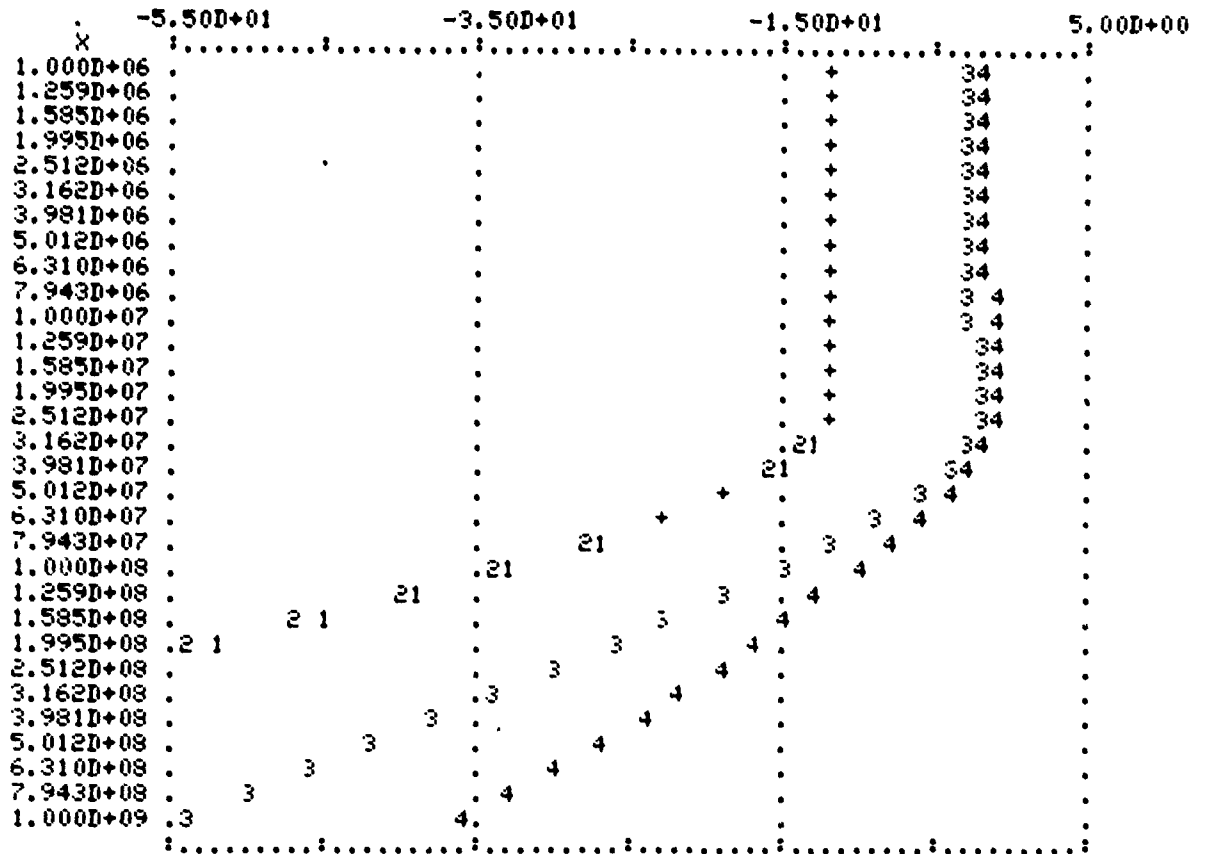
AC SIMULATION OF CIRCUIT: AMP3 COMPLETED
 31 SWEEP POINTS COMPUTED TO FREQ = 1.000D+09
 HIT RETURN FOR OUTPUT >>

ISPICE 2.08 (12AUG79) - 07JAN80 16.03.03

AC SIMULATION OF CIRCUIT: AMP3

LEGEND

X : FREQ
 Y1 : DB(V(10.3)/.1) 1. MDAC OUTPUT
 Y2 : DB(V(54)/.1) 2. MDAC FEEDBACK LOOP
 Y3 : DB(V(31)/.1) 3. PUSH/PULL GENERATOR OUTPUT
 Y4 : DB(V(51)/.1) 4. SERIAL DIFFERENCER OUTPUT



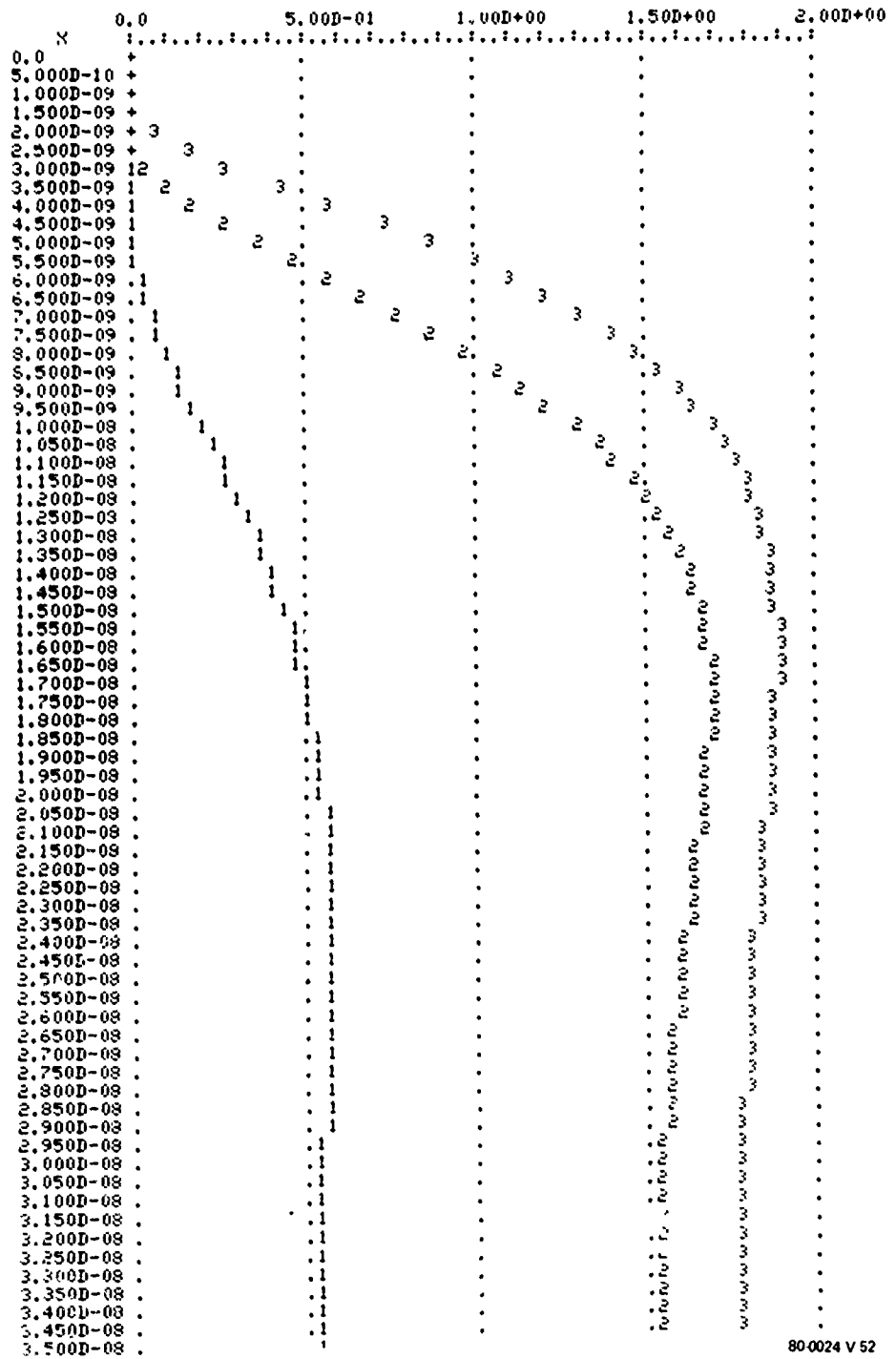
80-0024-V-53

Figure 7.4-8. Bandwidth Analysis of Cascaded Subcircuits

TRAN SIMULATION OF CIRCUIT: PPAMP3

LEGEND

X : TIME
 Y1 : V(10.5,10.3) 1. MDAC OUTPUT
 Y2 : V(31.1,31.2) 2. PUSH/PULL GENERATOR OUTPUT
 Y3 : V(51.1,51.2) 3. SERIAL DIFFERENCER OUTPUT



800024 V 52

Figure 7.4-9. Transient Response of Cascaded Subcircuits

of figure 7.4-3 needs only slight modification to meet that objective.

The overall loop gain must also be kept at unity. Since the circuit of figure 7.4-2 has an attenuation of 0.272, gain of 11.3 dB is needed to overcome that attenuation. Furthermore, because of the loading on the NDRO sensing FET, additional signal loss usually occurs in the NDRO process and can amount to an additional 10 dB to 15 dB. Typically, this loss arises from a very small sensing capacitance interior to the CCD channel being loaded by a FET gate and parasitic capacitance. The most attractive way to incorporate the needed 20 dB to 25 dB of gain is directly within the CCD by making use of its gain relationship:

$$\text{CCD GAIN} = (\text{INPUT C}) / (\text{OUTPUT C})$$

The attenuation of the gate and parasitic capacitance loading at the NDRO is automatically accounted for by using the total capacitance on the NDRO gate node which typically may range from $5\text{E-}14$ Fd to $2\text{E-}13$ Fd. Thus, the interior channel capacitance of the CCD input need only be 3.7 (i.e., 11.3 dB) times larger than (OUTPUT C).

Large "fill/spill" type input capacitances can easily be made using interdigitated techniques as shown in figure 7.4-10 where (INPUT C) $\sim 10\text{pFd}$. This approach has the added benefit of reducing the CCD "fill/spill" input noise labelled as item C in figure 7.4-11. Increasing the input capacitance has ultimate limitations: The first limitation occurs for the case of multiple input or output points and involves the offset nonuniformities between such multiple nodes. The gain (and thus input capacitance) cannot be so large that one or more of the parallel input or outputs become saturated for chip operation within the typical range of chip and signal biases. The second limitation is a reduced signal bandwidth due to charge transfer from a larger and larger input capacitor through the limited "throat" of the input injection gate. Consider, as an example adding a

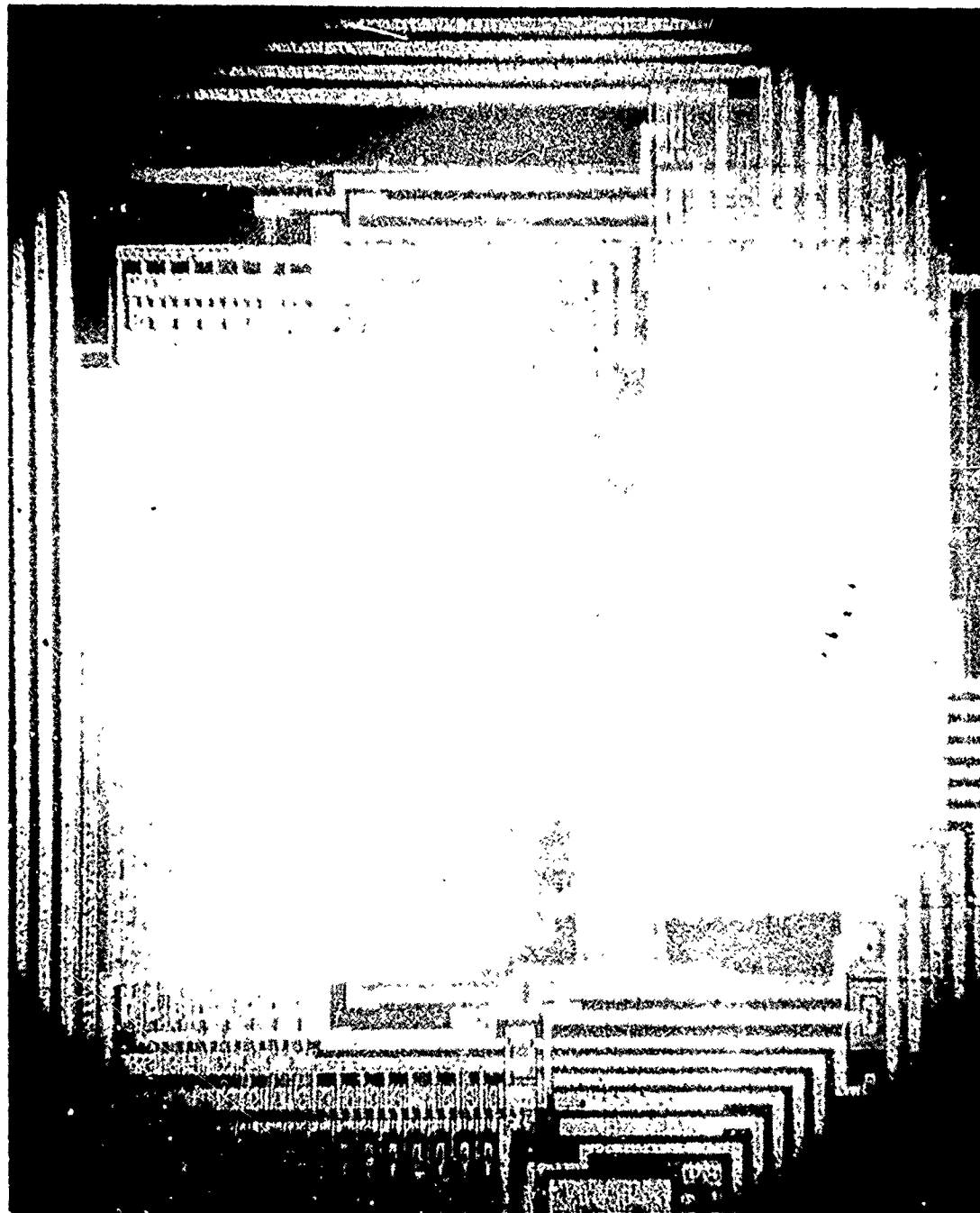
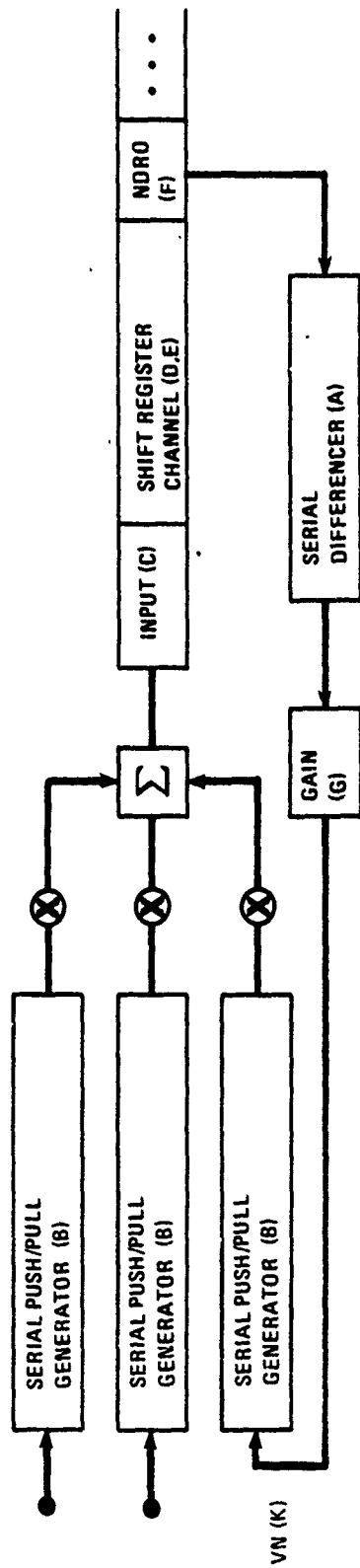


Figure 7.4-10. The Delay and Add CCD #7008 with an Interdigital 10 pFd. Input Capacitance and a Double Shielded Output



KEY TO NOISE SOURCE IDENTIFICATION:

- A. NDRO SERIAL DIFFERENCING TAP BUFFERS $(19.9 \text{ E-9 VOLT (Hz)}^{-1/2})$
- B. MDAC PUSH-PULL GENERATOR AND CURRENT COPIES $(54.2 \text{ E-9 VOLT(Hz)}^{-1/2})$
- C. CCD "FILL/SPILL" INPUT WITH 56.42 fFd GIVING $271 \mu\text{v}$ INPUT NOISE
- D. THERMAL LEAKAGE AT $10^{-8} \text{ AMP (cm)}^{-2}$ FOR 10^{-3} SEC IN $16 \mu\text{x} 32 \mu$ GIVING 18 ELECTRONS NOISE
- E. TRAPPING NOISE, UP TO 87 ELECTRONS
- F. NDRO RESET NOISE (UNITY GAIN GIVES 56.42 fFd WITH $271 \mu\text{v}$ NOISE); NOT PRESENT WITH "INTERNAL NDRO."
- G. HYPOTHETICAL NOISE-FREE GAIN, G (ALL OTHER ELEMENTS ASSUMED UNITY GAIN).

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Figure 7.4-11. Distribution of Dominant Noise Sources in the APUP Signal Loop

gain of 24.1 dB in the loop of figure 7.4-10. This means an input capacitance 16 times larger, giving a 0.905 pFd input capacitance, and a fill/spill noise reduced from 271 microvolts to 68 microvolts. This much gain, however, is probably near the limitation arising from offset nonuniformities and the desire to keep power dissipation low and avoid the chip temperature rise which aggravates the analog memory blemishes.

7.4.2 The Predicted "Dynamic Range - Sample Rate" Product

The "dynamic range - sample rate" product defined only by a short numerical example in the purchase request is now more clearly specified. Because the correlation transform and recursive filters both involve signal-to-noise enhancement via coherent signal addition versus non-coherent noise power addition, this figure of merit must be associated with only a single pass of the signal through the signal channel as for the case of a double buffer application. But the "additive refresh" feature, needed to give adequate isolation from sample to sample, for multiple passes through the memory can then be dropped by eliminating the two dummy isolation stages yielding complementary signal packets in adjacent memory positions and doubling the sample rate as well as quadrupling the memory size as per figure 6-4.

Since figure 7.4-9 indicated a settling time of 29 nanoseconds, the shortest time period for two complementary charge packets of the same analog signal is $4 \times 29 = 116$ nanoseconds. Thus the analog sample rate becomes $(116E-9 \text{ sec})^{-1} = 8.62 \text{ MHz}$ or 69.36 (dB) Hz. From figure 7.4-1, the maximum usable dynamic range appears to be around 63 dB. Thus, the "dynamic range-sample rate" figure-of-merit product becomes $(69.4) + (63) = 132.4 \text{ (dB)}^2 \text{ Hz}$, when only temporal noise is considered, complementary push/pull operation assumed, and blemishes and offset nonuniformities serial subtracted as per the paths of travel of figures 6-12 and 6-13. Of course, excessive chip ambient temperatures may aggravate the blemishes so much that the simpler compensation assumed above leaves a fixed pattern noise exceeding the temporal noise.

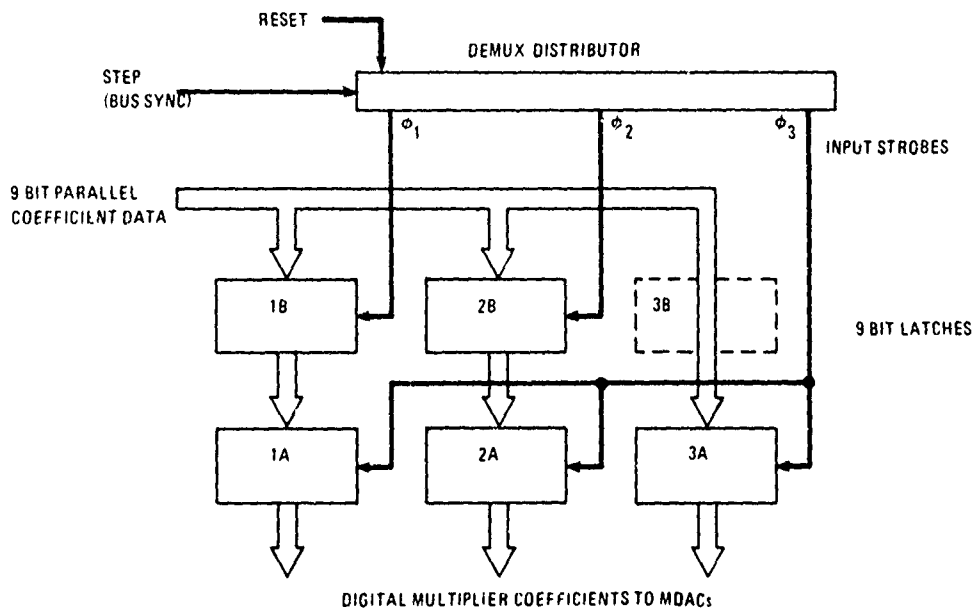
An estimate of the likely chip temperature rise is therefore useful. A typical thermal resistance from the silicon device junction to the ambient air outside the package for a 40-pin ceramic DIP is approximately 50°C per watt.* Combining this with the power consumption prediction of 627 milliwatts yields a 31°C temperature rise over ambient. Of course, radiating-fin heat sinks could lower this temperature rise by as much as 50 to 60 percent, if the thermally-generated fixed pattern represents the limitation on the dynamic range.

*Signetics Data Book, Signetics Corp, Sunnyvale, Calif., 1974, page (9-13)

7.5 DIGITAL DATA HANDLING CIRCUITS

The objective of the digital-multiplier-coefficient handling circuits is to receive the digital data from a high speed digital data bus from the host computer, transport these data to the proper locations, then have the data available when needed for the full multiply operation. In a recursive filter generating output at the rate of 10^6 output points per second, a whole new set of six coefficients is needed every 100 nanoseconds, yielding an effective digital data rate of 60 MHz. But in the correlation transform mode, only half of these coefficients need be changed rapidly for multiplexing. Thus, the digital data circuits break naturally into halves, each half handling the multiplier coefficients for one sum of three products at an equivalent data rate of 30 million words per second, which is a data bus rate within the capability of today's technology. Such a data bus may be Schottky TTL or ECL in basic technology. On the APUP chip, however, today's MOS technology (using either CMOS or NMOS) is not ready for that speed. In the course of development for the VHSIC program funded by DOD., the ability to perform logic monolithically at the 30 MHz to 60 MHz rates using micron-feature-size MOS should be a direct fall-out within the next several years. Meanwhile, the lowest power technique for 30 MHz logic is "Integrated Schottky Logic (ILS)".

The digital data flow pattern, illustrated in figure 7.5-1 was selected for two reasons. It simultaneously minimizes the transistor count (and thus chip area and power) while also providing for a constant data flow rate with data arriving at 30 MHz per second rate, the first word is stored in word latch (1-B) via the input strobe ϕ_1 , and the second word is stored in word latch (2-B) by strobe ϕ_2 . With the arrival of the third word, strobe ϕ_3 not only stores the third word in latch (3-A) but also parallel transfers the first two words from latches (1-B) and (2-B) to latches (1-A) and (2-A). Thus effectively one out of six word registers or latches is saved in this approach when compared to a traditional serial shift register with a parallel

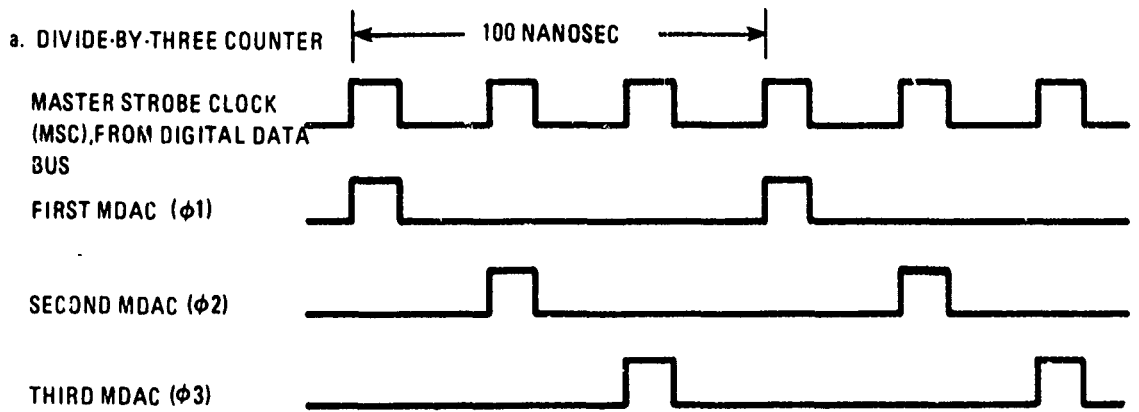
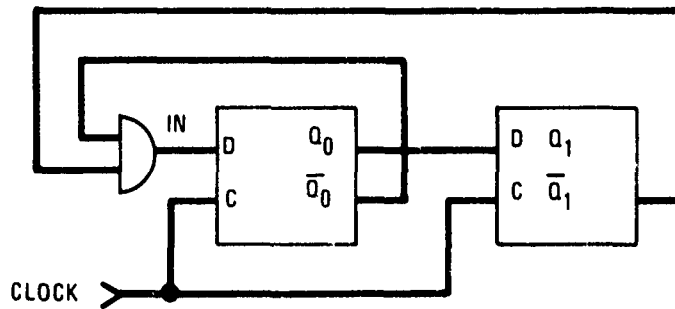


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Figure 7.5-1. Digital Multiplier Coefficient Data Flow transfer to the latches which hold the digital multiplication coefficient for the full multiply time.

The demultiplexer/distributor of figure 7.5-1 is described in more detail in figure 7.5-2. Two flip-flops are connected for "divided-by-three", with appropriate decoders generating the strobe pulses (ϕ_1 , ϕ_2 , ϕ_3). The table is intended to show that this demultiplexer/distributor goes into the proper sequence independent of its arbitrary initial state. The circuit details of the divide-by-three counter and the demux and storage latches are given in figures 7.5-3 and 7.5-4, respectively. The reset or synchronization of the demultiplexer/distributor need not be done every three words, but could occur at such intervals as once every interpulse period or every new transform batch. The reset nodes of the distributor counter are indicated in figure 7.5-3.

ISL circuitry similar to that of figure 7.5-3 will also be used in the high speed waveform generation part of the chip which both creates, then translates through drivers, all the waveforms needed to operate all the rest of the APUP.



TRUTH TABLE:

CLOCK PERIOD	Q_0	Q_1	IN, D	\bar{Q}_0	\bar{Q}_1	
1	1	1	0	0	0	(ASSUMED)
2	0	1	0	1	0	($\phi 3$)
3	0	0	1	1	1	($\phi 1$)
4	1	0	0	0	1	($\phi 2$)
5	0	1	0	1	0	($\phi 3$)

b. COUNTER DECODING FOR DEMUX SCANNING

$$\phi 1 = \bar{Q}_0 \cdot \bar{Q}_1 \cdot (\text{MSC})$$

$$\phi 2 = Q_0 \cdot \bar{Q}_1 \cdot (\text{MSC})$$

$$\phi 3 = \bar{Q}_0 \cdot Q_1 \cdot (\text{MSC})$$

80-0024-V 63

Figure 7.5-2. MDAC Digital Data Demux/Scan

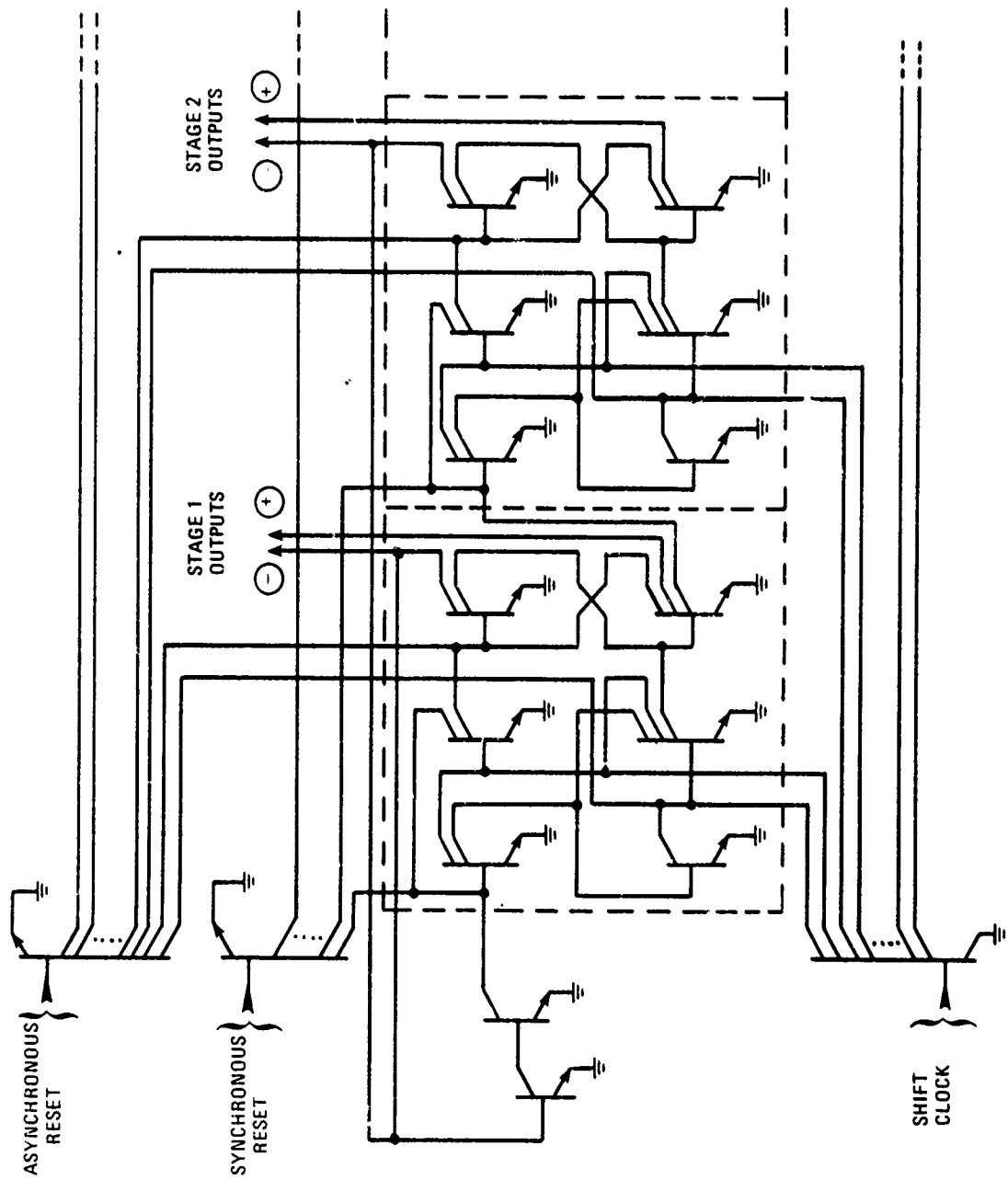


Figure 7.5-3. The ISL "Divide-by-Three"
Digital Data Demux Scan Counter

80-0024-V-64

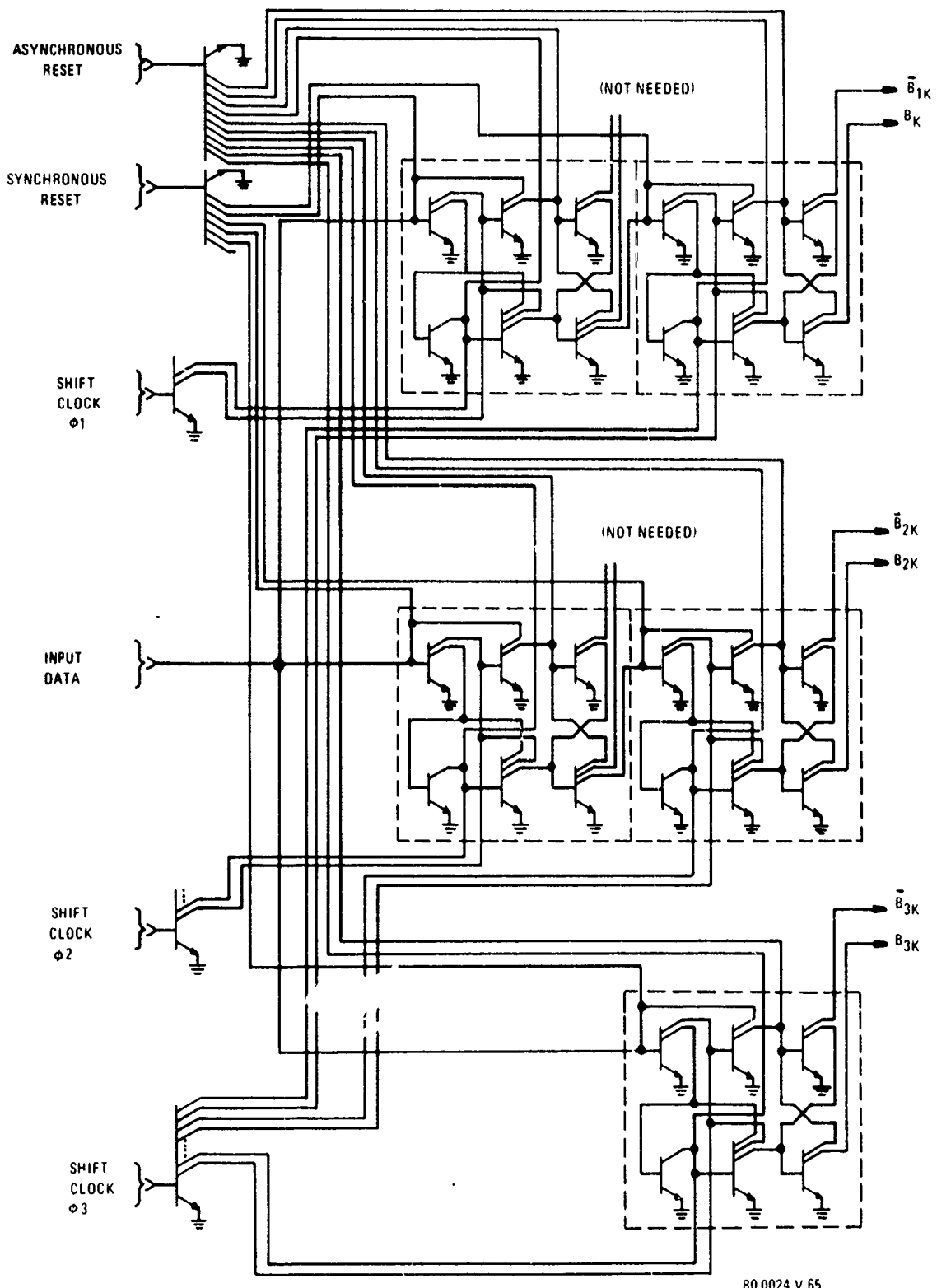


Figure 7.5-4. The MDAC Digital Data Demux and Storage Latches

7.6 CONFIGURATION CONTROL AND ON-CHIP SUPPORT CIRCUITRY

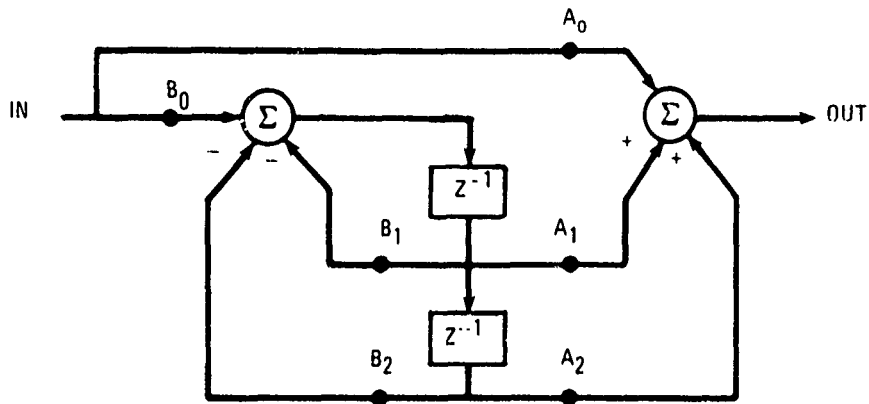
7.6.1 Configuration Command Structure

The overall similarity between the recursive filter mode and the correlation transform mode is emphasized in figure 7.6-1. The buffer memory mode is technically a sub-set of the correlation transform mode. As indicated in figure 7.6-2, for the case of four binomially-distributed taps on the memory, there will be at least twelve analog switching nodes of the types SPST or SPDT which can be controlled by a single bit in a configuration control word. Additional configuration control switches occur in the digital parts of the APUP chip such as the memory mode select switch used to choose either the "high accuracy" mode which uses the additive refresh operation or the "maximum data handling" mode where the number of analog samples can be quadrupled but sample-to-sample isolation and blemish rejection are diminished. Overall, the configuration command word is approximately 16 bits and will provide for the following choices:

- o Recursive filter versus correlation transform.
- o General correlation transform versus buffer memory only.
- o Which taps to be used.
- o High-accuracy mode versus maximum data handling mode (with reduced isolation and blemish rejection).

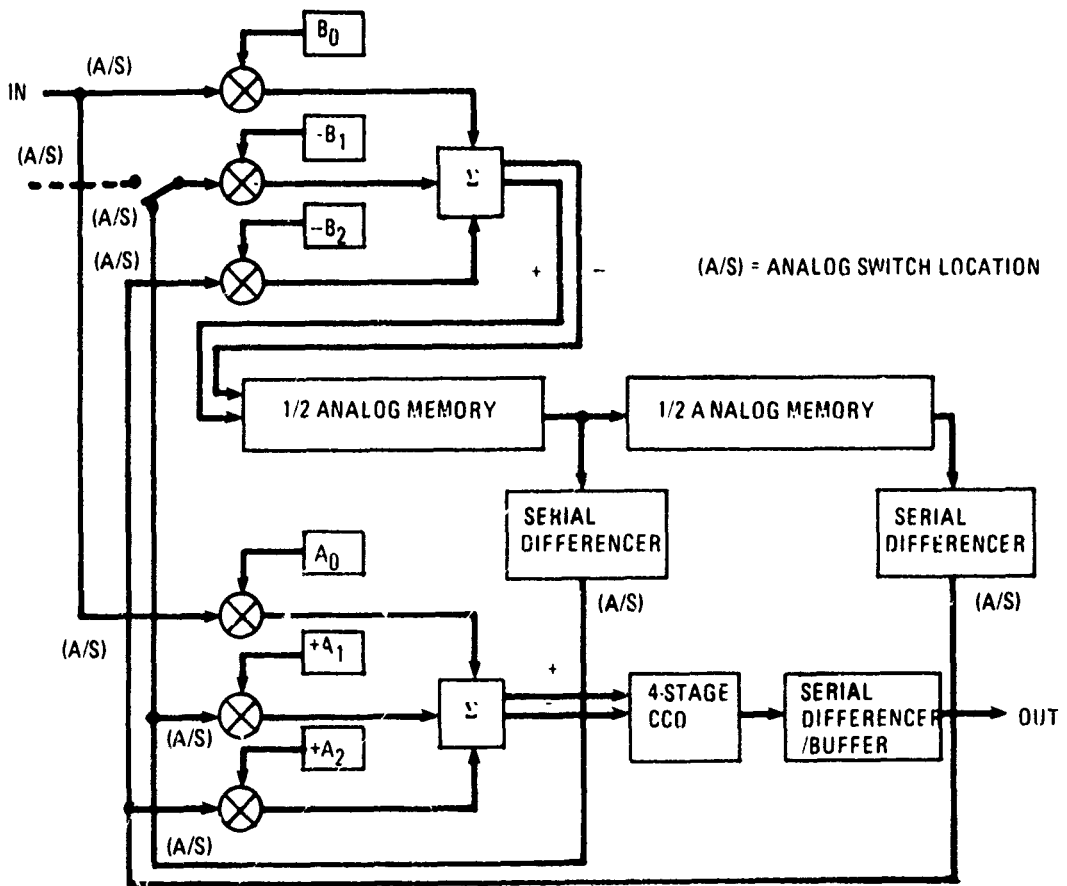
All configurations allow multiplexing several filters by appropriately interlacing the digital multiplication coefficients on the digital data bus from the host computer.

The 16-bit configuration command word is fed serially into a shift register, after which it is stored for extended use on static latches. These registers and latches as well as the analog switches are all CMOS to guarantee low power consumption in the logic parts during extended data retention periods as well as bi-directional and low switch resistance combined with low switch feedthrough for the analog switches. The CMOS configuration command input register can easily accept data at any rates below four megahertz. The total reconfiguration time is under one microsecond for latch transfer and settling.



a) 2ND ORDER RECURSIVE FILTER

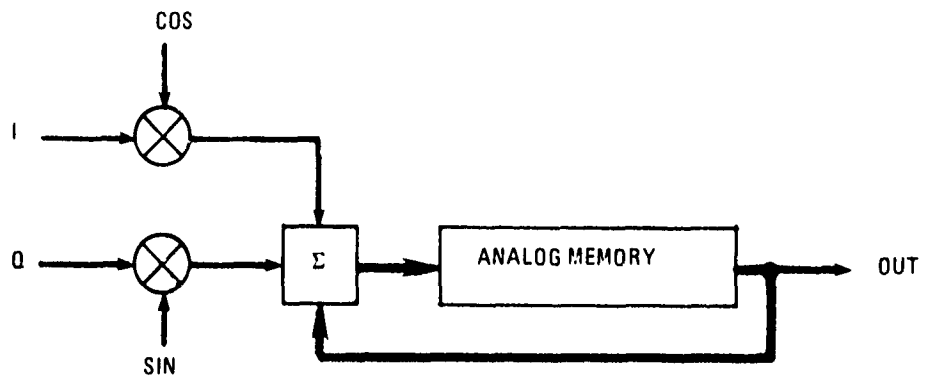
$$H(z) = A_0 \frac{1 + \left(B_1 + B_0 \frac{A_1}{A_0} \right) z^{-1} + \left(B_2 + B_0 \frac{A_2}{A_0} \right) z^{-2}}{1 + B_1 z^{-1} + B_2 z^{-2}}$$



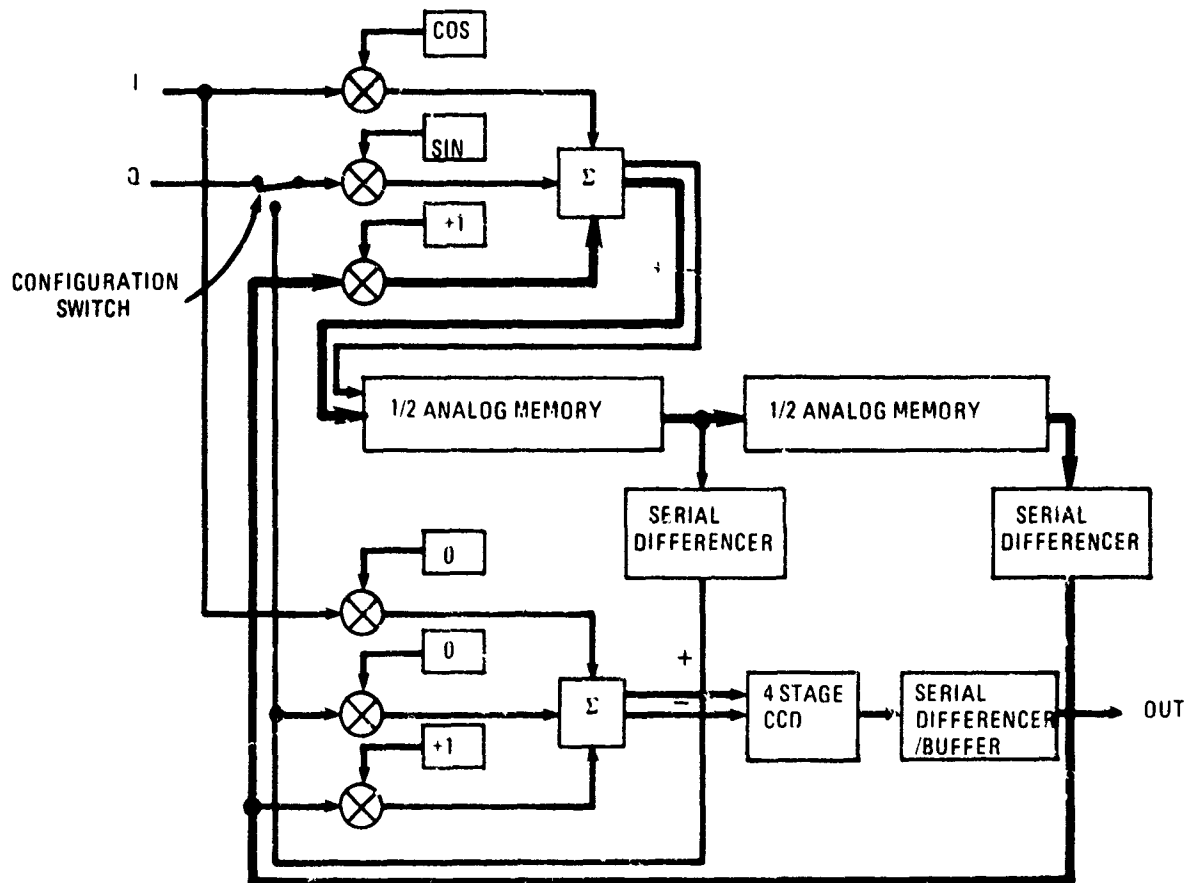
b) RECURSIVE FILTER CONFIGURATION

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Figure 7.6-1. Demonstration APUP Modes



A) TRANSFORM CONFIGURATION



B) TRANSFORM RECONFIGURED FROM RECURSIVE FILTER

80-0024 V-20

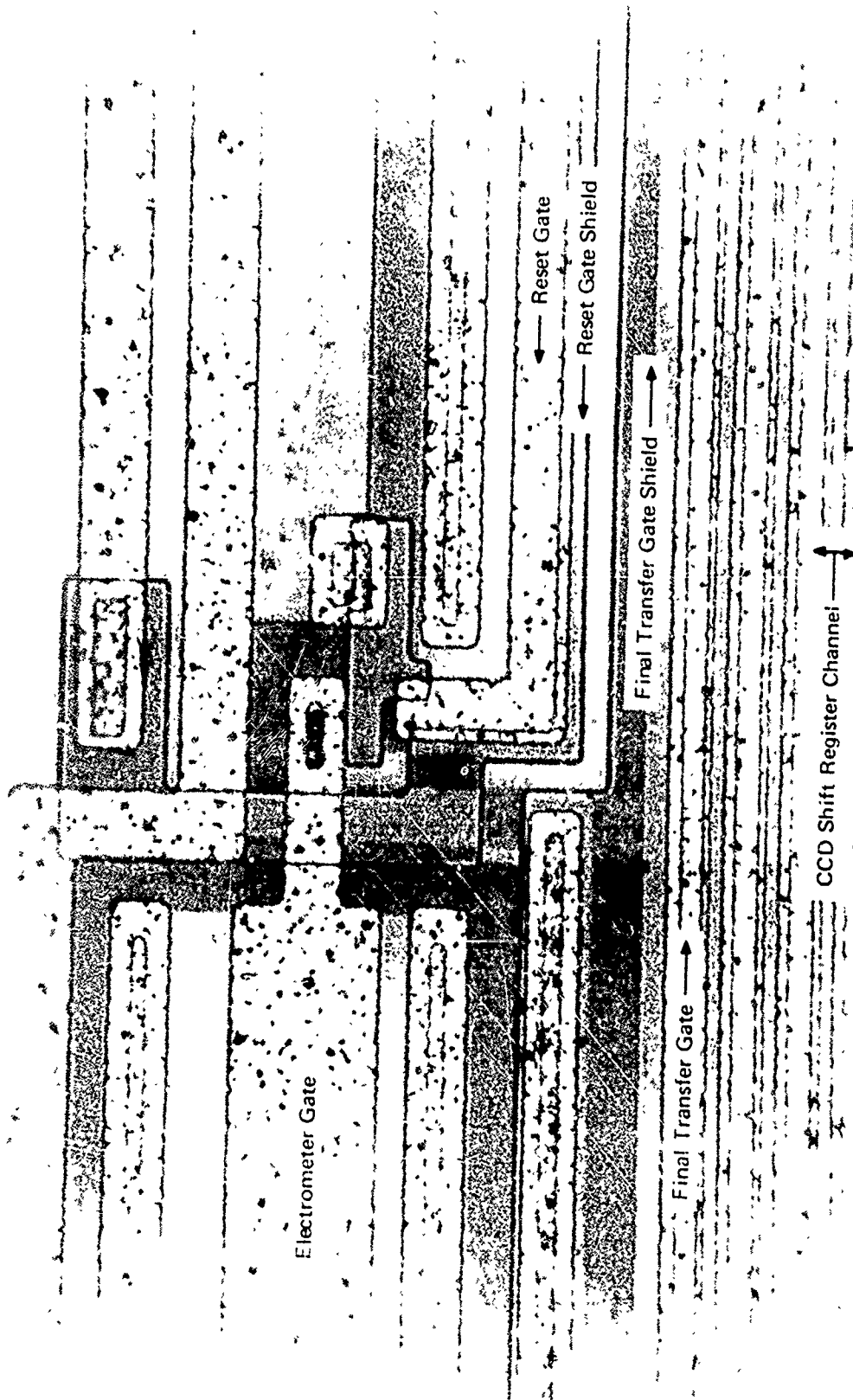
Figure 7.6-2. Demonstration APUP Modes

7.6.2 Analog-Digital Isolation

While all the low-resistance analog switches for configuration control are of the CMOS variety and remain static during the processing of any one batch of data, numerous dynamic switches like those indicated in figure 7.4-2 are repeatedly activated during processing, such as ϕ_C , ϕ_D , ϕ_{IN} , ϕ_R , etc. In each case, a capacitor is being set by a relatively low impedance source acting through the switch. It is intended to hold the applied voltage on the capacitive-high-impedance node for further processing.

Conventional MOS switches (even of the self-aligned variety) have capacitive digital gate feedthrough to the high impedance node. Nonuniformities in these feedthroughs are indistinguishable from other array offset nonuniformities and must be reduced or eliminated by differencing. Therefore, smaller feedthroughs at key points can greatly ease the further processing requirements like the accuracy of the differencing. A large inherent capacitance on such a node relative to the feedthrough capacitance naturally attenuates the amplitude of the feedthrough. Thus key nodes, susceptible to feedthrough problems, are those where minimum capacitance is dictated such as the CCD readout nodes and the MDAC-resistor ladder output nodes.

A dc-biased shield gate lying between pulsed digital gate and the high impedance analog node is very effective in reducing capacitive feedthrough. Such shields were used as early as 1976 at the output of an analog delay - and - add CCD (#7008) as shown in the photomicrograph of figure 7.6-3. The results of the shields are vividly demonstrated in the photos of figures 7.6-4 and 7.6-5, wherein the same device was used except the shields were connected to their associated pulsed waveform. Clearly, coupling from the shift-register clocks was completely removed while that from the reset switch was greatly reduced. Shielding like that described above is to be incorporated on all critical low capacitance nodes on the APUP.

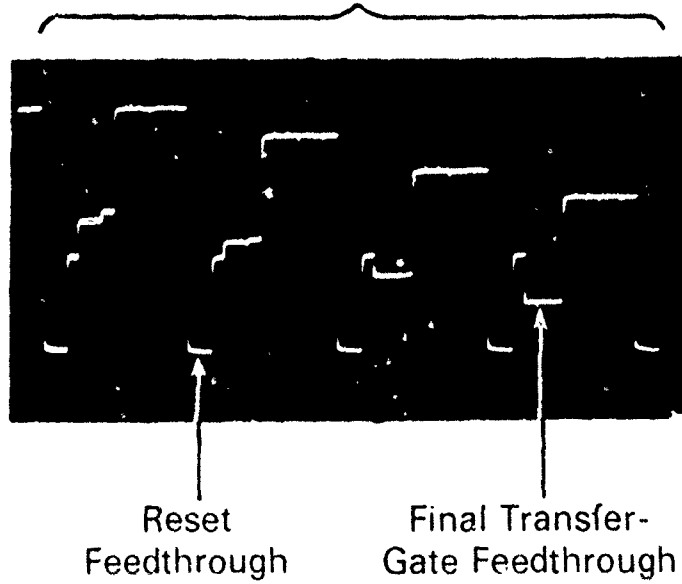


Double-Shielded Output/Electrometer

77-0211-PA-3

Figure 7.6-3. Double-Shielded CCD Output (on CCD/DAA 7008)

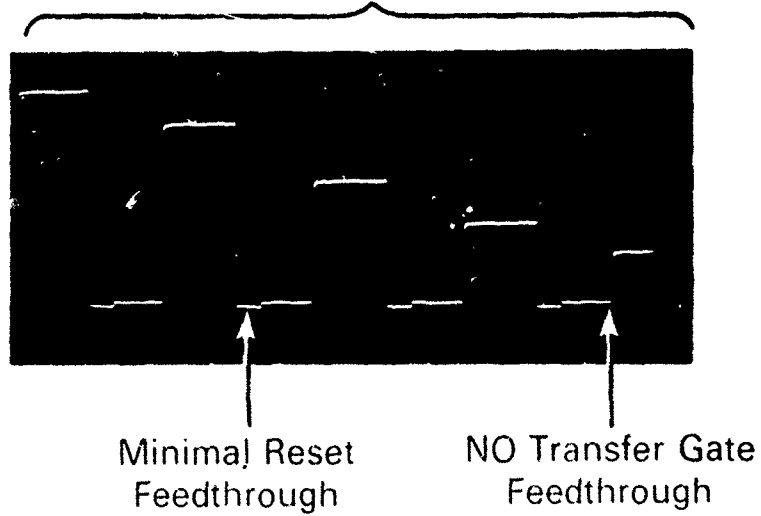
Early CCD Output Waveforms



77-0095-VG-8

Figure 7.6-4. Early CCD Output Waveforms

Double-Shielded-Output Waveforms



77-0095-VG-6

Figure 7.6-5. Double-Shielded Output Waveforms

7.6.3 On-Chip Support Circuitry

The on-chip support circuitry accepts such inputs as a master clock, an interpulse period synchronization (sync) pulse, and a batch sync pulse from which are generated all the waveforms at the proper levels as needed to operate all the remaining parts of the APUP chip. In either the high accuracy mode or the maximum data handling mode, the goal for the high-speed CCD operation is 40 MHz. Thus, the incoming master clock must be 40 MHz or some multiple thereof. Again, to minimize both area and power consumption needed for the generation of the high speed waveforms, that part of the logic is implemented in ISL technology. The waveforms so generated include, but are not limited to: high-speed CCD shift register clocks, NDRO clocks, high-speed additive refresh clocks, serial differencing and serial push/pull generation pulses, SPS lateral transfer gates, and the digital data demultiplexer/distributor.

The translation from ISL levels to MOS levels can easily be done by circuits like those pictured in figure 7.6-6, which may be described as a pseudo-complementary totempole. In one state, transistor Q3 is ON, actively pulling the driven node negative, while Q1, Q2, Q4, and M2 are all OFF. In the opposite or HIGH state, the latter group of transistors are all on while Q3 is OFF, yielding M2 and Q4 to pull the driven node positive with no opposition from Q3. Thus the dominant power consumption is dynamic, occurring only at the waveform transition edges. A plot of the transient response as simulated by ISPIICE is given in figure 7.6-7. The example described in figures 7.6-6 and 7.6-7 is intended to be simply illustrative and must be adjusted to each of the specific translator-driver requirements for APUP.

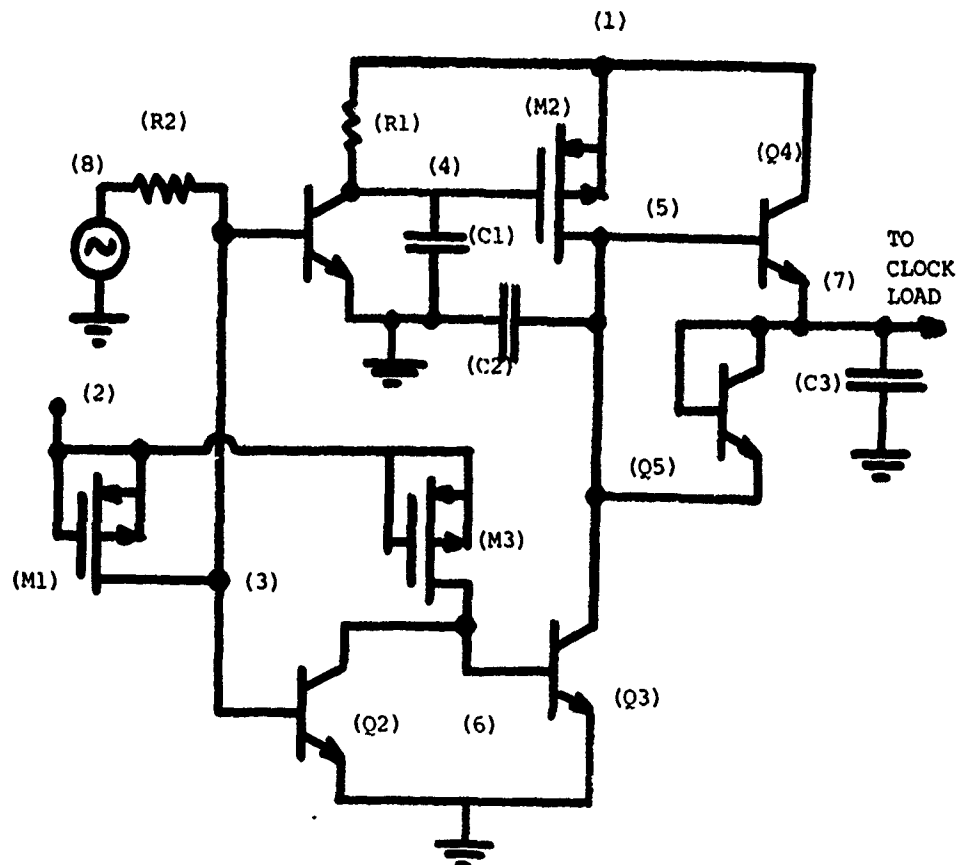
13.22.39 .EDIT DRVC CKT
 NONSTANDARD FILETYPE
 NEW FILE.

INPUT:

```
>M1 3 2 2 2 PMOSD 48E-4 4E-4
>M2 5 4 1 1 PMOS2 45E-4 3E-4
>M3 6 2 2 2 PMOSD 24E-4 4E-4
>Q1 4 203 0 BP1
>Q2 6 3 0 BP1
>Q3 5 6 0 BP5
>Q4 1 5 7 BP5
>Q5 7 507 5 BP1
>R1 1 4 10K
>R2 8 3 100
>C1 4 0 .2P
>C2 5 0 .2P
>V1 1 0 5
>V2 2 0 2
>V3 8 0 PULSE(0,.7,1N,2N,2M0N,21N,50N)
C3 7 0 10P
```

◆◆◆ NODE VOLTAGES

NODE	VOLTAGE
1	5.000D+00
2	2.000D+00
3	1.239D-02
4	5.000D+00
5	1.827D-02
6	5.605D-01
7	3.166D-02
8	0.0



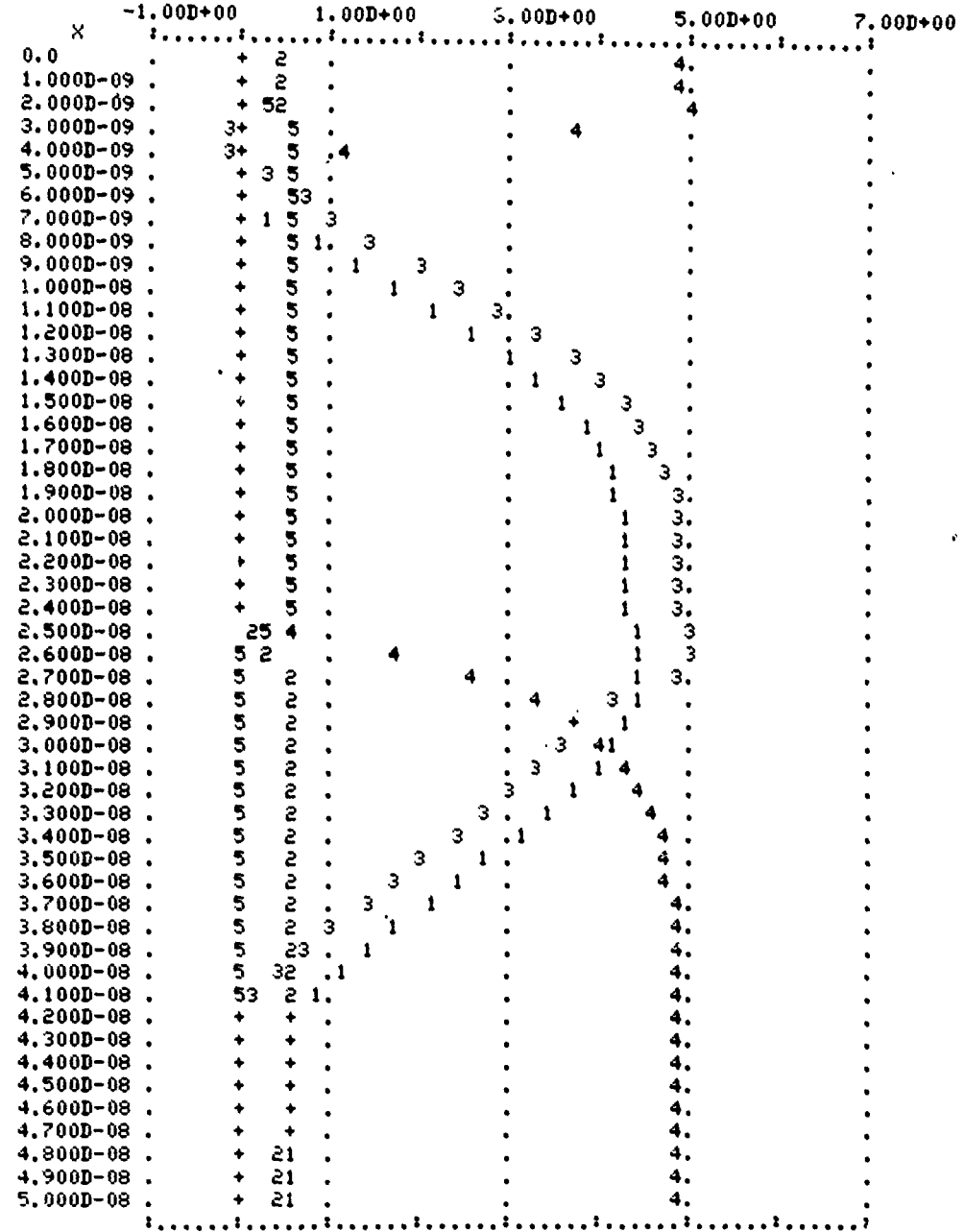
80-0024-V-16

Figure 7.6-6. A High Speed ISL to MOS Interface Circuit with Very Low Quiescent Dissipation

TRAN SIMULATION OF CIRCUIT: DRVC

LEGEND

% : TIME
 Y1 : V(7)
 Y2 : V(6)
 Y3 : V(5)
 Y4 : V(4)
 Y5 : V(3)



80-0024-V-17

Figure 7.6-7. ISPIICE Simulation of the ISL/MOS Interface Circuit for a 20-MHz Clock

7.7 TECHNOLOGY

7.7.1 PCCD Processing Considerations

Westinghouse has developed low leakage peristaltic CCD's using newly developed high lifetime epitaxial growth procedures. Using high lifetime epitaxial material, PCCD's with dark current densities as low as $10\text{-}15 \text{ nA cm}^{-2}$ have been fabricated and tested. There are three sources of dark current, two of which are related to epitaxial quality. These two are the bulk traps and the dislocations at the epitaxial substrate interface. The third contribution is from the surface traps at the Si-SiO₂ interface. Using the new epitaxial growth procedure the dislocations are reduced and the heavy metal ions in the bulk traps are gettered out. The optimum growth procedure was developed using a MOS structure consisting of an n type substrate, an n-type epitaxial layer, a gate dielectric, and aluminum C-V dots.

Capacitance-time measurements typical of that shown in figure 7.7-1 were made on this structure. Biasing the capacitor into strong accumulation and then applying a large negative voltage drives it into deep depletion, creating a space charge region. Thermal generation of hole-electron pairs occurs with the holes drifting to the Si-SiO₂ interface to form an inversion layer, while the electrons drift to the neutral bulk to neutralize the ionized donor atoms. Modelling this MOS structure as a series combination of an oxide capacitance and a depletion layer capacitance, the total capacitance changes with time until an inversion layer forms. The time it takes for the inversion layer to form, t_F , is related to the minority carrier lifetime by $\tau_g = 0.9 \times 10^{-6} t_F$ (seconds). Prior to the development of the high lifetime epitaxial material, lifetimes of approximately 75 μsec were typical. Using

(MOS CAPACITOR ON N-TYPE EPITAXIAL LAYER WITH
1200 °C HCL ETCH BEFORE EPI GROWTH, PH₃ GETTER AFTER EPI)

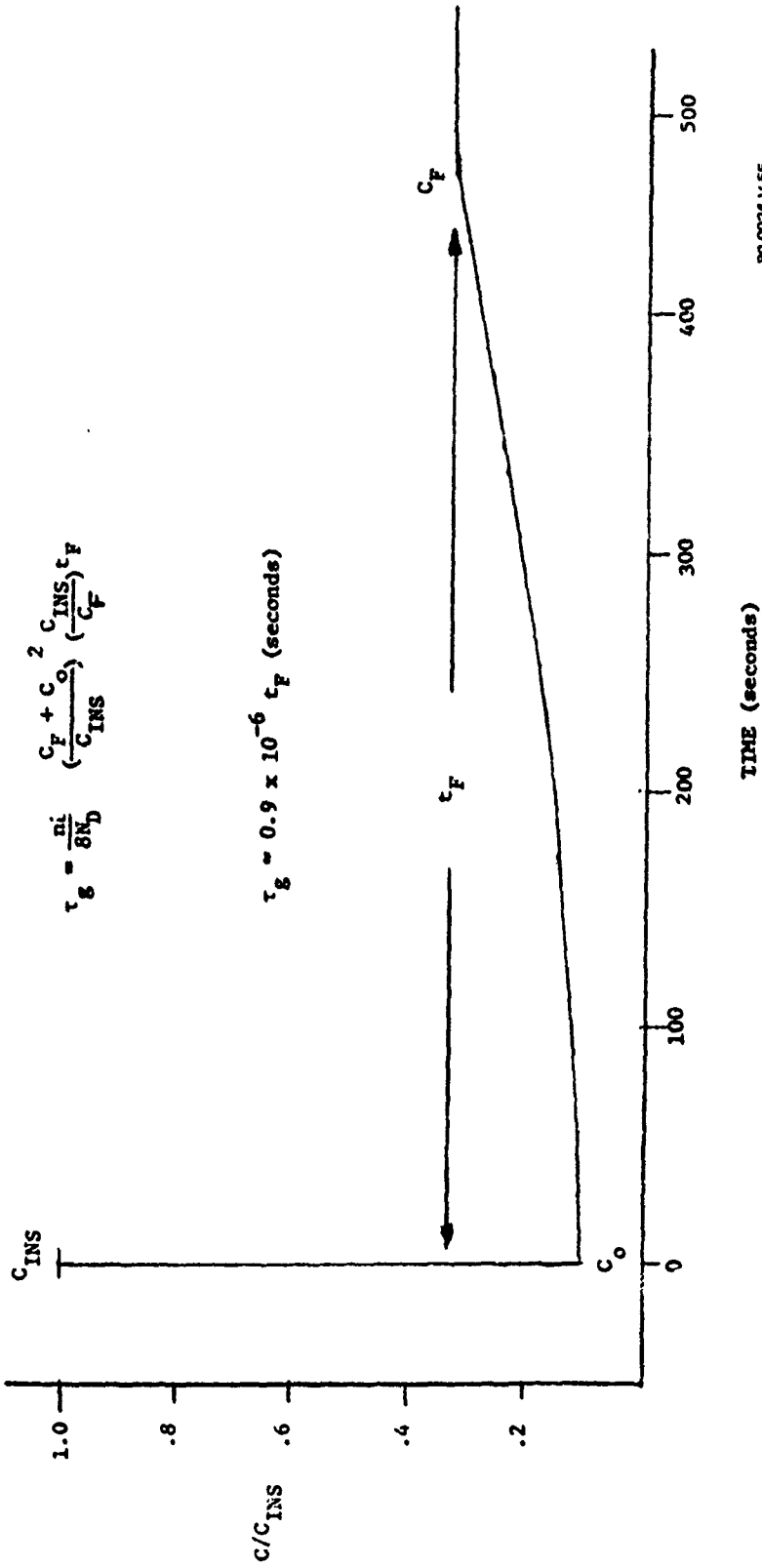
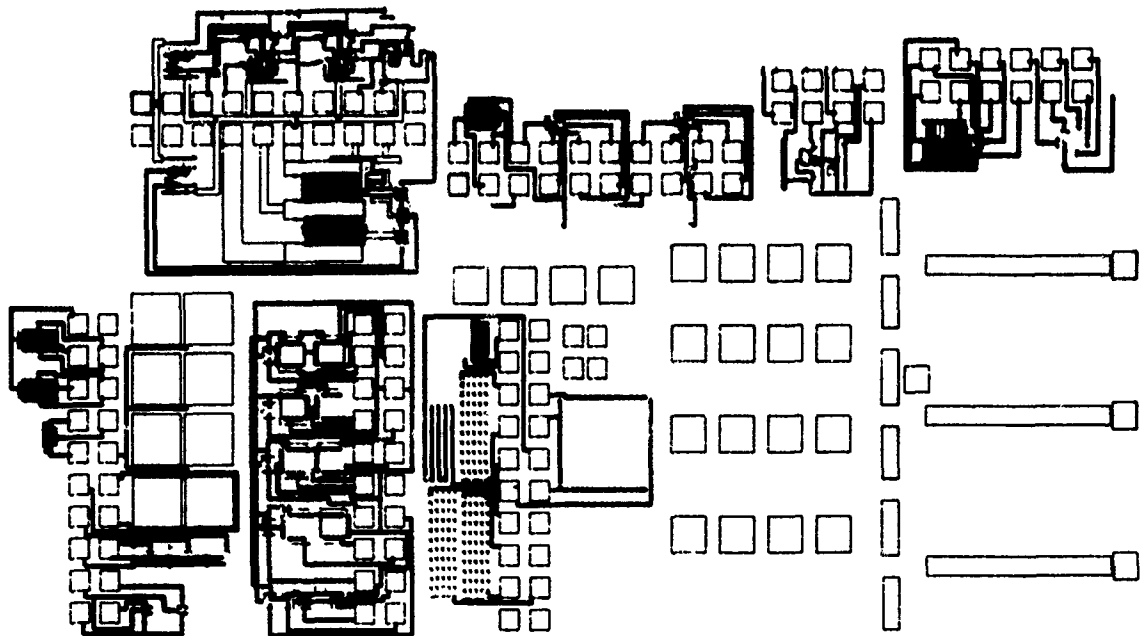


Figure 7.7-1 Capacitance - Time Curve

the newly developed process, the substrate receives a 1200°C HCl etch and no 1200°C pre-bake before epitaxial deposition. Lifetimes as high as $500\ \mu\text{sec}$ have been observed for this epitaxial material which is as good as that obtained on virgin silicon.

7.7.2 Test Vehicles and Structures

Westinghouse has developed test patterns to monitor processing and to determine optional processing parameters and operating biases for PCCD. An example of a test pattern developed for PCCD's, MOS, and ECL devices is the high speed CCD test pattern shown in figure 7.7-2. This test pattern includes various capacitors, gated diodes, dog bones, MOSFETS, and bipolar structures. There are MOS capacitors using different polysilicon or metal levels over the epitaxial layer or the epitaxial implanted with the graded implant or barrier. C-V measurements from these capacitors gives an idea of the various surface state densities and threshold voltages involved. Another test structure included is the gated diode with polysilicon gates over the graded or graded and barrier-implanted epitaxial body. C-V measurements on these



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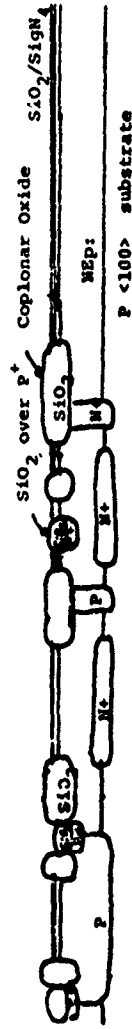
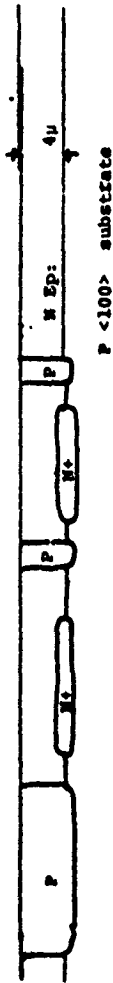
Figure 7.7-2. Test Pattern for PCCD, MOS, and ECL Combined Process

gated diode structures is a means of determining implant profiles and the optimum source, drain, and gate voltages. Gated diodes are also used to determine contributions to leakage from defects in the bulk, depletion region and surface states. Measurement of depletion MOSFETS gives flatband voltages, implant channel doping and depth, and bulk and surface carrier mobilities. These parameters are applicable to the PCCD's fabricated with the MOSFETS. These MOSFETS include various $\frac{W}{L}$ ratios with polysilicon or metal gates using an epitaxial channel. Dogbones for the P+ diffusion, the N epi, N+ emitter, first polysilicon, and second polysilicon give an accurate measure of the various sheet resistances. Integrity tests include contact windows to first polysilicon, second polysilicon, P+ diffusion, N+ emitter, short tests between first and second polysilicon, and step coverage metal over polysilicon steps and polysilicon over iso-planar oxide. Also, on the test patterns are ECL bipolar structures including a CCD driver, NOR gates, inverters, bipolar input test structures, and a bandwidth test structure.

7.7.3 Chip Fabrication

Westinghouse will use its unique process technology to produce PCCD circuits that include ISL and CMOS circuits providing increased circuit density, increased speed, and minimum off-chip support circuitry. The process sequence starts with a P-type (100) wafer upon which an arsenic implant is performed for the ISL's sub-collectors (see figure 7.7-3). An N-type, 4-micron thick epitaxial layer is then grown over these sub-diffusions using procedures specifically developed to achieve high lifetimes. A masking oxide is next grown and regions for P isolation diffusions are defined. The P isolation diffusions will serve the purpose of isolating separate devices, channel stop for the PCCD's, and in addition, will provide the N-type body for the N-channel MOSFET's. After this step a P⁺ base contact diffusion, followed by an oxidation that will be used for the oxide aligned emitters, is performed. Following a photo mask step, arsenic is implanted into the channel region of the CCD's to increase the CCD charge handling

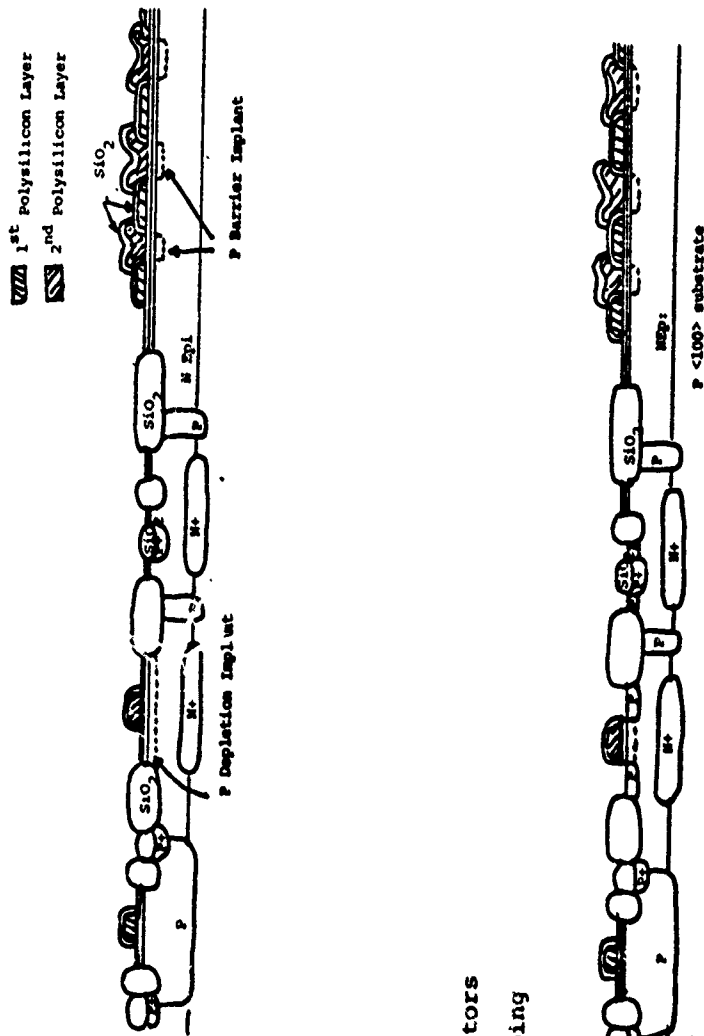
1. 6KÅ Oxidation
2. Photo 1 Define N⁺ Subdiffusion
3. Arsenic Ion Implant
4. Implant Anneal and Drive, Strip Oxide
5. N-Type Epitaxial Deposition (4μ)
6. 6KÅ Oxidation
7. Photo 2 Define P Isolation Diffusion and N Channel Body
8. Boron Implant
9. Implant Anneal and Drive (6μ) 16 cm⁻³ (Surface concentration 2 X 10¹⁶ cm⁻³)
10. Masking Oxide/Nitride
11. Photo 3 Define coplanar oxide region
12. 12KÅ Oxidation
13. Photo 4 Define P⁺ Diffusion for base resistance lowering and emitter Oxide alignment
14. Boron Implant
15. Implant anneal
16. 4KÅ Oxidation over P⁺
17. Strip Nitride, Arsenic Implant for Graded Implant to Increase Charge Handling In CCD
18. 800Å Nitride/10KÅ Silox



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Figure 7.7-3. Monolithic Oxide Aligned ISL/PCCD Technology (Sheet 1 of 3)

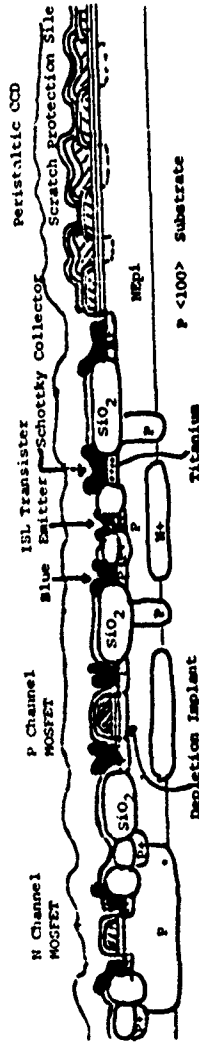
19. Implant Anneal
20. Strip Oxide from Wafers Backs
21. Phosphorous Backside Getter/
Strip Silox-Nitride
22. Silox on Backside to prevent
auto doping
23. 500Å Gate Oxide
24. 1000Å Gate Nitride
25. Polysilicon Deposition and
Phosphorous Doping
26. Photo 5. First Polysilicon
Definition
27. 1.8KÅ Poly Oxidation
28. Boron Implant for Two phase
Barriers, P Buried channel
of P Channel Depletion Transistors
29. Polysilicon Deposition and Doping
30. Photo 6. Second Polysilicon
Definition
31. 3KÅ Poly Oxidation
32. Photo 7. Nitride Removal from
Bipolar Emitter/Base Regions
and P channel Source and
Drain Regions
33. Boron Implant
34. Implant Anneal
35. 1.5KÅ Nitride Layer



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Figure 7.7-3. Monolithic Oxide Aligned ISL/PCCD Technology
(Sheet 2 of 3)

36. Photo 8. Nitride Removal from Bipolar Emitter/Base Region and N-Channel Source and Drain Regions
37. Arsenic Implant (The 1.5kÅ Nitride protects the P Channel Source and drain)
38. Implant Anneal
39. Photo 9. Contact windows to p⁺ and N⁺ Diffusions and Schottky Collectors
40. Deposit Titanium
41. Photo 10 Define Titanium over Schottky Collectors
42. Deposit Aluminum/Silicon/Copper
43. Photo 11 Define Metal Interconnect
44. Sinter Aluminum at 425^oC
45. 10kÅ Scratch Protection Silox
46. Photo 12. Vias to Bonding Pads.



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Figure 7.7-3. Monolithic Oxide Aligned ISL/PCCD Technology (Sheet 3 of 3)

capability. After this, a back side phosphorous getter is performed to minimize leakage in the PCCD's. The gate dielectric, oxide and nitride, is next grown. The first polysilicon is deposited, doped with phosphorous, defined, and etched. After etching, the first polysilicon layer is oxidized. Before depositing the second polysilicon, boron is implanted into the CCD channel using the first polysilicon as an implant mask. This implant gives the PCCD's built-in directional ability, allowing two or more and one-half phase clocking. The boron implant also provides the channel for the P channel depletion mode MOSFET's. After the implant, a second layer of polysilicon is then oxidized. Gate nitride is removed from the bipolar emitter/base regions and the P channel source and drain regions. A boron implant is performed and annealed. Following this step, a nitride layer is deposited and defined to remove nitride from the bipolar emitter/base regions and the N channel source and drain regions. Arsenic is then implanted. The contact windows to the P⁺ and N⁺ diffusions, to the polysilicon, and to the Schottky collectors are next opened up. Titanium is then deposited and defined for the interconnects. The last process step is to deposit and define a silox.

The process techniques that have already been successfully demonstrated include graded channel PCCD's with boron implanted barriers for two phase or one and a half phase operation. In addition, on-chip emitter-coupled logic transistors and PCCD's have been successfully combined for the High Speed CCD Program sponsored by the Naval Research Labs. The processing procedure used in the High Speed CCD Program is similar to that to be used for the Analog Programmable Microprocessor (APUP). Features of the fabrication process that have to be combined with the present High Speed CCD process are titanium Schottky collectors and the self-aligned N and P channel MOSFET's. Integrated Schottky logic transistors using titanium Schottky collectors have been demonstrated at Westinghouse on a universal gate array chip. The titanium Schottky collectors would be combined with the High Speed CCD process by opening a contact window to silicon

and defining titanium over the collector region. The processing procedures for forming the self-aligned N channel and P channel MOSFET's using the base and emitter implant along with the intervening nitride layer should not pose any serious processing problem. Westinghouse has fabricated other types of CCD's combining multiple technologies. An CCD Adaptive Filter Chip sponsored by NRL using on-chip CMOS clock logic circuits, P-channel CCD, and substrate bipolar transistors has been fabricated. The minority carrier storage time for this process was approximately 150 microseconds, demonstrating that the high temperature P well drive does not degrade lifetimes as long as the drive is followed by a phosphorous getter. Several processing techniques are presently being investigated for a combined ECL/PCCD Imager Pre-processor chip sponsored by the Naval Research Labs. The use of a phosphorous-doped reflowed silox procedure allows the metal interconnect lines to lie on top of a thick silox layer and thus have reduced capacitance. An additional process that is being investigated is an argon ion implant getter into the back side very near the end of the process. Both of these techniques will be available to be used on the Analog Programmable Microprocessor Program.

7.7.4 Area and Power Projections

The main analog components of the APUP Transform/Filter chosen are: Charge-Coupled MDACs (CC MDAC), CCD analog shift registers (S/R) of the serial-parallel-serial (SPS) configuration, input/output buffers, and interconnect buses and analog interconnect switches. CCMDAC's are used on (1), (2), (3). Copeland, et al., (1) have a summing array of 32 CCMDAC's, each with 8-bits amplitude and 1-bit sign, as well as the remainder of the operating circuitry, on a 171 mil x 191 mil chip, yielding less than $1000(\text{mil})^2$ per 9-bit CCMDAC. Pettengil, et al., (2) have four CCMDAC's each with 10-bit resolution and requiring about $1400(\text{mil})^2$ each. The Transform/Filter APUP needs two summing MDAC's, each with three

inputs and a resolution of 8-bits amplitude and 1-bit sign. The larger value of 1000 (mil)^2 , rather than $700 \text{ (mil)}^2 = 1/2 \times (1400 \text{ (mil)})^2$ includes a simple static shift register with no added latch to facilitate faster effective operation. Thus an added allowance of 750 (mil)^2 provides the area needed for the nine latches for each MDAC input. The total MDAC plus digital "coefficient" registers require $6 \times (1000 + 750) = 10,500 \text{ (mil)}^2$.

A commercially available CCD analog SPS array is described in (4), while another CCD area array is described in (5). Reference (4) also gives projections of defects or blemishes to be anticipated in such large SPS CCD analog memories. In both arrays, the average area per memory cell is about 2 (mil)^2 . On that basis, the area required for the 8192 memory cells is about $16,384 \text{ (mils)}^2$, which does not include the clock interconnect structure. Further extrapolation from reference (2), incorporating some adjustments for the higher-speed, smaller-area characteristics of some bipolar circuit elements, gives these preliminary area estimates: registers, switches, and latches for the "Command/Configuration Control" switches $\sim 4800 \text{ (mil)}^2$, input and output buffers $\sim 6000 \text{ (mil)}^2$, clock drivers $\sim 400 \text{ (mil)}^2$. All five major contributions add to $41,700 \text{ (mil)}^2$. With careful, personalized layout an overhead burden for interconnection regions as low as 50% may be achieved. Consequently the overall chip area is likely to around $(1.5) (41700) = 62,500 \text{ (mil)}^2$. which is exactly a quarter inch chip, typical of large scale integrated circuits. These projections, as well as for the R-2R MDAC approach, are summarized in table 7.7-1.

The power consumption tabulation presented in table 7.7-2 indicates that the chip will dissipate 627 mW when fully operating at rated speed. This is quite reasonable but it may require external heat sinking to meet full MIL-SPEC operation.

TABLE 7.7-1
SUMMARY OF APUP AREA PROJECTIONS

<u>GENERIC PART</u>	<u>AREA (INCH² x 10⁻⁶)</u>		
CCD ANALOG MEMORY			16,400
MDAC's: CAPACITANCE - OFFSET ZERO	10,500		
CAPACITANCE - REFERENCE STEERING		5,250	
R-2R ATTENUATING RESISTOR LADDER			4,200
INPUT AND OUTPUT BUFFERS			6,000
WAVEFORM GENERATION AND DRIVER/TRANSLATORS			4,000
CONFIGURATION COMMAND REGISTERS, LATCHES, SWITCHES			4,800
SUBTOTALS:	41,700	36,450	35,400
50% OVERHEAD FOR EFFICIENT PERSONALIZED LAYOUT AND INTERCONNECT	20,850	18,225	17,700
OVERALL TOTAL	62,550	54,675	53,100
(AREA) ^{1/2}	(.250" x .250")	(.234" x .234")	(.230" x .230")

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TABLE 7.7-2

POWER BUDGET TABULATION

- CCD Digital Control Clock Drivers
 - Quiescent. For each waveform, $0.2 \text{ ma} \times 2 \text{ volts} = 0.4 \text{ milliwatts PLUS } (5 \text{ volts})^2 / 10000 \text{ ohms} = 2.5 \text{ milliwatts}$ (only during the "active LOW" state).
 - No. of waveforms: 2 fast clocks. 2 slow clocks. 4 parallel transfer gates. 3 NDRO clocks, input sampling, 2" additive refresh" clocks, serial differencing, serial push/pull generation.....totalling 16 waveforms
 - Active low duty factor, is 50% for 2 clocks. (1/32) for parallel transfer, 50% for additive refresh, (1/8) for input sampling, serial differencing & serial push/pull generation and (1/2 + 1/4 + 1/8) for NDRO
 - Subtotal: $(16) \times (0.4) + (2.5) \times (16) = 16.1 \text{ milliwatts}$
 - Dynamic. Basis = 4 micron gate length with depletion capacitance about $C_0/10$; on-micron overlap; equal total area for interconnect but with field dielectric at $10K \times$ instead of K . Thus adjustment is $[(1/5) + (0.1) (4/5) + (1/10)] = 0.4$ for fast horizontal registers; for slower column $A_{f,\phi} = (8 \text{ registers}) \times (40 \text{ cells}) + (1+5+13) \text{ turn cells} \times (32 \mu \text{ wide}) \times (5 \mu \text{ long}) = 84.1 \times 10^{-6} \text{ in}^2$, so $C_{f,\phi} = 7.1 \text{ pFd}$. (for all fast horizontal clocks, per phase)
 - $A_{s,\phi} = (20 \text{ columns}) \times ((896 \text{ rows}) \times (37 \mu \text{ wide}) \times (5 \mu \text{ long})) = 4444 \times 10^{-6} \text{ in}^2$, so $C_{s,\phi} = 284 \text{ pFd}$. (for all slow column clocks, per phase).
 - For additive refresh & serial push/pull at 10 MHz, we have f (fast) = 40 MHz and f (slow) = $4 \times 10^7 / 10 = 4 \text{ MHz}$.
 - For 5 volt clock swings the reactive power becomes $\Sigma CV^2f =$
 - FAST: (2 phases) (7.1 pFd) (25 volts²) (40 MHz) = 14.2 milliwatts
 - SLOW: (2 phases) (289 pFd) (25 volts²) (4 MHz) = 57.8 milliwatts
 - For 75% efficient (class B) drivers, the resultant heat dissipation is 96 milliwatts.
- Digital Data Demux and Storage (ISL, at 30 MHz) (about 750 transistors) $\times (0.1 \text{ ma}) \times (2 \text{ volts}) = 150 \text{ milliwatts}$
 - CMOS Clock generation and housekeeping/control logic (negligible quiescent) (about 100 inverter equivalents) $\times (0.5 \text{ pFd per node}) \times (25 \text{ volts}^2) \times (10 \text{ MHz}) = 12.5 \text{ milliwatts}$
 - CMOS Processor configuration command logic
Negligible Quiescent; data changes only when processor configuration is modified (assumed rather infrequently).
 - Analog MOS bipolar circuits
CCD NDRO serial differencing tap buffers: (4 taps) $\times 9.2 \text{ mw} = 36.8 \text{ milliwatts}$
Output serial differencer/buffer: $9.2 \text{ mw} + 14.5 \text{ mw} = 23.7 \text{ milliwatts}$
MDAC push/pull generator & current copies: (6 MDACS) $\times 48.6 \text{ mw} = 291.6 \text{ milliwatts}$
 - Summary (at 20 MHz Sampling Rate)

CCD and MOS drivers	Constant (mw)	Frequency Dependent (mw)
Multiplier Coefficient (Digital) Handling (ISL)	16.1	$12.5 + 96 = 108.5$
Analog MOS -- Bipolar Circuitry	150 (more power needed for speeds above 30 MHz)	
Subtotals	352	
Total	518.2	108.5
		627 milliwatts

7.8 OPERATIONS WITH HOST MICROCOMPUTER

7.8.1 Host Microcomputer Proposed

Westinghouse has made extensive use of the Intel 8080-based single-board computer (SBC) hardware in its commercial system designs. We have in-house software assembler systems and ROM programmers available for developing the host computer programs to demonstrate the APUP operation.

We propose to use an Intel SBC 80/10A microcomputer (see figure 7.8 in a standard Intel molded 4-slot card cage (figure 7.8-2). A standard Intel SPC 635 power supply will provide all voltages needed by the computer hardware. Type 2708 EPROM's will be written directly from the MDS development system used to assemble and debug the program. A control switch bank will be connected to one port of the 80/10A and continually interrogated by the program. The modes of operation will be determined by these switches.

Needless to say, any such experimental demonstrator as this one will be in a continual state of flux as new modes are created and tested, so it is very convenient to have a software development system immediately available for updating the program on disk and rewriting the EPROM's. Westinghouse has an Intel Microcomputer Development System (MDS) similar to that in figure 7.8-3, located in another Baltimore plant and accessible for software assembly and modification.

The software is written in 8080 assembly language and may be stored on a floppy disc in the MDS. It may be "run" within the MDS for initial debugging purposes using the "GO FROM START" command in the EMULATOR mode. Once this appears satisfactory, the actual SBC hardware may be coupled to the MDS removing the 8080 DIP itself and plugging the ICE (In-Circuit Emulator) cable into its socket instead (figure 7.8-4).

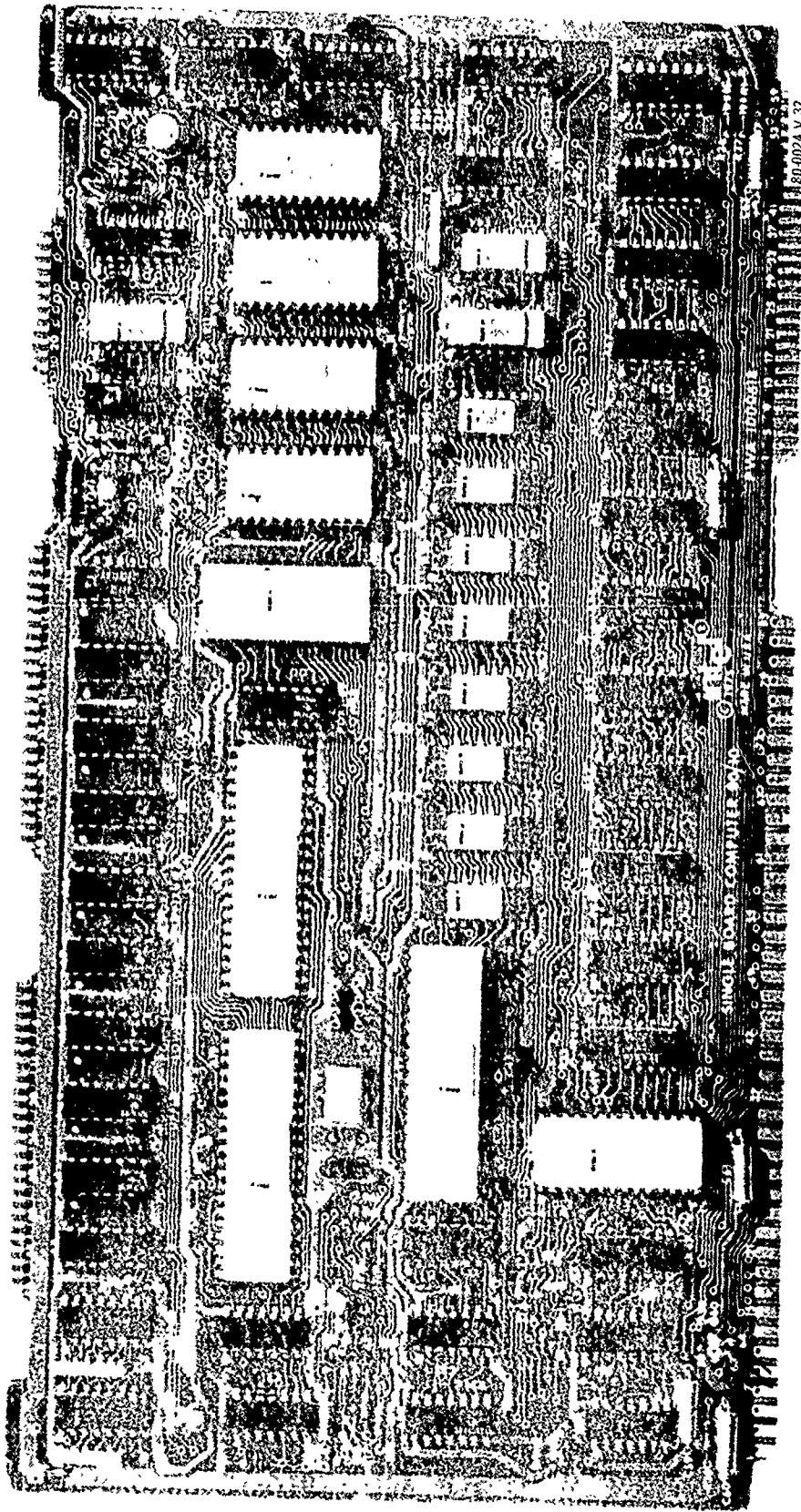


Figure 7.8-1. Intel SBC 80/10A Microcomputer

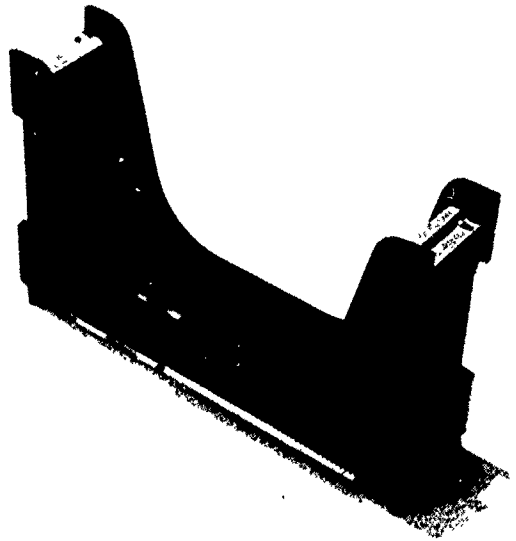
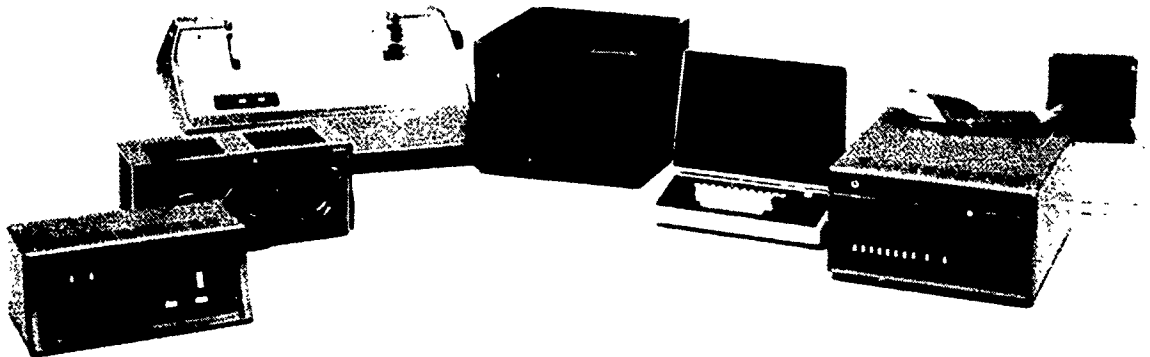
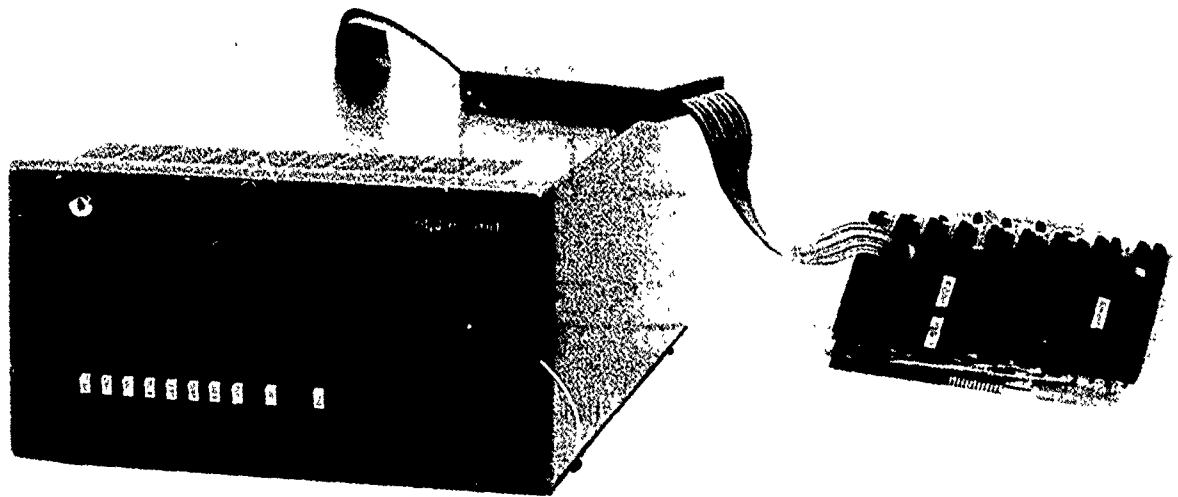


Figure 7.8-2. Intel 4-Slot Card Cage



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Figure 7.8-3. Intel Microcomputer Development System (MDS) Used by Westinghouse in 8080 Software Generation



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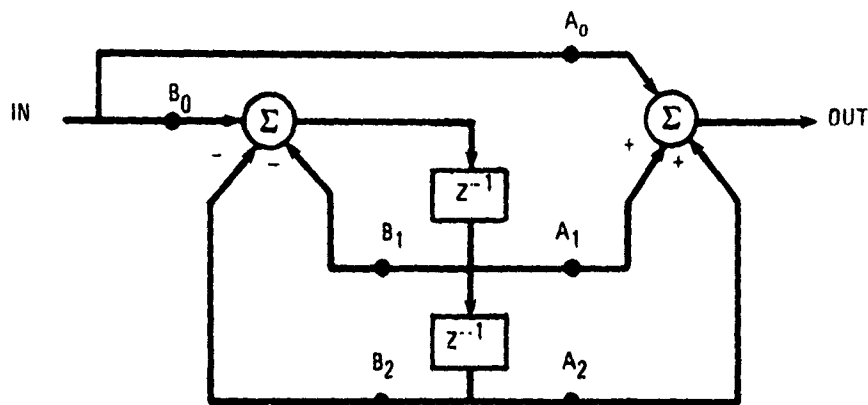
Figure 7.8-4. Intel In-Circuit Emulator (ICE) Operating a Microcomputer System in Its Own Card Cage Using the Software Under Development

(The SBC time-out circuit has to be jumpered as well.) Now the ICE program may be used to operate the microcomputer albeit at a reduced rate, directly from the software being debugged. After this passes all tests, an EPROM may be loaded with the debugged software and then plugged into the SBC for full-speed operation. The MDS is available for reprogramming the EPROM whenever a program extension is made.

7.8.2 APUP Demonstration Mode

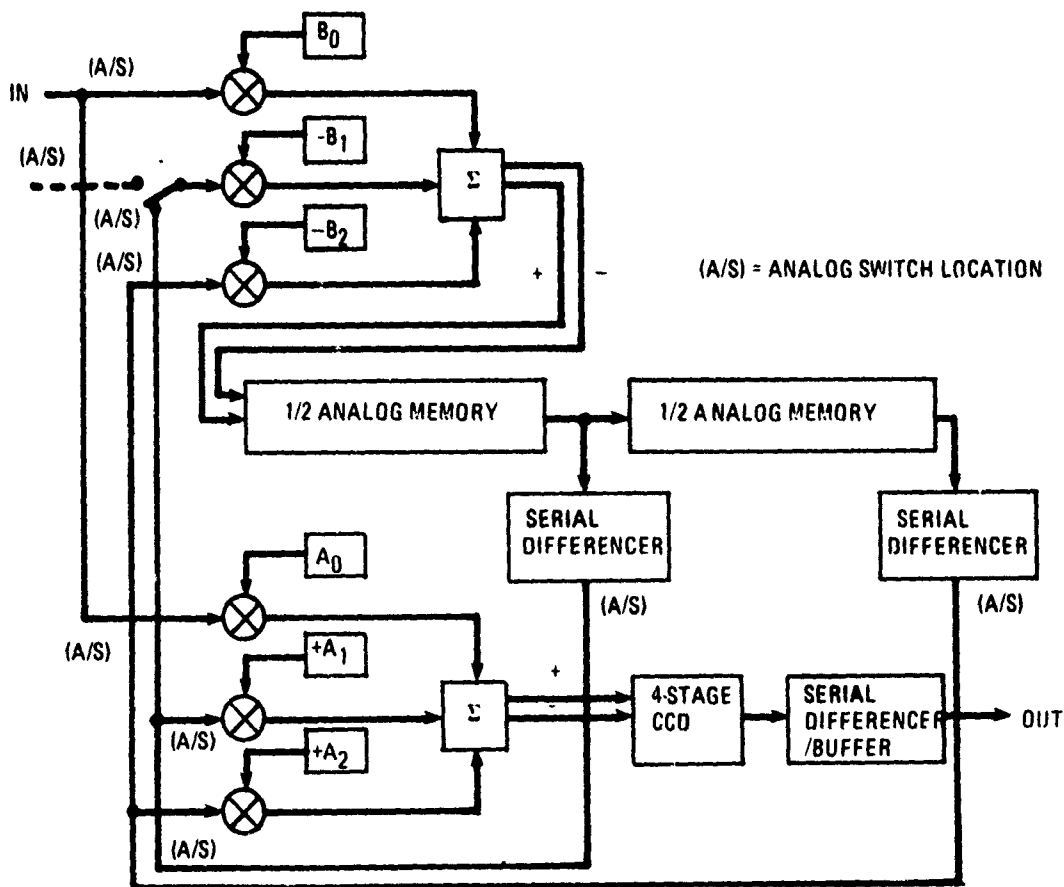
The 2-Pole recursive filter presented earlier in figure is a redrawn here as figure 7.8-5. The canonical form is shown in (a), but for hardware reasons, the unity-gain path between summers is deleted and instead, the input signal is presented to both summers, only with different gain factors. The revised transfer function is

$$H(Z) = A_0 \frac{1 + (B_1 + B_0 \frac{A_1}{A_0})Z^{-1} + (B_2 + B_0 \frac{A_2}{A_1})Z^{-2}}{1 + (B_1)Z^{-1} + (B_2)Z^{-2}}$$



a) 2ND ORDER RECURSIVE FILTER

$$H(z) = A_0 \frac{1 + \left(B_1 + B_0 \frac{A_1}{A_0} \right) z^{-1} + \left(B_2 + B_0 \frac{A_2}{A_0} \right) z^{-2}}{1 + B_1 z^{-1} + B_2 z^{-2}}$$



b) RECURSIVE FILTER CONFIGURATION

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Figure 7.8-5. Demonstration APUP Modes

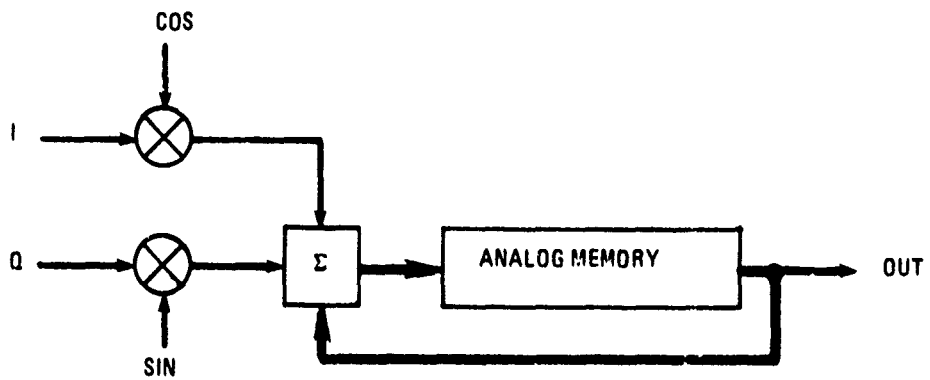
The hardware implementation is shown in figure 7.8-5b. The six multiplier gain factors are constants, loaded initially via the host computer. (The computer itself was loaded via toggle switches and interrupt instructions in the initialization mode.) Once loaded, this recursive filter is "independent" of the computer, so its speed is dependent only on the analog memory clocking speed and length (taps chosen).

In order to demonstrate the programmability feature, refer to figure 7.8-6. Here we have a transform configuration, a complex input with cisoidal multiplication and an integrate-and-dump filter. As presented, it is a discrete Fourier transformer, but the same transform configuration could, for example, use a Walsh function input signal if wal and cal multiplication factors are provided by the computer. Note that the hardware configuration is identical to that of the recursive filter. With the exception of a single input switch to one multiplier. Of course, the multiplier factors are changed (and the analog memory taps, probably), and two of these factors are non-constant and continuously supplied by the computer.

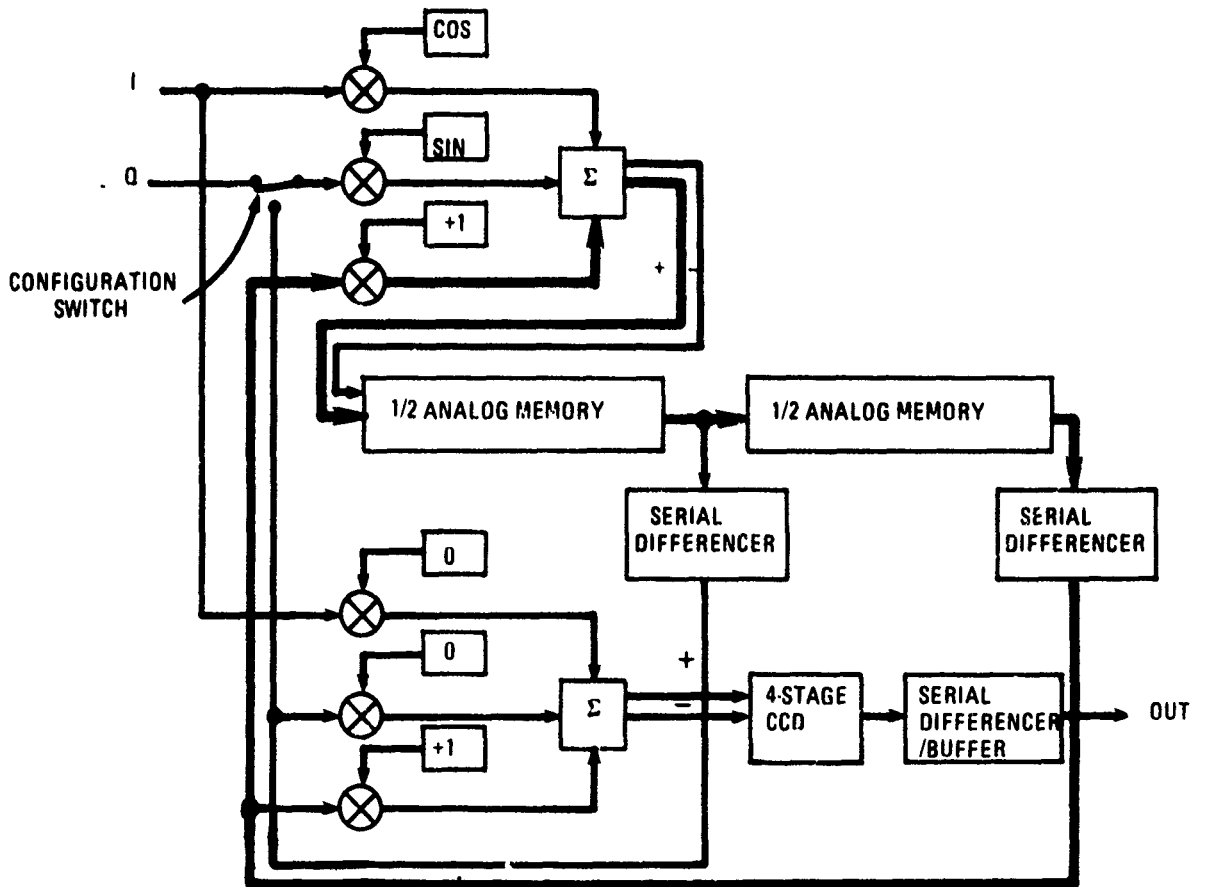
The transform mode is complex. The inputs are inphase and quadrature (I & Q) while the cisoidal multipliers can be shifted 90 degrees in phase for two multiplies and shifts per input sample so that the circuitry sample pairs represent the answers in rectangular coordinates. The summer becomes a subtractor for the "imaginary" half of the computation by changing the sign bit on the multiplier. The integrator is "dumped" by opening the recirculation path (multiplier equals zero).

The APUP in this configuration can perform as a store-delay-and-forward element by using the multipliers as "valves" to accept an input data stream, then open the input and close the recirculation path with unity gain. After the delay time, the output port is opened and the stored data presented.

For post-detection video enhancement, the same delay recirculation could be used only with continuous input and less-than-unity gain in the feedback loop.



A) TRANSFORM CONFIGURATION



B) TRANSFORM RECONFIGURED FROM RECURSIVE FILTER

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Figure 7.8-6. Demonstration APUP Modes

The control switches will direct the microcomputer to reconfigure the APUP to various digital filter forms, e.g., one-and two-pulse MTI or other 2-pole filter forms and discrete integral transform or integrate-and-dump filters, the fixed coefficients of which are selected by other switches. The Intel SBC can generate the required multiplier values, probably by table look-up, but its input rate in this service will limit the APUP to perhaps 10 kHz in transform mode. (The MDAC rate with fixed coefficients has no such limitation).

The test signals applied to the APUP input can be pure tones from a laboratory oscillator at first. Later, the SBC can be programmed to fabricate a controlled test waveform synchronized to the coefficient generation. Known "noise" may be computer-generated and added in as well so that the processing gain can be directly measured. Controlled input waveforms facilitate the measurement of frequency response, sidelobe spreading, SNR improvement, and residual noise.

7.9 REFERENCES

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APPENDIX 1.0

LIST OF ABBREVIATIONS

A/A	Air-to-Air
A/C	Aircraft
ADC	Analog-to-Digital Converter
A/G	Air-to-Ground
AGC	Automatic Gain Control
A/G/M	Air-to-Ground Mapping
A-O	Acousto-Optics
AWI	All Weather Interceptor
Az	Azimuth
BITE	Built-In Test Equipment
CCR	Correlator Doppler Filter Channel Data Rate
CDR	Correlator Input Data Rate
CFAR	Constant False Alarm Rate
CMOS	Complementary Metal-Oxide Semiconductor
CPNR	Clutter-Plus-Noise Region
CT	Corner Turn
CTD	Charge Transfer Device
DAC	Digital-to-Analog Converter
DBS	Unfocused Doppler Beam Sharpening
DFT	Discrete Fourier Transform
D _H	Radar Antenna Horizontal Dimension in Feet
DCA	Direction of Arrival
DTE	Digital Target Extractor
EAR	Electronically Agile Radar
ECCM	Electronic Counter Countermeasure
ECM	Electronic Countermeasures
E-O	Electro-Optics
EW	Electronic Warfare

f_c	Correlator or Doppler Filter Bandwidth
Δf_{DOP}	Total Doppler Signal Bandwidth required to give r_{az} ; if there is azimuth multilooks it must be multiplied by N.
FFT	Fast Fourier Transform
FIT	Fault Isolation Test
FLIR	Forward Looking Infra-Red
f_p	Prefilter output data rate
F_{PF}	Chirp superimposed on signal if prefilter is scanned
Δf_{PRE}	Prefilter Bandwidth
F_{SCAN}	Doppler frequency offset of a DBS antenna subbeam
FSE	Fractionally-Spaced Equalizer
F_{SIG}	Chirp on signal due to doppler
FTAT	First Time Around Target
FTC	Fast Time Constant
$h_{a/c}$	Aircraft Altitude
I	Inphase Signal Component
IF	Intermediate Frequency
IFF	Identification, Friend or Foe?
I^2L	Integrated Injection Logic
IPP	Radar inter-pulse period in seconds
ISL	Integrated Schottky Logic
K	Antenna beamwidth spreading factor due to illumination taper
KB	Kilo Bits
K_{OS}	Over Sampling Factor
K_s	Increase in magnitude due to amplitude weighting
LLTV	Low Light-Level Television
LORO	Lobe on Receive Only
M	Unfocused DBS Ratio
MDAC	Multiplying Digital-to-Analog Converter
MOS	Metal Oxide Semiconductor
MTAE	Multiple Time Around Echo
MTD	Moving Target Detection

MTI	Moving Target Indicator
MW	Total map width or spot width in feet
N_{CC}	Number of correlator parallel filter channels
N_{COR}	Number of samples correlated - number of times around loop
NDRO	Non- Destructive Read-Out
N_{FIL}	Number of correlator filters required to give final r_{az}
N_{LA}	Number of multilooks in azimuth
NMi	Nautical Miles
N_{OL}	Number of overlapping integrators in prefilter
N_{PRE}	Number of samples summed in prefilter integrator
NR	Noise Region
PCCD	Peristaltic Charge-Coupled Device
PDI	Post-Detection Integration
PDR	Prefilter Data Rate
PPI	Plan Position Indicator
PRF	Radar Pulse Repetition Frequency
Q	Quadrature Signal Component
RAM	Random Access Memory
r_{az}	Final Azimuth Resolution
RC	Number of Range Cells
REG	Register
RG	Range Gate
r_{rg}	Final Range Resolution
R_s	Radar Slant Range
SAR	Synthetic Aperture Radar
S/C	Scan Converter
S/C	Signal to Clutter Ratio
S/D	Serial Differencer
SL	Sidelobe
SPS	Serial-Parallel-Serial
STAE	Second Time Around Echo

STALO	Stable Local Oscillator
STC	Sensitivity-Time Control
TA	Terrain Avoidance
TF	Terrain Follow
T_I	Coherent Integration Time for SAR
T_{PRE}	Prefilter Integration Time
T_S	Time to scan a map of width M subbeams or MW feet
TTL	Transistor-Transistor Logic
TWS	Track While Scan
$V_{a/c}$	or V is aircraft velocity
VLSI	Very Large-Scale Integration
WPS	Words Per Second
α	Radar Real Beam Squint Angle
β_R	Radar Antenna Real Beamwidth
γ	Radar Carrier Wavelength
ψ	Radar Antenna Scan Angle in Ground
θ_{DBS}	Unfocused DBS Angular Resolution at Correlator Output

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SUPPLEMENTARY

INFORMATION

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